Student Name: University Roll No.:	Printed Pages:

School of Engineering
Second Theory Sessional Examination
Odd Semester (AS: 2024-25)

B. Tech: CSE/CSAI [Year: 2nd][Semester: 3rd]

Course Title: Digital Logic Design Course Code: NCS4303	Max Marks: 30 Time: 1*hrs*

Instructions: 1-Mention any assumptions made.
2-Notations have usual meaning.

	SECTION 'A' Q.N.1. Attempt all parts of the following:	Course Objective	Marks
a)	What is difference between Level triggered and edge triggered clock pulse?	CO3	1
b)	When does Race around condition occurs in the output of Flipflop?	CO2	1
c)	Draw the circuit diagram of D flip flop using NAND gate only.	CO3	1
d)	Explain RAM and ROM.	CO2	1
e)	Differentiate between Synchronous and Asynchronous sequential logic circuit.	CO3	1
	SECTION 'B' **Q.N.2. Attempt any two parts of the following:**	**Course Objective**	**Marks**
a)	Draw a PLA circuit to implement the following: $F_1(A, B, C) = A'B + AC' + A'BC'$ $F_2(A, B, C) = AB + AC + BC$	CO2	7.5
b)	Implement the function using multiplexer and draw its logic diagram. $F(A, B, C) = \sum m(0,2,3,5,7)$	CO2	7.5
c)	What is the different type of Shift register? Explain the operation of Serial in and Parallel out SIPO shift Register.	CO3	7.5

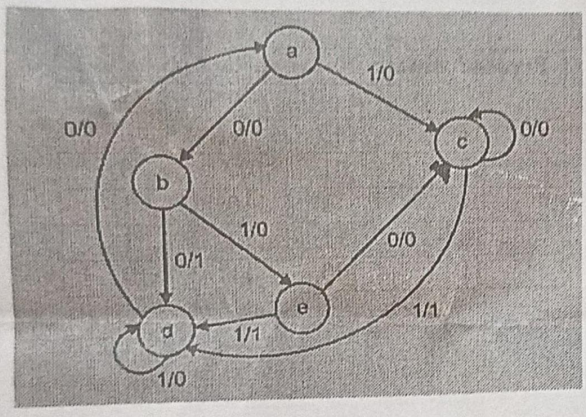
SECTION 'C'		Course Objective	Marks
Q.N.3. Attempt any one parts of the following:			
a)	Explain JK flip flop. Write its characteristic table, excitation table, circuit diagram and characteristic equation.	CO3	10
b)	Obtain the reduced state table and reduced state diagram for the sequential circuit whose state diagram is given below. 	CO3	10
c)	(i) Design a 4x16 decoder using two 3x8 decoders. (ii) Find a circuit that has no static hazards and implement the Boolean function: $F(A,B,C,D) = \sum(0,2,6,7,8,10,12)$	CO2	10

Table 1: Mapping between COs and questions

COs	Questions Numbers	Total Marks
CO2	1(b),1(d),2(a),2(b),3(c)	27
CO3	1(a),1(c),1(e),2(c), 3(a),3(b)	30.5