International Institute of Information Technology, Bangalore

Sizing of a Low Dropout Voltage Regulator (LDO)

Final Project for

Analog CMOS VLSI Design (VL502)

Done By:-

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Submitted to:-
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International Institute of Information Technology - Bangalore

1. Specifications

Instructions: All specifications used in the design.

Table 1: Specifications Summary

Parameter	**Value**
Vin	1.4
Vout	1
PSRR	60
Iload (min)	2m
Iload (max)	10m
Cload	1u
Iquiescent	50u
Transient duration	1

2. Purpose of an LDO

An LDO (Low Dropout Regulator) is a type of linear voltage regulator that provides a stable, low-noise output voltage while operating with a small difference (dropout voltage) between the input and output voltages. Its role in circuits is crucial for ensuring reliability and performance.

Key Purposes of an LDO

- **Voltage Regulation:** Maintains a stable output voltage despite variations in input voltage or load current, ensuring consistent operation of sensitive electronic components.
- **Low Noise Power Supply:** Provides clean, low-ripple power, which is essential for noise-sensitive applications such as RF circuits, audio devices, and ADCs/DACs.
- **Load Current Stability:** Supports a range of load currents while maintaining stability, which is vital in circuits with dynamic power requirements.
- **Protection for Downstream Components:** Safeguards sensitive downstream components from voltage fluctuations and overvoltage conditions.
- **Power Efficiency at Low Dropout:** Operates efficiently when the difference between input and output voltage is minimal, reducing energy loss compared to traditional linear regulators.

3. Relevance of Techplots

We Include all techplots generated after Python postprocessing, there are 5 takeaways, and we share a schematic of how these techplots were obtained.

- **Github Link**: https://github.com/TanayaMehta003/ACMOS$_P ROJECT_1$/$tree/main$
  Technology node : 45 nm
- f_T improves with shorter channel lengths, making circuits faster with scaling.
- Comparison of different FOMs at different lengths

Length (nm)	**gmro**	**Id/w**	**ft (GHz)**
45	8	170	180
90	50	100	65
270	155	50	13

Table 2: Comparison of different FOM at different lengths for NMOS

- In this project we have taken Vds to be 0.4 mV, and we expect that to result in some error because the Vds across every MOSFET might not be the same after sizing the circuit under a particular load. To solve this problem what we can do is generate differnt techplots for different values of Vds such as Vds=0.6v Vds=1v Vds=1.8v
- So using Vds of different volts will take care of change in load currents and the errors can be reduced.
- For this project we are using Vds of only 0.4 V

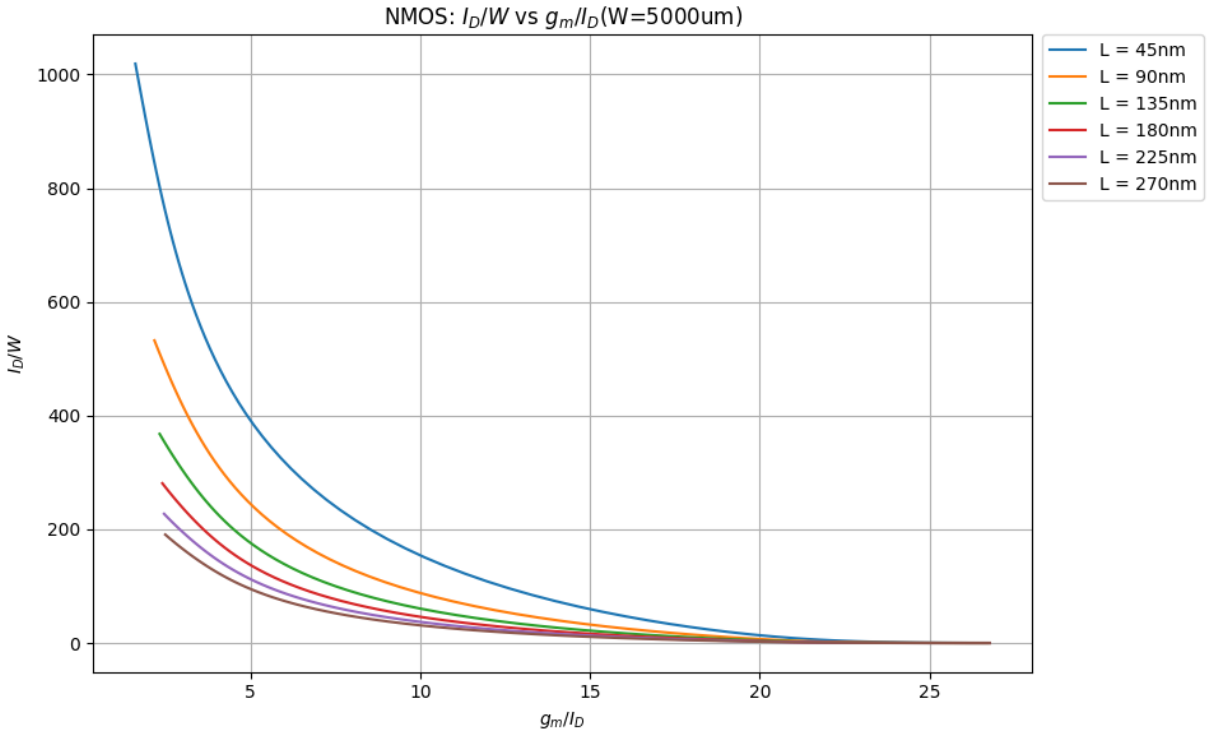

Figure 1: NMOS Techplots after Python postprocessing - Id/W

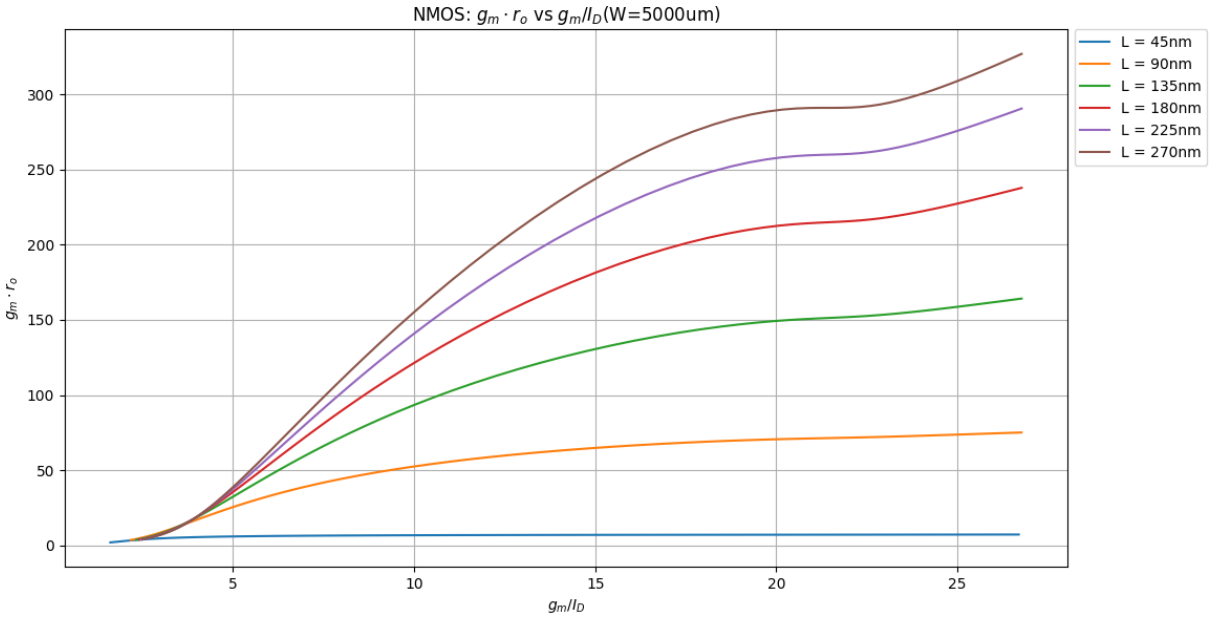

Figure 2: NMOS Techplots after Python postprocessing - gmro

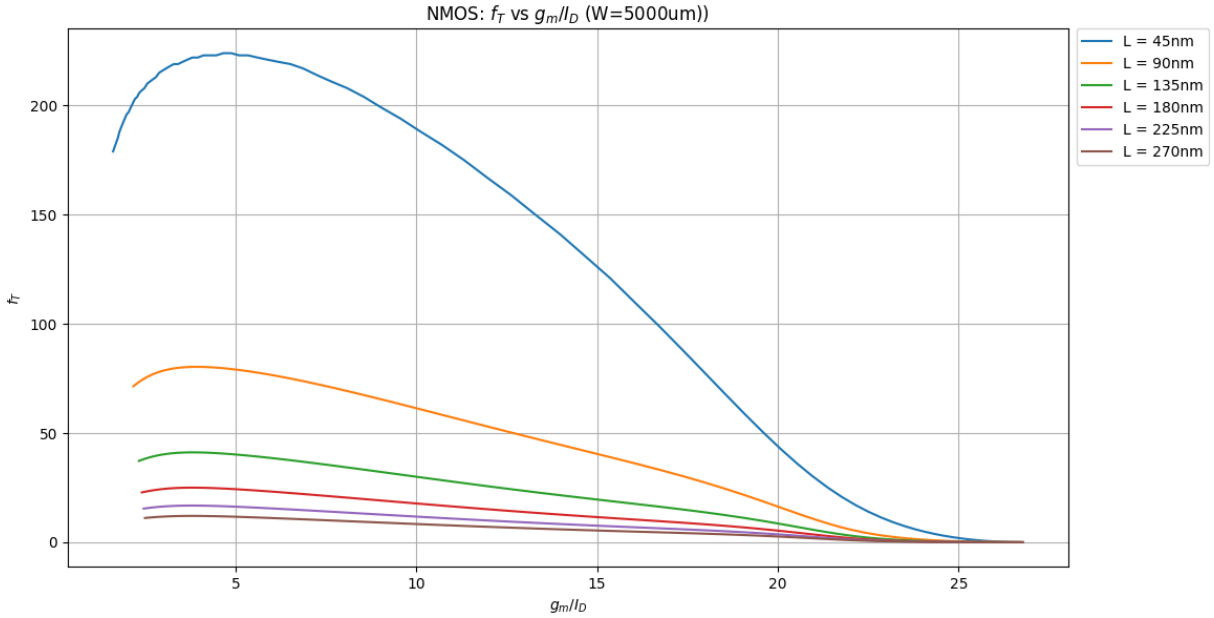

Figure 3: NMOS Techplots after Python postprocessing - fT

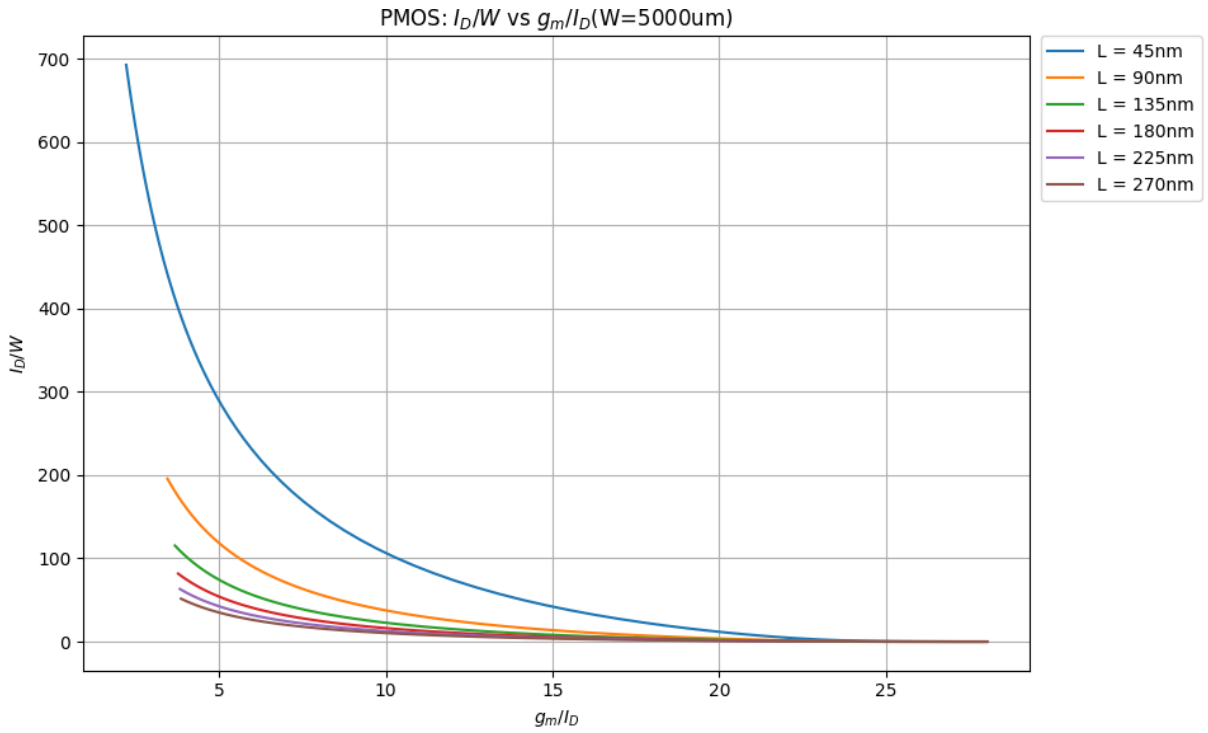

Figure 4: PMOS Techplots after Python postprocessing - Id/W

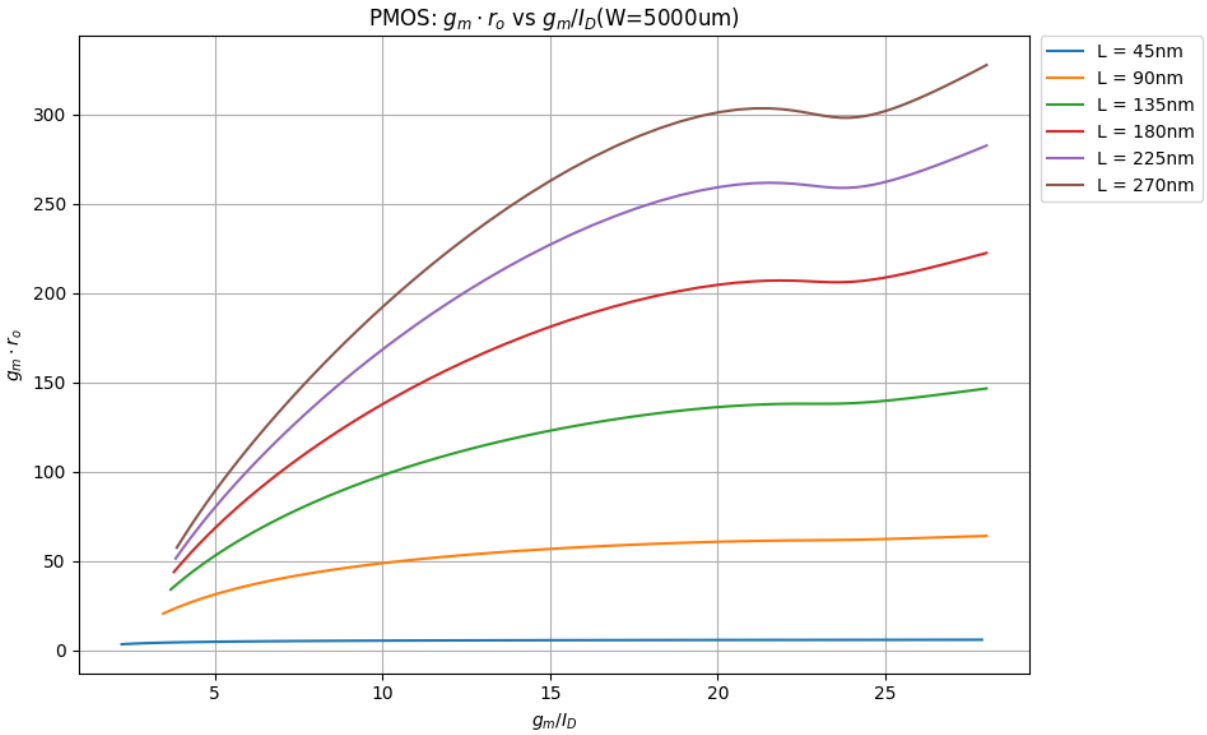

Figure 5: PMOS Techplots after Python postprocessing - gmro

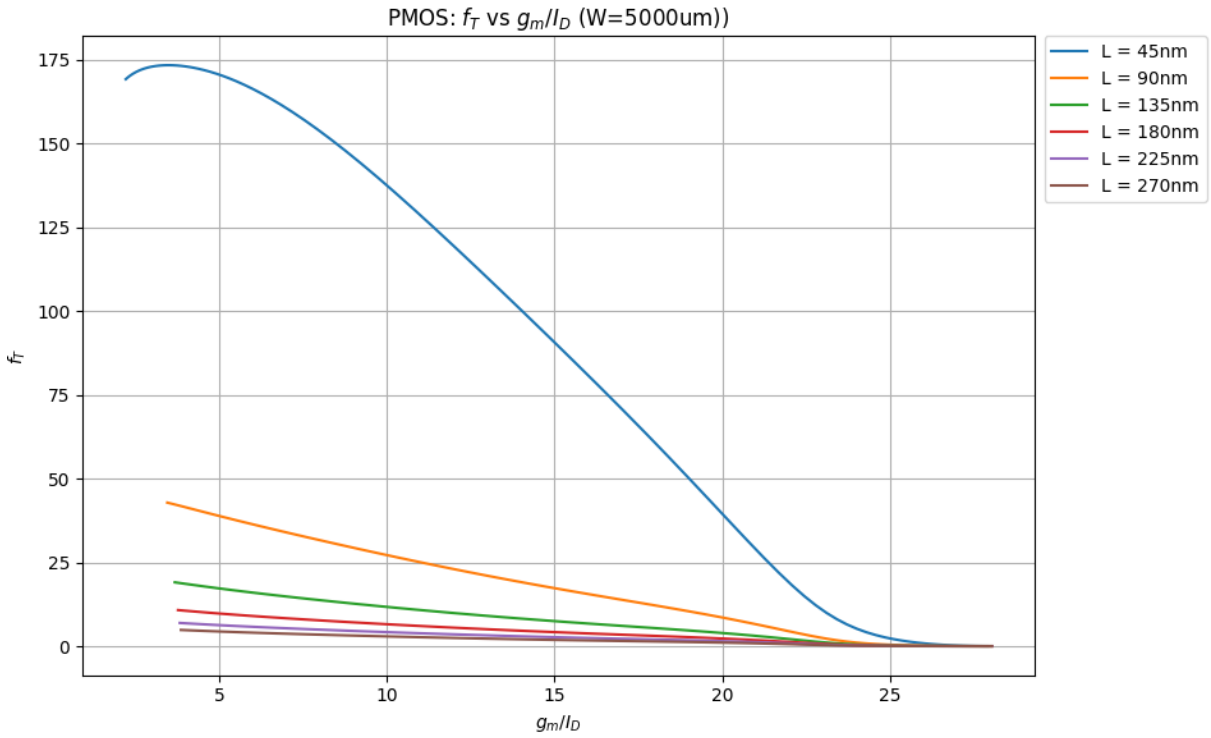

Figure 6: PMOS Techplots after Python postprocessing - fT

Table 3: Key Differences Between 180nm and 45nm Technology Nodes for NMOS

Parameter	**180nm Technology Node**	**45nm Technology Node**
gmro	20	6.721
Id/W (μA/μm)	28	154.324
fT (Hz)	1.6×10^{10}	18.93×10^{10}

Table 4: Observations on Technology Scaling Effects

Parameter	**Observation**
gmro	As the channel length decreases, the output resistance (r_o) decreases significantly, which dominates the intrinsic gain ($gmro$). As a result, the overall value of $gmro$ decreases.
Id/W	With reduced channel length, the drain current (I_d) increases due to higher mobility and lower channel resistance. Consequently, I_d/W increases, which is evident from the data.
fT	A decrease in channel length increases the transconductance (g_m), which directly leads to an increase in the unity-gain cutoff frequency (f_T). This trend is observed in the values.

4. FET Sizes

We Provide the sizes of the passFET, differential amplifier, and mirror transistors. here we also Include small-signal parameters and figures of merit (FOMs). Discuss loop gain under heavy and light load conditions.

Table 5: FET Sizes and Parameters

Transistor	Size (W/L)	g_m/I_d	$g_m * r_o$	I_d/W	f_t
PassFET pmos	285.7u/90n	10	50	37	28 GHz
Diff-Amp pmos	675.67n/90n	10	40	37	28 GHz
Diff-Amp nmos	283n/90n	10	40	88.33	60 GHz
Current Mirror nmos	1080n/10u	-	-	40	10 GHz

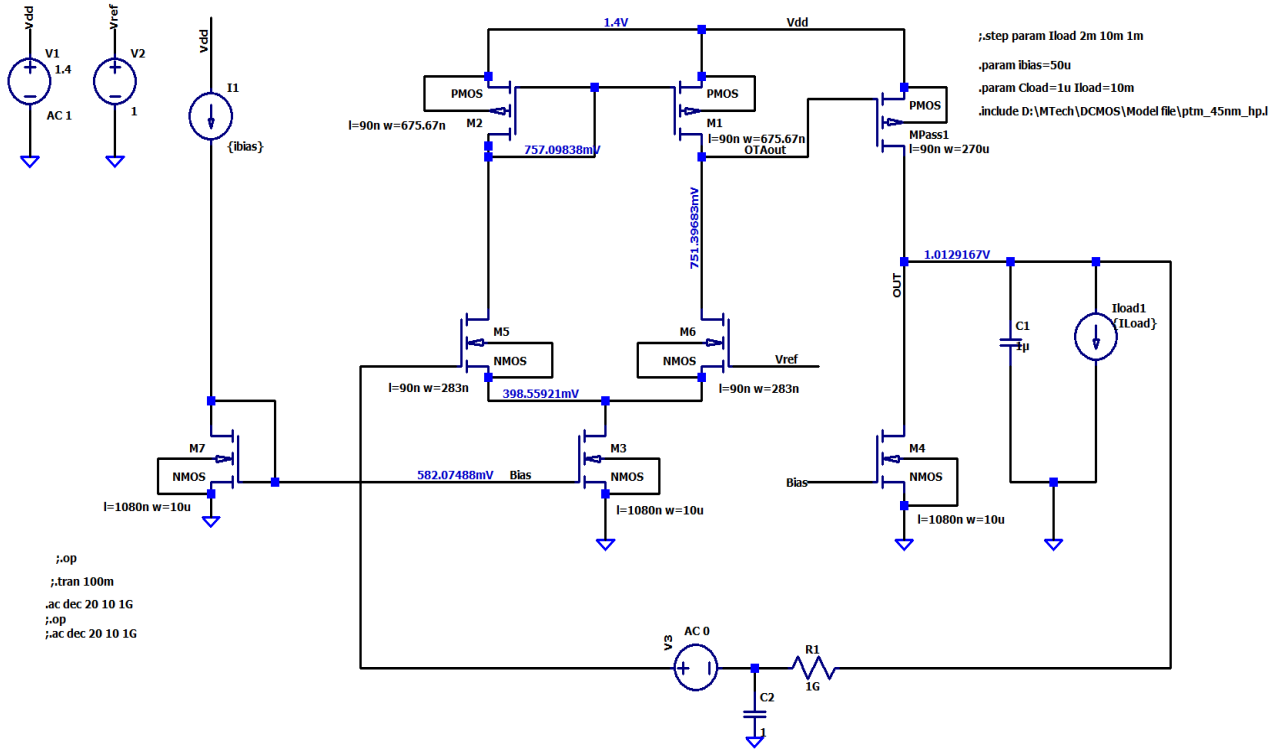

Figure 7: FET sizes and characteristics.

5. Stability Analysis

For Heavy load we get the following curve:

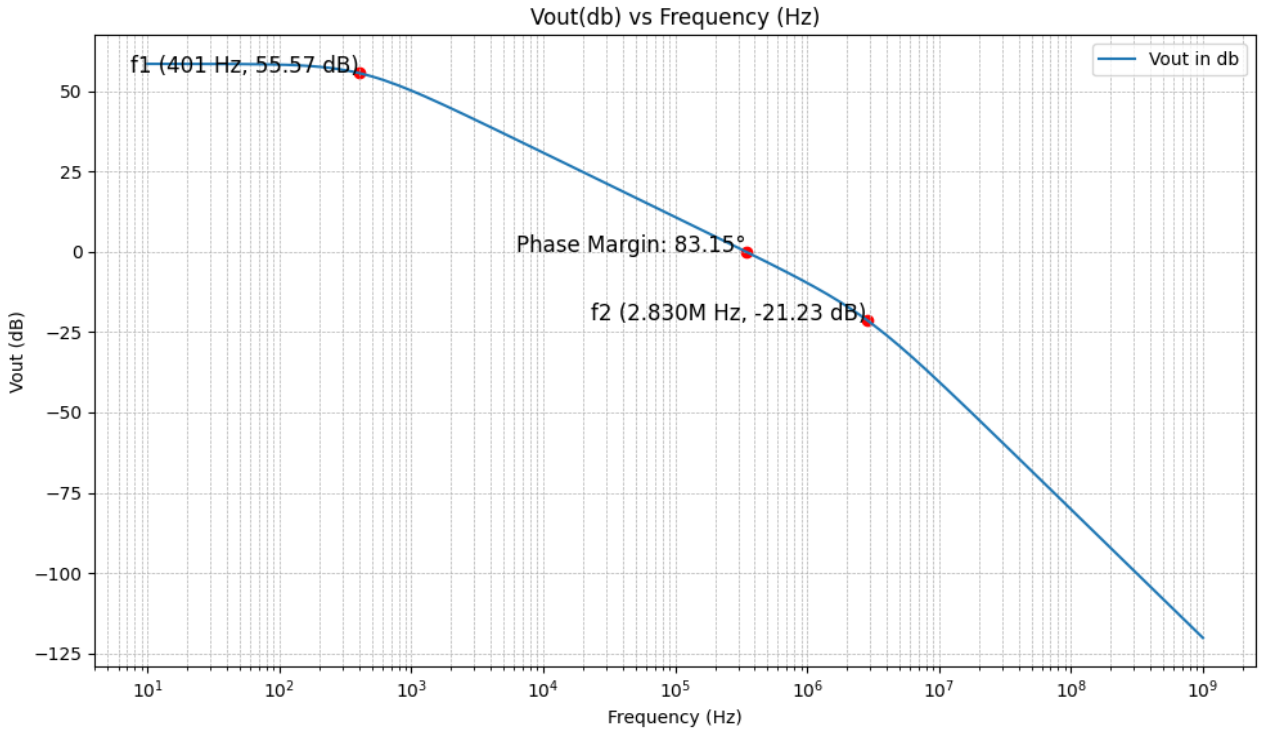

Figure 8: Stability Analysis for I=10 mA

For Light load we get the following curve

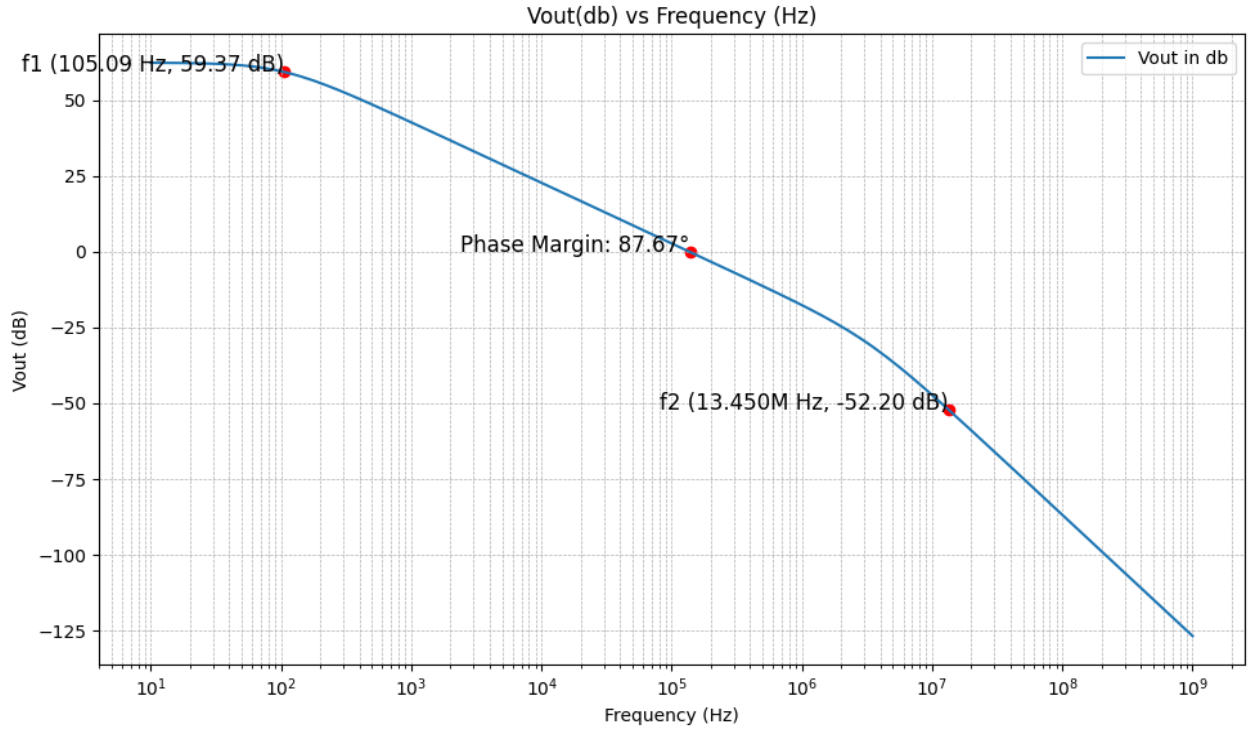

Figure 9: Stability Analysis for I=2 mA

From the above analysis we can see that the unity gain bandwidth is closer to the second pole for the heavy load case than the light load case. From the phase margin also we observe a smaller phase margin of 83.15 degrees for the heavy load case and 87.67 for light load case. From this analysis we can say that when we apply light load we get a more stable system.

Table 6: Key Metrics under Heavy and Light Load Conditions

Parameter	**Heavy Load**	**Light Load**
DC Loop Gain (dB)	58.6	62
Unity Gain Bandwidth (kHz)	401	105.09
Phase Margin (degrees)	83.15	87.67
Pole 1 (Hz)	401.27	105.09
Pole 2 (MHz)	2.83	13.45

6. PSRR Explanation

LDOs are essential components in the power supply of most ICs. They provide a ripple-free, stable fixed output voltage; isolating it from the input noise. An LDO has several important performance specifications and the power supply rejection ratio (PSRR) is one of them. PSRR is a quantitative measure of the attenuation of input ripples by the LDO at it's output. These ripples can originate from various parts of the circuit, like DC/DC converters or shared power supplies of other circuit blocks. PSRR is expressed as $PSRR = 20 * log(V_{out}/V_{in})$, where V_{out} and V_{in} refer to magnitudes of input and output ripples. In Figure 12, the PSRR of LDO is divided into two distinct regions:

- Region 1 covers the low and mid frequency range till the regulator bandwidth frequency (reg), where PSRR primarily depends on the loop gain (LG) of the regulator.
- Region 2 starts after reg, where PSRR is independent of LG and is dominated by output parasitics, PCB impedance, etc.

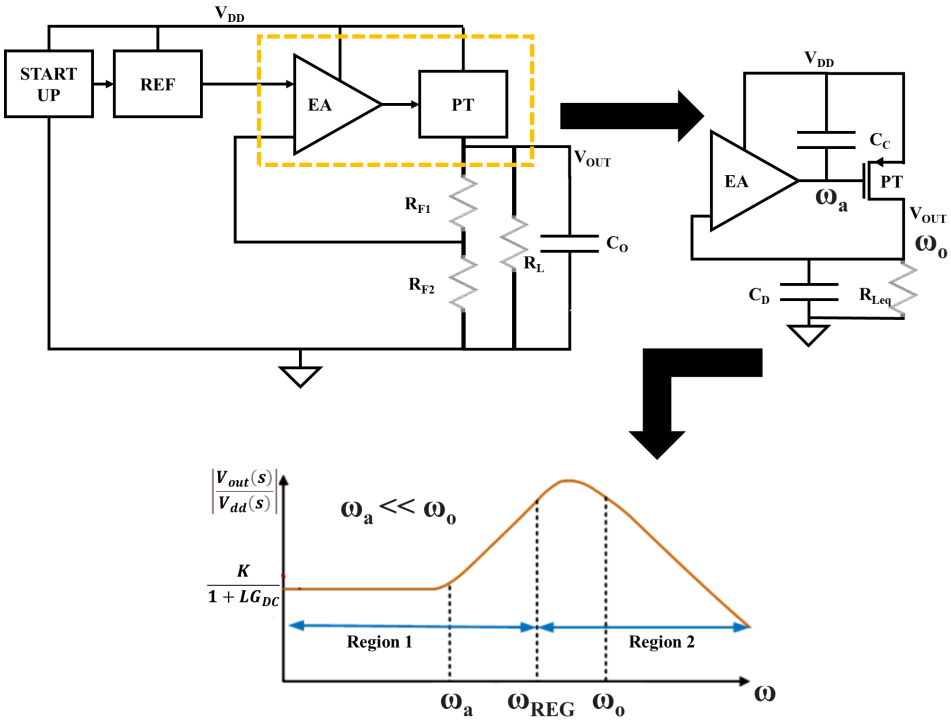

Figure 10: Block diagram of a low drop-out (LDO) regulator and its associated PSRR curve (linear scale)

Externally Compensated LDO

7. PSRR Simulation Results

Heavy Load (10 mA)

Case 1:- Loop Gain Analysis:-

Schematic

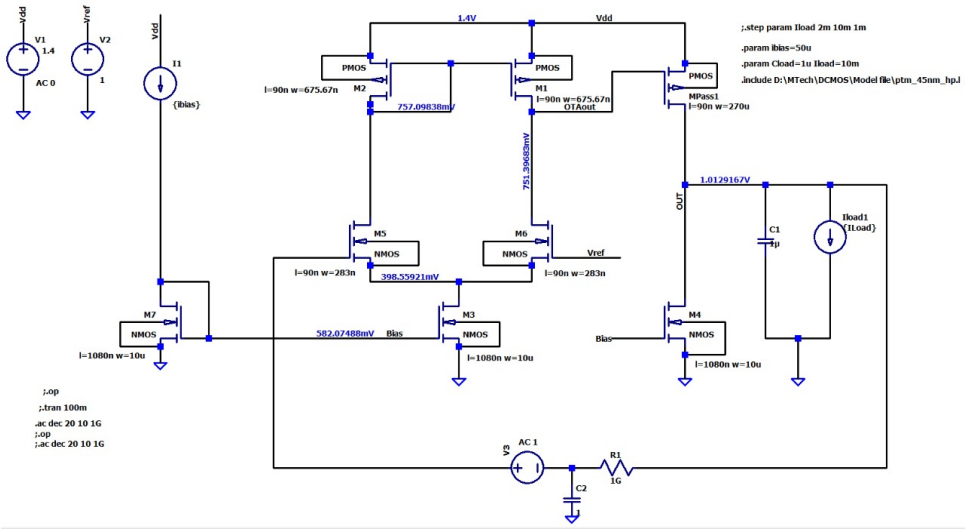

Figure 11: Schematic

Explanation of the artifact:- In order to calculate the loop gain we have given a RC circuit in the feedback loop alongwith a AC source with amplitude 1 (as we want to maintain an AC voltage of 1V) at the output. At the same time we also need to bias the circuit and provide a dc voltage to the gate of the nmos in the differential amplifier and for this we are giving the RC circuit which will prevent the flow of dc current to ground but will send any AC signal at the output to ground at high frequency. Also the drop across the resistor will be very less as we have given a very high resistance with very negligible current (since current going into the gate of the mosfet is zero). Thus we will bias the circuit and also calculate the loop gain.

Output Log File:-

SPICE Output Log: D:\MTech\ACMOS\Project\TusharOLckt2.log

```
LTspice 24.0.12 for Windows
Circuit: * D:\MTech\ACMOS\Project\TusharOLckt2.asc
Start Time: Mon Dec  2 16:30:27 2024
solver = Normal
Maximum thread count: 8
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                         --- BSIM4 MOSFETS ---
Name:     mpass1        m1            m2            m3          m4
Model:     pmos         pmos          pmos          nmos        nmos
Id:     -1.01e-02   -2.48e-05   -2.48e-05    4.97e-05    5.06e-05
Vgs:    -6.49e-01   -6.43e-01   -6.43e-01    5.82e-01    5.82e-01
Vds:    -3.87e-01   -6.49e-01   -6.43e-01    3.99e-01    1.01e+00
Vbs:     0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Vth:    -4.87e-01   -4.84e-01   -4.84e-01    4.69e-01    4.69e-01
Vdsat:  -1.77e-01   -1.75e-01   -1.75e-01    1.38e-01    1.38e-01
Gm:      9.95e-02    2.50e-04    2.49e-04    6.06e-04    6.16e-04
Gds:     2.52e-03    5.00e-06    5.01e-06    1.93e-06    1.30e-06
Gmb      2.11e-02    5.28e-05    5.28e-05    1.40e-04    1.42e-04
Cbd:     1.21e-13    2.86e-16    2.87e-16    4.48e-15    3.97e-15
Cbs:     2.16e-13    5.41e-16    5.41e-16    8.00e-15    8.00e-15

Name:       m5          m6          m7
Model:     nmos        nmos        nmos
Id:     2.48e-05    2.49e-05    5.00e-05
Vgs:    6.01e-01    6.01e-01    5.82e-01
Vds:    3.59e-01    3.53e-01    5.82e-01
Vbs:    0.00e+00    0.00e+00    0.00e+00
Vth:    4.66e-01    4.66e-01    4.69e-01
Vdsat:  1.43e-01    1.43e-01    1.38e-01
Gm:     2.44e-04    2.44e-04    6.10e-04
Gds:    5.07e-06    5.16e-06    1.48e-06
Gmb     5.62e-05    5.63e-05    1.41e-04
Cbd:    1.28e-16    1.28e-16    4.30e-15
Cbs:    2.26e-16    2.26e-16    8.00e-15


Total elapsed time: 0.100 seconds.
```

Figure 12: Log File

From the above file we can verify that all the devices are in saturation as follows:
Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Table 7: All MOSFETs in saturation

Device Name	Device Type	$\|V_{ds}\|$	$\|V_{gs}\|$	$\|V_t\|$	$\|V_{gs}\| - \|V_t\|$	Reason for saturation
MPass1	PMOS	0.38	0.649	0.48	0.16	$V_{sd} > 0.16$
M1	PMOS	0.64	0.643	0.48	0.163	$V_{sd} > 0.163$
M2	PMOS	0.643	0.643	0.48	0.163	$V_{sd} > 0.163$
M5	NMOS	0.359	0.601	0.468	0.133	$V_{ds} > 0.133$
M6	NMOS	0.353	0.601	0.468	0.133	$V_{ds} > 0.133$
M3	NMOS	0.399	0.582	0.468	0.114	$V_{ds} > 0.114$
M7	NMOS	0.582	0.582	0.468	0.114	$V_{ds} > 0.114$
M4	NMOS	1.01	0.582	0.468	0.114	$V_{ds} > 0.114$

Output Waveform

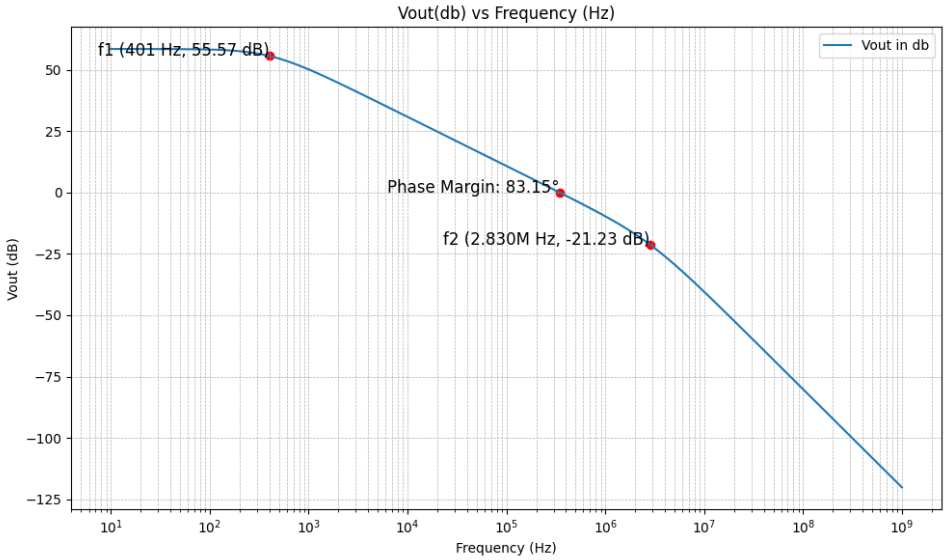

Figure 13: Output Waveform Vout

The phase margin is **83.15**. The output voltage (Loop Gain) comes out to be close to **58.6 dB** . The formula for loop gain is $A_{diff} * A_{pass}$ where:

- A_{diff} is differential amplifier gain
- A_{pass} is the passfet gain

Case 2:- Open Loop PSRR Calculation

Schematic

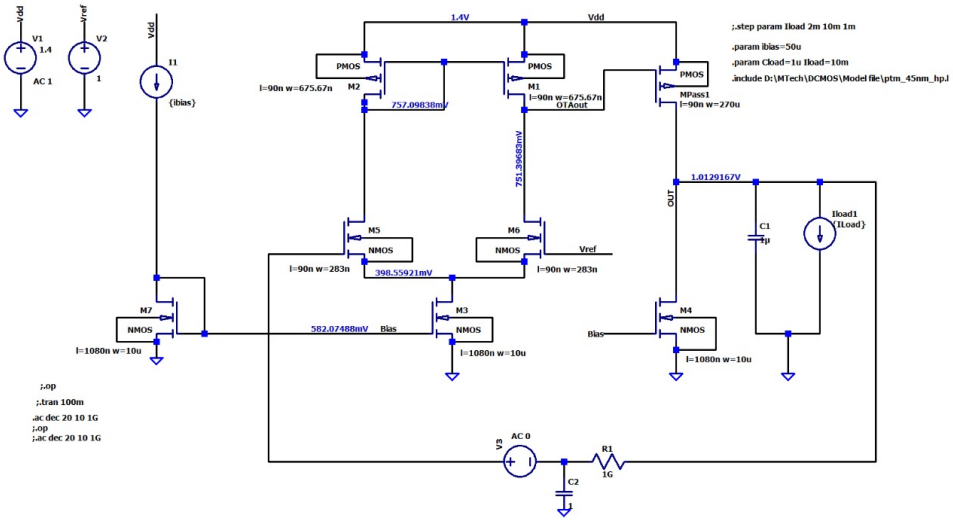

Figure 14: Schematic

Explanation of the artifact used:- In order to calculate the open loop PSRR we need to send an AC signal from the source which in our case is VDD. Here we are giving an AC 1 signal in the source. This signal is given to the source of the passfet and the source of pmos in the diffamp. We will ideally want very bad PSRR in the diffamp as we want the OTA output to have all the AC noise such that Vsg of pmos = 0 (small signal analysis). Thus all the noise will get rejected and we will get a noise free dc voltage at the output of the LDO. Here in order to calculate the open loop PSRR we have a RC circuit to bias the differential amplifier. You can see AC 0 in the circuit indicating that there is an open loop in the circuit . From here we have calculated the open loop PSRR in the circuit. Since there is no feedback in the circuit we can thus say that there will be noise at the output and thus the rejection will be very poor.

Note:- Always observe the Vota output should be closer to 1v, the better it is for PSRR at the output as the Vsg value will be close to 0.

Output Waveforms:

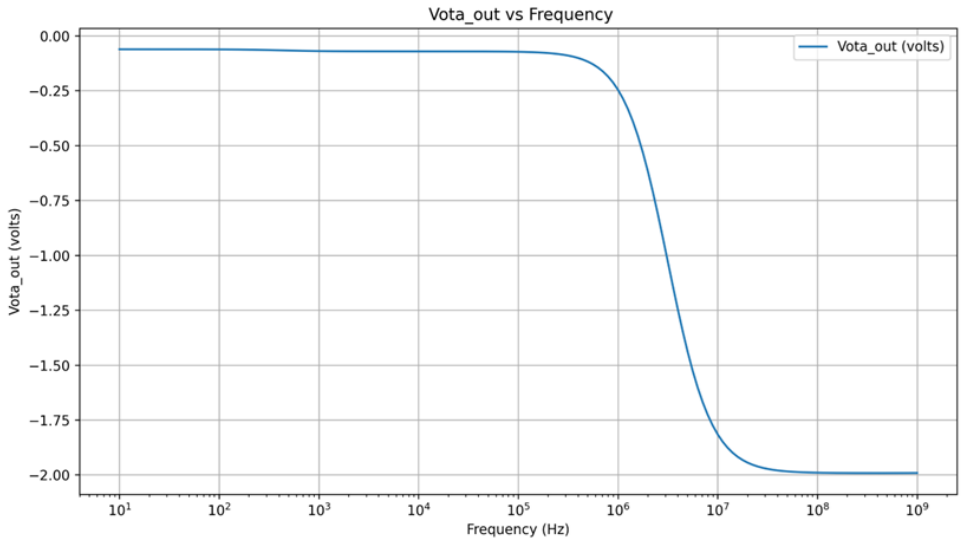

Figure 15: Output Waveform Vota

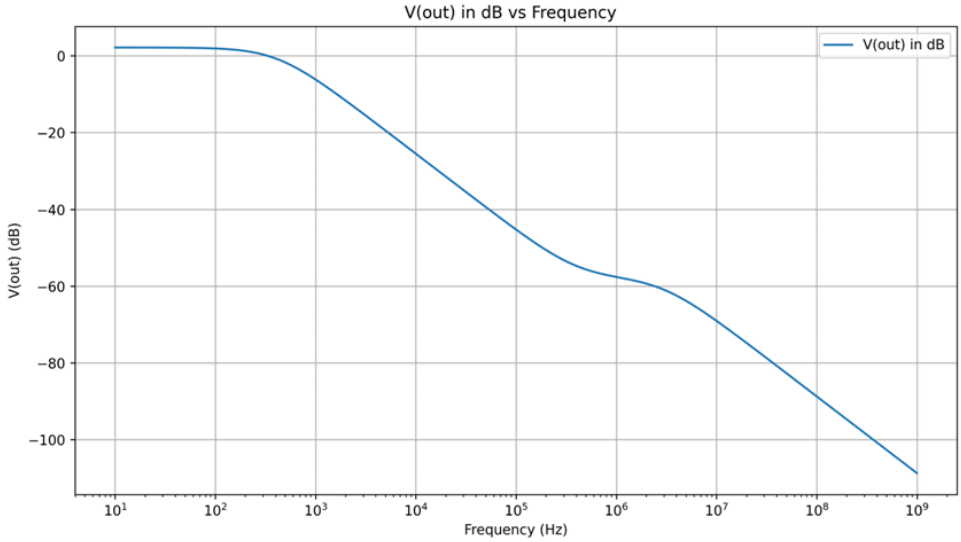

Figure 16: Output Waveform Vout

Case 3:- Closed Loop PSRR Calculation

Schematic

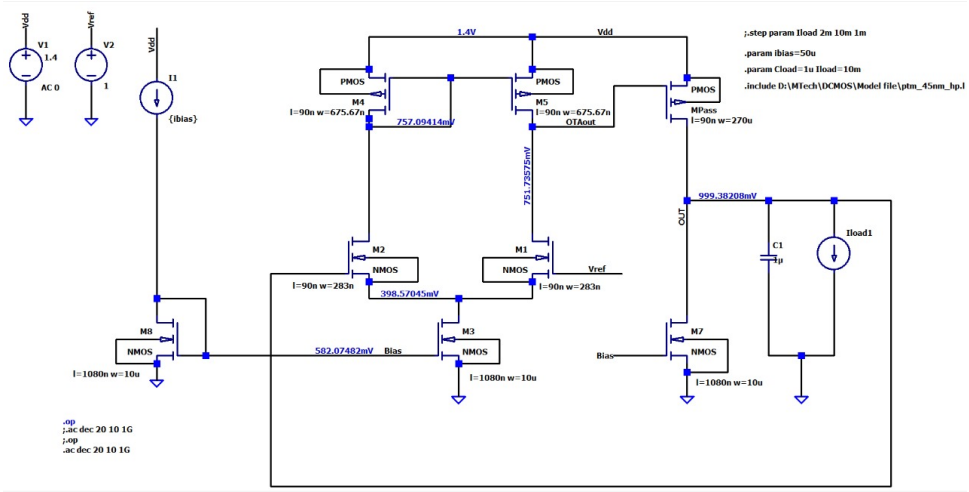

Figure 17: Schematic

Explanation of the artifact used:- In this case we can see that we have given a AC source in the voltage source VDD. We want to see the negative feedback in the circuit due to which we will get the output voltage cancelled out (small signal analysis). Here we should observe a high PSRR according to our specifications (60 dB) which tells us that our sizing is perfect. For this circuit we have given a feedback from the output terminal to the input of the diffamp which indicates the feedback path.

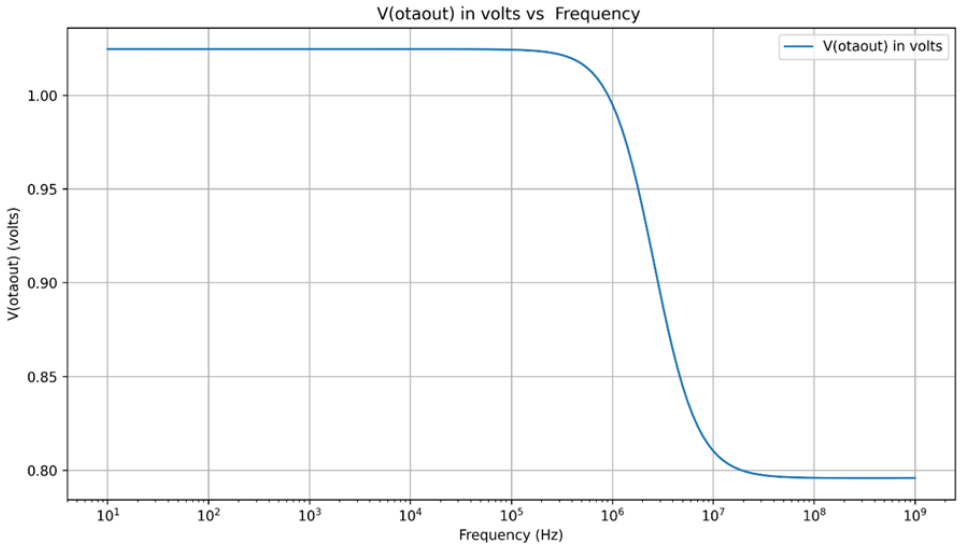

Figure 18: Output Waveform Vota

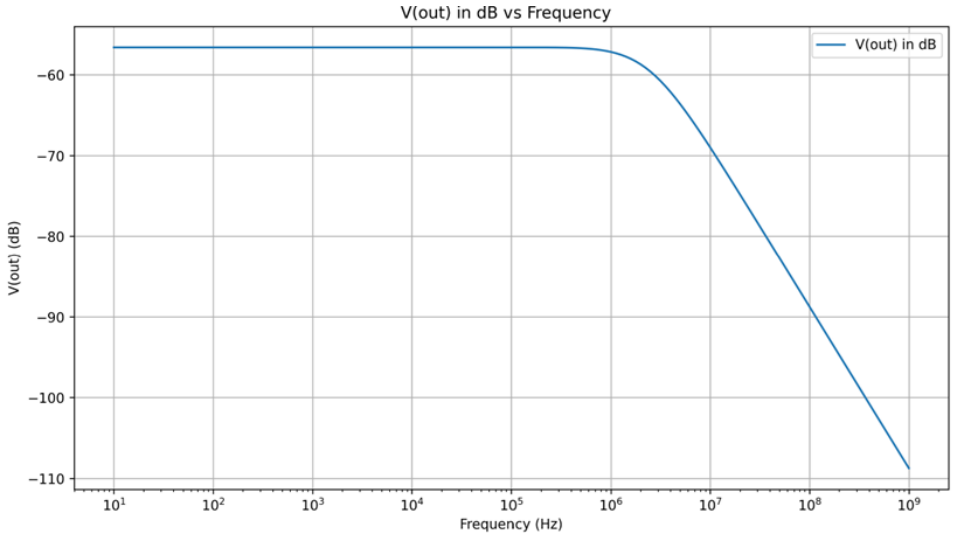

Figure 19: Output Waveform Vout

Light Load (2 mA)

Case 1:- Loop Gain Analysis

Schematic

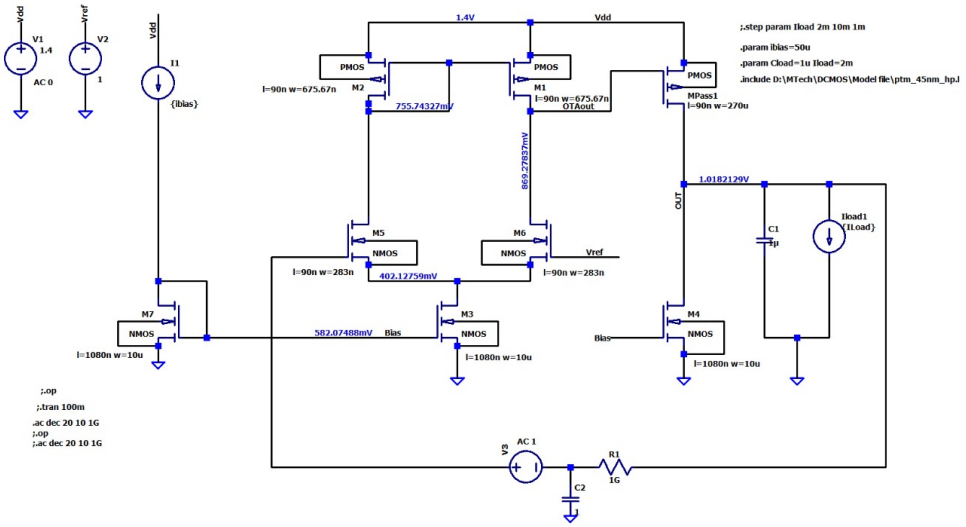

Figure 20: Schematic

Output Log File:-

SPICE Output Log: D:\MTech\ACMOS\Project\TusharOLckt2.log

```
LTspice 24.0.12 for Windows
Circuit: * D:\MTech\ACMOS\Project\TusharOLckt2.asc
Start Time: Sat Dec  7 19:43:32 2024
solver = Normal
Maximum thread count: 8
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                         --- BSIM4 MOSFETS ---
Name:     mpass1         m1           m2           m3           m4
Model:     pmos          pmos         pmos         nmos         nmos
Id:      -2.05e-03    -2.45e-05    -2.51e-05     4.97e-05     5.06e-05
Vgs:     -5.31e-01    -6.44e-01    -6.44e-01     5.82e-01     5.82e-01
Vds:     -3.82e-01    -5.31e-01    -6.44e-01     4.02e-01     1.02e+00
Vbs:      0.00e+00     0.00e+00     0.00e+00     0.00e+00     0.00e+00
Vth:     -4.87e-01    -4.85e-01    -4.84e-01     4.69e-01     4.69e-01
Vdsat:   -9.46e-02    -1.75e-01    -1.76e-01     1.38e-01     1.38e-01
Gm:       3.59e-02     2.47e-04     2.51e-04     6.06e-04     6.16e-04
Gds:      6.60e-04     5.24e-06     5.05e-06     1.91e-06     1.30e-06
Gmb       7.41e-03     5.22e-05     5.32e-05     1.40e-04     1.42e-04
Cbd:      1.21e-13     2.94e-16     2.87e-16     4.47e-15     3.97e-15
Cbs:      2.16e-13     5.41e-16     5.41e-16     8.00e-15     8.00e-15

Name:       m5           m6           m7
Model:     nmos         nmos         nmos
Id:       2.51e-05     2.46e-05     5.00e-05
Vgs:      6.02e-01     5.98e-01     5.82e-01
Vds:      3.54e-01     4.67e-01     5.82e-01
Vbs:      0.00e+00     0.00e+00     0.00e+00
Vth:      4.66e-01     4.65e-01     4.69e-01
Vdsat:    1.44e-01     1.42e-01     1.38e-01
Gm:       2.45e-04     2.44e-04     6.10e-04
Gds:      5.19e-06     4.33e-06     1.48e-06
Gmb       5.66e-05     5.63e-05     1.41e-04
Cbd:      1.28e-16     1.25e-16     4.30e-15
Cbs:      2.26e-16     2.26e-16     8.00e-15


Total elapsed time: 0.093 seconds.
```

Figure 21: Log File

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Table 8: All MOSFETs in Saturation

Device Name	**Device Type**	$\|V_{ds}\|$	$\|V_{gs}\|$	$\|V_t\|$	$\|V_{gs}\| - \|V_t\|$	**Reason for Saturation**
MPass1	PMOS	0.382	0.531	0.487	0.044	$V_{sd} > 0.044$
M1	PMOS	0.531	0.644	0.485	0.159	$V_{sd} > 0.159$
M2	PMOS	0.644	0.644	0.484	0.160	$V_{sd} > 0.160$
M5	NMOS	0.354	0.602	0.466	0.136	$V_{ds} > 0.136$
M6	NMOS	0.467	0.598	0.465	0.133	$V_{ds} > 0.133$
M3	NMOS	0.402	0.582	0.469	0.113	$V_{ds} > 0.113$
M7	NMOS	0.582	0.582	0.469	0.113	$V_{ds} > 0.113$
M4	NMOS	1.020	0.582	0.469	0.113	$V_{ds} > 0.113$

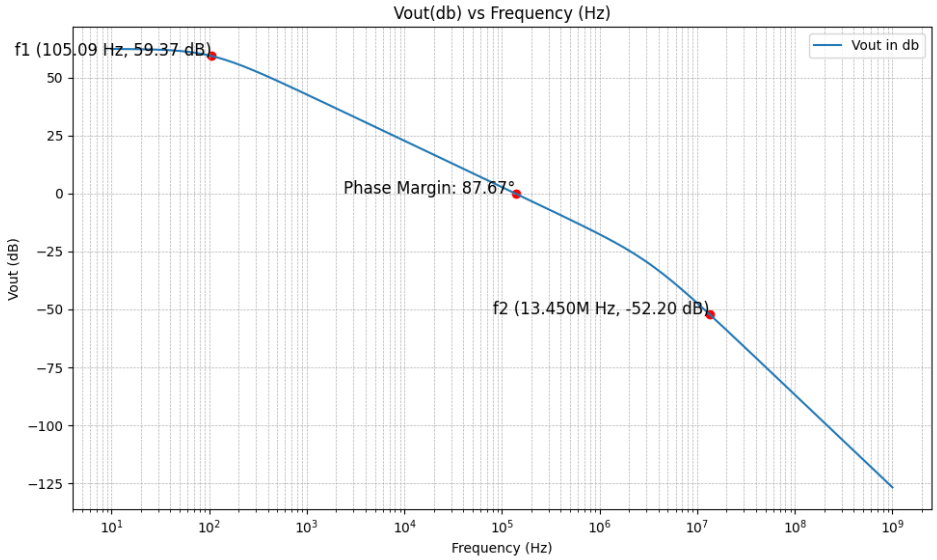

Figure 22: Output Waveform Vout

The phase margin obtained is 87.58 degrees. This value is more than that of the value obtained for heavy load. Proving the point that for light load we get a better phase margin as the 1st pole and the 2nd pole are far apart.

Case 2:- Open Loop PSRR Calculation

Schematic

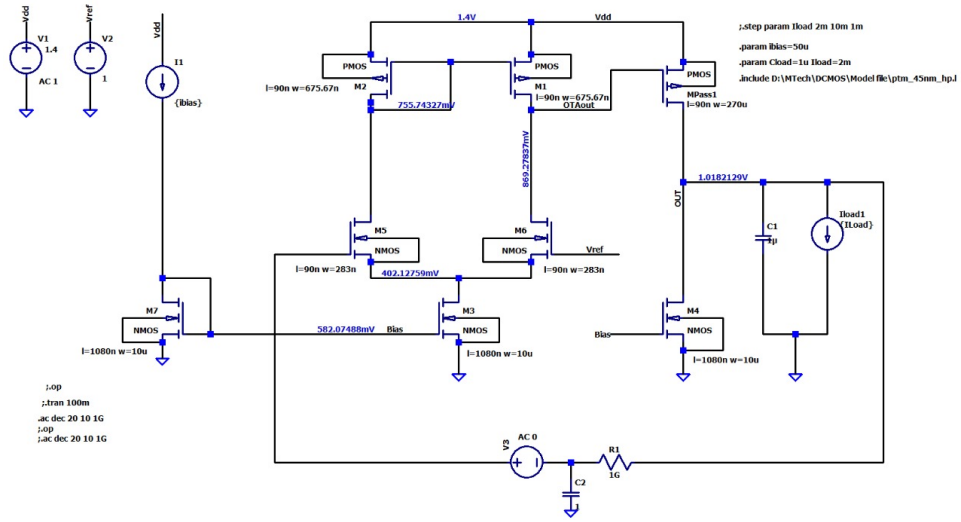

Figure 23: Schematic

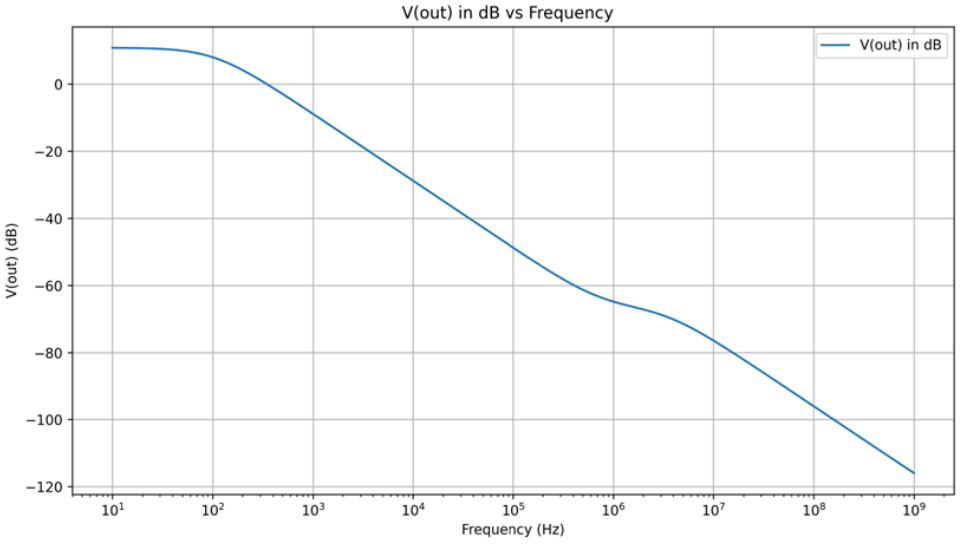

Figure 24: Output Waveform Vout

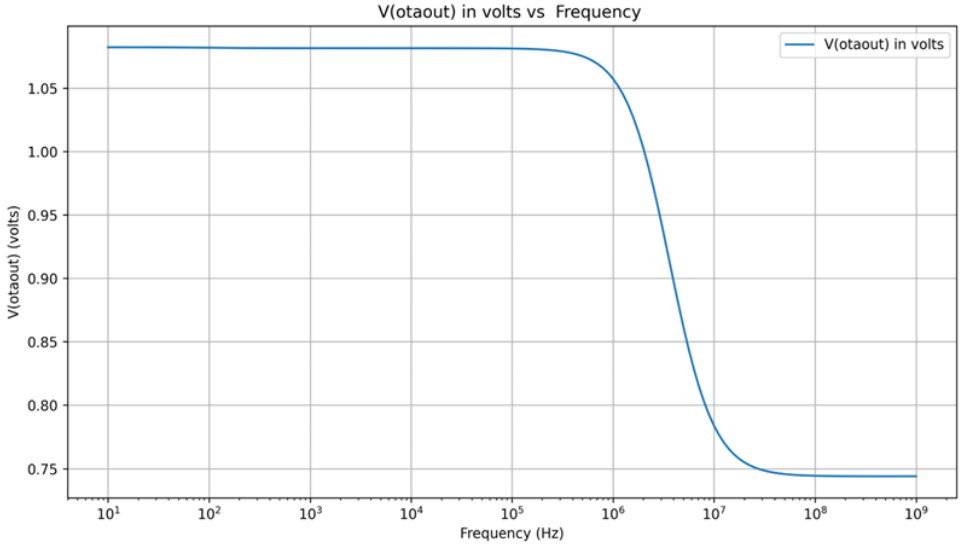

Figure 25: Output Waveform Vota

Case 3:- Closed Loop PSRR Calculation

Schematic:

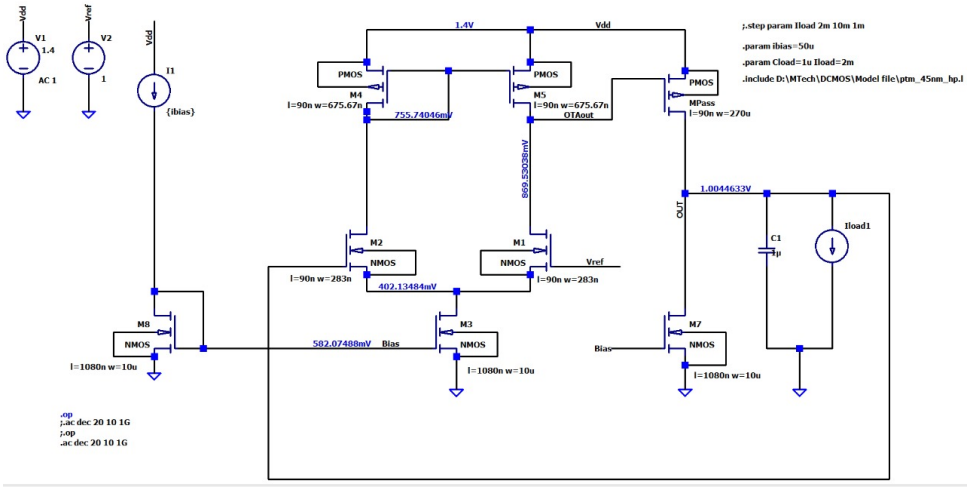

Figure 26: Schematic

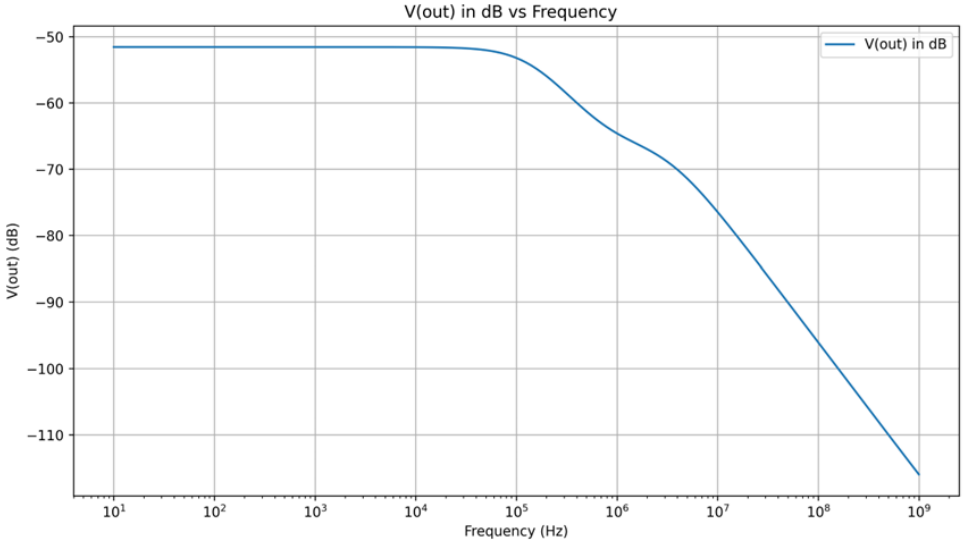

Figure 27: Output Waveform Vout

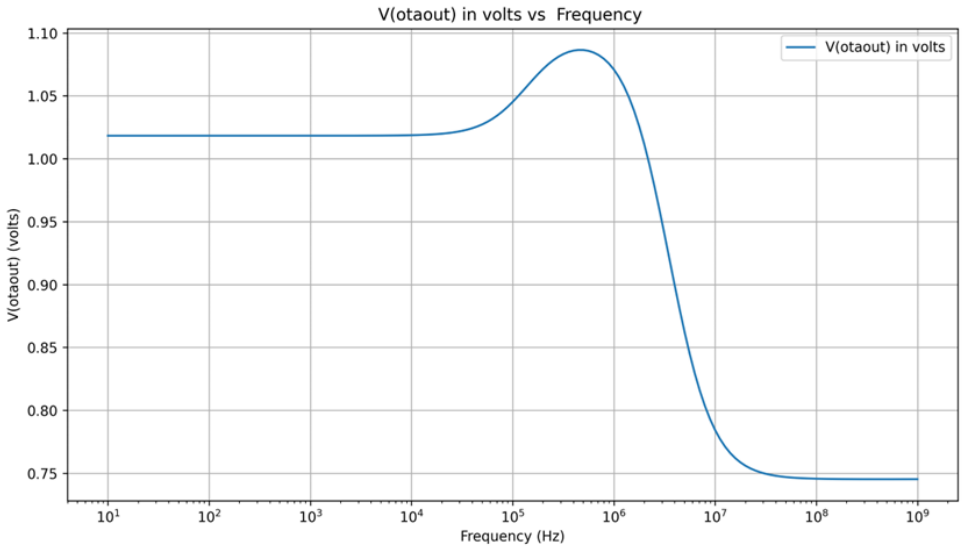

Figure 28: Output Waveform Vota

8. Transient Simulation Results

We have given a pulse at the load with a rise time and fall time of 1u. Also the period of the pulse is 10m with a 50% duty cycle. From the below figure we can understand that the output is able to settle within the specified range of time. We are not able to observe any overshoot or undershoot in the output.

Transient Analysis

Schematic

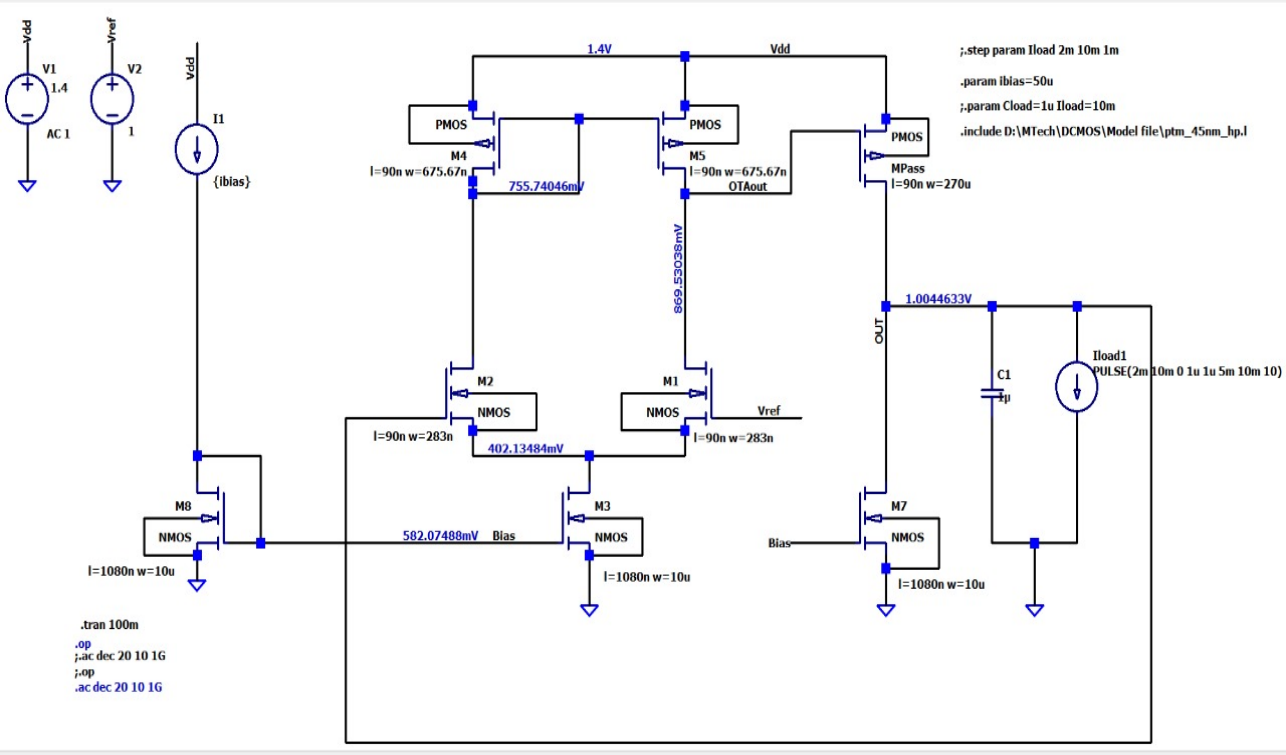

Figure 29: Schematic

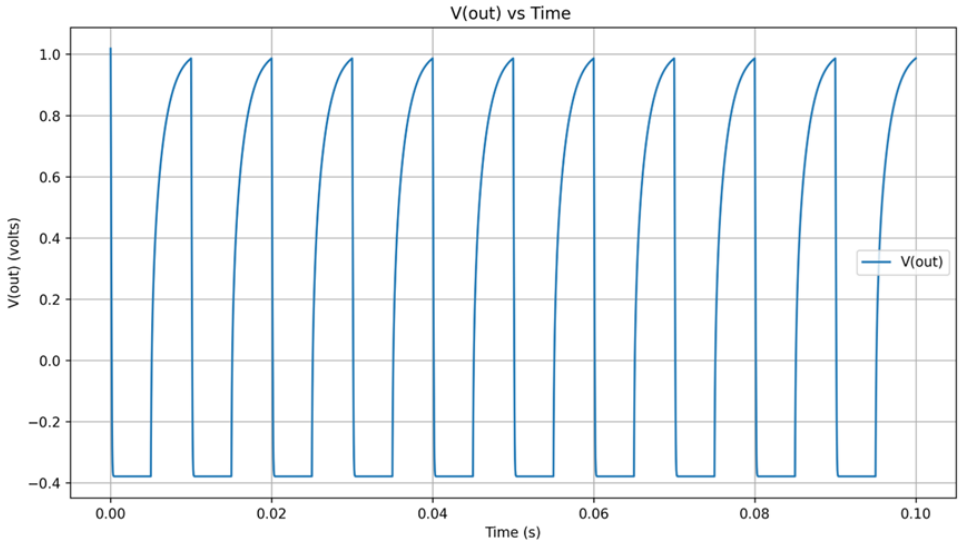

Figure 30: $V_{out} versus time$

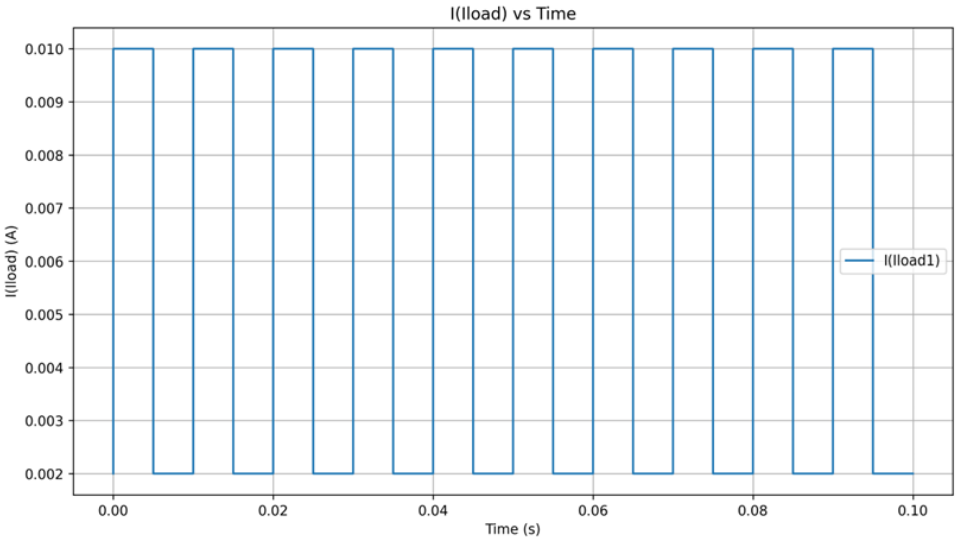

Figure 31: $I_{load} versus time$

9. Simulation vs. Hand Calculations

For Heavy Load of Passfet

Hand Calculations:

- $r_o = 500\,\Omega$
- $g_m = 0.1\,\text{A/V}$
- W_{p1} (First Pole Location) = 2k
- $g_m r_o = 50$
- $C_L = 1u$
- $C_{gg} = 0.568p$

Simulation Results from SPICE Error Log:

- $r_o = 1/g_{ds} = 396.82\,\Omega$
- $g_m = 0.0995\,\text{A/V}$
- W_{p1} (first pole location) = 2.52k
- $g_m r_o = 39.48$

Table 9: Hand Calculation vs Simulation Results

Parameter	Hand Calculation	Simulation Result	% Difference
r_o (ohm)	500.00	396.82	20.63%
g_m (A/V)	0.1	0.0995	0.5%
$g_m * r_o$	50	39.48	21.04%
W_{p1} (Hz)	2k	2.52k	20.63%
W_{p2} (Hz)	22.007M	17.82M	19.02%
W_{ugb} (Hz)	2M	2.52M	20.63%
r_{odiff} (ohm)	80k	99.304k	19.43%
g_{mdiff} (A/V)	250u	250u	0%

Name	mpass	m1	m2	m3	m4	m5	m6	m7
Model	pmos	pmos	pmos	nmos	nmos	nmos	nmos	nmos
Id	-1.01E-02	-2.48E-05	-2.48E-05	4.97E-05	5.06E-05	2.48E-05	2.49E-05	5.00E-05
Vgs	-6.49E-01	-6.43E-01	-6.43E-01	5.82E-01	5.82E-01	6.01E-01	6.01E-01	5.82E-01
Vds	-3.87E-01	-6.49E-01	-6.43E-01	3.99E-01	1.01E+00	3.59E-01	3.53E-01	5.82E-01
Vbs	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Vth	-4.87E-01	-4.84E-01	-4.84E-01	4.69E-01	4.69E-01	4.66E-01	4.66E-01	4.69E-01
Vdsat	-1.77E-01	-1.75E-01	-1.75E-01	1.38E-01	1.38E-01	1.43E-01	1.43E-01	1.38E-01
Gm	9.95E-02	2.50E-04	2.49E-04	6.06E-04	6.16E-04	2.44E-04	2.44E-04	6.10E-04
Gds	2.52E-03	5.00E-06	5.01E-06	1.93E-06	1.30E-06	5.07E-06	5.16E-06	1.48E-06
Gmb	2.11E-02	5.28E-05	5.28E-05	1.40E-04	1.42E-04	5.62E-05	5.63E-05	1.41E-04
Cbd	1.21E-13	2.86E-16	2.87E-16	4.48E-15	3.97E-15	1.28E-16	1.28E-16	4.30E-15
Cbs	2.16E-13	5.41E-16	5.41E-16	8.00E-15	8.00E-15	2.26E-16	2.26E-16	8.00E-15
rds	3.97E+02	2.00E+05	2.00E+05	5.18E+05	7.69E+05	1.97E+05	1.94E+05	6.76E+05
gm*rds	3.95E+01	5.00E+01	4.97E+01	3.14E+02	4.74E+02	4.81E+01	4.73E+01	4.12E+02

Table 10: Transistor Parameters

For Light Load of Passfet

Hand Calculation

- $r_o = 2500\,\Omega$
- $g_m = 0.02\,\text{A/V}$
- W_{p1} (first pole location) = 400
- $g_m r_o = 50$
- $C_L = 1u$
- $C_{gg} = 0.1136p$

Simulation Results from SPICE Error Log:

- $r_o = 1/g_{ds} = 1515.15\,\Omega$
- $g_m = 0.0359\,\text{A/V}$
- W_{p1} (first pole location) = 660
- $g_m r_o = 54.39$

Table 11: Hand Calculation vs Simulation Results

Parameter	**Hand Calculation**	**Simulation Result**	**% Difference**
r_o (ohm)	2500.00	1515.15	39.39%
g_m (A/V)	0.02	0.0359	44.28%
$g_m * r_o$	50	54.39	8%
W_{p1} (Hz)	400	660	39.3%
W_{p2} (Hz)	109.93M	84.5M	23.1%
W_{ugb} (Hz)	400k	660k	39.3%
r_{odiff} (ohm)	80k	104.04k	23.1%
g_{mdiff} (A/V)	250u	247u	1.2%

Parameter	**mpass**	**m1**	**m2**	**m3**	**m4**	**m5**	**m6**	**m7**
Id	-2.05E-03	-2.45E-05	-2.51E-05	4.97E-05	5.06E-05	2.51E-05	2.46E-05	5.00E-05
Vgs	-5.31E-01	-6.44E-01	-6.44E-01	5.82E-01	5.82E-01	6.02E-01	5.98E-01	5.82E-01
Vds	-3.82E-01	-5.31E-01	-6.44E-01	4.02E-01	1.02E+00	3.54E-01	4.67E-01	5.82E-01
Vbs	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Vth	-4.87E-01	-4.85E-01	-4.84E-01	4.69E-01	4.69E-01	4.66E-01	4.65E-01	4.69E-01
Vdsat	-9.46E-02	-1.75E-01	-1.76E-01	1.38E-01	1.38E-01	1.44E-01	1.42E-01	1.38E-01
Gm	3.59E-02	2.47E-04	2.51E-04	6.06E-04	6.16E-04	2.45E-04	2.44E-04	6.10E-04
Gds	6.60E-04	5.24E-06	5.05E-06	1.91E-06	1.30E-06	5.19E-06	4.33E-06	1.48E-06
Gmb	7.41E-03	5.22E-05	5.32E-05	1.40E-04	1.42E-04	5.66E-05	5.63E-05	1.41E-04
Cbd	1.21E-13	2.94E-16	2.87E-16	4.47E-15	3.97E-15	1.28E-16	1.25E-16	4.30E-15
Cbs	2.16E-13	5.41E-16	5.41E-16	8.00E-15	8.00E-15	2.26E-16	2.26E-16	8.00E-15
ro	1.52E+03	1.91E+05	1.98E+05	5.24E+05	7.69E+05	1.93E+05	2.31E+05	6.76E+05
gm*rds	5.44E+01	4.71E+01	4.97E+01	3.17E+02	4.74E+02	4.72E+01	5.64E+01	4.12E+02

Table 12: Transistor Parameters

Internally Compensated LDO

10. FET Sizes

We Provide the sizes of the passFET, differential amplifier, and mirror transistors. here we also Include small-signal parameters and figures of merit (FOMs). Discuss loop gain under heavy and light load conditions.

The value of the capacitance for the internal capacitor is 24.96 pf

Table 13: FET Sizes and Parameters

Transistor	Size (W/L)	g_m/I_d	$g_m * r_o$	I_d/W	f_t
PassFET pmos	285.7u/90n	10	50	37	28 GHz
Diff-Amp pmos	675.67n/90n	10	40	37	28 GHz
Diff-Amp nmos	283n/90n	10	40	88.33	60 GHz
Current Mirror nmos	1080n/10u	-	-	40	10 GHz

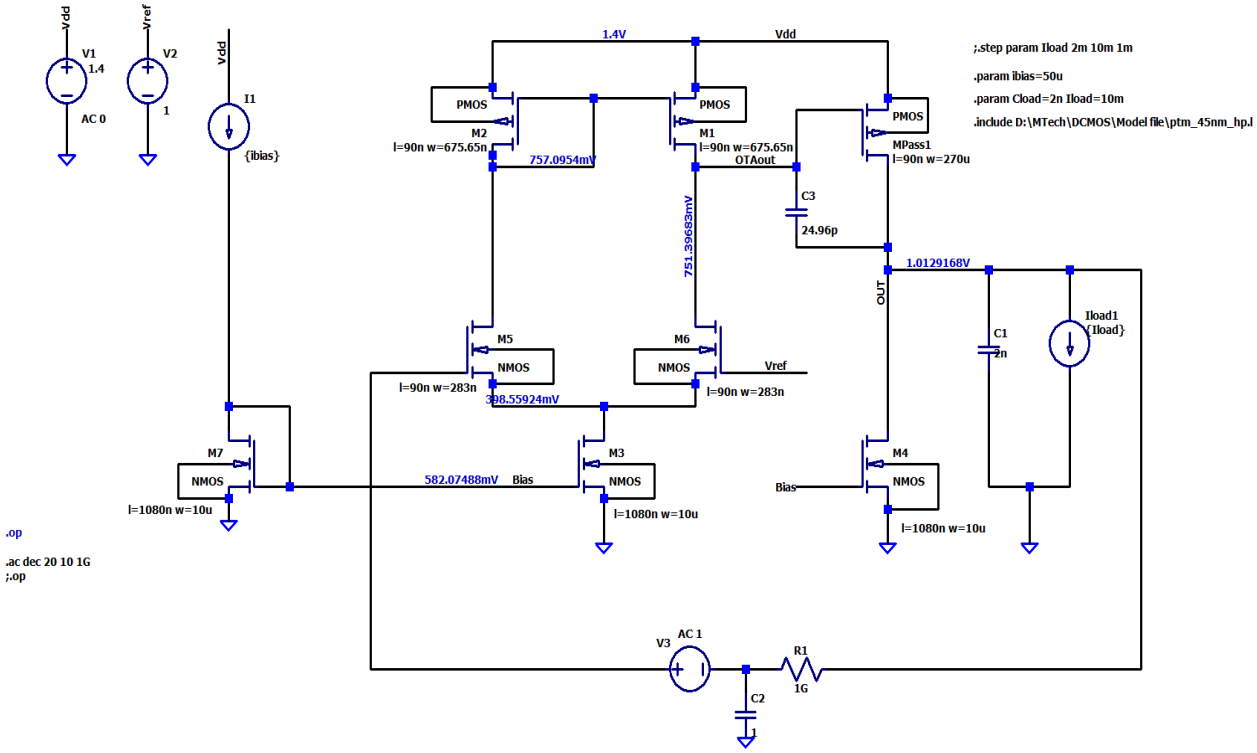

Figure 32: FET sizes and characteristics.

11. PSRR Simulation Result

Heavy Load (10 mA)

Case 1: Loop Gain Analysis

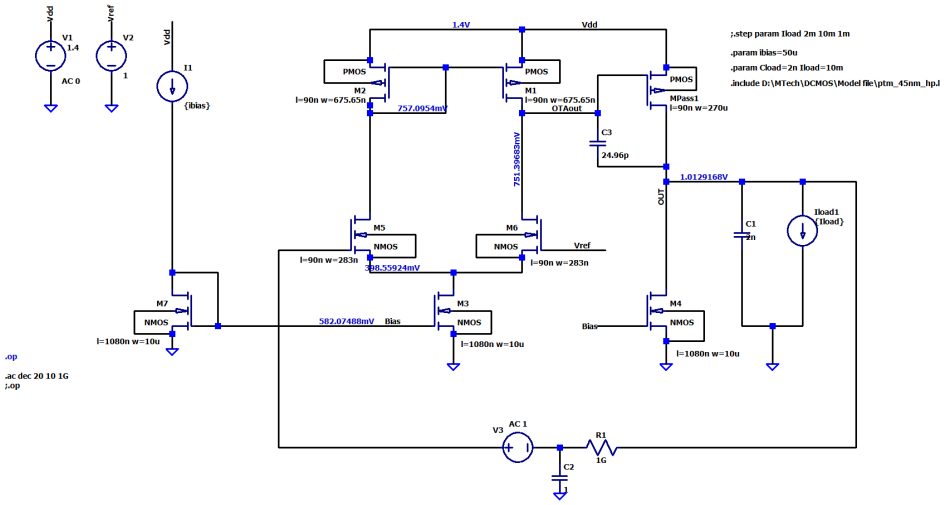

Figure 33: Schematic

Output Log File:-

SPICE Output Log: D:\MTech\ACMOS\Project\Internally_Comp_New\TusharOLckt2IntComp.log

```
LTspice 24.0.12 for Windows
Circuit: * D:\MTech\ACMOS\Project\Internally_Comp_New\TusharOLckt2IntComp.asc
Start Time: Sat Dec  7 20:52:05 2024
solver = Normal
Maximum thread count: 8
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                        --- BSIM4 MOSFETS ---
Name:     mpass1        m1          m2          m3          m4
Model:     pmos        pmos        pmos        nmos        nmos
Id:     -1.01e-02   -2.48e-05   -2.48e-05    4.97e-05    5.06e-05
Vgs:    -6.49e-01   -6.43e-01   -6.43e-01    5.82e-01    5.82e-01
Vds:    -3.87e-01   -6.49e-01   -6.43e-01    3.99e-01    1.01e+00
Vbs:     0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Vth:    -4.87e-01   -4.84e-01   -4.84e-01    4.69e-01    4.69e-01
Vdsat:  -1.77e-01   -1.75e-01   -1.75e-01    1.38e-01    1.38e-01
Gm:      9.95e-02    2.50e-04    2.49e-04    6.06e-04    6.16e-04
Gds:     2.52e-03    5.00e-06    5.01e-06    1.93e-06    1.30e-06
Gmb      2.11e-02    5.28e-05    5.28e-05    1.40e-04    1.42e-04
Cbd:     1.21e-13    2.86e-16    2.87e-16    4.48e-15    3.97e-15
Cbs:     2.16e-13    5.41e-16    5.41e-16    8.00e-15    8.00e-15

Name:       m5          m6          m7
Model:    nmos        nmos        nmos
Id:     2.48e-05    2.49e-05    5.00e-05
Vgs:    6.01e-01    6.01e-01    5.82e-01
Vds:    3.59e-01    3.53e-01    5.82e-01
Vbs:    0.00e+00    0.00e+00    0.00e+00
Vth:    4.66e-01    4.66e-01    4.69e-01
Vdsat:  1.43e-01    1.43e-01    1.38e-01
Gm:     2.44e-04    2.44e-04    6.10e-04
Gds:    5.07e-06    5.16e-06    1.48e-06
Gmb     5.62e-05    5.63e-05    1.41e-04
Cbd:    1.28e-16    1.28e-16    4.30e-15
Cbs:    2.26e-16    2.26e-16    8.00e-15

Total elapsed time: 0.116 seconds.
```

Figure 34: Log File

Table 14: All MOSFETs in saturation

Device Name	Device Type	$\lvert V_{ds}\rvert$	$\lvert V_{gs}\rvert$	$\lvert V_t\rvert$	$\lvert V_{gs}\rvert - \lvert V_t\rvert$	Reason for saturation
MPass1	PMOS	0.38	0.649	0.48	0.16	$V_{sd} > 0.16$
M1	PMOS	0.64	0.643	0.48	0.163	$V_{sd} > 0.163$
M2	PMOS	0.643	0.643	0.48	0.163	$V_{sd} > 0.163$
M5	NMOS	0.359	0.601	0.468	0.133	$V_{ds} > 0.133$
M6	NMOS	0.353	0.601	0.468	0.133	$V_{ds} > 0.133$
M3	NMOS	0.399	0.582	0.468	0.114	$V_{ds} > 0.114$
M7	NMOS	0.582	0.582	0.468	0.114	$V_{ds} > 0.114$
M4	NMOS	1.01	0.582	0.468	0.114	$V_{ds} > 0.114$

Output Waveform

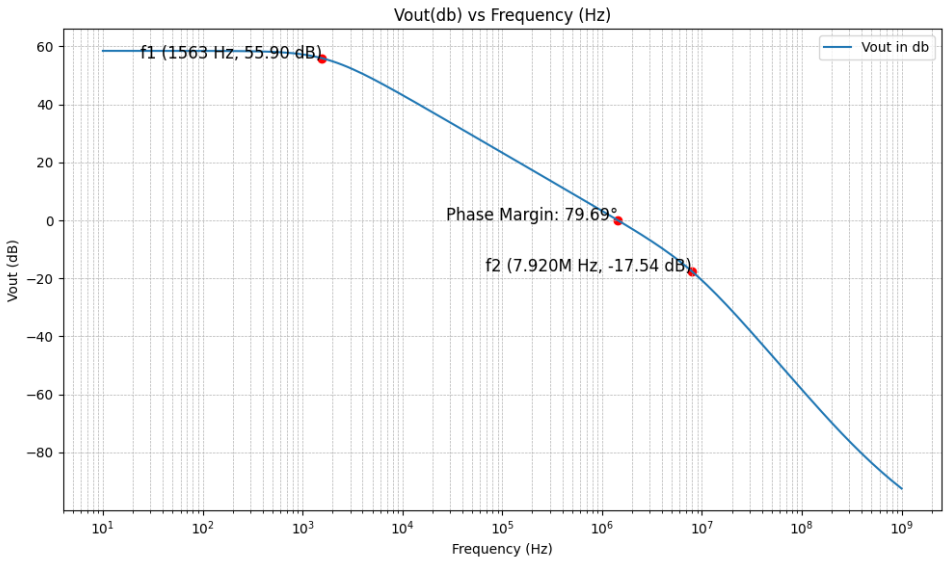

Figure 35: Output Waveform Vout

The phase margin is **79.69**.

Case 2:- Open Loop PSRR calculation

Schematic:

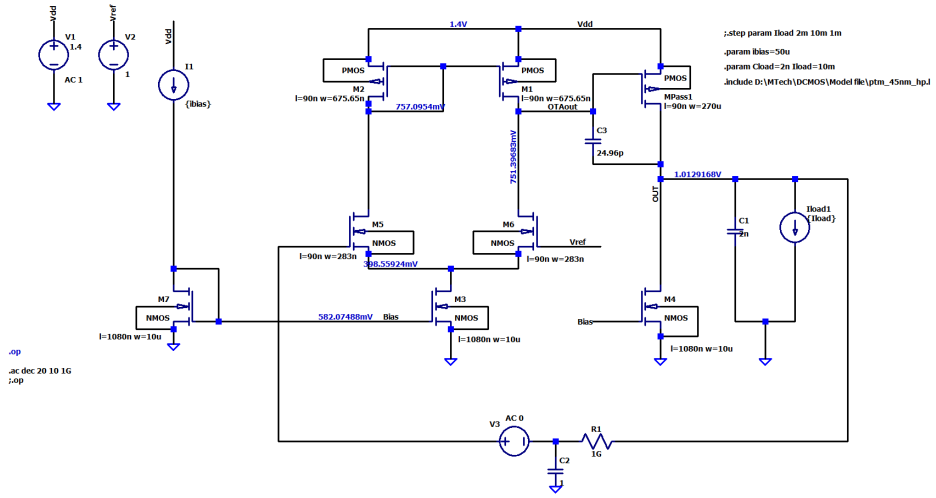

Figure 36: Schematic

Output Waveforms:

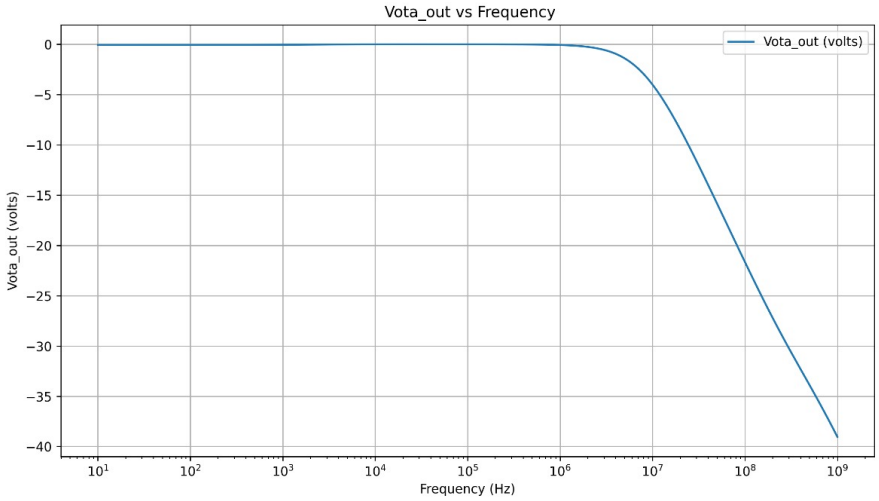

Figure 37: Output Waveform Vota

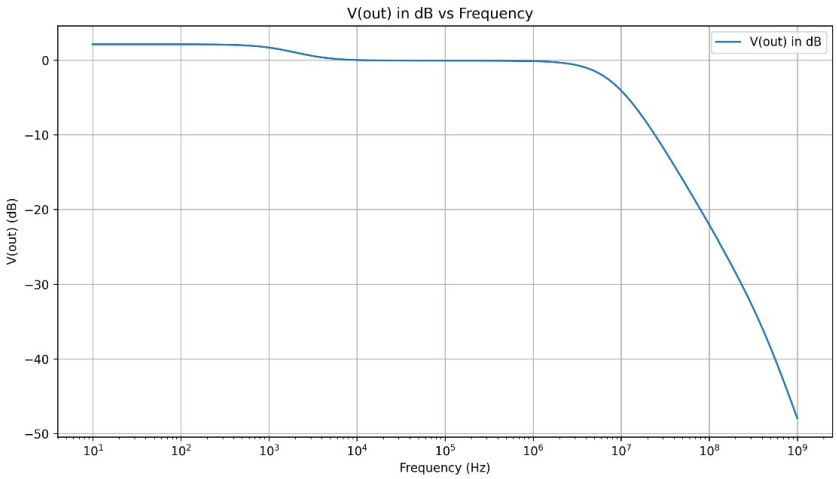

Figure 38: Output Waveform Vout

Case 3:- Closed Loop PSRR Calculation

Schematic:

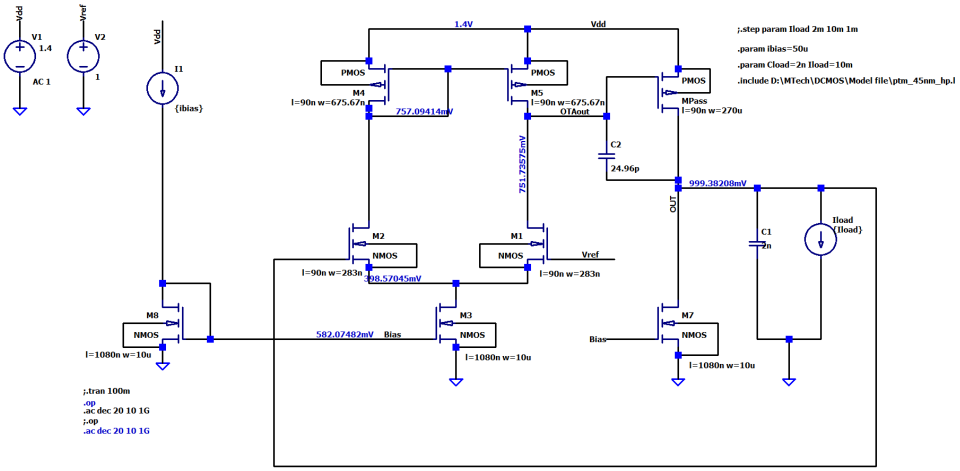

Figure 39: Schematic

Output Waveforms:

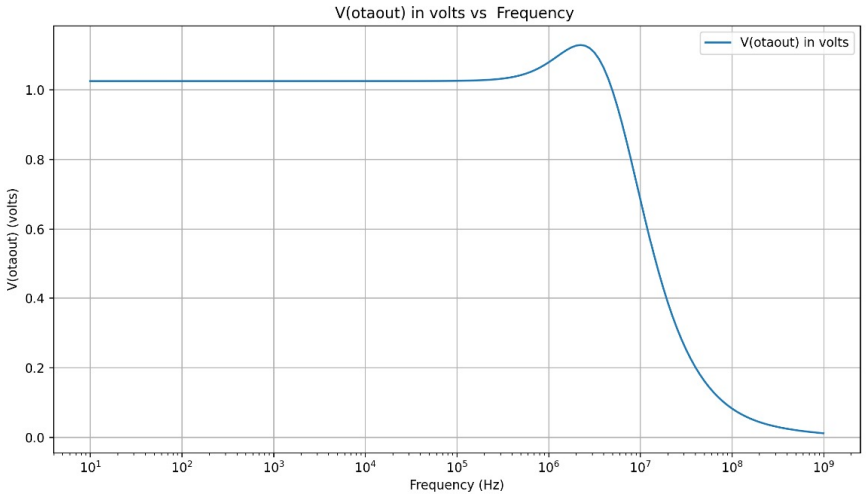

Figure 40: Output Waveform Vota

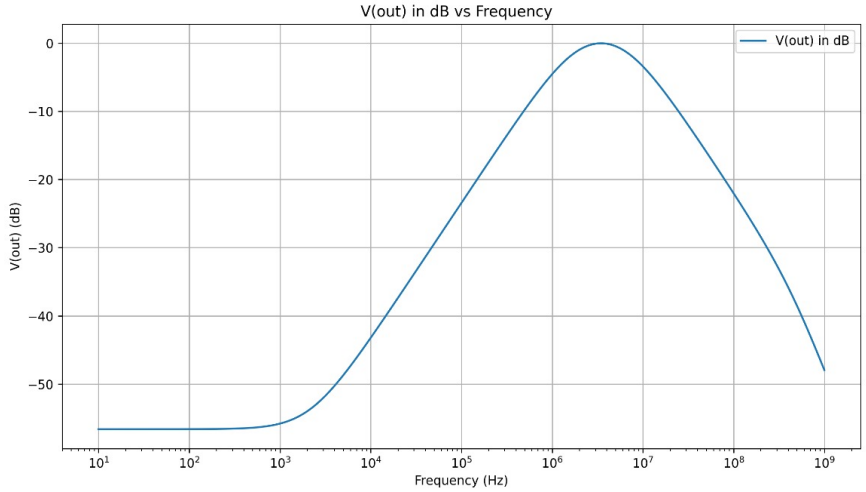

Figure 41: Output Waveform Vout

Light Load (2 mA)

Case 1: Loop Gain Analysis

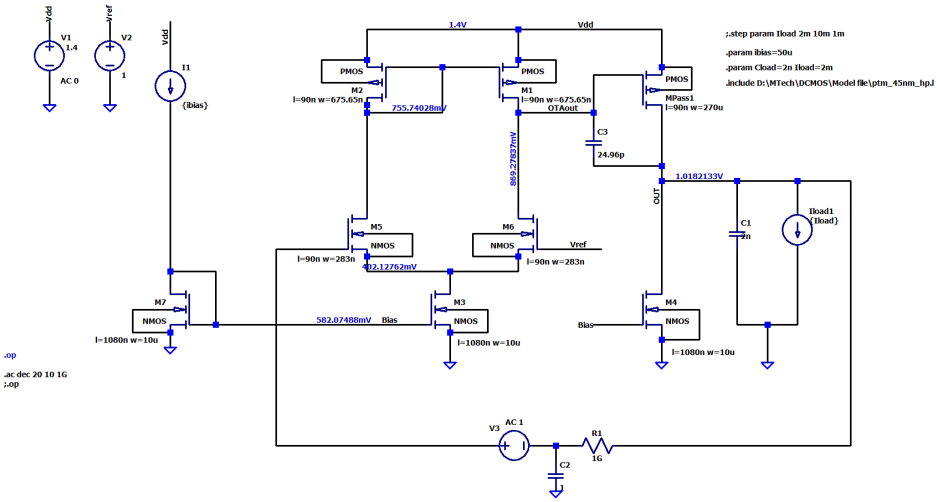

Figure 42: Schematic

Output Log File:-

SPICE Output Log: D:\MTech\ACMOS\Project\TusharOLckt2.log

```
LTspice 24.0.12 for Windows
Circuit: * D:\MTech\ACMOS\Project\TusharOLckt2.asc
Start Time: Sat Dec  7 19:43:32 2024
solver = Normal
Maximum thread count: 8
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                         --- BSIM4 MOSFETS ---
Name:     mpass1         m1           m2           m3           m4
Model:     pmos          pmos         pmos         nmos         nmos
Id:      -2.05e-03    -2.45e-05    -2.51e-05     4.97e-05     5.06e-05
Vgs:     -5.31e-01    -6.44e-01    -6.44e-01     5.82e-01     5.82e-01
Vds:     -3.82e-01    -5.31e-01    -6.44e-01     4.02e-01     1.02e+00
Vbs:      0.00e+00     0.00e+00     0.00e+00     0.00e+00     0.00e+00
Vth:     -4.87e-01    -4.85e-01    -4.84e-01     4.69e-01     4.69e-01
Vdsat:   -9.46e-02    -1.75e-01    -1.76e-01     1.38e-01     1.38e-01
Gm:       3.59e-02     2.47e-04     2.51e-04     6.06e-04     6.16e-04
Gds:      6.60e-04     5.24e-06     5.05e-06     1.91e-06     1.30e-06
Gmb       7.41e-03     5.22e-05     5.32e-05     1.40e-04     1.42e-04
Cbd:      1.21e-13     2.94e-16     2.87e-16     4.47e-15     3.97e-15
Cbs:      2.16e-13     5.41e-16     5.41e-16     8.00e-15     8.00e-15

Name:       m5           m6           m7
Model:     nmos         nmos         nmos
Id:       2.51e-05     2.46e-05     5.00e-05
Vgs:      6.02e-01     5.98e-01     5.82e-01
Vds:      3.54e-01     4.67e-01     5.82e-01
Vbs:      0.00e+00     0.00e+00     0.00e+00
Vth:      4.66e-01     4.65e-01     4.69e-01
Vdsat:    1.44e-01     1.42e-01     1.38e-01
Gm:       2.45e-04     2.44e-04     6.10e-04
Gds:      5.19e-06     4.33e-06     1.48e-06
Gmb       5.66e-05     5.63e-05     1.41e-04
Cbd:      1.28e-16     1.25e-16     4.30e-15
Cbs:      2.26e-16     2.26e-16     8.00e-15


Total elapsed time: 0.093 seconds.
```

Figure 43: Log File

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Table 15: All MOSFETs in Saturation

Device Name	**Device Type**	$\|V_{ds}\|$	$\|V_{gs}\|$	$\|V_t\|$	$\|V_{gs}\| - \|V_t\|$	**Reason for Saturation**
MPass1	PMOS	0.382	0.531	0.487	0.044	$V_{sd} > 0.044$
M1	PMOS	0.531	0.644	0.485	0.159	$V_{sd} > 0.159$
M2	PMOS	0.644	0.644	0.484	0.160	$V_{sd} > 0.160$
M5	NMOS	0.354	0.602	0.466	0.136	$V_{ds} > 0.136$
M6	NMOS	0.467	0.598	0.465	0.133	$V_{ds} > 0.133$
M3	NMOS	0.402	0.582	0.469	0.113	$V_{ds} > 0.113$
M7	NMOS	0.582	0.582	0.469	0.113	$V_{ds} > 0.113$
M4	NMOS	1.020	0.582	0.469	0.113	$V_{ds} > 0.113$

Output Waveform

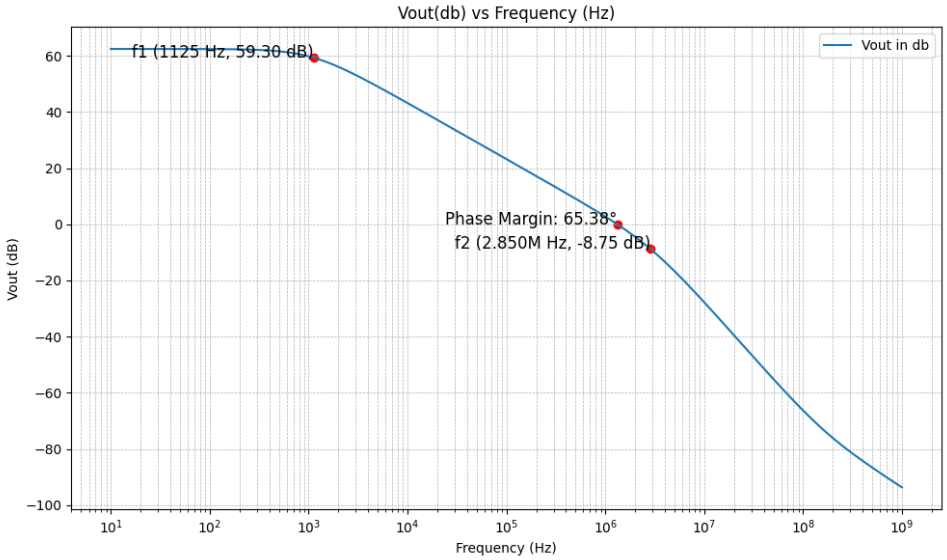

Figure 44: Output Waveform Vout

The phase margin is **65.38**.

Case 2:- Open Loop PSRR calculation

Schematic:

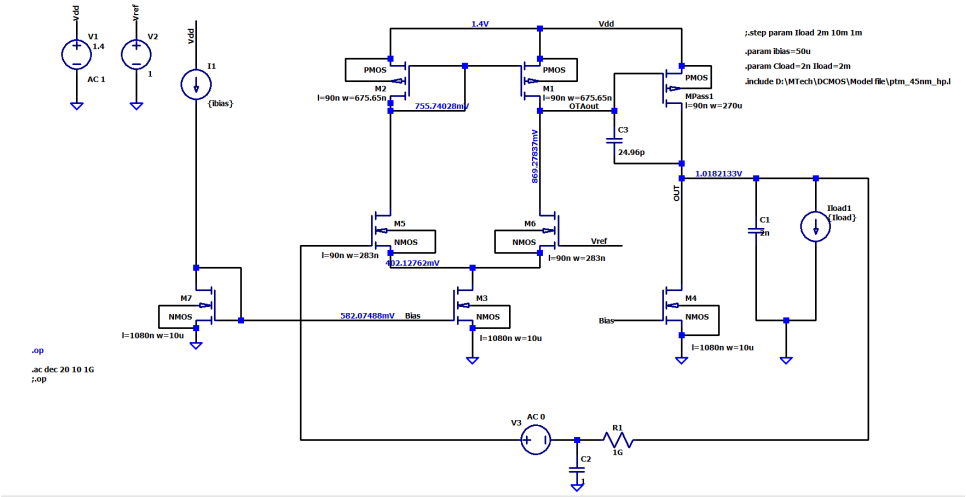

Figure 45: Schematic

Output Waveforms:

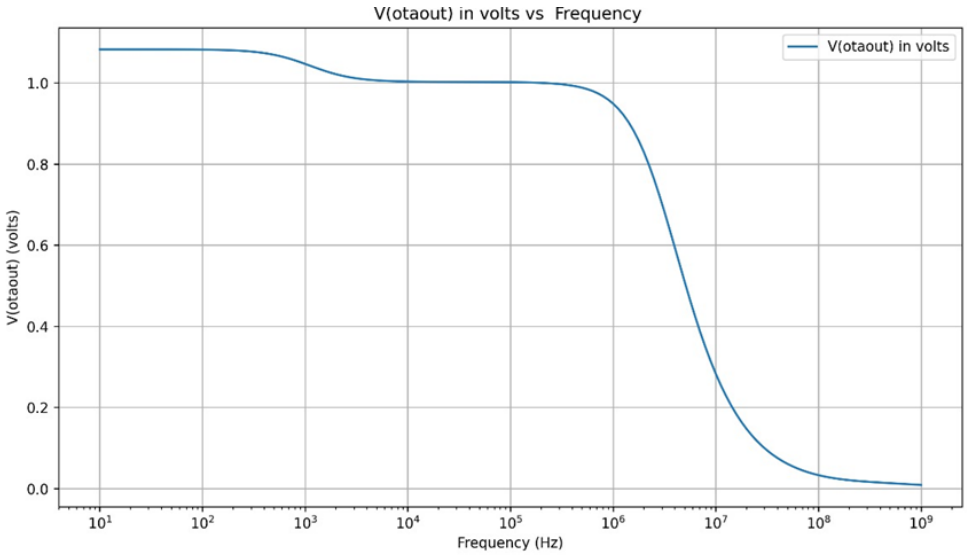

Figure 46: Output Waveform Vota

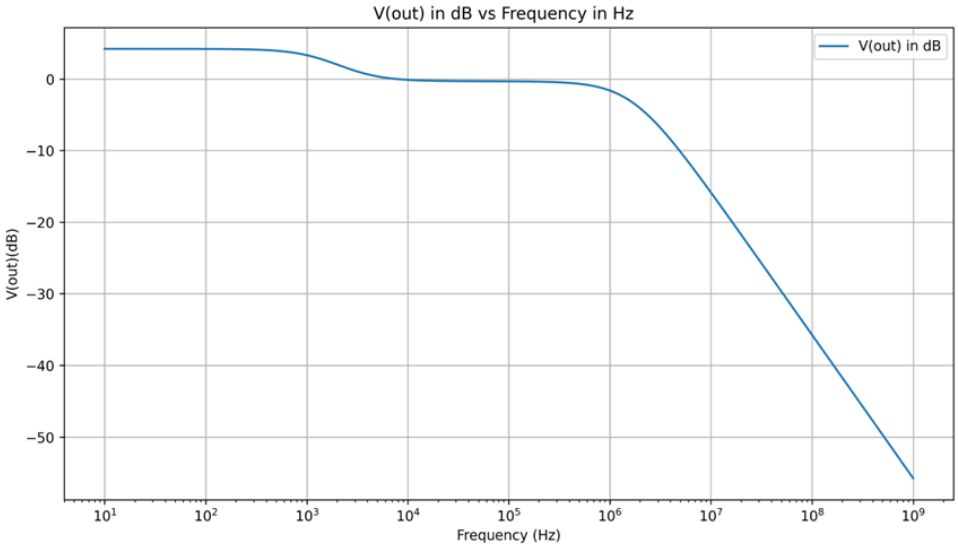

Figure 47: Output Waveform Vout

Case 3:- Closed Loop PSRR Calculation

Schematic:

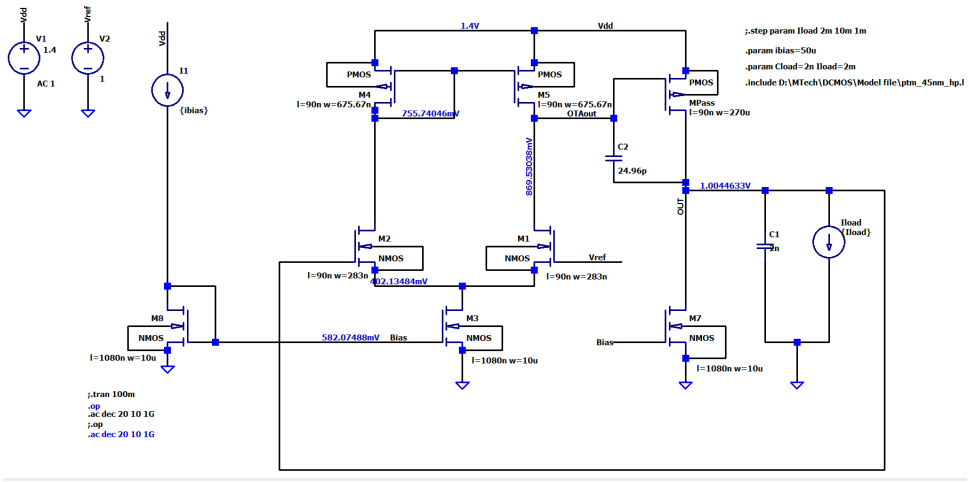

Figure 48: Schematic

Output Waveforms:

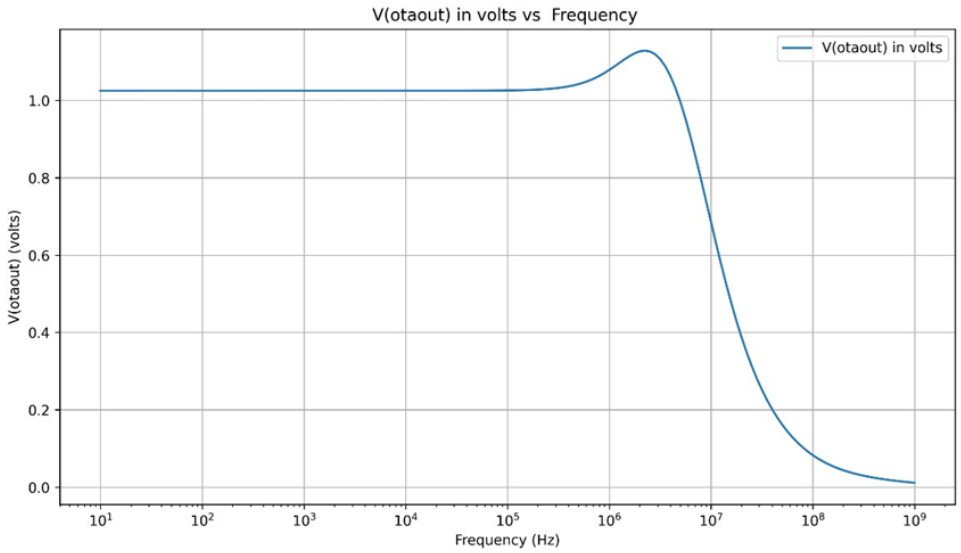

Figure 49: Output Waveform Vota

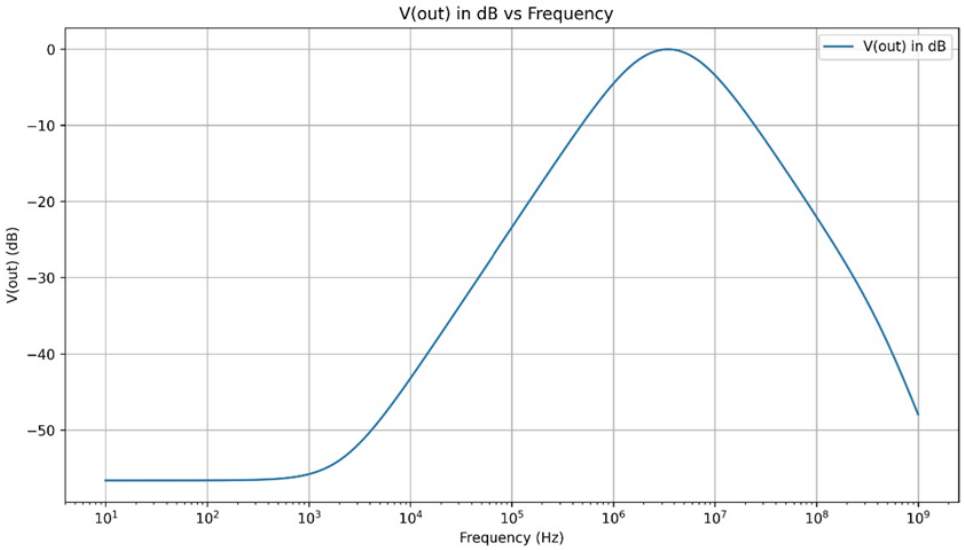

Figure 50: Output Waveform Vout

12. Transient Simulation Results

We have given a pulse at the load with a rise time and fall time of 1u. Also the period of the pulse is 10m with a 50% duty cycle. From the below figure we can understand that the output is not able to settle within the specified range of time. We are able to observe overshoot in the output.This is due to low output capacitor it is not able to hold the voltage.

Transient Analysis

Schematic

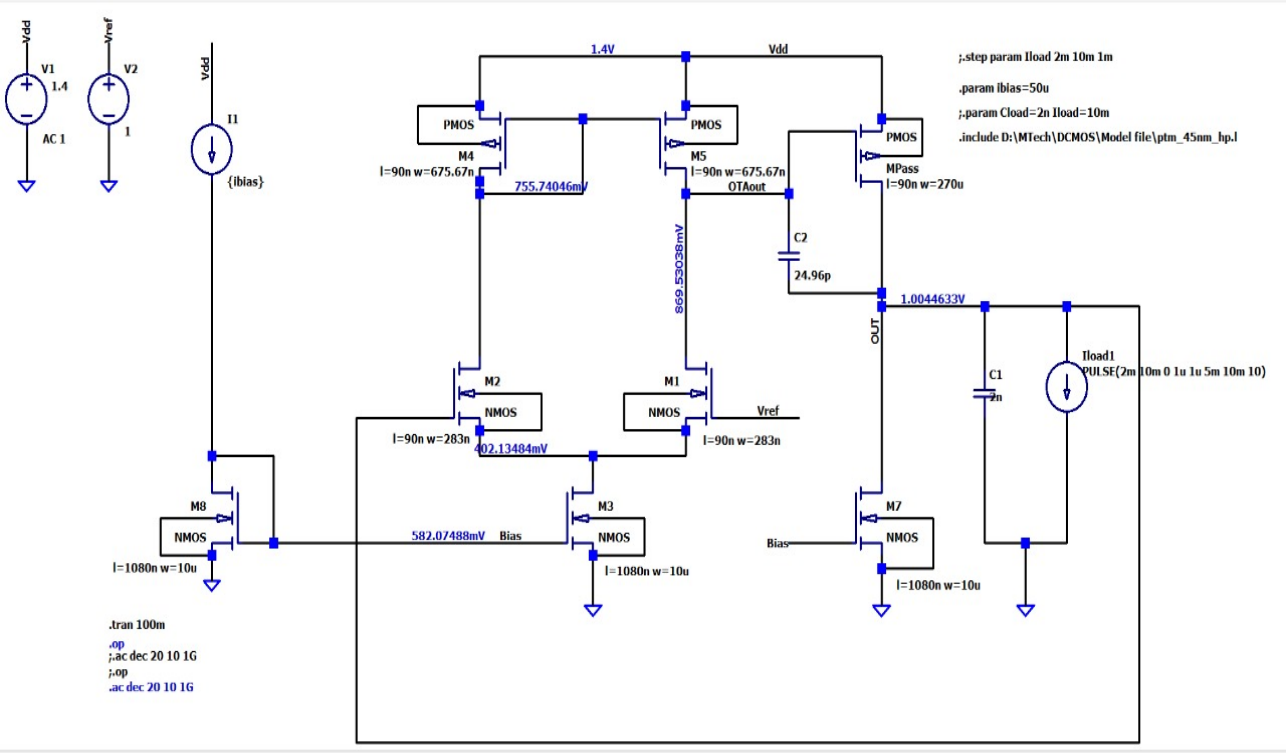

Figure 51: Schematic

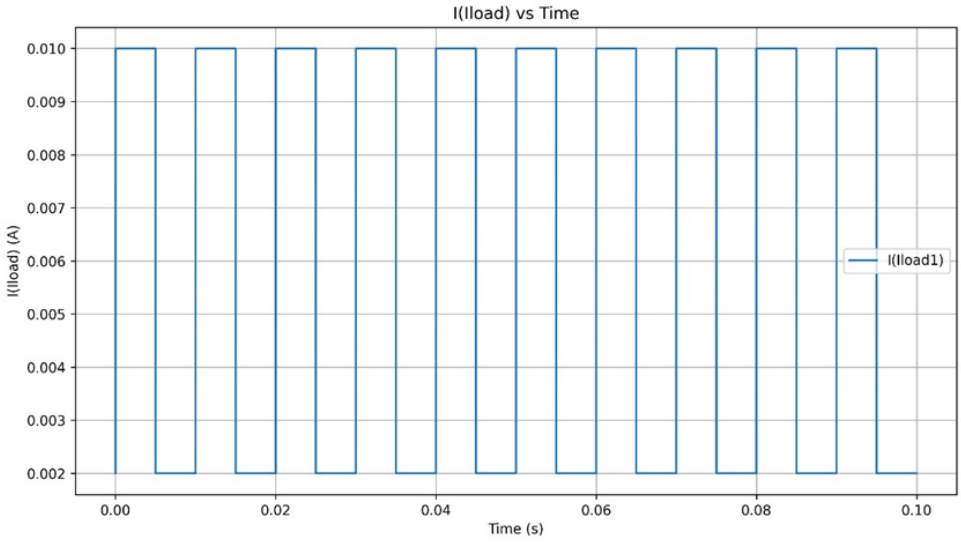

Figure 52: $I_{load} V stime$

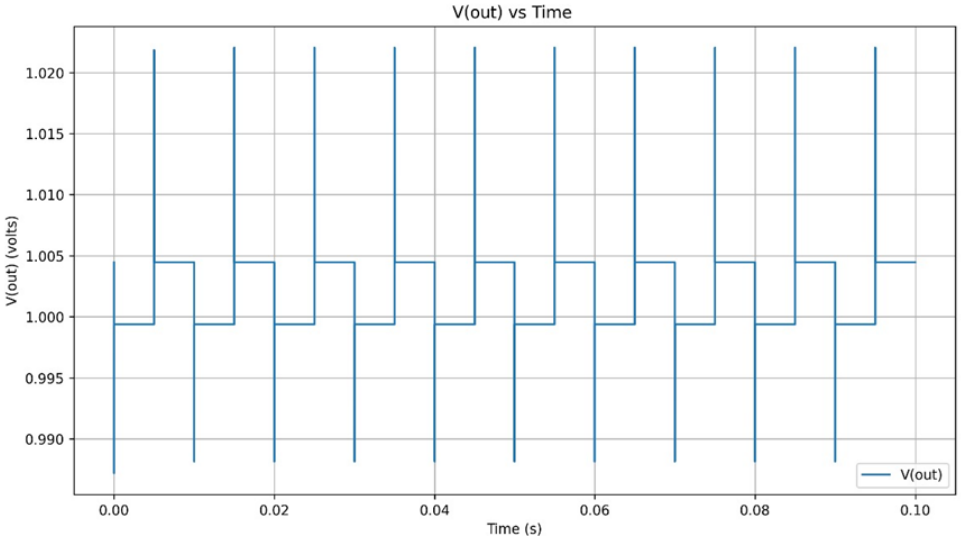

Figure 53: $V_{out} V stime$

13. Simulation vs. Hand Calculations

For Heavy Load of Passfet

Hand Calculations:

- $r_o = 500\,\Omega$
- $g_m = 0.1\,\text{A/V}$
- W_{p2} (Second Pole Location) = 10.33k
- $g_m r_o = 50$
- $C_L = 2n$
- $C_{gg} = 0.568p$

Simulation Results from SPICE Error Log:

- $r_o = 1/g_{ds} = 396.82\,\Omega$
- $g_m = 0.0995\,\text{A/V}$
- W_{p1} (First Pole Location) = 49.75M
- $g_m r_o = 39.48$

Table 16: Hand Calculation vs Simulation Results

Parameter	Hand Calculation	Simulation Result	% Difference
r_o (ohm)	500.00	396.82	20.63%
g_m (A/V)	0.1	0.0995	0.5%
$g_m * r_o$	50	39.48	21.04%
W_{p1} (Hz)	10.33k	9.82k	4.9%
W_{p2} (Hz)	50M	49.75M	0.5%
W_{ugb} (Hz)	10.33M	9.82M	4.9%
r_{odiff} (ohm)	80k	104.49k	23.4%
g_{mdiff} (A/V)	250u	247u	1.2%

Name	mpass	m1	m2	m3	m4	m5	m6	m7
Model	pmos	pmos	pmos	nmos	nmos	nmos	nmos	nmos
Id	-1.01E-02	-2.48E-05	-2.48E-05	4.97E-05	5.06E-05	2.48E-05	2.49E-05	5.00E-05
Vgs	-6.49E-01	-6.43E-01	-6.43E-01	5.82E-01	5.82E-01	6.01E-01	6.01E-01	5.82E-01
Vds	-3.87E-01	-6.49E-01	-6.43E-01	3.99E-01	1.01E+00	3.59E-01	3.53E-01	5.82E-01
Vbs	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Vth	-4.87E-01	-4.84E-01	-4.84E-01	4.69E-01	4.69E-01	4.66E-01	4.66E-01	4.69E-01
Vdsat	-1.77E-01	-1.75E-01	-1.75E-01	1.38E-01	1.38E-01	1.43E-01	1.43E-01	1.38E-01
Gm	9.95E-02	2.50E-04	2.49E-04	6.06E-04	6.16E-04	2.44E-04	2.44E-04	6.10E-04
Gds	2.52E-03	5.00E-06	5.01E-06	1.93E-06	1.30E-06	5.07E-06	5.16E-06	1.48E-06
Gmb	2.11E-02	5.28E-05	5.28E-05	1.40E-04	1.42E-04	5.62E-05	5.63E-05	1.41E-04
Cbd	1.21E-13	2.86E-16	2.87E-16	4.48E-15	3.97E-15	1.28E-16	1.28E-16	4.30E-15
Cbs	2.16E-13	5.41E-16	5.41E-16	8.00E-15	8.00E-15	2.26E-16	2.26E-16	8.00E-15
rds	3.97E+02	2.00E+05	2.00E+05	5.18E+05	7.69E+05	1.97E+05	1.94E+05	6.76E+05
gm*rds	3.95E+01	5.00E+01	4.97E+01	3.14E+02	4.74E+02	4.81E+01	4.73E+01	4.12E+02

Table 17: Transistor Parameters

For Light Load of Passfet

Hand Calculation

- $r_o = 2500\,\Omega$
- $g_m = 0.02\,\text{A/V}$
- W_{p1} (first pole location) = 10k
- $g_m r_o = 50$
- $C_L = 2n$
- $C_{gg} = 0.1136p$

Simulation Results from SPICE Error Log:

- $r_o = 1/g_{ds} = 1515.15\,\Omega$
- $g_m = 0.0359\,\text{A/V}$
- W_{p1} (first pole location) = 7.07k
- $g_m r_o = 54.39$

Table 18: Hand Calculation vs Simulation Results

Parameter	**Hand Calculation**	**Simulation Result**	**% Difference**
r_o (ohm)	2500.00	1515.15	39.39%
g_m (A/V)	0.02	0.0359	33.33%
$g_m * r_o$	50	54.39	8%
W_{p1} (Hz)	10k	7.07k	29.3%
W_{p2} (Hz)	10M	17.95M	44.28%
W_{ugb} (Hz)	10M	7.07M	29.3%
r_{odiff} (ohm)	80k	104.04k	23.1%
g_{mdiff} (A/V)	250u	250u	0%

Parameter	**mpass**	**m1**	**m2**	**m3**	**m4**	**m5**	**m6**	**m7**
Id	-2.05E-03	-2.45E-05	-2.51E-05	4.97E-05	5.06E-05	2.51E-05	2.46E-05	5.00E-05
Vgs	-5.31E-01	-6.44E-01	-6.44E-01	5.82E-01	5.82E-01	6.02E-01	5.98E-01	5.82E-01
Vds	-3.82E-01	-5.31E-01	-6.44E-01	4.02E-01	1.02E+00	3.54E-01	4.67E-01	5.82E-01
Vbs	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Vth	-4.87E-01	-4.85E-01	-4.84E-01	4.69E-01	4.69E-01	4.66E-01	4.65E-01	4.69E-01
Vdsat	-9.46E-02	-1.75E-01	-1.76E-01	1.38E-01	1.38E-01	1.44E-01	1.42E-01	1.38E-01
Gm	3.59E-02	2.47E-04	2.51E-04	6.06E-04	6.16E-04	2.45E-04	2.44E-04	6.10E-04
Gds	6.60E-04	5.24E-06	5.05E-06	1.91E-06	1.30E-06	5.19E-06	4.33E-06	1.48E-06
Gmb	7.41E-03	5.22E-05	5.32E-05	1.40E-04	1.42E-04	5.66E-05	5.63E-05	1.41E-04
Cbd	1.21E-13	2.94E-16	2.87E-16	4.47E-15	3.97E-15	1.28E-16	1.25E-16	4.30E-15
Cbs	2.16E-13	5.41E-16	5.41E-16	8.00E-15	8.00E-15	2.26E-16	2.26E-16	8.00E-15
ro	1.52E+03	1.91E+05	1.98E+05	5.24E+05	7.69E+05	1.93E+05	2.31E+05	6.76E+05
gm*rds	5.44E+01	4.71E+01	4.97E+01	3.17E+02	4.74E+02	4.72E+01	5.64E+01	4.12E+02

Table 19: Transistor Parameters

14. Stability Analysis

For Heavy load we get the following curve:

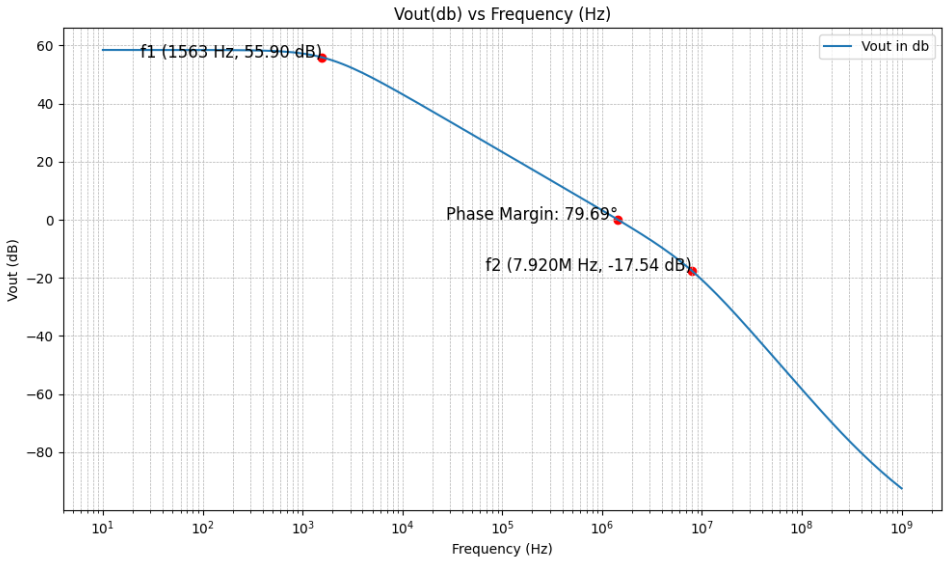

Figure 54: Stability Analysis for I=10 mA

For Light load we get the following curve

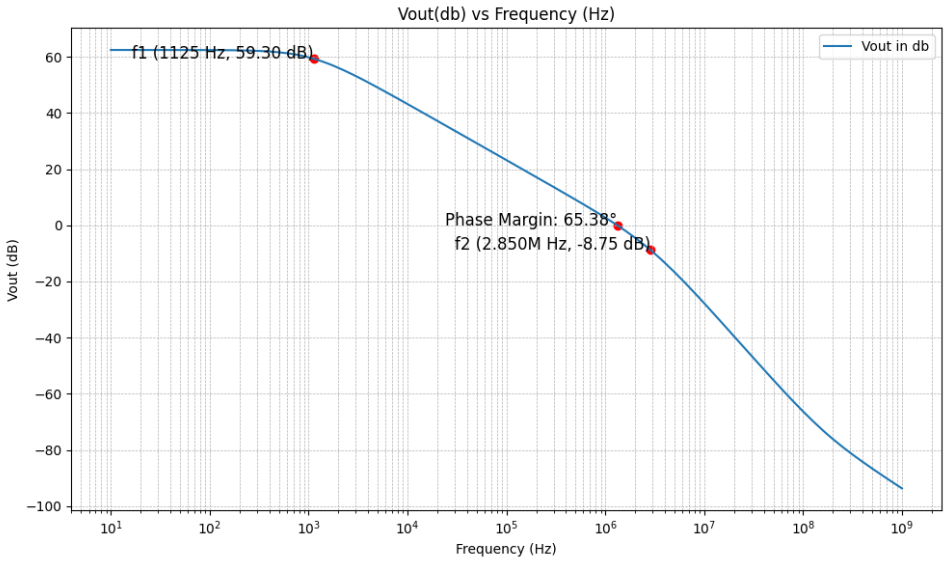

Figure 55: Stability Analysis for I=2 mA

Table 20: Key Metrics under Heavy and Light Load Conditions

Parameter	**Heavy Load**	**Light Load**
DC Loop Gain (dB)	58.6	62
Unity Gain Bandwidth (MHz)	1.56	1.125
Phase Margin (degrees)	79.69	65.38
Pole 1 (kHz)	1.563	1.125
Pole 2 (MHz)	7.92	2.85

From the above analysis we can see that the unity gain bandwidth is closer to the second pole for the light load case than the light load case. From the phase margin also we can observe that we observe a lesser phase margin of 65.38 degrees for the light load case than that of the heavy load case. From this analysis, we can say that we get a more stable system when we apply heavy load.

15. Obsevations

- From the above analysis we can conclude that we need to design the LDO for higher current ratings in each case.
- Externally Compensated LDO is best for low load current as Phase Margin reduces with high load current.
- Internally Compensated LDO is best for high load current as Phase Margin reduces with low load current.