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SET A (TT-1)

(Q1) (A)

An embedded system is a computing device that does a specific job. Both the hardware & software are optimized for that specific job.

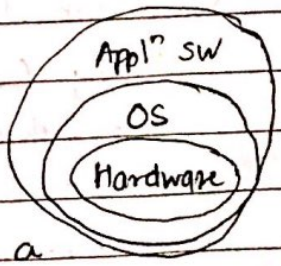
3 main components required to design an embedded system is -

① Firmware (Application specific embedded software)
② Processor
③ Hardware.

The specific features that characterize an embedded system -

- ES do very specific job/task, they can't be programmed to do diff things
- ES has limited resources, (memory). They do not have secondary storage devices.
- ES have to work against some deadlines. A specific job has to be completed within a specific time (realtime). Deadlines are stringent & missing one may cause a catastrophe (loss of life or damage to property).
- ES are constrained for power. Through a battery option, low power consumption
- ES needs to be highly reliable. Can't afford to reset any system
- Some ES have to operate in extreme environmental cond^n's (high temp, humid
- ES that address the consumer market are very cost-sensitive.
- Choosing the right platform is the most complex task as a wide variety of procssors & OS are available for ES.

(B) Layered Architecture of ES



Every ES consists of custom built hardware built around a CPU. This hardware also contains memory chips onto which the S/W is loaded, called as 'firmware'. The ES architecture can be represented as a layered architecture. The OS runs above the hardware and the application

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software runs above the OS. The same architecture is applicable to any computer (desktop computer). Including some differences, it is not necessary to have OS in every ES (eg: small scale appl^{n}s) but for complex appl^{n}s, it is advised to have OS.

The 4 categories/classification of ES are -

① Standalone ES - work in standalone mode. They take i/ps process them & produce the desired o/p.
eg: Digital cameras, oven, AC's, CD players.

② Real time Systems - ES in which some specific work has to be done in a specific time period are called realtime systems. Divided into 2 types - Hard → Deadline specific (may lead to catastrophe).
Soft → not deadline specific.
eg: Satellite/Missile Track & Launch (hard)
CD/DVD player/phone (soft).

③ Networked info Appliances - ES that are provided with n/w interfaces & accessed by n/w such as local area n/w or the internet.
eg: Door webcam connected over internet for security (firmware + HTTP).
Sensor nodes for agriculture (temp + pH + moisture).

④ Mobile devices - Special category of ES. They need to be designed just like the 'conventional' ES. limitations include - memory constraints, small size, lack of good user interfaces.

The 7 specialities of ES are explained below -

① Reliability : ES should work continously for hours without break. Many ES are inaccessible & hidden so can't be reset manually. Reset should be automatic and watchdog timer should be built to take care of reset. ES should be able to work in stringent, extreme environmental cond^{n}s (extr temp, humidity, vibrations, bumps), this ability is called ruggedness.

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(2)

(2) Performance : ES have time constraints. Every soft and hard real time system has to adhere to deadlines to avoid catastrophes & delays.

(3) Power consumption : ES operate on battery and to avoid frequent charging & battery drain, ES needs to have low power consumption. This can be done by reducing the no. of h/w components - also increases reliability

(4) Cost : Cost is dependant on first, criticality & second, mass production. Wrt criticality of any job, cost may not be an imp factor as to avoid any catastrophe. But on the other hand, if mass production of any thing, cost reduction plays a very imp. role and one can save millions.

(5) Size : Size along with weight are important factors which the designers have to reduce by reducing no. of components. ~~More~~ Lesser the size & weight, more is the popularity & usability of ES.

(6) Limited User interface : ES donot have sophisticated interfaces for i/p & o/p. i/p is through func^n keypad / buttons. o/p is displayed on LEDs / LCDs. Developing a user friendly interface with limitations of i/p/o/p devices is a challenging tasks for developers.

(7) Software upgradation capability : ES once fitted with s/w has to run till its life runs out but there's a procedure where an operator can update the s/w with latest trends and fit it again by paying them a fixed amount.

(Q2) (A)

No. of units = S

Product life = 2W.

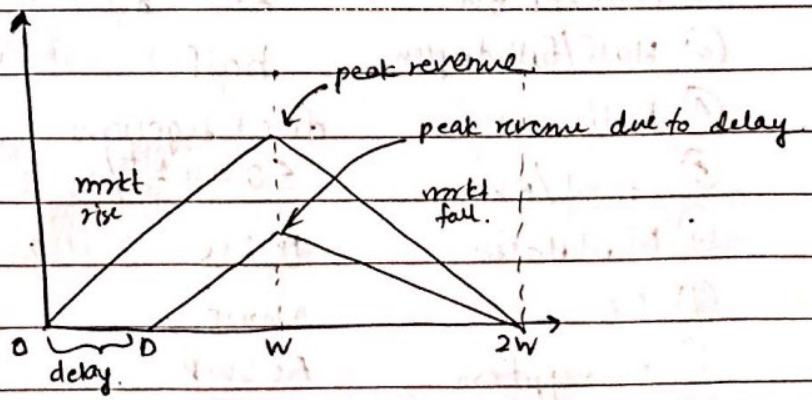
Delay time = D.

W = 24 months.

D = 2 months.

revenue loss ?

% revenue loss ?



Revenue loss = $\frac{D(3W-D)}{2}$. % loss = $\frac{D(3W-D)}{2W^2}$.

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Revenue loss = $\frac{2[3(24)-2]}{2}$ % loss = $\frac{2[3(24)-2]}{2(24)^2} \times 100$

Revenue loss = 70 ₹. % loss = 12.1528 %.

(B) cost per unit = ₹ = 18,000/-

Units manufactured per month = 2500 units.

Units manufactured per year = 12 × 2500 = 30,000 units. = N.

Total cost incurred for prodⁿ unit = 12,00,000 + 8,00,000

X = 20 lakhs

cost per unit = $\frac{x}{N} + y = \frac{20,00,000}{30,000} + 18,000$

∴ cost per unit = $\frac{200}{3} + 18,000$

∴ cost per unit = 18,066.6667/-

(Q3) (A) Wifi 802.11b standard with 802.11a,g standard.

Parameters	80.2.11b	802.11a	80211g
① Frequency Band	2.4GHz	5GHz	2.4GHz.
② Channel BW	22MHz	20MHz	20MHz.
③ Half/full duplex	half	half	half.
④ Radio techno	direct sequence	OFDM	OFDM
⑤ Speed /BW	≤0.44 bits/s/Hz.	2.7 bits/s/Hz	2.7 bits/s/Hz.
⑥ Modulation	QPSK	BPSK	QPSK
⑦ FEC	none	convolution	convolution
⑧ Encryption	AESWPS	WPA	WPA2.
⑨ Access protocol.	CSMA/CA	CSMA/CA	CSMA/CA

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(B). Bluetooth.

(i) Frequency Range & channels.

it has frequency range of 2402 - 2480 MHz. [79 MHz Band]
it has 3 non-overlapping channels with 1 MHz carriers.

(ii) Data Rate

it has a data rate of 1 Mbps using 1 MHz (nominal) and 720 kbps (user).

(iii) RF hopping

it has Radio frequency hopping of 1600 times/s which is nothing but 625 µs/hop.

(iv) Security

it has security provided due to challenge/response authentication as well as 128b encryption.

(v) Output transmitting power.

it is given by -

class 1 - 20 dBm max (0.1W) - 100m
class 2 - 4 dBm (2.5mW)
class 3 - 0 dBm (1mW) - 10m.

Bluetooth 1.1 : IEEE 802.15.1 - 2002			
Bluetooth 1.2 : IEEE 802.15.1 - 2005 (Nov 2003)	Extended SCO	Higher variable rate retransmission	Adaptive frequency hopping avoid interference
Bluetooth 2.0 : Enhanced data rate (Nov 2004)	3 Mbps BPSK	Video appln.	reduced power due to reduced duty cycle.
Bluetooth 2.1 : EDR (July 2007)	Secure simple pairing to speed up pairing.		
Bluetooth 3.0 : High speed (April 2009)	24 Mbps using WiFi PHY + Bluetooth PHY for low rate		
Bluetooth 4.0 : (June 2010) low energy	Smaller devices longer battery life	New incompatible PHY	Bluetooth smart or BLE
Bluetooth 4.1 : 4.0 - core specification amendments (CSA) 1, 2, 3, 4.			

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(Q4)(A) ARM architecture processor modes
frame format of Program status register.

- There are 7 processor modes -

	Modes.	Description
①	User (usr)	normal program execution mode.
②	FIQ (fiq)	entered when a high priority (fast) interrupt is raised.
③	IRQ (irq)	entered when a low priority (normal) interrupt is raised.
④	supervisory (svc)	protected mode for OS which entered on reset & when s/w interrupt is executed.
⑤	Abort (abt).	used to handle memory access violation
⑥	undefined (und)	used to handle undefined instructions.
⑦	system (sys).	runs privileged OS tasks.

The statuses of the registers when these modes are accessed are -

USR SYS	FIQ	IRQ	SVC	UNDEF	ABT
r0	User mode r0-r7 r15 CPSR	User mode r0-r12 r15 CPSR	User mode r0-r12 r15 CPSR	User mode r0-r12 r15 CPSR	User mode r0-r12 r15 CPSR
r1					
r2					
r3					
r4					
r5					
r6					
r7					
r8	r8				
r9	r9				
r10	r10				
r11	r11				
r12	r12				
r13 SP	r13 SP	r13 SP	r13 SP	r13 SP	r13 SP
r14 LR	r14 LR	r14 LR	r14 LR	r14 LR	r14 LR
r15 PC					
CPSR					
	SPSR	SPSR	SPSR	SPSR	SPSR

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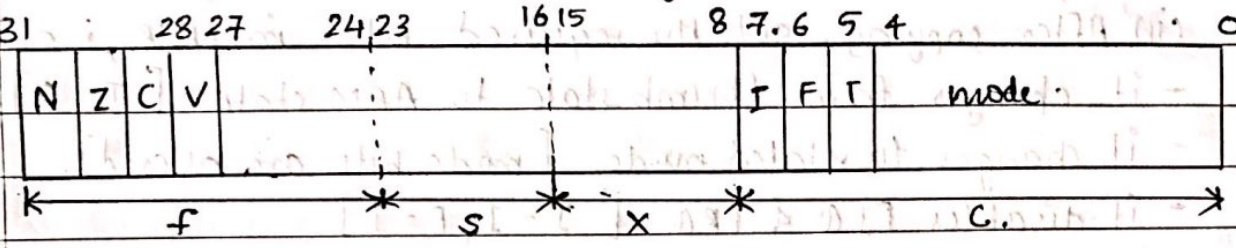
frame format of PSRs →

- ARM has 37 registers of 32 bits long each.
These contain 1 program counter, 1 current PSR, 5 saved PSR & 30 general purpose registers.
- The frame format of PSR is given below –



(i) Condition code flags – these flags show the status of the result from ALU. They include – N (negative), Z (zero), C (carry), V (overflow).
N : set if there is negative result from ALU, else, reset.
Z : set if there is zero result from ALU, else, reset.
C : set if carry is generated from ALU, else, reset.
V : set if result of ALU is overflowed, else, reset.

(ii) Interrupt disable bits – these bits show the status of interrupts.
I : for IRQ, if I = 1, disables IRQ mode. Else, enables.
F : for FIQ, if F = I, disables FIQ mode, Else, enables.

(iii) T bit (Thumb mode) – this bit shows the state of the processor. Either ARM state or thumb state.
T = 0 ; processor in ARM mode.
T = 1 ; processor in thumb state.

(iv) Mode bits – these bits show the mode in which processor is working.

10000	– User	10111	– Abort
10001	– FIQ	11011	– undefined
10010	– IRQ	11111	– System.
10011	– Supervisor		

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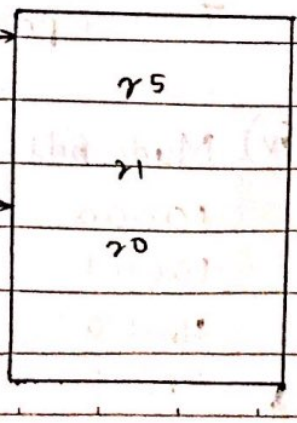
(Q4) (B) Exception Handling using PC & LR

- When any exception occurs in the ARM processor, the µP/µC follows the following steps –.
  (i) Copies the status of CPSR into SPSR-mode.
  (ii) After copying, sets the required bits in CPSR, i.e,
  - it changes from thumb state to ARM state [T = 0].
  - it changes to related mode [mode bits are altered].
  - it disables FIQ & IRQ [I = 1, F = 1].
  (iii) Stores return to address in the LR-mode, i.e, it stores in the link register.
  (iv) sets the PC (program counter) to vector address obtained by calculating using vector table.
  (v) After execution, it restores CPSR from SPSR-mode.
  (vi) Later, it restores PC (program counter) from LR-mode.

(i) LDR r0, [r1, #12]!
Contents : 1000 - 10, 1004 - 20, 1008 - 30, 100C - 40.
- Contents of r0 = 40.
- If PC started at 1000, r1 is pointing to 1004.

(ii) STMIA r9!, {r0, r1, r5} & STMDB r9!, {r0, r1, r5}.
Location of r9 = 100C

- STMIA : the IA instruction stands for increment after. r9 first points at 100C & value of r0 is stored 100C & r9 is incremented & it's value is 1010 & then next value is stored in r9. Location of r9 will be 1014.



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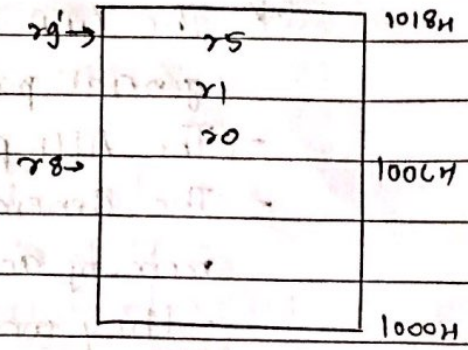
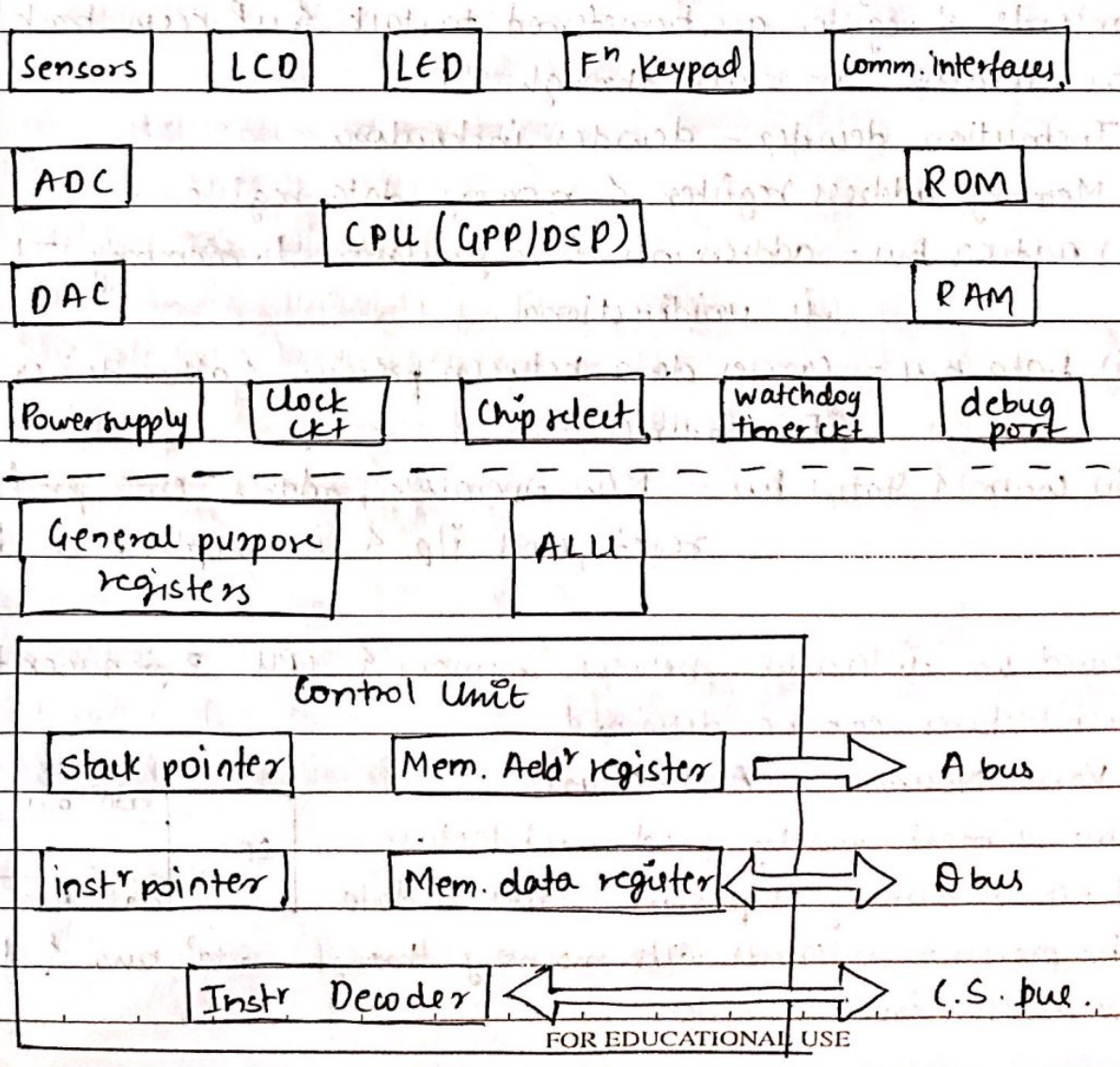
- STMDB : the instruction stands for increment before. The value of r9 is 1st incremented & then, r0 is stored in r9 & location of r9 will be 1018H.



SET B (T.T-1)

(Q1) (A) Internal Architecture of a General Purpose Processor. (Memory - CPU) — 3 prominent architectures.



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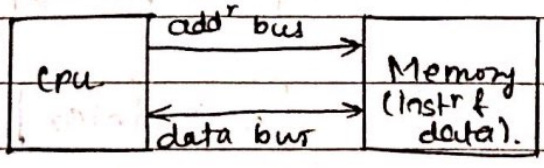
* The GPP consists mainly of 3 parts — ALU, control unit & general purpose registers.
- The ALU performs basic arithmetic & logical operations.
- The General purpose registers form the processor's internal memory and it varies from µP to µP.
- they contain current data & operands which are being manipulated.
- 8-bit, 16-bit processors refers to the width of the registers.
- The control unit comprises of 5 parts used to fetches instruction, decodes & executes them.
- Instruction pointer - this points to the next instruction to be executed.
- Stack pointer - points to stack in memory. During interrupts, contents of register are transferred to stack & µP keeps track of next free location in stack through S.P.
- Instruction decoder - decodes instruction.
- Memory address register & memory data register -
(i) Address Bus - address info from processor to memory. It is unidirectional.
(ii) Data Bus - carries data between processor & other devices. It is bidirectional.
(iii) Control & Status Bus - R/W operation, address error, processor reset, clock i/p & interrupts. it is bidirectional.

* Based on interaction between memory & CPU, 3 prominent architectures can be described -:

(i) Von Neumann Architecture.
- this is most widely used architecture.
- it has 1 memory chip stores instr & data.
- the processor interacts with memory through addr bus & data bus to fetch instr & data.



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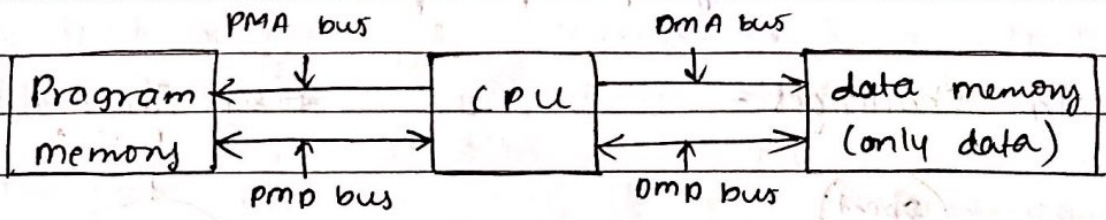
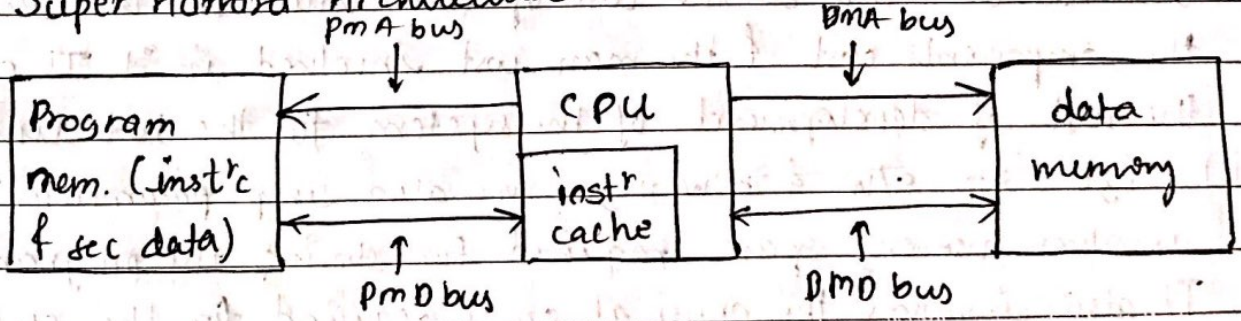
(ii) Harvard Architecture



- there are 2 separate memory blocks → 1) program memory & 2) data memory.
- PM stores only inst'c & data memory stores only data.
- 2 pairs of buses used btwn CPU & the memory blocks.
- PMA (program memory address) & PMD (program memory data) buses are used to access PM by CPU.
- DMA (data memory address) & DMD (data memory data) buses are used to access DM by CPU.
- This architecture is much more efficient due fast access of data & inst'c

(iii) Super Harvard Architecture



- It has a slight modification in Harvard type.
- Due to more access of Data memory in Harvard, provision has been made to store some secondary data in the program memory to balance load on both memory blocks.
-

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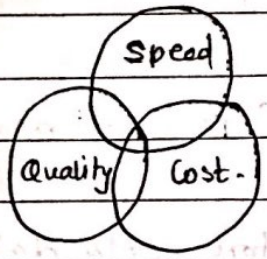
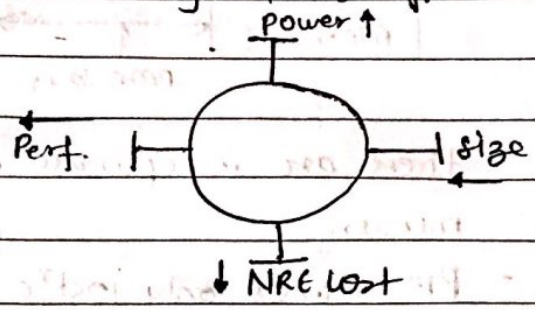
(Q2) (A) Design Challenges, Design Trade offs, Design metrics in HW-SW co-design principles of ES.

(i) Design Challenges -



Design Trade-offs -



- Design metrics - While desiging an ES the following points are to be considered -

(i) NRE (non-reuring expentidure) cost :- this includes the costs that are incurred only once & are not for each system. This includes the development cost of the system are other investments that are to be done.

(ii) Unit cost :- This is the cost of each unit. The cost includes the components cost & the man cost involved in it. It excludes the cost of development of the system for the 1st time.

(iii) Size :- S/W & H/W size are also imp parameters. It involves memory space required for storing the program & data. It also involves the physical space required for the circuits required for the system.

(iv) Performance :- The perf. of the system is to be compared with the already existing systems. The response time & the speed are imp. parameters to measure the perf. of the system.

(v) Power :- ES are battery operated. So, power consumption is more imp. parameter for the system design.

(vi) Flexibility :- It is a measure of cost involved in changing certain operational behaviour of the system. This cost is normally the NR. cost

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(vii) Maintainability :- It is the ability to make modifications & upgradations to the design of the ES.

(viii) Time to prototype :- It is the time taken by the designer to build a basic working version of the ES (PoC).

(ix) Time to market :- It is the time required to design system to make it available commercially.

(x) Safety :- It is an important aspect for design. It includes to check if ES has any adverse effects on operating environment.

- Design Trade-Offs -

① NRE cost - It is the non-recurring engineering cost. It is only one time cost including research, prototype preparing, PCB design cost.

② Size - Size of the system is measured in the terms of - Physical space required, memory capacity measured for S/W (bytes) & data, No of logic gates used in H/W.

③ Power - ES are powered by batteries. If power consumption is less, the battery lasts longer & hence, it is considered as a better system.

④ Performance - It is measured by time required to execute a task. Smaller the execution time, means higher performance.

These metrics typically compete with eachother. Improving one often leads to degrading another. For example, if we reduce the size of ES, it will affect the performance of system. If we reduce the power consumption of the system, the NRE cost can be affected. This phenomenon is compared to a wheel with three & pins called as design tradeoffs.

- Design Challenges -

Any ES when being designed, 3 factors are considered to be important including. Quality of the system, speed of the system & it's cost.

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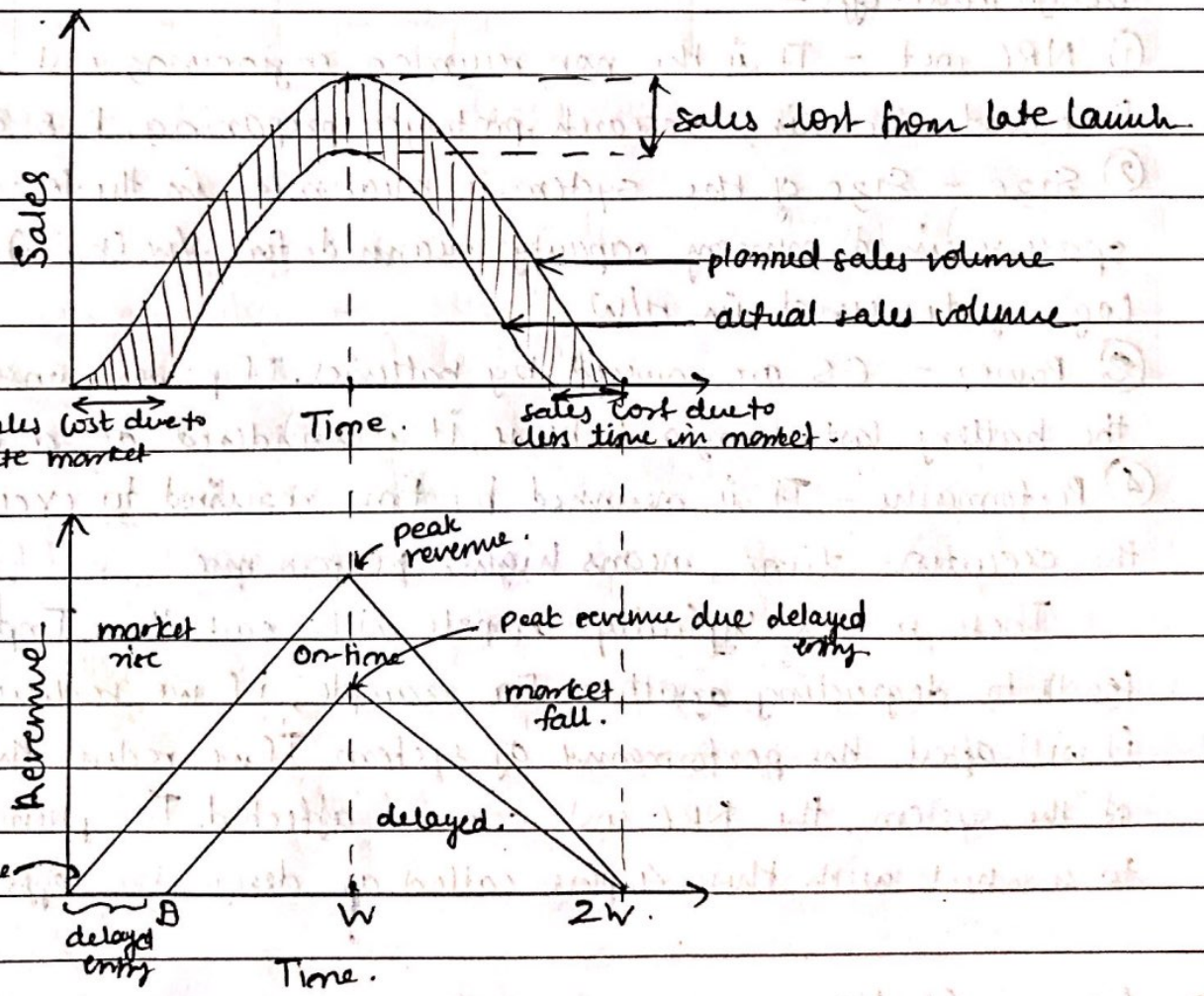
For any system, it's quality of the materials used and it's speed of execution should be as high as possible. If there were to be implemented, the overall cost of the system will increase which has to be avoided.

So, the designer has to design a system very efficiently where its quality & speed wont be compromised for reasonable cost. All the 3 factors will be perfectly balanced.

(Q2) (B) Product lifecycle curve on sales & revenue model.



In this model, the life cycle of a product right from its expected release to its end is described. The graphs describe and compare between the sales & revenue if the product was launched on the

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scheduled time & if it was released on delayed time. The loss of sales & revenue loss is also found out. Due to delayed launch, it is clear that revenue (peak value) is lot less & a loss is incurred.

product lifecycle = 2W

max sale at = W

Area of triangle = total revenue.

loss = Diff btwn the areas of expected & actual triangle.

$$\text{Area (on time)} = \frac{1}{2} \times 2W \times W = W^2$$

$$\text{Area (delayed)} = \frac{1}{2} \times (2W-D) \times (W-D)$$

$$\text{Loss} = W^2 - \frac{(2W-D)(W-D)}{2} = \frac{2W^2 - 2W^2 + 2WD + DW - D^2}{2}$$

$$\boxed{\text{Loss} = \frac{D(3W-D)}{2}}$$

$$\% \text{ revenue loss} = \frac{\text{delayed}}{\text{original}} \times 100 = \frac{D(3W-D)}{2 \times W^2} \times 100.$$

Choice A - C_{NRC} = 25,000/-, C_{unit} = 5000/-, time to market = 9 months.

Choice B - C_{NRC} = 45,000/-, C_{unit} = 3500/-, time to market = 8 months

Choice C - C_{NRC} = 36,000/-, C_{unit} = 4200/-, time to market = 7 months.

N = 10,000 units.

Choice A :	Choice B :	Choice C :
X = 25,000	X = 45,000	X = 36,000
Y = 5,000	Y = 3500	Y = 4200
Total cost = X + N.Y.	Total cost = X + N.Y.	total cost = X + N.Y
total cost = 5,00,25,000	total cost = 3,50,45,000	total cost = 4,20,36,000
Per unit cost = (X/N) + Y.	Per unit cost = (X/N) + Y	Per unit cost = (X/N) + Y
per unit cost = 5002.5	per unit cost = 3504.5	per unit cost = 4203.6

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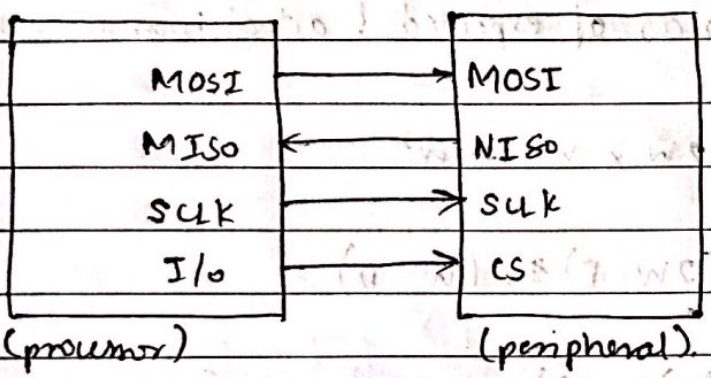
(Q3) (A) SPI & I2C interface to the processor.

→ SPI was developed by motorola. Peripheral devices such as memory chips, potentiometer, ADCs & DACs, real time clock are provided with SPI interface so that they can be interfaced to the processor. The processor generates the clock & the peripherals use the clok to synchronize its acquisition of data.



SPI use 4 types of signals for interfacing peripherals to processor -

(i) Master out slave in (MOSI)
(ii) Master in slave out (MISO)
(iii) Serial clock (SCLK)
(iv) Chip select (CS) [for peripherals].

SPI is based on master-slave protocol. Processor acts as the master and the peripherals act as a slave. Connection btwn both is done by these 4 signals. Both the master & slave contain shift registers. The master sends a byte to the slave on MOSI line & slave sends its register contents on MISO line. Both read & write can be simultaneously. If the master has to read a byte from the slave, it has to write a dummy byte to initialize the slave for transmission. This is a synchronous protocol for communication between the processor & peripherals.

→ I^2C bus used 2 wires for connecting devices. The bus is bidirectional and synchronous to a common clock, ucs with builtin I^2C are available

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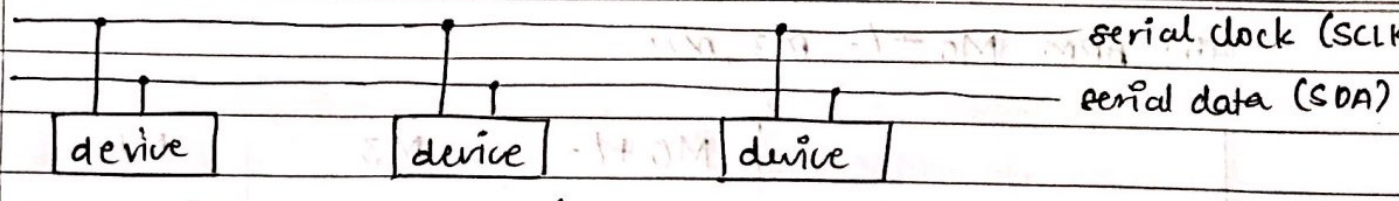

Data rates of 100 kbps (standard mode) & 400kbps (fast mode) are used.

The bus consists of 2 lines - serial clock & serial data. Both remain high when not in use. A device using the bus drives the line low. Each device has a unique address of 7bits or 10bits. If 7bits are used, 128 devices can be connected to the bus. A device acts as a master or a slave. Transmitting device is the master & the receiving device is the slave. The same line is used for master transmission & slave response. I2C bus is a multi-master bus more than that one device can act as a master. You can interface a RTC such as Philips PCF8353, a display of matrix.

(Q3) (B) (i) ARM 7, 9, 10, 11.

	ARM 7	ARM 9	ARM 10	ARM 11.
Pipeline depth	3 stage	5 stage	6stage	8-stage
typical clk frequency (mHz)	80	150	260	335
Power (mW/mHz)	0.06	0.19	0.50	0.040
Throughput (mIPS/mHz)	0.097	1.1	1.3	1.2
Architecture	Von Neuman	Harvard	Harvard.	Harvard.
Multiplier	8*32.	8*32.	16*32	16*32

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(ii) ARM M0 +/-, M3, M4.

	M0 +/-	M3	M4.	M0
Pipeline Depth.	2 stage	3 stage	3 stage	3 stage
Power (watts)	474	.141	151	66
Throughput (MIPS/mHz)	1.31	1.89	1.95	1.21
Architecture	ARMV6-M Von Neumann	ARMV7-M standard.	ARM-7M. Harvard.	ARMV6-M Von Neumann

(Q4) (A) Branch instructions & cond^n execution instruction

- Branch instruction

```
CMP   r5, #20
BNE   SKIP        { if zero flag is set }
---
---
SKIP : ADD r0, r5, r2, LSL #4.
```

- conditional execution inst^r.

```
CMP   r5, #20
ADDEQ r0, r5, r2, LSL #4
```

By comparing code density of case I & II, we can see that by using cond^n instruc^n, it requires less code/instructions which makes code more dense. Compare to branch instruction extra machine cycle gets wasted.

→ LDR r0, [r1, #4]

contents of r1 are added by 4 & stored in r0.

r0 = mem [r1 + 4]

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→ STR r0, [r1, #12]
stores the value found in r0 in the memory address found in r1 plus 12.
mem[r1+12] = r0.

→ LDR r0[r1, #4]!
used for auto indexing.
contents of r1 are added by 4, & value of r1 is incremented by 4 stored in r0.

→ STR r0 [r1, #12]!
stores value found in r0 in the memory address found in r1 plus 12 and then, r1 is incremented by 4.

→ LDR r0, [r1], #4
first, loads the contents of r1 into r0, increments r1 by 4.

→ STR r0, [r1], #12.
first, stores value found in r0 in the mem. addr found by r1, then increments r1 by 12.

→ LDRSH r0, [r1].
'SH' describes halfword.
2 bytes are transferred from memory addresses r1 to r0.

→ STRB r0, [r1]
'B' describes bytes.
1 byte is transferred from mem. addr r1 to r0.

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(Q4) (B) 8 stage pipeline

Stage delays – 15, 22, 26, 14, 19, 21, 12, 18 ns.

data items = 8000

latch delay = 6 ns. Highest stage delay = τ_m = 26 ns.

k = 8, N = 8000, d = 6 ns

- τ (clock period of pipeline) = $\tau_m + d$ = 26 ns + 6 ns

$\therefore$ $\boxed{\tau = 32\text{ ns}}$ //.

- T (time required to process data) = $[(k-1) + N] \times \tau$

$\therefore$ $T = (7 + 8000) \times 32\text{ ns}$.

$\therefore$ $T = 2.56 \times 10^{-4}$

$\therefore$ $\boxed{T = 256.22\text{ ms}}$ //.

- maximum clock freq^n (F) = $\frac{1}{\tau} = \frac{1}{32\text{ ns}}$

$\therefore$ $\boxed{F = 31.25\text{ MHz}}$ //.

(Q4) (C). mem loc^{n}s – 1000, 1004, 1008

data – 15, 18, 24

r1 = 1000 r2 = ?

~~r5 = 15~~

LDR r5, [r1]

LDR r6, [r1, #4]

LDR r7, [r1, #8]

ADD r2, r5, r6, LSL #3.

SUB r2, r2, r7, LSR #2.

(i) LDR r5, [r1].

r5 ← r1

$\therefore$ $\boxed{r5 = 15}$ // $\Longrightarrow$ r5 is loaded with value present in location pointed by r1.

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(ii) LDR r6, [r1, #4]

r6 ← [r1 + 4]. r1 + 4 = 1000 + 4 = 1004.

r6 ← [1004].

∴ **r6 = 18** ⟹ r6 is loaded with value present in location pointed by [r1 + 4].

(iii) LDR r7, [r1, #8]

r7 ← [r1 + 8] r1 + 8 = 1000 + 8 = 1008.

∴ r7 ← [1008].

∴ **r7 = 24** ⟹ r7 is loaded with value present in location pointed by [r1 + 8].

(iv) ADD r2, r5, r6, LSL #3

- firstly, r6 is left shifted by 3

r6 <<< 3.

r6 → 00000000 00000000 00000000 00010010

r6<<3 → 00000000 00000000 00000000 10010000

- then, r2 ← r5 + (r6 << 3).

r2 ← 15 + 144

r2 ← 159 //.

(v) SUB r2, r2, r7, LSR #2.

- firstly, r7 is right shifted by 2.

r7 >> 2

r7 → 00000000 00000000 00000000 00011000

r7>>2 → 00000000 00000000 00000000 00000110

- then, r2 ← r2 - (r7 >> 2)

r2 ← 159 - 6

r2 ← 153 //.

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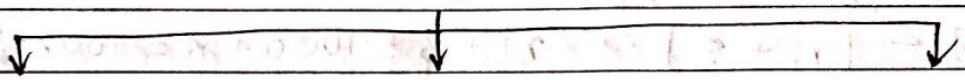
(Q1)(B) Services provided by an OS are -

(i) Proces / task management.
(ii) memory management.
(iii) I/o management + file system management.
(iv) providing services to appl^cs.
(v) Providing user interface to access OS via API.



Single task OS v/s multitask OS.	single user OS v/s multi user OS.	command v/s GUI.
→ msdos v/s windows & unix	mspos & windows v/s unix	MSDOS v/s windows & unix.

- Services required by an OS.

(i) Reliability (99.999% downtime per year).
(ii) multi-tasking with time constraints.
(iii) small footprint (No frills memory, hence, no GUI).
(iv) support diskless systems (no secondary storage).
(v) portability (variety of processors unlike intel).
(vi) scalability (8bit to 64 bit).
(vii) support for API (function calls) via POSIX.

* POSIX - portable O.S interface.

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