Cat No. 25-4113

Tandy MINI-PC

# Technical Reference Manual

TANDY®

Tandy 3000 NL Technical Reference Manual

Copyright 1988, Tandy Corporation
All Rights Reserved.

Reproduction or use of any portion of this manual, without express written permission from Tandy Corporation and/or its licensor, is prohibited. While reasonable efforts have been made in the preparation of this manual to assure its accuracy, Tandy Corporation assumes no liability resulting from any errors in or omissions from this manual, or from the use of the information obtained herein.

Tandy 3000 NL
Page Insertion Guide

Important Customer Note:

A gray stripe has been printed along the right edge of the title page of each of the sections to facilitate your finding the beginning of the section.

Also, a tabbed divider for each section has been provided for insertion at this point.

- Exploded view: Insert at the end of the Assembly/Disassembly section

- Foldout schematic pages: Insert at the end of the Main Logic Board section

| | |
|---|---|
| Schematics | C8000301 - Rev B<br>Sheets 1 of 11 thru 11 of 11 |
| Schematics | C8000301 - Rev D<br>Sheets 1 of 11 thru 11 of 11 |

- Foldout PCB art: Insert after the Main Logic Board schematics

| | |
|---|---|
| Layer Top Silkscreen<br>Layer 1 Top Side<br>Layer 2 GND Plane<br>Layer 3 + 5V Plane<br>Layer 4 Bottom Side | 1700377 - Rev B |
| Layer Top Silk Screen<br>Layer 1 Top Side<br>Layer 2 GND Plane<br>Layer 3 + 5V Plane<br>Layer 4 Bottom Side | 1700377 - Rev D |

- Foldout schematic pages: Insert at the end of the Power Supply section

| | |
|---|---|
| Schematic | Tandy Schematic SD1043 Rev D<br>Sheet 1 of 1 |
| Assembly Drawing | Assembly Dwg 1 of 2<br>and 2 of 2 |

- Foldout keyboard art pages: Insert after the Fujitsu Keyboard Assembly information in the Keyboard section

| | |
|---|---|
| Keyboard Unit Assembly | N860-4703-U001 |
| Block Diagram | 4700 |
| Circuit Specification | N86C-4700-0001 |
| Circuit Specification | N86C-4700-0101 |

- Foldout schematic page: Insert after the Fujitsu Custom IC Pin Signal sheet 2 of 3 in the Keyboard section

| | |
|---|---|
| Schematic | Fujitsu Custom IC Pin Signals & Function Sheet 3 of 3 |

- Exploded view of Parts Assembly location: Insert after the Section 4 Part Replacement portion of the Disk Drive section

- Foldout schematic page: Insert Circuit Diagram after the Overall Diagram (6-3) in the Disk Drive section

The Technical Reference Manual for the Tandy 3000 NL describes the computer hardware components and their relationships to one another, as well as the BIOS (Basic Input Output Services).

The information in this manual is intended for hardware and software designers, engineers, programmers, and anyone who requires an understanding of the design and operation of the computer.

The Tandy 3000 NL Technical Reference Manual is divided into two major sections, Hardware and Software. The hardware section provides information on system hardware architecture, including specifications, jumpers and switch settings, a theory of operation, schematics, and a devices section including timing diagrams. The hardware section is grouped into the following subsections:

| | |
|---|---|
| Introduction | Power Supply |
| Assembly/Disassembly | Keyboard |
| Main Logic Board | Disk Drive |
| Devices | |

The Software section contains information on system BIOS, scan codes, and other reference material needed for system assembly language programming. The software section is grouped into the following subsections:

A Quick Reference list of software interrupts
(for all device, I/O, and system status services)
Keyboard ASCII and scan codes
An MS-DOS memory map

The information in this manual is a supplement to and based on a working knowledge of the following literature:

The 3000 NL Installation and Operation Guide (Packaged with the computer)

The Intel 80286 Programing Reference Manual. Intel order number 210498-005

The Intel 80286 Hardware Reference Manual. Intel order number 210760-002

80286 Data Sheet. Intel order number 210253-012

This Intel literature may be ordered directly from Intel at the following number: 1-800-549-4725

## Table Of Contents


Introduction 1
System Assembly/Disassembly (Including Exploded Views) 3
Main Logic Board 5
- Specifications 6
- Switch Settings and Jumper Pin Configurations 7
- Theory of Operation 11
  - 80286 Processor (U13) 11
  - 80287 Numeric Processor (Optional) 12
  - Clock Generation 12
  - Command and Control Signals 13
  - Local Memory Expansion Board (Optional) 15
  - System Reset 18
  - Wait State and Ready Logic 18
  - NMI Logic and Port B Register 19
  - Address Buffers 19
  - Data Buffers and Conversion Logic 19
  - I/O Decode 20
    - Interrupt Controller 23
    - Timer/Counter 26
    - Real-time Clock 27
    - Floppy Disk Controller 28
  - Serial Interface 30
  - Parallel Interface 34
    - Parallel Connector Pin Assignments 36
  - Keyboard Control 36
  - Interface Requirements 41
    - PC Interface Compatibility 41
    - AT Interface Compatibility 44
  - Memory Map 47
  - I/O Port Map 48

# Introduction

## Introduction

The Tandy® 3000 NL is designed to be as compatible in both hardware and software as possible with the existing Tandy 3000 and the IBM PC AT®.

All operating systems and application programs that run on the Tandy 3000 run on this machine.

Certain hardware functions from the Tandy 3000 are duplicated on the Tandy 3000 NL. All I/O & memory maps, interrupts, DMA channels, and keyboard interface have the same configurations and timing parameters.

The Tandy 3000 NL is modular in design to allow maximum flexibility in system configuration. The computer consists of a main unit and a detachable keyboard with coiled cable. The main unit is supplied with one internal 3½-inch, 1.44 megabyte floppy disk drive. The standard types of monitors used with this Tandy 3000 NL are the monochrome, color RGB, VGA, and EGA monitors. Since these units are modular, you can place them on top of the main unit or at any convenient location.

The Tandy 3000 NL comes standard with 512K of system RAM, upgradable to 640K. You can expand local memory to 8 megabytes using the Tandy Local Memory Expansion board, which provides high speed 16-bit local memory on the Tandy proprietary memory bus, or by adding standard 16-bit memory expansion boards. By adding additional standard memory expansion boards, the system memory may be increased up to 16 megabytes; however, this does depend on the number of expansion slots that are available for use by standard memory expansion boards.

Other features include a parallel printer port, a serial port, and a speaker for audio output.

The main unit houses the main logic assembly, system power supply, and floppy disk drive. The main logic assembly is a large board mounted to the bottom of the main unit and interconnected to the keyboard, power supply, and disk drive by a series of cables.

The power supply is a 135W switching regulator type, designed to provide adequate power capacity for a fully configured system using all the option slots.

The floppy disk drive uses 3½-inch, double-sided, high-density 1.44M diskettes to read, write, or store data. These are soft sector diskettes. The floppy disk is also capable of reading and writing 720K formats. All system programs, with the exception of the system startup sequence, are stored on disk, or optional hard disk.

# Assembly/Disassembly

System Assembly/Disassembly (Including Exploded Views)

The following instructions explain how the major subassemblies are removed from the Tandy 3000 NL. Re-assembly of major sub-assemblies is accomplished by reversing the order of the removal procedures.

1. Top Cover Removal

a. Remove the (3) screws from the rear of the computer.

b. Slide the cover forward and off.

2. 3½-Inch Floppy Disk Removal

a. Remove the top cover.

b. Unplug all cables from the disk drive.

c. Remove the (3) screws attaching the drive to the drive mounting tower.

d. Slide the drive forward out of the drive mounting tower.

3. Power Supply Removal

a. Remove top cover.

b. Remove all cables from the main logic board and disk drives.

c. Remove the cable for the power on indicator, then remove the arm attached to the power supply switch.

d. Remove the (4) screws from the rear of the computer that secure the power supply to the rear of the machine.

e. Slide the power supply forward until clear of the restraining tab at the bottom of the machine and then up and out.

## 4. Main Logic Board Removal

a. Remove the top cover.

b. Unplug all cables and remove all the adapter boards from the system.

c. Remove the (2) screws holding the card guide in place and remove the card guide.

d. Remove the power supply.

e. Remove the (2) screws holding the serial/parallel connectors in place.

f. Remove the (10) screws holding the main logic board in place.

g. Remove the main logic board by lifting it straight up and out of the system to the left.

NOTE: BE CAREFUL OF THE CONNECTORS FOR THE KEYBOARD, MONITOR, SERIAL INTERFACE, AND PARALLEL INTERFACE WHEN REMOVING THE MAIN LOGIC BOARD.

MECHANICAL BILL OF MATERIAL - TANDY 3000 NL

## CHASSIS SUBASSEMBLY

| QTY | DESCRIPTION | PART NO. |
|---|---|---|
| 1 | WELDMENT - CHASSIS | 8729695 |
| 1 | CHASSIS | " |
| 1 | MOUNT - DISK DRIVE | " |
| 1 | SUPPORT - REAR - OPTION CARD | " |
| 1 | PANEL - CONNECTOR, KEYBD | " |
| 2 | CLIP - GROUNDING, RFI | 8529053 |
| 3 | FINGER CONTACT STRIP - 8 FINGERS | 8529065 |
| 7 | PANEL - OPTION SLOT COVER | 8729562 |
| 5 | FEET | 8719517 |
| 1 | SPEAKER SUBASSEMBLY | 889HL27 |
| 1 | SPEAKER | 8490010 |
| 1 | HARNESS | 8709800 |
| 15 | SCREW - #6-32 X 5/16 | 8569219 |
| | MOUNT SPEAKER - 2 SCREWS | |
| | MOUNT POWER SUPPLY - 4 SCREWS | |
| | MOUNT MAIN PCB - 9 SCREWS | |
| | MOUNT 3 1/2" DRIVE BRACKET - 2 SCREWS | |
| 1 | LOCK | 8739035 |
| | * C1091, 2 KEY PULLS AT 12 & 3 O'CLOCK, SATIN CHROME FINISH, NO CAM, 10 COMBINATIONS | |
| 1 | CAM MOUNT | 8729703 |
| 1 | CAM | 8719583 |
| 1 | ACTUATOR - KEYBOARD INHIBIT | 8729650 |
| 2 | POST - SUPPORT, MAIN PCB | 8589122 |
| 1 | GUIDE - CARD, OPTION | 8719534 |
| 1 | BATTERY ASSEMBLY - 3.6V | 8491007 |
| | ON DRIVE SUPPORT - PRODUCTION | |
| 1 | MAIN PCB ASSEMBLY | 889NL01 |
| 1 | SHROUD - I/O CONNECTOR | 8729706 |
| 4 | STANDOFF - #4-40 HEX | 8589070 |
| | MOUNT SHROUD TO MAIN PCB | |
| 2 | SCREW - #6-32 X 3/16 PPH | 8569103 |
| | SECURE SHROUD TO CHASSIS REAR WALL | |
| 1 | MOUNTING KIT - OPTIONAL DRIVES | 889MC16 |
| 4 | RAILS - DRIVE MOUNT | 8719603 |
| 8 | SCREW - #6-32 X 5/16 PPH ROLOK | 8569219 |
| | FOR MOUNTING 5 1/4" DRIVES TO RAILS | |
| 1 | BAG - 4 MIL POLY, 6" X 8" | 8590231 |
| 4 | CLIP-GROUNDING | 8529064 |

## FINAL ASSEMBLY

| QTY | DESCRIPTION | PART NO. |
|---|---|---|
| 1 | CHASSIS SUBASSEMBLY | |
| 1 | CASE TOP | 8729685 |
| 1 | BEZEL - FRONT | 8719609 |
| 2 | LENS | 8719560 |
| 2 | PIN - GUIDE | 8729705 |
| 1 | PANEL - DRIVE COVER (3 1/2") | 8719635 |
| | SNAPS INTO BLANK 3 1/2" FDD OPENING | |
| 1 | PANEL - FRONT, BLANK (5 1/4") | 8719608 |
| 1 | NAMEPLATE 25-4072 | 8719616 |
| 5 | SCREW - #6 X 3/8 PLASTITE, PPHD | 8569047 |
| | MT. FRONT BEZEL | |
| 2 | SCREW - #6 X 1/4 PLASTITE, PPHD | 8569309 |
| | MT. FRONT PANEL HEX WASHER HD. | |
| 3 | SCREW - #8-32 X 1/2 PPA | 8569338 |
| | MOUNT CASE TOP ASSY TO CHASSIS | |
| 1 | BUTTON - RESET | 8719615 |
| 1 | ACTUATOR - POWER SWITCH | 8719610 |
| 1 | BUTTON - POWER ACTUATOR | 8719611 |
| 1 | LED (GREEN) | 8469506 |
| 1 | CABLE - POWER LED | 8709864 |
| 1 | POWER CORD | 8709057 |
| 1 | POWER CORD - ENGLAND | 8709676 |
| 1 | POWER CORD - EUROPEAN | 8709677 |
| 1 | BAG - PLASTIC 4" X 12" | 8590077 |
| | POWER CORD - PROD | |
| 1 | BRACKET - 3 1/2" DISK DRIVE | 8729708 |
| 1 | LABEL-SERIAL/UL/FCC CLASS B/#25-4072 | 87891631 |
| | BOTTOM OF CHASS-PROD | |
| 1 | LABEL-SERIAL #25-4072 (CAN/INT'L) | 87891636 |
| | BOTTOM OF CHASSIS - PROD | |
| 1 | LABEL-CAUTION, OPTION BOARD (6 LANGUAGES) | 87891572 |
| | ALL UNITS-ON P.S.-PROD | |
| 1 | LABEL-CAUTION, ELECTRICAL SHOCK HEAT SINK | 87891569 |
| | INT'L ONLY - ON P.S. - PRODUCTION | |
| 1 | LABEL-SERVICE ADVISEMENTS (6 LANGUAGES) | 87891571 |
| | BEL.UNITS ONLY-ON P.S. PROD. | |
| 1 | LABEL-SERVICE ADVISEMENTS NOTES | 87891444 |
| | USA/CANADA UNITS-PROD ON POWER SUPPLY | |
| 1 | LABEL - WARNING, BATTER;Y (6 LANGUAGES) | 87891570 |
| | ALL UNITS - ON DRIVE SUPPORT - PROD. | |
| 1 | SOFTWARE PKG. | 8899069 |
| 1 | CARTON- DOM., PRINTED, CLAY WHT. | 8769452 |

## FINAL ASSEMBLY

| QTY | DESCRIPTION | PART NO. |
|---|---|---|
| 1 | CARTON - INT'L<br>BEL. & CANADA (TBP) - PRODUCTION | 8769451 |
| 1 | END CAP - LEFT | 8779315 |
| 1 | END CAP - RIGHT | 8779314 |
| 1 | BAG - PLASTIC, 19 X 19 X 7<br>FOR UNIT | 8590173 |
| 1 | BAG - DESICCANT | 8590209 |
| 1 | KEYBOARD | 8790575 |
| 1 | LABEL - SERIAL, KBD, USA<br>MT. TO KBD CASE BOTTOM | 87891628 |
| 1 | BAG - PLASTIC, 12 X 24 X 4MIL<br>FOR KDB - PROD (TBP) | 8590237 |
| 1 | PACKAGE - ERROR MAP<br>FOR PACKING LOCK KEYS (TBP) | 8590109 |
| 3 | SCREW - #6-32 X 3/16 PPH<br>MOUNT 3 1/2" FDD TO DRIVE MT | 8569171 |

## POWER SUPPLY SUBASSEMBLY

| QTY | DESCRIPTION | PART NO. |
|---|---|---|
| 1 | POWER SUPPLY - 135W | 8790094 |
| 1 | RECEPTACLE(AC IN)/EMI FILTR, SING. STAGE<br>MOUNT TO EMI SHIELD | 8519360 |
| 1 | MOUNT - POWER SWITCH | 8729701 |
| 1 | ENCLOSURE - UPPER | 8729697 |
| 1 | ENCLOSURE - LOWER | 8729698 |
| 1 | SWITCH - POWER | 8489112 |
| 2 | SCREW M3 X 5<br>MOUNT PWR SWITCH | 8569292 |
| 11 | SCREW #6-32 X 5/16 ROLOK, BRIGHT ZINC<br>MOUNT UPPER PS ENCLOSURE (4)<br>MOUNT EMI SHIELD (2)<br>MOUNT PS MAIN PCB (4)<br>MOUNT EMI PCB (1) | 8569219 |
| 2 | CABLE TIE 4" | 8559027 |
| 1 | BUSHING - STRAIN RELIEF | 8589134 |
| 1 | NUT - #6-32 KEPS<br>SECURE GROUND CABLE | 8579004 |
| 1 | SWITCH - INPUT VOLT SELECTOR | 8489103 |
| 4 | POP RIVETS - 1/8 DIA. CTSK HD.<br>MT. VOLTAGE SEL.SWITCH(2)<br>MT. POWER SWITCH MOUNT(2) | 8565028 |
| 1 | FAN SUBASSEMBLY<br>MT. TO UPPER ENCLOSURE - PROD. | 889HL36 |
| 4 | SCREW - #10-12 X 1/2 TAPIT BRIGHT ZINC<br>MT. FAN & GUARD TO UPPER P/S ENC. | 8569331 |
| 1 | FAN GUARD<br>MT TO UPPER ENC. | 8729655 |
| 1 | CLIP-CABLE ROUTING<br>ROUTE DC HARNESS - MT TO LOWER P/S ENC. | 8559087 |
| 1 | CLIP-CABLE ROUTING<br>ROUTE LED CABLE - MT TO UPPER P/S ENC. | 8559088 |
| 1 | SHIELD - EMI<br>MT BETWEEN MAIN P/S BD & EMI PCB | 8729718 |
| 1 | CABLE - POWER SWITCH TO AC IN | 8709866 |
| 1 | CABLE - AC IN TO GND | 8709865 |
| 2 | PATCH - COVER<br>COVER HOLES IN END OF LOWER ENC. | 87891660 |
| 1 | MASK - POWER-IN RECEPTACLE<br>MT TO RECEPTABLE - PRODUCTION | 8719586 |

## FAN SUBASSEMBLY 889HL36

| QTY | DESCRIPTION | PART NO. |
|---|---|---|
| 1 | FAN | 8790427 |
| 1 | CONNECTOR HOUSING | 8519331 |
| 2 | CONTACT PIN | 8529061 |

## 3 1/2" FLOPPY DISK DRIVE SUBASSEMBLY 889MC07

| QTY | DESCRIPTION | PART NO. |
|---|---|---|
| 1 | 3 1/2" DISK DRIVE 1.44 MB | 8790145 |
| 1 | BUTTON - DISK DRIVE EJECT | 8719597 |
| 1 | CABLE - INT. 34 POS, CONTROL | 8709845 |

Top Cover

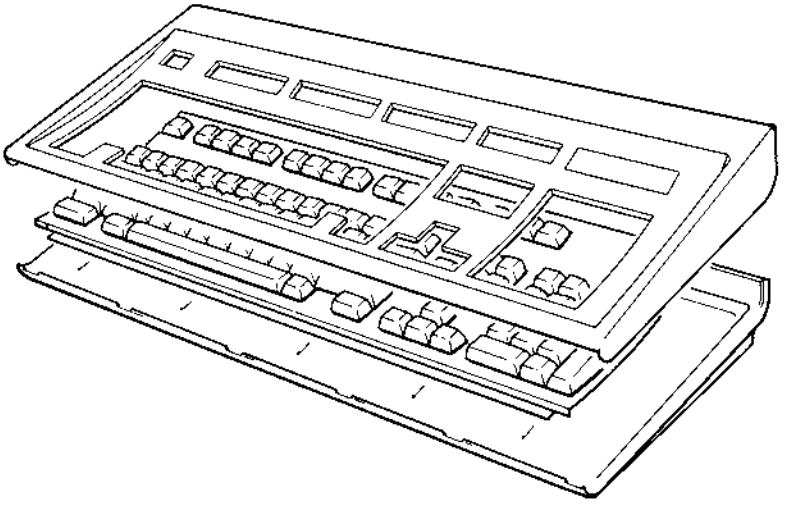
3½" Floppy Disk Drive

Power Switch Arm

Power Supply

Main Logic Board

Cover Mounting Screws



Main Logic Board

Main Logic Board

Specifications

Features

- 10 MHz one wait state 16-bit 80286 with on-board memory management and protection

- Standard 512K memory on the motherboard, expandable to 640K

  - Supports up to 8 megabytes of high speed 16-bit local memory using the Tandy Local Memory Expansion board.

  - Supports up to 16 megabytes of memory using standard 16-bit memory expansion boards. (Depending on the number of expansion slots available for use by standard 16-bit expansion boards).

  - Bus addressing supports PC(8-bit) and AT(16-bit) data widths

- Standard 1.44 megabyte 3½-inch floppy disk drive with on-board controller

  - Selectable 720K formats

  - Channel for additional internal floppy disk drive of 3½-inch or 5¼-inch type

- Channel for customer selectable fixed disk drive
  - Total of two channels

- Three IBM-PC® and four IBM-AT® compatible slots for standard peripherals as well as a proprietary RAM expansion slot

- True software compatibility with the IBM-AT in the single user MS-DOS® mode or multi-user protected mode

- Standard real-time clock with CMOS RAM and battery backup

- Standard serial/parallel ports

- Enhanced PC/AT-compatible keyboard

- Support for optional 80287 math coprocessor

- Standard 135-Watt power supply

## Specifications

### System Unit

| | |
|---|---|
| Processor | Intel 80286, 10 megahertz |
| Size | |
| Length: | 15 11/16-inch (39.78 cm) |
| Width: | 17-inch (43.18 cm) |
| Height: | 6 1/4-inch (15.88 cm) |
| Weight | |
| 38 lbs. Total | System unit, keyboard, power cord, mounting kit, manual, and packing material |
| 32.7 lbs. | System unit only one 1.44 megabyte, 3 1/2-inch diskette drive |
| Power Requirements | 105 - 130 VAC, 60 Hz (U.S.)<br>220 VAC, 50 Hz (International)<br>2.1 amps maximum current drain |
| Heat Output | 363 Btu/hr |
| Environment | |
| Air Temperature | |
| Operating | 13°C - 29°C (55°F - 85°F) |
| Storage | -40°C - 65°C (-40°F -149°F) |
| Humidity | |
| Operating | 20% to 80% (non-condensing) |
| Storage | 10% to 80% (non-condensing) |

Switch Settings and Jumper Pin Configurations

1. Video Monitor Type

| Configuration | Jumper Setting |
|---|---|
| Monochrome Video | E14-E15 |
| Color Video | E15-E16 |

2. BIOS ROM Type

| Configuration | Jumper Setting | |
|---|---|---|
| 128K (16K X 8) | E26-E27 | E29-E31 |
| 256K (32K X 8) | E26-E27 | E28-E29 |
| 512K (64K X 8) | E27-E30 | E28-E29 |

3. RAM Bank Select

| Configuration | Jumper Setting |
|---|---|
| Bank 0 On-board (512K) | E23-E24 |
| Bank 0 on Local Mem. Exp. Bd. (512K/2M) | E24-E25 |
| Bank 1 On-board (128K) | E21-E22 |
| Bank 1 on Local Mem. Exp. Bd. (512K/2M) | E20-E21 |

4. On-board Parallel Port

| Configuration | Jumper Setting | Dip Switch S1 |
|---|---|---|
| Parallel Port Enabled | N.A. | SW1 = ON |
| Parallel Port Disabled | N.A. | SW1 = OFF |
| Port One | N.A | SW1 = ON<br>SW2 = ON |
| Parallel Port Interrupt = IRQ7 | E12-E13 | N.A. |
| Port Two | N.A | SW1 = ON<br>SW2 = OFF |
| Parallel Port Interrupt = IRQ5 | E11-E12 | N.A. |

5. On-board Serial Port

| Configuration | Jumper Setting | Dip Switch HS1 |
|---|---|---|
| Serial Port Enabled | N.A. | SW3 = ON |
| Serial Port Disabled | N.A. | SW3 = OFF |
| Port One | N.A. | SW3 = ON<br>SW4 = ON |
| Serial Port Interrupt = IRQ4 | E8-E9 | N.A. |
| Port Two | N.A. | SW3 = ON<br>SW4 = OFF |
| Serial Port Interrupt = IRQ3 | E9-E10 | N.A. |

6. On-board Floppy Port

| Configuration | Jumper Setting | Dip Switch HS1 |
|---|---|---|
| Primary Port | N.A. | SW5 = ON |
| Secondary Port | N.A. | SW5 = OFF |

7. Numeric Processor (Optional) Clock Selection

| Configuration | Jumper Setting |
|---|---|
| 10 MHZ 80287 with optional 10MHZ, 33% duty-cycle Oscillator Effective Operation of 10 MHZ Tandy Options Kit Cat. No. 90-2192 | E2-E3 E4-E6 |
| 8 MHZ 80287 with on-board clock. Effective operation of 6.7MHZ | E1-E2 E6-E7 |

## 8. Summary - Standard Configuration as Shipped from Factory

| Configuration | Jumper Setting | Dip Switch HS1 |
|---|---|---|
| Video Monitor Type<br>Monochrome | E14-E15 | |
| BIOS ROM Type<br>128K (16K X 8) | E26-E27 E29-E31 | |
| DRAM Bank Select<br>Bank 0,1 On-board | E23-E24<br>E21-E22 | |
| On-board Parallel<br>Port 1 Enabled | N.A. | SW1 = ON<br>SW2 = ON |
| Parallel Port<br>Interrupt = IRQ7 | E12-E13 | |
| On-board Serial<br>Port 1 Enabled | N.A. | SW3 = ON<br>SW4 = ON |
| Serial Port<br>Interrupt = IRQ4 | E8-E9 | |
| On-board Floppy | N.A. | SW5 = ON |
| Numeric Processor<br>10MHZ OPTION KIT | E2-E3 E4-E6 | |

## 80286 Processor (U13)

Refer to the system block diagram and schematics during this discussion. For a more detailed description, refer to the individual device data sheets in the "Devices" section of this manual and device data sheets on the 80286 and 80287 available though Intel Corporation.

The 80286 (U13) is an advanced, high-performance, 16-bit microprocessor with special capabilities for multi-tasking and multi-user systems. The 80286, operating in real address mode, is compatible with existing 8086 and 8088 software and allows addressing of 1 megabyte of memory space.

The 80286 processor's data bus consists of the D0 - D15 bi-directional pins. These pins input data during memory, I/O, and interrupt acknowledge read cycles. These lines also output data during memory and I/O write cycles. The Address Bus consists of signals A0 - A23. These signals output the physical memory and I/O port addresses required by the system. The Bus Cycle Status signals (S0-,S1-) indicate the initiation of a bus cycle and, along with the M/(IO-) signal, define the type of bus cycle.

The Memory I/O Select signal M/I- distinguishes memory access from I/O access. If high during Ts, a memory cycle or halt/shutdown cycle is in progress. If low, an I/O cycle or an interrupt acknowledge cycle is in progress.

The Bus Ready (READY-) signal terminates a bus cycle. Bus cycles are extended without limit until the READY- signal goes low.

The Bus Hold Request input signal (HOLD) and Hold Acknowledge Output signal (HLDA) control ownership of the 80286 local bus. The HOLD signal allows another local bus master to request control of the bus. The Interrupt Request input signal (INTR) requests the 80286 to suspend its current program execution and service a pending external request. When the 80286 responds to an interrupt request, it performs two interrupt acknowledge bus cycles to read an 8-bit interrupt vector that identifies the source of the interrupt.

## 80287 Numeric Processor (Optional)

You can use this 40-pin dip as an option in the available socket on the main logic board. This part executes mathematical calculations independently allowing the CPU to perform other tasks. Incorporated into the 82C211 bus controller (U28) is the circuitry to interface an 80287 Numeric Processor to the 80286.

This circuitry handles the decoding required for selecting and requesting the Numeric Processor, handling BUSY-/ERROR- from the 80287 (U15) to the CPU, and generating error signals for error handling.

Intel Data Sheets providing a detailed explanation of the 80287 can be ordered through Intel.

A detailed description of interfacing the 80287 to the system can be found in the 82C211 Data Sheets in the "Devices" section of this manual.

## Clock Generation

Most of the clocks for the system are generated by the 82C211 bus controller (U28). The Bus Controller receives its input clocks from a 20 MHz TTL crystal oscillator and a 16 MHz crystal. The clock inputs are selectable by software.

In order to program the clock input, a write of 060H must be performed to I/O port address 022H, selecting the Clock Selector Register. The appropriate data must then be written to I/O port 023H for clock selection. For a detailed description of clock selection, refer to the CS8221 NEAT™ Chipset Bus Controller data sheets in the "Devices" section of this manual. (Section 1.4.)

The 20 MHz signal is applied to the CLK2IN pin of the 82C211 bus controller (U28). The 16 MHz crystal is tied to the ATCLK1 pin of the 82C211 (U28). The 82C211 (U28) generates the Processor Clock (PROCCLK) at 20 MHz and supplies it to the 80286 CPU (U13) and 82C212 memory controller (U36). The 82C211 also generates the SYSCLK signal at 8 or 10 MHz used to drive the SYSCLK line on the AT I/O bus.

A separate 14.31818 MHz crystal is provided as input (X1) for the 82C212 memory controller (U36). The 82C212 then provides the OSC clock on the system bus and the OSC/12 clock at 1.19 MHz for the system Interval Timer. The Real-time Clock and the Interval Timer are part of the 82C206 Integrated Peripherals Controller covered later in this manual.

NOTE: The Real-time Clock inside the 82C206 IPC (U41) uses a separate 32.968KHz clock oscillator for its reference clock, which can be adjusted by variable capacitor C182. (OSCI Pin 72)

## Command and Control Signals

Command and control signals for the system are generated by the 80286 CPU (U13), 82C211 bus controller (U28), and the 82C212 memory controller (U36). These signals are used to control data flow and direction, reading and writing of memory, input to and output from peripheral devices, and internal housekeeping within the system. The following sections describe briefly the functions of the above devices and their associated command and control signals. For a detailed description of the command and control signals used by each device, the CS8221 NEAT Chipset data sheets may be found in the "Devices" section of this manual.

Status lines S0- (Pin 5), S1- (Pin 4), and M/IO- (Pin 67) are used by the 80286 CPU (U13) to inform the 82C211 and 82C212 of the type of cycle the CPU is performing. The 82C211 bus controller (U28) also uses the signal HOLD (Pin 55) to inform the CPU when another Master, such as DMA or REFRESH, wishes to gain control of the local bus, and HOLDA (Pin 37) to inform the bus controller that the CPU has released control of the local bus to the requesting Master.

## Buffer Control

Data direction on the system bus is controlled by the 82C211 bus controller (U28) by generating the signals SDIR0 (Pin 34) and SDIR1 (Pin 36). These signals control the low and high byte data paths on the system bus. The bus controller also uses the ACEN- (Pin 47), AC0 (Pin 45), and AC1 (Pin 46) signals to control the size and byte assembly operations of the 82C215 data/address buffer (U27).

## Memory Control and Refresh

Memory control and refresh in the system is handled by the 82C211 bus controller (U28) and the 82C212 memory controller (U36). The bus controller uses the AF16- (Pin 78) signal to determine if the current cycle is a local bus cycle or an AT bus cycle.

The 82C212 memory controller (U36) generates the RAS (0-3-), CAS- (00-31-), and MWE- (Pin 28) signals necessary for DRAM access. READY- (Pin 29) is used by the memory controller to inform the 80286 CPU (U13) of the completion of a memory cycle. The 82C212 memory controller (U36) also generates the Data Latch Enable

(DLE) (Pin 45) and Data Read (DRD-) (Pin 33) signals needed to control the direction of data flow on the CPU Data bus and Memory Data bus.

## Memory Configuration Settings

An extensive set of registers are provided in the 82C212 memory controller (U36) to set up memory configuration. The definitions for those registers can be found in the CS8221 NEAT Chipset (Sect 2.3) data sheets in the "Devices" section of this manual.
NOTE: Not all memory configurations listed in the CS8221 data sheets are supported by the 3000NL. Refer to the memory configuration table in this section.

During a refresh cycle the bus controller will place the refresh address on the A0-A9 address lines and generate the Refresh (REF-) (Pin 58) signal to the 82C212 memory controller (U36) (Pin 20). The memory controller then uses these signals to generate the proper refresh address on the Memory Address lines MA0-MA9.

## DMA Control

DMA access in the system is controlled by the 82C211 bus controller (U28). In response to a DMA request (HRQ1) from the 82C206 (Pin 69), the bus controller will issue a HOLD signal (Pin 55) to the CPU. The CPU will acknowledge by sending a Hold Acknowledge (HLDA) (Pin 65) back to the controller and the bus controller will send HLDA1 (Pin 40) to the requesting device. At this time the requesting device has control of the CPU local bus until the HRQ1 signal is de-asserted.

The bus controller then issues the proper signals for bus sizing along with the ALE, ACEN-, and EALE- needed to control direction and data flow. A detailed description of DMA control may be found in the CS8221 NEAT Chipset and 82C206 data sheets in the "Devices" section of this manual.

## ROM Control

The 82C212 memory controller (U36) is responsible for generating the ROMCS- (Pin 13) signal necessary for ROM accesses. The 82C212 contains several configuration registers that may be programmed to use Shadow RAM, load ROM at different addresses in memory, and select the ROM segment size. The memory controller then generates the DRD- (Pin 33) and DLE (Pin 45) signals to gate the data onto the Memory Data bus (MD). At the end of the read, the memory

controller de-asserts AF16- (Pin 59) and asserts READY- (Pin 29) to inform the CPU of the completion of the cycle. (These options and how to program them is covered in the Chipset® CS8221 Data Book, Section 2.5. The data book can be found in the "Devices" section of this manual.)

Local Memory Expansion Board (Optional)

During the following discussion, please refer to the block diagram on the next page. The local memory expansion board allows the addition of high performance 16-bit memory on Tandy's proprietary local memory bus, without taking away any of the standard expansion slots. This memory is accessed at 10 MHz, 1 wait state (or less). The system can be upgraded to a total memory capacity of 8MB using this board. Only one of these boards may be installed per system. Additional 16-bit memory boards can also be installed in the expansion slots to achieve full 16MB memory capability per system. Note that some memory expansion boards may not operate at 10 MHz 1 wait state, but somewhat slower. It is therefore recommended that the Local Memory Expansion board be used where possible, or that the I/O channel speed be reduced from 10 MHz to 8 MHz through the system setup utility. Some early 16-bit Memory Expansion Boards made for the IBM-AT® will only function at the original AT bus speed of 6 MHz. These boards will not function in the Tandy 3000NL.

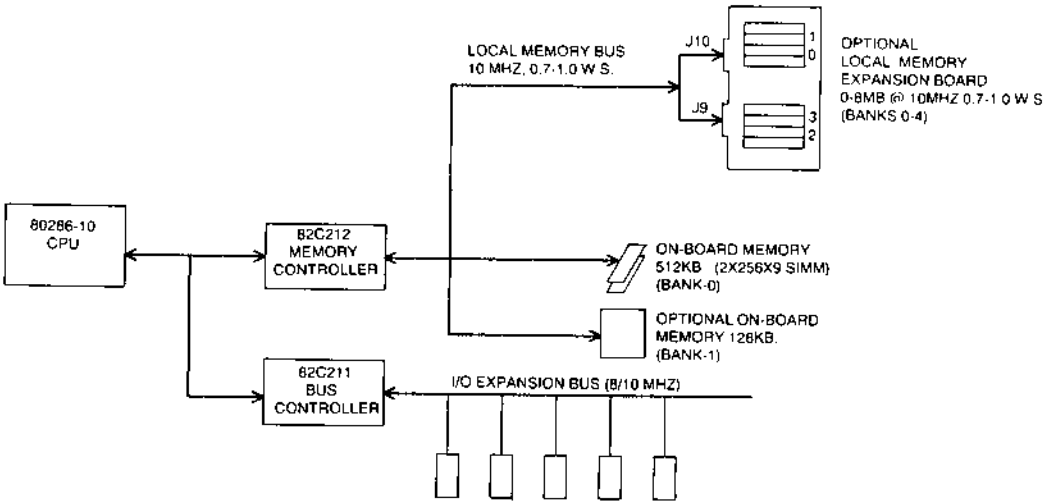
The local 16-bit memory bus can address up to four banks of memory. There are two banks (0,1) on the mother-board, which are also shared with the first two banks on local memory expansion board. Thus, these two banks can be enabled only at one place.

The table below describes the option jumpers on the mother-board to select the memory banks either on the mother-board or the memory expansion board.

| | BANK-0 | BANK-1 |
|---|---|---|
| MOTHER-BOARD (M.B.) | E23-E24 | E21-E22 |
| EXPANSION BOARD (EX.BD) | E24-E25 | E20-E21 |

The system comes equipped with 512K of memory in Bank 0 on the mother-board. An additional 128K (optional) may be installed in Bank 1, also on the mother-board. Each of the four banks on the expansion board may be installed with either 512K or 2M memory modules.

IMPORTANT NOTE: When using the Memory Expansion Board, move the SIMMs from the Main Board Memory Bank to the Expansion Memory Board Bank 0 and change the jumper accordingly.




BLOCK DIAGRAM - MEMORY ARCHITECTURE

The table below shows the memory configurations supported by Tandy Corporation.

| BANK 0 | | BANK 1 | | BANK 2 | BANK 3 | | |
|---|---|---|---|---|---|---|---|
| M.B. | EX.BD | M.B | EX.BD | EX.BD | EX.BD | TOTAL | OPT ON JUMPER |
| 512K | - | - | - | - | - | 512K | E23-E24 E21-E22 |
| 512K | - | 128K | - | - | - | 640K | E23-E24 E21-E22 |
| * - | 512K | - | 512K | - | - | 1.0 M | E24-E25 E20-E21 |
| - | 512K | 128K | - | 512K | 512K | 1.64M | E24-E25 E21-E22 |
| * - | 512K | - | 512K | 512K | 512K | 2.0 M | E24-E25 E20-E21 |
| - | 512K | 128K | - | 2.0M | 2.0M | 4.64M | E24-E25 E21-E22 |
| * - | 512K | - | 512K | 2.0M | 2.0M | 5.0 M | E24-E25 E20-E21 |
| * - | 2.0M | - | 2.0M | 2.0M | 2.0M | 8.0 M | E24-E25 E20-E21 |

* BEST PERFORMANCE (AVG. 0.7WS OR LESS)
CONFIGURATIONS UNMARKED WITH * PROVIDE 1WS OR LESS

\- BANK DISABLED: RAM UN-USABLE.

## Installing Additional RAM

Install the required number of Single-In-Line Memory Modules (SIMMs) on the expansion memory board. Ensure that the memory modules are fully plugged into the edge-card connectors on the memory board and snapped in place properly. The connectors assigned to each bank on the memory expansion board are as follows:

| | | | | | |
|---|---|---|---|---|---|
| BANK 0 | J3 | J4 | BANK 2 | J7 | J8 |
| BANK 1 | J1 | J2 | BANK 3 | J5 | J6 |

Set the bank-select jumpers on the mother board as discussed previously. Install the Expansion Memory Board in the proprietary Memory Expansion slot (nearest the power supply), with components on the Memory Board facing the power supply.

## System Reset

System reset may be accomplished in three ways. By depression of the reset switch, by entering a simultaneous Ctrl, Alt, and Del from the keyboard, and by the detection of an error which causes a shut down condition.

When the reset switch at the front of the system unit is depressed, a signal (RESET1-) is generated to the Bus Controller that causes the 82C211 to generate the RESET3 and RESET4 signals which clear and reset all of the system devices and controllers. When the system is reset from the keyboard or because of a shut down condition, only the RESET3 signal is generated to reset only the 80286 CPU (U13), allowing the other system devices and controllers to remain in their last state.

## Wait State and Ready Logic

Wait state generation in the system is handled by both the 82C211 bus controller (U28) and the 82C212 memory controller (U36). Both devices are programmable and can insert various numbers of wait states and command delays in CPU, memory, and I/O cycles.

Ready is generated to the CPU by the 82C211 bus controller (U28). The bus controller uses the READY- signal from the 82C212 memory controller (U36) to generate READY- to the CPU after a memory data transfer is complete. Command delays and wait states may be programmed into the 82C211 and 82C212 to delay the generation of READY- to the CPU. A detailed explanation of wait state programming, command delay programming, and ready logic can be found in the data sheets for the 82C211 and 82C212 in the "Devices" section of this manual.

Command Delay Register and Wait State Register definitions are located in Section 1.4 of the NEAT Chipset data sheets. DRAM Configuration Register definitions are located in Section 2.5 of the NEAT Chipset data sheets.

## NMI Logic and Port B Register

The 82C211 bus controller (U28) generates the NMI interrupt if it is enabled. NMI is generated in response to an I/O or Parity error in the system. To enable NMI, you must write to I/O Port 070H with data bit 7 set to a 0. To disable NMI, write to I/O Port 070H with bit 7 a 1.

The bus controller contains an AT-compatible configuration register called the Port B register. The following table gives the bit definitions for it:

| Port | Bit | Default | Type | Function |
|---|---|---|---|---|
| 61H | 7 | 0 | Read Only | System Parity Check |
| | 6 | 0 | Read Only | I/O Channel Check |
| | 5 | 0 | Read Only | Timer 2 Out |
| | 4 | 0 or 1 | Read Only | Refresh Detect |
| | 3 | 1 | R/W | Enable I/O Check |
| | 2 | 1 | R/W | Enable Parity Check |
| | 1 | 0 | R/W | Speaker Data |
| | 0 | 0 | R/W | Timer 2 Gate (speaker) |

Bit Definitions for Port B Register.

## Address Buffers

Address buffers and latches for the system are contained in the 82C215 Address/Data Buffer. CPU addresses A1-A16 are latched by the IALE signal to generate XA1-XA16. A detailed description of address buffers and latches can be found in the CS8221 NEAT Chipset data sheet in the "Devices" section of this manual.

## Data Buffers and Conversion Logic

The 82C215 data/address buffer (U27) provides buffering between the CPU data bus (D0-D15) and the memory data bus (MD0-MD15). Latching and enabling of the data is controlled by the DRD-, HLDA, AC0, and AC1 signals generated by the 82C211 bus controller (U28). 8- to 16-bit and 16- to 8-bit data conversion is also provided by the 82C215 in response to action codes (AC0, AC1) and the ACEN- signals from the 82C211 bus controller (U28). A detailed description of data buffers and conversion logic can be found in the data sheets on the 82C211 and 82C215 in the "Devices" section of this manual.

I/O Decode

The 82C206 IPC (Integrated Peripherals Controller) (U41) is a VLSI implementation of the standard peripherals required to implement an IBM-AT system board. This device contains the equivalent of:

- Two 8237A DMA controllers
- A 74LS612 address mapper
- Two 8259A interrupt controllers
- An 8254 counter/timer
- An MC146818 real-time clock with RAM

The IPC provides all the standard peripherals required for a system board implementation, except the keyboard interface controller.

DMA Controllers -- The two DMA controllers are connected in such a way as to provide four channels of DMA for 8-bit transfers and three channels of DMA for 16-bit transfers. (The first 16-bit DMA channel is used for cascading.)

Mapper -- Included as part of the DMA subsystem is the Page Register (DMAPAGE) device, which is used to supplement the DMA and drive the upper address lines when required.

Interrupt Controllers -- The IPC provides 16 channels of interrupt, partitioned into two cascaded controllers with eight inputs each. Three of the 16 channels are connected internally to various devices. The remaining 13 interrupt channels are user-definable.

The three internally connected channels are:

- Channel 0 - Counter/Timer Counter 0 Interrupt
- Channel 2 - Cascade to Slave Interrupt Controller
- Channel 8 - Real-time Clock Interrupt

Counter/Timer -- The counter/timer (CTC) subsystem contains three independent counters: Counters 0, 1, and 2. All three counters are driven from a clock input pin TMRCLK of 1.19 MHz and are independent from the other clock inputs to the device.

Counter 0 is internally connected to Interrupt 0 of the master interrupt controller. It is intended to be used as a multi-level interrupt to the system for such tasks as timekeeping and task-switching.

Counter 1 is connected to Refresh Request. It is programmed by BIOS to establish a 15 usec refresh rate.

Counter 2 is a full-function counter/timer that has a gate input for controlling the internal counter. You can use this counter as an internal counter, a timer, or a gated rate/pulse generator. It is also connected to the speaker and drives it when Port 61h Bit 1 is set.

Real-time Clock -- The real-time clock (RTC) subsystem contains a clock/calendar to maintain the real time and date and is driven by an external 32.768KHz clock oscillator. In addition, it contains 114 bytes of RAM. To keep the clock/calendar and RAM active when the system is turned off, the device is connected to an external battery.

For a detailed description of the 82C206 IPC, refer to the Data Sheet in the "Devices" section of this manual.

## General Overview

Interconnection and control of all the major subsystems is accomplished via a top-level control section. The IPC top-level control section provides eight separate enables to various subsystems of the device. The enabling of the IPC output buffers is also controlled by the top-level control section. The output buffers are enabled whenever an enable is generated to an internal subsystem.

The decode scheme employed in the IPC is designed to comply with the IBM-AT® requirements. The IPC does not respond to the unused address spaces established by the top-level control section. The extra peripherals can be tied directly to the data lines, because the IPC output buffers are not enabled unless an internal subsystem is enabled.

## Clock and Wait State Control

The clock and wait state control subsystem performs three functions:

1. Control of the DMA command width
2. Control of the CPU read or write cycle length
3. Selection of the DMA clock rate.

All these functions are user-selectable by writing to the Configuration Register located at Address 23H.

Writing and reading this register is accomplished by first writing a 01H to Location 22H to select the IPC Configuration Register and then performing either a read or write to Location 23H. The layout of Configuration Register 23H Index 01H and the explanation of the individual bits can be found in the data sheets on the 82C206 in the "Devices" section of this manual.

Configuration Register Defaults. The Configuration Register contents are pre-loaded by reset to an initial value of 0C0H. This value establishes a default that is compatible with the IBM-AT and corresponds to:

| | |
|---|---|
| Read/Write Cycles | 4 wait states |
| 16-Bit DMA Transfers | 1 wait state |
| 8-Bit DMA Transfers | 1 wait state |

Wait states are in increments of one SCLK cycle and are not affected by the DMA clock divider. DMAMEMR- is delayed one clock cycle later than XIOR-. The DMA clock is equal to SCLK/2.

## Description of DMA Controller Functions

As previously stated, the equivalent of two 8237A DMA controllers is implemented in the IPC. Each controller is a four-channel DMA device that generates the memory addresses and control signal necessary to transfer information directly between a peripheral device and memory. This allows high-speed information transfer with little CPU intervention.

The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals and three channels for transfers to 16-bit peripherals. DMA2 Channel 0 provides the cascade interconnection of the two DMA devices, thereby maintaining IBM-AT compatibility.

DMA cycle length control is provided internally in the IPC allowing independent control for both 8-bit and 16-bit cycles. This is done through the programmable registers, which can extend command signals or insert wait states.

The DMA subsystem can be programmed on a channel-by-channel basis to operate in one of four modes:

- Single Transfer Mode
- Block Transfer Mode
- Demand Transfer Mode
- Cascade Mode

## Description of Registers

Current Address Register -- Each DMA channel has a 16-bit Current Address Register that holds the address used during transfers. Each channel can be programmed to increment or decrement this register whenever a transfer is completed.

Current Word Count Register -- Each DMA channel also has a Current Word Count Register, which determines the number of transfers to perform. The actual number of transfers performed is one greater than the value programmed into the register.

Base Address Register -- Associated with each Current Address Register is a Base Address Register. This is a write-only register that is loaded by the CPU when writing to the Current Address Register. The purpose of the Base Address Register is to store the initial value of the Current Address Register for autoinitialization.

Base Word Count Register -- The Base Word Count Register preserves the initial value of the Current Word Count Register. It is also a write-only register that is loaded by writing to the Current Word Count Register. The Base Word Count Register is loaded into the Current Word Count Register during autoinitialization.

Command Register -- The Command Register controls the overall operation of the DMA subsystem. This register can be read or written by the CPU and is cleared by either a reset or a Master Clear command. The format and explanation of this register can be found in the data sheets on the 82C206 in the "Devices" section of this manual.

## Interrupt Controller

### Overview

Two interrupt controllers are included in the IPC. Each of the controllers is equivalent to an 8259A device operating in iAPX86 Mode. The two devices are connected and must be programmed to operate in Cascade Mode for proper operation of all 16 interrupt channels.

Interrupt controller 1 is located at Addresses 020h-021h and is configured for master operation in Cascade Mode. Interrupt controller 2 is a slave device and is located at Addresses 0A0h-0A1h. The interrupt request output signal from Interrupt controller 2 is internally connected to the Interrupt Request Input Channel 2 of Interrupt controller 1. The address decoding and cascade interconnection matches that of the IBM-AT.

Two additional interconnections are made to the interrupt request inputs of the interrupt controllers. The output of Timer 0 in the counter/timer subsystem is connected to Channel 0 of interrupt controller 1. Interrupt request from the real-time clock is connected to Channel 0 of interrupt controller 2.

When register addresses are used, the address for the interrupt controller 1 register is listed first and the address for the interrupt controller 2 register follows in parentheses, for example 020h (0A0h).

The following table defines the interrupt request sources:

| Controller | Channel No. | Interrupt Request Source |
|---|---|---|
| INTC1 | IR0 | IRQ0 - Counter/Timer Out0 |
| INTC1 | IR1 | IRQ1 - Keyboard |
| INTC1 | IR2 | IRQ2 - INTC2 Cascade |
| INTC1 | IR3 | IRQ3 - Bus, Often Serial Port 2/FDC 2 |
| INTC1 | IR4 | IRQ4 - Serial Port 1/FDC 2 |
| INTC1 | IR5 | IRQ5 - Bus, Often Parallel Port 2 |
| INTC1 | IR6 | IRQ6 - Diskette Controller |
| INTC1 | IR7 | IRQ7 - Parallel Port 1 |
| INTC2 | IR0 | IRQ8 - Real-time Clock IRQ |
| INTC2 | IR1 | IRQ9 - Software Redirected To IRQ2 |
| INTC2 | IR2 | IRQ10 - Reserved/Unused |
| INTC2 | IR3 | IRQ11 - Reserved/Unused |
| INTC2 | IR4 | IRQ12 - Reserved/Unused |
| INTC2 | IR5 | IRQ13 - 80287 Interrupt |
| INTC2 | IR6 | IRQ14 - Hard Disk Controller (16-bit) |
| INTC2 | IR7 | IRQ15 - Reserved/Unused |

Interrupt Request Sources.

## Programming the Interrupt Controller

Two types of commands are used to control the IPC interrupt controllers: initialization command words (ICWs) and operational command words (OCWs).

Initialization Command Words -- The initialization process consists of writing a sequence of four bytes to each interrupt controller. The initialization sequence is started by writing the first initialization command word (ICW1) to Address 020h (0A0h) with a 1 in Bit 4 of the data byte. The interrupt controller interprets this as the start of an initialization sequence and does the following:

Resets the Initialization Command Word Counter to 0.
Latches ICW1 to the device.
Selects Fixed Priority Mode.
Assigns IR7 the highest priority.
Clears the Interrupt Mask Register.
Sets the Slave Mode address to 7.
Disables Special Mask Mode.
Selects the Interrupt Request Register for status read operations.

The next three I/O writes to Address 021h (0A1h) load ICW2-ICW4. (All four bytes must be written for the controller to initialize properly.) You can terminate the initialization sequence at any point by writing to Address 020h (0A0h) with a 0 in Data Bit 4. Note that this causes OCW2 or OCW3 to be written.

Registers ICW1-ICW4 are write-only registers. For a detailed description of Initialization Command Words (ICWs), refer to the data sheets on the 82C206 IPC in the "Devices" section of this manual.

Operational Command Words -- Operational command words (OCWs) allow the IPC interrupt controllers to be controlled or reconfigured at any time while operating. Each interrupt has three operational command words, which can be programmed to affect the proper operating configuration, and a Status Register to monitor controller operation.

Operational Command Word 1 (OCW1) is located at Address 021h (0A1h). It can be written any time the controller is not in Initialization Mode. OCW2 and OCW3 are located at Address 020h (0A0h). Writing to Address 020h (0A0h) with a 0 in Bit 4 places the controller in Operational Mode and loads OCW2 (if Data Bit 3 = 0) or OCW3 (if Data Bit 3 = 1). Detailed descriptions for OCW1-OCW3 can be found in the data sheets on the 82C206 in the "Devices" section of this manual.

## Timer/Counter

The counter/timer circuit (CTC) in the IPC contains three 16-bit counters (Counters 0-2) that you can program to count in binary or binary-coded decimal (BCD). Each counter operates independently of the others and can be programmed as a timer or a counter. All three counters are driven from a common set of control logic. The control logic decodes control information written to the CTC and provides the control necessary to load, read, configure, and control each counter.

You can operate Counter 2 in any of the following six modes:

Mode 0 - Interrupt on Terminal Count
Mode 1 - Hardware-Triggered One-Shot
Mode 2 - Rate Generator
Mode 3 - Square Wave Generator
Mode 4 - Software-Triggered Strobe
Mode 5 - Hardware-Retriggerable Strobe

You can also program Counters 0 and 1 for all six modes. However, the usefulness of Modes 1 and 5 is limited because of the lack of an external hardware trigger signal.

All three counters are driven from a common clock input pin (TMRCLK Pin 23) that is independent from other clock inputs to the IPC. Counter 0's output is connected to IR0 of INTC1 and can be used as an interrupt to the system for keeping time and task switching. You can program Counter 1 to generate pulses or square waves for use by external devices. Counter 2 is a full-function counter/timer. You can use it as an interval timer, a counter, or a gated rate/pulse generator.

## Programming the CTC

After turning on the system, the condition of the CTC is undefined. Each counter must be programmed before it can be used. This is done either by the BIOS or by the software application.

Counters are programmed by writing a control word and then an initial count. The Control Register of a counter is written by writing to the Control Word address. The Control Register is a write-only location. The following table shows the addresses of the counter/timers and the Control Word Register:

| Address | Function |
|---|---|
| 040h | Counter 0 Read/Write |
| 041h | Counter 1 Read/Write |
| 042h | Counter 2 Read/Write |
| 043h | Control Register Write Only |

Control Word Addresses.

For a detailed description of programming the CTC, refer to the data sheets on the 82C206 in the "Devices" section of this manual.

Real-time Clock

This section of the IPC combines a complete time-of-day clock with alarm, 100-year calendar, programmable period interrupt, and 114 bytes of CMOS RAM. This section of the device can operate in a battery-powered mode to protect the contents stored in the SRAM and keep the clock functioning. The Alarm function is not implemented in the Tandy 3000 NL.

Register Access

Reading and writing to the 128 locations in the real-time clock is accomplished by first writing the index address out to 070H and then writing the desired data out to 071H. A complete description of how to program the RTC and access the CMOS configuration RAM can be found in the data sheets on the 82C206 IPC in the "Devices" section of this manual.

Time, Calendar, and Alarm Bytes

The CPU can obtain the time and calendar information by reading the appropriate locations in the real-time clock. Initialization of the time, calendar, and alarm information is accomplished by writing to these locations. Information is stored in these locations in binary-coded decimal format. The Alarm function is not implemented in the Tandy 3000 NL.

A complete description of programming and reading the RTC and CMOS RAM can be found in the data sheets on the 82C206 located in the "Devices" section of this manual.

## Floppy Disk Controller

The floppy disk controller resides on the main logic board and is located on the system data bus (SD0-SD15). It is a Western Digital WD37C65 integrated system (U10). It supports two 3½-inch or 5¼-inch drives through an internal, daisy-chained flat cable.

The controller supports data rates of 250K, 300K, or 500K. High- and low-capacity, 5¼-inch or 3½-inch floppy disk drives can be used on the same internal controller. The FDC interface uses the DMA (DRQ2-DACK2-) and interrupt request (IRQ6) controls from the system bus. The on-board controller can be strapped to either the primary (3F2-3F7 hex) or the secondary (372-377 hex) FDC port address. The control signals can be disabled through software, allowing two devices to share the same DMA and IRQ channels.

NOTE 1: If a separate floppy controller is installed on the expansion bus, as in the case of a combination floppy/hard disk controller, then the on-board controller must always be selected as the secondary port.

IMPORTANT NOTE 2: When using the above mentioned combination Floppy/Hard Disk Controller, the built-in 3½-inch 1.44 meg Floppy Drive becomes unuseable. This is due to the drive obtaining power from the system board via the flat ribbon cable.

## Host Interface

The host interface is the host microprocessor peripheral bus. This bus is composed of eight control signals and eight data lines. In either the Special or PC/AT Mode, IRQ and DMA requests are tri-stated and qualified by DMA enable (internally provided by the Operations Register). The data bus, DMA, and IRQ outputs are designed to handle 20 LSTTL loads. Inputs, except the data bus, are Schmitt Trigger receivers.

During the command or result phase, the Main Status Register must be read by the CPU before each byte of information is written into or read from the Data Register. After each byte is written into or read from the Data Register, the CPU should wait 12us before reading the Main Status Register.

Bits D6 and D7 in the Main Status Register must be 0 and 1, respectively, before each byte of the command word can be written into the FDC. Many of the commands require multiple bytes. As a result, the Main Status Register must be read prior to each byte transfer to the FDC.

During the result phase, Bits D6 and D7 in the Main Status Register must both be 1 before reading each byte from the Data Register. Note that this reading of the Main Status Register before each byte transferred to the FDC is required only in the command and result phases, not during the execution phase.

During the execution phase, the Main Status Register need not be read. If the FDC is in the Non-DMA Mode, the receipt of each data byte from the FDD is indicated by an interrupt signal on pin 16 (IRQ). The generation of a read signal (RD-) or write signal (WR-) clears the interrupt and outputs the data onto the data bus. The CPU can also poll the Main Status Register and Bit D7 (RQM) functions as the interrupt signal. If a write command is in process, the WR- signal performs the reset to the interrupt signal.

Note that in the Non-DMA Mode, it is necessary to examine the Main Status Register to determine the cause of the interrupt. It might be a data interrupt or a command interrupt, either normal or abnormal. If the FDC is in the DMA Mode, no interrupt signals are generated during the execution phase. The FDC generates DMA requests when each byte of data is available. The DMA controller responds to these requests with both the DACK- and RD- signal. When the DACK- signal goes low, the DMA Request (DMA) signal is cleared. If a write command has been issued, a WR- signal appears instead of the RD- signal. After the execution phase is completed, the terminal count occurs, or the EOT sector is read or written; an interrupt occurs (IRQ). This signifies the beginning of the result phase. When the first byte of data is read during the result phase, the interrupt is automatically cleared.

The RD- or WR- signals should be asserted while the DACK- signal is true. The CS- signal is used in conjunction with the RD- and WR- signals as a gating function during programmed I/O operations. CS- has no effect during DMA operations. It is very important to note that in the result phase all bytes must be read. The Read Data command, for example, has several bytes of data in the result phase. All seven bytes must be read to successfully complete the Read Data command. The FDC does not accept a new command until all seven bytes have been read. Other commands might require fewer bytes to be read during the result phase.

The FDC contains five status registers. The Main Status Register, mentioned previously, can be read by the processor at any time. The other four status registers (ST0, ST1, ST2, and ST3) are available only during a result phase and can be read only after completing a command. The particular command that is executed determines how many status registers are read.

## Commands

The FDC can perform 15 different commands. Each command is initiated by a multibyte transfer from the processor. The result after the execution of the command can also be a multibyte transfer back to the processor.

Command operation consists of three phases:

- Command Phase--The FDC receives all information required to perform a particular operation from the processor.
- Execution Phase--The FDC performs the operation as instructed.
- Result Phase--After completion of the operation, status and other housekeeping information are made available to the processor.

For a detailed description of registers, commands, and programming the Floppy Disk Controller refer to the WD37C65 data sheet in the "Devices" section of this manual.

## Serial Interface

The serial interface for the system is contained in VL16C451 Parallel/Asynchronous Communications Element (P/ALE) (U2). The VL16C451 is programmable and allows independent control of individual modem signals, data bit length, parity generation, and stop bit length. Complete status of the Asynchronous Communications Element can be read at any time by the CPU. A programmable baud rate generator is also provided. The following is a table of register bit definitions for the serial port. The first address is for the primary port, and the second address is for the secondary port:

| Address | Description |
|---|---|
| 03F8-03FF | Serial Port Primary (COM1) |
| 02F8-02FF | Serial Port Secondary (COM2) |

| Address | Description |
|---|---|
| 03F8(02F8) | Write Transmitter Holding Register (Character to Send) |

| Bit | Description |
|---|---|
| 0 | Bit 0 - LSB (First Bit Sent Serially) |
| 1 | Bit 1 |
| 2 | Bit 2 |
| 3 | Bit 3 |
| 4 | Bit 4 |
| 5 | Bit 5 |
| 6 | Bit 6 |
| 7 | Bit 7 - MSB |

03F8(02F8) Read Receiver Buffer Register (Character Received)

| Bit | Description |
|---|---|
| 0 | Bit 0 - LSB (First Bit Received Serially) |
| 1 | Bit 1 |
| 2 | Bit 2 |
| 3 | Bit 3 |
| 4 | Bit 4 |
| 5 | Bit 5 |
| 6 | Bit 6 |
| 7 | Bit 7 - MSB |

03F8(02F8) Divisor Latch LSB (Divisor Latch Access Bit DLAB ="1")

| Bit | Description |
|---|---|
| 0 | Bit 0 |
| 1 | Bit 1 |
| 2 | Bit 2 |
| 3 | Bit 3 |
| 4 | Bit 4 |
| 5 | Bit 5 |
| 6 | Bit 6 |
| 7 | Bit 7 |

| Address | Description |
|---|---|
| 03F9(02F9) | Divisor Latch MSB (Divisor Latch Access Bit DLAB ="1") |

| Bit | Description |
|---|---|
| 0 | Bit 0 |
| 1 | Bit 1 |
| 2 | Bit 2 |
| 3 | Bit 3 |
| 4 | Bit 4 |
| 5 | Bit 5 |
| 6 | Bit 6 |
| 7 | Bit 7 |

03F9(02F9) Interrupt Enable Register

| Bit | Description |
|---|---|
| 0 | "1" = Enables the Received Data Available Interrupt |
| 1 | "1" = Enables the Transmitter Holding Register Int |
| 2 | "1" = Enables Receive Line Status Interrupt |
| 3 | "1" = Enables the Modem Status Interrupt |
| 4-7 | Always Logical "0" |

03FA(02FA) Interrupt Identification Register

| Bit | Description | | |
|---|---|---|---|
| 0 | "0" = Interrupt Pending | | |
| 1-2 | Bit 2 | Bit 1 | |
| | "0" | "0" | Fourth Level Priority |
| | "0" | "1" | Third Level Priority |
| | "1" | "0" | Second Level Priority |
| | "1" | "1" | Highest Level Priority |
| 3-7 | Always Logical "0" | | |

| Address | Description |
|---|---|

03FB(02FB) Line Control Register

| Bit | Description | | |
|---|---|---|---|
| 0-1 | Bit 1 | Bit 0 | |
| | "0" | "0" | Five Bit Word Length |
| | "0" | "1" | Six Bit Word Length |
| | "1" | "0" | Seven Bit Word Length |
| | "1" | "1" | Eight Bit Word Length |
| 2 | "0" = One Stop Bit | | |
| | "1" = 1½ Stop Bits When Five Bit Length Selected | | |
| | Two Stop Bits With Six, Seven, or Eight Bit | | |
| 3 | "1" = Parity Enable | | |
| 4 | "0" = Odd Parity Select | | |
| | "1" = Even Parity Select | | |
| 5 | Stick Parity Bit | | |
| 6 | "1" = Set Break Enable | | |
| 7 | "1" = Divisor Latch Access Bit Enable | | |

03FC(02FC)

| Bit | Description |
|---|---|
| 0 | "1" = Data Terminal Ready Set (DTR) |
| | "0" = Data Terminal Ready Reset (DTR) |
| 1 | Request To Send (RTS) |
| 2 | Out 1 |
| 3 | Out 2 |
| 4 | Loop |
| 5-7 | Always Logical "0" |

03FD(02FD) Line Status Register

| Bit | Description |
|---|---|
| 0 | Data Ready (DR) |
| 1 | Overrun Error (OR) |
| 2 | "1" = Detect Parity Error (PE) |
| 3 | "1" = Detect Framing Error (FE) |
| 4 | "1" = Break Interrupt (BI) |
| 5 | Transmitter Holding Register |
| | "1" = Character Transferred From Holding To Shift Register |
| | "0" = Loading Transmitter Holding Register |
| 6 | Transmitter Shift Register Empty |
| | "1" = Shift Register Idle |
| | "0" = Data Transfer From Holding Register |
| 7 | Always Logical "0" |

| Address | Description |
|---|---|
| 03FE(02FE) | Modem Status Register |

| Bit | Description |
|---|---|
| 0 | Clear to Send (DCTS) |
| 1 | Data Set Ready (DDSR) |
| 2 | Trailing Edge Ring Indicator<br>"1" = On<br>"0" = Off |
| 3 | Delta Received Line Signal Detect (If Bit 0, 1, 2, or 3 is set to a "1" modem status interrupt is generated |
| 4 | "0" = Clear to Send (CTS) |
| 5 | "0" = Data Set Ready (DSR) |
| 6 | "0" = Ring Indicator (RI) |
| 7 | "0" = Received Line Signal Detect (RLSD) |

For a complete description of the VL16C451, refer to the data sheet on the VL16C451 in the "Devices" section of this manual.

Serial Port Connector

The nine pin D-sub serial port connector pinout is shown below.

| Pin Number | RS-232-C Signal | (Abbreviate) |
|---|---|---|
| 1 | Carrier Detect | (DCD) |
| 2 | Received Data | (RD) |
| 3 | Transmitted Data | (CD) |
| 4 | Data Terminal Ready | (DTR) |
| 5 | Signal Ground | (GND) |
| 6 | Data Set Ready | (DSR) |
| 7 | Request to Send | (RTS) |
| 8 | Clear to Send | (CTS) |
| 9 | Ring Indicator | (RI) |

9 Pin RS-232-C Pin Arrangement

Parallel Interface

The parallel interface for the system is also contained in the VL16C451 P/ALE (U2). It provides a bi-directional parallel data port that is fully Centronics® compatible. The following is a table of register bit definitions for the parallel port. The first address is for the primary printer port, the second is for the secondary port:

| Address | Description |
|---|---|
| 0378(0278) | Printer - Data Latch |

| Bit | Description |
|---|---|
| 0 | Bit 0 - LSB |
| 1 | Bit 1 |
| 2 | Bit 2 |
| 3 | Bit 3 |
| 4 | Bit 4 |
| 5 | Bit 5 |
| 6 | Bit 6 |
| 7 | Bit 7 - MSB |

| Address | Description |
|---|---|
| 0379(0279) | Printer - Read Status |

| Bit | Description |
|---|---|
| 0 | Not Used |
| 1 | Not Used |
| 2 | Not Used |
| 3 | "0" = Error |
| 4 | "1" = Printer Select |
| 5 | "1" = Out of Paper |
| 6 | "0" = Acknowledge |
| 7 | "0" = Busy |

037A(027A) Printer - Control Latch

| Bit | Description |
|---|---|
| 0 | "1" = Strobe - Low to high latches character, High to low prints character |
| 1 | "1" = Auto FD XT |
| 2 | "0" = Initialize |
| 3 | "1" = Select Printer |
| 4 | "1" = Enable Interrupt |
| 5 | "0" = Direction Control<br>0 = Enable Output Data<br>1 = Enable Input Data |
| 6 | Not Used |
| 7 | Not Used |

A complete description of the parallel port and its registers can be found in the data sheet on the VL16C451 in the "Devices" section of this manual.

Parallel Connector Pin Assignments

| Pin Number | Signal Name |
|---|---|
| 1 | Strobe |
| 2 | Data Bit 0 |
| 3 | Data Bit 1 |
| 4 | Data Bit 2 |
| 5 | Data Bit 3 |
| 6 | Data Bit 4 |
| 7 | Data Bit 5 |
| 8 | Data Bit 6 |
| 9 | Data Bit 7 |
| 10 | ACKNOWLEDGE |
| 11 | BUSY |
| 12 | PAPER END |
| 13 | SELECT |
| 14 | AUTO FEED |
| 15 | ERROR |
| 16 | INITIALIZE |
| 17 | SELECT IN |
| 18-25 | GROUND |

Keyboard Control (Ports 60, 64)

The keyboard controller, (U14), is a single-chip microcomputer (8042) that is programmed to be IBM-AT compatible.

The controller receives serial data from the keyboard (Port 60), checks the parity of the data, translates scan codes, and presents the data to the system as a byte of data in its output buffer. The controller interrupts the CPU when data is available to be read.

Data is sent to the keyboard by writing to the controller's input buffer at Port 60. (Status Register bits inform the CPU of any error encountered in receiving the data.) The byte of data is serialized and sent to the keyboard, with odd parity bits automatically inserted. The keyboard acknowledges all data transmissions with an acknowledgment response, hex FA.

The keyboard sends serial format data to the controller, using an 11-bit frame. (Data sent is synchronized by a keyboard-supplied clock.) The first bit is a start bit. It is followed by 8 data bits, an odd parity bit, and a stop bit. At the end of a transmission, the controller disables the interface until the system accepts the data byte.

For a received byte of data with a parity error, a resend command is sent to the keyboard.

Whenever the controller is unable to receive the data correctly, FF hex is placed in its output buffer, and the parity bit in the Status Register is set to 1.

The controller also times a byte of data from the keyboard, and if the byte transmission does not end within 2 milliseconds, FF hex is placed in the controller's output buffer, and the receive time-out bit in the Status Register is set. (No retries are attempted on a receive time-out error.)

For scan codes received from the keyboard, the controller converts these codes to system scan codes before they are put into the controller's output buffer.

Data is sent to the keyboard in the same serial format used to receive data from the keyboard. If the keyboard does not start clocking the data out of the controller within 15 milliseconds or if it completes that clocking within 2 milliseconds, FE hex is placed in the controller's output buffer, and the transmit time-out error bit is set in the Status Register.

If the response contains a parity error, FE hex is placed in the controller's output buffer, and the transmit time-out and parity error bits are set in the Status Register. The controller is programmed to a set time limit for the keyboard to respond. After more than 25 milliseconds, the controller places FE hex in its output buffer and sets the transmit and receive time-out error bits in the Status Register. (No retry is made by the controller for any transmission error.)

A fuse has been provided for pin 5 of the keyboard connector for use in an international unit only.

**Status Register Bit Definitions (Port 64)**

The status register may be read at port address hex 64 and the bit definitions are as follows:

<u>Bit 0, Output Buffer Full</u> - When this bit is a 0 it indicates that the output buffer is empty. A 1 indicates that there is data in the output buffer but the system has not yet read the data. When the system does read the data this bit is returned to a 0.

<u>Bit 1, Input Buffer Full</u> - A 0 in this position means the input buffer at I/O address 60h or 64h is empty. A 1 indicates that data has been written into the buffer but the controller (8042) has not read it yet. When the data is read by the controller this bit returns to a 0.

<u>Bit 2, System Flag</u> - This bit may be set to 0 or 1 by writing to the flag bit in the controller's command byte. It is set to 0 on power up reset.

Bit 3, Command/Data - The input buffer may be addressed as I/O address 60h or 64h. Address 60h is defined as a data port while address 64h is a command port. Writing to address 64h sets this bit to a 1, and writing to address 60h sets it to 0. The controller uses this bit to determine if the byte in the input buffer is a data or command byte.

Bit 4, Inhibit Switch - This bit is updated when data is placed in the output buffer. It reflects the state of the keyboard inhibit switch. A 0 in this bit means the keyboard is inhibited.

Bit 5, Auxiliary Output Buffer Pull - A 1 in this bit indicates that a transmit by the keyboard controller was not properly completed.

Bit 6, General Time Out - A 1 indicates that a transmission was started by the keyboard but did not finish within the programmed time limit.

Bit 7, Parity Error - A 0 indicates the last byte received from the keyboard had odd parity. A 1 indicates the last byte received had even parity. The keyboard should send data with odd parity.

Keyboard Controller Command Set (Port 64)

20-3F -- Read Keyboard Controller's RAM. Bits D5-D0 specify address.

20 -- Read Keyboard Controller's Command Byte. The controller sends the current command byte to the output buffer.

60-7F -- Write Keyboard Controller's RAM. Bits D5-D0 specify address.

60 -- Write Keyboard Controller's Command Byte. The next byte of data written to I/O address 60h is put in the controller's command byte. Bit definitions for the command byte are as follows:

Bit 7 - Reserved. Should be a 0.

Bit 6 - IBM Personal Computer Compatibility Mode.

Writing a 1 to this bit causes the controller to convert the scan codes it receives to those used by the IBM Personal Computer.

Bit 5 - IBM Personal Computer Mode.

Writing a 1 to this bit programs the keyboard to support the IBM Personal Computer keyboard interface. The controller will not check parity or convert scan codes.

Bit 4 - Disable Keyboard.

Writing a 1 to this bit disables the keyboard interface by driving the clock line low. Data is not sent or received.

Bit 3 - Inhibit Override.

A 1 in this bit disables the keyboard inhibit function.

Bit 2 - System Flag.

The value written to this bit is put in the system flag bit of the status register.

Bit 1 - Reserved. Should be written to a 0.

Bit 0 - Enable Output Buffer Full Interrupt.

Writing a 1 to this bit causes the controller to generate an interrupt when it places data into the output buffer.

A4 -- Test Password. This command checks if there is a password currently installed in the 8042. The test result is placed in the output buffer (I/O Address 060h). A hex FA means the password is installed. An F1 means no password is installed.

A5 -- Load Security. This command starts the load password procedure. Following this command, the 8042 will input from the data port until a null (0) is detected, which terminates the password entry.

A6 -- Enable Security. This command enables the 8042 security feature. This command is only valid when a password pattern is currently loaded into the 8042.

A7 -- Disable Auxiliary Device Interface. This command sets Bit 5 of the 8042 command byte. This disables the auxiliary device and data is not sent or received.

A8 -- Enable Auxiliary Device Interface. This command clears Bit 5 of the 8042 command byte. This releases the auxiliary device interface.

A9 -- Interface Test. This command causes the 8042 to test the auxiliary device clock and data lines. The test result is placed in the output buffer (I/O Address 060h). The test results are as follows:

00 - No Error
01 - Auxiliary device clock line stuck low
02 - Auxiliary device clock line stuck high
03 - Auxiliary device data line stuck low
04 - Auxiliary device data line stuck high

AA -- Self Test. Causes the controller to perform internal diagnostics. 55h is placed in the output buffer if no errors are encountered.

AB -- Interface Test. Causes the controller to test the clock and data lines. The result is placed in the output buffer as follows:

00 - No error detected
01 - Clock line stuck low
02 - Clock line stuck high
03 - Data line stuck low
04 - Data line stuck high

AC -- Diagnostic Dump. Sends 16 bytes of the controller's RAM, current state of the input port, current state of the output port, and the controller's program status word to the system. All items are sent in scan code format.

AD -- Disable Keyboard Feature. This sets Bit 4 of the controller's command byte. This disables keyboard interfacing by driving the clock line low. Data will not be sent or received.

AE -- Enable Keyboard Interface. This command clears Bit 4 of the command byte. This releases the keyboard interface.

C0 -- Read Input Port. Tells the controller to read the input port and place the data in the output buffer. This command should be used only if the output buffer is empty.

C1 -- Poll Input Port Low. Port 1 Bits 0-3, in Status Bits 4-7.

C2 -- Poll Input Port High. Port 1 Bits 4-7, in Status Bits 4-7.

D0 -- Read Output Port. Causes the controller to read the output port and place the contents in the output buffer. This command should only be used if the output buffer is empty.

D1 -- Write Output Port. The next byte of data written to I/O address 60h is placed in the output port. Note that Bit 0 of the controller's output port is connected to system reset and should not be written low.

E0 -- Read Test Inputs. This causes the controller to read its T0 and T1 inputs. The data is placed in the output buffer with data Bit 0 representing T0 and data Bit 1 representing T1.

F0-FF -- Pulse Output Port. Bits 0-3 of the controllers output port may be pulsed low for approximately 6usec. Bits 0-3 of this command indicate which bits are to be pulsed. A 0 causes the bit to be pulsed, and a 1 causes the bit not to be pulsed. Note that Bit 0 of the controller's output port is connected to system reset and should not be written low.

## Interface Requirements

### System I/O Bus Interface

This section identifies the I/O interface requirements for both the PC-compatible option cards and the AT-compatible option cards. There are eight expansion slots in the Tandy 3000 NL -- two slots are PC-type slots having one 62 position connector, and six are AT-type slots having one 62 and one 36 position connector.

### PC Interface Compatibility

The following connector pin assignments are used on both the PC and the AT option slots for the 62 position connector.

| PIN | SIGNAL NAME | PIN | SIGNAL NAME |
|---|---|---|---|
| A1 | IOCHCK- | B1 | Ground |
| A2 | SD7 | B2 | RESETDRV |
| A3 | SD6 | B3 | +5 V |
| A4 | SD5 | B4 | IRQ9 |
| A5 | SD4 | B5 | -5 V |
| A6 | SD3 | B6 | DRQ2 |
| A7 | SD2 | B7 | -12 V |
| A8 | SD1 | B8 | OWS- |
| A9 | SD0 | B9 | +12 V |
| A10 | BIOCHRDY | B10 | Ground |
| A11 | AEN | B11 | SMEMW- |
| A12 | SA19 | B12 | SMEMR- |
| A13 | SA18 | B13 | IOW- |
| A14 | SA17 | B14 | IOR- |
| A15 | SA16 | B15 | DACK3- |
| A16 | SA15 | B16 | DRQ3 |
| A17 | SA14 | B17 | DACK1- |
| A18 | SA13 | B18 | DRQ1 |
| A19 | SA12 | B19 | REF- |
| A20 | SA11 | B20 | SCLK |
| A21 | SA10 | B21 | IRQ7 |
| A22 | SA9 | B22 | IRQ6 |
| A23 | SA8 | B23 | IRQ5 |
| A24 | SA7 | B24 | IRQ4 |
| A25 | SA6 | B25 | IRQ3 |
| A26 | SA5 | B26 | DACK2- |
| A27 | SA4 | B27 | T/C |
| A28 | SA3 | B28 | BALE |
| A29 | SA2 | B29 | +5 V |
| A30 | SA1 | B30 | OSC |
| A31 | SA0 | B31 | Ground |

PC Bus Pin Definitions

The following signal descriptions for the System I/O Bus are for PC and AT bus-compatible option cards. Note that all signal lines are TTL compatible levels and that I/O adapters should be designed with a maximum of two low power Shottky (LS) loads per line.

SCLK (B20). SCLK is the System clock. It has a 50% duty cycle and is used only for synchronization with the CPU. It is not intended for uses requiring a fixed frequency.

SA0 through SA19 (A12-A31). These lines are 20 address bits used to address memory and I/O devices within the Tandy 3000. They are gated on the system bus when the BALE signal is high and are latched on the falling edge of the BALE signal. Generation of these signals is accomplished by the CPU or a DMA controller. SA0-SA19 are active high.

BALE (B28). BALE is a Buffered Address Latch Enable generated by the CPU Bus Controller. It is used to latch valid addresses from the CPU, and can be used by an I/O board to indicate a valid CPU address, in conjunction with AEN. BALE is pulled to a high state during DMA cycles, which include Refresh cycles. BALE is active high.

AEN (A11). AEN is an Address Enable signal used to remove the CPU and other devices from the bus to allow DMA transfers to take place. During AEN active, the DMA controller has control of the address bus, the data bus, the READ command lines, and the WRITE command lines. AEN is active high.

SD0 through SD7 (A2-A9). These signals are the data bus bits 0 through 7 from the CPU to memory and I/O devices on the bus. SD0 is the least significant bit (lsb), and SD7 is the most significant bit (msb).

RESETDRV (B2). RESETDRV is used to reset or initialize the expansion logic during power-up time, line voltage outage, or when the Reset switch on the front panel is pressed. BRESETDRV is active high.

IOCHCHK- (A1). This signal indicates an uncorrectable system error when active. The IOCHCHK- signal provides the system board with parity information about memory or devices on the bus. IOCHCHK- is active low.

BIOCHRDY (A10). This signal is used to lengthen I/O or memory cycles when driven low by the active device. (This signal should not be held low more than 15 microseconds.) Any slow device using this line should drive it low immediately upon detecting its valid address and a READ or WRITE command. See the timing diagram for setup times. BIOCHRDY is active high (Ready condition).

IRQ9 and IRQ3 through IRQ7 (B4, B21-B25). These signals are used to tell the CPU that an I/O device needs attention. The Interrupt Requests are prioritized with IRQ2 having the highest priority and IRQ7 the lowest. An Interrupt Request is generated when any IRQ signal is driven high and held high until the CPU acknowledges the interrupt.

IOR- (B14). IOR- is a read signal that instructs an I/O device to drive its data onto the data bus (SD0-SD7). This line can be driven by the CPU Bus Controller or by the DMA controller. IOR- is active low.

IOW- (B13). IOW- is a write signal that instructs an I/O device to read, or latch, the data from the data bus (SD0-SD7). This line can be driven by the CPU Bus Controller or by the DMA controller. IOW- is active low.

SMEMR- (B12). SMEMR- is a read signal that instructs a memory device to drive its data onto the data bus (SD0-SD7). This line can be driven by the CPU Bus Controller or by the DMA controller through the CPU Bus Controller. SMEMR- is active only when the memory address is within the first 1 megabyte range (000000-0FFFFFH). SMEMR- is active low.

SMEMW- (B11). SMEMW- is a write signal that instructs a memory device to read or latch the data from the data bus (SD0-SD7). This line can be driven by the CPU Bus Controller or by the DMA controller through the CPU Bus Controller. SMEMW- is active only when the memory address is within the first 1 megabyte range (000000-0FFFFFH). SMEMW- is active low.

DRQ1, DRQ2, and DRQ3 (B18, B6, B16). These lines are asynchronous DMA requests by peripheral devices to gain DMA service. They are prioritized with DRQ1 having the highest priority, DRQ2 next, and DRQ3 lowest. A DMA request is generated by driving a DRQ line active high and holding it until the corresponding DACK (DMA acknowledge) signal goes active. DRQ1, DRQ2, and DRQ3 perform only 8-bit transfers. All DRQ lines are active high.

DACK1-, DACK2-, and DACK3- (B17, B26, B15). These lines are DMA acknowledge signals used to acknowledge DMA requests DRQ1, DRQ2, and DRQ3. All DACK signals are active low.

REF- (B19). This signal is used to indicate a refresh cycle that can be used by a memory board to refresh Dynamic memory. REF- is active low and generated every 15 usec.

T/C (B27). T/C is a signal that provides a pulse when the terminal count for any DMA channel is reached. T/C is active high.

OSC (B30). OSC is an oscillator signal that is a high-speed clock with a 70 nanosecond period (14.31818 megahertz). It has a 50% duty cycle.

AT Interface Compatibility

The following pin assignments are used on the 36 position connectors found only on the AT type slots.

| PIN | SIGNAL NAME | PIN | SIGNAL NAME |
|---|---|---|---|
| C1 | SBHE- | D1 | MEMCS16- |
| C2 | SA23 | D2 | IOCS16- |
| C3 | SA22 | D3 | IRQ10 |
| C4 | SA21 | D4 | IRQ11 |
| C5 | SA20 | D5 | IRQ12 |
| C6 | SA19 | D6 | IRQ15 |
| C7 | SA18 | D7 | IRQ14 |
| C8 | SA17 | D8 | DACK0- |
| C9 | MEMR- | D9 | DRQ0 |
| C10 | MEMW- | D10 | DACK5- |
| C11 | SD08 | D11 | DRQ5 |
| C12 | SD09 | D12 | DACK6- |
| C13 | SD10 | D13 | DRQ6 |
| C14 | SD11 | D14 | DACK7- |
| C15 | SD12 | D15 | DRQ7 |
| C16 | SD13 | D16 | +5 V |
| C17 | SD14 | D17 | MASTER- |
| C18 | SD15 | D18 | Ground |

AT Bus Pin Definitions

SBHE- (C1). Bus High Enable indicates a transfer on the upper eight bits of the data bus, SD8-SD15. Sixteen bit devices use this signal to condition the data bus buffers tied to SD8-SD15. SBHE is active low.

SA17-SA23 (C2 through C8). These signals are used to address memory and I/O devices in the system. These signals are valid when BALE is high. These signals are not latched during microprocessor cycles, therefore, they do not stay valid for the entire cycle. They generate decodes for 1 wait state memory cycles. These decodes should be latched by the I/O adapters on the falling edge of BALE. These signals may also be driven by other DMA controllers or microprocessors that reside on the bus. SA17-SA23 are active high.

MEMR- (C9). This signal, along with SMEMR-, is used to instruct memory devices to drive data onto the data bus and is active on all 16 bit memory read cycles. MEMR- may be driven by any DMA controller or microprocessor on the I/O bus. When a microprocessor on the bus wishes to assert MEMR-, it must have address lines valid on the bus for at least one system clock period before asserting MEMR-. MEMR- is active low.

MEMW- (C9). This signal, along with SMEMW-, is used to instruct memory devices store data present on the data bus and is active on all 16 bit memory write cycles. MEMW- may be driven by any DMA controller or microprocessor on the I/O bus. When a microprocessor on the bus wishes to assert MEMW-, it must have address lines valid on the bus for at least one system clock period before asserting MEMW-. MEMW- is active low.

SD8-SD15 (C11 through C18). These are the upper eight bus bits for the memory and I/O devices. 16 bit devices will use SD0-SD7 of the PC bus and SD8-SD15 of the AT bus.

MEMCS16- (D1). This signal is used to tell the system board if the present data transfer is a 16-bit 1 wait state memory cycle. It is decoded from the SA17-SA23 lines. MEMCS16- is active low.

IOCS16- (D2). This signal is used to tell the system board if the present data transfer is a 16-bit 1 wait state I/O cycle. IOCS16- is active low.

IRQ10-IRQ12, IRQ14-IRQ15 (D3 through D7). Interrupt Requests IRQ10-IRQ14 are used to signal the microprocessor that an I/O device needs attention. An interrupt request is generated by raising an IRQ line high. The line must be held high until the microprocessor acknowledges the request. IRQ13 is reserved for the system board.

DRQ0, DRQ5-DRQ7 (D9, D11, D13, D15). DMA request 0 and DMA request 5 through 7 are asynchronous channel requests used by peripheral devices on the I/O bus to gain DMA service. A request is generated by bringing the DRQ line high, and the line must be held high until a DMA Acknowledge line goes active. DRQ0 will perform 8-bit transfers, and DRQ5-DRQ7 will perform 16-bit transfers. These signals are active high.

DACK0-, DACK5- - DACK7- (D8, D10, D12, D14). These lines are used to acknowledge DRQ0 and DRQ5-DRQ7. These signals are active low.

+5V (D16). Bus connector power.

MASTER- (D17). This signal is used with the DRQ lines to gain control of the system. A processor or DMA controller on the I/O bus can issue a DRQ to a DMA channel and receive a DACK. In response to the DACK, the processor or DMA controller can pull the MASTER- signal low, thus allowing it to control the system data, address, and control lines. After MASTER- is low, the I/O device must wait one system clock period before driving the address and data lines, and two clock periods before issuing a read or write command.

Warning: If this signal is held low for more than 15 microseconds, system memory may be lost due to lack of refresh.

GROUND (D18). Ground for I/O bus.

Memory Map

| ADDRESS HEX | RANGE DECIMAL | FUNCTION |
|---|---|---|
| FFFFFF | 16M | |
| | | 64K ROM IMAGE, DUPLICATED AT 0F0000 |
| FF0000 | | |
| | | 64K EXP ROM IMAGE, DUPLICATED AT 0E0000 |
| FE0000 | 15.875M | |
| | | 15M MEMORY EXP ON I/O BUS |
| 100000 | 1M | |
| | | 64K ROM ON SYS BOARD |
| 0F0000 | 960K | |
| | | 64K EXP ROM ON SYS BOARD |
| 0E0000 | 896K | |
| | | 128K I/O EXP ROM ON I/O BUS |
| 0C0000 | 768K | |
| | | 128K VIDEO MEMORY ON I/O BUS |
| 0A0000 | 640K | |
| | | 640K MEM ON SYS BOARD |
| 000000 | 000000 | |

I/O Port Map

| HEX RANGE | DEVICE |
|---|---|
| 000 - 00F | DMA Controller 1 |
| 020 - 021 | Interrupt Controller 1, Master |
| 022 - 023 | Configuration Registers (See Chipset Data Sheets) |
| 040 - 043 | Counter/Timer |
| 060 | Keyboard (8042) |
| 061 | Port B Register |
| 064 | Keyboard Status Port (8042) |
| 070 | NMI Mask |
| 071 | Real-time Clock |
| 080 - 08F | DMA Page Register |
| 0A0 - 0A1 | Interrupt Controller 2 |
| 0C0 - 0DF | DMA Controller 2 |
| 0E0 - 0EF | UNDEFINED |
| 0F0 | Clear Math Coprocessor Busy |
| 0F1 | Reset Math Coprocessor |
| 0F8 - 0FF | Math Coprocessor |
| 100 - 1EF | UNDEFINED |
| 1F0 - 1F8 | Fixed Disk |
| 1F9 - 1FF | UNDEFINED |
| 200 - 207 | Game I/O |
| 278 - 27F | Parallel Printer Port 2 |
| 280 - 2F7 | UNDEFINED |
| 2F8 - 3FF | Serial Port 2 |
| 300 - 31F | Prototype Card |
| 320 - 35F | UNDEFINED |
| 360 - 36F | Reserved |
| 370 - 377 | UNDEFINED |
| 378 - 37F | Parallel Printer Port 1 |
| 380 - 38F | SDLC, Bisynchronous 2 |
| 390 - 39F | UNDEFINED |
| 3A0 - 3AF | Bisynchronous 1 |
| 3B0 - 3BF | Monochrome Display |
| 3C0 - 3CF | Reserved |
| 3D0 - 3DF | Color/Graphics Monitor Adapter |
| 3E0 - 3EF | UNDEFINED |
| 3F0 - 3F7 | Diskette Controller |
| 3F8 - 3FF | Serial Port 1 |

ELECTRICAL BILL OF MATERIAL - TANDY 3000 NL

TANDY 3000 NL MAIN LOGIC SUBASSY. 8899066

| QTY. | DESCRIPTION | DESIGNATOR | VENDOR | PART NUMBER |
|---|---|---|---|---|
| 1 | TANDY 3000 NL MAIN LOGIC PCB - REV. B | | | 8709844 |
| 28 | STAKING PIN | E1-4,6-16, 20-31,Y6 | AMP#1-87022-0 | 8529014 |
| 1 | SOCKET 4-PIN (OSCILLATOR) | Y3 | AMP, MOLEX | 8509041 |
| 1 | INSULATOR SPACER, CRYSTAL | Y5 | | 8589132 |
| 2 | SOCKET 16-PIN DIP | U24,25 | AMP#640358-3 | 8509036 |
| 4 | SOCKET 18-PIN DIP | U16,17,22,23 | AMP#640359-3 | 8509037 |
| 2 | SOCKET 20-PIN DIP | U1,4 | AMP#640464-3 | 8509009 |
| 1 | SOCKET 24-PIN DIP(300 MIL) | U42 | AMP#641932-3 | 8509029 |
| 2 | SOCKET 28-PIN DIP | U38,39 | AMP#640362-3 | 8509007 |
| 3 | SOCKET 40-PIN DIP | U10,14,15 | AMP#640379-3 | 8509002 |
| 2 | SOCKET 68-PIN PLCC JEDEC-C | U2,13 | BURNDY#QILE68P-410T AMP#821574-1 | 8509020 |
| 4 | SOCKET 84-PIN PLCC JEDEC-C | U27,28,36,41 | BURNDY#QILE84P-410T AMP#321573-1 | 8509031 |
| 1 | SOCKET DUAL ROW SIMMS | J15,16 | | 8509040 |
| 6 | CONNECTOR 18-POS.DBL. | J9,10,12,14, 18,20 | | 8519258 |
| 7 | CONNECTOR 31-POS.DBL. | J11,13,17,19, 21-23 | | 8519236 |
| 1 | CONNECTOR 7-PIN DIN | J8 (KYBD) | | 8519358 |
| 1 | CONNECTOR 2-PIN SINGLE | J1 (LED) | MOLEX#22-29-2021 | 8519193 |
| 1 | CONNECTOR 3-PIN | J3 (BATTERY) | MOLEX#22-23-2031 | 8519301 |
| 1 | CONNECTOR 4-PIN SINGLE | J4 (SPEAKER) | MOLEX#22-22-2041 | 8519210 |
| 1 | CONNECTOR 12-PIN | J6 (POWER) | BURNDY#UHP1250T | 8519259 |
| 1 | CONNECTOR 2X17-PIN DBL. | J5 (FDC) | MOLEX#70246-3402 | 8519324 |
| 1 | CONNECTOR 9-PN D-SUB | J7 (RS-232) | AMP#747840-3 | 8519269 |
| 1 | CONNECTOR 25-PIN D-SUB | J2 (PRINTER) | AMP#747846-4 | 8519270 |
| 2 | SWITCH SPST-RESET/KEYLOCK | S2,3 | ALPS#KH15901 | 8489065 |
| 1 | SWITCH 8-POS.DIP | S1 | AMP#2-435668-4 | 8489004 |
| 26 | RES 33 OHM 1/8W 5% SMD R1206 | R1-6,8-10, 11,12-18,20, 23,25-27,30, 31,33,34 | GENERIC | X20303330 |
| 16 | RESISTOR 33 OHM 1/4W 5% | R19,22,29,32, 39,46,47,50, 52,53,57-59, 61,67,77 | " | 8207033 |
| 1 | RESISTOR 51 OHM 1/4W 5% | R62 | " | 8207051 |
| 4 | RESISTOR 75 OHM 1/4W 5% | R45,65,72,83 | " | 8207075 |
| 1 | RESISTOR 100 OHM 1/4W, 5% | R79 | | 8207110 |
| 2 | RESISTOR 150 OHM 1/4W 5% | R7,54 | " | 8207115 |
| 2 | RESISTOR 330 OHM 1/4W 5% | R55,63 | " | 8207133 |
| 2 | RESISTOR 470 OHM 1/4W 5% | R37,38 | " | 8207147 |
| 1 | RESISTOR 620 OHM 1/4W 5% | R56 | " | 8207162 |

ELECTRICAL BILL OF MATERIAL - TANDY 3000 NL

TANDY 3000 NL MAIN LOGIC SUBASSY. 8899066

| QTY. | DESCRIPTION | DESIGNATOR | VENDOR | PART NUMBER |
|---|---|---|---|---|
| 6 | RESISTOR 1K OHM 1/4W 5% | R21,28,68,69, 75,76 | " | 8207210 |
| 2 | RESISTOR 2.2K OHM 1/4W 5% | R35,66 | " | 8207222 |
| 4 | RESISTOR 4.7K OHM 1/4W 5% | R49,51,74,82, RX1 | GENERIC | 8207247 |
| 11 | RESISTOR 10K OHM 1/4W 5% | R24,36,40-43, 48,60,71,78, 80 | " | 8207310 |
| 2 | RESISTOR 1 MEG OHM 1/4W 5% | R64,81 | " | 8207510 |
| 2 | RES. NETWORK 33 OHM 8R SIP | RP11,12 | KYOCERA# SRNSB-16PC-330GA | 8290044 |
| 1 | RES.NETWORK 75 OHM 8R DIP | RP15 | KYOCERA# SRNSB-16PC-750GA | 8290081 |
| 1 | RES.PAK 150 OHM 5R SIP | RP3 | KYOCERA# SRNSA-06PC-151GA | 8290012 |
| 6 | RES.PAK 4.7K OHM 9R SIP | RP2,4, 5,X7,X2,X3 | KYOCERA# SRNSA-10PC-472GA | 8294247 |
| 12 | RES.PAK 10K OHM 9R SIP | RP1,6-10,13, 14,16-19 | KYOCERA# SRNSA-10PC-103GA | 8290010 |
| 28 | CAP 220 PF 50V 10% SMD C0805 | C1-4,7, 10-13,15,16, 18,19,21,22, 28,29,33,36, 43,44,48,53, 58,64,65,79, 101 | | X30122243 |
| 2 | CAP 0.1UF 50V 20% SMD C0805 | C74,75 | | X37410341 |
| 13 | CAP 22 PF 50V CD 5% NPO | C25,56,63,93, 103-105,124, 129-132,144 | | 8300222 |
| 3 | CAP 47 PF 50V CD 5% NPO | C80,157,183 | | 8300473 |
| 2 | CAP 100 PF 50V CD 10% NPO | C136,148 | | 8301103BAA |
| 2 | CAP 220 PF 50V CD 10% Z5P | C142,175 | | 8301223 |
| 31 | CAP 1000 PF 50V CD 10% Z5P | C5,8,23,24, 26,35,37,39, 45,50,59,60, 70,83,86,92, 96,99,100,107, 109,113,114,116, 119,154,165,166, 176,177,178 | | 8302104 |
| 7 | CAP .022 UF 50V 80% CD Z5U | C90,91,122,137, 151,155,173 | | 8303224 |
| 1 | CAP .047 UF 50V 10% CD Z5P | C73 | | 8303473 |

ELECTRICAL BILL OF MATERIAL - TANDY 3000 NL

TANDY 3000 NL MAIN LOGIC SUBASSY. 8899066

| QTY. | DESCRIPTION | DESIGNATOR | VENDOR | PART NUMBER |
|---|---|---|---|---|
| 51 | CAP .1UF 50V +80/-20% MONO AX. Z5P | C6,9,14,17, 20,27,30,31, 38,40,47,49, 51,52,54,55, 61,66-69,76-78, 81,82,102,106, 111,115,121, 123,125,126, 133,141,143, 145,150,158-162, 168-172,179,181 | | 8374104 |
| 12 | CAP .33 UF 50V MONO AX. | C71,72,84,85, 88,97,98,108 120,134,149,153 | | 8374334 |
| 25 | CAP 10 UF 16V ELECT.TANT 20% RAD. | C32,34,41,57, 87,94,95,110, 112,117,118,127, 128,138-140,146, 147,152,156,163, 164,167,174,180 | | 8336104 |
| 3 | CAP 33 UF 16V ELECT.TANT | C42,46,62 | | 8336331 |
| 1 | CAP VARIABLE 2.8-10PF | C182 | MATSUSHITA# ECU-1ZW10X535 | 8360310 |
| 1 | CAP VARIABLE 6-70 PF | C135 | MATSUSHITA | 8360607 |
| 4 | DIODE 1N4148 | CR4-6,CRX | GENERIC | 8150148 |
| 3 | DIODE - SCHOTTKY 1N5817 | CR1-3 | MOTOROLA | 8150817 |
| 1 | REGULATOR 78L05ACP (5V) | VR1 | MOTOROLA, FAIRCHILD, T.I. | 8052805 |
| 1 | CRYSTAL 14.31818 MHZ | Y5 | | 8409048 |
| 1 | CRYSTAL 32.768 KHZ | Y6 | | 8409033 |
| 1 | OSCILLATOR 1.8432 | Y1 | | 8409054 |
| 1 | OSCILLATOR 20 MHZ | Y4 | DAIWA | 8409074 |
| 1 | DUAL OSCILLATOR 16/9.6 MHZ | Y2 | | 8409063 |
| 6 | FERITE BEAD | FB1-3,5-7 | FAIRRITE | 8419013 |
| 12 | EMI FILTER .022 UF | CF1-9,13, 14,17 | MURATA | 8418013 |
| 1 | DELAY LINE 150NS 14-PIN | DL1 | DALLAS SEMI | 8429033 |
| 1 | IC 7407 | U18 | GENERIC 14-PIN | 8000007 |
| 1 | IC 74HC00 | U40 | 14-PIN | 8026000 |
| 2 | IC 74ALS244 | U30,31 | GENERIC 20-PIN | 8025244 |
| 7 | IC 74ALS245 | U20,21,26,33, 37,46,47 | " 20-PIN | 8025245 |
| 2 | IC 74ALS573 | U44,45, | " 20-PIN | 8025573 |
| 1 | IC 74F00 | U32 | " 14-PIN | 8015000 |

ELECTRICAL BILL OF MATERIAL - TANDY 3000 NL

TANDY 3000 NL MAIN LOGIC SUBASSY. 8899066

| QTY. | DESCRIPTION | DESIGNATOR | VENDOR | | PART NUMBER |
|---|---|---|---|---|---|
| 2 | IC 74F04 | U19,29 | " | 14-PIN | 8015004 |
| 1 | IC 74F08 | U43 | " | 14-PIN | 8015008 |
| 1 | IC 74F74 | U3, | " | 14-PIN | 8015074 |
| 2 | IC 74F244 | U34,35 | " | 20-PIN | 8015244 |
| 1 | IC 74F543 | U48 | " | 24-PIN SLIM | 8015543 |
| 1 | IC 14069 | U50 | " | 14-PIN | 8030069 |
| 1 | IC 74F573 | U49 | " | 24-PIN SLIM | 8015573 |
| 1 | IC 75477 | U6 | " | 8-PIN | 8040477 |
| 1 | IC MC1488 | U8 | " | 14-PIN | 8050188 |
| 2 | IC MC1489A | U5,9 | " | 14-PIN | 8050189 |
| 1 | BAG - STATIC SHIELDING | | | | 8590212 |

THESE COMPONENTS ARE NOT INSTALLED:

| | | |
|---|---|---|
| 4 | STAKING PIN | E5,17-19 |
| 2 | ZERO-OHM RESISTORS | R70,73 |
| 1 | RESISTOR, 75 OHM | R44 |
| 1 | CAPACITOR | C89 |
| 1 | IC 74FR04 | U7 |
| 1 | 74F08 | U11 |
| 1 | 74F20 | U12 |
| 6 | EMI FILTER | CF10-12,15,16,18 |

## TANDY 3000 NL MAIN LOGIC ASSEMBLY

| QTY. | DESCRIPTION | DESIGNATOR | VENDOR | PART NUMBER |
|---|---|---|---|---|
| 1 | TANDY 3000 NL MAIN LOGIC SUBASSEMBLY | | | 8899066 |
| 9 | JUMPER PLUG | E2-3,4-6, 8-9,12-13, 14-15,21-22, 23-24,26-27, 29-31 | | 8519098 |
| 1 | IC 80286-10 10MHZ | U13 | INTEL 68-PIN | 8043286 |
| 1 | IC 8042 | U14 | FUJITSU 40-PIN | 8070142 |
| 1 | IC 82C206 | U41 | CHIPS 84-PIN | 8075206 |
| 1 | IC 82C211 | U28 | CHIPS 84-PIN | 8040211 |
| 1 | IC 82C212 | U36 | CHIPS 84-PIN | 8041012 |
| 1 | IC 82C215 | U27 | CHIPS 84-PIN | 8040215 |
| 1 | IC WD37C65 | U10 | W. D. 40-PIN | 8040065 |
| 1 | IC VL16C451-QC | U2 | VTI 68-PIN | 8040451 |
| 2 | IC 27128 150NS ROM | U38,39 | 28-PIN | 8048128 |
| 2 | IC 16L8A PAL | U1,4 | 20-PIN | 8042168 |
| 1 | IC 20L10A | U42 | 24-PIN | 8044010 |
| 2 | IC 256K X 9 SIMM 150NS | J15,16 | SAMSUNG | 8899074 |
| 1 | PICOFUSE (CANADA ONLY) | F1 | MIDWEST COMPONENTS | 8479045 |

OPTIONAL PARTS:

| | | | | |
|---|---|---|---|---|
| 1 | OSCILLATOR 8 MHZ 40% DC (COPROCESSOR) | Y3 | MF OSCILLATORS# A1902-8MHZ | 8409065 |
| 1 | IC 80287-8 (NUMERIC PROCESSOR, 8MHZ) | U15 | INTEL 40-PIN | 8040287 |
| 1 | OSCILLATOR 10 MHZ 33% DC (COPROCESSOR) | Y3 | MF OSCILLATORS# A1901-10M | 8409079 |
| 1 | IC 80287-10 (NUMERIC PROCESSOR, 10MHZ) | U15 | INTEL 40-PIN | 8042287 |
| 2 | IC 64K X 1 DRAM 150NS *OPTIONAL - SOCKET ONLY* | U24,25 | HITACHI 16-PIN | 8049164 |
| 4 | IC 64K X 4 DRAM 150NS *OPTIONAL - SOCKET ONLY* | U16,17,22,23 | HITACHI 18-PIN | 8040464 |

ELECTRICAL BILL OF MATERIAL - TANDY 3000 NL

TANDY 3000 NL MAIN LOGIC SUBASSY. 8899066

| QTY. | DESCRIPTION | DESIGNATOR | VENDOR | PART NUMBER |
|---|---|---|---|---|
| 1 | TANDY 3000 NL MAIN LOGIC PCB - REV. D | | | 8709844 |
| 28 | STAKING PIN | E1-4,6-16, 20-31,Y6 | AMP#1-87022-0 | 8529014 |
| 1 | SOCKET 4-PIN (OSCILLATOR) | Y3 | AMP, MOLEX | 8509041 |
| 2 | SOCKET 16-PIN DIP | U24,25 | AMP#640358-3 | 8509036 |
| 4 | SOCKET 18-PIN DIP | U16,17,22,23 | AMP#640359-3 | 8509037 |
| 2 | SOCKET 20-PIN DIP | U1,4 | AMP#640464-3 | 8509009 |
| 1 | SOCKET 24-PIN DIP(300 MIL) | U42 | AMP#641932-3 | 8509029 |
| 2 | SOCKET 28-PIN DIP | U38,39 | AMP#640362-3 | 8509007 |
| 3 | SOCKET 40-PIN DIP | U10,14,15 | AMP#640379-3 | 8509002 |
| 2 | SOCKET 68-PIN PLCC JEDEC-C | U2,13 | BURNDY#QILE68P-410T AMP#821574-1 | 8509020 |
| 4 | SOCKET 84-PIN PLCC JEDEC-C | U27,28,36,41 | BURNDY#QILE84P-410T AMP#321573-1 | 8509031 |
| 1 | SOCKET DUAL ROW SIMMS | J15,16 | | 8509040 |
| 6 | CONNECTOR 18-POS.DBL. | J9,10,12,14, 18,20 | | 8519258 |
| 7 | CONNECTOR 31-POS.DBL. | J11,13,17,19, 21-23 | | 8519236 |
| 1 | CONNECTOR 7-PIN DIN | J8 (KYBD) | | 8519358 |
| 1 | CONNECTOR 2-PIN SINGLE | J1 (LED) | MOLEX#22-29-2021 | 8519193 |
| 1 | CONNECTOR 3-PIN | J3 (BATTERY) | MOLEX#22-23-2031 | 8519301 |
| 1 | CONNECTOR 4-PIN SINGLE | J4 (SPEAKER) | MOLEX#22-22-2041 | 8519210 |
| 1 | CONNECTOR 12-PIN | J6 (POWER) | BURNDY#UHP1250T | 8519259 |
| 1 | CONNECTOR 2X17-PIN DBL. | J5 (FDC) | MOLEX#70246-3402 | 8519324 |
| 1 | CONNECTOR 9-PN D-SUB | J7 (RS-232) | AMP#747840-3 | 8519269 |
| 1 | CONNECTOR 25-PIN D-SUB | J2 (PRINTER) | AMP#747846-4 | 8519270 |
| 2 | SWITCH SPST-RESET/KEYLOCK | S2,3 | ALPS#KH15901 | 8489065 |
| 1 | SWITCH 8-POS.DIP | S1 | AMP#2-435668-4 | 8489004 |
| 1 | RESISTOR 0 OHM | R85 | | 8290000 |
| 26 | RES 33 OHM 1/8W 5% SMD R1206 | R1-6,8-10, 11,12-18,20, 23,25-27,30, 31,33,34 | GENERIC | X20303330 |
| 16 | RESISTOR 33 OHM 1/4W 5% | R19,22,29,32, 39,46,47,50, 52,53,56,58, 59,61,67,77 | " | 8207033 |
| 1 | RESISTOR 51 OHM 1/4W 5% | R62 | " | 8207051 |
| 4 | RESISTOR 75 OHM 1/4W 5% | R45,65,72,83 | " | 8207075 |
| 1 | RESISTOR 100 OHM 1/4W, 5% | R79 | | 8207110 |
| 3 | RESISTOR 150 OHM 1/4W 5% | R7,44,54 | " | 8207115 |
| 2 | RESISTOR 330 OHM 1/4W 5% | R55,63 | " | 8207133 |
| 2 | RESISTOR 470 OHM 1/4W 5% | R37,38 | " | 8207147 |
| 1 | RESISTOR 620 OHM 1/4W 5% | R57 | " | 8207162 |

ELECTRICAL BILL OF MATERIAL - TANDY 3000 NL

TANDY 3000 NL MAIN LOGIC SUBASSY. 8899066

| QTY. | DESCRIPTION | DESIGNATOR | VENDOR | PART NUMBER |
|---|---|---|---|---|
| 6 | RESISTOR 1K OHM 1/4W 5% | R21,28,68,69, 75,76 | " | 8207210 |
| 2 | RESISTOR 2.2K OHM 1/4W 5% | R35,66 | " | 8207222 |
| 4 | RESISTOR 4.7K OHM 1/4W 5% | R49,51,74,82, RX1 | GENERIC | 8207247 |
| 11 | RESISTOR 10K OHM 1/4W 5% | R24,36,40-43, 48,60,71,78, 80 | " | 8207310 |
| 2 | RESISTOR 1 MEG OHM 1/4W 5% | R64,81 | " | 8207510 |
| 2 | RES. NETWORK 33 OHM 8R SIP | RP11,12 | KYOCERA# SRNSB-16PC-330GA | 8290044 |
| 1 | RES.NETWORK 75 OHM 8R DIP | RP15 | KYOCERA# SRNSB-16PC-750GA | 8290081 |
| 1 | RES.PAK 150 OHM 5R SIP | RP3 | KYOCERA# SRNSA-06PC-151GA | 8290012 |
| 5 | RES.PAK 4.7K OHM 9R SIP | RP2,3A,4, 4A,5 | KYOCERA# SRNSA-10PC-472GA | 8294247 |
| 11 | RES.PAK 10K OHM 9R SIP | RP1,6-10,13, 14,16-19 | KYOCERA# SRNSA-10PC-103GA | 8290010 |
| 28 | CAP 220 PF 50V 10% SMD C0805 | C1-4,7, 10-13,15,16, 18,19,21,22, 28,29,33,36, 43,44,48,53, 58,64,65,79, 101 | | X30122243 |
| 2 | CAP 0.1UF 50V 20% SMD C0805 | C74,75 | | X37410341 |
| 14 | CAP 22 PF 50V CD 5% NPO | C25,56,63,89,93, 103-105,124, 129-132,144 | | 8300222 |
| 3 | CAP 47 PF 50V CD 5% NPO | C80,157,183 | | 8300473 |
| 2 | CAP 100 PF 50V CD 10% NPO | C136,148 | | 8301103BAA |
| 1 | CAP 220 PF 50V CD 10% Z5P | C175 | | 8301223 |
| 29 | CAP 1000 PF 50V CD 10% Z5P | C5,8,23,24, 26,35,37,39, 45,50,59,60, 70,83,86,92, 96,99,100,107, 109,113,114,116, 154,165,166, 176,177,178 | | 8302104 |
| 7 | CAP .022 UF 50V 80% CD Z5U | C90,91,122,137, 151,155,173 | | 8303224 |
| 1 | CAP .047 UF 50V 10% CD Z5P | C73 | | 8303473 |

ELECTRICAL BILL OF MATERIAL - TANDY 3000 NL

TANDY 3000 NL MAIN LOGIC SUBASSY. 8899066

| QTY. | DESCRIPTION | DESIGNATOR | VENDOR | PART NUMBER |
|---|---|---|---|---|
| 50 | CAP .1UF 50V +80/-20% MONO AX. Z5P | C6,9,14,17, 20,27,30,31, 38,40,47,49, 51,52,54,55, 61,66-69,76-78, 81,82,102,106, 111,115,121, 123,125,126, 133,141,143, 145,150,158-162, 168-172,179,181 | | 8374104 |
| 12 | CAP .33 UF 50V MONO AX. | C71,72,84,85, 88,97,98,108 120,134,149,153 | | 8374334 |
| 25 | CAP 10 UF 16V ELECT.TANT 20% RAD. | C32,34,41,57, 87,94,95,110, 112,117,118,127, 128,138-140,146, 147,152,156,163, 164,167,174,180 | | 8336104 |
| 3 | CAP 33 UF 16V ELECT.TANT | C42,46,62 | | 8336331 |
| 1 | CAP VARIABLE 2.8-10PF | C182 | MATSUSHITA# ECU-1ZW10X535 | 8360310 |
| 1 | CAP VARIABLE 6-70 PF | C135 | MATSUSHITA | 8360607 |
| 4 | DIODE 1N4148 | CR4-6,CRX | GENERIC | 8150148 |
| 3 | DIODE - SCHOTTKY 1N5817 | CR1-3 | MOTOROLA | 8150817 |
| 1 | REGULATOR 78L05ACP (5V) | VR1 | MOTOROLA, FAIRCHILD, T.I. | 8052805 |
| 1 | CRYSTAL 14.31818 MHZ | Y5 | | 8409048 |
| 1 | CRYSTAL 32.768 KHZ | Y6 | | 8409033 |
| 1 | OSCILLATOR 1.8432 | Y1 | | 8409054 |
| 1 | OSCILLATOR 20 MHZ | Y4 | DAIWA | 8409074 |
| 1 | DUAL OSCILLATOR 16/9.6 MHZ | Y2 | | 8409063 |
| 6 | FERITE BEAD | FB1-3,5-7 | FAIRRITE | 8419013 |
| 12 | EMI FILTER .022 UF | CF1-9,13, 17,18 | | 8418013 |
| 1 | DELAY LINE 150NS 14-PIN | DL1 | DALLAS SEMI | 8429033 |
| 1 | IC 7407 | U18 | GENERIC 14-PIN | 8000007 |
| 1 | IC 74HC00 | U40 | 14-PIN | 8026000 |
| 2 | IC 74ALS244 | U30,31 | GENERIC 20-PIN | 8025244 |
| 7 | IC 74ALS245 | U20,21,26,33, 37,46,47 | " 20-PIN | 8025245 |
| 2 | IC 74ALS573 | U44,45, | " 20-PIN | 8025573 |
| 1 | IC 74F00 | U32 | " 14-PIN | 8015000 |

ELECTRICAL BILL OF MATERIAL - TANDY 3000 NL

TANDY 3000 NL MAIN LOGIC SUBASSY. 8899066

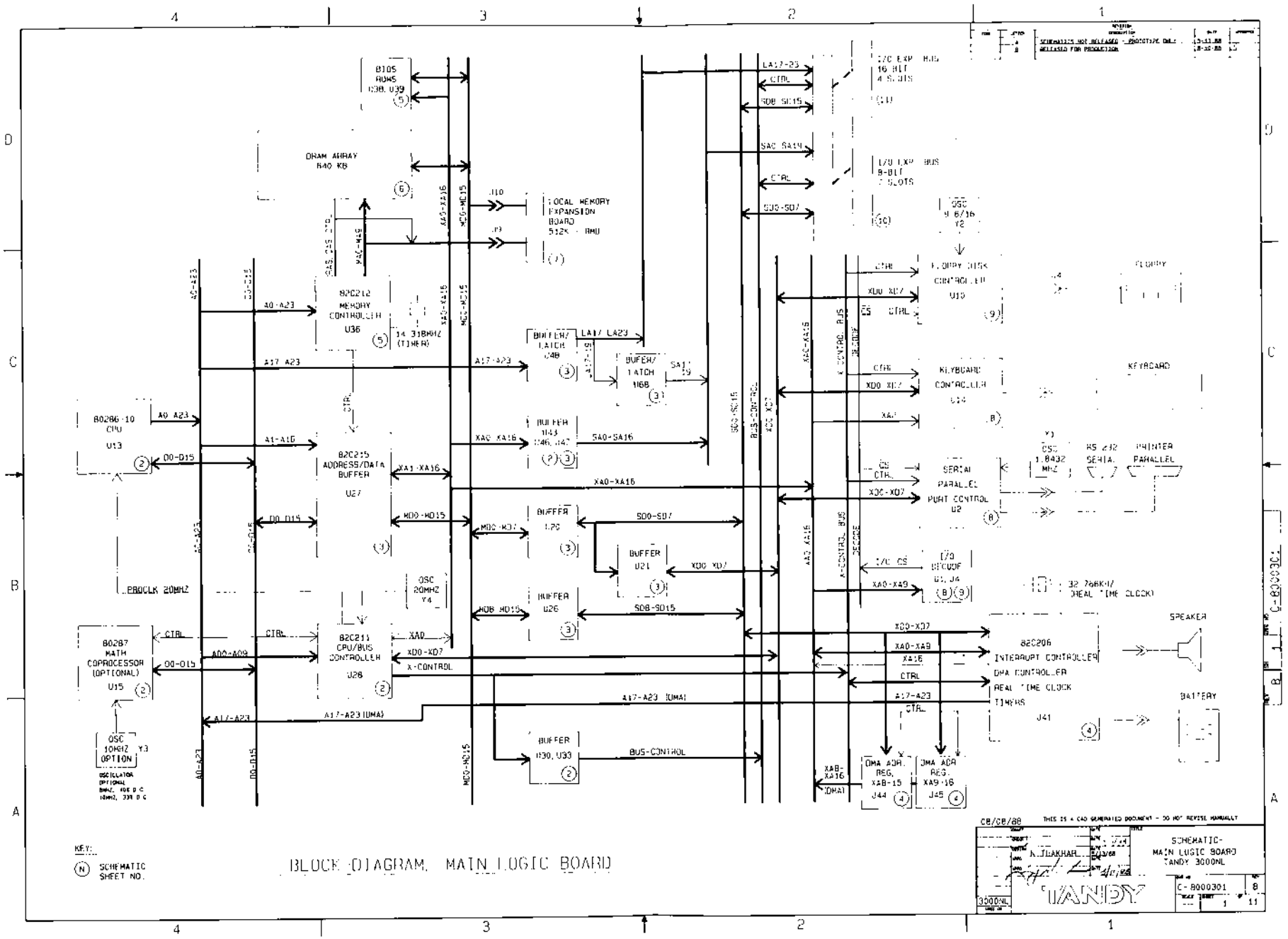
| QTY. | DESCRIPTION | DESIGNATOR | VENDOR | | PART NUMBER |
|---|---|---|---|---|---|
| 2 | IC 74F04 | U19,29 | " | 14-PIN | 8015004 |
| 2 | IC 74F08 | U11,43 | " | 14-PIN | 8015008 |
| 2 | IC 74F74 | U3,7 | " | 14-PIN | 8015074 |
| 2 | IC 74F244 | U34,35 | " | 20-PIN | 8015244 |
| 1 | IC 74F543 | U48 | " | 24-PIN SLIM | 8015543 |
| 1 | IC 14069 | U50 | " | 14-PIN | 8030069 |
| 1 | IC 74F573 | U49 | " | 24-PIN SLIM | 8015573 |
| 1 | IC 75477 | U6 | " | 8-PIN | 8040477 |
| 1 | IC MC1488 | U8 | " | 14-PIN | 8050188 |
| 2 | IC MC1489A | U5,9 | " | 14-PIN | 8050189 |
| 1 | BAG - STATIC SHIELDING | | | | 8590212 |

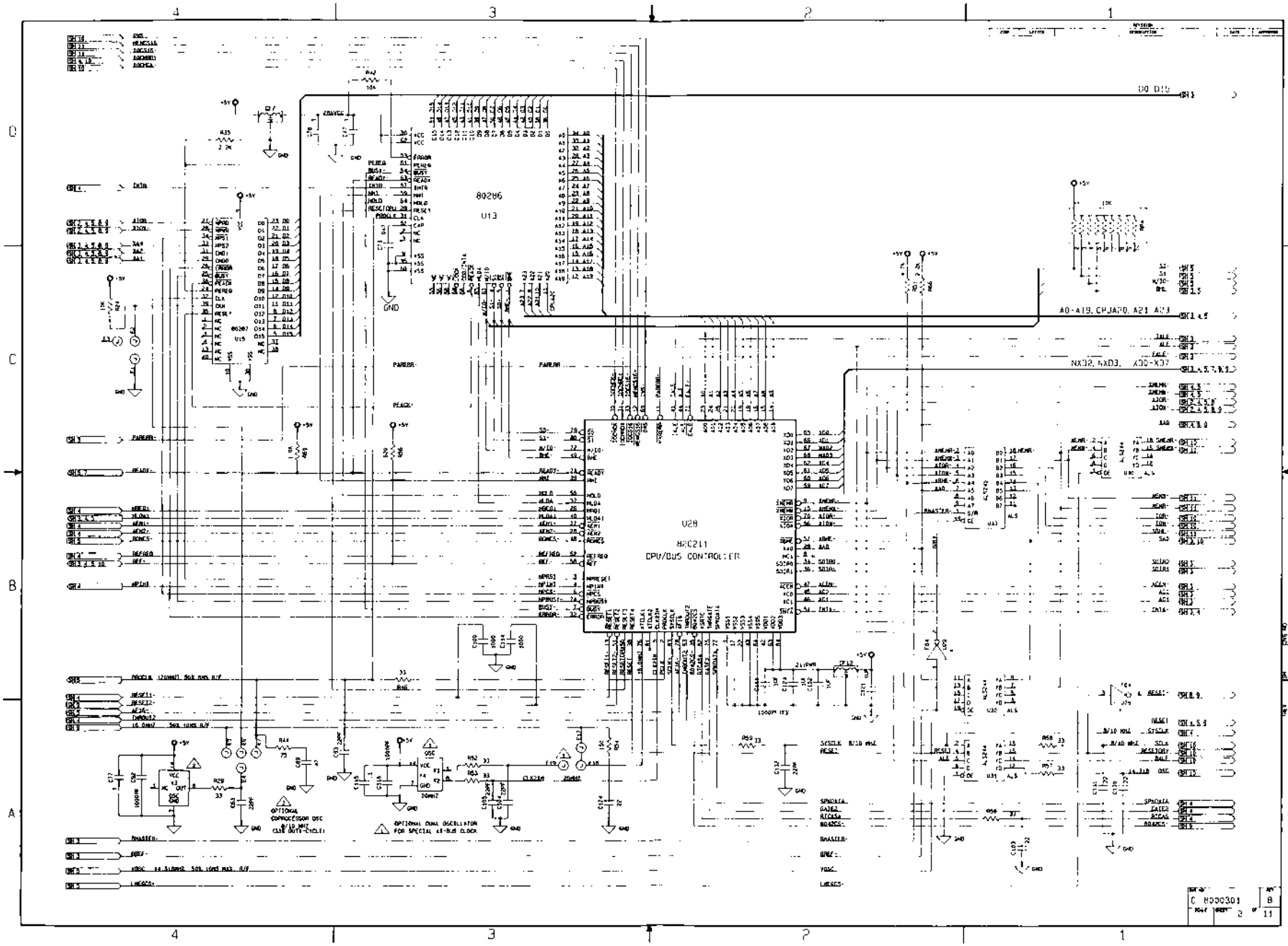
## TANDY 3000 NL MAIN LOGIC ASSEMBLY

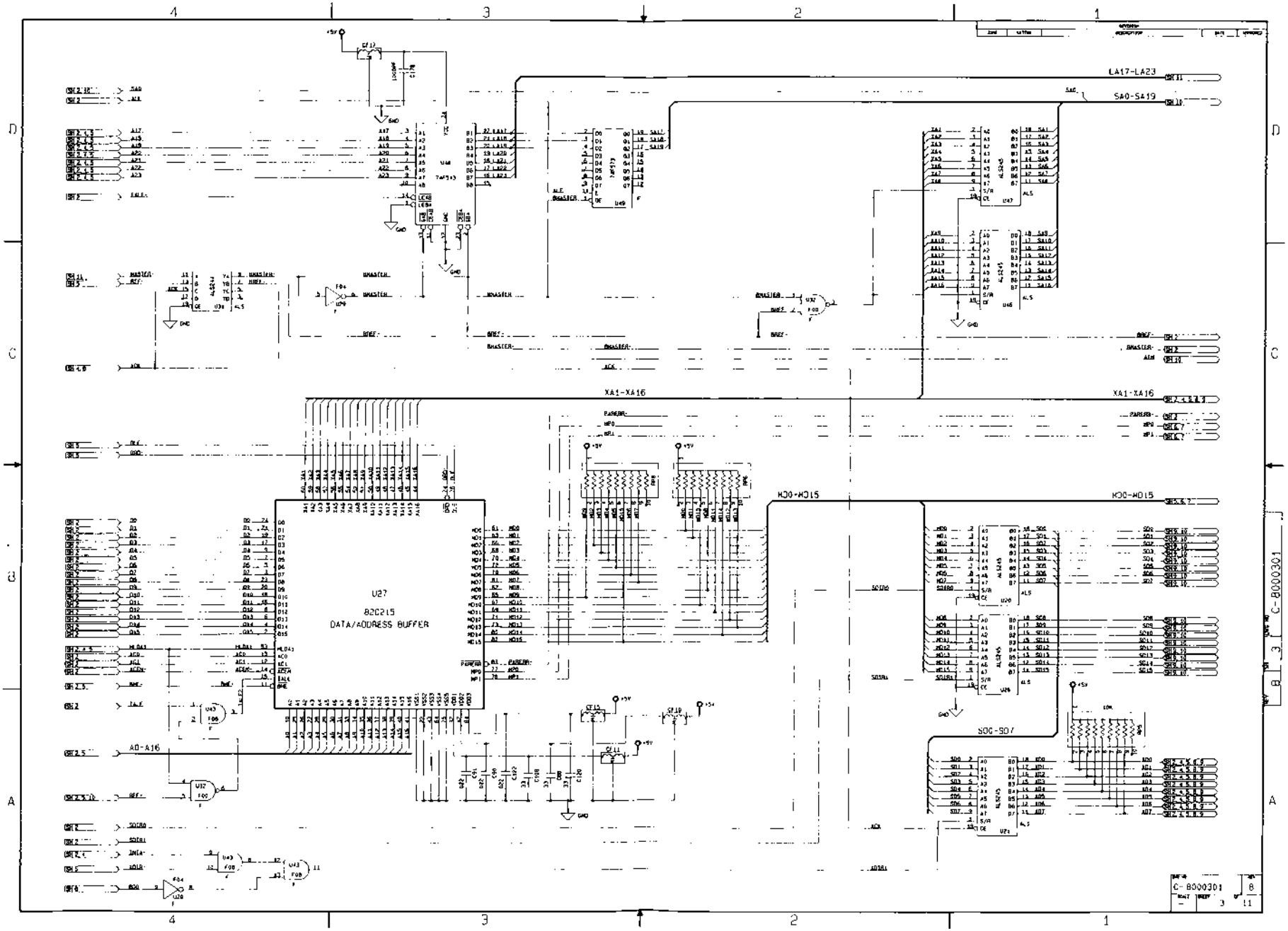
| QTY. | DESCRIPTION | DESIGNATOR | VENDOR | PART NUMBER |
|---|---|---|---|---|
| 1 | TANDY 3000 NL MAIN LOGIC SUBASSEMBLY | | | 8899066 |
| 9 | JUMPER PLUG | E2-3,4-6, 8-9,12-13, 14-15,21-22, 23-24,26-27, 29-31 | | 8519098 |
| 1 | IC 80286-10 10MHZ | U13 | INTEL 68-PIN | 8043286 |
| 1 | IC 8042 | U14 | FUJITSU 40-PIN | 8070142 |
| 1 | IC 82C206 | U41 | CHIPS 84-PIN | 8075206 |
| 1 | IC 82C211 | U28 | CHIPS 84-PIN | 8040211 |
| 1 | IC 82C212 | U36 | CHIPS 84-PIN | 8041012 |
| 1 | IC 82C215 | U27 | CHIPS 84-PIN | 8040215 |
| 1 | IC WD37C65 | U10 | W. D. 40-PIN | 8040065 |
| 1 | IC VL16C451-QC | U2 | VTI 68-PIN | 8040451 |
| 2 | IC 27128 150NS ROM | U38,39 | | 8048128 |
| 2 | IC 16L8A PAL | U1,4 | | 8042168 |
| 1 | IC 20L10A | U42 | | 8044010 |
| 2 | IC 256K X 9 SIMM 150NS | J15,16 | SAMSUNG | 8899074 |
| 1 | PICOFUSE (CANADA ONLY) | F1 | SP5-1A-SANO MIDWEST COMPONENTS | 8479045 |

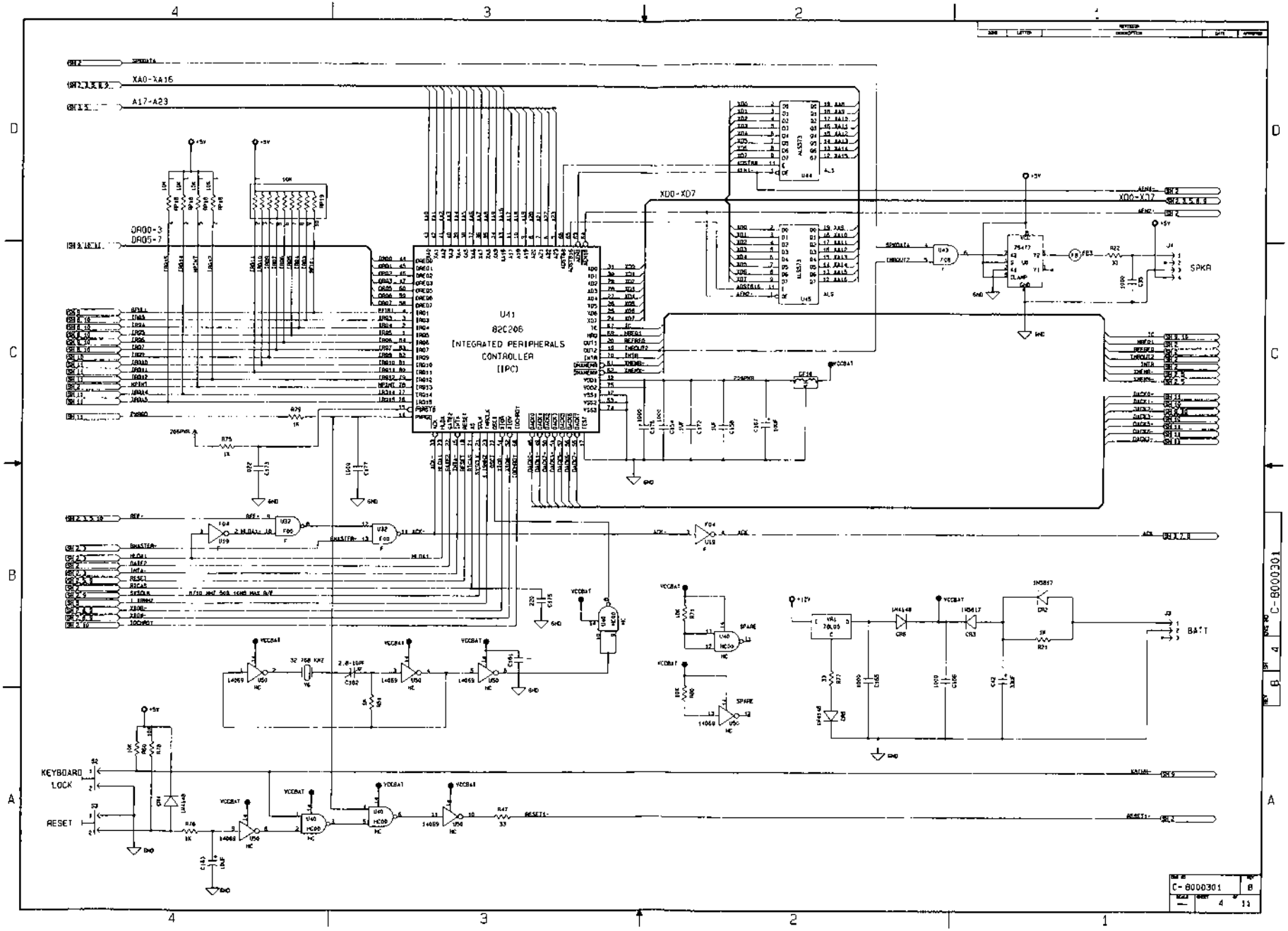
OPTIONAL PARTS:

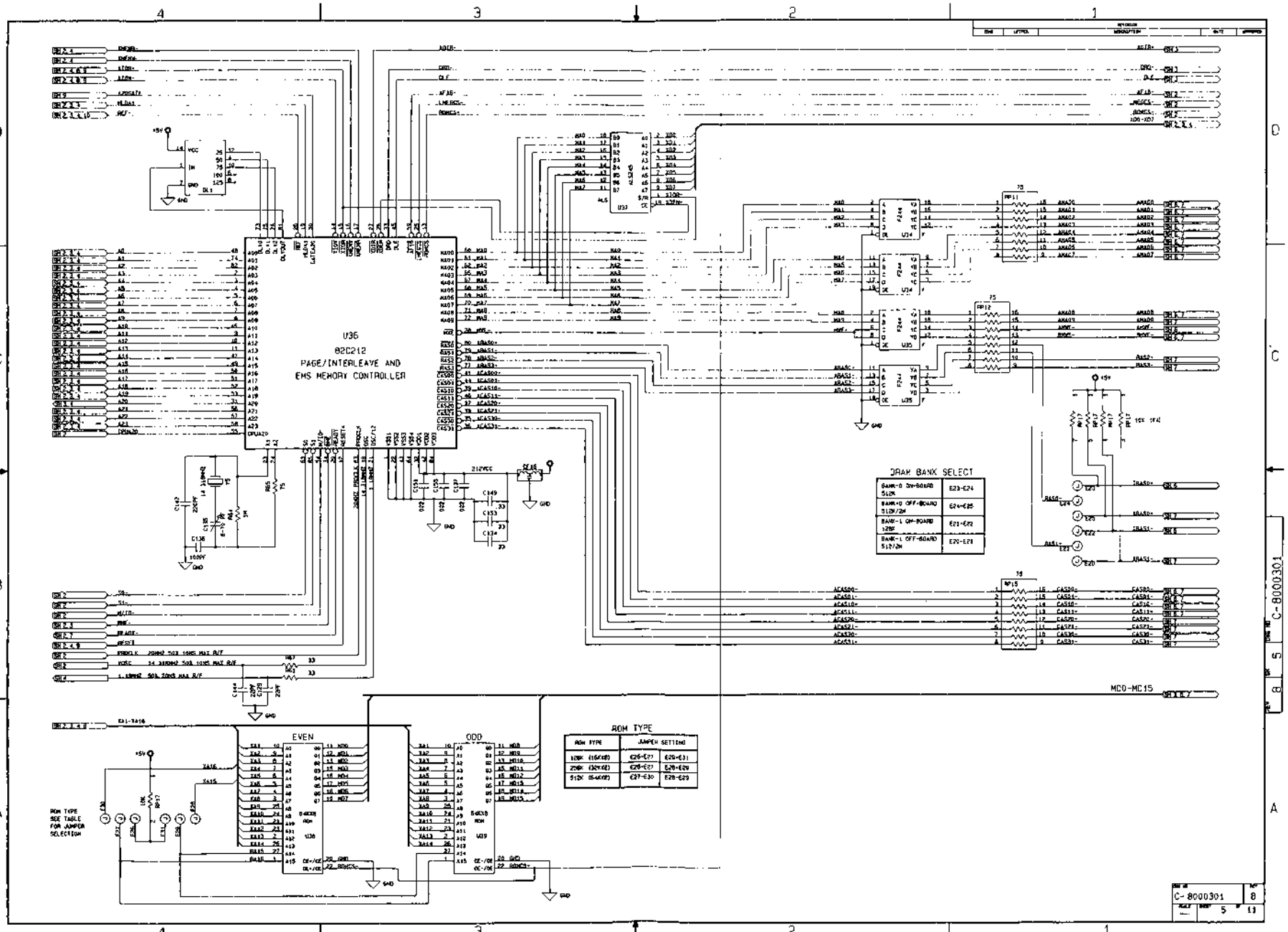
| | | | | |
|---|---|---|---|---|
| 1 | OSCILLATOR 8 MHZ 40% DC (COPROCESSOR) | Y3 | MF OSCILLATORS# A1902-8MHZ | 8409065 |
| 1 | IC 80287-8 (NUMERIC PROCESSOR, 8MHZ) | U15 | INTEL 40-PIN | 8040287 |
| 1 | OSCILLATOR 10 MHZ 33% DC (COPROCESSOR) | Y3 | MF OSCILLATORS# A1901-10M | 8409079 |
| 1 | IC 80287-10 (NUMERIC PROCESSOR, 10MHZ) | U15 | INTEL 40-PIN | 8042287 |
| 2 | IC 64K X 1 DRAM 150NS *OPTIONAL - SOCKET ONLY* | U24,25 | HITACHI 16-PIN | 8049164 |
| 4 | IC 64K X 4 DRAM 150NS *OPTIONAL - SOCKET ONLY* | U16,17,22,23 | HITACHI 18-PIN | 8040464 |

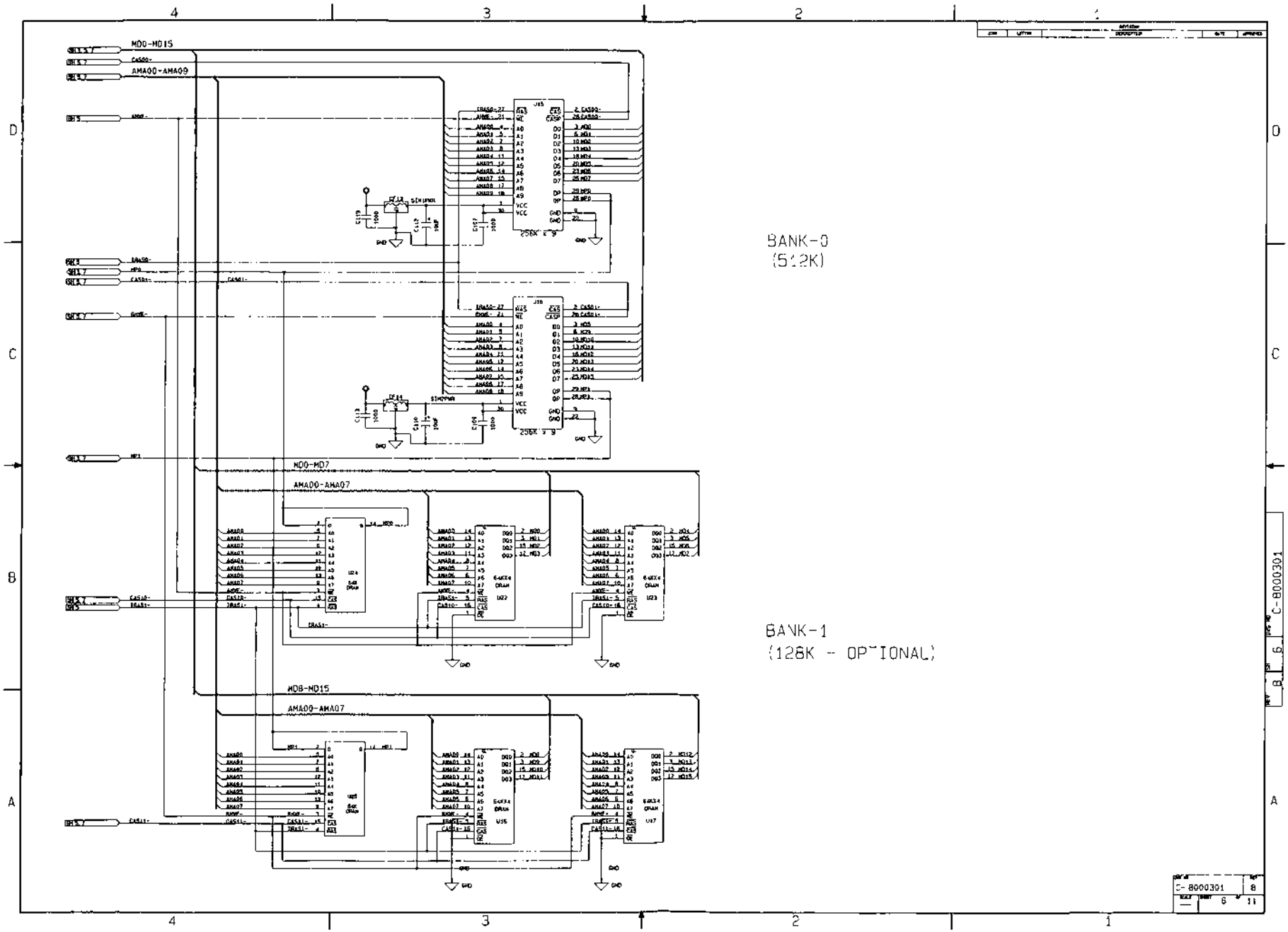

BLOCK DIAGRAM, MAIN LOGIC BOARD
KEY:
SCHEMATIC SHEET NO.
DRAM ARRAY 640 KB
B105 ROMS U38, U39
LOCAL MEMORY EXPANSION BOARD 512K - 8MB
82C212 MEMORY CONTROLLER U36
14.31818MHZ (TIMER)
B0286-10 CPU U13
82C215 ADDRESS/DATA BUFFER U27
BUFFER/ LATCH U48
BUFFER/ LATCH U68
BUFFER U43 U46, U47
BUFFER U20
BUFFER U21
BUFFER U26
BUFFER U30, U33
PBOCLK 20MHZ
OSC 20MHZ Y4
B0287 MATH COPROCESSOR (OPTIONAL) U15
OSC 10MHZ Y3 OPTION
82C211 CPU/BUS CONTROLLER U28
I/O EXP. BUS 16 BIT
I/O EXP. BUS 8-BIT
OSC 9.6/16 Y2
FLOPPY DISK CONTROLLER U10
FLOPPY
KEYBOARD CONTROLLER U14
KEYBOARD
SERIAL PARALLEL PORT CONTROL U2
OSC 1.8432 MHZ
RS 232 SERIAL
PRINTER PARALLEL
I/O DECODE U5, U4
32.768KHZ REAL TIME CLOCK
SPEAKER
82C206 INTERRUPT CONTROLLER DMA CONTROLLER REAL TIME CLOCK TIMERS J41
BATTERY
DMA ADR. REG. XA8-15 J44
DMA ADR. REG. XA9-16 J45
BUS-CONTROL
X-CONTROL BUS DECODE
THIS IS A CAD GENERATED DOCUMENT - DO NOT REVISE MANUALLY
SCHEMATIC- MAIN LOGIC BOARD TANDY 3000NL
TANDY
C-8000301
3000NL

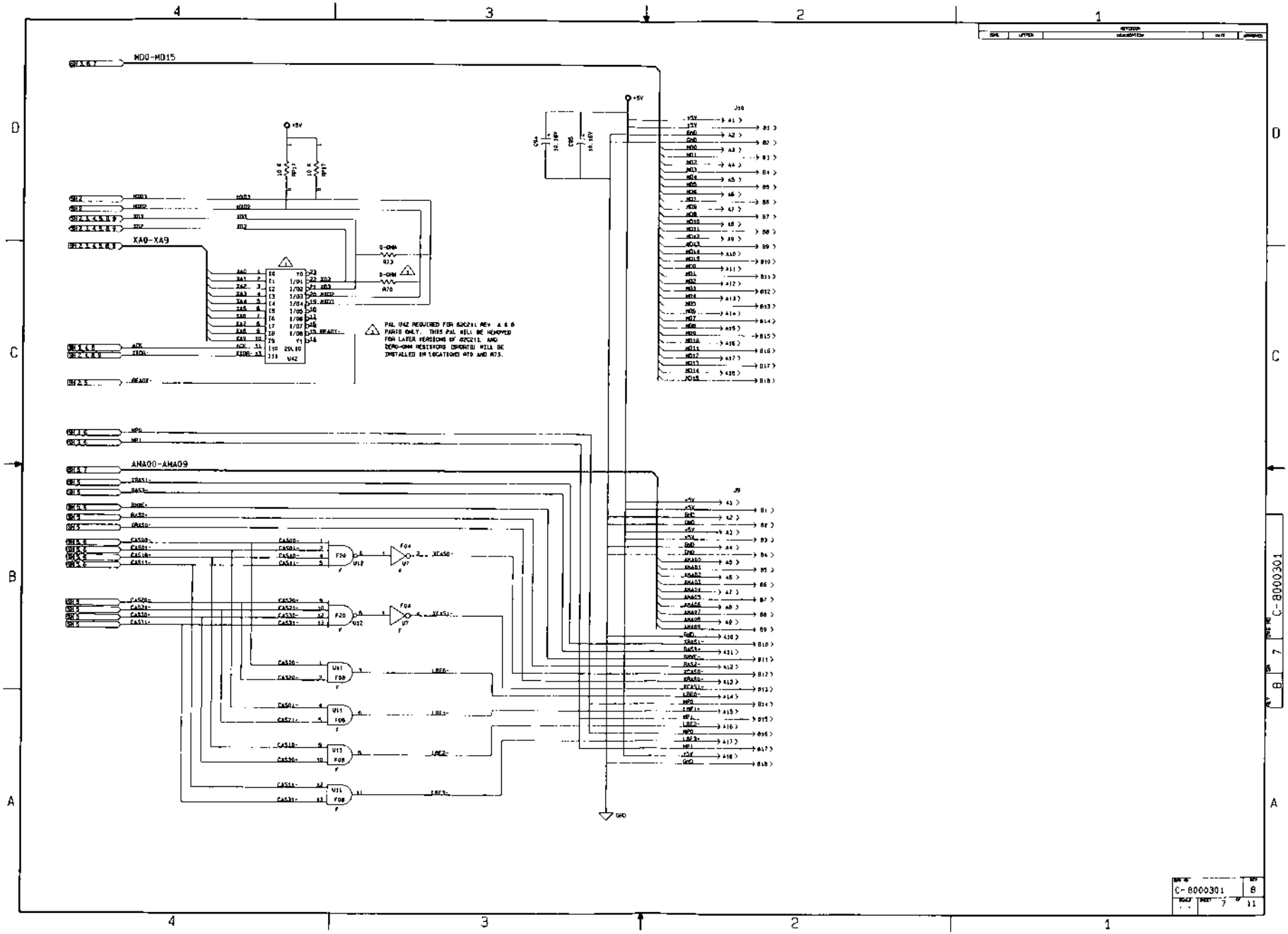

80286
U13
U28
82C211
CPU/BUS CONTROLLER
OPTIONAL COPROCESSOR OSC
OPTIONAL DUAL OSCILLATOR FOR SPECIAL 48-BUS CLOCK
A0-A19, CPUAPD, A21 A23
NX02, NXD3, AD0-AD7
C 800030
B
11

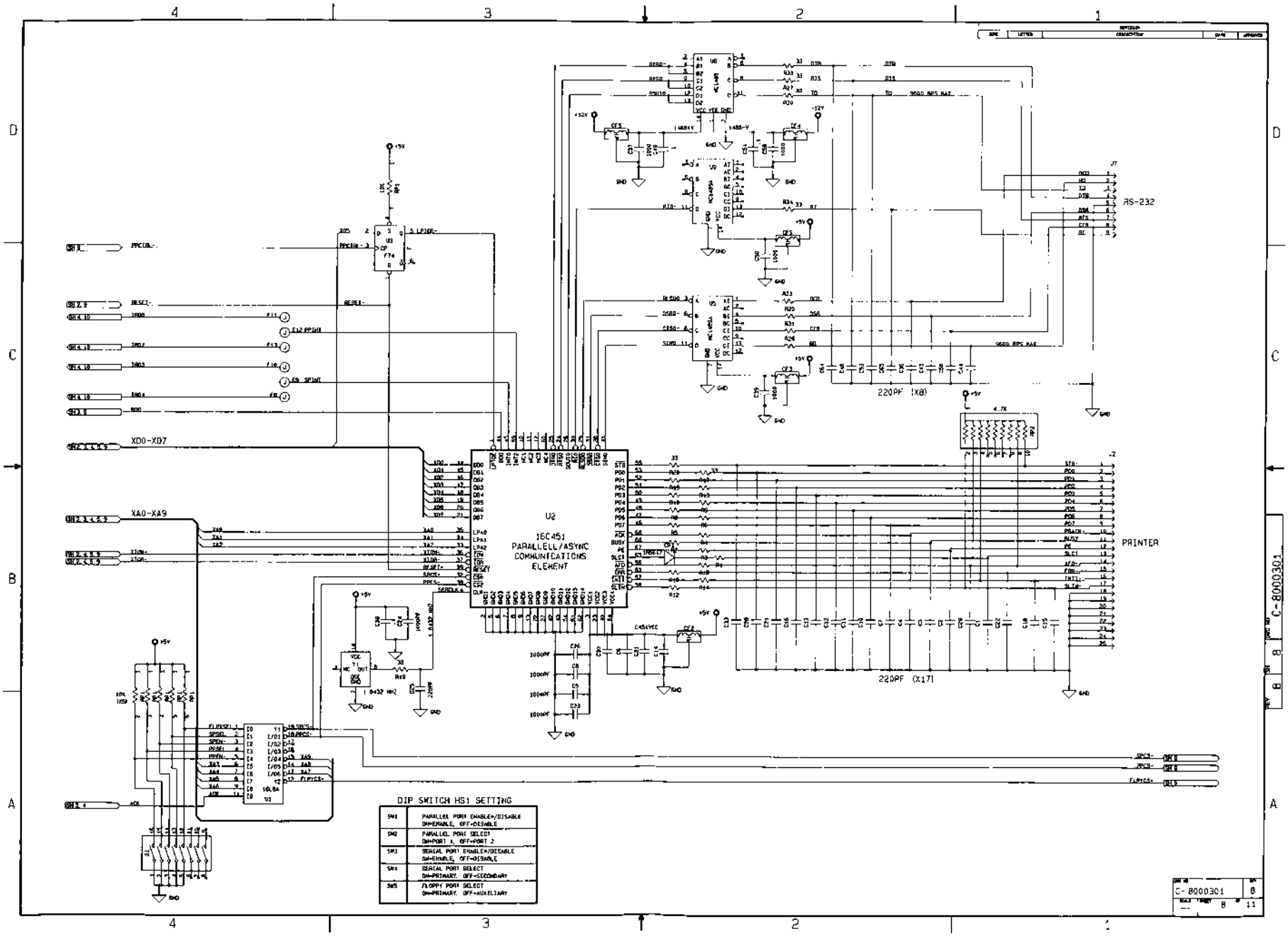

LA17-LA23
SA0-SA19
XA1-XA16
XD0-XD15
SD0-SD7
A0-A16
U27
82C215
DATA/ADDRESS BUFFER
C-8000301


XA0-XA16
A17-A23
DA00-3
DA05-7
XD0-XD7
U41
82C206
INTEGRATED PERIPHERALS
CONTROLLER
(IPC)
SPKR
BATT
KEYBOARD
LOCK
RESET
C-8000301
B
4
11


U36
82C212
PAGE/INTERLEAVE AND
EMS MEMORY CONTROLLER
DRAM BANK SELECT
ROM TYPE
EVEN
ODD
ROM TYPE
SEE TABLE
FOR JUMPER
SELECTION
MD0-MD15
C-8000301
8
5
13

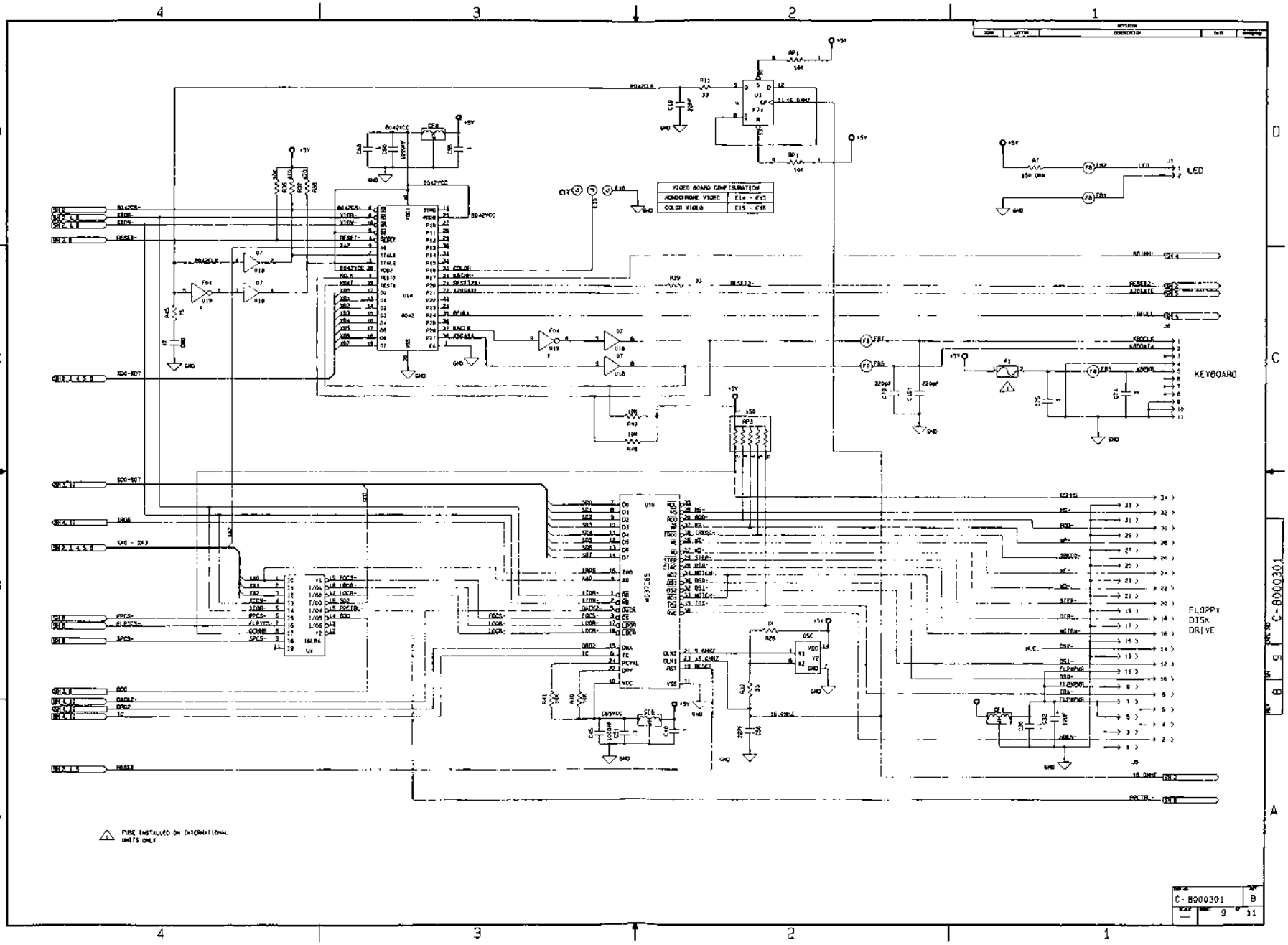

MD0-MD15
CASD0-
AMA00-AMA09
BANK-0
(512K)
256K x 9
MD0-MD7
AMA00-AMA07
BANK-1
(128K - OPTIONAL)
MD8-MD15
AMA00-AMA07
C-8000301

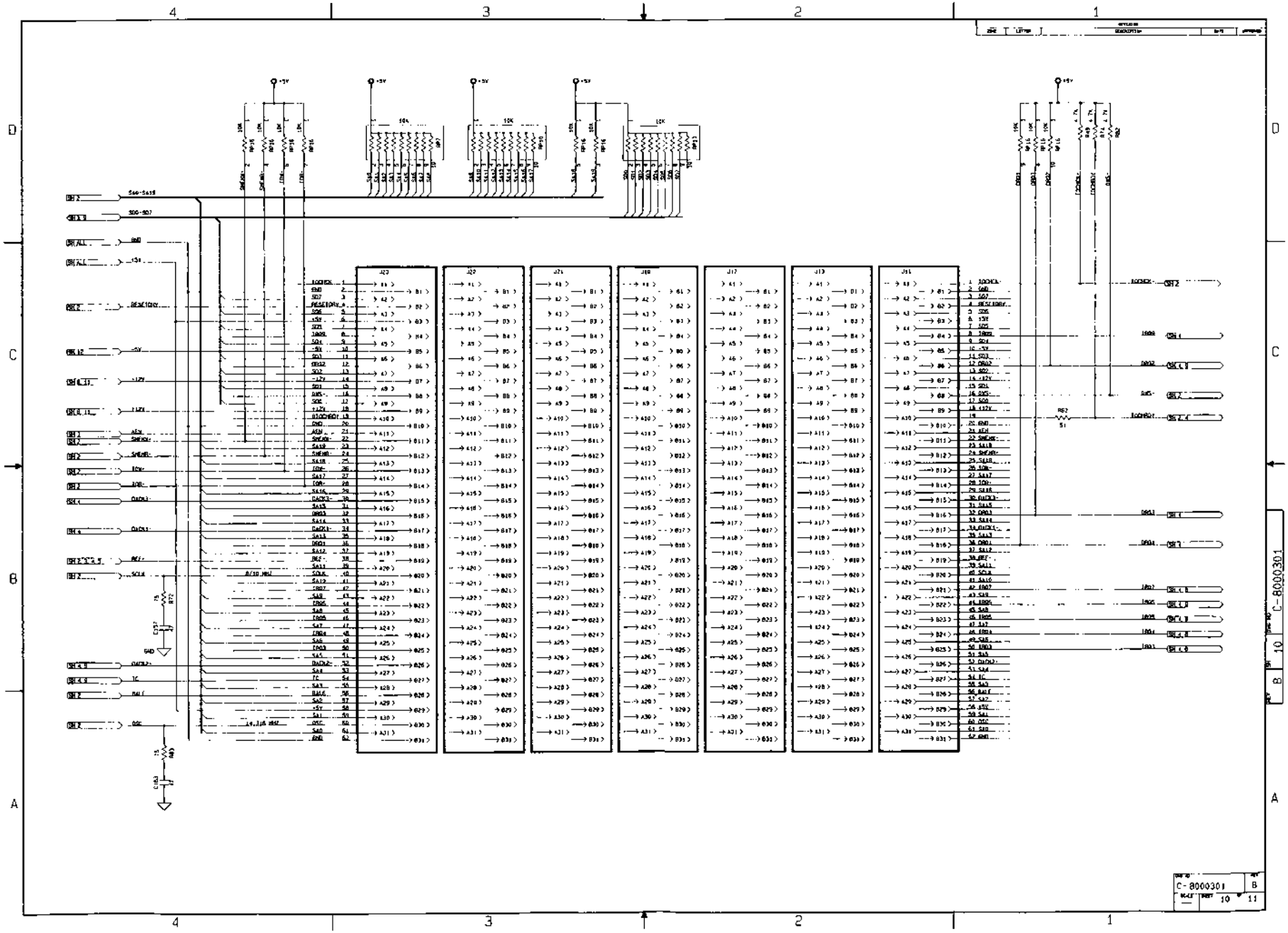

MD0-MD15
XA0-XA9
AMA00-AMA09
J10
J9
PAL U42 REQUIRED FOR 62C211 REV 4 & 6 PARTS ONLY. THIS PAL WILL BE REMOVED FOR LATER VERSIONS OF 62C211. AND ZERO-OHM RESISTORS (SHORTS) WILL BE INSTALLED IN LOCATIONS A70 AND A73.
C-8000301
8
7
11

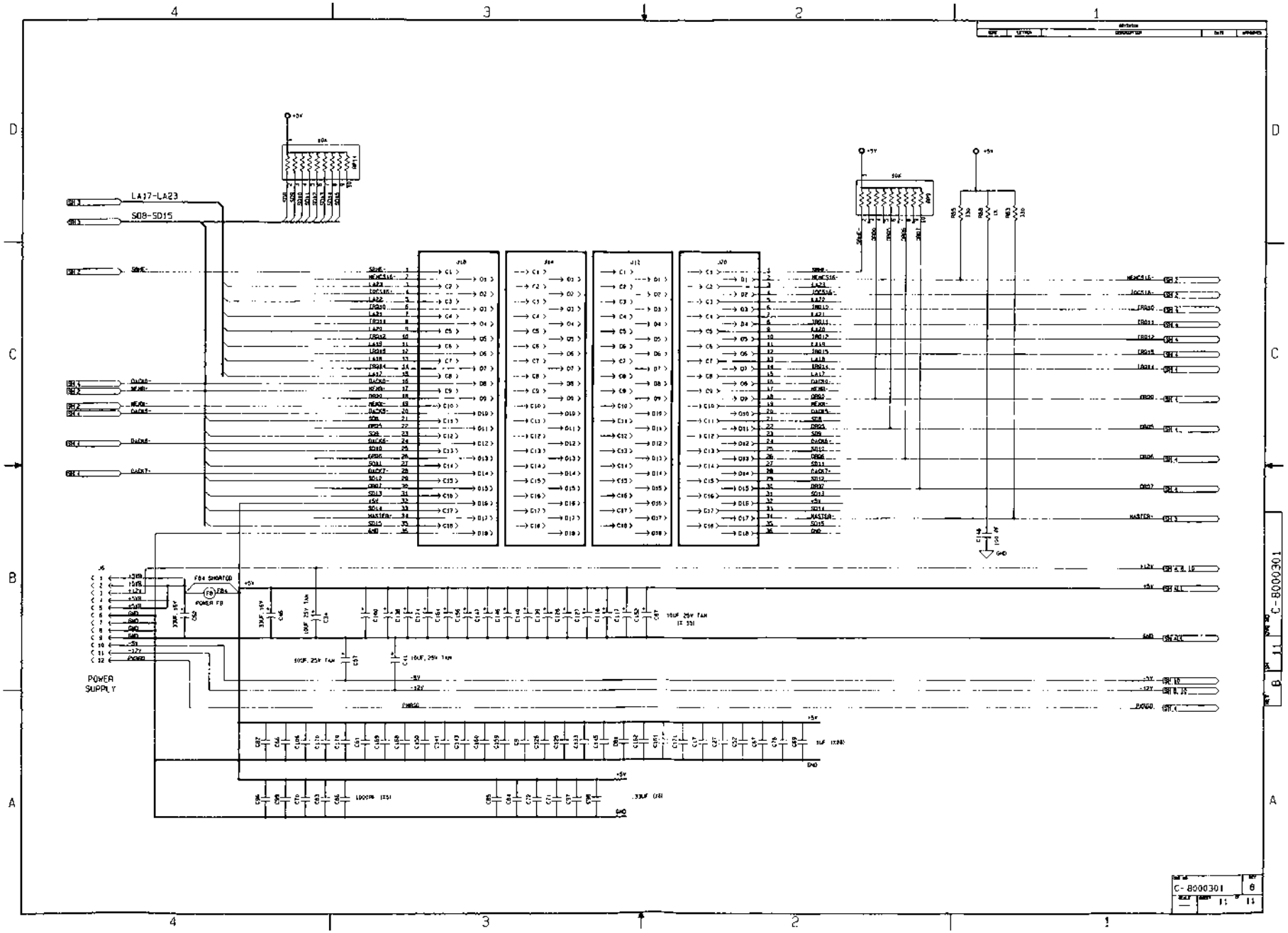


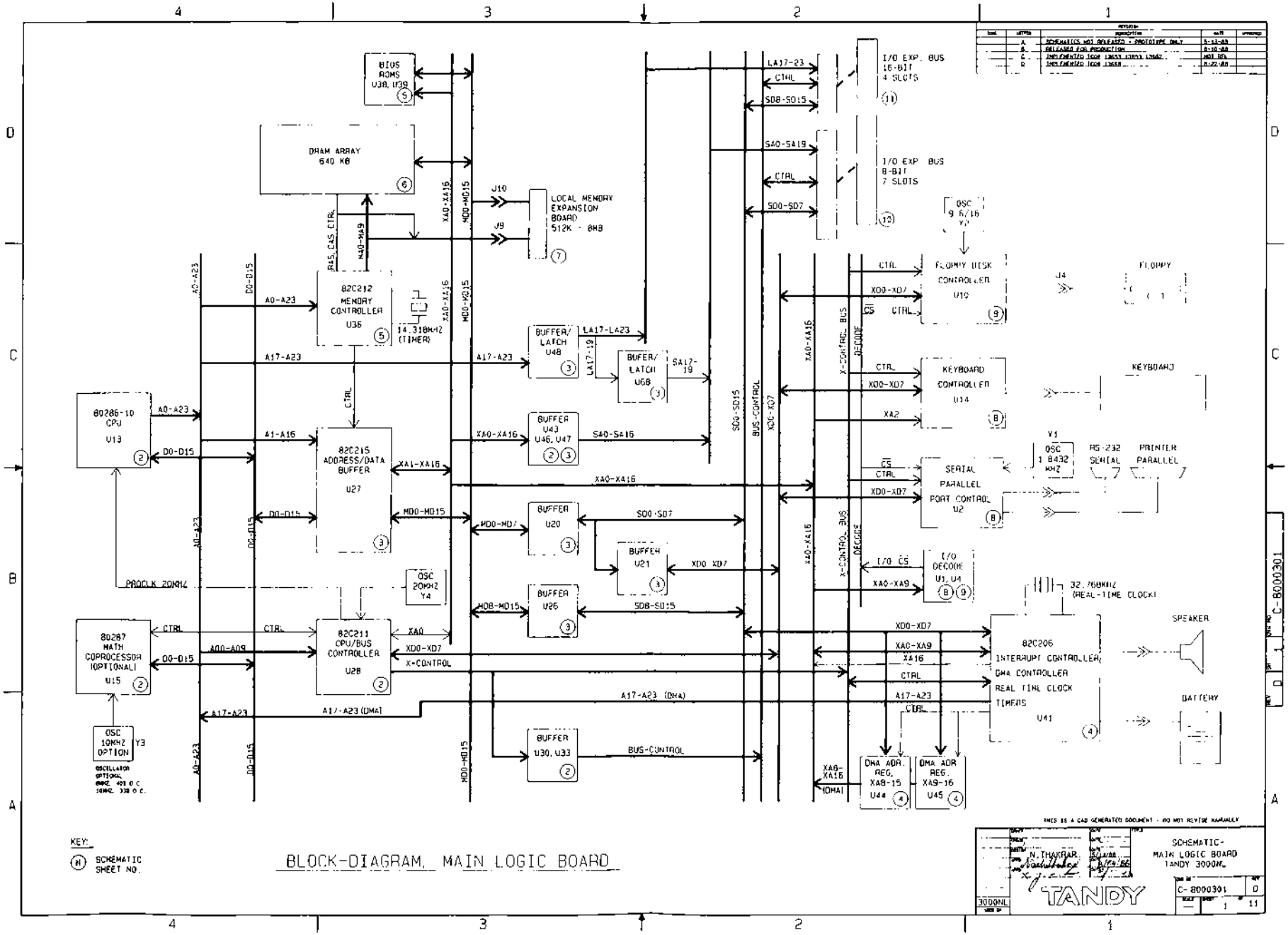

DIP SWITCH HS1 SETTING

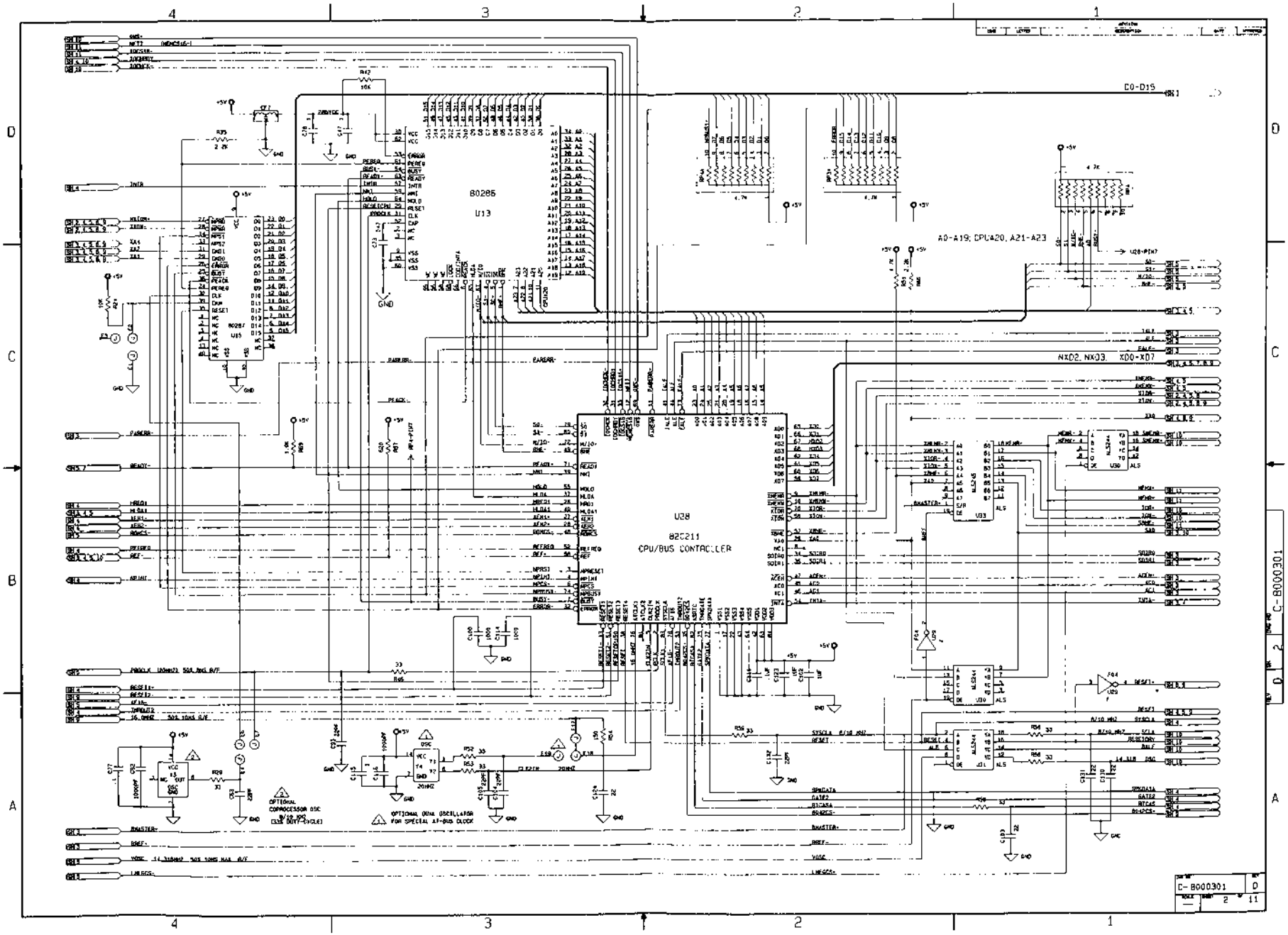
| | |
|---|---|
| SW1 | PARALLEL PORT ENABLE=/DISABLE ON=ENABLE, OFF=DISABLE |
| SW2 | PARALLEL PORT SELECT ON=PORT 1, OFF=PORT 2 |
| SW3 | SERIAL PORT ENABLE=/DISABLE ON=ENABLE, OFF=DISABLE |
| SW4 | SERIAL PORT SELECT ON=PRIMARY, OFF=SECONDARY |
| SW5 | FLOPPY PORT SELECT ON=PRIMARY, OFF=AUXILIARY |

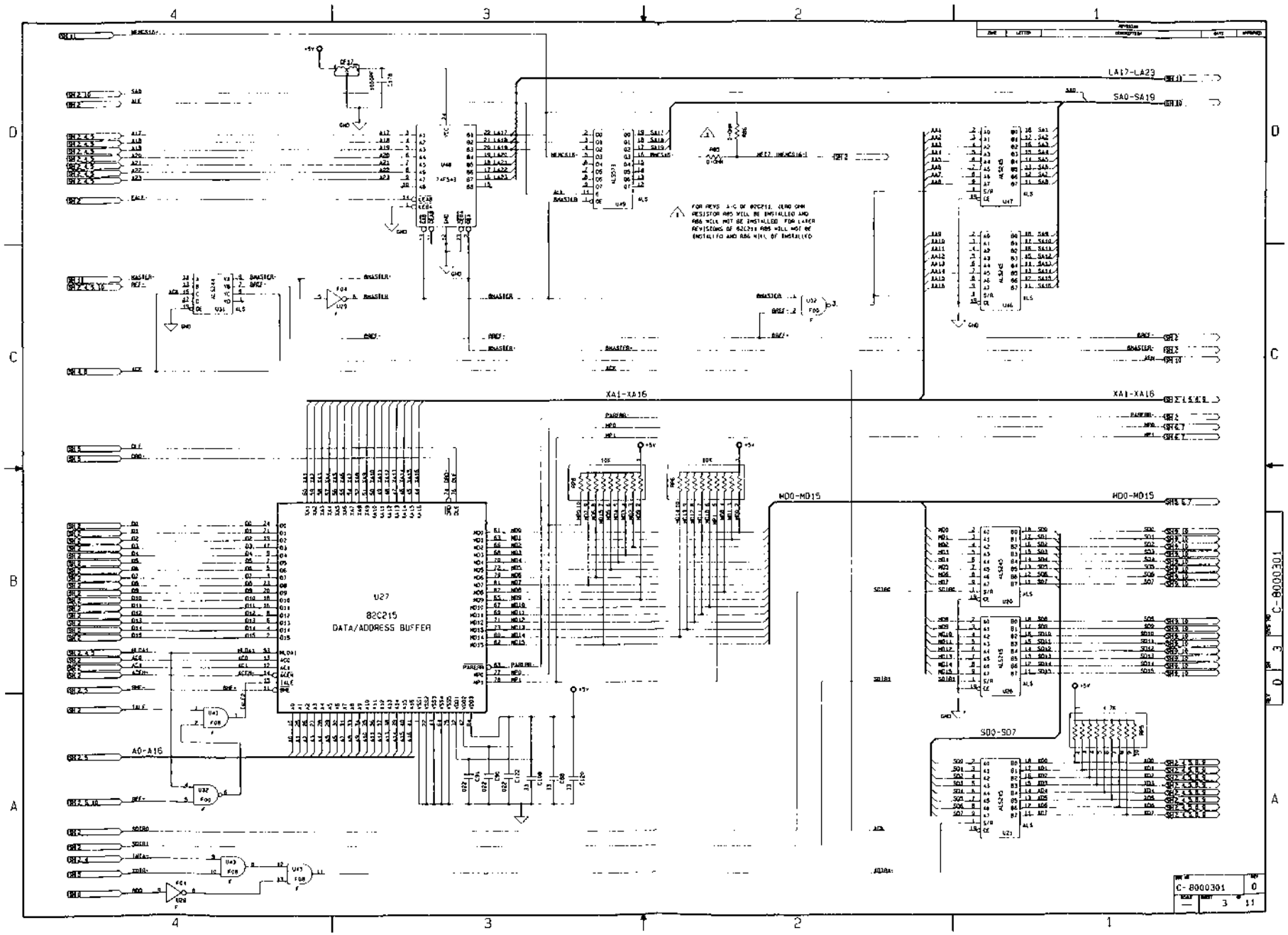

VIDEO BOARD CONFIGURATION
MONOCHROME VIDEO
E14 - E33
COLOR VIDEO
E15 - E35
LED
KEYBOARD
FLOPPY DISK DRIVE
FUSE INSTALLED ON INTERNATIONAL UNITS ONLY
C-8000301
B
9
11

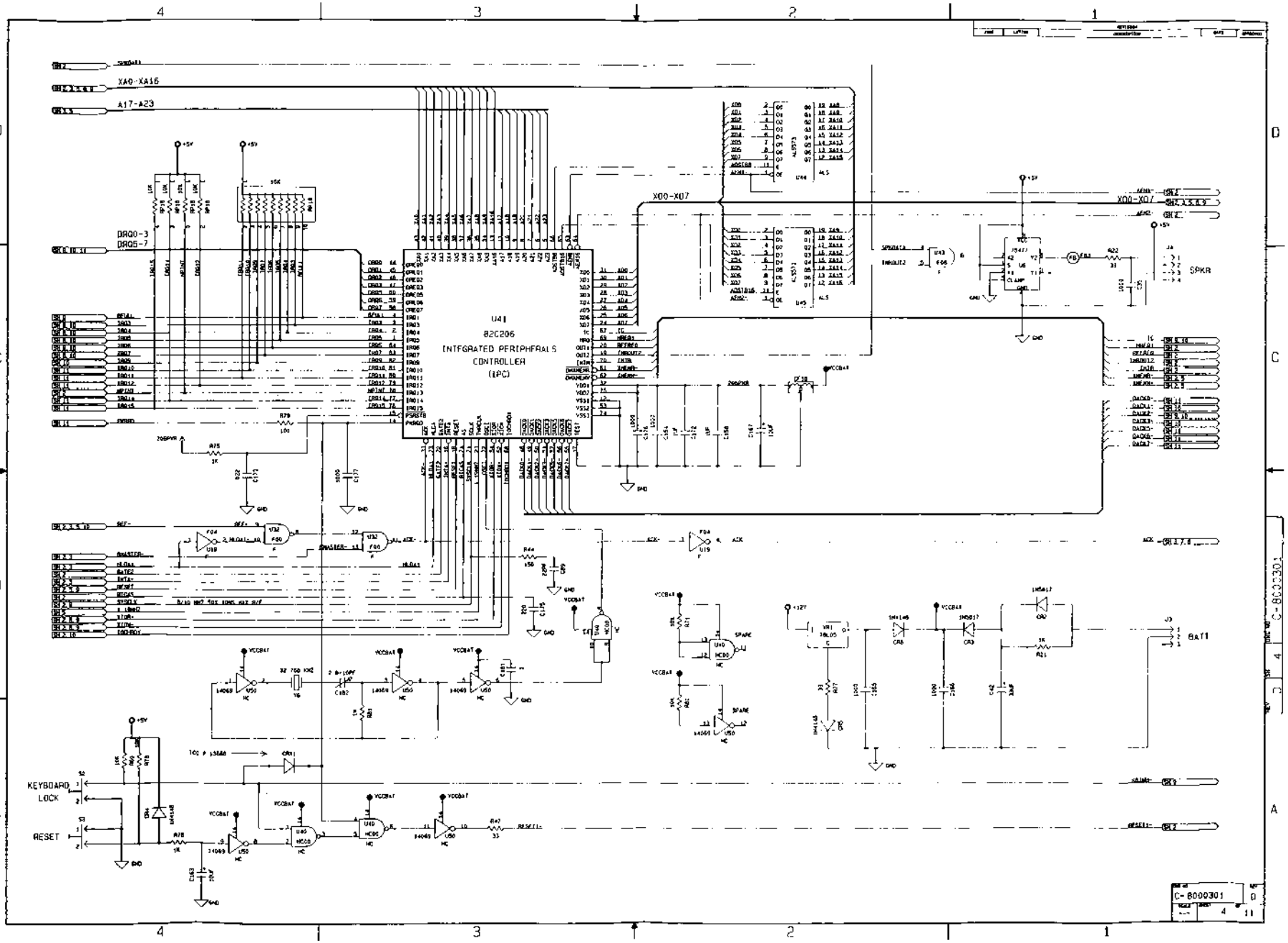

J20
J21
J18
J17
J13
J11
C-8000301
B
10
11

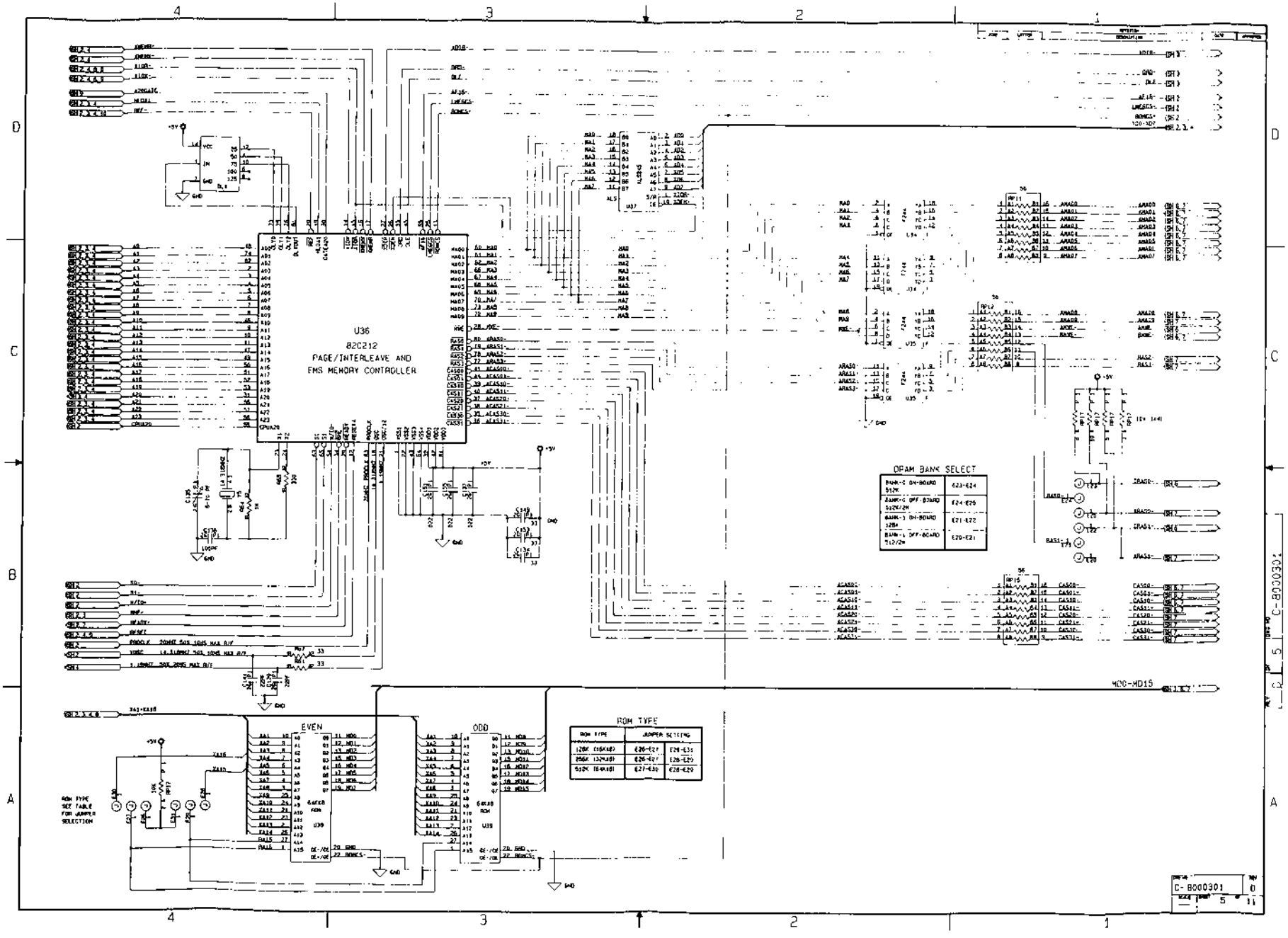

LA17-LA23
SD8-SD15
POWER SUPPLY
FB4 SHORTED
POWER FB
C-8000301
6

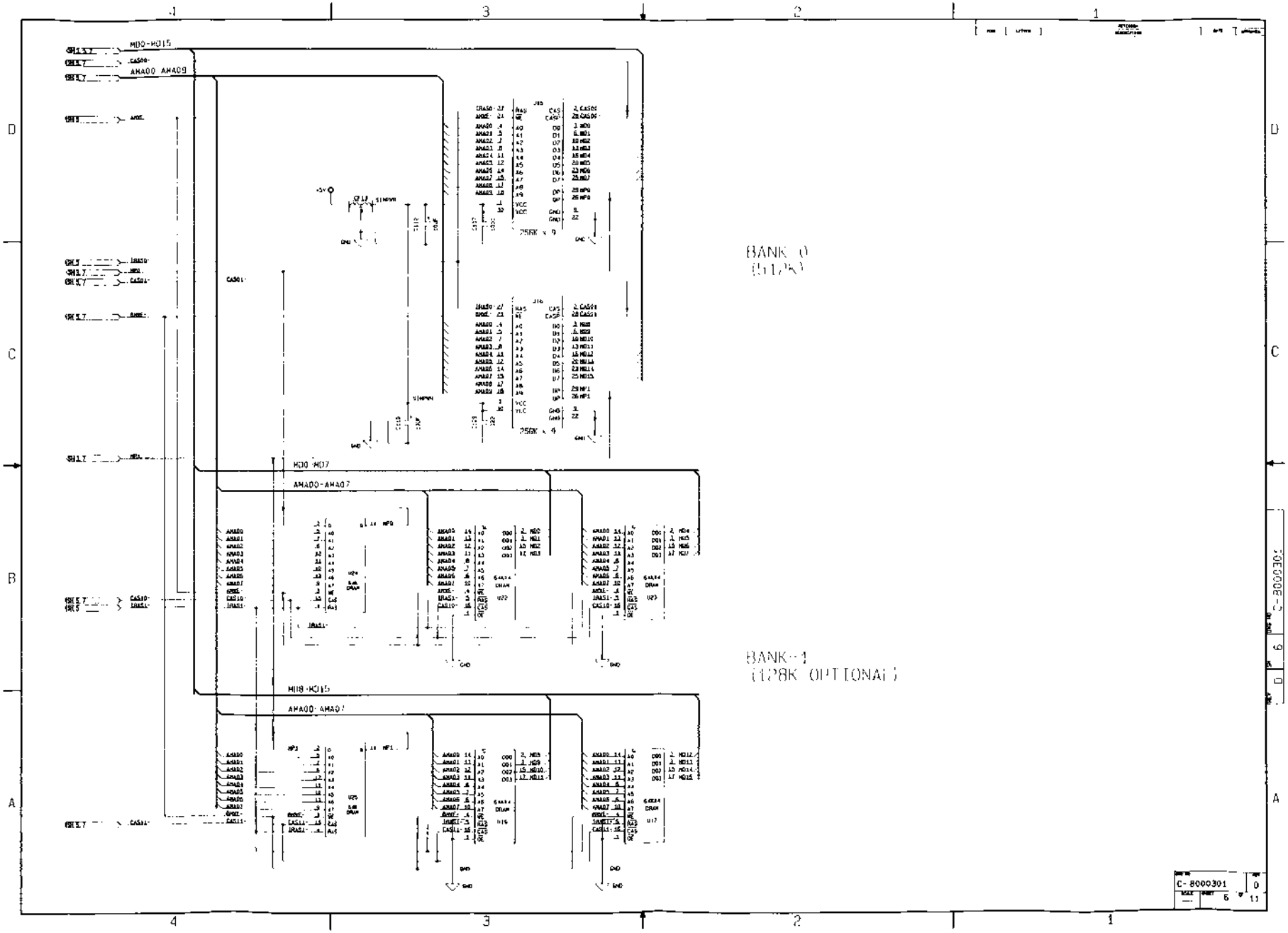

BIOS ROMS U38, U39
DRAM ARRAY 640 KB
LOCAL MEMORY EXPANSION BOARD 512K - 8MB
82C212 MEMORY CONTROLLER U36
14.318MHZ (TIMER)
80286-10 CPU U13
82C215 ADDRESS/DATA BUFFER U27
BUFFER/ LATCH U48
BUFFER/ LATCH U68
BUFFER U43 U46, U47
BUFFER U20
BUFFER U21
BUFFER U26
BUFFER U30, U33
OSC 20MHZ Y4
PROCLK 20MHZ
80287 MATH COPROCESSOR (OPTIONAL) U15
82C211 CPU/BUS CONTROLLER U28
OSC 10MHZ OPTION Y3
OSCILLATOR OPTIONAL
I/O EXP. BUS 16-BIT 4 SLOTS
I/O EXP BUS 8-BIT 7 SLOTS
OSC 9.6/16 Y2
FLOPPY DISK CONTROLLER U19
FLOPPY
KEYBOARD CONTROLLER U14
KEYBOARD
SERIAL PARALLEL PORT CONTROL U2
RS-232 SERIAL
PRINTER PARALLEL
OSC 1.8432 MHZ
I/O DECODE U1, U4
32.768KHZ (REAL-TIME CLOCK)
82C206 INTERRUPT CONTROLLER DMA CONTROLLER REAL TIME CLOCK TIMERS U41
SPEAKER
BATTERY
DMA ADR. REG. XA8-15 U44
DMA ADR REG. XA9-16 U45
KEY:
SCHEMATIC SHEET NO.
BLOCK-DIAGRAM, MAIN LOGIC BOARD
THIS IS A CAD GENERATED DOCUMENT - DO NOT REVISE MANUALLY
N.THAKKAR
SCHEMATIC- MAIN LOGIC BOARD TANDY 3000NL
TANDY
C-8000301
3000NL

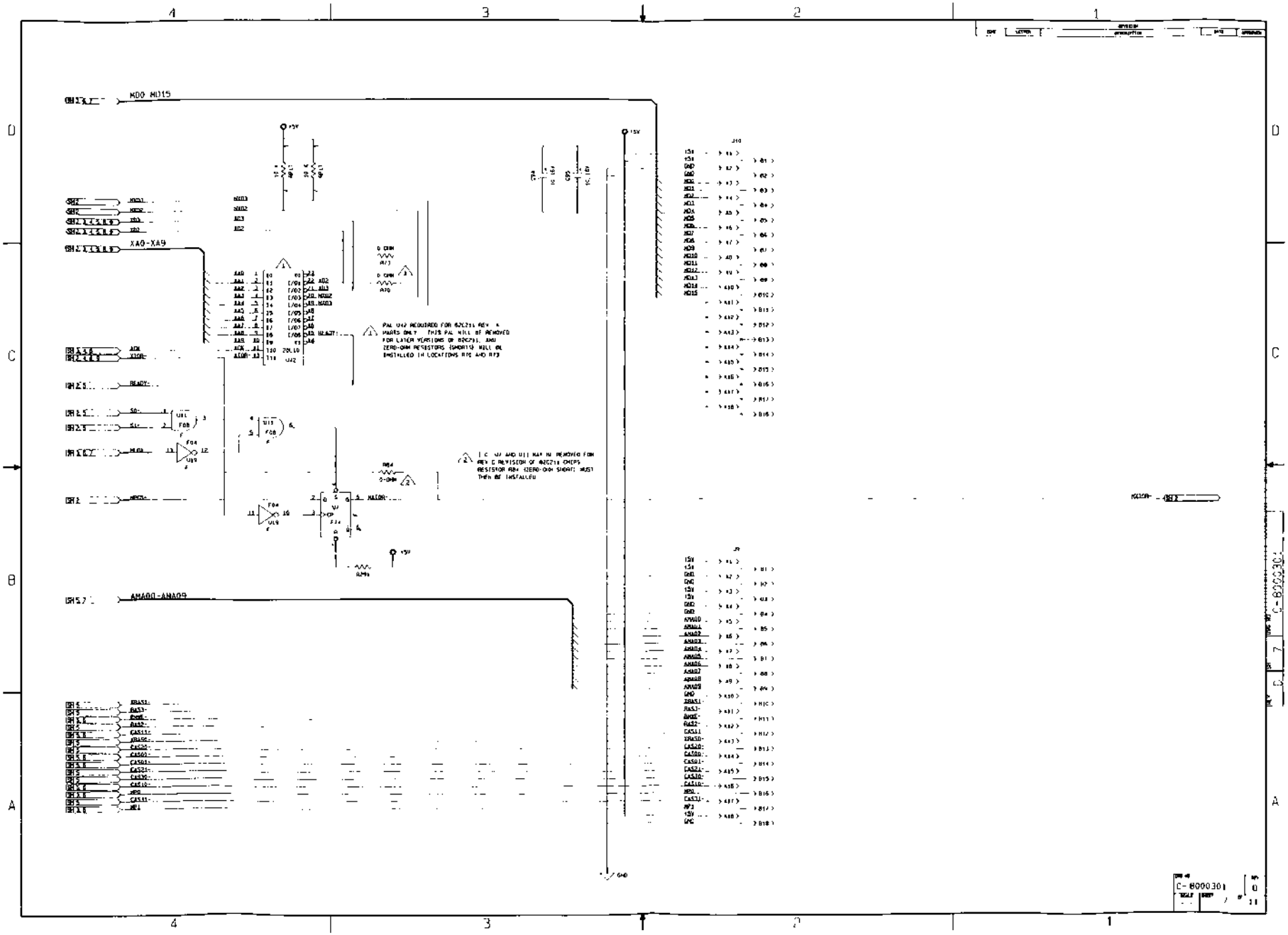

80286
U13
U28
82C211
CPU/BUS CONTROLLER
D0-D15
A0-A19, CPU420, A21-A23
NXD2, NXD3, XD0-XD7
OPTIONAL COPROCESSOR OSC
OPTIONAL (NON OSCILLATOR FOR SPECIAL AT-BUS CLOCK
C-B000301
D
2
11

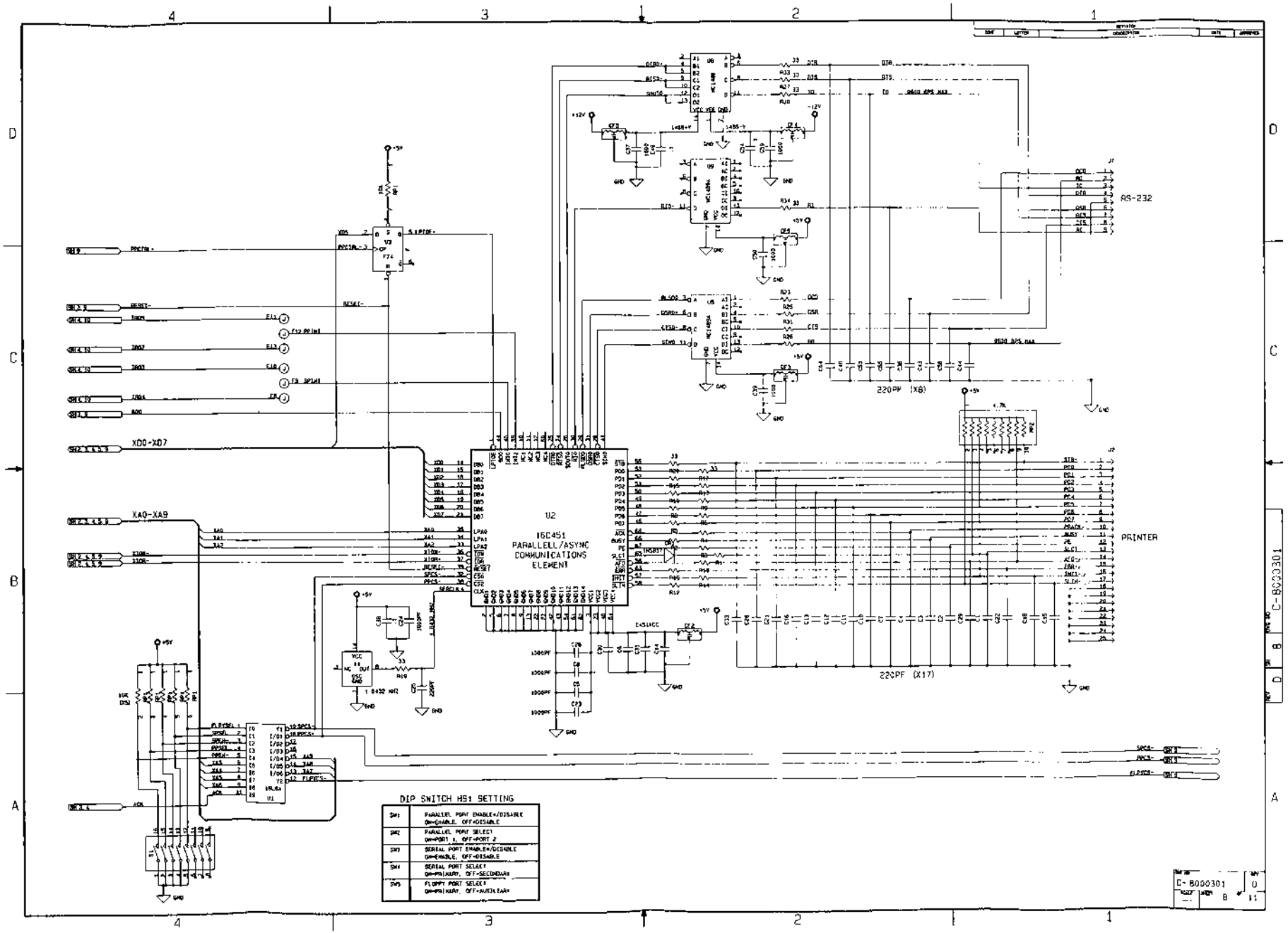

LA17-LA23
SA0-SA19
XA1-XA16
MD0-MD15
SD0-SD7
A0-A16
U27
82C215
DATA/ADDRESS BUFFER
C-8000301
3
11

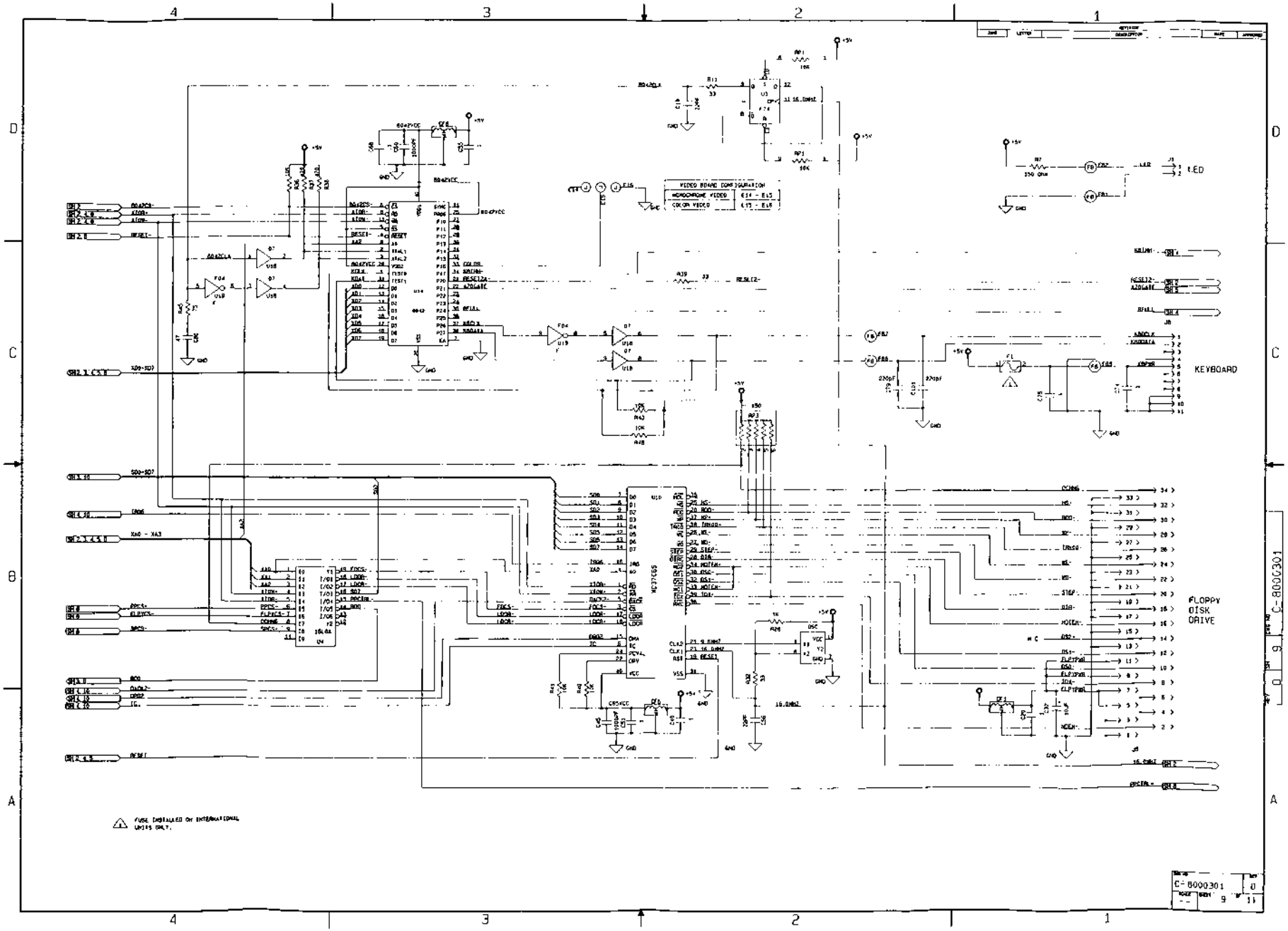

XA0-XA16
A17-A23
DRQ0-3
DRQ5-7
U41
82C206
INTEGRATED PERIPHERALS
CONTROLLER
(IPC)
XD0-XD7
SPKR
BAT1
KEYBOARD
LOCK
RESET
C-8000301

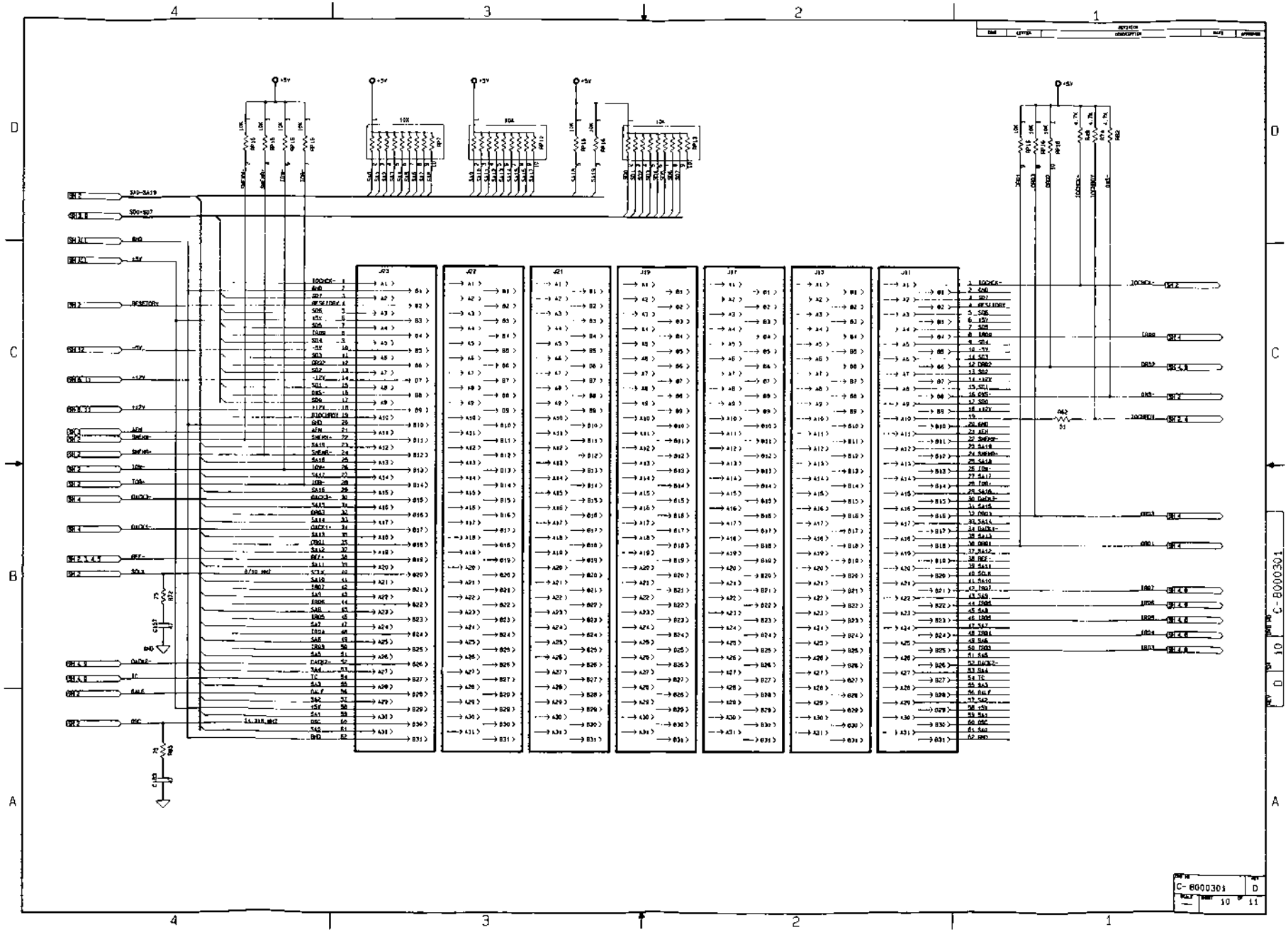

U36
82C212
PAGE/INTERLEAVE AND
EMS MEMORY CONTROLLER
DRAM BANK SELECT
ROM TYPE
EVEN
ODD
ROM TYPE
SEE TABLE
FOR JUMPER
SELECTION
C-B000301

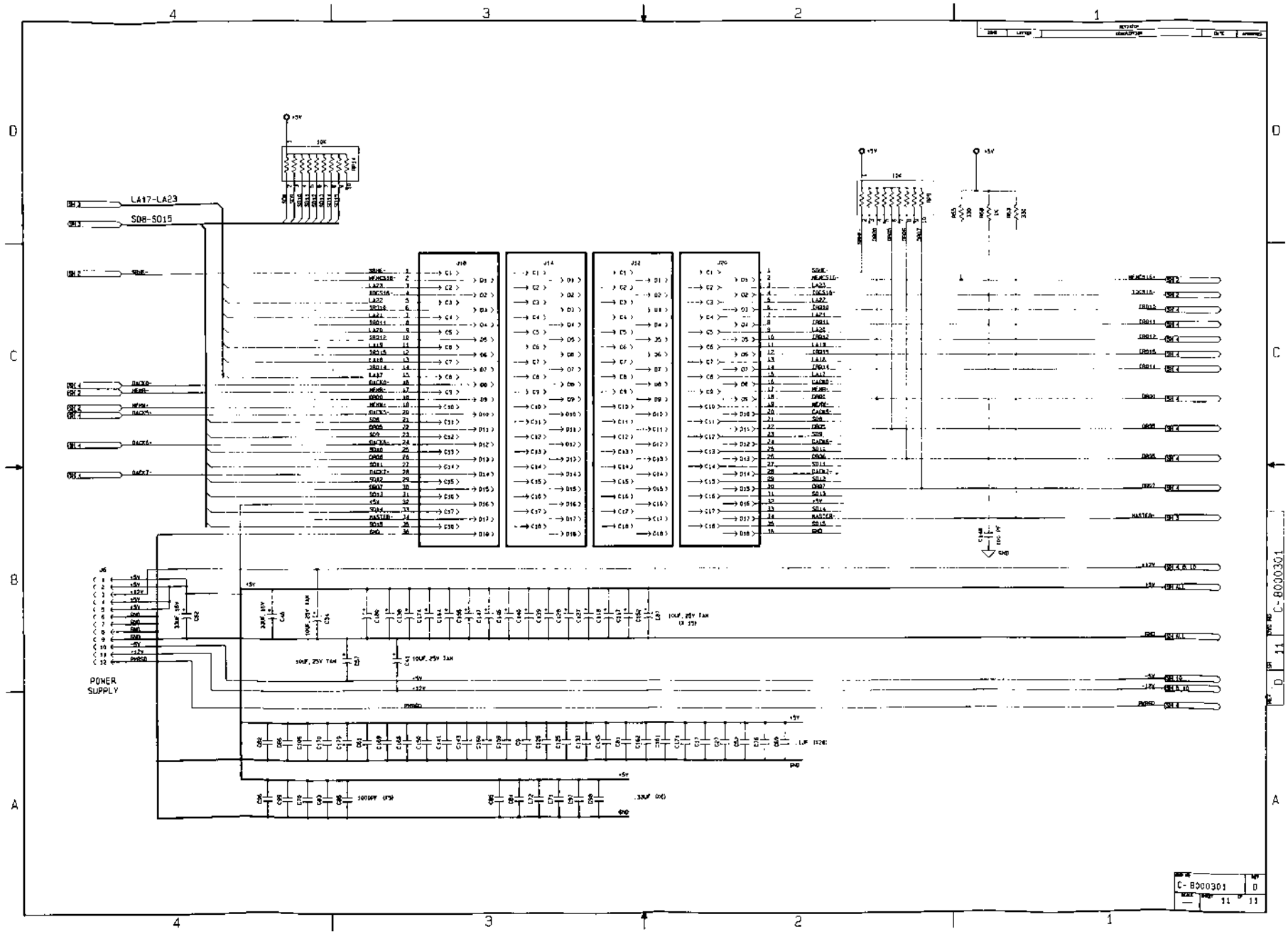

BANK 0
(512K)
BANK 1
(128K OPTIONAL)
MD0-MD15
CASO0-
AMA00 AMA09
CASO1-
MD0-MD7
AMA00-AMA07
MD8-MD15
AMA00-AMA07
256K x 9
256K x 4
C-8000301
0
5
11

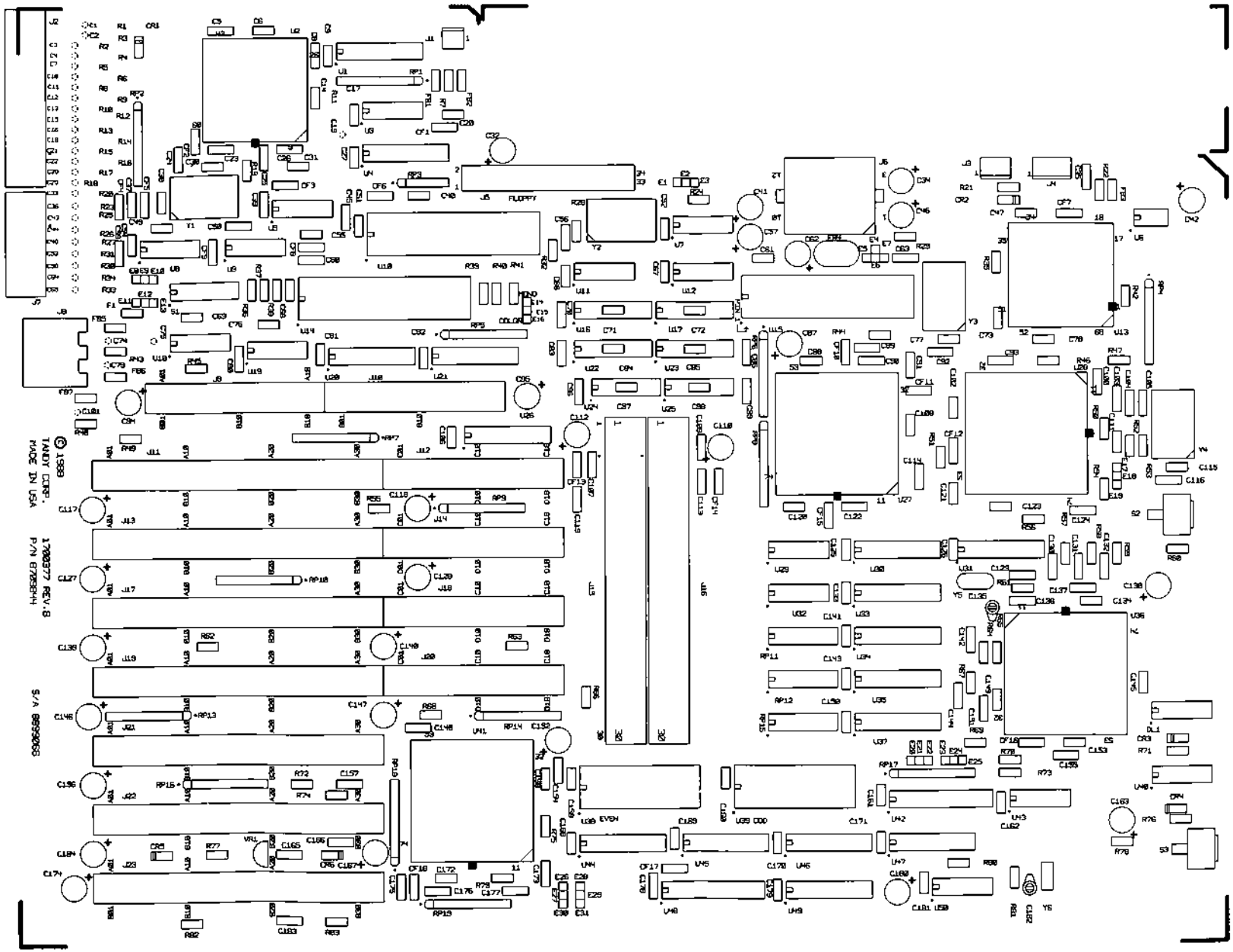

MD0-MD15
XA0-XA9
AMA00-AMA09
PAL U42 REQUIRED FOR 82C211 REV. A PARTS ONLY. THIS PAL WILL BE REMOVED FOR LATER VERSIONS OF 82C211, AND ZERO-OHM RESISTORS (SHORTS) WILL BE INSTALLED IN LOCATIONS RP2 AND RP3
J10
J9
C-8000301


U2
16C451
PARALLELL/ASYNC
COMMUNICATIONS
ELEMENT
RS-232
PRINTER
XD0-XD7
XA0-XA9
220PF (X8)
220PF (X17)
DIP SWITCH HS1 SETTING
SW1 PARALLEL PORT ENABLE#/DISABLE ON=ENABLE, OFF=DISABLE
SW2 PARALLEL PORT SELECT ON=PORT 1, OFF=PORT 2
SW3 SERIAL PORT ENABLE#/DISABLE ON=ENABLE, OFF=DISABLE
SW4 SERIAL PORT SELECT ON=PRIMARY, OFF=SECONDARY
SW5 FLOPPY PORT SELECT ON=PRIMARY, OFF=AUXILIARY
C-B000301
B

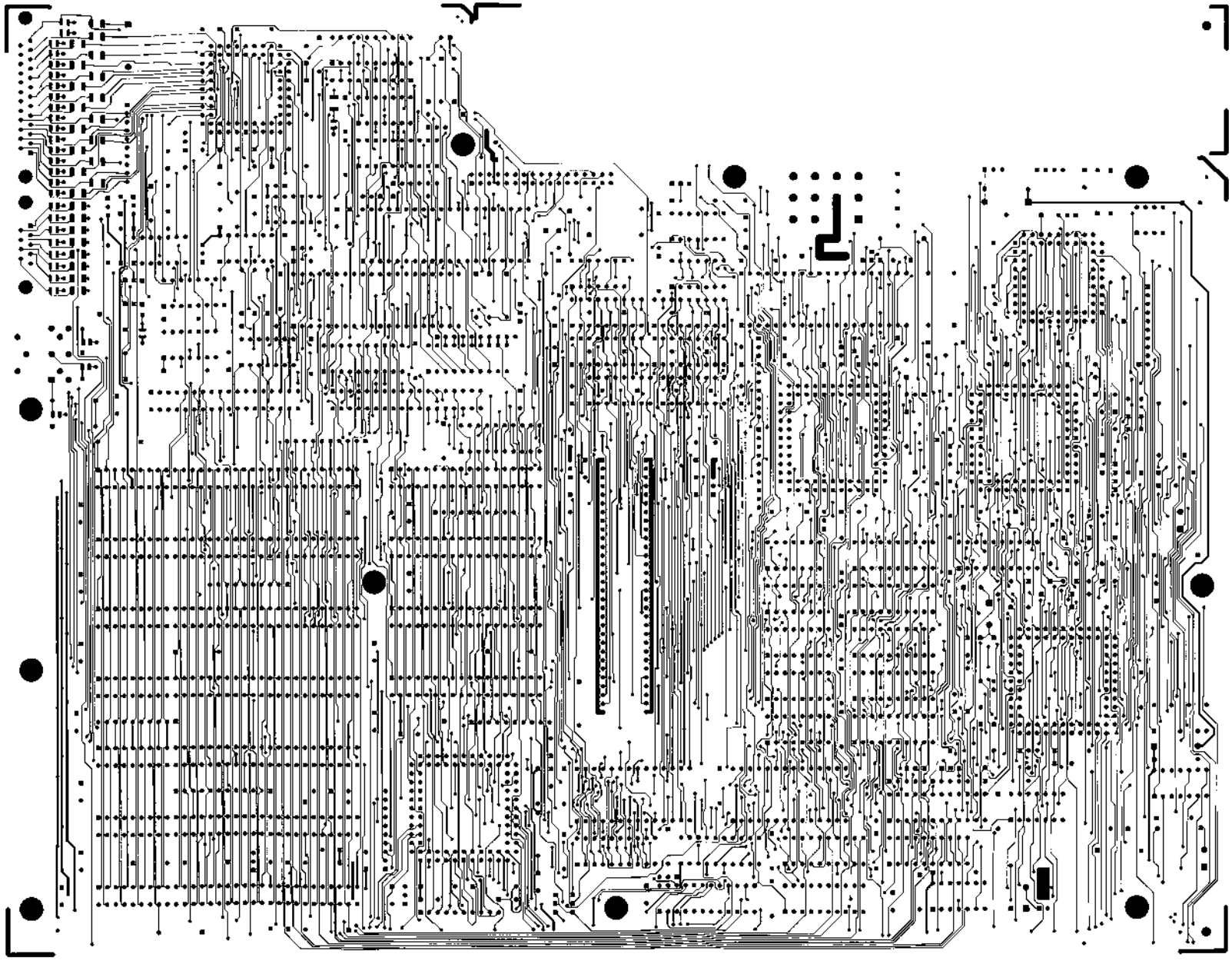

KEYBOARD
FLOPPY DISK DRIVE
LED
VIDEO BOARD CONFIGURATION
MONOCHROME VIDEO
COLOR VIDEO
C-8000301
FUSE INSTALLED ON INTERNATIONAL UNITS ONLY.


J23
J27
J21
J19
J17
J13
J11
C-8000301
D
10
11

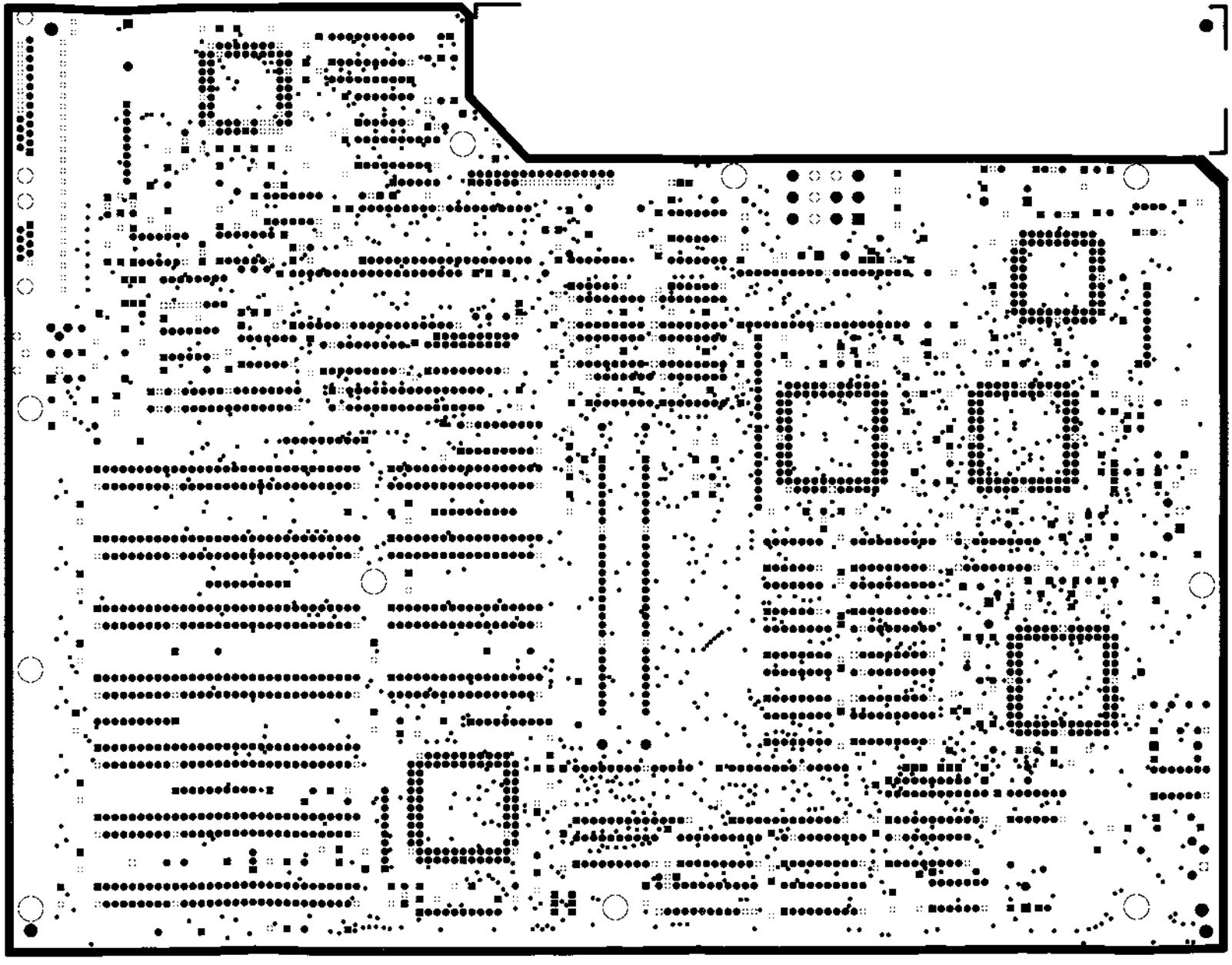

LA17-LA23
SD8-SD15
POWER SUPPLY
C-B000301
11



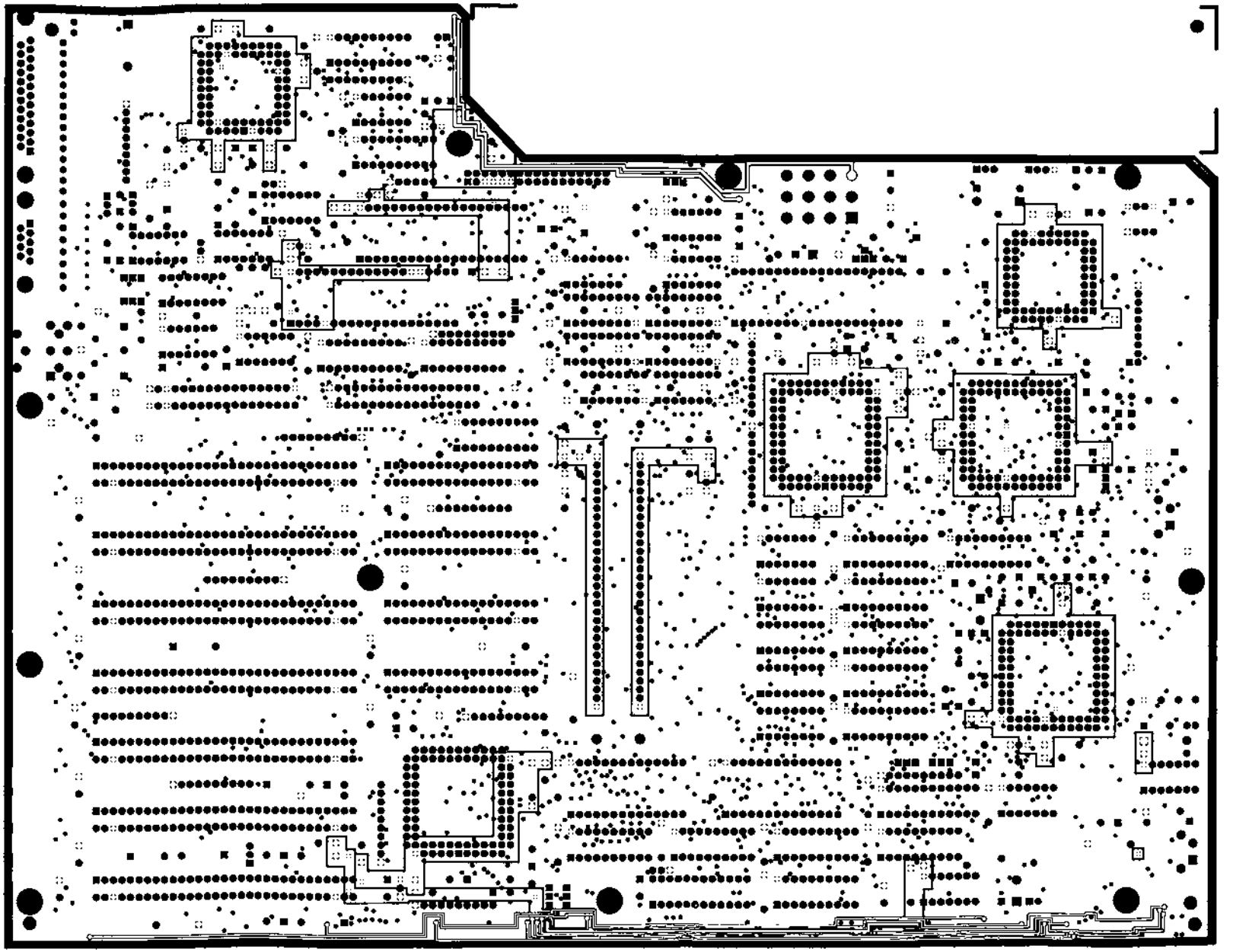

1700377 REV.B
6/3/88
LAYER TOP SILKSCREEN



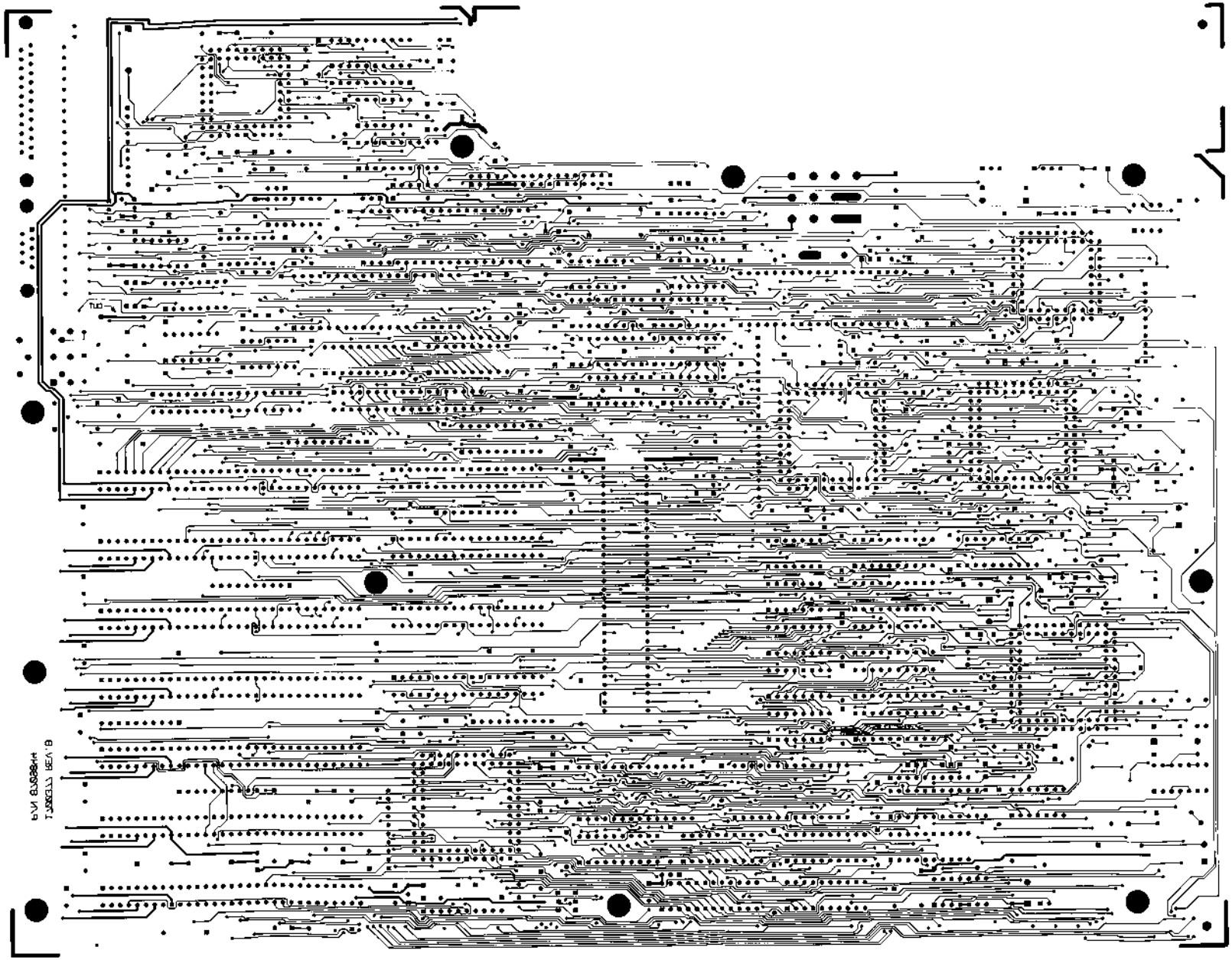
1700377 REV.B
6/3/88
LAYER 1 TOP SIDE



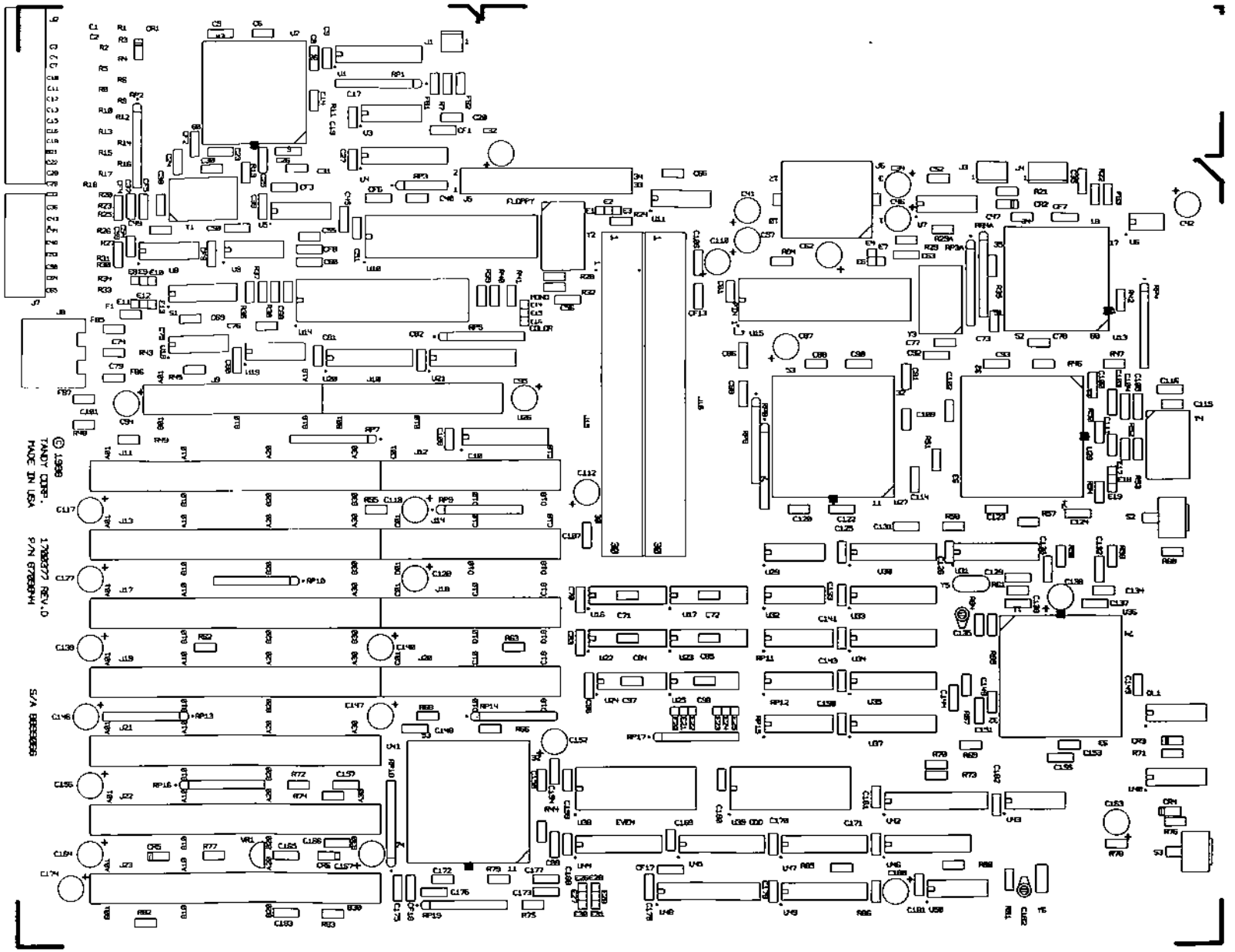
1700377 REV.B
6/3/88
LAYER 2 GROUND PLANE



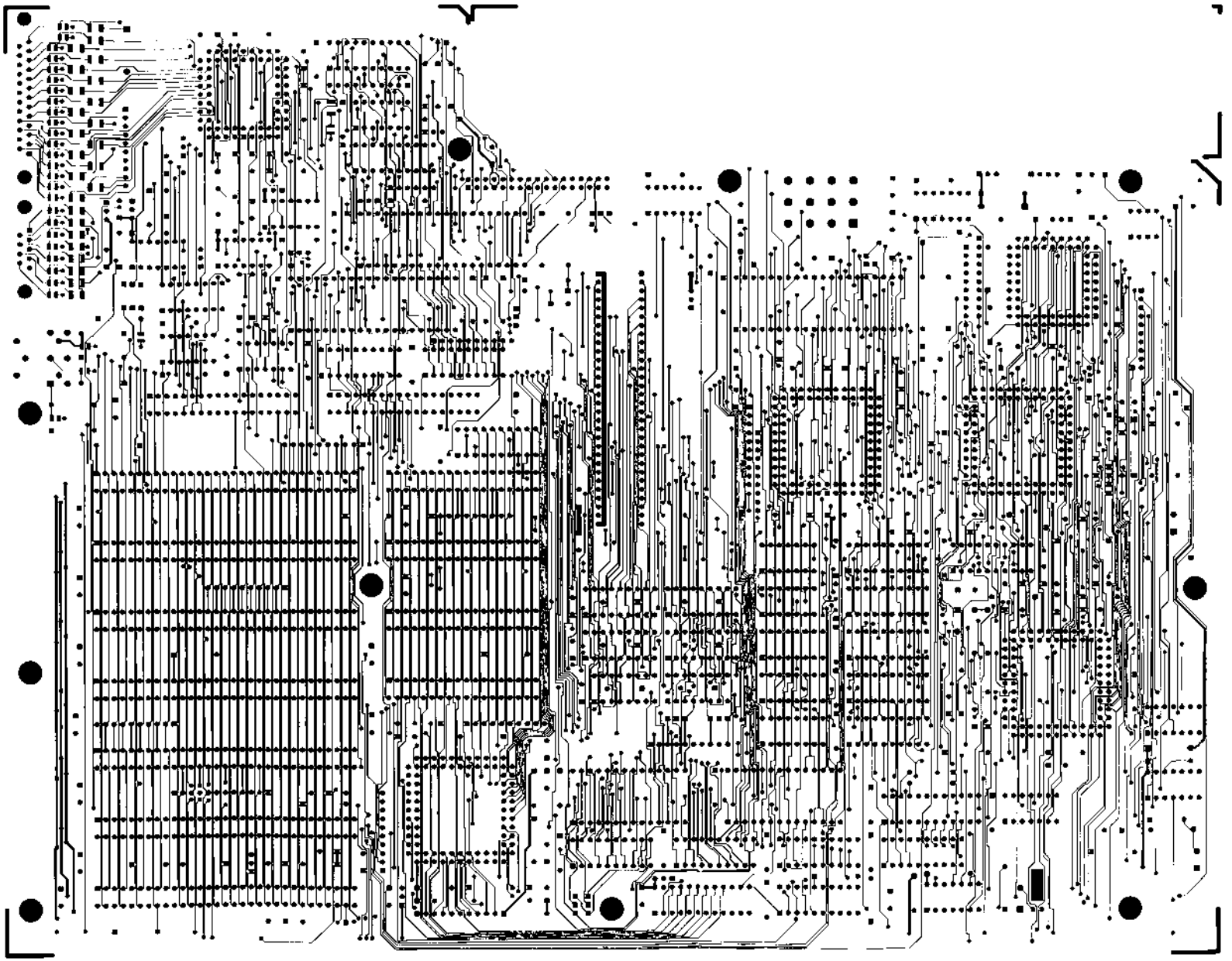
1700377 REV.B
6/3/88 LAYER 3 +5V PLANE



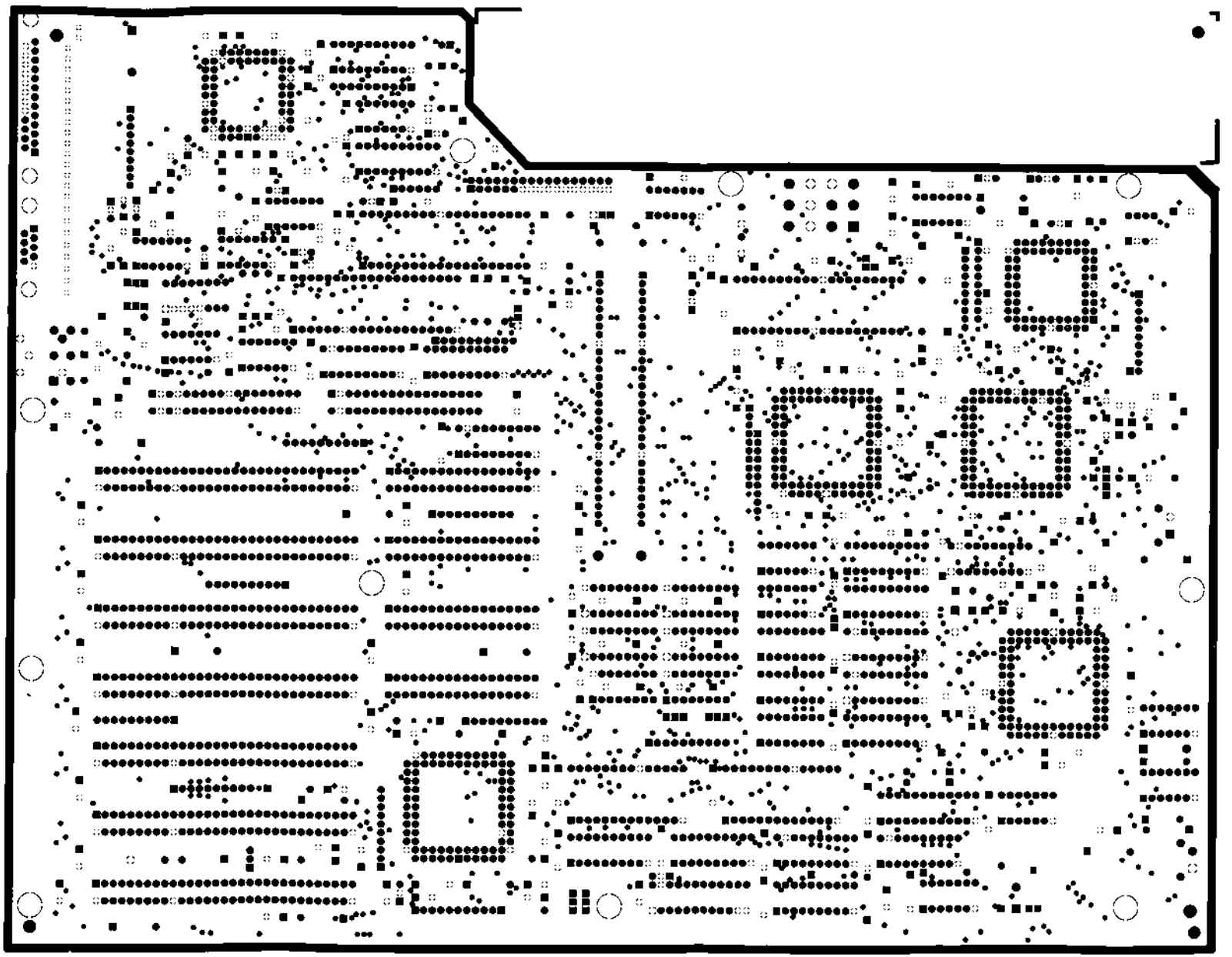
1700377 REV.8
6/3/88
LAYER 4 BOTTOM SIDE



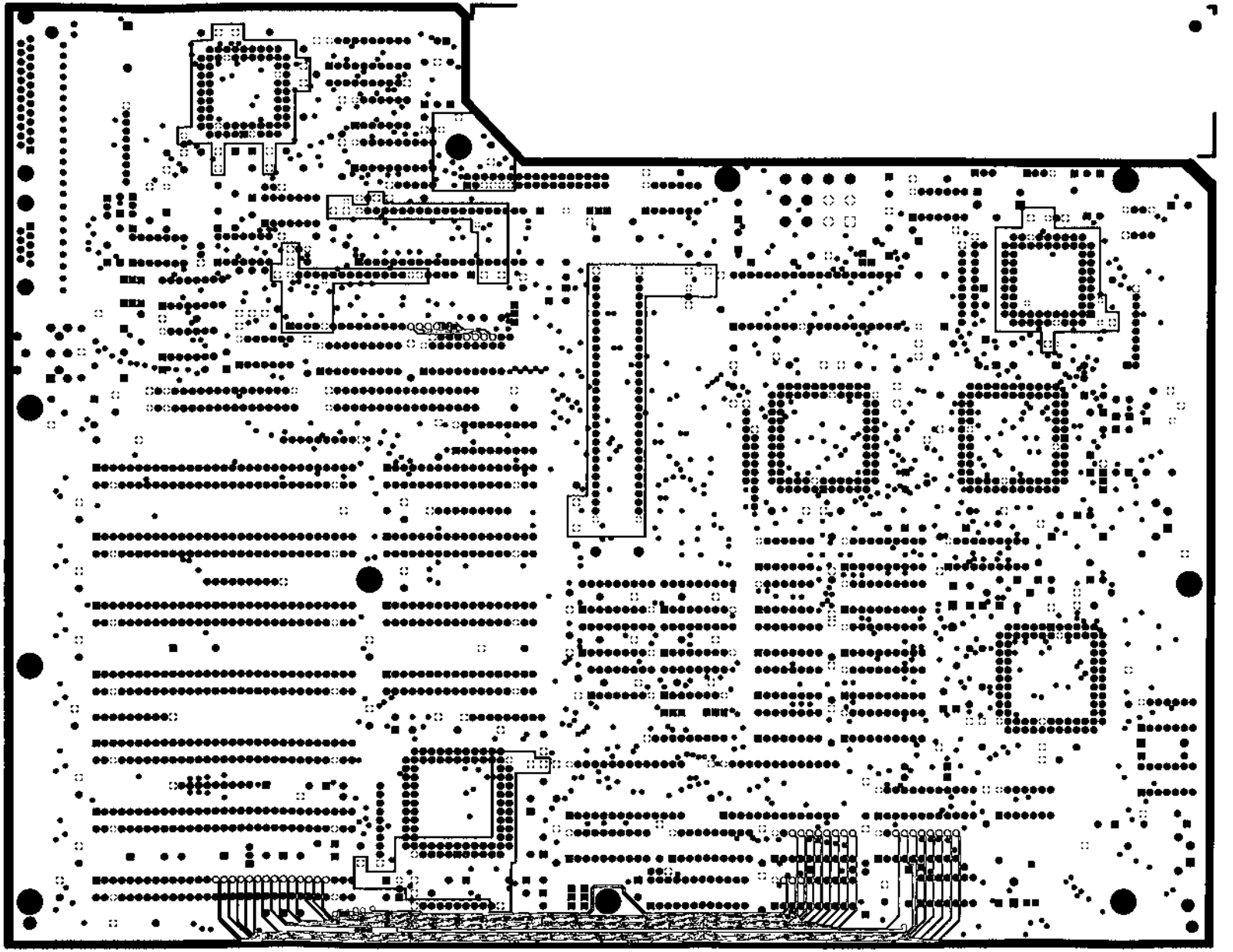

1700377 REV.D
8/11/88
LAYER TOP SILKSCREEN



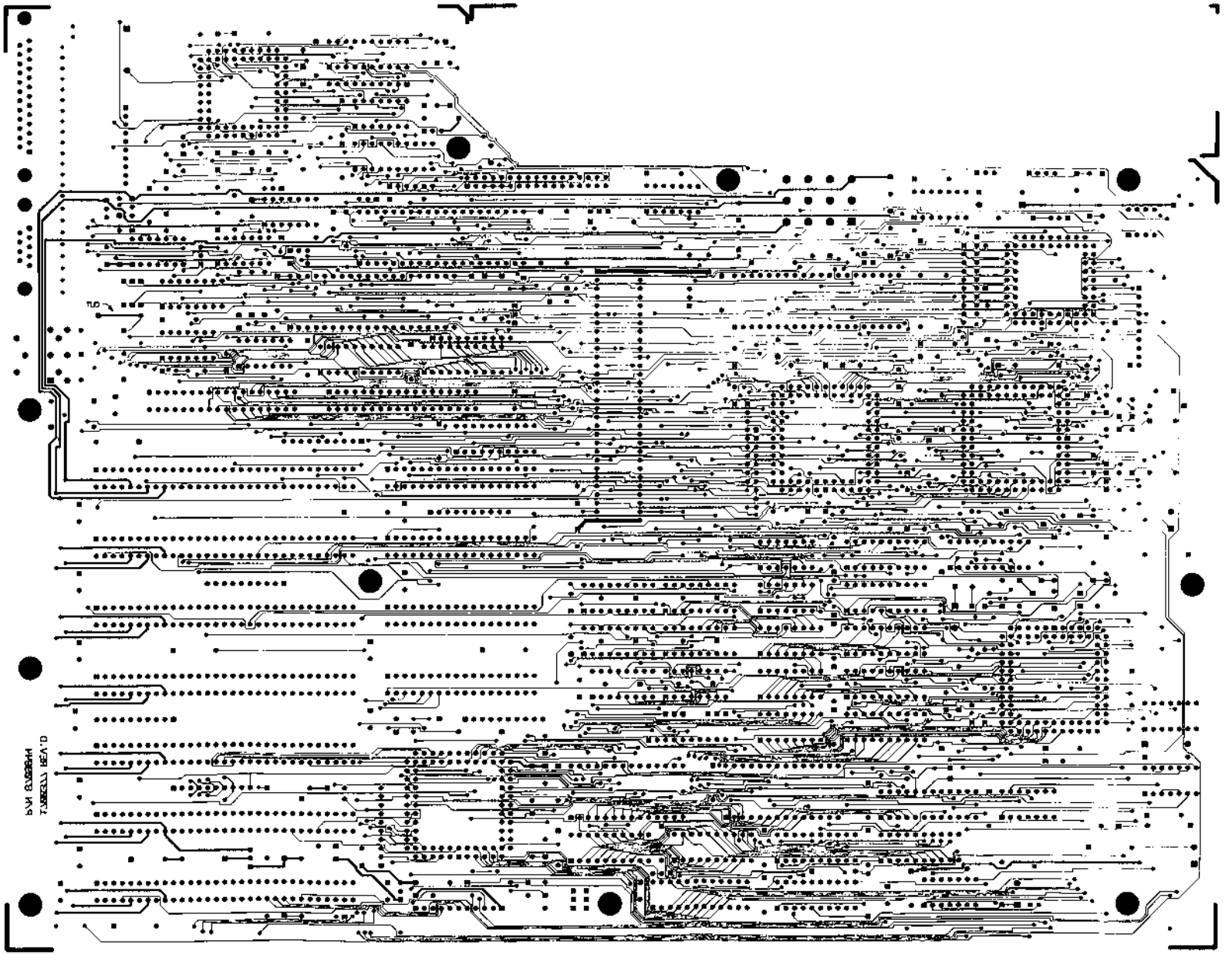
1700377 REV.D
8/11/88
LAYER 1 TOP SIDE



1700377 REV.D
8/11/88
LAYER 2 GROUND PLANE



1700377 REV.D
8/11/88 LAYER 3 +5V PLANE



1700377 REV.D
8/11/88
LAYER 4 BOTTOM SIDE

Devices

PRELIMINARY

# UPI™-41, 42: 8041AH/8042AH/8741AH/8742AH UNIVERSAL PERIPHERAL INTERFACE 8-BIT SLAVE MICROCONTROLLER

- UPI-41: 6 MHz; UPI-42: 12 MHz
- Pin, Software and Architecturally Compatible with all UPI-41 and UPI-42 Products
- 8-Bit CPU plus ROM/EPROM, RAM, I/O, Timer/Counter and Clock in a Single Package
- 2048 x 8 ROM/EPROM, 256 x 8 RAM on UPI-42, 1024 x 8 ROM/EPROM, 128 x 8 RAM on UPI-41, 8-Bit Timer/Counter, 18 Programmable I/O Pins
- One 8-Bit Status and Two Data Registers for Asynchronous Slave-to-Master Interface
- DMA, Interrupt, or Polled Operation Supported
- Fully Compatible with all Intel and Most Other Microprocessor Families
- Interchangeable ROM and EPROM Versions
- Expandable I/O
- Sync Mode Available
- Over 90 Instructions: 70% Single Byte
- Available in EXPRESS — Standard Temperature Range
- Intelligent Programming™ Algorithm — Fast EPROM Programming
- Available in 40-Lead Cerdip, 40-Lead Plastic and 44-Lead Plastic Leaded Chip Carrier Packages

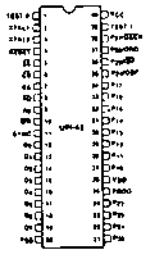
(See Packaging Spec., Order #231369)

The Intel UPI-41 and UPI-42 are general-purpose Universal Peripheral Interfaces that allow the designer to develop customized solutions for peripheral device control.

They are essentially "slave" microcontrollers, or microcontrollers with a slave interface included on the chip. Interface registers are included to enable the UPI device to function as a slave peripheral controller in the MCS™ Modules and iAPX family, as well as other 8-, 16-bit systems.

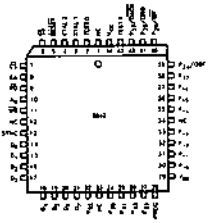
To allow full user flexibility, the program memory is available in ROM, One-Time Programmable EPROM (OTP) and UV-erasable EPROM. All UPI-41 and UPI-42 devices are fully pin compatible for easy transition from prototype to production level designs. These are the memory configurations available.

| UPI Device | ROM | EPROM | RAM | Programming Voltage |
|---|---|---|---|---|
| 8042AH | 2K | — | 256 | — |
| 8742AH | — | 2K | 256 | 12.5V |
| 8041AH | 1K | — | 128 | — |
| 8741AH | — | 1K | 128 | 12.5V |



210393-2

Figure 1. DIP Pin Configuration



210393-3

Figure 2. PLCC Pin Configuration



October 1987
Order Number: 210393-004

**Table 1. Pin Description**

| Symbol | DIP Pin No. | PLCC Pin No. | Type | Name and Function |
|---|---|---|---|---|
| TEST 0, TEST 1 | 1<br>39 | 2<br>43 | I | **TEST INPUTS:** Input pins which can be directly tested using conditional branch instructions.<br>**FREQUENCY REFERENCE: TEST 1 ($T_1$)** also functions as the event timer input (under software control). **TEST 0 ($T_0$)** is used during PROM programming and ROM/EPROM verification. It is also used during Sync Mode to reset the instruction state to S1 and synchronize the internal clock to PH1. See the Sync Mode Section. |
| XTAL 1, XTAL 2 | 2<br>3 | 3<br>4 | I | **INPUTS:** Inputs for a crystal, LC or an external timing signal to determine the internal oscillator frequency. |
| $\overline{RESET}$ | 4 | 5 | I | **RESET:** Input used to reset status flip-flops and to set the program counter to zero. $\overline{RESET}$ is also used during EPROM programming and verification. |
| $\overline{SS}$ | 5 | 6 | I | **SINGLE STEP:** Single step input used in conjunction with the SYNC output to step the program through each instruction (EPROM). This should be tied to +5V when not used. This pin is also used to put the device in Sync Mode by applying 12.5V to it. |
| $\overline{CS}$ | 6 | 7 | I | **CHIP SELECT:** Chip select input used to select one UPI microcomputer out of several connected to a common data bus. |
| EA | 7 | 8 | I | **EXTERNAL ACCESS:** External access input which allows emulation, testing and ROM/EPROM verification. This pin should be tied low if unused. |
| $\overline{RD}$ | 8 | 9 | I | **READ:** I/O read input which enables the master CPU to read data and status words from the OUTPUT DATA BUS BUFFER or status register. |
| $A_0$ | 9 | 10 | I | **COMMAND/DATA SELECT:** Address input used by the master processor to indicate whether byte transfer is data ($A_0$ = 0, F1 is reset) or command ($A_0$ = 1, F1 is set). $A_0$ = 0 during program and verify operations. |
| $\overline{WR}$ | 10 | 11 | I | **WRITE:** I/O write input which enables the master CPU to write data and command words to the UPI INPUT DATA BUS BUFFER. |
| SYNC | 11 | 13 | O | **OUTPUT CLOCK:** Output signal which occurs once per UPI instruction cycle. SYNC can be used as a strobe for external circuitry; it is also used to synchronize single step operation. |
| $D_0$–$D_7$ (BUS) | 12–19 | 14–21 | I/O | **DATA BUS:** Three-state, bidirectional DATA BUS BUFFER lines used to interface the UPI microcomputer to an 8-bit master system data bus. |
| $P_{10}$–$P_{17}$ | 27–34 | 30–33<br>35–38 | I/O | **PORT 1:** 8-bit, PORT 1 quasi-bidirectional I/O lines. $P_{10}$–$P_{17}$ access the signature row and security bit. |
| $P_{20}$–$P_{27}$ | 21–24<br>35–38 | 24–27<br>39–42 | I/O | **PORT 2:** 8-bit, PORT 2 quasi-bidirectional I/O lines. The lower 4 bits ($P_{20}$–$P_{23}$) interface directly to the 8243 I/O expander device and contain address and data information during PORT 4–7 access. The upper 4 bits ($P_{24}$–$P_{27}$) can be programmed to provide interrupt Request and DMA Handshake capability. Software control can configure $P_{24}$ as Output Buffer Full (OBF) interrupt, $P_{25}$ as Input Buffer Full ($\overline{IBF}$) interrupt, $P_{26}$ as DMA Request (DRQ), and $P_{27}$ as DMA ACKnowledge ($\overline{DACK}$). |
| PROG | 25 | 28 | I/O | **PROGRAM:** Multifunction pin used as the program pulse input during PROM programming. During I/O expander access the PROG pin acts as an address/data strobe to the 8243. This pin should be tied high if unused. |
| $V_{CC}$ | 40 | 44 | | **POWER:** +5V main power supply pin. |
| $V_{DD}$ | 26 | 29 | | **POWER:** +5V during normal operation. +12.5V during programming operation. Low power standby supply pin. |
| $V_{SS}$ | 20 | 22 | | **GROUND:** Circuit ground potential. |

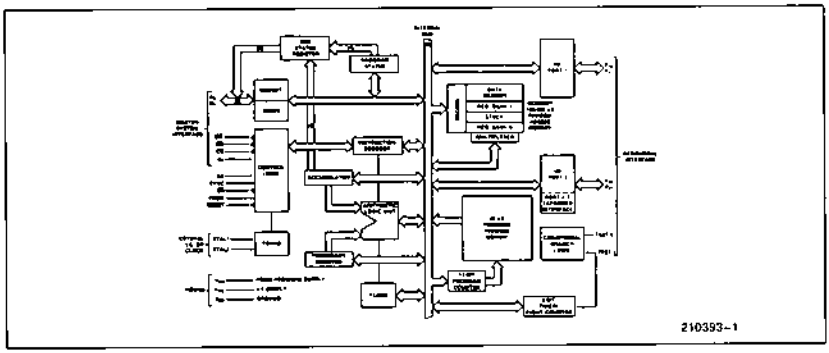
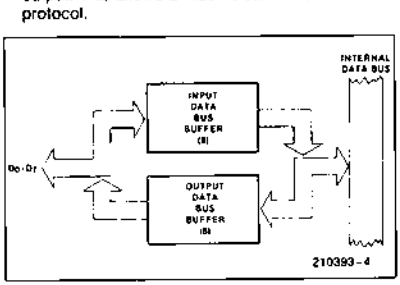



**Figure 3. Block Diagram**

## UPI-41 and UPI-42 FEATURES

1. Two Data Bus Buffers, one for input and one for output. This allows a much cleaner Master/Slave protocol.




2. 8 Bits of Status

| $ST_7$ | $ST_6$ | $ST_5$ | $ST_4$ | $F_1$ | $F_0$ | IBF | OBF |
|---|---|---|---|---|---|---|---|
| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |

$ST_4$–$ST_7$ are user definable status bits. These bits are defined by the "MOV STS, A" single byte, single cycle instruction. Bits 4–7 of the acccumulator are moved to bits 4–7 of the status register. Bits 0–3 of the status register are not affected.

**MOV STS, A Op Code: 90H**

| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|
| $D_7$ | | | | | | | $D_0$ |

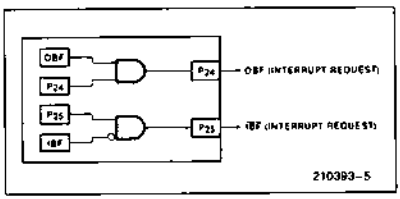
3. $\overline{RD}$ and $\overline{WR}$ are edge triggered. IBF, OBF, $F_1$ and INT change internally after the trailing edge of $\overline{RD}$ or $\overline{WR}$.

During the time that the host CPU is reading the status register, the UPI is prevented from updating this register or is 'locked out.'

4. $P_{24}$ and $P_{25}$ are port pins or Buffer Flag pins which can be used to interrupt a master processor. These pins default to port pins on Reset.

If the "EN FLAGS" instruction has been executed, $P_{24}$ becomes the OBF (Output Buffer Full) pin. A "1" written to $P_{24}$ enables the OBF pin (the pin outputs the OBF Status Bit). A "0" written to $P_{24}$ disables the OBF pin (the pin remains low). This pin can be used to indicate that valid data is available from the UPI (in Output Data Bus Buffer).

If "EN FLAGS" has been executed, $P_{25}$ becomes the $\overline{IBF}$ (Input Buffer Full) pin. A "1" written to $P_{25}$ enables the $\overline{IBF}$ pin (the pin outputs the inverse of the IBF Status Bit. A "0" written to $P_{25}$ disables the $\overline{IBF}$ pin (the pin remains low). This pin can be used to indicate that the UPI is ready for data.




**Data Bus Buffer Interrupt Capability**

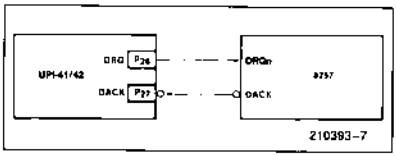
**EN FLAGS Op Code: 0F5H**

| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
|---|---|---|---|---|---|---|---|
| $D_7$ | | | | | | | $D_0$ |

5. $P_{26}$ and $P_{27}$ are port pins or DMA handshake pins for use with a DMA controller. These pins default to port pins on Reset.

   If the "EN DMA" instruction has been executed, $P_{26}$ becomes the DRQ (DMA Request) pin. A "1" written to $P_{26}$ causes a DMA request (DRQ is activated). DRQ is deactivated by DACK•RD, DACK•WR, or execution of the "EN DMA" instruction.

   If "EN DMA" has been executed, $P_{27}$ becomes the DACK (DMA ACKnowledge) pin. This pin acts as a chip select input for the Data Bus Buffer registers during DMA transfers.




**DMA Handshake Capability**

**EN DMA Op Code: 0E5H**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| $D_7$ | | | | | | | $D_0$ |

6. When EA is enabled on the UPI, the program counter is placed on Port 1 and the lower three bits of Port 2 (MSB = $P_{22}$, LSB = $P_{10}$). On the UPI this information is multiplexed with PORT DATA (see port timing diagrams at end of this data sheet).
7. The 8741AH and 8742AH support the intelligent Programming Algorithm. (See the Programming Section.)

## APPLICATIONS

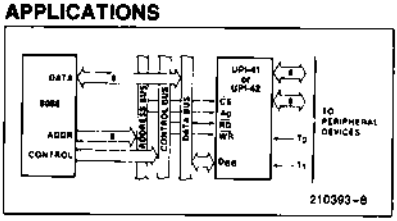



**Figure 3. 8088-UPI-41/42 Interface**

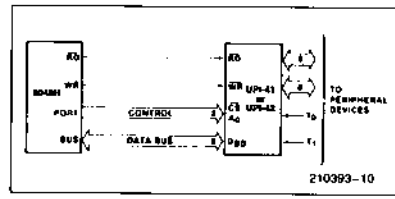



**Figure 4. 8048H-UPI-41/42 Interface**

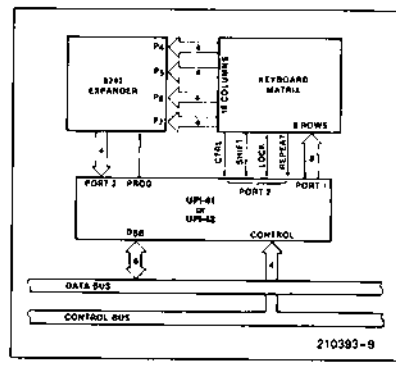



**Figure 5. UPI-41/42-8243 Keyboard Scanner**

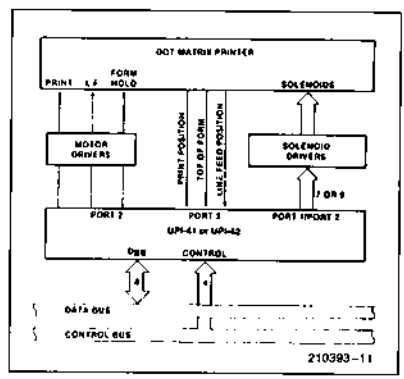



**Figure 6. UPI-41/42 80-Column Matrix Printer Interface**

## PROGRAMMING, VERIFYING, AND ERASING THE 8741AH and 8742AH EPROM

### Programming Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

| Pin | Function |
|---|---|
| XTAL 1 | 2 Clock Inputs |
| $\overline{\text{Reset}}$ | Initialization and Address Latching |
| Test 0 | Selection of Program or Verify Mode |
| EA | Activation of Program/Verify Signature Row/Security Bit Modes |
| BUS | Address and Data Input<br>Data Output During Verify |
| $P_{20-22}$ | Address Input |
| $V_{DD}$ | Programming Power Supply |
| PROG | Program Pulse Input |

**WARNING**
An attempt to program a missocketed 8741AH or 8742AH will result in severe damage to the part. An indication of a properly socketed part is the appearance of the SYNC clock output. The lack of this clock may be used to disable the programmer.

The Program/Verify sequence is:

1. CS = 5V, $V_{CC}$ = 5V, $V_{DD}$ = 5V, RESET = 0V, $A_0$ = 0V, TEST 0 = 5V, clock applied or internal oscillator operating, BUS floating, PROG = 5V.
2. Insert 8741AH or 8742AH in programming socket
3. TEST 0 = 0V (select program mode)
4. EA = 12.5V (active program mode)
5. $V_{CC}$ = 6V (programming supply)
6. $V_{DD}$ = 12.5V (programming power)
7. Address applied to BUS and $P_{20-22}$
8. $\overline{\text{RESET}}$ = 5V (latch address)
9. Data applied to BUS
10. PROG = 5V followed by one 1 ms pulse to 0V
11. TEST 0 = 5V (verify mode)
12. Read and verify data on BUS
13. TEST 0 = 0V
14. Apply overprogram pulse
15. $\overline{\text{RESET}}$ = 0V and repeat from step 6
16. Programmer should be at conditions of step 1 when 8741AH or 8742AH is removed from socket

Please follow the intelligent Programming flow chart for proper programming procedure.

### 8741AH/8742AH Erasure Characteristics

The erasure characteristics of the 8741AH/8742AH are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 8741AH/8742AH in approximately 3 years while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 8741AH/8742AH is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8741AH/8742AH window to prevent unintentional erasure.

The recommended erasure procedure for the 8741AH/8742AH is exposure to shortwave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 w-sec/cm$^2$. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 $\mu$W/cm$^2$ power rating. The 8741AH/8742AH should be placed within one inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Exposure of the 8741AH/8742AH to high intensity UV light for long periods may cause permanent damage.

### intelligent Programming™ Algorithm

The intelligent Programming Algorithm rapidly programs Intel 8741AH/8742AH EPROMs using an efficient and reliable method particularly suited to the production programming environment. Typical programming time for individual devices is on the order of 10 seconds. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the 8741AH/8742AH intelligent Programming Algorithm is shown in Figure 7.

The intelligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial PROG pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular 8741AH/8742AH location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

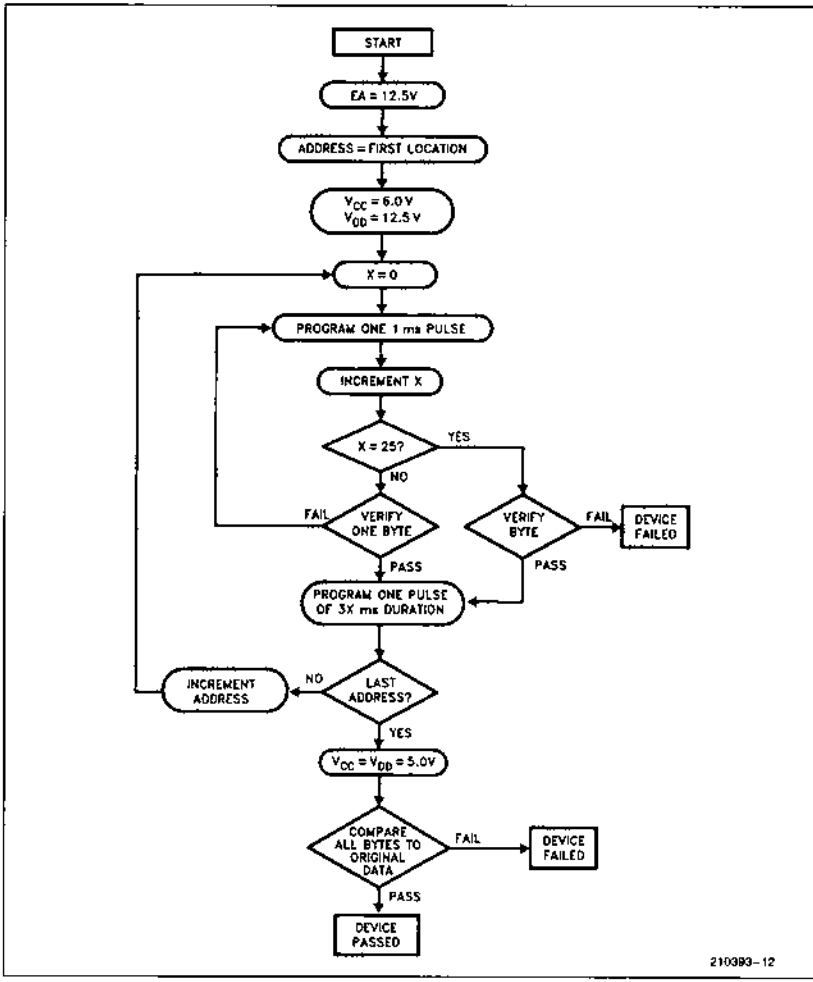

START
EA = 12.5V
ADDRESS = FIRST LOCATION
$V_{CC}$ = 6.0V
$V_{DD}$ = 12.5V
X = 0
PROGRAM ONE 1 ms PULSE
INCREMENT X
X = 25?
YES
NO
VERIFY ONE BYTE
FAIL
PASS
VERIFY BYTE
FAIL
PASS
DEVICE FAILED
PROGRAM ONE PULSE OF 3X ms DURATION
LAST ADDRESS?
NO
INCREMENT ADDRESS
YES
$V_{CC}$ = $V_{DD}$ = 5.0V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
DEVICE FAILED
PASS
DEVICE PASSED
210393-12

Figure 7

The entire sequence of program pulses and byte verifications is performed at $V_{CC}$ = 6.0V and $V_{DD}$ = 12.5V. When the intelligent Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC}$ = 5.0, $V_{DD}$ = 5V.

### Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with T0 = 5V, $V_{DD}$ = 5V, EA = 12.5V, $\overline{SS}$ = 5V, PROG = 5V, A0 = 0V, and $\overline{CS}$ = 5V.

## SECURITY BIT

The security bit is a single EPROM cell outside the EPROM array. The user can program this bit with the appropriate access code and the normal programming procedure, to inhibit any external access to the EPROM contents. Thus the user's resident program is protected. There is no direct external access to this bit. However, the security byte in the signature mode has the same address and can be used to check indirectly whether the security bit has been programmed or not. The security bit has no effect on the signature mode, so the security byte can always be examined.

## SECURITY BIT PROGRAMMING/ VERIFICATION

### Programming

a. Read the security byte of the signature mode. Make sure it is 00H.

b. Apply access code to appropriate inputs to put the device into security mode.

c. Apply high voltage to EA and $V_{DD}$ pins.

d. Follow the programming procedure as per the intelligent Programming Algorithm with known data on the databus. Not only the security bit, but also the security byte of the signature mode is programmed.

e. Verify that the security byte of the signature mode contains the same data as appeared on the data bus. (If DB0–DB7 = high, the security byte will contain FFH.)

f. Read two consecutive known bytes from the EPROM array and verify that the wrong data are retrieved in at least one verification. If the EPROM can still be read, the security bit may have not been fully programmed though the security byte in the signature mode has.

### Verification

Since the security bit address overlaps the address of the security byte of the signature mode, it can be used to check indirectly whether the security bit has been programmed or not. Therefore, the security bit verification is a mere read operation of the security byte of the signature row (1 = security bit programmed; 0 = security bit unprogrammed). Note that during the security bit programming, the reading of the security byte does not necessarily indicate that the security bit has been successfully programmed. Thus, it is recommended that two consecutive known bytes in the EPROM array be read and the wrong data should be read at least once, because it is highly improbable that random data coincides with the correct ones twice.

## SIGNATURE MODE

The UPI-41/42 has an additional 32 bytes of EPROM available for Intel and user signatures and miscellaneous purposes. The 32 bytes are partitioned as follows:

A. **Test code/checksum**—This can accommodate up to 25 bytes of code for testing the internal nodes that are not testable by executing from the external memory. The test code/checksum is present on ROMs, and OTPs.

B. **Intel signature**—This allows the programmer to read from the UPI-41/42 the manufacturer of the device and the exact product name. It facilitates automatic device identification and will be present in the ROM and OTP versions. Location 10H contains the manufacturer code. For Intel, it is 89H. Location 11H contains the device code. The code is 43H and 42H for the 8042AH and OTP 8742AH, and 41H and 40H for the 8041AH and OTP 8741AH, respectively.

C. **User signature**—The user signature memory is implemented in the EPROM and consists of 2 bytes for the customer to program his own signature code (for identification purposes and quick sorting of previously programmed materials).

D. **Test signature**—This memory is used to store testing information such as: test data, bin number, etc. (for use in quality and manufacturing control).

E. **Security byte**—This byte is used to check whether the security bit has been programmed (see the security bit section).

The signature mode can be accessed by setting P10 = 0, P11–P17 = 1, and then following the programming and/or verification procedures. The location of the various address partitions are as follows:

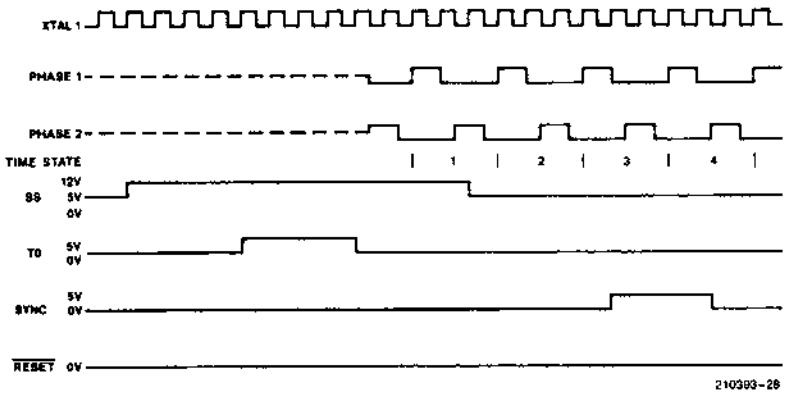
| | Address | | Device Type | No. of Bytes |
|---|---|---|---|---|
| Test Code/Checksum | 0<br>16H | 0FH<br>1EH | ROM/OTP | 25 |
| Intel Signature | 10H | 11H | ROM/OTP | 2 |
| User Signature | 12H | 13H | EPROM/OTP | 2 |
| Test Signature | 14H | 15H | ROM/OTP | 2 |
| Security Byte | 1FH | | EPROM/OTP | 1 |

## SYNC MODE

The UPI-41/42 has incorporated a new mode. The Sync Mode is provided to ease the design of multiple controller circuits by allowing the designer to force the device into known phase and state time. The Sync Mode may also be utilized by automatic test equipment (ATE) for quick, easy, and efficient synchronizing between the tester and the DUT (device under test).

Sync Mode is enabled when $\overline{SS}$ pin is raised to high voltage level of +12 volts. To begin synchronization, T0 is raised to 5 volts at least four clock cycles after $\overline{SS}$. T0 must be high for at least four X1 clock cycles to fully reset the prescaler and time state generators. T0 may then be brought down during low state of X1. Two clock cycles later, with the rising edge of X1, the device enters into Time State 1, Phase 1. $\overline{SS}$ is then brought down to 5 volts 4 clocks later after T0. RESET is allowed to go high 5 tCY (75 clocks) later for normal execution of code.

## SYNC MODE TIMING DIAGRAMS




**Minimum Specifications**
SYNC Operation Time, $t_{SYNC}$ = 3.5 XTAL 1 Clock cycles. Reset Time, $t_{RS}$ = 4 $t_{CY}$.

**NOTE:**
The rising and falling edges of T0 should occur during low state of XTAL1 clock.

## ACCESS CODE

**The following table summarizes the access codes required to invoke the Sync Mode, Signature Mode, and the Security Bit, respectively. Also, the programming and verification modes are included for comparison.**

| Modes | | Control Signals | | | | | | | Data Bus | | | | | | | | Port 2 | Access Code Port 1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | T0 | RST | SS | EA | PROG | $V_{DD}$ | $V_{CC}$ | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 1 2 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Programming Mode | | 0 | 0 | 1 | HV | 1 | $V_{DDH}$ | $V_{CC}$ | Address | | | | | | | | Addr | $a_0$ | $a_1$ | X | X | X | X | X | X |
| | | 0 | 1 | 1 | HV | STB | $V_{DDH}$ | $V_{CC}$ | Data In | | | | | | | | Addr | | | | | | | | |
| Verification Mode | | 0 | 0 | 1 | HV | 1 | $V_{CC}$ | $V_{CC}$ | Address | | | | | | | | Addr | $a_0$ | $a_1$ | X | X | X | X | X | X |
| | | 1 | 1 | 1 | HV | 1 | $V_{CC}$ | $V_{CC}$ | Data Out | | | | | | | | Addr | | | | | | | | |
| Sync Mode | | STB High | 0 | HV | 0 | X | $V_{CC}$ | $V_{CC}$ | X | X | X | X | X | X | X | X | X X X | X | X | X | X | X | X | X | X |
| Signature Mode | Prog | 0 | 0 | 1 | HV | 1 | $V_{DDH}$ | $V_{CC}$ | Addr. (see Sig Mode Table) | | | | | | | | 0 0 0 | 0 | 1 | 1 | 1 | 1 | X | X | 1 |
| | | 0 | 1 | 1 | HV | STB | $V_{DDH}$ | $V_{CC}$ | Data In | | | | | | | | 0 0 0 | | | | | | | | |
| | Verify | 0 | 0 | 1 | HV | 1 | $V_{CC}$ | $V_{CC}$ | Addr. (see Sig Mode Table) | | | | | | | | 0 0 0 | | | | | | | | |
| | | 1 | 1 | 1 | HV | 1 | $V_{CC}$ | $V_{CC}$ | Data Out | | | | | | | | 0 0 0 | | | | | | | | |
| Security Bit/Byte | Prog | 0 | 0 | 1 | HV | 1 | $V_{DDH}$ | $V_{CC}$ | Address | | | | | | | | 0 0 0 | | | | | | | | |
| | | 0 | 1 | 1 | HV | STB | $V_{DDH}$ | $V_{CC}$ | Data In | | | | | | | | 0 0 0 | | | | | | | | |
| | Verify | 0 | 0 | 1 | HV | 1 | $V_{CC}$ | $V_{CC}$ | Address | | | | | | | | 0 0 0 | | | | | | | | |
| | | 1 | 1 | 1 | HV | 1 | $V_{CC}$ | $V_{CC}$ | Data Out | | | | | | | | 0 0 0 | | | | | | | | |

**NOTES:**
1. $a_0$ = 0 or 1; $a_1$ = 0 or 1. $a_0$ must = $a_1$.

## ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin with
Respect to Ground.....−0.5V to +7V
Power Dissipation .....1.5 W

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*NOTICE: Specifications contained within the following tables are subject to change.*

## D.C. CHARACTERISTICS $T_A$ = 0°C to +70°C, $V_{CC}$ = $V_{DD}$ = +5V ±10%

| Symbol | Parameter | 8042/8742 Min | 8042/8742 Max | Units | Notes |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage (Except XTAL1, XTAL2, RESET) | −0.5 | 0.8 | V | |
| $V_{IL1}$ | Input Low Voltage (XTAL1, XTAL2, RESET) | −0.5 | 0.6 | V | |
| $V_{IH}$ | Input High Voltage (Except XTAL1, XTAL2, RESET) | 2.0 | $V_{CC}$ | V | |
| $V_{IH1}$ | Input High Voltage (XTAL1, RESET) | 3.5 | $V_{CC}$ | V | |
| $V_{IH2}$ | Input High Voltage (XTAL2) | 2.2 | $V_{CC}$ | V | |
| $V_{OL}$ | Output Low Voltage ($D_0$–$D_7$) | | 0.45 | V | $I_{OL}$ = 2.0 mA |

## D.C. CHARACTERISTICS $T_A$ = 0°C to +70°C, $V_{CC}$ = $V_{DD}$ = +5V ±10% (Continued)

| Symbol | Parameter | 8042/8742 | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $V_{OL1}$ | Output Low Voltage ($P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$, Sync) | | 0.45 | V | $I_{OL}$ = 1.6 mA |
| $V_{OL2}$ | Output Low Voltage (PROG) | | 0.45 | V | $I_{OL}$ = 1.0 mA |
| $V_{OH}$ | Output High Voltage ($D_0$-$D_7$) | 2.4 | | V | $I_{OH}$ = −400 μA |
| $V_{OH1}$ | Output High Voltage (All Other Outputs) | 2.4 | | | $I_{OH}$ = −50 μA |
| $I_{IL}$ | Input Leakage Current ($T_0$, $T_1$, RD, WR, CS, $A_0$, EA) | | ±10 | μA | $V_{SS} \le V_{IN} \le V_{CC}$ |
| $I_{OFL}$ | Output Leakage Current ($D_0$-$D_7$, High Z State) | | ±10 | μA | $V_{SS}$ + 0.45 $\le V_{OUT} \le V_{CC}$ |
| $I_{LI}$ | Low Input Load Current ($P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | 0.3 | mA | $V_{IL}$ = 0.8V |
| $I_{LI1}$ | Low Input Load Current (RESET, SS) | | 0.2 | mA | $V_{IL}$ = 0.8V |
| $I_{DD}$ | $V_{DD}$ Supply Current | | 20 | mA | Typical = 8 mA |
| $I_{CC}$ + $I_{DD}$ | Total Supply Current | | 135 | mA | Typical = 80 mA |
| $I_{DD}$ Standby | Power Down Supply Current | | 20 | mA | Typical = 8 mA |
| $I_{IH}$ | Input Leakage Current ($P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | 100 | μA | $V_{IN}$ = $V_{CC}$ |
| $C_{IN}$ | Input Capacitance | | 10 | pF | $T_A$ = 25°C (1) |
| $C_{IO}$ | I/O Capacitance | | 20 | pF | $T_A$ = 25°C (1) |

**NOTE:**
1. Sampled, not 100% tested.

## D.C. CHARACTERISTICS—PROGRAMMING

$T_A$ = 25°C ±5°C, $V_{CC}$ = 6V ±0.25V, $V_{DD}$ = 12.5V ±0.5V

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $V_{DDH}$ | $V_{DD}$ Program Voltage High Level | 12 | 13 | V(1) |
| $V_{DDL}$ | $V_{DD}$ Voltage Low Level | 4.75 | 5.25 | V |
| $V_{PH}$ | PROG Program Voltage High Level | 2.0 | 5.5 | V |
| $V_{PL}$ | PROG Voltage Low Level | −0.5 | 0.8 | V |
| $V_{EAH}$ | Input High Voltage for EA | 12.0 | 13.0 | V(2) |
| $V_{EAL}$ | EA Voltage Low Level | −0.5 | 5.25 | V |
| $I_{DD}$ | $V_{DD}$ High Voltage Supply Current | | 50.0 | mA |
| $I_{EA}$ | EA High Voltage Supply Current | | 1.0 | mA |

**NOTES:**
1. Voltages over 13V applied to pin $V_{DD}$ will permanently damage the device.
2. $V_{EAH}$ must be applied to EA before $V_{DDH}$ and removed after $V_{DDL}$.
3. $V_{CC}$ must be applied simultaneously or before $V_{DD}$ and must be removed simultaneously or after $V_{DD}$.

## A.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{SS} = 0V$, $V_{CC} = V_{DD} = +5V \pm 10\%$

**DBB READ**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{AR}$ | CS, $A_0$ Setup to RD ↓ | 0 | | ns |
| $t_{RA}$ | CS, $A_0$ Hold After RD ↑ | 0 | | ns |
| $t_{RR}$ | RD Pulse Width | 160 | | ns |
| $t_{AD}$ | CS, $A_0$ to Data Out Delay | | 130 | ns |
| $t_{RD}$ | RD ↓ to Data Out Delay | 0 | 130 | ns |
| $t_{DF}$ | RD ↑ to Data Float Delay | | 85 | ns |

**DBB WRITE**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{AW}$ | CS, $A_0$ Setup to WR ↓ | 0 | | ns |
| $t_{WA}$ | CS, $A_0$ Hold After WR ↑ | 0 | | ns |
| $t_{WW}$ | WR Pulse Width | 160 | | ns |
| $t_{DW}$ | Data Setup to WR ↑ | 130 | | ns |
| $t_{WD}$ | Data Hold After WR ↑ | 0 | | ns |

**CLOCK**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{CY}$ (UPI-41) | Cycle Time | 2.5 | 9.20 | μs(1) |
| $t_{CYC}$ (UPI-41) | Clock Period | 167 | 613 | ns |
| $t_{CY}$ (UPI-42) | Cycle Time | 1.25 | 9.20 | μs(1) |
| $t_{CYC}$ (UPI-42) | Clock Period | 83.3 | 613 | ns |
| $t_{PWH}$ | Clock High Time | 33 | | ns |
| $t_{PWL}$ | Clock Low Time | 33 | | ns |
| $t_R$ | Clock Rise Time | | 10 | ns |
| $t_F$ | Clock Fall Time | | 10 | ns |

**NOTE:**
1. $t_{CY} = 15/f(XTAL)$

## A.C. CHARACTERISTICS DMA

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{ACC}$ | DACK to WR or RD | 0 | | ns |
| $t_{CAC}$ | RD or WR to DACK | 0 | | ns |
| $t_{ACD}$ | DACK to Data Valid | 0 | 130 | ns |
| $t_{CRQ}$ | RD or WR to DRQ Cleared | | 110 | ns(1) |

**NOTE:**
1. $C_L = 150$ pF.

## A.C. CHARACTERISTICS—PROGRAMMING

$T_A$ = 25°C ±5°C, $V_{CC}$ = 6V ±0.25V, $V_{DDL}$ = +5V ±0.25V, $V_{DDH}$ = 12.5V ±0.5V
**(8741AH/8742AH ONLY)**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{AW}$ | Address Setup Time to RESET ↑ | $4t_{CY}$ | | |
| $t_{WA}$ | Address Hold Time After RESET ↑ | $4t_{CY}$ | | |
| $t_{DW}$ | Data in Setup Time to PROG ↓ | $4t_{CY}$ | | |
| $t_{WD}$ | Data in Hold Time After PROG ↑ | $4t_{CY}$ | | |
| $t_{PW}$ | Initial Program Pulse Width | 0.95 | 1.05 | ms(1) |
| $t_{TW}$ | Test 0 Setup Time for Program Mode | $4t_{CY}$ | | |
| $t_{WT}$ | Test 0 Hold Time After Program Mode | $4t_{CY}$ | | |
| $t_{DO}$ | Test 0 to Data Out Delay | | $4t_{CY}$ | |
| $t_{WW}$ | RESET Pulse Width to Latch Address | $4t_{CY}$ | | |
| $t_r$, $t_f$ | PROG Rise and Fall Times | 0.5 | 100 | μs |
| $t_{CY}$ | CPU Operation Cycle Time | 2.5 | 3.75 | μs |
| $t_{RE}$ | RESET Setup Time Before EA ↑ | $4t_{CY}$ | | |
| $t_{OPW}$ | Overprogram Pulse Width | 2.85 | 78.75 | ms(2) |
| $t_{DE}$ | EA High to $V_{DD}$ High | $1t_{CY}$ | | |

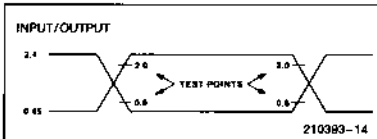
**NOTES:**
1. Typical Initial Program Pulse width tolerance = 1 ms ±5%.
2. This variation is a function of the iteration counter value, X.
3. If TEST 0 is high, $t_{DO}$ can be triggered by RESET ↑.

## A.C. CHARACTERISTICS PORT 2 $T_A$ = 0°C to +70°C, $V_{CC}$ = +5V ±10%

| Symbol | Parameter | f($t_{CY}$)(3) | Min | Max | Units |
|---|---|---|---|---|---|
| $t_{CP}$ | Port Control Setup Before Falling Edge of PROG | 1/15 $t_{CY}$ − 28 | 55 | | ns(1) |
| $t_{PC}$ | Port Control Hold After Falling Edge of PROG | 1/10 $t_{CY}$ | 125 | | ns(2) |
| $t_{PR}$ | PROG to Time P2 Input Must Be Valid | 8/15 $t_{CY}$ − 16 | | 650 | ns(1) |
| $t_{PF}$ | Input Data Hold Time | | 0 | 150 | ns(2) |
| $t_{DP}$ | Output Data Setup Time | 2/10 $t_{CY}$ | 250 | | ns(1) |
| $t_{PD}$ | Output Data Hold Time | 1/10 $t_{CY}$ − 80 | 45 | | ns(2) |
| $t_{PP}$ | PROG Pulse Width | 6/10 $t_{CY}$ | 750 | | ns |

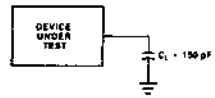
**NOTES:**
1. $C_L$ = 60 pF.
2. $C_L$ = 20 pF.
3. $t_{CY}$ = 1.25 μs.

## A.C. TESTING INPUT/OUTPUT WAVEFORM



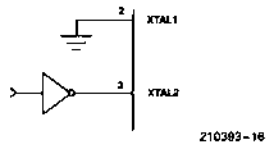

210393-14

## A.C. TESTING LOAD CIRCUIT

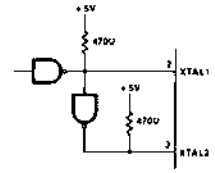



210393-15

## DRIVING FROM EXTERNAL SOURCE-TWO OPTIONS




210393-16

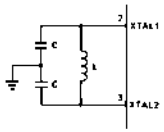



210393-17

Rise and Fall Times Should Not Exceed 10 ns. Resistors to $V_{CC}$ are Needed to Ensure $V_{IH}$ = 3.5V if TTL Circuitry is Used.

## LC OSCILLATOR MODE

| L | C | NOMINAL |
|---|---|---|
| 45 H | 20 pF | 5.2 MHz |
| 120 H | 20 pF | 3.2 MHz |




$$f = \frac{1}{2\pi\sqrt{LC'}}$$

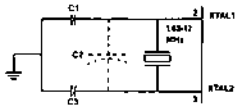
$$C' = \frac{C + 3Cpp}{2}$$

Cpp = 5–10 pF
Pin-to-Pin Capacitance

210393-18

Each C Should be Approximately 20 pF, including Stray Capacitance

## CRYSTAL OSCILLATOR MODE



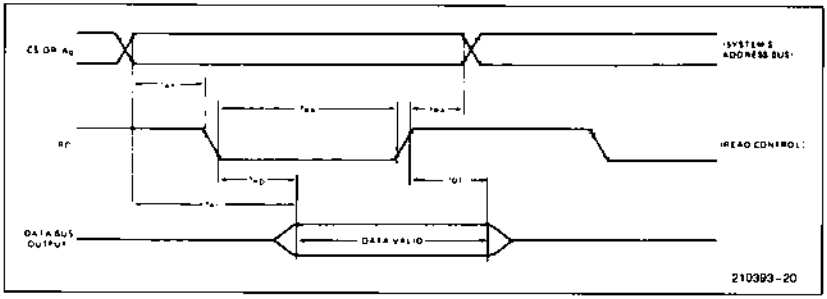

210393-19

C1 5 pF (STRAY 5 pF)
C2 (CRYSTAL + STRAY) 8 pF
C3 20–30 pF INCLUDING STRAY

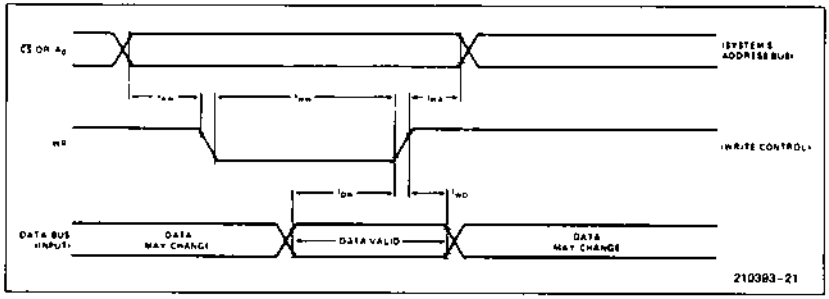
Crystal Series Resistance Should be Less Than 30Ω at 12 MHz; Less Than 75Ω at 6 MHz; Less Than 180Ω at 3.6 MHz.

## WAVEFORMS

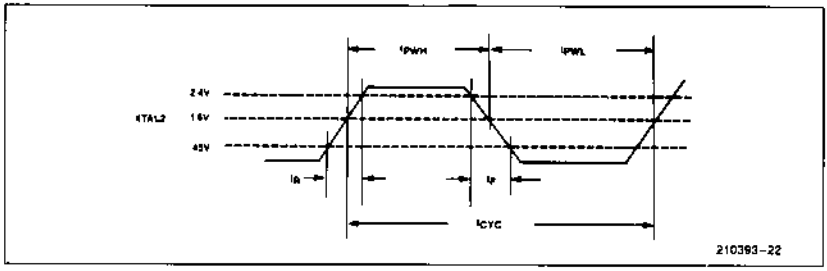
### READ OPERATION—DATA BUS BUFFER REGISTER




### WRITE OPERATION—DATA BUS BUFFER REGISTER

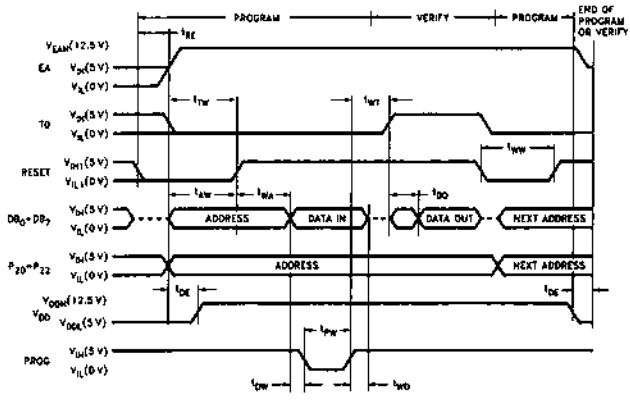



### CLOCK TIMING



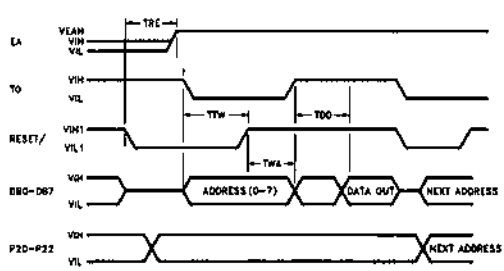
## WAVEFORMS (Continued)

### COMBINATION PROGRAM/VERIFY MODE




**NOTES:**
1. $A_0$ must be held low (0V) during program/verify modes.
2. For $V_{IH}$, $V_{IH1}$, $V_{IL}$, $V_{IL1}$, $V_{DDH}$, and $V_{DDL}$, please consult the D.C. Characteristics Table.
3. When programming the 8741AH/8742AH, a 0.1 μF capacitor is required across $V_{DD}$ and ground to suppress spurious voltage transients which can damage the device.

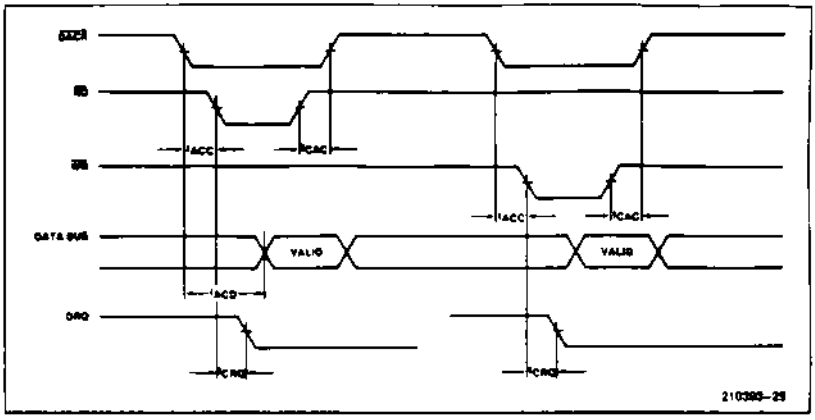
### VERIFY MODE



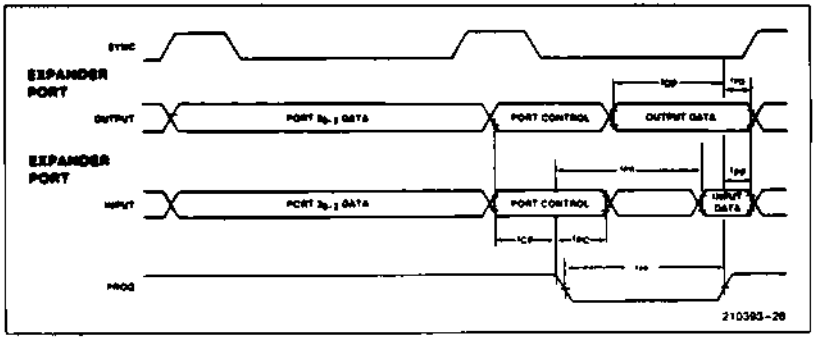

**NOTES:**
1. PROG must float if EA is low.
2. PROG must float or = 5V when EA is high.
3. $P_{10}$–$P_{17}$ = 5V or must float.
4. $P_{24}$–$P_{27}$ = 5V or must float.
5. $A_0$ must be held low during programming/verify modes.

## WAVEFORMS (Continued)

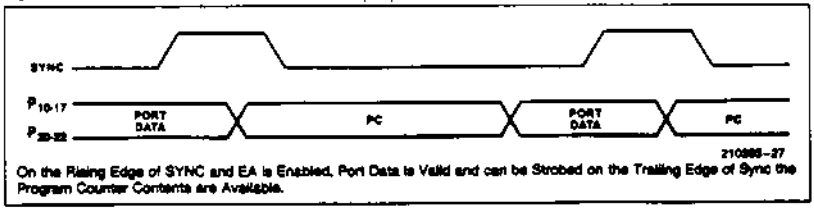
### DMA




### PORT 2




### PORT TIMING DURING EXTERNAL ACCESS (EA)




On the Rising Edge of SYNC and EA is Enabled, Port Data is Valid and can be Strobed on the Trailing Edge of Sync the Program Counter Contents are Available.

**Table 2. UPI™ Instruction Set**

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| **ACCUMULATOR** | | | |
| ADD A, Rr | Add register to A | 1 | 1 |
| ADD A, @Rr | Add data memory to A | 1 | 1 |
| ADD A, #data | Add immediate to A | 2 | 2 |
| ADDC A, Rr | Add register to A with carry | 1 | 1 |
| ADDC A, @Rr | Add data memory to A with carry | 1 | 1 |
| ADDC A, #data | Add immediate to A with carry | 2 | 2 |
| ANL A, Rr | AND register to A | 1 | 1 |
| ANL, A @Rr | AND data memory to A | 1 | 1 |
| ANL A, #data | AND immediate to A | 2 | 2 |
| ORL A, Rr | OR register to A | 1 | 1 |
| ORL, A, @Rr | OR data memory to A | 1 | 1 |
| ORL A, #data | OR immediate to A | 2 | 2 |
| XRL A, Rr | Exclusive OR register to A | 1 | 1 |
| XRL A, @Rr | Exclusive OR data memory to A | 1 | 1 |
| XRL A, #data | Exclusive OR immediate to A | 2 | 2 |
| INC A | Increment A | 1 | 1 |
| DEC A | Decrement A | 1 | 1 |
| CLR A | Clear A | 1 | 1 |
| CPL A | Complement A | 1 | 1 |
| DA A | Decimal Adjust A | 1 | 1 |
| SWAP A | Swap nibbles of A | 1 | 1 |
| RL A | Rotate A left | 1 | 1 |
| RLC A | Rotate A left through carry | 1 | 1 |
| RR A | Rotate A right | 1 | 1 |
| RRC A | Rotate A right through carry | 1 | 1 |
| **INPUT/OUTPUT** | | | |
| IN A, Pp | Input port to A | 1 | 2 |
| OUTL Pp, A | Output A to port | 1 | 2 |
| ANL Pp, #data | AND immediate to port | 2 | 2 |
| ORL Pp, #data | OR immediate to port | 2 | 2 |
| IN A, DBB | Input DBB to A, clear IBF | 1 | 1 |
| OUT DBB, A | Output A to DBB, set OBF | 1 | 1 |
| MOV STS, A | $A_4$–$A_7$ to Bits 4–7 of Status | 1 | 1 |
| MOVD A, Pp | Input Expander port to A | 1 | 2 |
| MOVD Pp, A | Output A to Expander port | 1 | 2 |
| ANLD Pp, A | AND A to Expander port | 1 | 2 |
| ORLD Pp, A | OR A to Expander port | 1 | 2 |

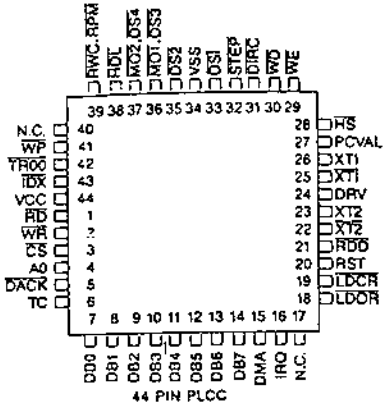
| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| **DATA MOVES** | | | |
| MOV A, Rr | Move register to A | 1 | 1 |
| MOV A, @Rr | Move data memory to A | 1 | 1 |
| MOV A, #data | Move immediate to A | 2 | 2 |
| MOV Rr, A | Move A to register | 1 | 1 |
| MOV @Rr, A | Move A to data memory | 1 | 1 |
| MOV Rr, #data | Move immediate to register | 2 | 2 |
| MOV @Rr, #data | Move immediate to data memory | 2 | 2 |
| MOV A, PSW | Move PSW to A | 1 | 1 |
| MOV PSW, A | Move A to PSW | 1 | 1 |
| XCH A, Rr | Exchange A and register | 1 | 1 |
| XCH A, @Rr | Exchange A and data memory | 1 | 1 |
| XCHD A, @Rr | Exchange digit of A and register | 1 | 1 |
| MOVP A, @A | Move to A from current page | 1 | 2 |
| MOVP3, A, @A | Move to A from page 3 | 1 | 2 |
| **TIMER/COUNTER** | | | |
| MOV A, T | Read Timer/Counter | 1 | 1 |
| MOV T, A | Load Timer/Counter | 1 | 1 |
| STRT T | Start Timer | 1 | 1 |
| STRT CNT | Start Counter | 1 | 1 |
| STOP TCNT | Stop Timer/Counter | 1 | 1 |
| EN TCNTI | Enable Timer/Counter Interrupt | 1 | 1 |
| DIS TCNTI | Disable Timer/Counter Interrupt | 1 | 1 |
| **CONTROL** | | | |
| EN DMA | Enable DMA Handshake Lines | 1 | 1 |
| EN I | Enable IBF Interrupt | 1 | 1 |
| DIS I | Diable IBF Interrupt | 1 | 1 |
| EN FLAGS | Enable Master Interrupts | 1 | 1 |
| SEL RB0 | Select register bank 0 | 1 | 1 |
| SEL RB1 | Select register bank 1 | 1 | 1 |
| NOP | No Operation | 1 | 1 |
| **REGISTERS** | | | |
| INC Rr | Increment register | 1 | 1 |
| INC @Rr | Increment data memory | 1 | 1 |
| DEC Rr | Decrement register | 1 | 1 |

**Table 2. UPI™ Instruction Set** (Continued)

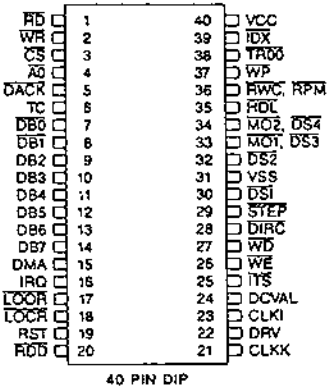
| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| **SUBROUTINE** | | | |
| CALL addr | Jump to subroutine | 2 | 2 |
| RET | Return | 1 | 2 |
| RETR | Return and restore status | 1 | 2 |
| **FLAGS** | | | |
| CLR C | Clear Carry | 1 | 1 |
| CPL C | Complement Carry | 1 | 1 |
| CLR F0 | Clear Flag 0 | 1 | 1 |
| CPL F0 | Complement Flag 0 | 1 | 1 |
| CLR F1 | Clear F1 Flag | 1 | 1 |
| CPL F1 | Complement F1 Flag | 1 | 1 |
| **BRANCH** | | | |
| JMP addr | Jump unconditional | 2 | 2 |
| JMPP @A | Jump indirect | 1 | 2 |
| DJNZ Rr, addr | Decrement register and jump | 2 | 2 |
| JC addr | Jump on Carry = 1 | 2 | 2 |
| JNC addr | Jump on Carry = 0 | 2 | 2 |
| JZ addr | Jump on A Zero | 2 | 2 |
| JNZ addr | Jump on A not Zero | 2 | 2 |
| JT0 addr | Jump on T0 = 1 | 2 | 2 |
| JNT0 addr | Jump on T0 = 0 | 2 | 2 |
| JT1 addr | Jump on T1 = 1 | 2 | 2 |
| JNT1 addr | Jump on T1 = 0 | 2 | 2 |
| JF0 addr | Jump on F0 Flag = 1 | 2 | 2 |
| JF1 addr | Jump on F1 Flag = 1 | 2 | 2 |
| JTF addr | Jump on Timer Flag = 1, Clear Flag | 2 | 2 |
| JNIBF addr | Jump on IBF Flag = 0 | 2 | 2 |
| JOBF addr | Jump on OBF Flag = 1 | 2 | 2 |
| JBb addr | Jump on Accumulator Bit | 2 | 2 |

**WESTERN DIGITAL**
**C O R P O R A T I O N**

# WD37C65 FLOPPY DISK SUBSYSTEM CONTROLLER




44 PIN PLCC




40 PIN DIP

FEATURES

- IBM PC/AT COMPATIBLE FORMAT (SINGLE AND DOUBLE DENSITY)
  - FLOPPY CONTROL AND OPERATIONS ON CHIP
  - IN PC/AT MODE, PROVIDES REQUIRED SIGNAL QUALIFICATION TO DMA CHANNEL
  - BIOS COMPATIBLE
  - DUAL SPEED SPINDLE DRIVE SUPPORT
- ADDRESS MARK DETECTION CIRCUITRY INTERNAL TO FLOPPY DISK CONTROLLER
- MULTISECTOR AND MULTITRACK TRANSFER CAPABILITY
- DIRECT FLOPPY DISK DRIVE INTERFACE WITH NO BUFFERS NEEDED
  - 48mA SINK OUTPUT DRIVERS
  - SCHMITT TRIGGER LINE RECEIVERS
- COMPATIBLE WITH PD8080/85, PD8085, AND PD780 (Z80 (TM)) MICROPROCESSORS
- ON CHIP CLOCK GENERATION
- TWO TTL CLOCK INPUTS FOR 40 PIN DIP
- TWO XTAL OSCILLATOR CIRCUITS FOR 44 PIN PLCC
- AUTOMATIC WRITE PRECOMPENSATION
- INNER TRACK VALUE OF 125 OR 187NS PIN SELECTABLE
- ENHANCED HOST INTERFACE
  - READ/WRITE ACCESSES COMPATIBLE REGISTERS WITH 8 OR 12 MHz 286 MICROPROCESSOR WITH 0 WAIT STATES
  - 20 LSTTL OUTPUT DRIVE CAPABILITY
  - INPUTS ARE TTL LEVEL SCHMITT TRIGGER (EXCEPT DATA BUS)
  - DMA TIMING CORRECTED
- USER PROGRAMMABLE TRACK STEPPING RATE AND HEAD LOAD/UNLOAD TIME
- DRIVES UP TO FOUR FLOPPY OR MICRO FLOPPYDISK (TM) DRIVES
- DATA TRANSFER IN DMA OR NON-DMA MODE
- PARALLEL SEEK OPERATIONS
  - ON UP TO FOUR DRIVES
- HIGH PERFORMANCE, CLASSICAL 2ND ORDER, TYPE 2, PHASE LOCKED LOOP DIGITAL DATA SEPARATOR
- 125, 250, 300, 500 KBITS/SEC DATA RATES
- CMOS LOW POWER 125mW
- +5VDC POWER SUPPLY

November, 1986

## DESCRIPTION

The WD37C65 Floppy Disk Subsystem Controller is an LSI device that provides all the needed functionality between the Host processor peripheral bus and the cable connector to the floppy disk drive. This 'superchip' intergrates: Formatter/Controller, Data Separation, Write Precompensation, Data Rate Selection, Clock Generation, Drive Interface Drivers and Receivers.

On the disk drive interface, the WD37C65 includes Data Separation that has been designed to address high performance error rates on floppy disk drives, and contains all the necessary logic to achieve classical 2nd order, type 2, phase locked loop performance. Write Precompensation is included, in addition to the usual Formating, Encoding/Decoding, Stepper Motor Control, and Status Sensing Functions. All inputs are TTL compatible Schmitt Trigger line receivers, and outputs are high current, open drain, with the drivers meeting the 48 mA ANSI Specification.

The Host interface has been improved for speed operation supporting 8 or 12 MHz, 286 microprocessor bus without the use of wait states, the inputs are Schmitt Triggers (except the data bus). Output drive capability is 20 LSTTL loads, allowing direct interconnection to bus structures without the use of buffers or transceivers. For PC and PC/AT applications, qualification of interrupt request and DMA request is provided.

Traditionally, Data Rate Selection, Drive Selection, and Stepper Motor Control have been output ports of the Host processor architecture. In the PC/AT these functions are latched into registers addressed within the I/O mapping of the system. The Control Register provides support logic that latches the two LSBs used to select the desired data rate that controls internal clock generation. The Operations Register replaces the standard latched port used in floppy subsystems. These registers are incorporated into the WD37C65.

All Clock Generation: SCLK – Sampling Clock, WCLK – Write Clock, and MCLK – Master Clock, are included in the WD37C65. XTAL oscillator circuits provide the necessary signals for internal timing when using the 44 pin PLCC. If the 40 pin DIP is used, the TTL level clock inputs must be provided. There are two oscillators in the WD37C65; one at 16 MHz that handles all standard data rates (500, 250, and 125 Kb/Sec). The other oscillator is at 9.6 MHz to support the 300 Kb/Sec data rate used in PC/AT designs. Some AT compatibles use two-speed disk drives. If two-speed disk drives are used, the drive type input pin is grounded and only the 16 MHz clock is required. A $\overline{RPM}$ output signal will become active when a spindle speed rate of 300 RPM is desired.

## PIN DESCRIPTIONS

| D/P PIN NUMBER | MNEMONIC | SIGNAL NAME | I/O | FUNCTION |
|---|---|---|---|---|
| 1/1 | $\overline{RD}$ | $\overline{READ}$ | I | Control signal for transfer of data or status onto the data bus by the WD37C65. |
| 2/2 | $\overline{WR}$ | $\overline{WRITE}$ | I | Control signal for latching data from the bus into the WD37C65 Buffer Register. |
| 3/3 | $\overline{CS}$ | $\overline{CHIP\ SELECT}$ | I | Selected when 0 (low) allowing $\overline{RD}$ or $\overline{WR}$ operation from the Host. |
| 4/4 | A0 | ADDRESS LINE | I | Address line selecting data (=1) or status (=0) information. (A0 = logic 0 during $\overline{WR}$ is illegal). |
| 5/5 | $\overline{DACK}$ | $\overline{DMA}$ ACKNOWLEDGE | I | Used by the DMA controller to transfer data from the WD37C65 onto the bus. Logical equivalent to $\overline{CS}$ and A0=1. In Special or PC/AT Mode, this signal is qualified by DMAEN from the Operations Register. |
| 6/6 | TC | TERMINAL COUNT | I | This signal indicates to WD37C65 that data transfer is complete. If DMA operational mode is selected for command execution, TC will be qualified by $\overline{DACK}$, but not in the programmed I/O execution. In PC/AT or Special Mode, qualification by $\overline{DACK}$ requires the Operations Register signal DMAEN to be logically true. Note also that in PC/AT Mode, TC will be qualified by $\overline{DACK}$, whether in DMA or non-DMA Host operation. Programmed I/O in PC/AT Mode will cause an abnormal termination error at the completion of a command. |
| 7-14<br>7-14 | DB0 thru<br>DB7 | DATA BUS 0 thru<br>DATA BUS 7 | I/O | 8-Bit, bi-directional, tri-state, data bus. D0 is the least significant bit (LSB). D7 is the most significant bit (MSB). |

PIN DESCRIPTIONS (cont.)

| D/P PIN NUMBER | MNEMONIC | SIGNAL NAME | I/O | FUNCTION |
|---|---|---|---|---|
| 15/15 | DMA | DIRECT MEMORY ACCESS | O | DMA request for byte transfers of data. In Special or PC/AT mode, this pin is tri-stated, enabled by the DMAEN signal from the Operation Register. This pin is driven in the Base Mode. |
| 16/16 | IRQ | INTERRUPT | O | Interrupt request indicating the completion of command execution or data transfer requests (in non-DMA mode). Normally driven in base mode. In Special or PC/AT Mode, this pin is tri-stated, enabled by the DMAEN signal from the Operations Register. |
| 17 | | | | Not connected in the 44 pin PLCC. |
| 17/18 | $\overline{LDOR}$ | $\overline{LOAD}$ $\overline{OPERATIONS}$ $\overline{REGISTER}$ | I | Address decode which enables the loading of the Operations Register. Internally gated with $\overline{WR}$ creates the strobe which latches the data bus into the Operations Register. |
| 18/19 | $\overline{LDCR}$ | $\overline{LOAD\ CONTROL}$ $\overline{REGISTER}$ | I | Address decode which enables loading of the Control Register. Internally gated with $\overline{WR}$ creates the strobe which latches the two LSBs from the data bus into the Control Register. |
| 19/20 | RST | RESET | I | Resets controller, placing microsequencer in idle. Resets device outputs. Puts device in Base Mode, not PC/AT or Special Mode. |
| 20/21 | $\overline{RDD}$ | $\overline{READ\ DISK}$ $\overline{DATA}$ | I | This is the raw serial bit stream from the disk drive. Each falling edge of the pulses represents a flux transition of the encoded data. |
| 21/ | CLK2 | CLOCK2 | I | TTL level clock input used for non-standard data rates; is 9.6MHz for 300 Kb/s, and can only be selected from the Control Register. |
| /22 | $\overline{XT2}$ | $\overline{XTAL2}$ | O | XTAL oscillator drive output. |
| /23 | XT2 | XTAL2 | I | XTAL oscillator input used for non-standard data rates. It may be driven with a TTL level signal. |
| 22/24 | DRV | DRIVE TYPE | I | Drive type input indicates to the device that a two-speed spindle motor is used if logic is 0. In that case, the second clock input will never be selected and must be grounded. |
| 23/ | CLK1 | CLOCK1 | I | TTL level clock input is used to generate all internal timings for standard data rates. Frequency must be 16MHz ± 0.1%, and may have 40/60 or 60/40 duty cycle. |
| /25 | $\overline{XT1}$ | $\overline{XTAL1}$ | O | XTAL oscillator drive output. |
| /26 | XT1 | XTAL1 | I | XTAL oscillator input requiring 16MHz crystal. This oscillator is used for all standard data rates, and may be driven with a TTL level signal. |
| 24/27 | PCVAL | PRECOMPEN-SATION VALUE | I | PRECOMPENSATION VALUE select input. This pin determines the amount of write precompensation used on the inner tracks of the diskette. Logic 1 – 125ns, Logic 0 – 187ns. |
| 25/28 | $\overline{HS}$ | $\overline{HEAD\ SELECT}$ | O | High current driver (HCD) output selects the head (side) of the floppy disk that is being read or written. Logic 1 – side 0. Logic 0 – side 1. |
| 26/29 | $\overline{WE}$ | $\overline{WRITE\ ENABLE}$ | O | This HCD output becomes true, active low, just prior to writing on the diskette. This allows current to flow through the write head. |

PIN DESCRIPTIONS (cont.)

| D/P PIN NUMBER | MNEMONIC | SIGNAL NAME | I/O | FUNCTION |
|---|---|---|---|---|
| 27/30 | $\overline{WD}$ | $\overline{WRITE\ DATA}$ | O | This HCD output is $\overline{WRITE\ DATA}$. Each falling edge of the encoded data pulse stream causes a flux transition on the media. |
| 28/31 | $\overline{DIRC}$ | $\overline{DIRECTION}$ | O | This HCD output determines the direction of the head stepper motor. Logic 1 – outward motion. Logic 0 – inward motion. |
| 29/32 | $\overline{STEP}$ | $\overline{STEP\ PULSE}$ | O | This HCD output issues an active low pulse for each track to track movement of the head. |
| 30/33 | $\overline{DS1}$ | $\overline{DRIVE\ SELECT\ 1}$ | O | This HCD output, when active low is $\overline{DRIVE\ SELECT\ 1}$, in PC/AT Mode, enabling the interface in this disk drive. This signal comes from the Operations Register. In Base, or Special Mode, this output is #1 of the four decoded Unit Selects, as specified in the device command syntax. |
| 31/34 | VSS | GROUND | | Ground. |
| 32/35 | $\overline{DS2}$ | $\overline{DRIVE\ SELECT\ 2}$ | O | This HCD output when active low is $\overline{DRIVE\ SELECT\ 2}$, in PC/AT Mode, enabling the interface in this disk drive. This signal comes from the Operations Register. In Base or the Special Mode, this output is #2 of the four decoded Unit Selects as specified in the device command syntax. |
| 33/36 | $\overline{MO1}$, $\overline{DS3}$ | $\overline{MOTOR\ ON\ 1}$, $\overline{DRIVE\ SELECT\ 3}$ | O | This HCD output when active low is MOTOR ON enable for disk drive #1, in PC/AT Mode. This signal comes from the Operations Register. In the Base or Special Mode, this output is #3 of the four decoded Unit Selects as specified in the device command syntax. |
| 34/37 | $\overline{MO2}$, $\overline{DS4}$ | $\overline{MOTOR\ ON\ 2}$, $\overline{DRIVE\ SELECT\ 4}$ | O | This HCD output when active low is MOTOR ON enable for disk drive #2, in PC/AT mode. This signal comes from the Operations Register. In the Base or Special Mode, this output is #4 of the four decoded Unit Selects as specified in the device command syntax. |
| 35/38 | $\overline{HDL}$ | $\overline{HEAD\ LOADED}$ | O | This HCD output when active low causes the head to be loaded against the media in the selected drive. |
| 36/39 | $\overline{RWC}$, $\overline{RPM}$ | $\overline{REDUCED\ WRITE\ CURRENT}$, $\overline{REVOLUTIONS\ PER\ MINUTE}$ | O | This HCD output when active low causes a $\overline{REDUCED\ WRITE\ CURRENT}$ when bit density is increased toward the inner tracks, becoming active when tracks > 28 are accessed. This condition is valid for Base or Special Mode, and is indicative of when write precompensation is necessary. In the PC/AT mode, this signal can be used on two-speed disk drives to select 300 RPM spindle rate, active low, when 250 MFM or 125 FM KB/s is selected. |
| 40 | | | | Not connected in the 44 pin PLCC. |
| 37/41 | $\overline{WP}$ | $\overline{WRITE\ PROTECTED}$ | I | This Schmitt Trigger (ST) input senses status from the disk drive indicating active low, when a diskette is $\overline{WRITE\ PROTECTED}$. |
| 38/42 | $\overline{TR00}$ | $\overline{TRACK\ 00}$ | | This ST input senses status from disk drive indicating active low, when the head is positioned over the outermost track, $\overline{TRACK\ 00}$. |
| 39/43 | $\overline{IDX}$ | $\overline{INDEX}$ | I | This ST input senses status from the disk drive indicating active low, when the head is positioned over the beginning of a track marked by an index hole. |
| 40/44 | VCC | +5VDC | | Input power supply. |

## ARCHITECTURE

The WD37C65 Floppy Disk Subsystem Controller is an LSI device that provides all the needed functionality between the Host processor peripheral bus and the cable connector to the floppy disk drive. This "superchip" integrates: Formatter/Controller, Data Separation, Write Precompensation, Data Rate Selection, Clock Generation, Drive Interface Drivers and Receivers.

Figure 1 illustrates a block diagram of the WD37C65 Floppy Disk Subsystem Controller.

Figure 2 illustrates a typical WD37C65 system.

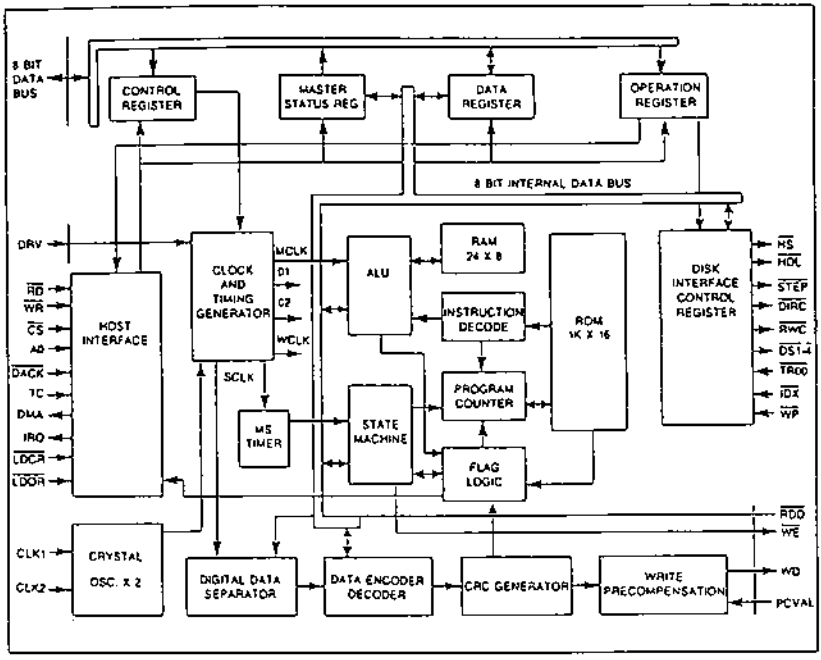



FIGURE 1. WD37C65 BLOCK DIAGRAM

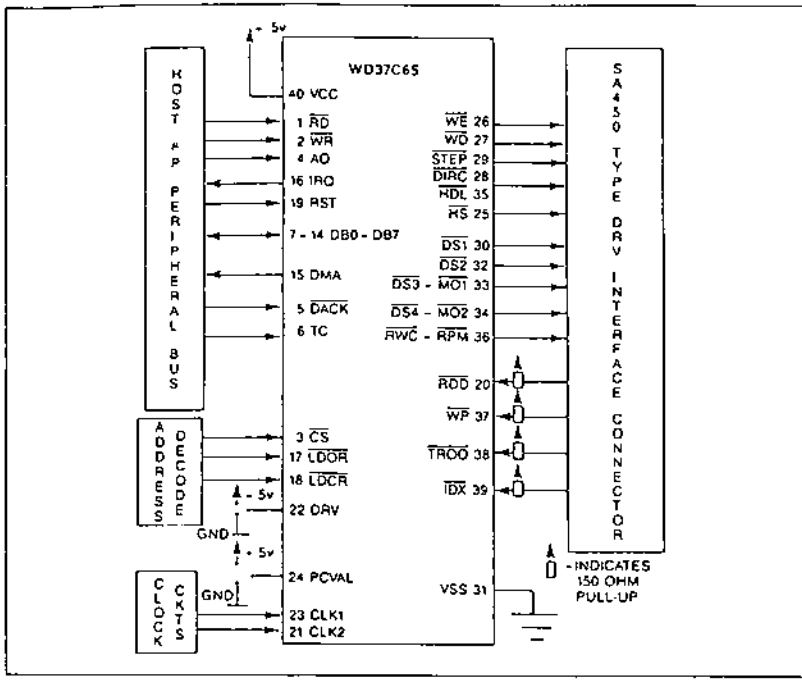



FIGURE 2. TYPICAL WD37C65 SYSTEM

## HOST INTERFACE

The Host Interface is the Host Microprocessor Peripheral Bus. This bus is composed of eight control signals and eight data signals. In the Special or PC/AT Modes, IRQ and DMA request are tri-stated and qualified by DMA enable, internally provided by the Operations Register. The data bus, DMA, and IRQ outputs are designed to handle 20 LSTTL loading. Inputs, except the data bus, are Schmitt Trigger receivers and can be hooked up to a bus or backplane without any additional buffering.

During the Command or Result phases the Main Status Register must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data is read from or written into the Data Register, the CPU should wait for 12µs before reading the Main Status Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the WD37C65. Many of the commands require multiple bytes, as result the Main Status Register must be read prior to each byte transfer to the WD37C65. During the Result phase, Bits D6 and D7 in the Main Status Register must both be 1's (D6–1 and D7–1) before reading each byte from the Data Register. Note that this reading of the Main Status Register before each byte transfer to the WD37C65 is required only in the Command and Result phases, and not during the Execution phase.

During the Execution phase, the Main Status Register need not be read. If the WD37C65 is in the non-DMA Mode, then the receipt of each data byte (WD37C65 is reading data from the FDD) is indicated by an interrupt signal on pin 16 (IRQ–1). The generation of a Read signal ($\overline{RD}$–0) or Write signal ($\overline{WR}$–0) will clear the interrupt as well as output the data onto the data bus. If the processor cannot handle interrupts fast enough (every 13µs for the MFM Mode and 27µs for the FM Mode), then it may poll the Main Status Register and bit D7 (ROM) functions as the Interrupt signal. If a Write Command is in process then the $\overline{WR}$ signal performs the reset to the Interrupt signal.

All timings mentioned above double for mini floppy data rates.

Note that in the non-DMA Mode it is necessary to examine the Main Status Register to determine the cause of the interrupt, since it could be a data interrupt or a command termination interrupt, either normal or abnormal. If the WD37C65 is in the DMA Mode, no Interrupt signals are generated during the Execution phase. The WD37C65 generates DMA's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both $\overline{DACK}$ = 0 (DMA Acknowledge) and an $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0), then the DMA Request is cleared (DMA = 0). If a Write Command has been issued then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution phase has been completed (Terminal Count has occurred) or the EOT sector read/written, then an Interrupt will occur (IRQ = 1). This signifies the beginning of the Result phase. When the first byte of data is read during the Result phase, the Interrupt is automatically cleared (IRQ = 0).

It should be noted that in PC/AT usage, non-DMA Host transfers are not the normal procedure. If the user chooses to do so, the WD37C65 will successfully complete commands, but will always give abnormal termination error status since TC is qualified by an inactive $\overline{DACK}$.

The $\overline{RD}$ or $\overline{WR}$ signals should be asserted while $\overline{DACK}$ is true. The $\overline{CS}$ signal is used in conjunction with $\overline{RD}$ and $\overline{WR}$ as a gating function during programmed $\overline{I/O}$ operations. $\overline{CS}$ has no effect during DMA operations. If the non-DMA Mode is chosen, the $\overline{DACK}$ signal should be pulled up to Vcc. It is important to note that during the Result phase all bytes shown in the Command Table must be read. The Read Data Command for example, has several bytes of data in the Result phase. All seven bytes must be read in order to successfully complete the Read Data Command. The WD37C65 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result phase. The WD37C65 contains five Status Registers. The Main Status Register mentioned may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are available only during the Result phase and may be read only after completing a command. The particular command that has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the WD37C65 to form the Command phase, and are read out of the WD37C65 in the Result phase, must occur in the order shown in the Command Table. The Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result phases is allowed. After the last byte of data in the Command phase is sent to the WD37C65, the Execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result phase, the command is automatically ended and the WD37C65 is ready for a new command.

## CONTROL REGISTER

The Control Register provides support logic that latches the two LSBs of the data bus upon receiving $\overline{LDCR}$ and $\overline{WR}$. These bits are used to select the desired data rate which in turn controls the internal clock generation. Clock switchover is internally "deglitched", allowing continuous operation after changing data rates. If the Control Register is not used, the data rate is governed by the supplied clock or crystal. The frequency must be 64X the desired MFM data rate, up to a maximum frequency of 16 MHz. This implies a maximum data rate of 250 Kb/s unless the Control Register is used. Switching this clock must be "glitchless" or the device will need to be reset. Table 1 presents the Control Register.

TABLE 1. CONTROL REGISTER

| CR1 | CR0 | DRV | DATA RATE | COMMENTS | RPM (IN PC/AT MODE) |
|---|---|---|---|---|---|
| 0 | 0 | X | 500 K | MFM | 1 |
| 0 | 0 | X | 250 K | FM | 1 |
| 0 | 1 | 0 | 250 K | MFM | 0 |
| 0 | 1 | 1 | 300 K | MFM | 0 |
| 1 | 0 | X | 250 K | MFM, RST Default | 1 |
| 1 | 0 | X | 125 K | FM, RST Default | 1 |
| 1 | 1 | X | 125 K | FM | 0 |

## MASTER STATUS REGISTER

The Master Status Register is an 8-bit register that contains the status information of the FDC, and may be accessed at any time. Only the Master Status Register may be read and used to facilitate the transfer of data between the processor and WD37C65. The DIO and RQM bits in the Master Status Register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last $\overline{RD}$ or $\overline{WR}$ during a command or result phase and DIO and RQM getting set is 12μs if 500 Kb/s MFM data rate is selected. (If 250 Kb/s MFM is selected, the delay is 24μs.) For this reason everytime the Master Status Register is read the CPU should wait 12μs. The maximum time from the trailing edge of the last $\overline{RD}$ in the result phase to when DB4 (FDC busy) goes low is 12μs.

The bits in the Master Status Register are listed in Table 2.

TABLE 2. MASTER STATUS REGISTER BITS

| BIT NO. | BIT NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| DB0 | FDD 0 BUSY | D0B | FDD number is 0 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE Commands. |
| DB1 | FDD 1 BUSY | D1B | FDD number 1 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE Commands. |
| DB2 | FDD 2 BUSY | D2B | FDD number 2 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE Commands. |
| DB3 | FDD 3 BUSY | D3B | FDD number 3 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE Commands. |
| DB4 | FDC BUSY | CB | A READ or WRITE Command is in progress. FDC will not accept any other command. |
| DB5 | EXECUTION MODE | EXM | This bit is set only during Execution Phase in non-DMA Mode. When DB5 goes low Execution Phase has ended and Results Phase has started. It operates only during non-DMA Mode of operation. |
| DB6 | DATA INPUT | DIO | Indicates direction of data transfer between FDC and Data Register. If DIO=1, then transfer is from Data Register to the processor. If DIO=0, then transfer is from the processor to Data Register. |
| DB7 | REQUEST FOR MASTER | ROM | Indicates Data Register is ready to send or receive data to or from the processor. Both bits DIO and ROM should be used to perform the handshaking functions of "ready" and "direction" to the processor. |

The bits in Status Register 0 are listed in Table 3.

TABLE 3. STATUS REGISTER 0 BITS

| BIT NO. | BIT NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| D7<br>D6 | INTERRUPT CODE | IC | D7=0 and D6=0. Normal Termination of command was completed and properly executed.<br>D7=0 and D6=1. Abnormal Termination of command, (AT). Execution of command was started but was not successfully completed.<br>D7=1 and D6=0.<br>Invalid Command issue, (IC). Command which was issued was never started.<br>D7=1 and D6=1.<br>Abnormal Termination because during command execution the ready signal from FDD changed state. |
| D5 | SEEK END | SE | When the FDC completes the SEEK Command this flag is set to 1 (high). |
| D4 | EQUIPMENT CHECK | EC | If a fault signal is received from the FDD, or if the Track 0 signal fails to occur after 255 step pulses (Recalibrate Command) then this flag is set. |
| D3 | NOT READY | NR | Since drive Ready is always presumed true, this will always be a logic 0. |
| D2 | HEAD SELECT | HS | This flag is used to indicate the state of the head at interrupt. |
| D1 | UNIT SELECT 1 | US1 | This flag is used to indicate a Drive Unit Number at interrupt. |
| D0 | UNIT SELECT 0 | US0 | This flag is used to indicate a Drive Unit Number at interrupt. |

The bits in Status Register 1 are listed in Table 4.

TABLE 4. STATUS REGISTER 1 BITS

| BIT NO. | BIT NAME | BIT SYMBOL | DESCRIPTION |
|---|---|---|---|
| D7 | END OF CYLINDER | EN | When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set. |
| D6 | | | Not used. This bit is always 0 (low). |
| D5 | DATA ERROR | DE | When the FDC detects a * CRC error in either the ID field or the data field, this flag is set. |
| D4 | OVERRUN | OR | If the FDC is not serviced by the Host system during data transfers within a certain time interval, this flag is set. |
| D3 | | | Not used. This bit is always 0 (low). |
| D2 | NO DATA | ND | During execution of READ DATA, WRITE DELETED DATA, or SCAN Command, if the FDC cannot find the sector specified in the * * IDR Register, this flag is set. During execution of the READ ID Command if the FDC cannot read the ID field without an error, then this flag is set.<br>During execution of the READ A TRACK Command, if the starting sector cannot be found, then this flag is set. |
| D1 | NOT WRITABLE | NW | During execution of WRITE DATA, WRITE DELETED DATA or FORMAT A TRACK Command, if the FDC detects a $\overline{WP}$ signal from the FDD, then this flag is set. |
| D0 | MISSING ADDRESS MARK | MA | If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.<br>If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. At the same time the MD (Missing Address Mark in data field) of Status Register 2 is set. |

The bits in Status Register 2 are listed in Table 5.

TABLE 5. STATUS REGISTER 2 BITS

| BIT NO. | BIT NAME | BIT SYMBOL | DESCRIPTION |
|---|---|---|---|
| D7 | | | Not Used. This bit is always 0 (low). |
| D6 | CONTROL MARK | CM | During execution of the READ DATA or SCAN Command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set. |
| D5 | DATA ERROR | DD | If the FDC detects a CRC error in the data field then this flag is set. |
| D4 | WRONG CYLINDER | WC | This bit is related to the ND bit, and the contents of * * *C on the medium is different from that stored in the IDR, this flag is set. |
| D3 | SCAN EQUAL | SH | During execution of the SCAN Command if the condition of "equal" is satisfied, this flag is set. |
| D2 | SCAN NOT | SN | During execution of the SCAN Command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set. |
| D1 | BAD CYLINDER | BC | This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FF, then this flag is set. |
| D0 | MISSING ADDRESS MARK IN DATA FIELD | MD | When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set. |

The bits in Status Register 3 are listed in Table 6.

TABLE 6. STATUS REGISTER 3 BITS

| BIT NO. | BIT NAME | BIT SYMBOL | DESCRIPTION |
|---|---|---|---|
| D7 | | – | Not used. Will always be logic 0. |
| D6 | WRITE PROTECTED | $\overline{WP}$ | This bit is used to indicate the status of the WRITE PROTECTED signal from the FDD. |
| D5 | READY | RY | This bit will always be a logic 1. Drive is presumed to be ready. |
| D4 | TRACK 0 | T0 | This bit is used to indicate the status of the Track 0 signal from the FDD. |
| D3 | WRITE PROTECTED | $\overline{WP}$ | This bit is used to indicate the status of the WRITE PROTECTED signal from the FDD. |
| D2 | HEAD SELECT | HS | This bit is used to indicate the status of the Side Select signal to the FDD. |
| D1 | UNIT SELECT 1 | US1 | This bit is used to indicate the status of the Unit Select 1 signal to the FDD. |
| D0 | UNIT SELECT 2 | US0 | This bit is used to indicate the status of the Unit Select 0 signal to the FDD. |

* CRC - Cyclic Redundancy Check
** IDR - Internal Data Register
*** C - Cylinder

## DATA REGISTER

The 8-bit Data Register stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command.

The relationship between the Master Status Register and the Data Register and the signals $\overline{RD}$, $\overline{WR}$, and A0 are shown in Table 7.

TABLE 7. MASTER STATUS AND DATA REGISTERS RELATIONSHIP

| A0 | $\overline{RD}$ | $\overline{WR}$ | FUNCTION |
|---|---|---|---|
| 0 | 0 | 1 | Read Main Status Register |
| 0 | 1 | 0 | Illegal |
| 0 | 0 | 0 | Illegal |
| 1 | 0 | 0 | Illegal |
| 1 | 0 | 1 | Read from Data Register |
| 1 | 1 | 0 | Write into Data Register |

## OPERATIONS REGISTER

The Operations Register provides support logic that latches the data bus upon receiving $\overline{LDOR}$ and $\overline{WR}$. The Operations Register replaces the typical latched port found in floppy subsystems used to control disk drive spindle motors and to select the desired disk drive. Table 8 represents the Operations Register.

TABLE 8. OPERATIONS REGISTER

| | | |
|---|---|---|
| OR0 | DSEL | ; Drive Select, if low and MOEN1 = 1, then $\overline{DS1}$ is active. If high and MOEN2 = 1, then $\overline{DS2}$ is active, but only in the PC/AT Mode. |
| OR1 | ( X ) | ; Has no defined function. A spare. |
| OR2 | $\overline{SRST}$ | ; Soft reset, active low. |
| OR3 | DMAEN | ; DMA enable, active in Special and PC/AT Mode. Qualifies DMA and IRQ outputs and $\overline{DACK}$ input. |
| OR4 | MOEN1 | ; Motor On enable, inverted output $\overline{MO1}$ is active only in PC/AT Mode. |
| OR5 | MOEN2 | ; Motor On enable, inverted output $\overline{MO2}$ is active only in PC/AT Mode. |
| OR6 | ( X ) | ; Has no defined function. A spare. |
| OR7 | ( X ) | ; Mode Select. During a soft reset condition, may be used to select between Special Mode and PC/AT Mode. |

## BASE, SPECIAL, AND PC/AT MODES

Base, Special, and PC/AT Modes allow subtle differences which the user may find desirable. The Control Register may be used in any mode without altering functionality.

### Base Mode

After a hardware reset, RST active, the WD37C65 will be held in soft reset, $\overline{SRST}$ active, with the normally driven signals, DMA request and IRQ request outputs tri-stated. Base Mode may be initiated at this time by a chip access by the Host. Although this may be any read or write, it is strongly recommended that the Base Mode user's first chip access be a read of the Master Status Register. Once Base Mode is entered the soft reset is released, and IRQ and DMA are driven. Base Mode prohibits the use of the Operations Register, hence there can be no qualifying by DMAEN and no soft resets. The Drive Select outputs, $\overline{DS1}$ to $\overline{DS4}$, offer a 1 of 4 decoding of the Unit Select bits resident in the command structure. Pin $\overline{RWC}$ represents Reduce Write Current and is indicative of when write precompensation is necessary.

### Special Mode

Special Mode allows use of the Operations Register for the DMAEN signal as a qualifier and to do a software driven device reset $\overline{SRST}$. To enter Special Mode, the Operations Register is loaded with (1 X 0 0 X 0 X X), setting Mode Select to a logic 1 disabling MOEN1 and MOEN2 and causing $\overline{SRST}$ to be active. Then a read of the Control Register address, $\overline{LDCR}$ and $\overline{RD}$, will set the device into Special Mode. The $\overline{DS1}$ through $\overline{DS4}$ is again offered in this mode, as is $\overline{RWC}$.

### PC/AT Mode

For PC/AT compatibility, users will write to the Operations Register, $\overline{LDOR}$ and $\overline{WR}$; this action performed after a hardware reset, or in the Base Mode, initiates PC/AT Mode. PC/AT Mode can also be entered from Special Mode by loading the Operations Register with (0 X 0 0 X 0 X X), setting Mode Select to a logic 0, disabling MOEN1 and MOEN2, and causing $\overline{SRST}$ to be active. Then a read of the Control Register address sets the device into PC/AT Mode. The $\overline{DS}$ outputs are now replaced with the DSEL and MOEN signals buffered from the Operations Register. DMAEN and $\overline{SRST}$ are supported and compatible with the current BIOS. $\overline{RWC}$ pin function is now $\overline{RPM}$ so that users with two-speed drives may reduce spindle speed from a nominal 360 revolutions per minute, to 300 revolutions per minute when active low, or used to reduce write current when a slower data rate is selected for a given drive.

## POLLING ROUTINE

After any reset the WD37C65, a hard RST or soft $\overline{SRST}$, US0 and US1, will automatically go into a Polling Routine. In between commands (and between step pulses in the SEEK Command) the WD37C65 polls all four FDDs looking for a change in the Ready line from any of the drives. Since the drive is always presumed Ready, an interrupt will only be generated following a reset. This occurs because a reset forces Not Ready status, which then promptly becomes Ready. Note that in Special or PC/AT Modes, if DMAEN is not valid prior to 1ms after reset goes inactive, then IRQ may be already set and pending when finally enabled onto the bus. The polling of the Ready line by the WD37C65 occurs continuously between commands. Each drive is polled every 1.024ms except during the READ/WRITE Commands. For mini-floppies, the polling rate is 2.048ms. The drive polling sequence is 1-2-4-3.

Figure 2 illustrates the Drive Select Polling Timing.

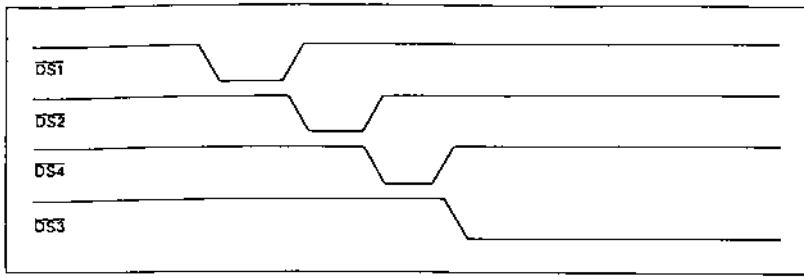



FIGURE 2. DRIVE SELECT POLLING TIMING

## DEVICE RESETS

The WD37C65 supports both hardware reset (RST) pin (19), and a software reset ($\overline{SRST}$), through use of the Operations Register. The RST pin will cause a device reset for the active duration. RST causes a default to Base Mode, and default selects 250K MFM (or 125K FM, code dependent) as the data rate (16 MHz input clock). $\overline{SRST}$ will reset the microcontroller as did the RST, but will not affect the current data rate selection or the mode. Both RST and $\overline{SRST}$, when active, will disable the high current driver outputs to the disk drive.

If the XTAL oscillators are used, instead of the TTL driven clock inputs, the hardware RST active time requirement will be extended. The oscillator circuit is designed so that RST will bootstrap the circuit into guaranteed oscillation in a fixed amount of time. The extended reset time allows the growth of the oscillation to produce stable internal clock timing.

## DATA SEPARATOR

The Data Separator is a WD92C32 Digital Phase Lock Loop Floppy Disk Data Separator (DPLL). It was designed to address high performance error rates on floppy disk drives, and to provide a superior performance in terms of available bit jitter tolerance. It contains the necessary logic to achieve classical 2nd order, type 2, phase locked loop performance. Figure 1 illustrates the WD92C32 used as the Data Separator in the WD37C65 system. Figure 3 illustrates the WD92C32 simplified block diagram.

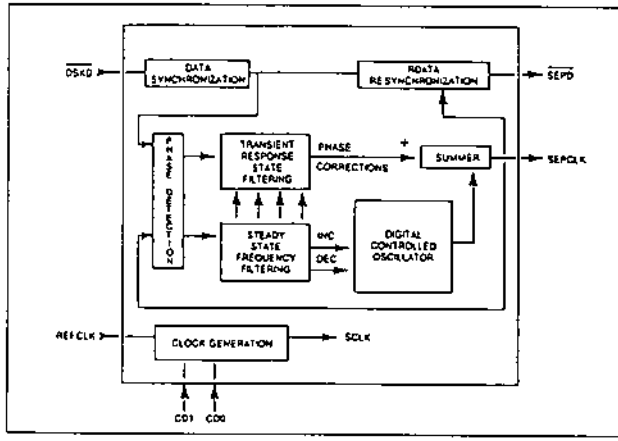



FIGURE 3. WD92C32 SIMPLIFIED BLOCK DIAGRAM

## WRITE PRECOMPENSATION

The WD37C65 maintains the standard first level algorithm to determine when Write Precompensation should be applied. The EARLY and LATE signals are used internally to select the appropriate delay in the write data pulse stream. The encoded WRITE DATA signal is synchronized to the 16 MHz clock, if this is the frequency on CLK1 pin (23), and clocked through a shift register. Signals EARLY, NOM, and LATE determine the amount of delay through the shift register before a multiplexer gates the chosen bit to the output. The output data pulse width has a 25% duty cycle, i.e., ¼ of the bit cell period, and equal to ½ the WCLK period.

When PCVAL pin (24) = 1 all data will be precompensated by ± 125ns regardless of track number and data rate, however, this is only for MFM encoding. There is no Write Precompensation for FM. If PCVAL = 0, and if a track inside number 28 is accessed, then ± 187ns precompensation will be generated. For frequencies other than 16 MHz on the CLK1 pin, the precompensation values will be two and three clock cycles respectively.

When the non-standard data rate using CLK2 is chosen, the MFM precompensation will always be 2 clock cycles. For 9.6 MHz this is ± 208ns. In this case, the PCVAL function is disabled.

## CLOCK GENERATION

This logical block provides all the clocks needed by the WD37C65. They are: Sampling Clock (SCLK), Write Clock (WCLK), and the Master Clock (MCLK).

SCLK drives the WD92C32 Data Separator used during data recovery. This clock's frequency is always 32X the selected data rate.

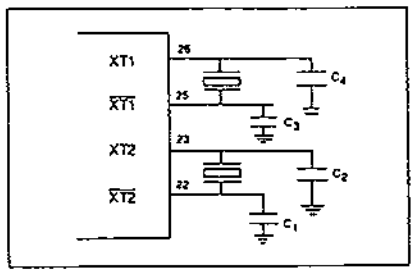
WCLK is used by the encoder logic to place MFM or FM on the serial WD-stream to the disk. WCLK always has a frequency 2X the selected data rate.

MCLK is used by the microsequencer. MCLK and $\overline{MCLK}$ clock all latches in a two-phase scheme. One microinstruction cycle is four MCLK cycles. MCLK has a frequency equal to 8X the selected MFM data rate or 16X the FM data rate. Table 9 presents the Clock Data Rate.

TABLE 9. CLOCK DATA RATE

| DATA RATE | CODE | SCLK | MCLK | WCLK |
|---|---|---|---|---|
| 500 Kb/S | MFM | 16.0 MHz | 4.0 MHz | 1.0 MHz |
| 250 Kb/S | FM | 8.0 MHz | 4.0 MHz | 500 KHz |
| 250 Kb/S | MFM | 8.0 MHz | 2.0 MHz | 500 KHz |
| 125 Kb/S | FM | 4.0 MHz | 2.0 MHz | 250 KHz |
| 300 Kb/S | MFM | 9.6 MHz | 2.4 MHz | 600 KHz |

Figure 4 illustrates the XTAL oscillator circuits for the 44 pin PLCC configuration.




SERIES RESONANT XT 2

9.6 MHz ± 100 ppm
R series = 30 ohm max
C shunt = 10 pf max
C1 = 68 pf 5% mica
C2 = 56 pf 5% mica

SERIES RESONANT XT 1

16.0 MHz ± 100 ppm
R series = 30 ohm max
C shunt = 10 pf max
C3 = 47 pf 5% mica
C4 = 15 pf 5% mica

FIGURE 4. XTAL OSCILLATOR CIRCUITS FOR THE 44 PIN PLCC

## COMMANDS

The WD37C65 is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor. The results after execution of the command may also be a multibyte transfer back to the processor. The commands consist of three phases: Command Phase, Execution Phase, and the Result Phase.

Command Phase – The Floppy Disk Controller (FDC) receives all information required to perform a particular operation from the processor.

Execution Phase – The FDC performs the operation it was instructed to do.

Result Phase – After completion of the operation, status and other housekeeping information are made available to the processor.

Table 10 lists the 15 WD37C65 commands.

TABLE 10. WD37C65 COMMANDS

| |
|---|
| READ DATA |
| READ DELETED DATA |
| WRITE DATA |
| WRITE DELETED DATA |
| READ A TRACK |
| READ ID |
| FORMAT A TRACK |
| SCAN EQUAL |
| SCAN LOW OR EQUAL |
| SCAN HIGH OR EQUAL |
| RECALIBRATE |
| SENSE INTERRUPT STATUS |
| SPECIFY |
| SENSE DRIVE STATUS |
| SEEK |

Tables 11 through 25 are presented to show the required parameters and results for each command. Most commands require nine command bytes and return seven bytes during the result phase. The "W" to the left of each byte indicates a command phase byte to be written. An "R" indicates a result byte.

TABLE 11. READ DATA

| PHASE | R/W | D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| COMMAND | W | MT | MF | SK | 0 | | 0 | 1 | 1 | 0 | Command Codes |
| | W | X | X | X | X | | X | HS | US1 | US0 | |
| | W | ← | | | | C | | | | → | Sector ID information prior to command execution. The four bytes are compared against header on floppy disk. |
| | W | ← | | | | H | | | | → | |
| | W | ← | | | | R | | | | → | |
| | W | ← | | | | N | | | | → | |
| | W | ← | | | | EOT | | | | → | |
| | W | ← | | | | GPL | | | | → | |
| | W | ← | | | | DTL | | | | → | |
| EXECUTION | | | | | | | | | | | Data transfer between FDD and main system. |
| RESULTS | R | ← | | | | ST0 | | | | → | Status information after command execution. |
| | R | ← | | | | ST1 | | | | → | |
| | R | ← | | | | ST2 | | | | → | |
| | R | ← | | | | C | | | | → | Sector ID information after command execution. |
| | R | ← | | | | H | | | | → | |
| | R | ← | | | | R | | | | → | |
| | R | ← | | | | N | | | | → | |

TABLE 12. READ DELETED DATA

| PHASE | R/W | D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| COMMAND | W | MT | MF | SK | 0 | | 1 | 1 | 0 | 0 | Command Codes |
| | W | X | X | X | X | | X | HS | US1 | US0 | |
| | W | ← | | | | C | | | | → | Sector ID information prior to command execution. The four bytes are compared against header on floppy disk. |
| | W | ← | | | | H | | | | → | |
| | W | ← | | | | R | | | | → | |
| | W | ← | | | | N | | | | → | |
| | W | ← | | | | EOT | | | | → | |
| | W | ← | | | | GPL | | | | → | |
| | W | ← | | | | DTL | | | | → | |
| EXECUTION | | | | | | | | | | | Data transfer between FDD and main system. |
| RESULTS | R | ← | | | | ST0 | | | | → | Status information after command execution. |
| | R | ← | | | | ST1 | | | | → | |
| | R | ← | | | | ST2 | | | | → | |
| | R | ← | | | | C | | | | → | Sector ID information after command execution. |
| | R | ← | | | | H | | | | → | |
| | R | ← | | | | R | | | | → | |
| | R | ← | | | | N | | | | → | |

TABLE 13. WRITE DATA

| PHASE | R/W | D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| COMMAND | W | MT | MF | 0 | 0 | | 0 | 1 | 0 | 1 | Command Codes |
| | W | X | X | X | X | | X | HS | US1 | US0 | |
| | W | ← | | | | C | | | | → | Sector ID information prior to command execution. The four bytes are compared against header on floppy disk. |
| | W | ← | | | | H | | | | → | |
| | W | ← | | | | R | | | | → | |
| | W | ← | | | | N | | | | → | |
| | W | ← | | | | EOT | | | | → | |
| | W | ← | | | | GPL | | | | → | |
| | W | ← | | | | DTL | | | | → | |
| EXECUTION | | | | | | | | | | | Data transfer between FDD and main system. |
| RESULTS | R | ← | | | | ST0 | | | | → | Status information after command execution. |
| | R | ← | | | | ST1 | | | | → | |
| | R | ← | | | | ST2 | | | | → | |
| | R | ← | | | | C | | | | → | Sector ID information after command execution. |
| | R | ← | | | | H | | | | → | |
| | R | ← | | | | R | | | | → | |
| | R | ← | | | | N | | | | → | |

TABLE 14. WRITE DELETED DATA

| PHASE | R/W | D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| COMMAND | W | MT | MF | 0 | 0 | | 1 | 0 | 0 | 1 | Command Codes |
| | W | X | X | X | X | | X | HS | US1 | US0 | |
| | W | ← | | | | C | | | | → | Sector ID information prior to command execution. The four bytes are compared against header on floppy disk. |
| | W | ← | | | | H | | | | → | |
| | W | ← | | | | R | | | | → | |
| | W | ← | | | | N | | | | → | |
| | W | ← | | | | EOT | | | | → | |
| | W | ← | | | | GPL | | | | → | |
| | W | ← | | | | DTL | | | | → | |
| EXECUTION | | | | | | | | | | | Data transfer between FDD and main system. |
| RESULTS | R | ← | | | | ST0 | | | | → | Status information after command execution. |
| | R | ← | | | | ST1 | | | | → | |
| | R | ← | | | | ST2 | | | | → | |
| | R | ← | | | | C | | | | → | Sector ID information after command execution. |
| | R | ← | | | | H | | | | → | |
| | R | ← | | | | R | | | | → | |
| | R | ← | | | | N | | | | → | |

TABLE 15. READ A TRACK

| PHASE | R/W | D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| COMMAND | W | 0 | MF | SK | 0 | | 0 | 0 | 1 | 0 | Command Codes |
| | W | X | X | X | X | | X | HS | US1 | US0 | |
| | W | ← | | | | C | | | | → | Sector ID information prior to command execution. |
| | W | ← | | | | H | | | | → | |
| | W | ← | | | | R | | | | → | |
| | W | ← | | | | N | | | | → | |
| | W | ← | | | | EOT | | | | → | |
| | W | ← | | | | GPL | | | | → | |
| | W | ← | | | | DTL | | | | → | |
| EXECUTION | | | | | | | | | | | Data transfer between FDD and main system. FDD reads all data fields from index hole to EOT. |
| RESULTS | R | ← | | | | ST0 | | | | → | Status information after command execution. |
| | R | ← | | | | ST1 | | | | → | |
| | R | ← | | | | ST2 | | | | → | |
| | R | ← | | | | C | | | | → | Sector ID information after command execution. |
| | R | ← | | | | H | | | | → | |
| | R | ← | | | | R | | | | → | |
| | R | ← | | | | N | | | | → | |

TABLE 16. READ ID

| PHASE | R/W | D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| COMMAND | W | 0 | MF | 0 | 0 | | 1 | 0 | 1 | 0 | Command Codes |
| | W | X | X | X | X | | X | HS | US1 | US0 | |
| EXECUTION | | | | | | | | | | | The first correct ID information on the cylinder is stored in Data Register. |
| RESULTS | R | ST0 | | | | | | | | | Status information after command execution. |
| | R | ST1 | | | | | | | | | |
| | R | ST2 | | | | | | | | | |
| | R | C | | | | | | | | | Sector ID information read during Execution Phase from floppy disk. |
| | R | H | | | | | | | | | |
| | R | R | | | | | | | | | |
| | R | N | | | | | | | | | |

TABLE 17. FORMAT A TRACK

| PHASE | R/W | D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| COMMAND | W | 0 | MF | 0 | 0 | | 1 | 1 | 0 | 1 | Command Codes |
| | W | X | X | X | X | | X | HS | US1 | US0 | |
| | W | N | | | | | | | | | Bytes/Sector |
| | W | SC | | | | | | | | | Sectors/Track |
| | W | GPL | | | | | | | | | Gap 3 |
| | W | D | | | | | | | | | Filler Byte |
| EXECUTION | | | | | | | | | | | Floppy Disk Controller (FDC) formats an entire track. |
| RESULTS | R | ST0 | | | | | | | | | Status information after command execution. |
| | R | ST1 | | | | | | | | | |
| | R | ST2 | | | | | | | | | |
| | R | C | | | | | | | | | In this case, the ID information has no meaning. |
| | R | H | | | | | | | | | |
| | R | R | | | | | | | | | |
| | R | N | | | | | | | | | |

TABLE 18. SCAN EQUAL

| PHASE | R/W | D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| COMMAND | W | MT | MF | SK | 1 | | 0 | 0 | 0 | 1 | Command Codes |
| | W | X | X | X | X | | X | HS | US1 | US0 | |
| | W | C | | | | | | | | | Sector ID information prior to command execution. |
| | W | H | | | | | | | | | |
| | W | R | | | | | | | | | |
| | W | N | | | | | | | | | |
| | W | EOT | | | | | | | | | |
| | W | GPL | | | | | | | | | |
| | W | STP | | | | | | | | | |
| EXECUTION | | | | | | | | | | | Data compared between the FDD and main system. |
| RESULTS | R | ST0 | | | | | | | | | Status information after command execution. |
| | R | ST1 | | | | | | | | | |
| | R | ST2 | | | | | | | | | |
| | R | C | | | | | | | | | Sector ID information after command execution. |
| | R | H | | | | | | | | | |
| | R | R | | | | | | | | | |
| | R | N | | | | | | | | | |

TABLE 19. SCAN LOW OR EQUAL

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| COMMAND | W | MT | MF | SK | 1 | 1 | 0 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HS | US1 | US0 | |
| | W | ← C → | | | | | | | | Sector ID information prior to command execution. |
| | W | ← H → | | | | | | | | |
| | W | ← R → | | | | | | | | |
| | W | ← N → | | | | | | | | |
| | W | ← EOT → | | | | | | | | |
| | W | ← GPL → | | | | | | | | |
| | W | ← STP → | | | | | | | | |
| EXECUTION | | | | | | | | | | Data compared between the FDD and main system. |
| RESULTS | R | ← ST0 → | | | | | | | | Status information after command execution. |
| | R | ← ST1 → | | | | | | | | |
| | R | ← ST2 → | | | | | | | | |
| | R | ← C → | | | | | | | | Sector ID information after command execution. |
| | R | ← H → | | | | | | | | |
| | R | ← R → | | | | | | | | |
| | R | ← N → | | | | | | | | |

TABLE 20. SCAN HIGH OR EQUAL

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| COMMAND | W | MT | MF | SK | 1 | 1 | 1 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HS | US1 | US0 | |
| | W | ← C → | | | | | | | | Sector ID information prior to command execution. |
| | W | ← H → | | | | | | | | |
| | W | ← R → | | | | | | | | |
| | W | ← N → | | | | | | | | |
| | W | ← EOT → | | | | | | | | |
| | W | ← GPL → | | | | | | | | |
| | W | ← STP → | | | | | | | | |
| EXECUTION | | | | | | | | | | Data compared between the FDD and main system. |
| RESULTS | R | ← ST0 → | | | | | | | | Status information after command execution. |
| | R | ← ST1 → | | | | | | | | |
| | R | ← ST2 → | | | | | | | | |
| | R | ← C → | | | | | | | | Sector ID information after command execution. |
| | R | ← H → | | | | | | | | |
| | R | ← R → | | | | | | | | |
| | R | ← N → | | | | | | | | |

**TABLE 21. RECALIBRATE**

| PHASE | R/W | D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| COMMAND | W | 0 | 0 | 0 | 0 | | 0 | 1 | 1 | 1 | Command Codes |
| | W | X | X | X | X | | X | 0 | US1 | US0 | |
| EXECUTION | | | | | | | | | | | Head retracted to Track zero. |

**TABLE 22. SENSE INTERRUPT STATUS**

| PHASE | R/W | D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| COMMAND | W | 0 | 0 | 0 | 0 | | 1 | 0 | 0 | 0 | Command Codes |
| RESULTS | R | ← ST0 → | | | | | | | | | Status information about the FDC at the end of seek operation. |
| | R | ← PCN → | | | | | | | | | |

**TABLE 23. SPECIFY**

| PHASE | R/W | D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| COMMAND | W | 0 | 0 | 0 | 0 | | 0 | 0 | 1 | 1 | Command Codes |
| | W | ← SRT → | | | | | ← HUT → | | | | |
| | W | ← HLT → | | | | | | | | ND | |

**TABLE 24. SENSE DRIVE STATUS**

| PHASE | R/W | D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| COMMAND | W | 0 | 0 | 0 | 0 | | 0 | 1 | 0 | 0 | Command Codes |
| | W | X | X | X | X | | X | HS | US1 | US0 | |
| RESULTS | R | ← ST3 → | | | | | | | | | Status Information about the FDC. |

**TABLE 25. SEEK**

| PHASE | R/W | D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| COMMAND | W | 0 | 0 | 0 | 0 | | 1 | 1 | 1 | 1 | Command Codes |
| | W | X | X | X | X | | X | HS | US1 | US0 | |
| | W | ← NCN → | | | | | | | | | |
| EXECUTION | | | | | | | | | | | Head is positioned over proper cylinder on the diskette. |

Table 26 defines, in alphabetical order, the symbols used in Command Tables 11 through 25.

**TABLE 26. COMMAND SYMBOL DESCRIPTIONS**

| SYMBOL | NAME | DESCRIPTION |
|---|---|---|
| A0 | ADDRESS LINE 0 | A0 controls selection of Main Status Register (A0=0) or Data Register (A0=1). |
| C | CYLINDER NUMBER | C stands for the current/selected cylinder (track) numbers 0 through 255 of the medium. |
| D | DATA | D stands for the data pattern which is going to be written into a sector. |
| D7 - D0 | DATA BUS | 8-bit DATA BUS, where D7 stands for a most significant bit, and D0 stands for a least significant bit. |
| DTL | DATA LENGTH | When N is defined as 00, DTL stands for the DATA LENGTH which users are going to read out or write into the sector. |

TABLE 26. COMMAND SYMBOL DESCRIPTIONS (cont.)

| SYMBOL | NAME | DESCRIPTION |
|---|---|---|
| EOT | END OF TRACK | EOT stands for the final sector number on a cylinder. During Read or Write operations, FDC will stop data transfer after a sector number equal to EOT. |
| GPL | GAP LENGTH | CPL stands for the length of Gap 3. During the FORMAT Command it determines the size of Gap 3. |
| H | HEAD ADDRESS | H stands for head number 0 or 1, as specified in the ID field. |
| HLT | HEAD LOAD TIME | HLT stands for the HEAD LOAD TIME in FDD (2 to 254ms in 2ms increments). |
| HS | HEAD SELECT | HS stands for a selected head number 0 or 1 and controls the polarity of pin 25 (in 40 pin DIP) or pin 28 (in 44 pin PLCC). |
| HUT | HEAD UNLOAD TIME | HUT stands for the HEAD UNLOAD TIME after a Read or Write operation has occurred (16 to 240ms in 16ms increments). |
| MF | FM or MFM | If MF is low, FM mode is selected, and if it is high, MFM mode is selected. |
| MT | MULTITRACK | If MT is high, a MULTITRACK operation is performed. If MT=1 after finishing Read/Write operation on side 0, FDC will automatically start searching for sector 1 on side 1. |
| N | NUMBER | N stands for the NUMBER of data bytes written in a sector. |
| NCN | NEW CYLINDER NUMBER | NCN stands for a NEW CYLINDER NUMBER which is going to be reached as a result of the Seek operation. Desired position of head. |
| ND | NON-DMA MODE | ND stands for operation in the NON-DMA MODE. |
| PCN | PRESENT CYLINDER | PCN stands for the cylinder number at the completion of the SENSE INTERRUPT STATUS Command. Position of head at present time. |
| R | RECORD | R stands for the sector number which will be read or written. |
| R/W | READ/WRITE | R/W stands for either READ or WRITE signal. |
| SC | SECTOR | SC indicates the number of Sectors per cylinder. |
| SK | SKIP | SK stands for SKIP Deleted Data Address mark. |
| SRT | STEP RATE TIME | SRT stands for the Stepping Rate for the FDD (1 to 16ms in 1ms increments). Stepping Rate applies to all drives. In 2's complement format, F(Hex)=1ms, E(Hex)=2ms, etc. |
| ST0<br>ST1<br>ST2<br>ST3 | STATUS 0<br>STATUS 1<br>STATUS 2<br>STATUS 3 | ST0 – 3 stands for one of four registers which store the STATUS information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by A0–0). ST0 – 3 may be read only after a command has been executed and contains information relevant to that particular command. |
| STP | | During a SCAN operation, if STP=1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); if STP=2, then alternate sectors are read and compared. |
| US0,US1 | UNIT SELECT | US stands for a selected drive; binary encoded, 1 of 4. |

## ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS

Operating Temperature ..... 0°C (32°F) to 70°C (158°F)
Storage Temperature ..... −55°C (−67°F) to +125°C (257°F)
Voltage on any pin with respect to ground ..... −0.3V to VCC +0.3V
Supply Voltage with respect to ground ..... 7V

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

DC Operating Characteristics
TA = 0°C (32°F) to 70°C (158°F); VCC = +5V ± 10%

| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|---|---|---|---|---|
| VCC | +5VDC Power Supply | 4.5 | 5.5 | V |
| VIL | Input Low Voltage – Data Bus & XTOSC | | 0.8 | V |
| VIH | Input High Volt – Data Bus & XTOSC | 2.0 | | V |
| VILT | Input Low Threshold – Schmitt Trigger | 0.9 | 1.1 | V |
| VIHT | Input High Threshold – Schmitt Trigger | 1.7 | 1.9 | V |
| VOL | Output Low – DBx,IRQ,DMA.; Io = 12.0mA | | 0.4 | V |
| VOH | Output High – DBx,IRQ,DMA.; Io = −5.0mA | 2.8 | | V |
| VOLHC | Output Low – High Current; Io = 48.0mA | | 0.4 | V |
| ILUL | Latch Up Current Low | 40.0 | | mA |
| ILUH | Latch Up Current High | −40.0 | | mA |
| ILL | Leakage Current Low | | 10.0 | uA |
| ILH | Leakage Current High | | −10.0 | uA |
| ICC | Supply Current – 100uA Source Loads | | 35.0 | mA |
| ICCHL | Supply Current – 5.0mA Source Loads | | 85.0 | mA |
| PD | Power Dissipation – ICC Max * | | 375.0 | mW |
| PDHL | Power Dissipation – ICCHL Max * | | 525.0 | mW |

* Includes open drain high current drivers at Vol = 0.4V.

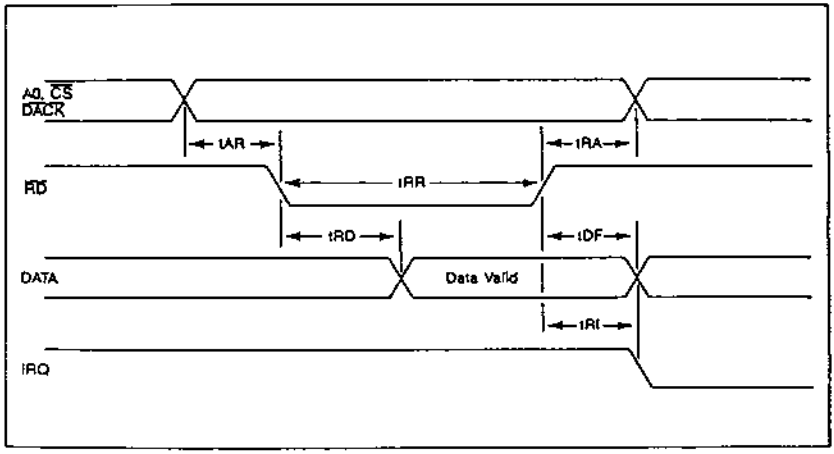



FIGURE 5. READ TIMING

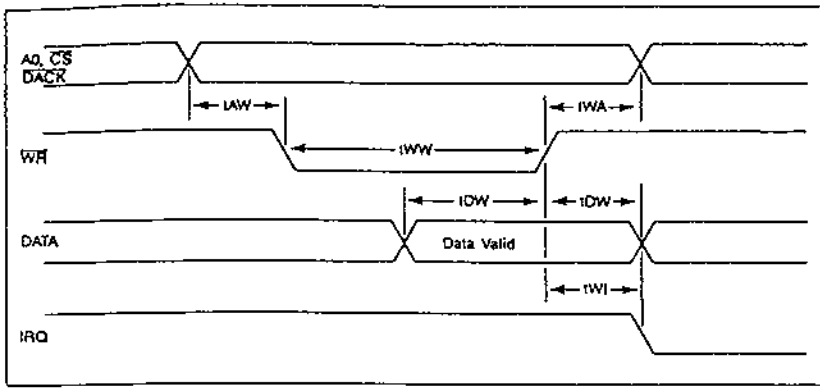



FIGURE 6. WRITE TIMING

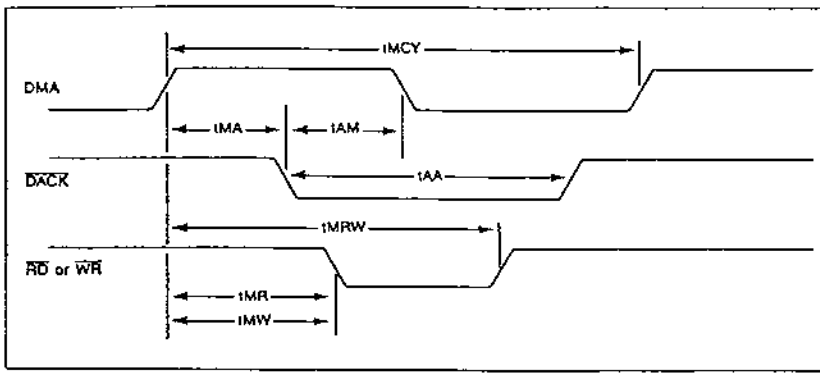



FIGURE 7. DMA TIMING

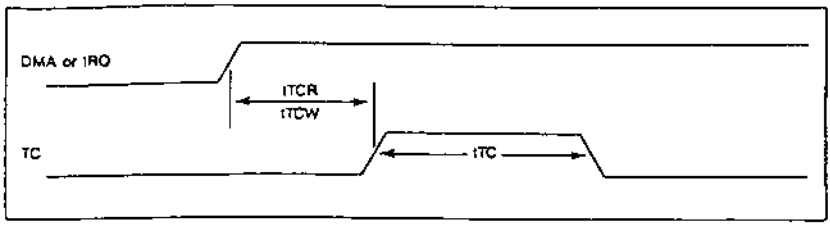



FIGURE 8. TERMINAL COUNT TIMING

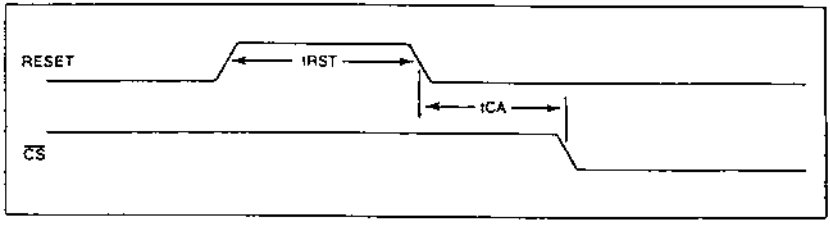



FIGURE 9. RESET TIMING

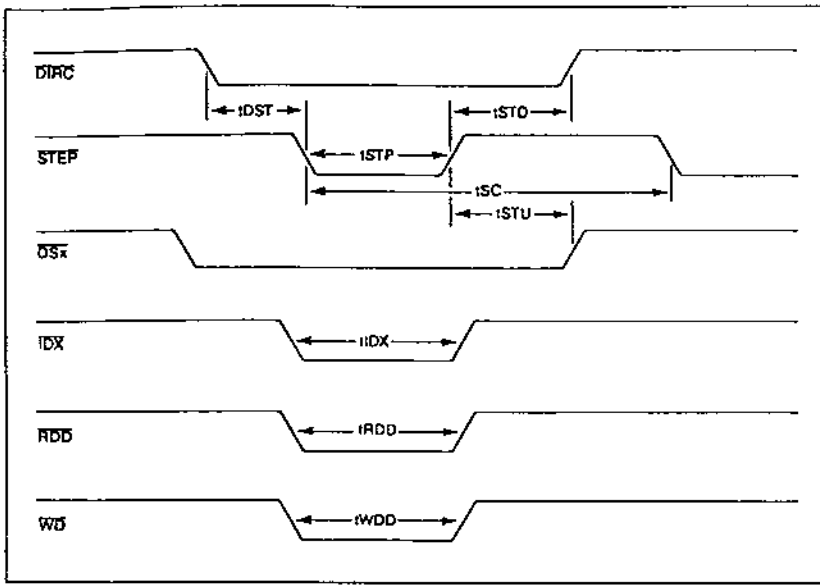



FIGURE 10. DISK DRIVE TIMING

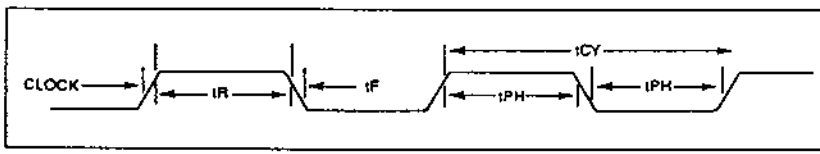



FIGURE 11. CLOCK TIMING

AC Operating Characteristics
TA = 0°C (32°F) to 70°C (158°F); VCC = +5V ± 10%
CL = 100pf

| SYMBOL | PARAMETER | MIN | MAX | UNITS |
|---|---|---|---|---|
| tCY | Clock Period | 60 | | nS |
| tPH | Clock Active (High or Low) | 25 | | nS |
| tR | Clock Rise Time (Vin 0.8 to 2.0) | | 5 | nS |
| tF | Clock Fall Time (Vin 2.0 to 0.8) | | 5 | nS |
| tAR | A0,$\overline{CS}$,$\overline{DACK}$ Set Up Time to $\overline{RD}$ Low | 0 | | nS |
| tRA | A0,$\overline{CS}$,$\overline{DACK}$ Hold Time to RD High | 0 | | nS |
| tRR | $\overline{RD}$ Width | 90 | | nS |
| tRD | Data Access Time From $\overline{RD}$ Low | | 90 | nS |
| tDF | DB To Float Delay From $\overline{RD}$ High | 10 | 65 | nS |
| tAW | A0,$\overline{CS}$,$\overline{DACK}$,$\overline{LDCR}$,$\overline{LDOR}$, Set Up Time To $\overline{WR}$ Low | 0 | | nS |
| tWA | A0,$\overline{CS}$,$\overline{DACK}$,$\overline{LDCR}$,$\overline{LDOR}$, Hold Time From $\overline{WR}$ High | 0 | | nS |
| tWW | $\overline{WR}$ Width | 60 | | nS |
| tDW | Data Set Up Time To $\overline{WR}$ High | 80 | | nS |
| tWD | Data Hold Time From $\overline{WR}$ High | 0 | | nS |
| tRI | IRQ Reset Delay Time From $\overline{RD}$ High | | 1MCY | +150nS |
| tWI | IRQ Reset Delay Time From $\overline{WR}$ High | | 1MCY | +150nS |
| tMCY | DMA Cycle Time | 52 | | MCY |
| tAM | DMA Reset Delay Time From $\overline{DACK}$ Low | | 140 | nS |
| tMA | $\overline{DACK}$ Delay Time From DMA High | 0 | | nS |
| tAA | $\overline{DACK}$ Width | 2 | | MCY |
| tTC | TC Width | 60 | | nS |
| tRST | Reset Width – TTL Driven CLK1 | 224 | | CY |
| tSRST | Reset Width – Software Reset | 5 | | MCY |
| tRDD | $\overline{RDD}$ Active Time Low | 40 | | nS |
| tWDD | $\overline{WD}$ Write Data Width Low | 1/2 (TYP) | | WCY |
| tDST | $\overline{DIRC}$ Hold & Set Up To $\overline{STEP}$ Low | 4 | | MCY |
| tSTU | $\overline{DSX}$ Hold Time From $\overline{STEP}$ Low | 20 | | MCY |
| tSTP | $\overline{STEP}$ Active Time Low | 24 | | MCY |
| tSC | $\overline{STEP}$ Cycle Time | 132 | | MCY |
| tSTD | $\overline{DIRC}$ Hold Time After $\overline{STEP}$ | 96 | | MCY |
| tIDX | $\overline{IDX}$ Index Pulse Width | 2 | | MCY |
| tMR | $\overline{RD}$ Delay From DMA | 0 | | nS |
| tMW | $\overline{WR}$ Delay From DMA | 0 | | nS |
| tMRW | $\overline{RD}$ Or $\overline{WR}$ Response From DMA High | | 48 | MCY |
| tCA | Chip Access Delay From RST Low – TTL | 32 | | MCY |
| tCAS | Chip Access Delay From tSRST Low | 40 | | MCY |
| tXCA | Chip Access Delay from RST – OSC XT1 At 16 MHz | 500 | | uS |
| tXTS | XT2 Access Delay After RST 9.6 MHz | 1000 | | uS |
| tTCR | TC Delay From Last DMA Or IRQ, $\overline{RD}$ | 0 | 192 | MCY |
| tTCW | TC Delay From Last DMA Or IRQ, $\overline{WR}$ | 0 | 384 | MCY |

CY Specifies CLK1 or XT1 period
MCY Specifies MCLK period, dependent on selected data rate
WCY Specifies WCLK period, dependent on selected data rate

VLSI TECHNOLOGY, INC.

# VL16C451

## PARALLEL/ASYNCHRONOUS COMMUNICATIONS ELEMENT

### FEATURES

- IBM PC/AT-compatible
- VL16C450 with on-board Centronix printer interface
- Completely pin- and upward-compatible with the dual serial channel VL16C452
- Independent control of transmit, receive, line status and data set interrupts
- Individual modem control signals
- Programmable serial interface characteristics:
  - 5-,6-,7- or 8-bit characters
  - Even-, odd- or no-parity bit generation and detection
  - 1, 1 1/2 or 2 stop bit generation
- Three-state TTL drive for the data and control bus

### DESCRIPTION

The VL16C451 is an enhanced version of the popular VL16C450 asynchronous communications element (ACE). The serial channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of the Parallel/Asynchronous Communications Element (P/ACE) can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions. It is fully pin- and upward-compatible with the dual serial channel VL16C452. The second serial channel of the VL16C452 occupies pins that are VCC, GND, or N.C. (not connected) on the VL16C451.

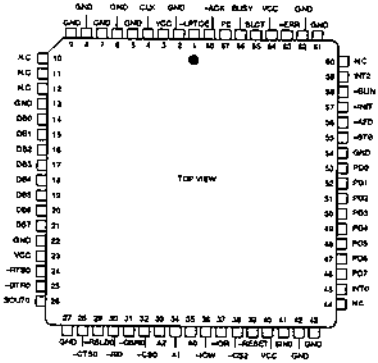
The VL16C451 also provides the user with a fully bidirectional parallel data port that fully supports the parallel Centronics type printer. This port allows information received from either serial communication port to be printed from the P/ACE. The parallel port, together with the serial port, provide IBM PC/AT-compatible computers with a single device to serve the two system ports.

A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and ($2^{16}$-1).

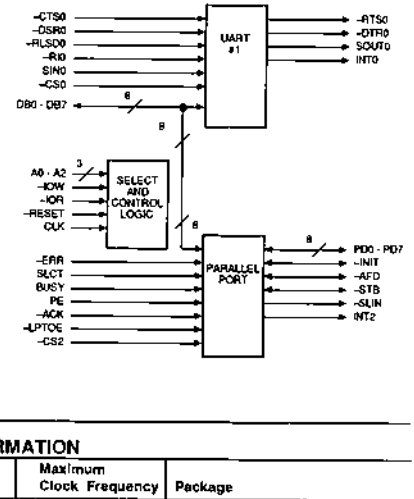
The VL16C451 is housed in a 68-pin plastic leaded chip carrier.

### PIN DIAGRAM

VL16C451




### BLOCK DIAGRAM




### ORDER INFORMATION

| Part Number | Maximum Clock Frequency | Package |
|---|---|---|
| VL16C451-QC | 3.1 MHz | Plastic Leaded Chip Carrier (PLCC) |

Note: Operating temperature range is 0°C to +70°C.



VLSI Technology, Inc. • 8375 South River Parkway • Tempe, AZ 85284 • 602-752-8574

## SIGNAL DESCRIPTIONS

| Signal Name | Pin Number | Signal Description |
|---|---|---|
| –IOR | 37 | Input/Output Read Strobe - This is an active low input which causes the serial channel to output data to the data bus (DB0-DB7). The data output depends upon the register selected by the address inputs A0, A1, A2. Chip Select 0 (–CS0) selects the UART and Chip Select 2 (–CS2) selects the line printer port. |
| –IOW | 36 | Input/Output Write Strobe - This is an active low input which causes data from the data bus (DB0-DB7) to be input to the UART or to the parallel port. The data input depends upon the register selected by the address inputs A0, A1, A2. The chip select inputs (–CS0 and –CS2) enable the UART and the parallel port (respectively). |
| DB0-DB7 | 14-21 | Data Bits DB0-DB7 - The Data Bus provides eight, three-state I/O lines for the transfer of data, control and status information between the VL16C451 and the CPU. These lines are normally in a high-impedance state except during read operations. D0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted. |
| A0, A1, A2 | 35, 34, 33 | Address Lines A0-A2 - The address lines select the internal registers during CPU bus operations. See Table 1 for the decode of the serial channels, Table 11 for the decode of the parallel line printer port. |
| CLK | 4 | Clock Input - The external clock input to the UART baud rate divisor. |
| SOUT0. | 26 | Serial Data Output - This line is the serial data output from the UART's transmitter circuitry. A mark (1) is a logic "one" (high) and space (0) is a logic "zero" (low). SOUT0 is held in the mark condition when the transmitter is disabled, Reset is true, the Transmitter Register is empty, or when in the Loop Mode. |
| –CTS0 | 28 | Clear to Send Input - The logical state of the –CTS pin is reflected in the CTS bit of the (MSR) Modem Status Register [CTS is bit 4 of the MSR, written MSR (4)] of the UART. A change of state of the –CTS pin, since the previous reading of the MSR causes the setting of DCTS [MSR(0)] of the Modem Status Register. When the –CTS pin is low, the modem is indicating that data on SOUT0 can be transmitted. |
| DSR0 | 31 | Data Set Ready Input - The logical state of the DSR0 pin is reflected in MSR(5) of the Modem Status Register. DDSR [MSR(1)] indicates whether the DSR0 pin has changed state since the previous reading of the MSR. When the DSR0 pin is low, the modem is indicating that it is ready to exchange data with the UART. |
| DTR0 | 25 | Data Terminal Ready Output - The DTR0 pin can be set (low) by writing a logic 1 to MCR(0), Modem Control Register bit 0 of the UART. This signal is cleared (high) by writing a logic 0 to the DTR bit [MCR(0)] or whenever a reset occurs. When active (low), the DTR0 pin indicates to the DCE that the UART is ready to receive data. |
| –RTS0 | 24 | Request to Send Output - The –RTS0 signal is an output on the UART used to enable the modem. The –RTS0 pin is set low by writing a logic 1 to MCR(1) bit 1 of the UART's Modem Control Register. The –RTS0 pin is reset high by Reset. A low on the –RTS0 pin indicates to the DCE that the UART has data ready to transmit. In half duplex operations, –RTS0 is used to control the direction of the line. |
| –RI0 | 30 | Ring Indicator Input - When low, –RI0 indicates that a telephone ringing signal has been received by the modem or data set. The –RI0 signal is a modem control input whose condition is tested by reading MSR(6) (RI) of the UART. The Modem Status Register output TERI [MSR(2)] indicates whether the RI input has changed from high to low since the previous reading of the MSR. If the Interrupt is enabled [IER(3)=1] and –RI0 changes from a high to low, an interrupt is generated. |
| –LPTOE | 1 | Parallel Data Output Enable - When low, this signal enables the Write Data Register to the PD0 - PD7 lines. A high puts the PD0 - PD7 lines in the high-impedance state allowing them to be used as inputs. –LPTOE is usually tied low for line printer operation. |
| SIN0 | 41 | Serial Data Input - The serial data input moves information from the communication line or modem to the VL16C451 receiver circuits. A mark (1) is high, and a space (0) is low. Data on serial data inputs is disabled when operating in the loop mode. |

## SIGNAL DESCRIPTIONS (Cont.)

| Signal Name | Pin Number | Signal Description |
|---|---|---|
| –RLSD0, | 29 | Receive Line Signal Detect - When low, the –RLSD output indicates that the data carrier has been detected by the modem or data set. –RLSD is a modem input whose condition can be tested by the CPU by reading MSR(7) (RLSD) of the Modem Status Register. MSR(3) (DRLSD) of the Modem Status Register indicates whether the –RLSD input has changed since the previous reading of the MSR. –RLSD has no effect on the receiver. If the –RLSD changes state with the modem status interrupt enabled, an interrupt occurs. |
| –RESET | 39 | Reset - When low, the reset input forces the VL16C451 into an idle mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its output is cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities. |
| INT0 | 45 | Serial Channel Interrupt Output - This three-state output is enabled by the MCR bit 2. The serial channel interrupt goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the Interrupt Enable Register of the serial channel: Receiver Error flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. The interrupt is reset low upon appropriate service or a reset. |
| –CS0, –CS2 | 32, 38 | Chip Selects - Each Chip Select input acts as an enable for the write and read signals for its channel. –CS0 enables the serial port, while –CS2 enables the the signals to the line printer port. |
| PD0-PD7 | 53-46 | Parallel Data Bits (0-7) - These eight lines provide a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when –LPTOE is held in the high state. |
| –STB | 55 | Line Printer Strobe - This open-drain line provides communication between the VL16C451 and the line printer. When it is active low, it provides the line printer with a signal to latch the data currently on the parallel port. |
| –AFD | 56 | Line Printer Autofeed - This open-drain line provides the line printer with an active low signal when continuous form paper is to be autofed to the printer. |
| –INIT | 57 | Line Printer Initialize - This open-drain line provides the line printer with a signal that allows the line printer initialization routine to be started. |
| –SLIN | 58 | Line Printer Select - This open-drain line selects the printer when it is active low. |
| INT2 | 59 | Printer Port Interrupt - This signal is an active high, three-state output, generated by the positive transition of –ACK. It is enabled by bit 4 of the Write Control Register. |
| –ERROR | 63 | Line Printer Error - This is an input line from the line printer. The line printer reports an error by holding this line low during the error condition. |
| SLCT | 65 | Line Printer Selected - This is an input line from the line printer that goes high when the line printer has been selected. |
| BUSY | 66 | Line Printer Busy - This is an input line from the line printer that goes high when the line printer is not ready to accept data. |
| PE | 67 | Line Printer Paper Empty - This is an input line from the line printer that goes high when the printer runs out of paper. |
| –ACK | 68 | Line Printer Acknowledge - This input goes low to indicate a successful data transfer has taken place. It generates a printer port interrupt during its positive transition. |
| VCC | 3, 23, 40, 64 | Power Supply - The power supply requirement is 5 V ±5%. |
| GND | 2, 5-9, 13, 22, 27, 42, 43, 54, 61, 62 | Ground (0 V) - All pins must be tied to ground for proper operation. |
| N.C. | 10-12, 44, 60 | No Connection. |

## FUNCTIONAL DESCRIPTION:

### SERIAL CHANNEL REGISTERS

Three types of internal registers are used in the serial channel of the VL16C451. They are used in the operation of the device, and are the control, status, and data registers. The control registers are the Bit Rate Select Register DLL (Divisor Latch LSB) and DLM (Divisor Latch MSB), Line Control Register, Interrupt Enable Register, and the Modem Control registers, while the status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and the Transmitter Holding Register. The Address, Read, and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register [LCR(7)] to select the register to be written or read (see Table 1). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. An example, LCR(7) refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers holding from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The VL16C451 data registers are double-buffered so that read and write operations can be performed at the same time the UART is performing the parallel-to-serial and serial-to-parallel conversion.

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. The contents of the LCR are described below:

- LCR (0) Word Length Select Bit 0 (WLS0)
- LCR (1) Word Length Select Bit 1 (WLS1)
- LCR (2) Stop Bit Select (STB)
- LCR (3) Parity Enable (PEN)
- LCR (4) Even Parity Select (EPS)
- LCR (5) Stick Parity
- LCR (6) Set Break
- LCR (7) Divisor Latch Access Bit (DLAB)

LCR (0) and LCR(1) word length select bit 1: The number of bits in each serial character is programmed as shown in the following chart:

| LCR(1) | LCR(0) | Word Length |
|---|---|---|
| 0 | 0 | 5 Bits |
| 0 | 1 | 6 Bits |
| 1 | 0 | 7 Bits |
| 1 | 1 | 8 Bits |

LCR(2) Stop Bit Select: LCR(2) specifies the number of stop bits in each transmitted character. If LCR(2) is a logic 0, one stop bit is generated in the transmitted data. If LCR(2) is a logic 1 when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR(2) is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The receiver checks for two stop bits if programmed.

LCR(3) Parity Enable: When LCR(3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR(4) Even Parity Select: When parity is enabled [LCR(3)=1], LCR(4)=0 selects odd parity, and LCR(4)=1 selects even parity.

LCR(5) Stick Parity: When parity is enabled [LCR(3)=1], CLR(5)=1 causes the transmission and reception of a parity bit to be in the opposite state from that indicated by LCR(4). This allows the user to force parity to a known state and for the receiver to check the parity bit in a known state.

LCR(6) Break Control: When LCR(6) is set to a logic "1", the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting LCR(6) to a logic "0". The Break Control bit acts only on SOUT and has no effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all "0"s pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the transmitter to be idle (TEMT=1), and clear break when normal transmission has to be restored.

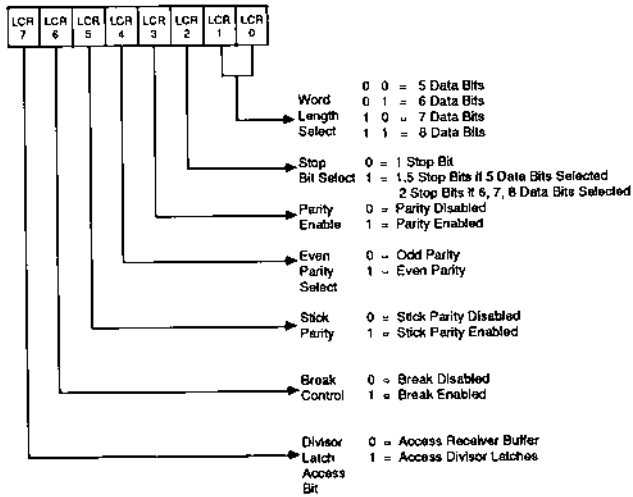
### TABLE 1. SERIAL CHANNEL INTERNAL REGISTERS

| DLAB | A2 | A1 | A0 | Mnemonic | Register |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | RBR | Receiver Buffer Register (read only) |
| 0 | 0 | 0 | 0 | THR | Transmitter Holding Register (write only) |
| 0 | 0 | 0 | 1 | IER | Interrupt Enable Register |
| X | 0 | 1 | 0 | IIR | Interrupt Identification Register (read only) |
| X | 0 | 1 | 1 | LCR | Line Control Register |
| X | 1 | 0 | 0 | MCR | Modem Control Register |
| X | 1 | 0 | 1 | LSR | Line Status Register |
| X | 1 | 1 | 0 | MSR | Modem Status Register |
| X | 1 | 1 | 1 | SCR | Scratch Register |
| 1 | 0 | 0 | 0 | DLL | Divisor Latch (LSB) |
| 1 | 0 | 0 | 1 | DLM | Divisor Latch (MSB) |

X = "Don't Care" 0 = Logic Low 1 = Logic High

**Note:** The serial channel is accessed when -CS0 is low.

FIGURE 1. LINE CONTROL REGISTER




LCR(7) Divisor Latch Access Bit (DLAB): LCR(7) must be set high (logic "1") to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR(7) must be input low to access the Receiver Buffer, the Transmitter Holding, or the Interrupt Enable Registers.

The Line Status Register (LSR) is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status the serial channel of the VL16C451.

Three error flags OE, FE, and PE provide the status of any error conditions detected in the receiver circuitry. During reception of the stop bits, the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last character only if no overrun occurred. The Overrun Error character in the Receiver Buffer Register has been overwritten by a character from the Receiver Shift Register before being read by the CPU. The character is thereby lost. Framing Error (FE) indicates that the last character received contained incorrect (low) stop bits. This is caused by the absense of the required stop bit or by a stop bit too short to be detected. Parity Error (PE) indicates that the last character received had a parity error based on the programmed and calculated parity of the received character.

The Break Interrupt (BI) status bit indicates that the last character received was a break character. A break character is an invalid data character. However, it is an entire character, including parity and stop bits.

The Transmitter Holding Register Empty (THRE) bit indicates that theTHR register is empty and may receive another character. The Transmission Shift Register Empty (TEMT) bit indicates that the Transmitter Shift Register is empty, and the serial channel has completed transmission of the last character to be sent. If the interrupt is enabled [IER(1)], an active THRE causes an Interrupt (INTRPT).

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Reading the LSR clears LSR(1)-LSR(4). (OE, PE, FE, and BI.)

The contents of the Line Status Register shown in Table 2 are described below:

LSR(0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR(0) is reset low by a CPU read of the data in the Reciever Buffer Register.

LSR(1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was

## TABLE 2. LINE STATUS REGISTER BITS

| LSR BITS | Logic 1 | Logic 0 |
|---|---|---|
| LSR (0) Data Ready (DR) | Ready | Not Ready |
| LSR (1) Overrun Error (OE) | Error | No Error |
| LSR (2) Parity Error (PE) | Error | No Error |
| LSR (3) Framing Error (FE) | Error | No Error |
| LSR (4) Break Interrupt (BI) | Break | No Break |
| LSR (5) Transmitter Holding Register Empty (THRE) | Empty | Not Empty |
| LSR (6) Transmitter Empty (TEMT) | Empty | Not Empty |
| LSR (7) Not Used | | |

transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR(2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit (LCR(4)). The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

LSR(3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR(3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR(4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR(1) - LSR(4) are the error conditions that produce a Reciever Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER(2)=1 in the Interrupt Enable Register.

LSR(5) Transmitter Holding Register Empty (THRE): THRE indicates that the VL82C50A is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR(5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR(5) is not reset by a CPU read of the LSR.

When the THRE interrupt is enabled (IER(1)=1). THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR(6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR(6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR(7): This bit is always 0.

The Modem Control Register (MCR) controls the interface with the modem or data set as described in Table 3.

MCR can be written and read. The –RTS and –DTR outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR Bits 0, 1, 3, and 4 are shown below:

MCR(0): When MCR(0) is set high, the -DTR output is forced low. When MCR(0) is reset low, the –DTR output is forced high. The –DTR output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(1): When MCR(1) is set high, the RTS output is forced low. Whe MCR(1) is reset low, the –RTS output is forced high. The –RTS output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

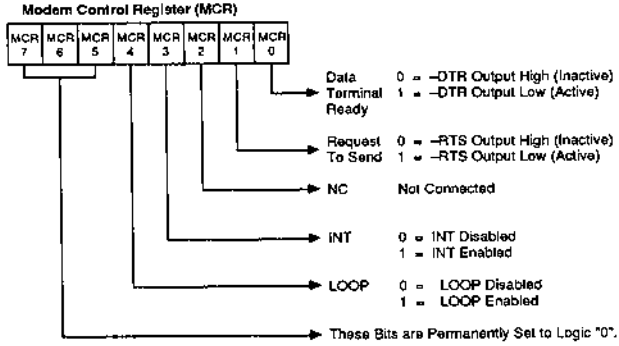
MCR(3): When MCR(3) is set high, the INT output is enabled.

MCR(4): MCR(4) provides a local loopback feature for diagnostic testing of the channel. When MCR(4) is set high, Serial Output (SOUT) is set to the marking (logic "1") state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The three modem control inputs (–CTS, –DSR, and –RI) are disconnected. The modem control outputs (–DTR and –RTS) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high).

## TABLE 3. MODEM CONTROL REGISTER BITS

| MCR BITS | Logic 1 | Logic 0 |
|---|---|---|
| MCR (0) DataTerminal Ready (DTR) | –DTR Output Low | –DTR Output High |
| MCR (1) Request to Send (RTS) | –RTS Output Low | –RTS OutputHigh |
| MCR (2) 0 | | |
| MCR (3) Interrupt (INT) Enable | INT Enabled | INT Disabled |
| MCR (4) LOOP | Loop Enabled | Loop Disabled |
| MCR (5) 0 | | |
| MCR (6) 0 | | |
| MCS (7) 0 | | |

FIGURE 2. MODEM CONTROL REGISTER




In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Bits MCR(5) - MCR(7) are permanently set to logic 0.

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the VL16C451. In addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines for the channel are –CTS, –DSR, –RI, and –RLSD. MSR(4) - MSR(7) are status indications of these lines. The status indications follow the status of the input lines. If the modem status interrupt in the Interrupt Enable Register is enabled [IER(3)], a change of state in a modem input signals will be reflected by the modem status bits in the IIR register, and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 4. Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

MSR(0) Delta Clear to Send (DCTS): DCTS indicates that the –CTS input to the serial channel has changed state since the last time it was read by the CPU.

MSR(1) Delta Data Set Ready (DDSR): DDSR indicates that the –DSR input to the serial channel has changed state since the last time it was read by the CPU.

MSR(2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the –RI input to the serial channel has changed state from high to low since the last time it was read by the CPU. Low to high transitions on –RI0 do not activate TERI.

MSR(3) Delta Data Carrier Detect (DRSLD): DRSLD indicates that the –RSLD input to the serial channel has changed state since the last time it was read by the CPU.

MSR(4) Clear to Send (CTS): Clear to Send (CTS) is the status of the –CTS input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output (SOUT). If the serial channel is in loop mode [MSR(4)=1], MSR(4) is equivalent to –RTS in the MCR.

MSR(5) Data Set Ready (DSR): Data Set Ready (DSR) is a status of the –DSR input from the modem to the serial channel which indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the channel is in the loop mode [MCR(4)=1], MSR(5) is equivalent to the DTR in the MCR.

## TABLE 4. MODEM STATUS REGISTER BITS

| MSR Bit | Mnemonic | Description |
|---|---|---|
| MSR (1) | DDSR | Delta Data Set Ready |
| MSR (2) | TERI | Trailing Edge of Ring Indicator |
| MSR (0) | DCTS | Delta Clear to Send |
| MSR (3) | DRLSD | Delta Data Carrier Detect |
| MSR (4) | -CTS | Clear To Send |
| MSR (5) | -DSR | Data Set Ready |
| MSR (6) | -RI | Ring Indicator |
| MSR (7) | -RLSD | Receiver Line Signal Detect |

MSR(6) Ring Indicator: Indicates the status to the RI input (pin 39). If the channel is in the loop mode [MCR(4)=1], MSR(6) is not connected in the MCR.

MSR(7) Receive Line Signal Detect : Receive Line Signal Detect indicates the status of the Receive Line Signal Detect (–RLSD) input . If the channel is in the loop mode [MCR(4)-1], MSR(4) is equivalent to OUT2 of the MCR.

The modem status inputs (–RI, –RLSD, –DSR, and –CTS) reflect the modem input lines with any change of status. Reading the MSR register will clear the delta modem status indications but has no effect on the status bits. The status bits reflect the state of the input pins regardless of the mask control signals. If a DCTS, DDSR, TERI, or DRLSD are true, and a state change occurs during a read operation (–IOR), the state change is not indicated in the MSR. If DCTS, DDSR, TERI, or DRLSD are false, and a state change occurs during a read operation, the state change is indicated after the read operation.

For LSR and MSR, the setting of status bits is inhibited during status register read –IOR operations. If a status condition is generated during a read –IOR operation, the status bit is not set until the trailing edge of the read –IOR.

If a status bit is set during a read –IOR operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read –IOR instead of being set again.

The VL16C451 serial channel contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 3.1 MHz) by any divisor from 1 to $2^{16-1}$ (see also BRG description). The output frequency of the Baud Generator is 16X the data rate [divisor # = clock ÷ (baud rate x 16)]. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These Divisor Latch registers must be loaded during initialization. Upon loading either of the Divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

The receiver circuitry in the serial channel of the VL16C451 is programmable for 5, 6, 7, or 8 data bits per character. For words of less than 8 bits, the data is right justified to the least significant bit LSB = Data Bit 0 [RBR(0)]. Data Bit 0 of a data word [RBR(0)] is the first data bit received. The unused bits in a character less than 8 bits are output low to the parallel output by the serial channel.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the 16X clock provided at the RCLK input. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the serial channel, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character result in the loss of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

RBR Bits 0 thru 7:

| | |
|---|---|
| RBR(0) | Data Bit 0 |
| RBR(1) | Data Bit 1 |
| RBR(2) | Data Bit 2 |
| RBR(3) | Data Bit 3 |
| RBR(4) | Data Bit 4 |
| RBR(5) | Data Bit 5 |
| RBR(6) | Data Bit 6 |
| RBR(7) | Data Bit 7 |

The Transmitter Holding Register (THR) holds parallel data from the data bus (D0-D7) until the Transmitter Shift Register is empty and ready to accept a new character for transmission. The transmitter and receiver word length and number of stop bits are the same. If the character is less than eight bits, unused bits at the microprocessor data bus are ignored by the transmitter.

Data Bit 0 [THR(0)] is the first serial data bit transmitted. The THRE flag [LSR(5)] reflect the status of the THR. The TEMT flag [LSR(5)] indicates if both the THR and TSR are empty.

THR Bits 0 thru 7

| | |
|---|---|
| THR(0) | Data Bit 0 |
| THR(1) | Data Bit 1 |
| THR(2) | Data Bit 2 |
| THR(3) | Data Bit 3 |
| THR(4) | Data Bit 4 |
| THR(5) | Data Bit 5 |
| THR(6) | Data Bit 6 |
| THR(7) | Data Bit 7 |

Scratchpad Register is an 8-bit Read/Write register that has no effect on either channel in the VL16C451. It is intended to be used by the programmer to hold data temporarily.

SCR Bits 0 thru 7

| | |
|---|---|
| SCR(0) | Data Bit 0 |
| SCR(1) | Data Bit 1 |
| SCR(2) | Data Bit 2 |
| SCR(3) | Data Bit 3 |
| SCR(4) | Data Bit 4 |
| SCR(5) | Data Bit 5 |
| SCR(6) | Data Bit 6 |
| SCR(7) | Data Bit 7 |

**INTERRUPTS**

The Interrupt Identification Register (IIR) in the serial channel of the VL16C451 has interrupt capability for interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (priority 1)
2. Received Data Ready (priority 2)
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). When addressed during chip select time, the IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The logic equivalent of the interrupt control circuit is shown in Figure 3. The contents of the IIR are indicated in Table 5 and are described below.

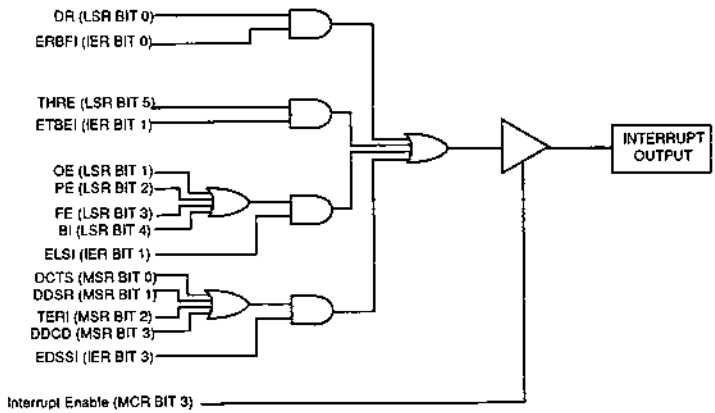
IIR(0): IIR(0) can be used in either a hard-wired prioritized or polled environment to indicate whether an interrupt is pending. When IIR(0) is low, an interrupt is pending, and IIR contents

## TABLE 5. INTERRUPT IDENTIFICATION REGISTER

| INTERRUPT IDENTIFICATION | | | | INTERRUPT SET AND RESET FUNCTIONS | | |
|---|---|---|---|---|---|---|
| Bit 2 | Bit 1 | Bit 0 | Priority Level | Interrupt Flag | Interrupt Source | Interrupt Reset Control |
| X | X | 1 | | None | None | |
| 1 | 1 | 0 | First | Receiver Line Status | OE, PE FE, or BI | LSR Read |
| 1 | 0 | 0 | Second | Received Data Available | Received Data Available | RBR Read |
| 0 | 1 | 0 | Third | THRE | THRE | IIR Read if THRE is the Interrupt Source or THR Write |
| 0 | 0 | 0 | Fourth | Modem Status | –CTS, –DSR –RI, –RSLD | MSR Read |

X = Not Defined.

FIGURE 3. INTERRUPT CONTROL LOGIC



## TABLE 6. SERIAL CHANNEL ACCESSIBLE REGISTERS

| Register Mnemonic | Register Bit Number | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| RBR (Read Only) | Data Bit 7 (MSB) | Data Bit 6 | Data Bit 5 | Data Bit 4 | Data Bit 3 | Data Bit 2 | Data Bit 1 | Data Bit 0 (LSB)* |
| THR (Write Only) | Data Bit 7 | Data Bit 6 | Data Bit 5 | Data Bit 4 | Data Bit 3 | Data Bit 2 | Data Bit 1 | Data Bit 0 |
| DLL | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DLM | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 |
| IER | 0 | 0 | 0 | 0 | (EDSSI) Enable Modem Status Interrupt | (ELSI) Enable Receiver Line Status Interrupt | (ETBEI) Enable Transmitter Holding Register Empty Interrupt | (ERBFI) Enable Received Data Available Interrupt |
| IIR (Read Only) | 0 | 0 | 0 | 0 | 0 | Interrupt ID Bit (1) | Interrupt ID Bit (0) | "0" If Interrupt Pending |
| LCR | (DLAB) Divisor Latch Access Bit | Set Break | Stick Parity | (EPS) Even Parity Select | (PEN) Parity Enable | (STB) Number of Stop Bits | (WLSB1) Word Length Select Bit 1 | (WLSB0) Word Length Select Bit 0 |
| MCR | 0 | 0 | 0 | Loop | Out 2 | Out 1 | (RTS) Request To Send | (DTR) Data Terminal Ready |
| LSR | 0 | (TEMT) Transmitter Empty | (THRE) Transmitter Holding Register Empty | (BI) Break Interrupt | (FE) Framing Error | (PE) Parity Error | (OE) Overrun Error | (DR) Data Ready |
| MSR | (DCD) Data Carrier Detect | (RI) Ring Indicator | (DSR) Data Ready Set | (CTS) Clear to Send | (DRSLD) Delta Receive Line Signal Detect | (TERI) Trailing Edge Ring Indicator | (DDSR) Delta Data Set Ready | (DCTS) Delta Clear to Send |
| SCR | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

*LSB Data Bit 0 is the first bit transmitted or received.

may be used as a pointer to the appropriate interrupt service routine. When IIR(0) is high, no interrupt is pending.

IIR(1) and IIR(2) are used to identify the highest priority interrupt pending as indicated in Table 2.

IIR(3) - IIR(7): These five bits of the IIR are logic 0.

The Interrupt Enable Register (IER) is a Write register used to independently enable the four serial channel interrupts which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER(0) - IER(3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register is described in Table 3 and below:

IER(0): When programmed high [IER(0)=Logic 1], IER(0) enables Received Data Available interrupt.

IER(1): When programmed high [IER(1)=Logic 1], IER(1) enables the Transmitter Holding Register Empty interrupt.

IER(2): When programmed high [IER(2)=Logic 1], IER(2) enables the Receiver Line Status interrupt.

IER(3): When programmed high [IER(3)=Logic 1], IER(3) enables the Modem Status Interrupt.

IER(4) - IER(7): These four bits of the IER are logic 0.

**TRANSMITTER**

The serial transmitter section consists of a Transmitter Holding Register (THR), Transmitter Shift Register (TSR), and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Shift Register Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR. To transmit a 5- to 8-bit word, the word is written through D0-D7 to the THR. The microprocessor should perform a write operation only if THRE is high. The THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

When the transmitter is idle, THRE and TEMT are high. The first word written causes THRE to be reset to 0. After the transfer, THRE returns high. TEMT remains low for at least the duration of the transmission of the data word. If a second character is transmitted to the THR, the THRE is reset low. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed sending the word. When the last word has been transmitted out of the TSR, TEMT is set high. THRE is set high one THR to TSR transfer time later.

**RECEIVER**

Serial asynchronous data is input into the SIN pin. The idle state of the line providing the input into SIN is high. A start bit detect circuit continually searches for a high to low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 7 1/2, which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR(0), LCR(1)), number of stop bits LCR(2), if parity is used LCR(3), and the polarity of parity LCR(4). Status for the receiver is provided in the Line Status Register to the Receiver Buffer Register, the Data Received indication in LSR(0) is set high. The CPU reads the Receiver Buffer Register through D0-D7. This read resets LSR(0). If D0-D7 are not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR(1). The parity check tests for even or odd parity on the parity bit, which precedes the first stop bit. If there is a parity error, the parity error is set in LSR(2). There is circuitry which tests whether the stop bit is high. If it is not, a framing error indication is generated in LSR(3).

The center of the start bit is defined as clock count 7 1/2. If the data into SIN is symmetrical square wave, the center of the data cells will occur within ± 3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16X clock cycle prior to being detected.

**BAUD RATE GENERATOR (BRG)**

The BRG generates the clocking for the UART function, providing standard ANSI/CCITT bit rates. The oscillator driving the BRG is provided by an external clock into CLK.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL=1 and DLM=0 selects the divisor to divide by 1 (divide by 1 gives maximum baud rate for a given input frequency at the CLK input).

The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 2.4576 MHz, and 3.072 MHz. With these frequencies, standard bit rates from 50 to 38.5 kbps are available. Tables 7, 8, and 9 illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

**RESET**

After power up, the VL16C451 –RESET input should be held low for 500 ns to reset the VL16C451 circuits to an idle mode until initialization. A low on –RESETcauses the following:

1. Initializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not affected.

Following removal of the reset condition (Reset high), the VL16C451 remains in the idle mode until programmed.

A hardware reset of the VL16C451 sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a reset on the VL16C451 is given in Table 10.

**PROGRAMMING**

Each serial channel of the VL16C451 is programmed by the control registers LCR, IER, DLL and DLM, and MCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control register can be written in any order, the IER should be written to last because it controls the interrupt enables. Once the serial channel is programmed and operational, these registers can be updated any time the VL16C451 serial channel is not transmitting or receiving data.

The control signals required to access each serial channel's internal registers are shown below.

**SOFTWARE RESET**

A software reset of the serial channel is a useful method for returning to a completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

**CLOCK INPUT OPERATION**

The maximum input frequency of the external clock of the VL16C451 is 3.1 MHz.

## TABLE 7. BAUD RATES (1.8432 MHz CLOCK)

| Desired Baud Rate | Divisor Used | Percent Error Difference Between Desired and Actual |
|---|---|---|
| 50 | 2304 | – |
| 75 | 1536 | – |
| 110 | 1047 | 0.026 |
| 134.5 | 857 | 0.058 |
| 150 | 768 | – |
| 300 | 384 | – |
| 600 | 192 | – |
| 1200 | 96 | – |
| 1800 | 64 | – |
| 2000 | 58 | 0.69 |
| 2400 | 48 | – |
| 3600 | 32 | – |
| 4800 | 24 | – |
| 7200 | 16 | – |
| 9600 | 12 | – |
| 19200 | 6 | – |
| 38400 | 3 | – |
| 56000 | 2 | 2.86 |

## TABLE 8. BAUD RATES (2.4576 MHz CLOCK)

| Desired Baud Rate | Divisor Used | Percent Error Difference Between Desired and Actual |
|---|---|---|
| 50 | 3072 | – |
| 75 | 2048 | – |
| 110 | 1396 | 0.026 |
| 134.5 | 1142 | 0.0007 |
| 150 | 1024 | – |
| 300 | 512 | – |
| 600 | 256 | – |
| 1200 | 128 | – |
| 1800 | 85 | 0.392 |
| 2000 | 77 | 0.260 |
| 2400 | 64 | – |
| 3600 | 43 | 0.775 |
| 4800 | 32 | – |
| 7200 | 21 | 1.587 |
| 9600 | 16 | – |
| 19200 | 8 | – |
| 38400 | 4 | – |

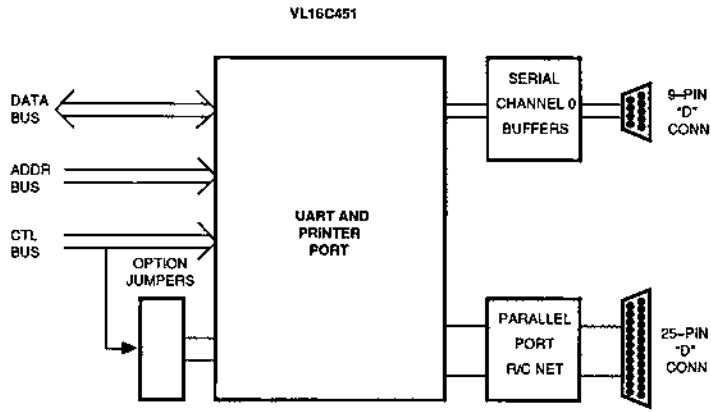
## TABLE 9. BAUD RATES (3.072 MHz CLOCK)

| Desired Baud Rate | Divisor Used | Percent Error Difference Between Desired and Actual |
|---|---|---|
| 50 | 3840 | – |
| 75 | 2560 | – |
| 110 | 1745 | 0.026 |
| 134.5 | 1428 | 0.034 |
| 150 | 1280 | – |
| 300 | 640 | – |
| 600 | 320 | – |
| 1200 | 160 | – |
| 1800 | 107 | 0.312 |
| 2000 | 96 | – |
| 2400 | 80 | – |
| 3600 | 53 | 0.628 |
| 4800 | 40 | – |
| 7200 | 27 | 1.23 |
| 9600 | 20 | – |
| 19200 | 10 | – |
| 38400 | 5 | – |

## TABLE 10. RESET

| Register/Signal | Reset Control | Reset |
|---|---|---|
| Interrupt Enable Register | Reset | All Bits Low (0–3 forced and 4–7 permanent) |
| Interrupt Identification Register | Reset | Bit 0 is High, Bits 1 and 2 Low<br>Bits 3–7 are Permanently Low |
| Line Control Register | Reset | All Bits Low |
| MODEM Control Register | Reset | All Bits Low |
| Line Status Register | Reset | All Bits Low, Except Bits 5 and 6 are High |
| MODEM Status Register | Reset | Bits 0–3 Low<br>Bits 4–7 Input Signal |
| SOUT | Reset | High |
| Intrpt (RCVR Errs) | Read LSR/Reset | Low |
| Intrpt (RCVR Data Ready) | Read RBR/Reset | Low |
| Intrpt (THRE) | Read IIR/Write THR/Reset | Low |
| Intrpt (Modem Status Changes) | Read MSR/Reset | Low |
| –Out2 | Reset | High |
| –RTS | Reset | High |
| –DTR | Reset | High |
| –Out1 | Reset | High |

## DEVICE APPLICATION



## FUNCTIONAL DESCRIPTION

### PARALLEL PORT REGISTERS

The VL16C451's parallel port interfaces the device to a Centronics-style printer. When Chip Select 2 (–CS2) is low, the parallel port is selected. Table 11 shows the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read (–IOR) and write (–IOW) pin as shown. The Read Data Register allows the microprocessor to read the information on the parallel bus.

The Read Status Register allows the microprocessor to read the status of the printer in the five most significant bits. The status bits are Printer Busy (–BUSY), Acknowledge (–ACK) which is a handshake function, Paper Empty (PE), Printer Selected (SLCT), and Error (–ERROR). The Read Control Register allows the state of the control lines to be read. The Write Control Register sets the state of the control lines.

They are Interrupt Enable (IRQ ENB), Select In (SLIN), Initialize the Printer (–INIT), Autofeed the Paper (AUTOFD), Strobe (STROBE), which informs the printer of the presence of a valid byte on the parallel bus. The Write Data Register allows the microprocessor to write a byte to the parallel bus.

The parallel port is completely compatible with the parallel port implementation used in the IBM Serial/Parallel Adaptor.

### TABLE 11. PARALLEL PORT REGISTERS

| Register | Register Bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Read Data | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Read Status | –BUSY | –ACK | PE | SLCT | –ERROR | 1 | 1 | 1 |
| Read Control | 1 | 1 | 1 | IRQ ENB | SLIN | –INIT | AUTOFD | STROBE |
| Write Data | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Write Control | 1 | 1 | 1 | IRQ ENB | SLIN | –INIT | AUTOFD | STROBE |

### TABLE 12. PARALLEL PORT REGISTER SELECT

| Control Pins | | | | | Register Selected |
|---|---|---|---|---|---|
| –IOR | –IOW | –CS2 | A1 | A0 | |
| 0 | 1 | 0 | 0 | 0 | Read Data |
| 0 | 1 | 0 | 0 | 1 | Read Status |
| 0 | 1 | 0 | 1 | 0 | Read Control |
| 0 | 1 | 0 | 1 | 1 | Invalid |
| 1 | 0 | 0 | 0 | 0 | Write Data |
| 1 | 0 | 0 | 0 | 1 | Invalid |
| 1 | 0 | 0 | 1 | 0 | Write Control |
| 1 | 0 | 0 | 1 | 1 | Invalid |

## AC CHARACTERISTICS TA= 0°C to +70°C, VCC= 5 V ±5% (Notes 1, 5)

| Symbol | Parameter | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| tDIW | –IOR Strobe Width | 125 | | ns | |
| RC | Read Cyte | 360 | | ns | |
| tDDD | Delay from –IOR to Data | | 125 | ns | 100 pF Load |
| tHZ | –IOR to Floating Data Delay | 0 | 100 | ns | 100 pF Load, Note 4 |
| tDOW | –IOW Strobe Width | 100 | | ns | |
| WC | Write Cycle | 360 | | ns | |
| tDS | Data Setup Time | 40 | | ns | |
| tDH | Data Hold Time | 40 | | ns | |
| tRA | Address Hold Time from –IOR | 20 | | ns | Note 2 |
| tRCS | Chip Select Hold Time from –IOR | 20 | | ns | Note 2 |
| tAR | –IOR Delay from Address | 60 | | ns | Note 2 |
| tCSR | –IOR Delay from Chip Select | 50 | | ns | Note 2 |
| tWA | Address Hold Time from–IOW | 20 | | ns | Note 2 |
| tWCS | Chip Select Hold Time from –IOW | 20 | | ns | Note 2 |
| tAW | –IOW Delay from Address | 60 | | ns | Note 2 |
| tCSW | –IOW Delay from Select | 50 | | ns | Note 2 |
| tRW | Reset Pulse Width | 5 | | µs | |
| tXH | Duration of Clock High Pulse | 140 | | ns | External Clock |
| tXL | Duration of Clock Low Pulse | 140 | | ns | External Clock |

**Notes:**

1. All timing specifications apply to pins on both serial channels (e.g. RI refers to both RI0 and RI1).
2. The internal address strobe is always active.
3. RCLK = tXH and tXL.
4. Charge and discharge time is determined by VOL, VOH and the external loading.
5. All timings are referenced to valid 0 and valid 1.
   (see AC TEST POINTS).

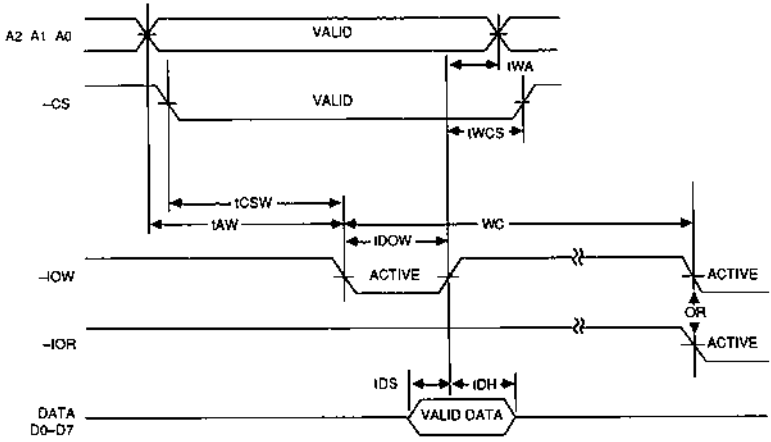
## AC CHARACTERISTICS (Cont.) TA= 0°C to +70°C, VCC= 5 V ±5% (Notes 1, 5)

| Symbol | Parameter | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| **Transmitter** | | | | | |
| tHR1 | Delay from Rising Edge of –IOW (WR THR) To Reset Interrupt | | 175 | ns | 100 pF Load |
| tRS | Delay from Initial INTR Reset to Transmit Start | | 16 | CLK Cycles | Note 3 |
| tSI | Delay from Initial Write to Interrupt | 8 | 24 | CLK Cycles | Note 3 |
| tSTI | Delay from Stop to Interrupt (THRE) | | 8 | CLK Cycles | Note 3 |
| tIR | Delay from –IOR (RD IIR) to Reset Interrupt (THRE) | | 250 | ns | 100 pF Load |
| **Modem Control** | | | | | |
| tMDO | Delay from –IOW (WR MCR) to Output | | 250 | ns | 100 pF Load |
| tSIM | Delay to Set Interrupt from MODEM Input | | 250 | ns | 100 pF Load |
| tRIM | Delay to Reset Interrupt from –IOR (RS MSR) | | 250 | ns | 100 pF Load |
| **Receiver** | | | | | |
| tSINT | Delay from Stop to Set Interrupt | | 1 | CLK Cycles | Note 3 |
| tRINT | Delay from –IOR (RD RBR/RDLSR) to Reset Interrupt | | 1 | µs | 100 pF Load |
| **Parallel Port** | | | | | |
| tDT | Data Time | 1 | | µs | |
| tSB | Strobe Time | 1 | 500 | µs | |
| tAD | Acknowledge Delay (Busy Start to Acknowledge) | | | µs | Defined by Printer |
| tAKD | Acknowledge Delay (Busy End to Acknowledge) | | | µs | Defined by Printer |
| tAK | Acknowledge Duration Time | | | µs | Defined by Printer |
| tBSY | Busy Duration Time | | | µs | Defined by Printer |
| tBSD | Busy Delay Time | | | µs | Defined by Printer |

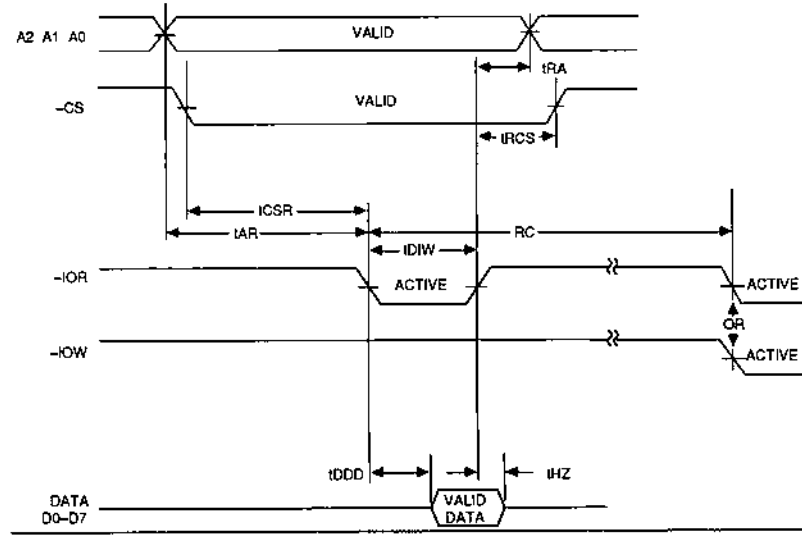
**Notes:**

1. All timing specifications apply to pins on both serial channels (e.g. RI refers to both RI0 and RI1).
2. The internal address strobe is always active.
3. RCLK = tXH and tXL.
4. Charge and discharge time is determined by VOL, VOH and the external loading.
5. All timings are referenced to valid 0 and valid 1 (see AC TEST POINTS).

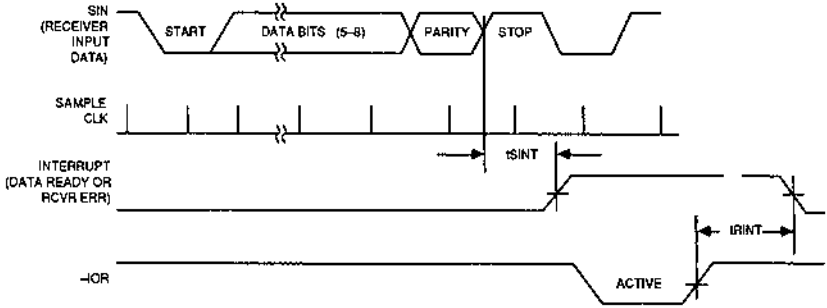
## WRITE CYCLE TIMING



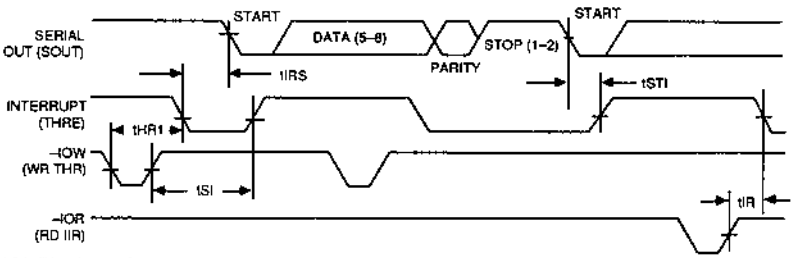

## READ CYCLE TIMING



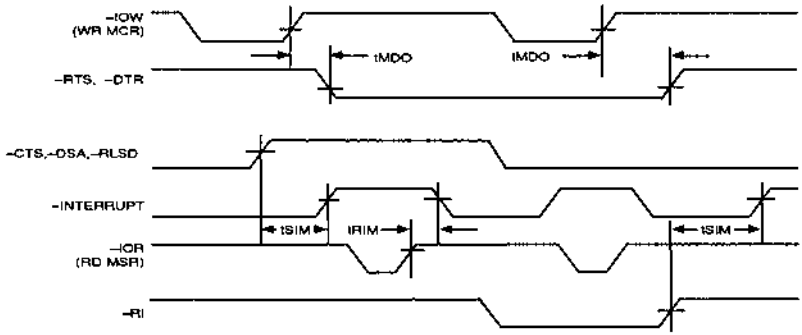
## RECEIVER TIMING



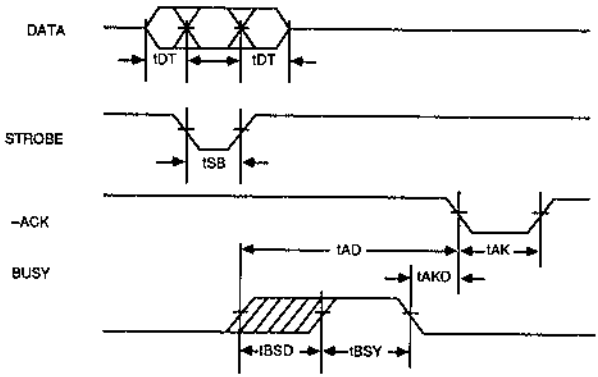

## TRANSMITTER TIMING



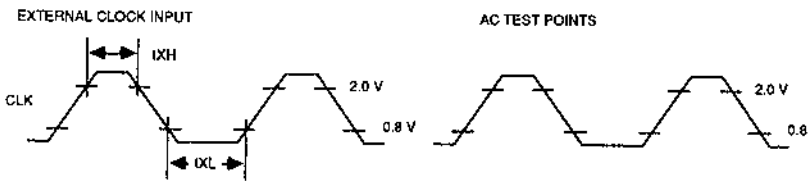

## MODEM TIMING



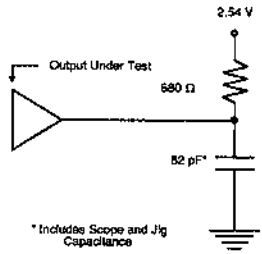
## PARALLEL PORT TIMING




## AC TESTING INPUT/OUTPUT WAVEFORMS




## TEST CIRCUIT



## ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature −10°C to +70°C

Storage Temperature −65°C to + 150°C

Supply Voltage to Ground Potential −0.5 V to VCC + 0.3 V

Applied Output Voltage −0.5 V to VCC + 0.3 V

Applied Input Voltage −0.5 V to + 7.0V

Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

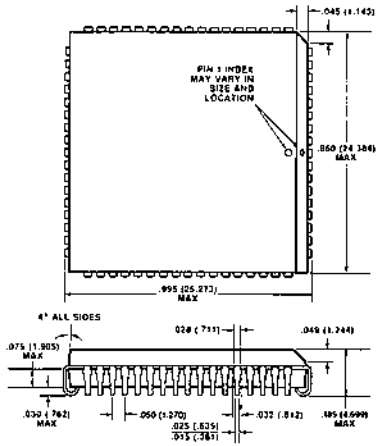
## DC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ± 5%

| Symbol | Parameter | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| VILX | Clock Input Low Voltage | −0.5 | 0.8 | V | |
| VIHX | Clock Input High Voltage | 2.0 | VCC | V | |
| VIL | Input Low Voltage | −0.5 | 0.8 | V | |
| VIH | Input High Voltage | 2.0 | VCC | V | |
| VOL | Output Low Voltage | | 0.4 | V | IOL = 4.0 mA on DB0 - DB7<br>IOL = 12 mA on PD0 - PD7<br>IOL = 10 mA on −INIT, −AFD, −STB, and −SLIN (see Note 1)<br>IOL = 2.0 mA on all other outputs |
| VOH | Output High Voltage | 2.4 | | V | IOH = −0.4 mA on DB0 - DB7<br>IOH = −2.0 mA on PD0 - PD7<br>IOH = −0.2 mA on −INIT, −AFD, −STB, and −SLIN<br>IOH = −0.2 mA on all other outputs |
| ICC | Power Supply Current | | 50 | mA | VCC = 5.25 V. No loads on SIN0; −DSR0; −RLSD0; −CTS0. −RI0 = 2.0 V. Other inputs = 0.8 V. Baud rate generator = 4 MHz. Baud rate = 56K |
| IIL | Input Leakage | | ±10 | µA | VCC = 5.25 V, GND = 0 V. All other pins floating. |
| ICL | Clock Leakage | | ±10 | µA | VIN = 0 V, 5.25 V |
| IOZ | 3-State Leakage | | ±20 | µA | VCC = 5.25 V, GND = 0 V.<br>VOUT = 0 V, 5.25 V<br>1) Chip deselected<br>2) Chip and write mode selected |
| VIL(RES) | Reset Schmitt VIL | | 0.8 | V | |
| VIH(RES) | Reset Schmitt VIH | 2.0 | | V | |

**Note 1.** −INIT, −AFD, −STB, and −SLIN are open collector output pins that each have an internal pull-up resistor (2.5 kΩ - 3.5 kΩ) to VCC. This will generate a maximum of 2.0 mA of internal IOL. In addition to this internal current, each pin will sink at least 10 mA, while maintaining the VOL specification of 0.4 V Max.

## PACKAGE OUTLINE

**68-PIN PLASTIC LEADED CHIP CARRIER (PLCC)**




NOTES: UNLESS OTHERWISE SPECIFIED
1. TOLERANCE TO BE ± .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG PULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES

VLSI TECHNOLOGY, INC.

# VL16C451

## VLSI CORPORATE OFFICES

CORPORATE HEADQUARTERS • ASIC AND MEMORY PRODUCTS • VLSI Technology, Inc. • 1109 McKay Drive • San Jose, CA 95131 • 408-434-3100
APPLICATION SPECIFIC LOGIC AND GOVERNMENT PRODUCTS • VLSI Technology, Inc. • 8375 South River Parkway • Tempe, AZ 85284 • 602-752-8574

## VLSI SALES OFFICES & DESIGN CENTERS

**CALIFORNIA**
2220 Dunn Dr
San Jose CA 95131
408-943-0864
FAX 408-943-9792
TELEX 278807
MAIL
1109 McKay Dr
San Jose CA 95131

1751 E Garry Ave Ste A
Santa Ana CA 92705
714-250-4700
FAX 714-250-9541

**FLORIDA**
2200 Park Central N Ste 400
Pompano Beach FL 33064
305-971-0404
FAX 305-971-2065

**ILLINOIS**
1300 Remington Rd Stes A-D
Schaumburg, IL 60195
312-310-9590
FAX 312-310-9632

**MASSACHUSETTS**
281 Ballardvale St
Wilmington, MA 01887
617-658-9501
FAX 617-657-6430

**NEW JERSEY**
101 Morgan Lane Ste 340
Plainsboro, NJ 08536
609-799-5700
FAX 609-799-5720

**TEXAS**
850 E Arapaho Rd Ste 270
Richardson, TX 75081
214-231-6715
FAX 214-669-1113

**FRANCE**
2 Allee du 10 Mai Arnouvel
Cravat
F-91120 Palaiseau France
1 64 47 04 79
TELEX Vlsifr 600 759 F
FAX 1-64 47 04 85

**GERMANY**
Rosenkavalierplatz 10
D-8000 Munich 81
West Germany
0 89/92 69 05 0
TELEX 521 4279 vlsid
FAX 0 89-9269345

**JAPAN**
Shuwa Kioicho Tower Bldg Rm 816
3-7 Kioicho Chiyoda Ku
Tokyo Japan 102
81 3 239 5211
FAX 81 3 239 5215

**UNITED KINGDOM**
496-498 Midsummer Blvd
South Gate West Central
Milton Keynes MK9 2EG
United Kingdom
0 0908 73 95
TELEX Vlsiuk 825 133
FAX 0 0908 00 27

## VLSI AUTHORIZED DESIGN CENTERS

**COLORADO**
SJS ENGINEERS ELECTRONICS, INC
Longmont 303 776-1607

**MAINE**
DIGITAL SYSTEMS, INC
South Portland 207-871-8214

**PENNSYLVANIA**
INTEGRATED CIRCUIT SYSTEMS, INC.
King of Prussia 215-265-8890

**IRELAND**
AXIOM ELECTRONICS LTD.
High Wycombe Bucks
0 94940 10 10

**SWEDEN**
NORDISK ARRAYTEKNIK AB
Solna (08) 734 99 33

## VLSI SALES OFFICES

**ALABAMA**
2814 Jane St, Ste 36
Huntsville AL 35805
205-539-3812
FAX 205-536-8622

**ARIZONA**
8375 South River Parkway
Tempe AZ 85284
602-752-8400
FAX 602 752-8000

**CALIFORNIA**
225 W Broadway, Ste 300
Glendale CA 91204
818-995-2404

**CONNECTICUT**
60 Church St
Waterbury CT 06492
203-263-6696
FAX 203-263-3653

**FLORIDA**
901 Cleveland St Ste 405
Clearwater FL 33515
813-443-5707
FAX 813-443-5674

**GEORGIA**
2400 Pleasant Hill Rd Ste 200
Duluth GA 30136
404-476-8374
FAX 404-476-3790

**MARYLAND**
P O Box 289
104 Maryland Rte 3 N
Millersville MD 21108
301 987 8777
FAX 301-987-0779

**MINNESOTA**
5851 Cedar Lake Rd Ste 9
St Louis Park MN 55416
612 545-1190
FAX 612 545-2409

**NORTH CAROLINA**
2400 West Paces Ch Ste 201
Research Triangle Park NC 27713
919-544-0811-42
FAX 919-361-1843

**OREGON**
10000 SW Greenburg Rd Ste 365
Portland OR 97223
503-241-9662
FAX 503-245-0215

## VLSI SALES REPRESENTATIVES

**ARIZONA**
SYSTEM SALES OF ARIZONA
Tempe 602-829-3338

**CALIFORNIA**
BESTRONICS
San Diego 619-693-1131

EMERGING TECHNOLOGY
San Jose 408-433-9366

EMERGING TECHNOLOGY
Fremont 510-792-3030

**COLORADO**
LUSCOMBE ENGINEERING
Longmont 303 772-3342

**IOWA**
SELTEC SALES
Cedar Rapids 319 364-7660

**KANSAS**
SPECTRUM SALES
Overland Park 913-648-8611

**MISSOURI**
SPECTRUM SALES
Maryland 314 731 5151

**NEW MEXICO**
SYSTEM SALES OF ARIZONA
Albuquerque 505-247-7958

**NEW YORK**
ebd ELECTRONICS
Rochester, 716-425-4101

**OHIO**
SAI MARKETING
Columbus 614-876-9660

SAI MARKETING
Dayton 513-435-3181

SAI MARKETING
Shaker Heights 216-751-3633

**OKLAHOMA**
LOGIC 1 SALES
Tulsa 918-494-0782

**OREGON**
MICRO SALES
Beaverton 503-643-7844

**TEXAS**
LOGIC 1 SALES
Austin 512-459-1797

LOGIC 1 SALES
Richardson 214-234-0166

**WASHINGTON**
MICRO SALES
Bellevue 206-641-0369

**AUSTRALIA**
ENERGY CONTROL
Brisbane 61 7 3762851

**BELGIUM AND LUXEMBURG**
DIODE
Brussels, (02) 218 2105

**CANADA**
ebd ELECTRONICS
Port Coquitlam, B C
604-941-7787

ebd ELECTRONICS
Mississauga Ontario
416-624-7800

ebd ELECTRONICS
Ottawa Ontario
613-729-0022

ebd ELECTRONICS
Pointe Claire Quebec
514 697-0804

**HONG KONG**
LESTICA INTERNATIONAL, LTD
Kowloon 3 7721736

**ISRAEL**
RET ELECTRONICS ENGINEERING LTD.
Tel-Aviv, (3) 44 32 11-9

**KOREA**
EASTERN ELECTRONICS
Seoul 82 02-444-0379

**SINGAPORE**
DYNAMIC SYSTEMS ELECTRONICS
Singapore, 65-293-9024

**TAIWAN**
PRINCETON TECH
Taipei 886-2-737-1439

## VLSI DISTRIBUTORS

(A) ARROW ELECTRONICS, INC.
(S) SCHWEBER ELECTRONICS

**ALABAMA**
Huntsville 205-837-6955 (A)
Huntsville 205-895-0480 (S)

**ARIZONA**
Phoenix 602 966-4600 (A)
Phoenix 602 997-4874 (S)

**CALIFORNIA**
Canoga Park 818-996-4100 (S)
Gardena 213-320-8090 (S)
Irvine 714-863-0200 (S)
Los Angeles 818-701-7500 (A)
Orange County 714-838-5422 (A)
Sacramento 916-929-9732 (S)
San Diego 619 163-4800 (A)
San Diego 619-450-0454 (S)
San Francisco 408-743-4600 (A)
San Jose 408-432-1171 (S)

**COLORADO**
Denver 303-696-1111 (A)
Englewood 303-799-0958 (S)

**CONNECTICUT**
Danbury 203-748-7080 (S)
Wallingford 203-265-7741 (A)

**FLORIDA**
Altamonte Springs 305-331-7555 (S)
Clearwater 813-576-8999 (A)
Fort Lauderdale 305-429-8200 (A)
Melbourne 305-725-1480 (A)
Pompano Beach 305-977-7511 (S)

**GEORGIA**
Atlanta 404-449-8252 (A)
Norcross 404-448-1800 (S)

**ILLINOIS**
Chicago 312 397-3440 (A)
Elk Grove Village 312-364-3750 (S)

**INDIANA**
Indianapolis 317-243-9353 (A)

**IOWA**
Cedar Rapids 319-395-7230 (A)
Cedar Rapids 319-373-1417 (S)

**KANSAS**
Overland Park 913-492-2922 (S)

**MARYLAND**
Baltimore 301-995-6002 (A)
Gaithersburg 301-840-9800 (S)

**MASSACHUSETTS**
Bedford 617 275 5100 (S)
Boston 617-933-8130 (A)

**MICHIGAN**
Detroit 313-971-8220 (A)
Grand Rapids 616-243-0912 (A)
Livonia 313-525-8100 (S)

**MINNESOTA**
Edina 612 941 5280 (S)
Minneapolis 612-830-1800 (A)

**MISSOURI**
Earth City 314 739-0526 (S)
St Louis 314-567-6888 (A)

**NEW HAMPSHIRE**
Manchester 603-668-6968 (A)
Manchester 603-625-2250 (S)

**NEW JERSEY**
Parsippany 201-575-5300 (A)
Fairfield 201 227-7880 (S)
Marlton 609 596-8000 (A)

**NEW MEXICO**
Albuquerque 505-243-4566 (A)

**NEW YORK**
Long Island, 516-231 1000 (A)
Rochester 716-427-0300 (A)
Rochester 716-424-2222 (S)
Syracuse 315-652 1000 (A)
Westbury 516-334-7474 (S)

**NORTH CAROLINA**
Raleigh 919-878-3132 (A)
Raleigh 919-878-0000 (S)
Winston Salem 919 725-8711 (A)

**OHIO**
Beachwood 216-464-2970 (S)
Cleveland 216-248-3990 (A)
Columbus 614-883-3087 (A)
Dayton 513-435-5563 (A)
Dayton 513-439-1800 (S)

**OKLAHOMA**
Tulsa 918-665-7700 (A)
Tulsa 918-622-8000 (S)

**OREGON**
Portland 503-641-3200 (A)

**PENNSYLVANIA**
Horsham, 215-441-0600 (S)
Philadelphia 215-995-1800 (A)
Pittsburgh 412-856-7000 (A)
Pittsburgh 412-782-1800 (S)

**RHODE ISLAND**
East Providence, 401-431-0980 (A)

**TEXAS**
Austin 512-835-4180 (A)
Austin 512-458-8253 (S)
Dallas 214-380-6464 (A)
Dallas, 214-661 5010 (S)
Houston 713-530-4700 (A)
Houston 713-784 3600 (S)

**UTAH**
Salt Lake City, 801 972-0404 (A)

**WASHINGTON**
Seattle, 206-843-4600 (A)

**WISCONSIN**
Menomonee 414-797-0150 (A)
New Berlin, 414 784 9020 (S)

**PUERTO RICO**
San Juan, 809-723-6500 (A)

**CANADA**
Montreal 514 735-5511 (A)
Ottawa, 613-226-6903 (A)
Quebec City 418-687-4231 (A)
Toronto, 416-661 0220 (A)

**FRANCE**
ASAP s.a.
Montigny-le-Bretonneux,
(1) 30 43 82 33

**GERMANY**
DATA MODUL GmbH
Munich 0 89/5 80 13 0

ebv-electronic AG
Munich 0 89/4180 07 20

SE SPEZIAL-ELECTRONIC KG
Buchenrain, 0 9722/70 32

**JAPAN**
ASAHI GLASS CO. LTD
Tokyo 81-3-218 5854

TESEL COMPANY, LTD.
Tokyo 81-3481-3211

TOKYO ELECTRON, LTD
Tokyo 81-03-35-8009

**NORWAY**
EASTERN ELECTRONICS
Seoul 82-02-484-0299

**NETHERLANDS**
OMODE
Houten (0) 34 001 912 34

**SOUTH AMERICA - BRAZIL**
INTERNATIONAL TRADE DEVELOPMENT
Sao Alto, 455-856-6696

**SPAIN AND PORTUGAL**
SEMICONDUCTORES s.a
Barcelona (3) 217 73 40

**SWITZERLAND**
FABRIMEX AG
Zurich (01) 2 39 79 79

The information contained in this document has been carefully checked and is believed to be reliable. However, VLSI Technology, Inc., (VLSI) makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon, it. VLSI does not guarantee that the use of any information contained herein will not infringe upon the patent or other rights of third parties, and no patent or other license is implied hereby.
This document does not in any way extend VLSI's warranty on any product beyond that set forth in its standard terms and conditions of sale. VLSI Technology, Inc., reserves the right to make changes in the products or specifications, or both, presented in this publication at any time and without notice.
LIFE SUPPORT APPLICATIONS
VLSI Technology, Inc., products are not intended for use as critical components in life support appliances, devices, or systems in which the failure of a VLSI Technology product to perform could reasonably be expected to result in personal injury. Please contact VLSI for the latest information concerning this product.
© 1988 VLSI Technology, Inc. Printed in U.S.A.
8350-190451-001 15M

# 82C206
# INTEGRATED PERIPHERALS CONTROLLER

- **100% Compatible to IBM™ PC AT**
- **Fully compatible to Intel™'s 8237 DMA controller, 8259 Interrupt controller, 8254 Timer/Counter, and Motorola™'s 146818 Real Time Clock**
- **Offers 7 DMA channels, 13 Interrupt request channels, 2 Timer/Counter channels, and a Real Time Clock**
- **Reduced recovery time (120 ns) between control**
- **114 bytes of CMOS RAM memory**
- **8 MHz DMA clock with programmable internal divider for 4 MHz operation**
- **Programmable wait states for the DMA cycle**
- **16 Mbytes DMA address space**
- **Single chip 84-pin CMOS implementation**

The 82C206 Integrated Peripheral Controller incorporates two 8237 DMA controllers, two 8259 Interrupt controllers, one 8254 Timer/Counter, one MC146818 Real Time Clock, 74LS612 memory mapper, in addition to several other TTL/SSI interface logic chips to offer a single chip integration of all the peripherals attached to the peripheral bus (X-Bus) in the IBM™ PC AT™. While offering a complete compatibility to the IBM PC AT architecture, the chip offers enhanced features and improved speed performance. These include an additional 64 bytes of user RAM for the Real Time Clock, and drastically reduced recovery specifications for the 8237, 8259 and 8254. Variable wait state option is provided for the DMA cycles. Programmable delays are provided for the CPU access to the internal registers of the chip. The chip also provides an option to select 8 or 4 MHz system clock.

The 82C206, along with the CS8220 PC AT Compatible CHIPSet, provides a highly integrated high performance solution for a PC AT compatible implementation.

The 82C206 is implemented using advanced CMOS technology and is packaged in an 84-pin PLCC.

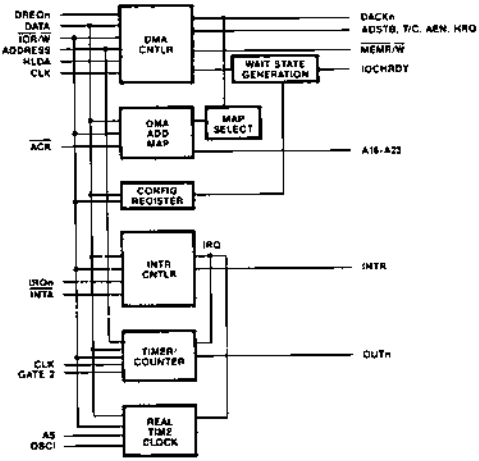
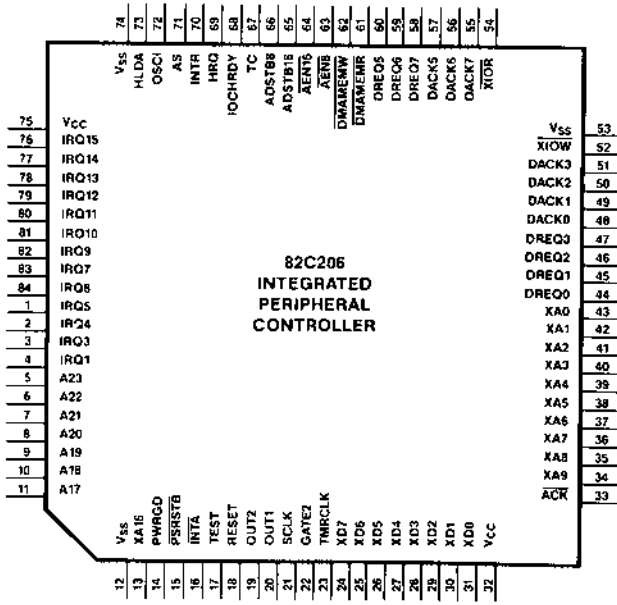



**Figure 1. 82C206 Integrated Peripheral Controller Block Diagram**


82C206
INTEGRATED
PERIPHERAL
CONTROLLER
Vcc 75
IRQ15 76
IRQ14 77
IRQ13 78
IRQ12 79
IRQ11 80
IRQ10 81
IRQ9 82
IRQ7 83
IRQ6 84
IRQ5 1
IRQ4 2
IRQ3 3
IRQ1 4
A23 5
A22 6
A21 7
A20 8
A19 9
A18 10
A17 11
Vss 12
XA16 13
PWRGD 14
PSRSTB 15
INTA 16
TEST 17
RESET 18
OUT2 19
OUT1 20
SCLK 21
GATE2 22
TMRCLK 23
XD7 24
XD6 25
XD5 26
XD4 27
XD3 28
XD2 29
XD1 30
XD0 31
Vcc 32
Vss 74
HLDA 73
OSCI 72
AS 71
INTR 70
HRQ 69
IOCHRDY 68
TC 67
ADSTB8 66
ADSTB16 65
AENTS 64
AENB 63
DMAMEMW 62
DMAMEMR 61
DREQ5 60
DREQ6 59
DREQ7 58
DACK5 57
DACK6 56
DACK7 55
XIOR 54
Vss 53
XIOW 52
DACK3 51
DACK2 50
DACK1 49
DACK0 48
DREQ3 47
DREQ2 46
DREQ1 45
DREQ0 44
XA0 43
XA1 42
XA2 41
XA3 40
XA4 39
XA5 38
XA6 37
XA7 36
XA8 35
XA9 34
ACK 33

## 82C206 Pin Description

| Pin No. | Name | Type | Function |
|---|---|---|---|
| 24-31 | XD7-XD0 | I/O | DATA BUS: The Data Bus lines are 3-state bi-directional lines connected to the system data bus (XD bus in a PC/AT design). The outputs are enabled in the program condition during the I/O Read to output the contents of the DMA controller registers (Address register, Status register, the Temporary register or a Word Count register), the three Interrupt Controller registers (Interrupt Request register, In Service register and the Interrupt Mask register), the Timer/Counters registers (namely the contents of these counters or states of the counters), the Real Time Clocks internal registers and page registers of memory mapper.<br><br>During an I/O write cycle, the outputs are disabled and the CPU can program the DMA Controller registers, the Interrupt Controller registers, the Timer/Counters registers, the DMA Page register and the Real Time Clock registers and internal RAM.<br><br>During DMA cycles, the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB8 or ADSTB16. During memory-to-memory operations, data from the memory comes into the DMA Controller on the data bus during read from the memory. In the write to memory transfer, the data bus outputs place the data into the new memory location.<br><br>During the interrupt sequence, the interrupt controllers output the interrupt vector byte on the data bus.<br><br>Data bus XD7-XD0 also acts as the multiplexed address/data bus for the Real Time Clock. |

**82C206 Pin Description** (Continued)

| Pin No. | Name | Type | Function |
|---|---|---|---|
| 35-43<br>34 | XA8-XA0<br>XA9 | I/O<br>I | ADDRESS BUS: This is the system address bus used to address various registers of the 82C206. It is tied to the external bus (XA bus) in a PC/AT compatible design. During a non-DMA cycle, A3-A0 act as inputs and are used by the CPU to address the registers of the DMA Controller corresponding to DMA channels 0-3 and A4-A1 address the registers of the DMA Controller corresponding to DMA channels 5-7. In the active DMA cycle, A7-A0 are outputs and carry address information for DMA channels 0-3. Correspondingly, A8-A1 are address outputs for 16 bit DMA channels 5-7. During program condition, A9-A0 are used to address configuration register and the internal registers of DMA Controller, INT Controller, Timer, RTC and Memory Mapper. |
| 18 | RESET | I | RESET: Reset is active high input which affects the following registers:<br><br>DMA Controllers: Clears the Command, Status, DMA Request, Temporary register, First/Last flip-flop; sets the Mask register. Following reset, the DMA controller is in an idle state.<br><br>INTERRUPT Controllers: Clears the edge sense circuit, the interrupt mask register, all ICW4 functions, IRQ0 is assigned highest priority, slave address is set to 7, special mask mode is disabled and status read is set to IRR. |
| 54 | $\overline{\text{XIOR}}$ | I/O | I/O READ: I/O Read is a bidirectional active low three-state line. In an idle cycle (non DMA, non-interrupt), it is an input control signal used by the CPU to read the 82C206 internal registers. In an active DMA cycle, it is an output control signal used by the DMA Controller to access data from a peripheral during a DMA write transfer. |
| 52 | $\overline{\text{XIOW}}$ | I/O | I/O WRITE: I/O Write is a bidirectional active low three-state signal. In an idle cycle (non-DMA, non-interrupt) it is an input control signal used by the CPU to load information to the 82C206 internal registers. In an active DMA cycle, it is an output control signal used by the DMA Controller to load data to the peripheral during a DMA Read transfer. |
| 61 | $\overline{\text{DMAMEMR}}$ | O | DMA MEMORY READ: $\overline{\text{DMAMEMR}}$ is an active low three-state output used to access data from the selected memory location during DMA Read or memory-to-memory transfer. |

**82C206 Pin Description** (Continued)

| Pin No. | Name | Type | Function |
|---|---|---|---|
| 62 | $\overline{\text{DMAMEMW}}$ | O | DMA MEMORY WRITE: $\overline{\text{DMAMEMW}}$ is an active low three-state output used to write data to the selected memory location during DMA write or a memory-to-memory transfer. In a PC/AT compatible design, this signal is connected to $\overline{\text{XMEMW}}$. |
| 21 | SCLK | I | CLOCK INPUT: The Clock Input is used to generate the timing signals which control DMA operations. This input may be driven from DC to 10 MHz. The Clock may be stopped in either state for standby operation. The internal clock used for DMAC is either the SCLK or SCLK/2 depending on the setting of DMA CLOCK SELECT bit in the configuration register. |
| 68 | IOCHRDY | I/O | I/O CHANNEL READY: In the input mode, a low on IOCHRDY causes the internal DMA ready signal to go low asynchronously. When IOCHRDY goes high, one DMA Clock cycle will elapse before internal DMA Ready goes up. This signal is used to extend memory read and write pulses for the DMA controllers to accommodate slow memories or I/O devices. IOCHRDY must satisfy set-up and hold times with respect to DMACLK in order to work reliably.<br><br>In the output mode, this pin is an open drain output and provides an active low output whenever any 82C206 register is addressed for read or write. This output will remain low for a programmed number of DMACLK cycles (as configured by bits 6 and 7 of 82C206 configuration register) and then goes high, if pulled up by an external register. IOCHRDY provides a means of introducing a programmed number of wait-states (as counted by DMACLK cycles) for I/O read/write cycles to 82C206. In a PC/AT architecture based design this pin should be wire-ored to PC/AT's IOCHRDY signal. |
| 73 | HLDA | I | HOLD ACKNOWLEDGE: The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system busses. |

**82C206 Pin Description** (Continued)

| Pin No. | Name | Type | Function |
|---|---|---|---|
| 44-<br>47<br>60-<br>58 | DREQ0-<br>DREQ3<br>DREQ5-<br>DREQ7 | I | DMA REQUEST: The DMA Request (DREQ) are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In Fixed Priority, DREQ0 has the highest priority and DREQ7 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active. DREQ will not be recognized while the clock is stopped. Unused DREQ inputs should be pulled High or Low (inactive) and the corresponding mask bit set.<br><br>DREQ0–DREQ3 support 8-bit transfers between 8-bit I/O and 8 or 16-bit system memory. DREQ5-DREQ7 support 16-bit data transfers between 16-bit peripheral and 16-bit system memory. DREQ4 is not available as it is used to cascade DREQ0-DREQ3. |
| 67 | TC | O | TERMINAL COUNT: Terminal Count (TC) is an active high signal. Information concerning the completion of DMA services is available at the TC output pin.<br><br>A pulse is generated by the DMA Controller when terminal count (TC) for any channel is reached, except for channel 0 in memory-to-memory mode. During memory-to-memory transfers TC will be output when the TC for channel 1 occurs.<br><br>When a TC pulse occurs, the DMA Controller will terminate the service, and if auto-initialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel unless the channel is programmed for auto-initialize. In that case, the mask bit remains clear. |

**82C206 Pin Description** (Continued)

| Pin No. | Name | Type | Function |
|---|---|---|---|
| 69 | HRQ | O | HOLD REQUEST: The Hold Request (HRQ) output is used to request control of the system bus. When a DREQ occurs and the corresponding mask bit is clear, or a software DMA request is made, the DMA Controller issues HRQ. The HLDA signal then informs the controller when access to the system busses is permitted. For stand-alone operation where the DMA Controller always controls the busses, HRQ may be tied to HLDA. This will result in one SO state before the transfer. |
| 48-<br>51<br>57-<br>55 | DACK0-<br>DACK3<br>DACK5-<br>DACK7 | O | DMA ACKNOWLEDGE: DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The active polarity of these lines is programmable. Reset initializes them to active low. Because these signals are used internally for cascading the DMA channels and for DMA page register selection, these signals must be programmed to be active low. |
| 66 | ADSTB8 | O | ADDRESS STROBE: This is an active high signal used to control latching of the upper address byte (A8-A15) for 8-bit peripherals. It will drive directly the strobe input of external transparent octal latches. During block operations, ADSTB8 will only be issued when the upper address byte must be updated, thus speeding operation through elimination of S1 states. ADSTB8 is active for DMA channels 0-3. |
| 64 | $\overline{\text{AEN16}}$ | 0 | ADDRESS ENABLE for 16-BIT DMA TRANSFERS: This signal enables the 8-bit latch containing the upper 8 address bits (A9-A16) on to system address bus. It is inactive when external bus master controls the system bus (MASTER=0). This signal is active low. |
| 65 | ADSTB16 | O | ADDRESS STROBE for 16-BIT TRANSFERS (channels 5-7). This is an active high signal used to control latching of the upper address byte A9-A16 for 16-bit DMA transfers. Its function is just like ADSTB8. |
| 63 | $\overline{\text{AEN8}}$ | O | ADDRESS ENABLE for 8-BIT DMA TRANSFERS: This signal is the output enable for the 8-bit latch containing upper 8 address bits (A8-A15). It enables A8-A15 system address bus. It is inactive when external bus master controls the system bus (MASTER=0). This signal is active low. |

**82C206 Pin Description** (Continued)

| Pin No. | Name | Type | Function |
|---|---|---|---|
| 33 | $\overline{ACK}$ (MSE) | I | MODULE SELECT ENABLE: When high, it enables the chip select function on one of the modules (DMA Controller, INT Controler, TIMER, RTC, DMA Page register or the Configuration register) for the programming function, i.e. CPU read or write of the command, status or other register of various modules of the 82C206. When low, the 82C206 is essentially disconnected from the system bus. The 82C206 at this time could be performing an active DMA or an interrupt cycle. In a PC/AT compatible design, this pin is tied to $\overline{ACK}$ signal. |
| 11–5<br>13 | A23-A17<br>XA16 | O<br>O | DMA PAGE REGISTER ADDRESS: XA16 and A17–A23 are 3-state output pins. XA16 is the least significant bit of the DMA page register and is used for DMA transfers for 8-bit peripherals only (channel 0–3). XA16 is not used for DMA transfers to 16-bit peripherals (channel 5–7) as XA9–XA16 is provided by demultiplexing the data bus. A17–A23 are the upper 7 bits of the DMA page register. |
| 76–82<br>83, 84<br>1–3<br>4 | IRQ15–IRQ9<br>IRQ7, IRQ6<br>IRQ5–IRQ3<br>IRQ1 | I<br>I | INTERRUPT REQUESTS: Asynchronous inputs. An interrupt request is executed by raising an IRQ input low to high and holding it high until it is acknowledged (edge triggered mode) or just a high level on an IRQ input (level triggered mode). |
| 16 | $\overline{INTA}$ | I | INTERRUPT ACKNOWLEDGE: This pin is used to enable the interrupt controllers interrupt vector data on to the data bus by a sequence of interrupt acknowledge pulses issued by the CPU. |
| 70 | INTR | O | INTERRUPT: This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, and is usually connected to the CPU's interrupt pin. |
| 23 | TMRCLK | I | TIMER CLOCK: Clock input for Counter 0, Counter 1 and Counter 2. |
| 22 | GATE2 | I | GATE 2: Gate input for Counter 2. In a PC/AT compatible design, the Counter 2 is used for tone generation for speaker. In this design, the GATE 2 input is driven by Bit 0 of I/O Port 61H (called TIM2GATE SPK). |
| 20 | OUT1 | O | OUT 1: Output of Timer 1. In a PC/AT compatible design, Timer 1 is programmed as a rate generation to produce 15 μsec period signal used for interrupt request for refresh cycles. |
| 19 | OUT 2 | O | OUT 2: Output of Timer 2. In a PC/AT compatible design, OUT 2 is used to drive the speaker. |

**82C206 Pin Description** (Continued)

| Pin No. | Name | Type | Function |
|---|---|---|---|
| 71 | AS | I | ADDRESS STROBE Address strobe is a positive pulse whose falling edge latches the address from the XD bus |
| 72 | OSCI | I | OSCILLATOR INPUT The time base for the time functions is connected to this pin External square waves of 32 768 KHz may be connected to this input |
| 15 | $\overline{PSRSTB}$ | I | This input is used to establish the condition of the control registers when power is applied to the device. In a PC/AT compatible design, this pin should be tied to the battery back-up circuit.<br><br>When $\overline{PSRSTB}$ and TEST are both low, the following occurs<br><br>(a) Periodic Interrupt Enable (PIE) bit is cleared to zero.<br>(b) Alarm Interrupt Enable (AIE) bit is cleared to zero.<br>(c) Update ended Interrupt Enable (UIE) bit is cleared to zero<br>(d) Update ended Interrupt Flag (UF) bit is cleared to zero.<br>(e) Interrupt Request status Flag (IRQF) is cleared to zero<br>(f) Periodic Interrupt Flag (PF) bit is cleared to zero.<br>(g) The part is not accessible.<br>(h) Alarm interrupt Flag (AF) bit is cleared to zero<br>(i) Square Wave output enable bit is cleared to zero. |
| 14 | PWRGD | I | PWRGOOD: The Power Good pin must be high for bus cycles in which the CPU accesses the RTC When PWRGD is low, all address, data, data strobe and R/W pins are disconnected from the processor. |
| 17 | TEST | I | TEST: Test is an active high input It initializes various internal registers so that the test program starts in a known state. It should be tied low for normal operation. |
| 32, 75 | $V_{CC}$ | — | Power Supply |
| 12, 53, 74 | $V_{SS}$ | — | Ground |

## 82C206—INTEGRATED PERIPHERALS CONTROLLER

The 82C206 is a LSI implementation of the standard peripherals required to implement an IBM PC/AT system board. This device contains the equivalent of two 8237A DMA Controllers, a 74LS612 Mapper, two 8259A Interrupt Controllers, an 8254 Counter/Timer, and a MC146818 Real Time Clock with RAM. The 82C206 provides all of the standard peripherals required for a system board implementation except the keyboard interface controller. Figure 1 illustrates the subsystems contained within the 82C206.

Two DMA Controllers are provided and connected in such a way as to provide the user with four channels of DMA (DMA1) for 8-bit transfers and three channels of DMA (DMA2) for 16-bit transfers (the first 16-bit DMA channel is used for cascading). Included as part of the DMA subsystem is the Page Register (DMAPAGE) device which is used to supplement the DMA and drive the upper address lines when required.

Sixteen channels of interrupt are provided in the 82C206. These channels are partitioned into two cascaded controllers (INTC1,INTC2) with 8 inputs each. Of these 16 channels, three are connected internally to various devices, allowing 13 user definable channels of interrupt. The three internally connected channels are as follows:

Channel 0 — Counter/Timer Counter 0 Interrupt
Channel 2 — Cascade to Slave Interrupt Controller (INTC2)
Channel 8 — Real Time Clock Interrupt

The remaining 13 channels may be defined and utilized as necessary to meet the users specific system requirements.

A Counter/Timer (CTC) subsystem is provided which contains three independent counters. All three counters are driven from a clock input pin which is independent from the other clock inputs to the device. Counter 0 is connected to Interrupt 0 of INTC1. It is intended to be used as a multi-level interrupt to the system for such tasks as time keeping and task switching. Counter 1 may be programmed to generate pulses or square waves for use by external devices. The third channel (Counter 2) is a full function Counter/Timer which has a gate input for controlling the internal counter. This channel can be used as an interval counter, a timer, or as a gated rate/pulse generator.

A Real Time Clock (RTC) is included in the 82C206 for maintaining the time and date. This subsystem also contains 114 bytes of RAM in addition to the Clock/Calendar. The Clock/Calendar information and RAM are kept active by connecting the device to an external battery when system power is turned off.

To interconnect and control all of these major subsystems a top level control section is employed which is divided into subsystems for purposes of discussion.

The first section is the Clock and Wait State Control section. This subsystem controls the generation of DMA wait states and the negation of IOCHRDY (if programmed to do so) during CPU access of the device. The last subsystem is the Top Level Decode.

In order to accommodate over 200 registers in the 82C206 and maintain I/O decode compatibility with the IBM PC/AT, a multilevel decode scheme is employed. The Top Level Decode subsystem performs the function of generating enables to the various subsystems. Control and direction of the XD0-XD7 data bus buffers are also handled by this subsystem.

Each of these subsystems will now be described separately.

### Top Level Decode

The 82C206 Top Level Decode provides 8 separate enables to various subsystems of the device. Figure 2 contains a truth table for the Top Level Decoder. The enabling of the 82C206 XD0-XD7 output buffers is also controlled by this section. The output buffers are enabled whenever an enable is generated to an internal subsystem *and* the $\overline{\text{XIOR}}$ signal is asserted.

| $\overline{ACK}$ | XA9 | XA8 | XA7 | XA6 | XA5 | XA4 | XA3 | XA2 | XA1 | XA0 | ADDRESS RANGE(Hex) | SELECTED DEVICE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | X | 000-00F | DMA1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | X | 020-021 | INTC1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | X | 022-023 | CONFIG |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | X | X | 040-043 | CTC |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 071 | RTC |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | X | X | X | X | 080-08F | DMAPAGE |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | X | 0A0-0A1 | INTC2 |
| 1 | 0 | 0 | 1 | 1 | 0 | X | X | X | X | X | 0C0-0DF | DMA2 |
| 0 | X | X | X | X | X | X | X | X | X | X | DISABLED | |
| X | 1 | X | X | X | X | X | X | X | X | X | DISABLED | |
| X | X | 1 | X | X | X | X | X | X | X | X | DISABLED | |

**Figure 2. 82C206 Internal Decode**

The decoder is enabled by three signals. These three signals are $\overline{ACK}$, XA9 and XA8. To enable any internal device $\overline{ACK}$ must be "1" and both XA9 and XA8 must be "0".

The decode scheme employed in the 82C206 is designed to comply with the IBM PC/AT requirements and is more fully decoded. If the user wishes to take advantage of the areas which are unused by inserting additional peripherals in the I/O map, he may do so since the subsystems in the 82C206 will not respond to the unused address spaces established by the Top Level Decoder. The extra peripherals may be tied directly to the XD0-XD7 data lines since the 82C206 output buffers are not enabled unless an internal subsystem is enabled.

**Clock and Wait State Control**

The Clock and Wait State Control subsystem performs four functions, control of the DMA command width, control of the CPU read or write cycle length, and selection of the DMA clock rate. All of these functions are user selectable by writing to the Configuration Register located at address 023H.

Writing and reading this register is accomplished by first writing a 01H to location 022H to select the 82C206 Configuration Register, and then performing either a read or write to location 023H.

Configuration Register (023H) (Index 01H)

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| RW1 | RW0 | 16W1 | 16W0 | 8W1 | 8W0 | EMR | CLK |

**RW1-RW0**—When the higher speed CPU's are accessing the 82C206, the cycle can be extended by programming up to four wait states into the Configuration Register. This will cause the 82C206 to assert a not ready condition on IOCHRDY (low) whenever a valid decode from the Top Level Decoder is detected and either $\overline{XIOR}$ or $\overline{XIOW}$ is asserted. IOCHRDY will remain low for the number of wait states programmed into the Configuration Register bits 6 and 7.

| RW1 | RW0 | Read/Write Cycle Wait States |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

Wait states are in increments of one SCLK cycle and are not affected by the DMA Clock Divider.

**16W1-16W0**—Wait states can be independently controlled for both 8-bit and 16-bit DMA cycles. This allows the user to tailor the DMA cycle more closely to the application.

| 16W1 | 16W0 | 16-Bit DMA Wait States |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

**8W1-8W0**—Wait states may be inserted in 8-bit DMA cycles by programming these two bits in the Configuration Register.

| 8W1 | 8W0 | 8-Bit DMA Wait States |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

Further control of the cycle length is available through the use of the IOCHRDY pin on the 82C206. During DMA this pin is used as an input to the wait state generation logic to extend the cycle if necessary. This input is driven low (0) by the peripheral to extend the cycle. The cycle can then be completed by releasing IOCHRDY and allowing it to return high (1).

**EMR**—This bit enables the extended $\overline{\text{DMAMEMR}}$ function. Normally the assertion of $\overline{\text{DMAMEMR}}$ is delayed one clock cycle later than $\overline{\text{XIOR}}$ in the IBM PC/AT implementation. This may not be desirable in some systems. A "1" programmed into this bit position will start $\overline{\text{DMAMEMR}}$ at the same time as $\overline{\text{XIOR}}$.

**CLK**—This bit allows the user to insert a divider between the DMA Controller subsystems and the SCLK input pin, or connect the two directly. When this bit position contains a "0", the SCLK input is divided by two and is used to drive both the 8-bit and 16-bit DMA subsystems. A "1" in this position bypasses the divider and uses the SCLK input directly. Whenever the state of this bit is changed, an internal synchronizer controls the actual switching of the clock to prevent a short clock pulse from causing a DMA malfunction.

The Configuration Register contents are preloaded by RESET to an initial value of 0C0 hex. This value establishes a default which is IBM PC/AT compatible and corresponds to:

Read/Write cycles —4 wait states

16-bit DMA transfers —1 wait state

8-bit DMA transfers —1 wait state

$\overline{\text{DMAMEMR}}$ delayed 1 DMA clock cycle later than $\overline{\text{XIOR}}$

DMA clock is equal to SCLK/2

**DMA FUNCTIONAL DESCRIPTION**

The equivalent of two 8237A DMA Controllers is implemented in the 82C206. Each controller is a four channel DMA device which will generate the memory addresses and control signals necessary to transfer information between a peripheral device and memory directly. This allows high speed information transfer with little CPU intervention.

The two DMA Controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1), and three channels for transfers to 16-bit peripherals (DMA2). DMA2 Channel 0 privides the cascade interconnection of the two DMA devices, thereby maintaining IBM PC/AT compatibility.

DMA cycle length control is provided internally in the 82C206 allowing independent control for both 8-bit and 16-bit cycles. This is done through the programmable registers which can extend command signals or insert wait states.

Each DMA Channel has a pair of 16-bit counters and a reload register for each counter. The 16-bit counters allow the DMA to transfer blocks as large as 65536 words. The register associated with each counter allows the channel to reinitialize without reprogramming.

From this point on the description of the DMA subsystem pertains to both DMA1 and DMA2 unless otherwise noted.

**DMA Operation**

During normal operation of the 82C206, the DMA subsystem will be in either the Idle condition, the Program condition or the Active condition. In the Idle condition the DMA controller will be executing cycles consisting of only one state. The idle state SI is the default condition and the DMA will remain in this condition unless the device has been initalized and one of the DMA requests is active or the CPU attempts to access one of the internal registers.

When a DMA request becomes active the device enters the Active condition and issues a hold request to the system. Once in the Active condition the 82C206 will generate the necessary memory addresses and command signals to accomplish a memory-to I/O, I/O-to-memory, or a memory-to-memory transfer. Memory-to-I/O and I/O-to-memory transfers take place in one cycle while memory-to-memory transfers require two cycles. During transfers between memory and I/O, data is presented on the system bus by either memory or the requesting device and the transfer is completed in one cycle. Memory-to-memory transfers however, require the DMA to store data from the read operation in an internal register. The contents of this register is then written to memory on the subsequent cycle.

During transfers between memory and I/O, two commands are activated during the same cycle. In the case of a memory-to-I/O transfer, the 82C206 will assert both $\overline{\text{DMAMEMR}}$ and $\overline{\text{XIOW}}$ allowing data to be transfered directly to the requesting device from memory. Note that 82C206 does not latch data from nor drive data out on this type of cycle.

The number of clock cycles required to transfer a word of data may be varied by programing the DMA or, optionally extended by the peripheral device. During an Active cycle the DMA will sequence through a series of states. Each state will be one DMA clock cycle in length and the number of states in a cycle will vary depending on how the device is programmed and what type of cycle is being performed. The states are labeled S0–S4 and will be explained in detail in the section entitled Active Condition.

**Idle Condition**

When no device is requesting service the DMA is in an Idle condition which maintains the state machine in the SI state. During this time the 82C206 will sample the DREQ input pins every clock cycle. The internal select from the top level decoder and HLDA are also sampled at the same time to determine if the CPU is attempting to access the internal registers. When either of the above two situations occurs, the DMA will exit the Idle condition. Note that the Program condition has priorit over the Active condition since a CPU cycle has already started.

**Program Condition**

The Program condition is entered whenever HLDA is inactive and an internal select is active. The internal select is derived from the top level decode described previously. During this time address lines XA0–XA3 become inputs if DMA1 is selected, or XA1-XA4 become inputs if DMA2 is selected. Note, when DMA2 is selected XA0 is ignored. These address inputs are used to select the DMA controller registers which are to be read or written. Figure 3 lists the register address assignment. Due to the large number of internal registers in the DMA subsystem, an internal flip-flop is used to supplement the addressing of the count and address registers. This bit is used to select between the high and low bytes of these registers. The flip-flop will toggle each time a read or write occurs to any of the word count or address registers in the DMA. This internal flip-flop will be cleared by hardware RESET or a Master Clear command and may be set or cleared by the CPU issuing the appropriate command.

Special commands are supported by the DMA subsystem in the Program condition to control the device. These commands do not make use of the data bus but are derived from a set of addresses, the internal select and $\overline{\text{XIOW}}$ or

| ADDRESS | | OPERATION | | | |
|---|---|---|---|---|---|
| DMA1 | DMA2 | $\overline{XIOR}$ | $\overline{XIOW}$ | Flip-Flop | Register Function |
| 000h | 0C0h | 0 | 1 | 0 | Read Channel 0 Current Address Low Byte |
| | | 0 | 1 | 1 | Read Channel 0 Current Address High Byte |
| | | 1 | 0 | 0 | Write Channel 0 Base and Current Address Low Byte |
| | | 1 | 0 | 1 | Write Channel 0 Base and Current Address High Byte |
| 001h | 0C2h | 0 | 1 | 0 | Read Channel 0 Current Word Count Low Byte |
| | | 0 | 1 | 1 | Read Channel 0 Current Word Count High Byte |
| | | 1 | 0 | 0 | Write Channel 0 Base and Current Word Count Low Byte |
| | | 1 | 0 | 1 | Write Channel 0 Base and Current Word Count High Byte |
| 002h | 0C4h | 0 | 1 | 0 | Read Channel 1 Current Address Low Byte |
| | | 0 | 1 | 1 | Read Channel 1 Current Address High Byte |
| | | 1 | 0 | 0 | Write Channel 1 Base and Current Address Low Byte |
| | | 1 | 0 | 1 | Write Channel 1 Base and Current Address High Byte |
| 003h | 0C6h | 0 | 1 | 0 | Read Channel 1 Current Word Count Low Byte |
| | | 0 | 1 | 1 | Read Channel 1 Current Word Count High Byte |
| | | 1 | 0 | 0 | Write Channel 1 Base and Current Word Count Low Byte |
| | | 1 | 0 | 1 | Write Channel 1 Base and Current Word Count High Byte |
| 004h | 0C8h | 0 | 1 | 0 | Read Channel 2 Current Address Low Byte |
| | | 0 | 1 | 1 | Read Channel 2 Current Address High Byte |
| | | 1 | 0 | 0 | Write Channel 2 Base and Current Address Low Byte |
| | | 1 | 0 | 1 | Write Channel 2 Base and Current Address High Byte |
| 005h | 0CAh | 0 | 1 | 0 | Read Channel 2 Current Word Count Low Byte |
| | | 0 | 1 | 1 | Read Channel 2 Current Word Count High Byte |
| | | 1 | 0 | 0 | Write Channel 2 Base and Current Word Count Low Byte |
| | | 1 | 0 | 1 | Write Channel 2 Base and Current Word Count High Byte |
| 006h | 0CCh | 0 | 1 | 0 | Read Channel 3 Current Address Low Byte |
| | | 0 | 1 | 1 | Read Channel 3 Current Address High Byte |
| | | 1 | 0 | 0 | Write Channel 3 Base and Current Address Low Byte |
| | | 1 | 0 | 1 | Write Channel 3 Base and Current Address High Byte |
| 007h | 0CEh | 0 | 1 | 0 | Read Channel 3 Current Word Count Low Byte |
| | | 0 | 1 | 1 | Read Channel 3 Current Word Count High Byte |
| | | 1 | 0 | 0 | Write Channel 3 Base and Current Word Count Low Byte |
| | | 1 | 0 | 1 | Write Channel 3 Base and Current Word Count High Byte |
| 008h | 0D0h | 0 | 1 | X | Read Status Register |
| | | 1 | 0 | X | Write Command Register |
| 009h | 0D2h | 0 | 1 | X | Read DMA Request Register |
| | | 1 | 0 | X | Write DMA Request Register |
| 00Ah | 0D4h | 0 | 1 | X | Read Command Register |
| | | 1 | 0 | X | Write Single Bit DMA Request Mask Register |
| 00Bh | 0D6h | 0 | 1 | X | Read Mode Register |
| | | 1 | 0 | | Write Mode Register |
| 00Ch | 0D8h | 0 | 1 | X | Set Byte Pointer Flip-Flop |
| | | 1 | 0 | X | Clear Byte Pointer Flip-Flop |
| 00Dh | 0DAh | 0 | 1 | X | Read Temporary Register |
| | | 1 | 0 | X | Master Clear |
| 00Eh | 0DCh | 0 | 1 | X | Clear Mode Register Counter |
| | | 1 | 0 | X | Clear All DMA Request Mask Register Bits |
| 00Fh | 0DEh | 0 | 1 | X | Read All DMA Request Mask Register Bits |
| | | 1 | 0 | X | Write All DMA Request Mask Register Bits |

**Figure 3. DMA Registers**

$\overline{XIOR}$. These commands are Master Clear Clear Mask Register, Clear Mode Register Counter, Set and Clear Byte Pointer Flip-Flop.

The 82C206 will enable programming whenever HLDA has been inactive for one DMA clock cycle. It is the responsibility of the system to ensure that programming and HLDA are mutually exclusive. Erratic operation of the 82C206 can occur if a request for service occurs on an unmasked channel which is being programmed. The channel should be masked or the DMA disabled to prevent the 82C206 from attempting to service a device with a channel which is partially programmed.

**Active Condition**

The 82C206 DMA subsystem enters the Active condition whenever a software request occurs or a DMA request on an unmasked channel occurs and the device is not in the Program condition. The 82C206 will then begin a DMA transfer cycle.

In a read cycle for example, after receiving a DREQ, the 82C206 will issue a HRQ to the system. Until a HLDA is returned the DMA will remain in an idle condition. On the next clock cycle the DMA will exit Idle and enter state S0. During S0 the device will resolve priority and issue DACK on the highest priority channel requesting service. The DMA will then proceed to state S1 where the multiplexed addresses are output and latched. State S2 is then entered, at which time the 82C206 will assert $\overline{DMAMEMR}$. The device then transitions into S3 where the $\overline{XIOW}$ command is asserted. The 82C206 DMA will then remain in S3 until the Wait State Counter has decremented to zero and IOCHRDY is true. Note that at least one additional S3 will occur unless Compressed Timing is selected. Once a ready condition is detected, the DMA will enter S4 where both commands are deasserted. In Burst Mode and Demand Mode (discussed below), subsequent cycles will begin in S2 unless the intermediate addresses require updating. In these subsequent cycles the lower addresses are changed in S2.

The DMA can be programmed on a channel by channel basis to operate in one of four modes. The four modes are listed below.

**Single Transfer Mode**—This mode directs the DMA to execute only one transfer cycle at a time. DREQ must be held active until DACK becomes active. If DREQ is held active throughout the cycle, the 82C206 will deassert HRQ and release the bus once the transfer is complete. After HLDA has gone inactive the 82C206 will again assert HRQ and execute another cycle on the same channel unless a request from a higher priority channel has been received. In this mode the CPU is ensured of being allowed to execute at least one bus cycle between transfers.

Following each transfer the word count is decremented and the address is incremented or decremented. When the word count decrements from 0000h to FFFFh the terminal count bit in the status register is set and a T/C pulse is generated. If the autoinitialization option has been enabled, the channel will reinitialize itself. If Autoinitialize is not selected the DMA will set the DMA request bit mask and suspend transfering on that channel.

**Block Transfer Mode**—When Block Transfer Mode is selected, the 82C206 will begin transfers in response to either a DREQ or a software request and will continue until a terminal count (FFFFh) is reached, at which time T/C is pulsed and the status register terminal count bit is set. In this mode DREQ need only be held active until DACK is asserted. Autoinitialization is optional in this mode also.

**Demand Transfer Mode**—In Demand Transfer mode the DMA will begin transfers in response to the assertion of DREQ and will continue until either terminal count is reached or DREQ becomes inactive. This mode is normally used for peripherals which have limited buffering ability. The peripheral can initiate a transfer and continue until its buffer capacity is exhausted. The peripheral may then re-establish service by again asserting DREQ. During idle periods between transfers the CPU is released to operate and can monitor the operation by reading intermediate values from the address and word count regis-

ters. Once DREQ has been deasserted, higher priority channels are allowed to intervene. Reaching terminal count will result in the generation of a T/C pulse, the setting of the terminal count bit in the status register and autoinitialization (if enabled).

**Cascade Mode**—This mode is used to interconnect more than one DMA controller, to extend the number of DMA channels while preserving the priority chain. In Cascade mode the master DMA controller does not generate address or control signals. The DREQ and DACK signals of the master are used to interface the HRQ and HLDA signals of the slave DMA devices. Once the master has received a HLDA from the CPU in response to a DREQ caused by the HRQ from a slave DMA controller, the master DMA controller will ignore all inputs except HLDA from the CPU and DREQ on the active channel. This prevents conflicts between the DMA devices.

Figure 4 shows the cascade interconnection for two levels of DMA devices. Note that Channel 0 of DMA2 is internally connected for Cascade mode to DMA1. Additional devices can be cascaded to the available channels in either DMA1 or DMA2 since cascade is not limited to two levels of DMA controllers.

When programming cascaded controllers, begin with the device which is actually generating HRQ to the system (first level device) and then proceed to the second level devices. RESET causes the DACK outputs to become active low and are placed in the inactive state. To allow the internal cascade between DMA1 and DMA2 to function correctly, the active low state of DACK should not be modified. This is because the 82C206 has an inverter between DACK0 of DMA2 and HLDA of DMA1. The first level device's DMA request mask bits will prevent second level cascaded devices from generating unwanted hold requests during the initialization process.

**DMA Transfers**

Four types of transfer modes are provided in the 82C206 DMA subsystem. These transfer types are:

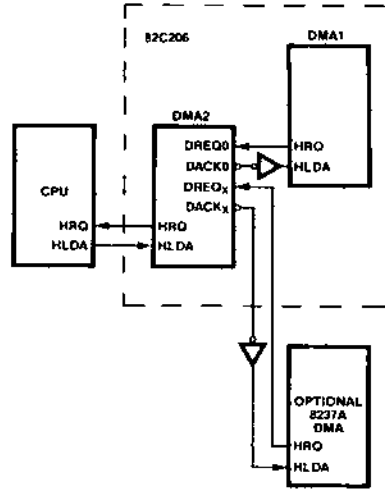



**Figure 4. Cascade Mode Interconnect**

**Read Transfer**—Read transfers move data from memory to an I/O device, by generating the memory address and asserting $\overline{\text{DMAMEMR}}$ and $\overline{\text{XIOW}}$ during the same cycle.

**Write Transfer**—Write transfers move data from an I/O device to memory by generating the memory address and asserting $\overline{\text{XIOR}}$ and $\overline{\text{DMAMEMW}}$.

**Memory-to-Memory Transfer**—The memory-to-memory transfer is used to move a block of memory from one location in memory to another. DMA channels 0 and 1 may be programmed to operate as memory-to-memory channels by setting a bit in the Command Register. Once programmed to perform a memory-to-memory transfer the process can be started by generating either a software or an external request to channel 0. Once the transfer is initiated, Channel 0 provides the address for the source block during the memory read portion of the cycle. Channel 1 generates the address for the memory write cycle. During the read cycle, a byte of data is

latched in the internal Temporary Register of the 82C206. The contents of this register are then output on the XD0-7 data lines during the write portion of the cycle and subsequently written to memory. Channel 0 may be programmed to maintain the same source address on every cycle. This allows the CPU to initalize large blocks of memory with the same value. The 82C206 will continue performing transfer cycles until Channel 1 reaches terminal count.

**Verify Transfer**—The verify transfer is a pseudo-transfer which is useful for diagnostics. In this type of transfer the DMA will operate as if it is performing a Read or Write Transfer by generating HRQ, addresses and DACK but will do so without asserting a command signal. Since no transfer actually takes place IOCHRDY is ignored during Verify transfer cycles.

**Autoinitialization**

Each of the four DMA channel Mode Registers contains a bit which will cause the channel to reinitialize after reaching terminal count. During this process, referred to as Autoinitialization, the Base Address and Base Word Count Registers, which were originally written by the CPU, are reloaded into the Current Address and Current Word Count Registers (both the base and current registers are loaded during a CPU write cycle). The base registers remain unchanged during DMA Active cycles and can only be changed by the CPU. If the channel has been programmed to autoinitialize, the request mask bit will not be set upon reaching terminal count. This allows the DMA to continue operation without CPU intervention.

During memory-to-memory transfers the Word Count Registers of both Channel 0 and Channel 1 must be programmed with the same starting value for full autoinitialization. If Channel 0 reaches terminal count before Channel 1, then Channel 0 will reload the starting address and word count and continue transferring data from the beginning of the source block. Should Channel 1 reach terminal count first, it will reload the current registers and Channel 0 will remain uninitialized.

**DREQ Priority**

The 82C206 supports two schemes for establishing DREQ priority. The first is fixed priority which assigns priority based on channel position. In this method Channel 0 is assigned the highest priority. Priority assignment then progresses downward through the channels in order with Channel 3 receiving the lowest priority.

The second type of priority assignment is rotating priority. In this scheme the ordering of priority from Channel 0 to Channel 3 is maintained but the actual assignment of priority changes. The channel most recently serviced will be assigned the lowest priority and, since the order of priority assignment remains fixed, the remaining three channels rotate accordingly. The rotating priority assignment is illustrated in Figure 5.

In instances where multiple requests occur at the same time the 82C206 will issue a HRQ but will not freeze the priority logic until HLDA is returned. Once HDLA becomes active the priority logic is frozen and DACK is asserted on the highest requesting channel. Priority will not be re-evaluated until HLDA has been deactivated.

**Address Generation**

Eight intermediate bits of the address are multiplexed onto the data lines during Active cycles of the DMA. This reduces the number of pins required by the DMA subsystem. During state S1, the intermediate addresses are output on data lines XD0-XD7. These addresses should be externally latched and used to drive the system address bus. Since DMA1 is used to transfer 8-bit data and DMA2 is used to transfer 16-bit data, a one bit skew occurs in the intermediate address fields. DMA1 will therefore output addresses A8-A15 on the data bus at this time whereas DMA2 will output A9-A16. A separate set of latch and enable signals are provided for both DMA1 and DMA2 to accommodate the address skew.

During 8-bit DMA cycles, in which DMA1 is active, the 82C206 will output the lower 8-bits

| First Arbitration | Second Arbitration | Third Arbitration | Priority |
|---|---|---|---|
| Channel 0 | [Channel 2] – Cycle Grant | [Channel 3] – Cycle Grant | Highest |
| [Channel 1] – Cycle Grant | [Channel 3] | Channel 0 | |
| Channel 2 | Channel 0 | Channel 1 | |
| Channel 3 | Channel 1 | Channel 2 | Lowest |

[Channel X] = Requested Channel

**Figure 5. Rotating Priority Scheme**

of address on XA0-XA7. The intermediate 8-bits of address will be output on XD0-XD7 and ADSTB8 will be asserted for one DMA clock cycle. The falling edge of ADSTB8 is used to latch the intermediate addresses A8-A15. An enable signal, AEN8, is used to control the output drivers of the external latch. A16-A23 are also generated at this time from a DMA Page Register in the 82C206. Note that A16 is output on the XA16 pin of the device.

16-bit DMA cycles from DMA2 require the 82C206 to output the lower 8-bits of the address on XA1-XA8. The intermediate addresses A9-A16 are output on XD0-XD7. Control for a separate latch is provided by signals ADSTB16 and AEN16. The DMA Page Register now generates A17-A23. During 16-bit DMA transfers XA0 and XA16 remain inactive.

The DMA Page Register is a set of 16 8-bit registers in the 82C206 which are used to generate the high order addresses during DMA cycles. Only 8 of the registers are actually used but all 16 were included to maintain IBM PC/AT compatibility. Each DMA channel has a register associated with it with the exception of Channel 0 of DMA2 which is used for internal cascading to DMA1. Assignment of each of these registers is shown in Figure 6 along with its Read/Write address.

| Address | Register Function |
|---|---|
| 080h | Unused |
| 081h | 8-bit DMA Channel 2 (DACK2) |
| 082h | 8-bit DMA Channel 3 (DACK3) |
| 083h | 8-bit DMA Channel 1 (DACK1) |
| 084h | Unused |
| 085h | Unused |
| 086h | Unused |
| 087h | 8-bit DMA Channel 0 (DACK0) |
| 088h | Unused |
| 089h | 16-bit DMA Channel 2 (DACK6) |
| 08Ah | 16-bit DMA Channel 3 (DACK7) |
| 08Bh | 16-bit DMA Channel 1 (DACK5) |
| 08Ch | Unused |
| 08Dh | Unused |
| 08Eh | Unused |
| 08Fh | Refresh Cycle |

**Figure 6.**
**DMA Address Extension Register Map**

During Demand and Block Transfers, the 82C206 generates multiple sequential transfers. For most of these transfers the informa-

tion in the external address latches will remain the same, eliminating the need to be relatched. Since the need to update the latches occurs only when a carry or borrow from the lower 8-bits of the Address Counter exists, the 82C206 will only update the latch contents when necessary. The 82C206 will therefore, only execute S1 cycles when necessary, resulting in an overall through-put improvement.

**Compressed Timing**

The DMA subsystem in the 82C206 can be programmed to transfer a word in as few as 3 DMA clock cycles. The normal DMA cycle consists of three states: S2, S3, and S4 (this assumes Demand or Block Transfer Mode). Normal transfers require 4 DMA clock cycles since S3 is executed twice due to the 1 wait state insertion. In systems capable of supporting higher through-put, the 82C206 can be programmed to omit one S3 and assert both commands in S2. S2 begins the cycle by generating the address and asserting both commands. One S3 cycle is executed and the cycle terminates in S4. If Compressed Timing is selected, T/C will be output in S2 and S1 cycles will be executed as necessary to update the address latch. Note that Compressed Timing is not allowed for memory-to-memory transfers.

**Register Description**

**Current Address Register**

Each DMA channel has a 16-bit Current Address Register which holds the address used during transfers. Each channel can be programmed to increment or decrement this register whenever a transfer is completed. This register can be read or written by the CPU in consecutive 8-bit bytes. If Autoinitialization is selected, this register will be reloaded from the Base Address Register upon reaching terminal count in the Current Word Count Register. Channel 0 can be prevented from incrementing or decrementing by setting the Address Hold Bit in the Command Register.

**Current Word Count Register**

Each channel has a Current Word Count Register which determines the number of transfers to perform. The actual number of transfers performed will be one greater than the value programmed into the register. The register is decremented after each transfer until it goes from zero to FFFFh. When this roll-over occurs the 82C206 will generate T/C and either suspend operation on that channel and set the appropriate Request Mask Bit or Autoinitialize and continue.

**Base Address Register**

Associated with each Current Address Register is a Base Address Register. This is a write only register which is loaded by the CPU when writing to the Current Address Register. The purpose of this register is to store the initial value of the Current Address Register for Autoinitialization. The contents of this register are loaded into the Current Address Register whenever terminal count is reached and the Autoinitialize Bit is set.

**Base Word Count Register**

This register preserves the initial value of the Current Word Count Register. It is also a write only register which is loaded by writing to the Current Word Count Register. This register is loaded into the Current Word Count Register during Autoinitialization.

**Command Register**

This register controls the overall operation of a DMA subsystem. The register can be read or written by the CPU and is cleared by either RESET or a Master Clear command.

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| DAK | DRQ | EW | RP | CT | CD | AH | M-M |

**DAK**—DACK active level is determined by bit 7. Programming a 1 in this bit position makes DACK an active high signal.

**DRQ**—DREQ active level is determined by bit 6. Writing a 1 in this bit position causes DREQ to become active low.

**EW**—Extended Write is enabled by writing a 1 to bit 5, causing the write commands to be asserted one DMA cycle earlier during a transfer. The read and write commands both begin in state S2 when enabled.

**RP**—Writing a 1 to bit 4 causes the 82C206 to utilize a rotating priority scheme for honoring DMA requests. The default condition is fixed priority.

**CT**—Compressed timing is enabled by writing a 1 to bit 3 of this register. The default 0 condition causes the DMA to operate with normal timing.

**CD**—Bit 2 is the master disable for the DMA controller. Writing a 1 to this location disables the DMA subsystem (DMA1 or DMA2). This function is normally used whenever the CPU needs to reprogram one of the channels to prevent DMA cycles from occuring.

**AH**—Writing a 1 to bit 1 enables the address hold feature in Channel 0 when performing memory-to-memory transfers.

**M-M**—A 1 in the bit 0 position enables Channel 0 and Channel 1 to be used for memory-to-memory transfers.

**Mode Register**

Each DMA channel has a Mode Register associated with it. All four Mode Registers reside at the same I/O address. Bits 0 and 1 of the Write Mode Register command determine which channel's Mode Register gets written. The remaining six bits control the mode of the selected channel. Each channel's Mode Register can be read by sequentially reading the Mode Register location. A Clear Mode Register Counter command is provided to allow the CPU to restart the mode read process at a known point. During mode read operations, bits 0 and 1 will both be 1.

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| M1 | M0 | DEC | AI | TT1 | TT0 | CS1 | CS0 |

(Read/Write Register)

**M1-M0**—Mode selection for each channel is accomplished by bits 6 and 7.

| M1 | M0 | MODE |
|---|---|---|
| 0 | 0 | Demand Mode |
| 0 | 1 | Single Cycle Mode |
| 1 | 0 | Block Mode |
| 1 | 1 | Cascade Mode |

**DEC**—Determines direction of the address counter. A one in bit 5 decrements the address after each transfer.

**AI**—The Autoinitialization function is enabled by writing a 1 in bit 4 of the Mode Register.

**TT1-TT0**—Bits 2 and 3 control the type of transfer which is to be performed.

| TT1 | TT0 | TYPE |
|---|---|---|
| 0 | 0 | Verify Transfer |
| 0 | 1 | Write Transfer |
| 1 | 0 | Read Transfer |
| 1 | 1 | Illegal |

**CS1-CS0**—Channel Select bits 1 and 0 determine which channel's Mode Register will be written. Read back of a mode register will result in bits 1 and 0 both being ones.

| CS1 | CS0 | CHANNEL |
|---|---|---|
| 0 | 0 | Channel 0 select |
| 0 | 1 | Channel 1 select |
| 1 | 0 | Channel 2 select |
| 1 | 1 | Channel 3 select |

**Request Register**

This is a four bit register used to generate software requests (DMA service can be requested either externally or under software control). Request Register bits can be set or

reset independently by the CPU. The Request Mask has no effect on software generated requests. All four bits are read in one operation and appear in the lower four bits of the byte. Bits 4 through 7 are read as ones. All four request bits are cleared to zero by RESET.

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| X | X | X | X | X | RB | RS1 | RS0 |

(Write Operation)

**RB**—The request bit is set by writing a 1 to bit 2. RS1-RS0 select which bit (channel) is to be manipulated.

**RS1-RS0**—Channel Select 0 and 1 determine which channel's Mode Register will be written. Read back of the mode register will result in bits 0 and 1 both being ones.

| RS1 | RS0 | CHANNEL |
|---|---|---|
| 0 | 0 | Channel 0 select |
| 0 | 1 | Channel 1 select |
| 1 | 0 | Channel 2 select |
| 1 | 1 | Channel 3 select |

Format for the Request Register read operation is shown below.

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| 1 | 1 | 1 | 1 | RC3 | RC2 | RC1 | RC0 |

(Read Operation)

**RC3-RC0**—During a Request Register read, the state of the request bit associated with each channel is returned in bits 0 through 3 of the byte. The bit position corresponds to the channel number.

**Request Mask Register**

The Request mask register is a set of four bits which are used to inhibit external DMA requests from generating transfer cycles. This register can be programmed in two ways. Each channel can be independently masked by writing to the Write Single Mask Bit location. The data format for this operation is shown below.

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| X | X | X | X | X | MB | MS1 | MS0 |

(Set/Reset Operation)

**MB**—Bit 2 sets or resets the request mask bit for the channel selected by MS1 and MS0. Writing a 1 in this bit position sets the mask, inhibiting external requests

**MS1-MS0**—These two bits select the specific mask bit which is to be set or reset.

| MS1 | MS0 | CHANNEL |
|---|---|---|
| 0 | 0 | Channel 0 select |
| 0 | 1 | Channel 1 select |
| 1 | 0 | Channel 2 select |
| 1 | 1 | Channel 3 select |

Alternatively all four mask bits can be programmed in one operation by writing to the Write All Mask Bits address. Data format for this and the Read All Mask Bits function is shown below.

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| X | X | X | X | MB3 | MB2 | MB1 | MB0 |

(Read/Write Operation)

**MB3-MB0**—Each bit position in the field represents the mask bit of a channel. The mask bit number corresponds to the channel number associated with the mask bit

All four mask bits are set following a RESET or a Master Clear command. Individual channel mask bits will be set as a result of terminal count being reached, if Autoinitialize is disabled. The entire register can be cleared,

enabling all four channels, by performing a Clear Mask Register operation.

**Status Register**

The status of all four channels can be determined by reading the Status Register. Information is available to determine if a channel has reached terminal count and whether an external service request is pending. Bits 0-3 of this register are cleared by RESET, Master Clear or each time a Status Read takes place. Bits 4-7 are cleared by RESET, Master Clear or the pending request being deasserted. Bits 4-7 are not affected by the state of the Mask Register Bits. The channel number corresponds to the bit position.

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| DRQ3 | DRQ2 | DRQ1 | DRQ0 | TC3 | TC2 | TC1 | TC0 |

(Read Only Register)

**Temporary Register**

The Temporary Register is used as a temporary holding register for data during memory-to-memory transfers. The register is loaded during the first cycle of a memory-to-memory transfer from XD0-XD7. During the second cycle of the transfer, the data in the Temporary Register is output on the XD0-XD7 pins. Data from the last memory-to-memory transfer will remain in the register unless a RESET or Master Clear occurs.

**Special Commands**

Five Special Commands are provided to make the task of programming the device easier. These commands are activated as a result of a specific address and assertion of either a $\overline{XIOR}$ or $\overline{XIOW}$. Information on the data lines is ignored by the 82C206 whenever an $\overline{XIOW}$ activated command is issued, thus data returned on $\overline{XIOR}$ activated commands is invalid.

**Clear Byte Pointer Flip-Flop**—This command is normally executed prior to reading or writing to the address or word count registers. This initializes the flip-flop to point to the low byte of the register and allows the CPU to read or write the register bytes in correct sequence.

**Set Byte Pointer Flip-Flop**—Setting the Byte Pointer Flip-Flop allows the CPU to adjust the pointer to the high byte of an address or word count register.

**Master Clear**—This command has the same effect as a hardware RESET. The Command Register, Status Register, Request Register, Temporary Register, Mode Register Counter and Byte Pointer Flip-Flop are cleared and the Request Mask Register is set. Immediately following Master Clear or RESET, the DMA will be in the Idle Condition.

**Clear Request Mask Register**—This command enables all four DMA channels to accept requests by clearing the mask bits in the register.

**Clear Mode Register Counter**—In order to allow access to four Mode Registers while only using one address, an additional counter is used. After clearing the counter all four Mode Registers may be read by doing successive reads to the Read Mode Register address. The order in which the registers will be read is Channel 0 first, Channel 3 last.

## INTERRUPT CONTROLLER FUNCTIONAL DESCRIPTION

The programmable interrupt controllers in the 82C206 function as a system wide interrupt manager in an iAPX86 system. They accept requests from peripherals, resolve priority on pending interrupts and interrupts in service, issue an interrupt request to the CPU, and provide a vector which is used as an index by the CPU to determine which interrupt service routine to execute.

A variety of priority assignment modes are provided,which can be reconfigured at any time during system operation, allowing the complete interrupt subsystem to be restructured, based on the system environment.

### Overview

Two interrupt controllers, INTC1 and INTC2, are included in the 82C206. Each of the interrupt controllers is equivalent to an 8259A device operating in iAPX86 Mode. The two devices are interconnected and must be programmed to operate in Cascade Mode (see Figure 7) for proper operation of all 16 interrupt channels. INTC1 is located at addresses 020H-021H and is configured for Master operation (defined below) in Cascade Mode. INTC2 is a Slave device (defined below) and is located at 0A0H-0A1H. The Interrupt Request output signal from INTC2 (INT) is internally connected to the interrupt request input Channel 2 (IR2) of INTC1. The address decoding and Cascade interconnection matches that of the IBM PC/AT.

Two additional interconnections are made to the interrupt request inputs of the interrupt controllers. The output of Timer 0 in the Counter/Timer subsystem is connected to Channel 0 (IR0) of INTC1. Interrupt request from the Real Time Clock is connected to Channel 0 (IR0) of INTC2. Figure 8 lists the 16 interrupt channels and their interrupt request source.

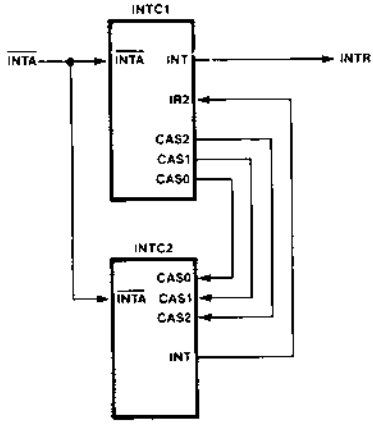



**Figure 7. Internal Cascade Interconnect**

Description of the Interrupt Subsystem will pertain to both INTC1 and INTC2 unless otherwise noted. Wherever register addresses are used, the address for the INTC1 register will be listed first and the address for the INTC2 register will follow in parenthesis. Example 020H (0A0H)

### Controller Operation

Figure 9 is a block diagram of the major elements in the interrupt controller. The Interrupt Request Register (IRR) is used to store requests from all of the channels which are requesting service. Interrupt Request Register bits are labeled using the Channel Name IR7-IR0. The In-Service Register (ISR) contains all the channels which are currently being serviced (more than one channel can be in service at a time). In-Service Register bits are labeled IS7-IS0 and correspond to IR7-IR0. The Interrupt Mask Register (IMR) allows the CPU to disable any or all of the interrupt channels. The Priority Resolver evaluates inputs from the above three registers, issues an interrupt request, and latches the corresponding bit into the In-Service Register. During interrupt acknowledge cycles, a master controller outputs a code to the slave device which is compared in the Cascade Buffer/Comparator with a three bit ID code previously written. If a match occurs in the slave controller, it will generate an interrupt vector. The contents of the Vector Register are used to provide the CPU with an interrupt vector during Interrupt Acknowledge (INTA) cycles.

### Interrupt Sequence

The 82C206 allows the CPU to perform an indirect jump to a service routine in response to a request for service from a peripheral device. The indirect jump is based on a vector which is provided by the 82C206 on the second of two CPU generated INTA cycles (the first INTA cycle is used for resolving priority and the second cycle is for transferring the vector to the CPU). The events which occur during an interrupt sequence are as follows:

1—One or more of the interrupt requests

| Controller Number | Channel Name | Interrupt Request Source |
|---|---|---|
| INTC1 | IR0 | Counter/Timer Out0 |
| INTC1 | IR1 | IRQ1 Input Pin |
| INTC1 | IR2 | INTC2 Cascade Interrupt |
| INTC1 | IR3 | IRQ3 Input Pin |
| INTC1 | IR4 | IRQ4 Input Pin |
| INTC1 | IR5 | IRQ5 Input Pin |
| INTC1 | IR6 | IRQ6 Input Pin |
| INTC1 | IR7 | IRQ7 Input Pin |
| INTC2 | IR0 | Real Time Clock IRQ |
| INTC2 | IR1 | IRQ9 Input Pin |
| INTC2 | IR2 | IRQ10 Input Pin |
| INTC2 | IR3 | IRQ11 Input Pin |
| INTC2 | IR4 | IRQ12 Input Pin |
| INTC2 | IR5 | IRQ13 Input Pin |
| INTC2 | IR6 | IRQ14 Input Pin |
| INTC2 | IR7 | IRQ15 Input Pin |

**Figure 8. Interrupt Request Source**

(IR7-IR0) becomes active, setting the corresponding IRR bit(s).

2—The interrupt controller resolves priority based on the state of the IRR, IMR and ISR and asserts the INTR output if appropriate.

3—The CPU accepts the interrupt and responds with an INTA cycle.

4—During the first INTA cycle, the highest priority ISR bit is set and the corresponding IRR bit is reset. The internal Cascade address is generated and the XD7-XD0 outputs remain tri-stated.

5—The CPU will execute a second INTA cycle, during which the 82C206 will drive an 8-bit vector onto the data pins XD7-XD0, which is in turn latched by the CPU. The format of this vector is shown in Figure 12. Note that V7-V3 in Figure 12 are programmable by writing to Ininialization Control Word 2 (see Initialization Command Words section below).

6—At the end of the second INTA cycle, the ISR bit will be cleared if the Automatic End Of Interrupt mode is selected (see End Of Interrupt section below). Otherwise, the ISR bit must be cleared by an End Of Interrupt (EOI) command from the CPU at the end of the interrupt service routine.

If no interrupt request is present at the beginning of the first INTA cycle (i.e., a spurious interrupt) INTC1 will issue an interrupt level 7 vector during the second INTA cycle.

**End Of Interrupt**

EOI is defined as the condition which causes an ISR bit to be reset. Determination of which ISR bit is to be reset can be done by a CPU command (specific EOI) or, the Priority Resolver can be instructed to clear the highest priority ISR bit (non-specific EOI).

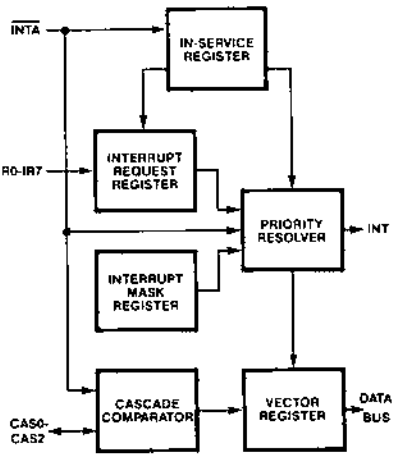



**Figure 9. Interrupt Controller Block Diagram**

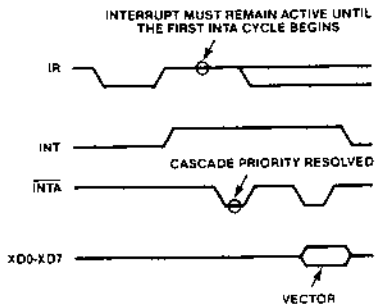



**Figure 10. Interrupt Sequence**

The 82C206 can determine the correct ISR bit to reset when operated in modes which do not alter the fully nested structure, since the current highest priority ISR bit is necessarily the last level acknowledged and serviced. In conditions where the fully nested structure is not preserved, a specific EOI must be generated at the end of the interrupt service routine. An ISR bit that is masked, in Special Mask Mode by a IMR bit, will not be cleared by a non-specific EOI command. The interrupt controller can optionally generate an Automatic End Of Interrupt (AEOI) on the trailing edge of the second INTA cycle.

**Priority Assignment**

Assignment of priority is based on an interrupt channel's position relative to the other channels in the interrupt controller. After the initialization sequence, IR0 has the highest priority, IR7 has the lowest, and priority assignment is fixed (Fixed Priority Mode). Priority assignment can be rotated either manually (Specific Rotation Mode) or automatically (Automatic Rotation Mode) by programming Operational Command Word 2 (OCW2).

**Fixed Priority Mode**—This is the default condition which exists unless rotation (either manual or automatic) is enabled, or the controller is programmed for Polled Mode. In Fixed Priority Mode, interrupts are fully nested with priority assigned as shown:

| | Lowest | | | | | | | Highest |
|---|---|---|---|---|---|---|---|---|
| Priority Status | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Nesting allows interrupts of a higher priority to generate interrupt requests prior to the completion of the interrupt in service. When an interrupt is acknowledged, priority is resolved, the highest priority request's vector is placed on the bus and the ISR bit for that channel is set. This bit remains set until an EOI (automatic or CPU generated) is issued to that channel. While the ISR bit is set, all interrupts of equal or lower priority are inhibited. Note that a higher priority interrupt which occurs during an interrupt service routine, will only be acknowledged if the CPU has internally re-enabled interrupts.

**Specific Rotation Mode**—Specific Rotation allows the system software to re-assign priority levels by issuing a command which redefines the highest priority channel.

**Before Rotation**

| | Lowest | | | | | | | Highest |
|---|---|---|---|---|---|---|---|---|
| Priority Status | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

(Specific Rotation command issued with Channel 5 specified)

**After Rotation**

| | Lowest | | | | | | | Highest |
|---|---|---|---|---|---|---|---|---|
| Priority Status | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 |

**Automatic Rotation Mode**—In applications where a number of equal priority peripherals are requesting interrupts, Automatic Rotation may be used to equalize the priority assignment. In this mode a peripheral, after being serviced, is assigned the lowest priority. All peripherals connected to the controller will be serviced at least once in 8 interrupt requests to the CPU from the controller. Automatic rotation will occur,if enabled, due to the occurrance of EOI (automatic or CPU generated).

**Before Rotation** (IR4 is highest priority request being serviced)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| ISR Status Bit | IS7 | IS6 | IS5 | IS4 | IS3 | IS2 | IS1 | IS0 |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| | Lowest | | | | | | | Highest |
| Priority Status | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**After Rotation** (IR4 service completed)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| ISR Status Bit | IS7 | IS6 | IS5 | IS4 | IS3 | IS2 | IS1 | IS0 |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Lowest | | | | | | | Highest |
| Priority Status | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 |

**Programming The Interrupt Controller**

Two types of commands are used to control the 82C206 interrupt controllers, Initialization Command Words (ICWs) and Operational Command Words (OCWs).

**Initialization Command Words**

The initialization process consists of writing a sequence of 4 bytes to each interrupt controller. The initialization sequence is started by writing the first Initialization Command Word (ICW1) to address 020H (0A0H) with a 1 on bit 4 of the data byte. The interrupt controller interprets this as the start of an initialization sequence and does the following:

1—The Initialization Command Word Counter is reset to zero.
2—ICW1 is latched into the device
3—Fixed Priority Mode is selected
4—IR7 is assigned the highest priority
5—The Interrupt Mask Register is cleared
6—The Slave Mode Address is set to 7
7—Special Mask Mode is disabled
8—The IRR is selected for Status Read operations

The next three I/O writes to address 021H (0A1H) will load ICW2-ICW4. See Figure 11 for a flow chart of the initialization sequence. The initialization sequence can be terminated

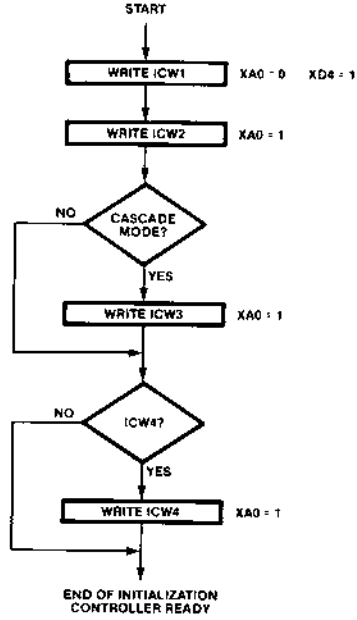



**Figure 11. Initialization Sequence**

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| IR7 | V7 | V6 | V5 | V4 | V3 | 1 | 1 | 1 |
| IR7 | V7 | V6 | V5 | V4 | V3 | 1 | 1 | 0 |
| IR7 | V7 | V6 | V5 | V4 | V3 | 1 | 0 | 1 |
| IR7 | V7 | V6 | V5 | V4 | V3 | 0 | 1 | 1 |
| IR7 | V7 | V6 | V5 | V4 | V3 | 0 | 1 | 0 |
| IR7 | V7 | V6 | V5 | V4 | V3 | 0 | 0 | 1 |
| IR7 | V7 | V6 | V5 | V4 | V3 | 0 | 0 | 0 |

**Figure 12. Interrupt Vector Byte**

at any point (all 4 bytes must be written for the controller to be properly initialized) by writing to address 020H (0A0H) with a 0 in data bit 4. Note, this will cause OCW2 or OCW3 to be written.

**ICW1**—Address 020H (0A0H)

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| X | X | X | SI | LTM | X | SM | X |

(Write Only Register)

**SI**—Bit 4 indicates to the interrupt controller that an Initialization Sequence is starting and must be a 1 to write ICW1.

**LTM**—Bit 3 selects level or edge triggered inputs to the IRR. If a 1 is written to LTM, a 'high' level on the IRR input will generate an interrupt request. The IR must be active until the first INTA cycle is started to generate the proper interrupt vector (an IR7 vector will be generated if the IRR input is deasserted early) and the IR must be removed prior to EOI to prevent a second interrupt from occuring.

**SM**—Bit 1 selects between Single Mode and Cascade Mode. Single Mode is used whenever only one interrupt controller (INTC1) is used and is not recommended for this device. Cascade Mode allows the two interrupt controllers to be connected through IR2 of INTC1. INTC1 will allow INTC2 to generate its own interrupt vectors if Cascade Mode is selected and the highest priority IR pending is from an INTC2 input. INTC1 and INTC2 must be programmed for Cascade Mode for both devices to operate.

**ICW2**—Address 021H (0A1H)

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| V7 | V6 | V5 | V4 | V3 | X | X | X |

(Write Only Register)

**V7-V3**—These bits are the upper 5 bits of the interrupt vector and are programmable by the CPU. The lower three bits of the vector are generated by the Priority Resolver during INTA (see Figure 12). INTC1 and INTC2 need not be programmed with the same value in ICW2.

**ICW3 Format for INTC1**—Address 021H

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 |

(Write Only Register)

**S7-S0**—Select which IR inputs have Slave Mode controllers connected. ICW3 in INTC1 must be written with a 04H for INTC2 to function.

**ICW3 Format for INTC2**—Address 0A1H

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| 0 | 0 | 0 | 0 | 0 | ID2 | ID1 | ID0 |

(Write Only Register)

**ID2-ID0**—Determine the Slave Mode address the controller will respond to during the cascaded INTA sequence. ICW3 in INTC2 should be written with a 02H for Cascade Mode operation. Note, b7-b3 should be zero.

**ICW4**—Address 021H (0A1H)

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| X | X | X | EMI | X | X | AEOI | X |

(Write Only Register)

**EMI**—Bit 4 will Enable Multiple Interrupts from the same channel in Fixed Priority Mode. This allows INTC2 to fully nest interrupts, when Cascade Mode with Fixed Priority Mode are both selected, without being blocked by INTC1. Correct handling of this mode requires the CPU to issue a non-specific EOI command to INTC2 and check its In-Service Register for zero, when exiting an interrupt service routine. If zero, a non-specific EOI command should be sent to INTC1. If non-zero, no command is issued.

**AEOI**—Auto End Of Interrupt is enabled when ICW4 is written with a zero in bit 1. The interrupt controller will perform a non-specific EOI on the trailing edge of the second INTA cycle. Note, this function should not be used in a device with fully nested interrupts unless the device is a cascade Master.

**Operational Command Words**

Operational Command Words (OCWs) allow the 82C206 interrupt controllers to be controlled or reconfigured at any time while operating. Each interrupt has 3 OCWs which can be programmed to affect the proper operating configuration and a Status Register to monitor controller operation.

Operational Command Word 1 (OCW1) is located at address 021h (0A1h) and may be written any time the controller is not in Initialization Mode. Operational Command Words 2 and 3 (OCW2,OCW3) are located at address 020H (0A0H). Writing to address 020H (0A0H) with a 0 in bit 4 will place the controller in operational mode and load OCW2 (if data bit 3 = 0) or OCW3 (if data bit 3 = 1).

**OCW1**—Address 021H (0A1H)

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| M7 | M6 | M5 | M4 | M3 | M2 | M1 | M0 |

(Read/Write Register)

**M7-M0**—These bits control the state of the Interrupt Mask Register. Each Interrupt Request can be masked by writing a 1 in the appropriate bit position (M0 controls IR0 etc.). Setting an IMR bit has no affect on lower priority requests. All IMR bits are cleared by writing ICW1.

**OCW2**—Address 020h (0A0h)

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| R | SL | EOI | SI | 2/3 | L2 | L1 | L0 |

(Write Only Register)

**R**—This bit in conjunction with SL and EOI selects operational function. Writing a 1 in bit 7 causes one of the rotate functions to be selected.

| R | SL | EOI | Function |
|---|---|---|---|
| 1 | 0 | 0 | Rotate on auto EOI enable* |
| 1 | 0 | 1 | Rotate on non-specific EOI |
| 1 | 1 | 0 | Specific Rotate Command |
| 1 | 1 | 1 | Rotate on specific EOI |

***This function is disabled by writing a zero to all three bit positions.**

**SL**—This bit in conjunction with R and EOI selects operational function. Writing a 1 in this bit position causes a specific or immediate function to occur. All specific commands require L2-L0 to be valid except no operation.

| R | SL | EOI | Function |
|---|---|---|---|
| 0 | 1 | 0 | No operation |
| 0 | 1 | 1 | Specific EOI Command |
| 1 | 1 | 0 | Specific Rotate Command |
| 1 | 1 | 1 | Rotate on specific EOI |

**EOI**—This bit in conjunction with R and SL selects operational function. Writing a 1 in this bit position causes a function related to EOI to occur.

| R | SL | EOI | Function |
|---|---|---|---|
| 0 | 0 | 1 | Non-specific EOI Command |
| 0 | 1 | 1 | Specific EOI Command |
| 1 | 0 | 1 | Rotate on non-specific EOI |
| 1 | 1 | 1 | Rotate on specific EOI |

**SI**—Writing a 0 in this bit position takes the interrupt controller out of initialize mode and writes OCW2 or OCW3.

**2/3**—If the I/O write places a 0 in bit 4 (SI), then writing a 0 in bit 3 (2/3) selects OCW2 and writing a 1 will select OCW3.

**L2-L0**—These three bits are internally decoded to select which interrupt channel is to be affected by the Specific command. L2-L0 must be valid during three of the four specific cycles (see SL above).

**OCW3**—Address 020H (0A0H)

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| 0 | ESMM | SMM | SI | 2/3 | PM | RR | RIS |

(Write Only Register)

**ESMM**—Writing a 1 in this bit position enables the Set/Reset Special Mask Mode function controlled by bit 5 (SMM). ESMM allows the other functions in OCW3 to be accessed and manipulated without affecting the Special Mask Mode state.

**SMM**—If ESMM and SMM both are written with a 1 the Special Mask Mode is enabled. Writing a 1 to ESMM and a 0 to SMM disables Special Mask Mode. During Special Mask Mode, writing a 1 to any bit position inhibits interrupts and a 0 enables interrupts on the associated channel by causing the Priority Resolver to ignore the condition of the ISR.

**SI**—See SI above.

**2/3**—See 2/3 above.

**PM**—Polled Mode is enabled by writing a 1 to bit 2 of OCW3, causing the 82C206 to perform the equivalent of an INTA cycle during the next I/O read operation to the controller. The byte read during this cycle will have bit 7 set if an interrupt is pending. If bit 7 of the byte is set, the level of the highest pending request will be encoded on bits 2-0. The IRR will remain frozen until the read cycle is completed at which time the PM bit is reset.

**RR**—When the RR bit (bit 1) is 1, reading the Status Port at address 020h (0A0h) will cause the contents of IRR or ISR (determined by RIS) to be placed on XD7-XD0. Asserting PM forces RR reset.

**RIS**—This bit selects between the IRR and the ISR during Status Read operations if RR = 1.

## COUNTER/TIMER FUNCTIONAL DESCRIPTION

The Counter/Timer (CTC) in the 82C206 is general purpose, and can be used to generate accurate time delays under software control. The CTC contains 3 16-bit counters (Counter 0-3) which can be programmed to count in binary or binary coded decimal (BCD). Each counter operates independently of the other two and can be programmed for operation as a timer or a counter.

All three of the counters shown in Figure 13 are controlled from a common set of control logic. The Control Logic decodes control in-

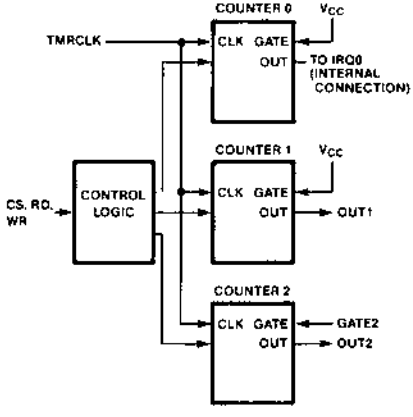



**Figure 13. Counter/Timer Block Diagram**

formation written to the CTC and provides the controls necessary to load, read, configure and control each counter. Counter 0 and Counter 1 can be programmed for all six modes, but Mode 1 and Mode 5 have limited usefulness due to the lack of an external hardware trigger signal. Counter 2 can be operated in any of six modes listed below.

| | |
|---|---|
| Mode 0 | Interrupt on terminal count |
| Mode 1 | Hardware retriggerable one-shot |
| Mode 2 | Rate generator |
| Mode 3 | Square wave generator |
| Mode 4 | Software triggered strobe |
| Mode 5 | Hardware retriggerable strobe |

All three counters in the CTC are driven from a common clock input pin (TMRCLK) which is independent from other clock inputs to the 82C206. Counter 0's output (Out0) is connected to IR0 of INTC1 (see Interrupt Controller Functional Description) and may be used as an interrupt to the system for time keeping and task switching. Counter 1 may be programmed to generate pulses or square waves for use by external devices. The third counter (Counter 2) is a full function Counter/Timer. This channel can be used as an interval timer, a counter, or as a gated rate/pulse generator.

**Counter Description**

Each counter in the CTC contains a Control Register, a Status Register, a 16-bit Counting Element (CE), a pair of 8-bit Counter Input Latches (CIL,CIH),and a pair of 8-bit Counter Output Latches (COL,COH). Each counter also has a clock input for loading and decrementing the CE, a mode defined GATE input for controlling the counter (only GATE2 is externally accessible), and an OUT signal (OUT0 is not externally accessible). The OUT signal's state and function are controlled by the Counter Mode and condition of the CE (see Mode Definitions).

The Control Register stores the mode and command information used to control the counter. The Control Register may be loaded by writing a byte, containing a pointer to the desired counter, to the Write Control Word address (043h). The remaining bits in the byte contain the mode, the type of command, and count format information.

The Status register allows the software to monitor counter condition and read back the contents of the Control Register.

The Counting Element is a loadable 16-bit synchronous down counter. The CE is loaded or decremented on the falling edge of TMRCLK. The CE contains the maximum count when a 0 is loaded; which is equivalent to 65536 in binary operation or 10000 in BCD. The CE does not stop when it reaches 0. In Modes 2 and 3 the CE will be reloaded and in all other modes it will wrap around to FFFF in binary operation or 9999 in BCD.

The CE is indirectly loaded by writing one or two bytes (optional) to the Counter Input Latches, which are in turn loaded into the CE. This allows the CE to be loaded or reloaded in one TMRCLK cycle.

The CE is also read indirectly by reading the contents of the Counter Output Latches. COL and COH are transparent latches which can be read while transparent or latched (see Latch Counter Command).

### Programming The CTC

After power-up the condition of CTC Control Registers, counter registers, CE, and the output of all counters is undefined. Each counter must be programmed before it can be used.

Counters are programmed by writing a Control Word and then an initial count. The Control Register of a counter is written by writing to the Control Word address (see Figure 14). The Control Word is a write only location.

**Control Word**—(043H)

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| F3 | F2 | F1 | F0 | M2 | M1 | M0 | BCD |

(Write Only Register)

**F3-F0**—Bits 7-4 determine the command to be performed.

**M2-M0**—Bits 3-1 determine the counter's mode during Read/Write Counter Commands (see Read/Write Counter Command) or select the counter during a Read-Back Command (see Read-Back Command). Bits 3-1 become "don't care" during Latch Counter Commands.

| Address | Function |
|---|---|
| 040h | Counter 0 Read/Write |
| 041h | Counter 1 Read/Write |
| 042h | Counter 2 Read/Write |
| 043h | Control Register Write Only |

**Figure 14. Counter/Timer Address Map**

**BCD**—Bit 0 selects binary coded decimal counting format during Read/Write Counter Commands. Note, during Read-Back Command this bit must be 0.

### Read/Write Counter Command

When writing to a counter, two conventions must be observed:

1—Each counters Control Word must be written before the initial count is written.

2—Writing the initial count must follow the

| F3 | F2 | F1 | F0 | Command |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Latch Counter 0 (see Counter Latch Command) |
| 0 | 0 | 0 | 1 | Read/Write Counter 0 LSB Only |
| 0 | 0 | 1 | 0 | Read/Write Counter 0 MSB Only |
| 0 | 0 | 1 | 1 | Read/Write Counter 0 LSB then MSB |
| 0 | 1 | 0 | 0 | Latch Counter 1 (see Counter Latch Command) |
| 0 | 1 | 0 | 1 | Read/Write Counter 1 LSB Only |
| 0 | 1 | 1 | 0 | Read/Write Counter 1 MSB Only |
| 0 | 1 | 1 | 1 | Read/Write Counter 1 LSB then MSB |
| 1 | 0 | 0 | 0 | Latch Counter 2 (see Counter Latch Command)2 |
| 1 | 0 | 0 | 1 | Read/Write Counter 2 LSB Only |
| 1 | 0 | 1 | 0 | Read/Write Counter 2 MSB Only |
| 1 | 0 | 1 | 1 | Read/Write Counter 2 LSB then MSB |
| 1 | 1 | X | X | Read-Back Command (see Counter Read-Back Command) |

**MSB** = most significant byte
LSB = least significant byte

format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

A new initial count can be written into the counter at any time after programming without rewriting the Control Word providing the programmed format is observed.

During Read/Write Counter Commands M3-M0 are defined as follows:

| M2 | M1 | M0 | Function |
|---|---|---|---|
| 0 | 0 | 0 | Select Mode 0 |
| 0 | 0 | 1 | Select Mode 1 |
| X | 1 | 0 | Select Mode 2 |
| X | 1 | 1 | Select Mode 3 |
| 1 | 1 | 0 | Select Mode 4 |
| 1 | 1 | 1 | Select Mode 5 |

**Latch Counter Command**

When a Latch Counter Command is issued, the counter's output latches (COL,COH) latch the current state of the CE. COL and COH remain latched until read by the CPU, or the counter is reprogrammed. The output latches then return to a "transparent" condition. In this condition the latches are enabled and the contents of the CE may be read directly.

Latch Counter Commands may be issued to more than one counter before reading the first counter to which the command was issued. Also, multiple Latch Counter Commands issued to the same counter without reading the counter will cause all but the first command to be ignored.

**Read-Back Command**

The Read-Back Command allows the user to check the count value, Mode, and state of the OUT signal and Null Count Flag of the selected counter(s).

The format of the Read-Back Command is:

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| 1 | 1 | LC | LS | C2 | C1 | C0 | 0 |

**LC**—Writing a 0 in bit 5 causes the selected counter(s) to latch the state of the CE in COL and COH.

**LS**—Writing a 0 in bit 4 causes the selected counter(s) to latch the current condition of it's Control Register, Null Count and Output into the Status Register. The next read of the Counter will result in the contents of the Status Register being read (see Status Read).

**C2-C0**—Writing a 1 in bit 3 causes Counter 3 to latch one or both of the registers specified by LC and LS. The same is true for bits 2 and 1 except that they enable Counters 1 and 0 respectively.

Each counter's latches remain latched until either the latch is read or the counter is reprogrammed.

If LS = LC = 0, status will be returned on the next read from the counter. The next one or two reads (depending on whether the counter is programmed to transfer one or two bytes) from the counter result in the count being returned.

**Status Byte**

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| OUT | NC | F1 | F0 | M2 | M1 | M0 | BCD |

**OUT**—Bit 7 contains the state of the OUT signal of the counter

**NC**—Bit 6 contains the condition of the Null Count Flag. This flag is used to indicate that the contents of the CE are valid. NC will be set to a 1 during a write to the Control Register or the counter. NC is cleared to a 0

whenever the counter is loaded from the counter input registers.

**F1-F0**—Bits 5-4 contain the F1 and F0 Command bits which were written to the Command Register of the counter during initialization. This information is useful in determining whether the high byte, the low byte or both must be transferred during counter read/write operations.

**M2-M1**—These bits reflect the mode of the counter and are interpreted in the same manner as in Write Command operations.

**BCD**—Bit 0 indicates the CE is operating in BCD format.

**Counter Operation**

Due to the previously stated restrictions in Counter 0 and Counter 1, Counter 2 will be used as the example in describing counter operation, but the description of Mode 0, 2, 3 and 4 is relevant to all counters.

The following terms are defined for describing CTC operation.

TMRCLK pulse—A rising edge followed by a falling edge of the 82C206 TMRCLK input.

trigger—The rising edge of the GATE2 input.

counter load—The transfer of the 16-bit value in CIL and CIH to the CE.

initialized—A Control Word written and the Counter Input Latches loaded.

Counter 2 operates in one of the following modes.

**Mode 0**—Interrupt on terminal count

Writing the Control Word causes OUT2 to go low and remain low until the CE reaches 0, at which time it goes back high and remains high until a new count or Control Word is written. Counting is enabled when GATE2 = 1. Disabling the count has no effect on OUT2.

The CE is loaded with the first TMRCLK pulse after the Control Word and initial count are loaded. When both CIL and CIH are written, the CE is loaded after CIH is written (see Write Operations). This TMRCLK pulse does not decrement the count, so for an initial count of N, OUT2 does not go high until N+1 TMRCLK pulses after initialization. Writing a new initial count to the counter reloads the CE on the next TMRCLK pulse and counting continues from the new count.

If an initial count is written with GATE2 = 0, it will still be loaded on the next TMRCLK pulse but counting does not begin until GATE2 = 1. OUT2 therefore, goes high N TMRCLK pulses after GATE2 = 1.

**Mode 1—Hardware retriggerable one-shot**

Writing the Control Word causes OUT2 to go high initially. Once initialized the counter is armed and a trigger causes OUT2 to go low on the next TMRCLK pulse. OUT2 then remains low until the counter reaches 0. An initial count of N results in a one-shot pulse N TMRCLK cycles long.

Any subsequent triggers while OUT2 is low cause the CE to be reloaded, extending the length of the pulse. Writing a new count to CIL and CIH will not affect the current one-shot unless the counter is retriggered.

**Mode 2—Rate generator**

Mode 2 functions as a divide-by-N counter, with OUT2 as the carry. Writing the Control Word during initialization sets OUT2 high.

When the initial count is decremented to 1, OUT2 goes low on the next TMRCLK pulse. The following TMRCLK pulse returns OUT2 high, reloads the CE and the process is repeated. In Mode 2 the counter continues counting (if GATE2 = 1) and will generate an OU T2 pulse every N TMRCLK cycles. Note that a count of 1 is illegal in Mode 2.

GATE2 = 0 disables counting and forces OUT2 high immediately. A trigger reloads the the CE on the next TMRCLK pulse. Thus GATE2 can be used to synchronize the counter to external events.

Writing a new count while counting does not

affect current operation unless a trigger is received. Otherwise, the new count will be loaded at the end of the current counting cycle.

**Mode 3—Square wave generator**

Mode 3 is similar to Mode 2 in every respect except for the duty cycle of OUT2. OUT2 is set high initially and remains high for the first half of the count. When the first half of the initial count expires, OUT2 goes low for the remainder of the count.

If the counter is loaded with an even count, the duty cycle of OUT2 will be 50% (high = low = N/2). For odd count values, OUT2 is high one TMRCLK cycle longer than it is low. Therefore, high = (N+1)/2 and low = (N-1)/2.

**Mode 4—Software triggered strobe**

Writing the Control Word causes OUT2 to go high initially. Expiration of the initial count causes OUT2 to go low for one TMRCLK cycle. GATE2 = 0 disables counting but has no effect on OUT2. Also, a trigger will not reload the CE.

The counting sequence is started by writing the initial count. The CE is loaded on the TMRCLK pulse after initialization. The CE begins decrementing one TMRCLK pulse later. OUT2 will go low for one TMRCLK cycle, (N+1) cycles after the initial count is written.

If a new initial count is written during a counting sequence, it is loaded into the CE on the next TMRCLK pulse and the sequence continues from the new count. This allows the sequence to be "retriggerable" by software.

**Mode 5—Hardware triggered strobe**

Writing the Control Word causes OUT2 to go high initially. Counting is started by trigger. The expiration of the initial count causes OUT2 to go low for one TMRCLK cycle. GATE2 = 0 disables counting.

The CE is loaded on the TMRCLK pulse after a trigger. Since loading the CE inhibits decrementing, OUT2 will go low for one TMRCLK cycle, (N+1) TMRCLK cycles after the trigger.

If a new count is loaded during counting, the current counting sequence will not be affected unless a trigger occurs. A trigger causes the counter to be reloaded from CIL and CIH, making the counter "retriggerable".

| Mode | Condition | | |
|---|---|---|---|
| | Low | Rising | High |
| 0 | Disables Counting | — | Enables Counting |
| 1 | — | a) Initiates Counting<br>b) Resets Out Pin | — |
| 2 | a) Disables Counting<br>b) Forces Out Pin High | Initates Counting | Enables Counting |
| 3 | a) Disables Counting<br>b) Forces Out Pin High | Initiates Counting | Enables Counting |
| 4 | Disables Counting | — | Enables Counting |
| 5 | — | Initiates Counting | — |

**Figure 15. Gate Pin Function**

### GATE2

In Modes 0, 2, 3 and 4 GATE2 is level sensitive and is sampled on the rising edge of TMRCLK. In Modes 1, 2, 3 and 5 the GATE2 input is rising-edge sensitive. This rising edge sets an internal flip-flop whose output is sampled on the next rising edge of TMRCLK. The flop-flop resets immediately after being sampled. Note that in Modes 2 and 3 the GATE2 input is both edge and level sensitive.

### REAL TIME CLOCK FUNCTIONAL DESCRIPTION

This section of the 82C206 combines a complete time-of-day clock with alarm, one hundred year calendar, a programmable periodic interrupt, and 114 bytes of low power static RAM. Provisions are made to enable the device to operate in a low power (battery powered) mode and protect the contents of both the RAM and clock during system power-up and power-down.

#### Register Access

Reading and writing to the 128 locations in the Real Time Clock is accomplished by first placing the Index Address of the location you wish to access on the data input pins XD0-XD6 and then strobing the AS input pin. The address will then be latched into the Index Address Register on the falling edge of AS. The Index Address Register is then used as a pointer to the specific byte in the Real Time Clock, which may be read or written to by asserting $\overline{XIOR}$ or $\overline{XIOW}$ with with an address on the XA9-XA0 inputs of 071H.

Since AS will most likely be generated by an I/O operation which will result in the assertion of $\overline{XIOW}$, it is recommended that an address of 070H be applied to the XA9-XA0 inputs during this time. This will prevent the modification of other registers in the 82C206.

#### Address Map

Figure 16 illustrates the internal register/RAM organization of the Real Time Clock portion of the 82C206. The 128 addressable locations in the Real Time Clock are divided into 10 bytes which normally contain the time, calendar, and alarm data, four control and status bytes and 114 general purpose RAM bytes. All 128 bytes are readable by the CPU. The CPU may also write to all locations except Registers C, D, Bit 7 of Register A and Bit 7 of the Seconds Byte which is always 0.

| Index | Function |
|---|---|
| 00 | SECONDS |
| 01 | SECONDS ALARM |
| 02 | MINUTES |
| 03 | MINUTES ALARM |
| 04 | HOURS |
| 05 | HOURS ALARM |
| 06 | DAY OF WEEK |
| 07 | DATE OF MONTH |
| 08 | MONTH |
| 09 | YEAR |
| 0A | REGISTER A |
| 0B | REGISTER B |
| 0C | REFISTER C |
| 0D | REGISTER D |
| 0E | USER RAM |
| 0F | USER RAM |
| . | |
| . | |
| . | |
| 7E | USER RAM |
| 7F | USER RAM |

**Figure 16. Address Map for Real Time Clock**

#### Time Calendar and Alarm Bytes

The CPU can obtain the time and calendar information by reading the appropriate locations in the Real Time Clock. Initialization of the time, calendar and alarm information is accomplished by writing to these locations. Information is stored in these locations in binary-coded decimal (BCD) format.

Before initalization of the internal registers can be performed, the SET bit in Register B should be set to a "1" to prevent Real Time Clock updates from occuring. The CPU then initalizes the first 10 locations in BCD format. The SET bit should then be cleared to allow updates. Once initalized and enabled, the Real Time Clock will perform Clock/Calendar updates at a 1 Hz rate.

| Index Register Address | Function | BCD Range |
|---|---|---|
| 0 | Seconds | 00-59 |
| 1 | Seconds Alarm | 00-59 |
| 2 | Minutes | 00-59 |
| 3 | Minutes Alarm | 00-59 |
| 4 | Hours (12 hour mode) | 01-12 (AM) 81-92 (PM) |
| | Hours (24 hour mode) | 00-23 |
| 5 | Hours Alarm (12 hour mode) | 01-12 (AM) 81-92 (PM) |
| | Hours Alarm (24 hour mode) | 00-23 |
| 6 | Day of Week | 01-07 |
| 7 | Day of Month | 01-31 |
| 8 | Month | 01-12 |
| 9 | Year | 00-99 |

**Figure 17. Time, Calendar, Alarm Data Format**

Figure 17 shows the format for the ten clock, calendar and alarm locations. The 24/12 bit in Register B determines whether the hour locations will be updated using a 1-12 or 0-23 format. After initalization the 24/12 bit cannot be changed without reinitalizing the hour locations. In 12 hour format the high order bit of the hours byte in both the time and alarm bytes will indicate PM when it is a "1".

During updates, which occur once per second, the 10 bytes of time, calendar and alarm information are unavailable to be read or written by the CPU for a period of 2ms. These 10 locations cannot be written during this time. Information read while the Real Time Clock is performing an update will be undefined. The Update Cycle section shows how to avoid Update Cycle/CPU contention problems.

The alarm bytes can be programmed to generate an interrupt at a specific time or they can be programmed to generate a periodic interrupt. To generate an interrupt at a specific time, the user need only program the time that the interrupt is to occur into the 3 alarm bytes. Alternately, a periodic interrupt can be generated by setting the high order two bits in an alarm register to a "1", which turns that byte into a "don't care". For instance, an interrupt can be generated every hour by programming a C0H into Register 5, or an interrupt can be generated once a second by programming the same value into all three alarm registers.

**Static RAM**

The 114 bytes of RAM from Index Address 0EH to 7FH are not affected by the Real Time Clock. These bytes are accessable during the update cycle and may be used for whatever the designer wishes. Typical applications will use this as nonvolatile storage for configuration and calibration parameters since this device is normally battery powered when the system in turned off.

**Control and Status Registers**

The 82C206 contains four registers used to control the operation and monitor the status of the Real Time Clock. These registers are located at Index Address 0AH-0DH and are accessable by the CPU at all times.

**REGISTER A** (0AH)

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| UIP | DV2 | DV1 | DV0 | RS3 | RS2 | RS1 | RS0 |

(Read/Write register except UIP)

**UIP**—Update in progress flag is a status bit used to indicate when an update cycle is about to take place. A "1" indicates that an update cycle is taking place or is imminent. UIP will go active (High) 244us prior to the start of an update cycle and will remain active for an additional 2ms while the update is taking place. The UIP bit is read only and is not affected by Reset. Writing a "1" to the SET bit in Register B will clear the UIP status bit.

**DV2-DV0**—These three bits are used to control the Divider/Prescaler on the Real Time Clock. While the 82C206 can operate at frequencies higher than 32.768 Khz, this is not recommended for battery powered operation due to the increased power consumption at these higher frequencies.

| DV2 | DV1 | DV0 | OSCI Freq. | Mode |
|---|---|---|---|---|
| 0 | 0 | 0 | 4.194304MHz | Operate |
| 0 | 0 | 1 | 1.048576MHz | Operate |
| 0 | 1 | 0 | 32.768KHz | Operate |
| 1 | 1 | X | Reset Divider | |

Divider Options

**RS3-RS0**—These four bits control the Periodic Interrupt rate. The Periodic interrupt is derived from the Divider/Prescaler in the Real Time Clock and is separate from the Alarm Interrupt. Both the alarm and periodic interrupts do however, use the same interrupt channel in the Interrupt Controller. Use of the Periodic Interrupt allows the generation of interrupts at rates higher than once per second. Below are the interrupt rates for which the Real Time Clock can be programmed.

| Rate Selection | | | | Time Base | |
|---|---|---|---|---|---|
| RS3 | RS2 | RS1 | RS0 | 4.194304 MHz<br>1.048576 MHz | 32.768 KHz |
| 0 | 0 | 0 | 0 | None | None |
| 0 | 0 | 0 | 1 | 30.517 μs | 3.90526 ms |
| 0 | 0 | 1 | 0 | 61.035 μs | 7.8125 ms |
| 0 | 0 | 1 | 1 | 122.070 μs | 122.070 μs |
| 0 | 1 | 0 | 0 | 244.141 μs | 244.141 μs |
| 0 | 1 | 0 | 1 | 488.281 μs | 488.281 μs |
| 0 | 1 | 1 | 0 | 976.562 μs | 976.562 μs |
| 0 | 1 | 1 | 1 | 1.953125 ms | 1.953125 ms |
| 1 | 0 | 0 | 0 | 3.90625 ms | 3.90625 ms |
| 1 | 0 | 0 | 1 | 7.8125 ms | 7.8125 ms |
| 1 | 0 | 1 | 0 | 15.625 ms | 15.625 ms |
| 1 | 0 | 1 | 1 | 31.25 ms | 31.25 ms |
| 1 | 1 | 0 | 0 | 62.5 ms | 62.5 ms |
| 1 | 1 | 0 | 1 | 125 ms | 125 ms |
| 1 | 1 | 1 | 0 | 250 ms | 250 ms |
| 1 | 1 | 1 | 1 | 500 ms | 500 ms |

Periodic Interrupt Rate

**REGISTER B** (0BH)

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| SET | PIE | AIE | UIE | 0 | 024/12 | DSE | |

(Read/Write Register)

**SET**—Writing a "0" to this bit enables the Update Cycle and allows the Real Time Clock to function normally. When set to a "1" the Update Cycle is inhibited and any cycle in progress is aborted. The SET bit is not affected by the $\overline{\text{RESET}}$ input pin.

**PIE**—The Periodic Interrupt Enable Bit controls the generation of interrupts based on the value programmed into the RS3-RS0 bits of Register A. This allows the user to disable this function without affecting the programmed rate. Writing a "1" to this bit enables the generation of periodic interrupts. This bit is cleared to a "0" by Reset.

**AIE**—The generation of alarm interrupts is enabled by setting this bit to a "1". Once this bit is enabled the Real Time Clock will generate an alarm whenever a match occurs between the programmed alarm and clock information. If the don't care condition is programmed into one or more of the Alarm Registers, this will enable the generation of periodic interrupts at rates of one second or greater. This bit is cleared by Reset.

**24/12**—The 24/12 control bit is used to establish the format of both the Hours and Hours Alarm bytes. If this bit is a "1", the Real Time Clock will interpret and update the the information in these two bytes using the 24 hour mode. This bit can be read or written by the CPU and is not affected by Reset.

**DSE**—The Real Time Clock can be instructed to handle daylight savings time changes by setting this bit to a "1". This enables two exceptions to the normal time keeping sequence to occur. On the last Sunday in April AM. Set-
ting this bit to a "0" disables the execution of these two exceptions. $\overline{\text{PSRSTB}}$ has no affect on this bit.

**REGISTER C** (0CH)

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| IRQF | PF | AF | UF | 0 | 0 | 0 | 0 |

(Read only register)

**IRQF**—The Interrupt Request Flag bit is set to a "1" when any of the conditions which can cause an interrupt is true and the interrupt enable for that condition is true. The condition which causes this bit to be set, also generates an interrupt. The logic expression for this flag is:

IRQF = PF & PIE
+ AF & AIE
+ UF & UIE

This bit and all other active bits in this register are cleared by reading the register or by activating the PSRSTB/ input pin. Writing to this register has no affect on the contents.

**PF**—The Periodic Interrupt Flag is set to a "1" when a transition, which is selected by RS3-RS0, occurs in the divider chain. This bit will become active, independent of the condition of the PIE control bit. The PF bit will then generate an interrupt a nd set IRQF if PIE is a "1".

**AF**—A "1" appears in the AF bit whenever a match has occured between the time registers and alarm registers during an update cycle. This flag is also independent of it's enable (AIE) and will generate an interrupt if AIE is true.

**REGISTER D** (0DH)

| msb | | | | | | | lsb |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| VRT | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

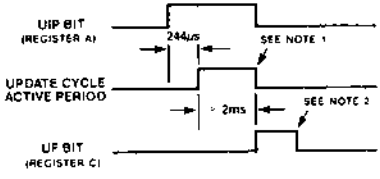
(Read only register)

**VRT**—The Valid RAM and Time Bit indicates the condition of the contents of the Real Time Clock. This bit is cleared to a "0" whenever the PS input pin is LOW. This pin

is normally derived from the power supply which supplies Vcc to the device and will allow the user to determine whether the registers have been initalized since power was applied to the device. $\overline{PSRSTB}$ has no affect on this bit and it can only be set by reading Register D.All unused register bits will be "0" when read and are not writable.

**Update Cycle**

During normal operation the Real Time Clock will perform an update cycle once every second. The performance of an update cycle is contingent upon the divider bits DV2-DV0 not being cleared, and the SET bit in Register B cleared. The function of the update cycle is to increment the clock/calendar registers and compare them to the Alarm Registers. If a match occurs between the two sets of registers, an alarm is issued and an interrupt will be issued if the alarm and interrupt control bits are enabled.




NOTE:
1. REGISTERS 0-9 ARE UNAVAILABLE TO BE READ OR WRITTEN DURING THIS TIME
2. UF BIT CLEARED BY CPU READ OF REGISTER C

**Figure 18. Update Cycle**

During the time that an update is taking place, the lower 10 registers are unavailable to the CPU. This is done to prevent the possible corruption of data in the registers or the reading of incorrect data. To avoid contention problems between the Real Time Clock and the CPU, a flag is provided in Register A to alert the user of an impending update cycle. This Update In Process Bit (UIP) is asserted 244μs before the actual start of the cycle and is maintained until the cycle is complete. Once the cycle is complete the UIP bit will be cleared and the Update Flag (UF) in Register C will be set. Figure 18 illustrates the update cycle. CPU access is always allowed to Registers A through D during update cycles.

Two methods for reading and writing to the Real Time Clock are recommended. Both of these methods will allow the user to avoid contention between the CPU and the Real Time Clock for access to the time and date information.

The first method is to read Register A, determine the state of the UIP bit and if it is "0", perform the read or write operation. For this method to work successfully the entire read or write operation (including any interrupt service routines which might occur) must not require longer than 244μs to complete from the beginning of the read of Register A to the completion of the last read or write operation to the Clock Calendar Registers.

The second method of accessing the lower 10 registers is to read Register C once and disregard the contents. Then subsequently continue reading this register until the UF bit is a "1". This bit will become true immediately after an update has been completed. The user then has until the start of the next update cycle to complete a read or write operation.

**Power-Up/Down**

Most applications will require the Real Time Clock to remain active whenever the system power is turned off. To accomplish this the user must provide an alternate source of power to the 82C206. This alternate source of power is normally provided by connecting a battery to the Vcc supply pin of the device. A means should be provided to switch from the system power supply to the battery. A circuit such as the one shown in Figure 19 may be used to eliminate power drain on the battery when the entire 82C206 is active. The circuit shown here will allow for reliable transitions between system and battery power without undue battery power drain.

*The user should also ensure that the Vin maximum specification is never exceeded when powering the system up or down. Failure to observe this specification may result in damage to the device.*

A pin is provided on the device to protect the contents of the Real Time Clock and reduce power consumption whenever the system is powered down. This pin (PWRGD) should be low whenever the system power supply is not within specifications for proper operation of the system. This signal may be generated by circuitry in either the power supply or on the system board. The PWRGD input will disable all unnecessary inputs during the time the system is powered down to prevent noise on the inactive pins from causing increased Icc. This pin must therefore be inactive for the remainder of the device to operate properly when system power is applied.

One pin is provided to initalize the device whenever power is applied to the 82C206. This pin (PSRSTB) will not alter the RAM or Clock/Calendar contents but it will initalize the necessary control register bits. (See Pin Description for a list of the control register bits affected by PSRSTB) Assertion of PSRSTB disables the generation of interrupts and sets a flag indicating that the contents of the device may not be valid. A recommended circuit for controlling the PSRSTB input is also shown in Figure 19.

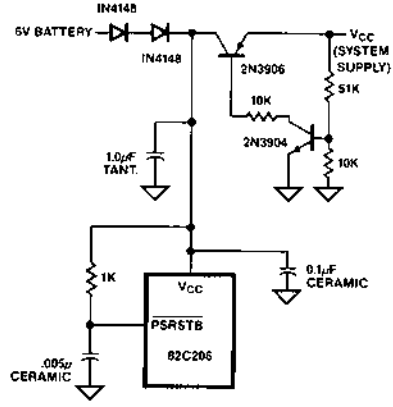



**Figure 19. Power Conversion and Reset Circuitry**

### 82C206 Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | — | 7.0 | V |
| Input Voltage | $V_I$ | -0.5 | 5.5 | V |
| Output Voltage | $V_O$ | -0.5 | 5.5 | V |
| Operating Temperature | $T_{op}$ | -25 | 85 | C |
| Storage Temperature | $T_{stg}$ | -40 | 125 | C |

**NOTE:** Permanent device may occur of Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

### 82C206 Operating Conditions

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.75 | 5.25 | V |
| Ambient Temperature | $T_A$ | 0 | 70 | C |

### DC Characteristics ($T_A$ = 0-70°C, $V_{CC}$ = 5 ± 5%)

| Symbol | Parameter | Min. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.5 | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.0 | $V_{CC}$+0.5 | V | |
| $V_{OL}$ | Output Low Voltage | | 0.4 | V | $I_{OL}$ = 2.0 mA |
| $V_{OH}$ | Output High Voltage | 2.4 | | V | $I_{OH}$ = -2.0 mA |
| $I_{OL}$ | Input Current | -10 | 10 | μA | $V_{IN}$ = $V_{CC}$ to 0V |
| $I_{OL}$ | Output Leakage Current | -10 | 10 | μA | $V_{OU}$ = $V_{CC}$ to 0.45 |
| $I_{CC}$ | $V_{CC}$ Supply Current | | 30 | mA | CLK Freq = 8 MHz |
| $I_{CCSB}$ | $V_{CC}$ Standby Supply Current | | 10 | μA | CLK Freq = DC |

### Capacitance ($T_A$ = 25°C, $V_{CC}$ = GND = 0V)

| Symbol | Parameter | Min. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | 10 | pF | FC = 1 MHz |
| $C_{I/O}$ | I/O Capacitance | | 20 | pF | Unmeasured pins |
| $C_{OUT}$ | Output Capacitance | | 20 | pF | Returned to $V_{SS}$ |

**AC Characteristics** ($T_A$ = 0–70°C, $V_{CC}$ = 5V + 5%)

| Symbol | Parameter | 6 MHz Min. | 6 MHz Max. | 8 MHz Min. | 8 MHz Max. | Units |
|---|---|---|---|---|---|---|
| t1 | Address Setup to Command Active | 25 | | 25 | | nsec |
| t2 | Command Active Period | 250 | | 200 | | nsec |
| t3 | Address Hold Time from Command Inactive | 0 | | 0 | | nsec |
| t4 | Data Valid Delay | 200 | | 160 | | nsec |
| t5 | Data Hold Time from $\overline{XIOR}$ Inactive | 10 | | 10 | | nsec |
| t6 | XD0-XD7 Active from $\overline{XIOR}$ | 5 | 40 | 5 | 40 | nsec |
| t7 | Data Setup to $\overline{XIOW}$ Inactive | 200 | | 160 | | nsec |
| t8 | Data Hold Time from $\overline{XIOW}$ Inactive | 0 | | 0 | | nsec |
| t9 | Command Recovery Time | 150 | | 120 | | nsec |
| t10 | Interrupt Request width (Low) | 120 | | 100 | | nsec |
| t11 | Interrupt Request width (High) | 250 | | 200 | | nsec |
| t12 | INT Output Delay | | 400 | | 300 | nsec |
| t20 | Real Time Clock Cycle Time | | 500 | | 500 | nsec |
| t21 | AS Pulse Width | 200 | | 160 | | nsec |
| t22 | Data Valid Setup to AS Inactive | 200 | | 160 | | nsec |
| t23 | Data Hold Time from AS Inactive | 0 | | 0 | | nsec |
| t24 | OSCI Period | 500 | | 500 | | nsec |
| t25 | OSCI High Time | 200 | | 200 | | nsec |
| t26 | OSCI Low Time | 200 | | 200 | | nsec |
| t27 | PSRSTB High Delay from $V_{CC}$ | 5 | | 5 | | μsec |
| t28 | PSRSTB Low Pulse Width | 5 | | 5 | | μsec |
| t29 | VRT Bit Valid Delay | | 2 | | 2 | μsec |
| t40 | TMRCLK Period | 200 | DC | 125 | DC | nsec |
| t41 | TMRCLK Low Time | 80 | | 50 | | nsec |
| t42 | TMRCLK High Time | 80 | | 50 | | nsec |
| t43 | GATE2 Setup to TMRCLK | 80 | | 50 | | nsec |
| t44 | GATE2 Hold Time from TMRCLK | 80 | | 50 | | nsec |
| t45 | GATE2 Low Time | 80 | | 50 | | nsec |
| t46 | GATE2 High Time | 80 | | 50 | | nsec |
| t47 | OUT2 Delay from TMRCLK | | 200 | | 120 | nsec |
| t48 | OUT2 Delay from GATE2 | | 200 | | 120 | nsec |

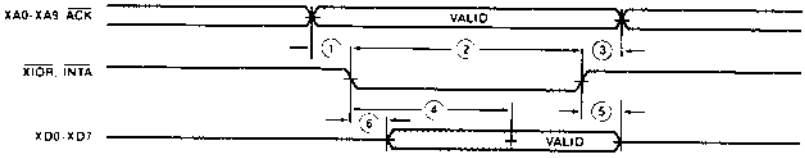
**AC Characteristics** ($T_A$ = 0-70°C, $V_{CC}$ = 5V + 5%) (Continued)

| Symbol | Parameter | 6 MHz Min. | 6 MHz Max. | 8 MHz Min. | 8 MHz Max. | Units |
|---|---|---|---|---|---|---|
| t50 | SCLK Period (1 X SCLK) | 186 | | 125 | | nsec |
| t50A | SCLK Period (2 X SCLK) | 93 | | 62 | | nsec |
| t51 | SCLK Low Time (1 X SCLK) | 75 | | 43 | | nsec |
| t51A | SCLK Low Time (2 X SCLK) | 32 | | 22 | | nsec |
| t52 | SCLK High Time (1 X SCLK) | 82 | | 55 | | nsec |
| t52A | SCLK High Time (2 X SCLK) | 40 | | 27 | | nsec |
| t53 | DREQx Setup to SCLK | 0 | | 0 | | nsec |
| t54 | HRQ Valid From SCLK | | 120 | | 75 | nsec |
| t55 | HLDA Setup to SCLK | 75 | | 45 | | nsec |
| t56 | AENx Valid Delay from SCLK | | 175 | | 105 | nsec |
| t57 | AENx Invalid Delay from SCLK | TBD | 130 | TBD | 80 | nsec |
| t58 | ADSTBx Valid Delay from SCLK | | 80 | | 50 | nsec |
| t59 | ADSTBx Invalid Delay from SCLK | | 120 | | 120 | nsec |
| t60 | XD0-XD7 Active Delay from SCLK | | 110 | | 60 | nsec |
| t61 | XD0-XD7 Valid Setup to ADSTBx Low | 80 | | 65 | | nsec |
| t62 | XD0-XD7 Hold Time from ADSTBx Low | 25 | | 25 | | nsec |
| t63 | XD0-XD7 Tristate Delay from SCLK | | 170 | | 135 | nsec |
| t64 | Address Valid Delay from SCLK | | 110 | | 60 | nsec |
| t65 | Address Hold Time from DMAMEMR High | 66 | | 50 | | nsec |
| t66 | Address Tristate Delay from SCLK | | 90 | | 55 | nsec |
| t67 | DACKx Delay from SCLK | | 170 | | 105 | nsec |
| t68 | Command Enable Delay from SCLK | | 150 | | 90 | nsec |
| t69 | Command Active Delay from SCLK | | 190 | | 120 | nsec |
| t70 | Write Cmnd Inactive Delay from SCLK | | 130 | | 80 | nsec |
| t71 | Address Hold Time from Write High | 116 | | 75 | | nsec |
| t72 | Command Tristate Delay from SCLK | | 120 | | 75 | nsec |

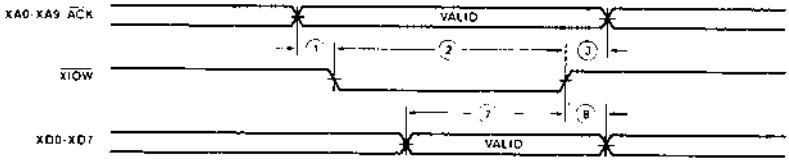
**AC Characteristics** ($T_A$ = 0–70°C, $V_{CC}$ = 5V ± 5%) (Continued)

| Symbol | Parameter | 6 MHz Min. | 6 MHz Max. | 8 MHz Min. | 8 MHz Max. | Units |
|---|---|---|---|---|---|---|
| t73 | Read Cmnd Inactive Delay from SCLK | | 190 | | 115 | nsec |
| t74 | TC Delay from SCLK | | 100 | | 60 | nsec |
| t75 | XD0-XD7 Setup to Read Cmnd Inactive | 155 | | 90 | | nsec |
| t76 | XD0-XD7 Hold from Read Cmnd Inactive | 0 | | 0 | | nsec |
| t77 | XD0-XD7 Valid Delay from SCLK | | 190 | | 120 | nsec |
| t78 | XD0-XD7 Hold from Write Inactive | 15 | | 15 | | nsec |
| t79 | IOCHRDY Input Setup to SCLK | 50 | | 35 | | nsec |
| t80 | IOCHRDY Input Hold Time from SCLK | 35 | | 20 | | nsec |

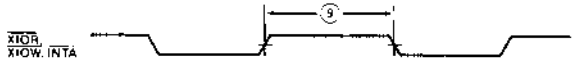
## 82C206 TIMING DIAGRAMS



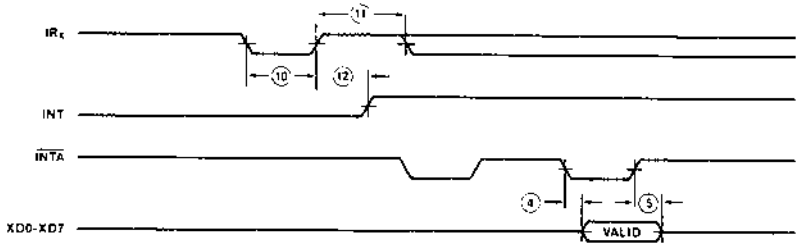

PERIPHERAL READ INTA CYCLE




PERIPHERAL WRITE CYCLE

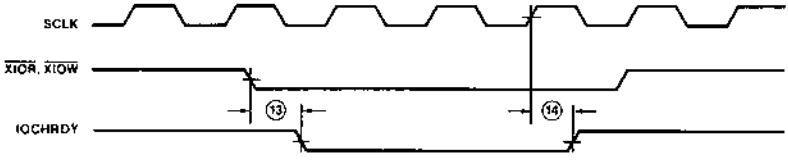



COMMAND RECOVERY

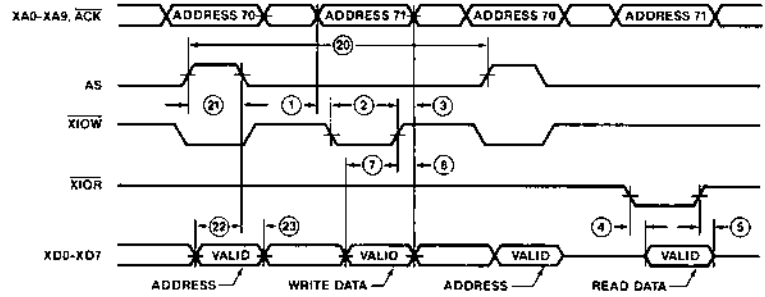



INTA SEQUENCE

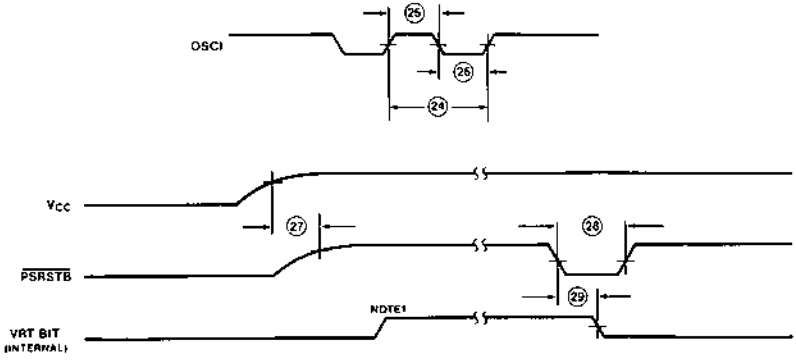
## 82C206 TIMING DIAGRAMS




IOCHRDY OUTPUT

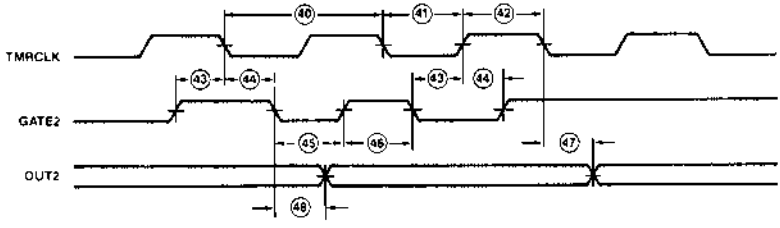



REAL TIME CLOCK ACCESS CYCLE

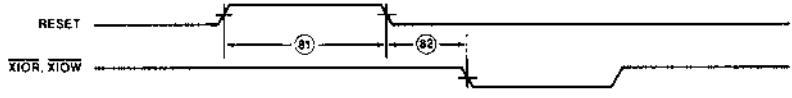



REAL TIME CLOCK POWER-UP SEQUENCE

## 82C206 TIMING DIAGRAMS

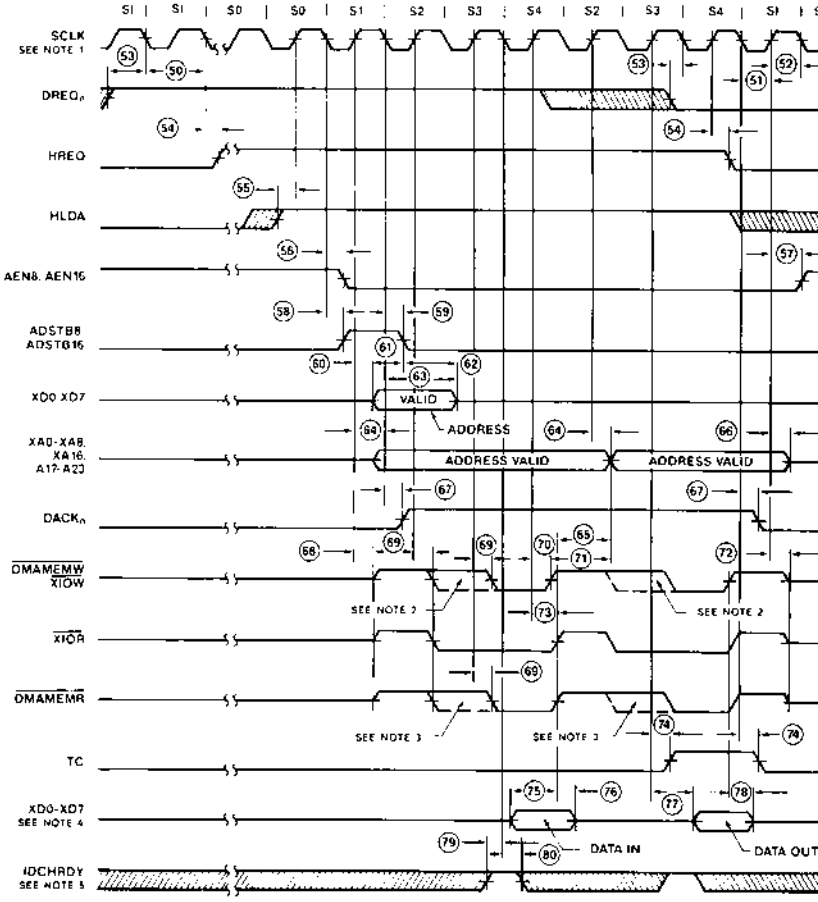



COUNTER/TIMER PARAMETERS




DMA RESET

## 82C206 TIMING DIAGRAMS

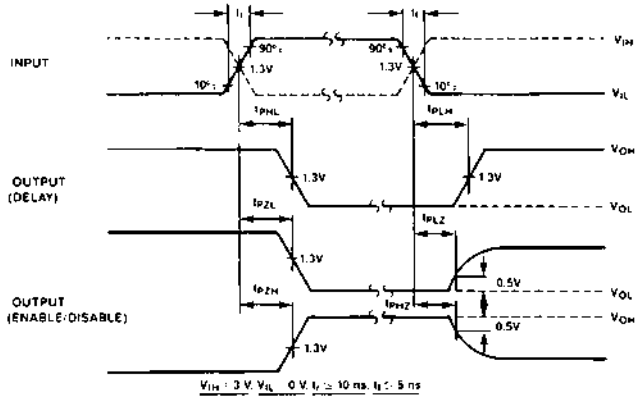



**NOTES:**

1. All timings referenced to SCLK are independent of the state of the clock select bit in the configuration register. SCLK shown in this diagram is the undivided clock directly from the input
2. Extended Write mode selected
3. Extended Read mode selected
4. Data Bus during memory to Memory Transfer
5. IOCHRDY Input Timing

**Load Circuit Measurement Conditions**

| Parameter | Output Type | Symbol | $C_L$(pF) | $R_1$ (Ω) | $R_L$ (Ω) | $SW_1$ | $SW_2$ |
|---|---|---|---|---|---|---|---|
| Propagation Delay Time | Totem pole<br>3-state<br>Bidirectional | $t_{PLH}$<br>$t_{PHL}$ | 50 | — | 1.0K | OFF | ON |
| Propagation Delay Time | Open drain or Open Collector | $t_{PLH}$<br>$t_{PHL}$ | 50 | 0.5K | — | ON | OFF |
| Disable Time | 3-state<br>Bidirectional | $t_{PLZ}$<br>$t_{PHZ}$ | 5 | 0.5K | 1.0K | ON<br>OFF | <br>ON |
| Enable Time | 3-state<br>Bidirectional | $t_{PZL}$<br>$t_{PZH}$ | 50 | 0.5K | 1.0K | ON<br>OFF | ON<br>ON |



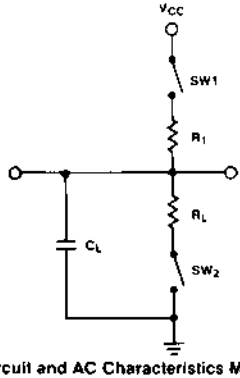
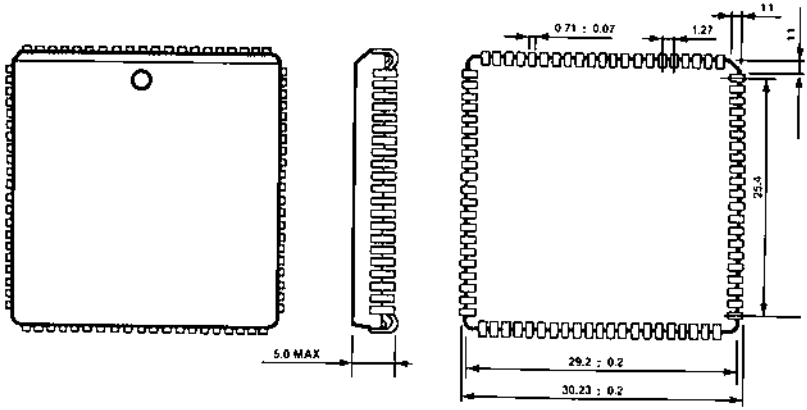




**Figure 10. Load Circuit and AC Characteristics Measurement Waveform**

84-PIN PLASTIC LEADED CHIP CARRIER

UNIT (mm)




## Ordering Information

| Order Number | Package Type | Operating Range |
|---|---|---|
| P82C206 | PLCC-84 | C (Note 1) |

NOTE:
1. PLCC-84 Plastic Leaded Chip Carrier 84-Pin Package
   C = Commercial Range, 0-70° C, ±5% Supply Voltage

CHIPS

CHIPS

Chips and Technologies, Incorporated
521 Cottonwood Drive, Milpitas, CA 95035 408-434-0600 Telex 272929 CHIPS UR

IBM, AT are the trademarks of International Business Machines, San Jose.
INTEL and iAPX 86 is a trademark of Intel Corporation, Santa Clara.

MOTOROLA™ is a trademark of Motorola.

CHIPSet is a trademark of Chips and Technologies, Incorporated.

CHIPS makes no warranty for the use of its products and bears no responsibility for any errors which may appear in this document.

# CS8221 NEW ENHANCED AT (NEAT™) DATA BOOK
## 82C211/82C212/82C215/82C206 (IPC) CHIPSet™

- **100% IBM™ PC/AT Compatible New Enhanced CHIPSet™ for 12MHz to 16MHz systems**
- **Supports 16MHz 80286 operation with only 0.5–0.7 wait states for 100ns DRAMs and 12 MHz operation with 150ns DRAMs, 0 wait state 12MHz operation with 80ns DRAMs**
- **Separate CPU and AT Bus clocks**
- **Page Interleaved Memory supports single bank page mode, 2 way and 4 way page interleaved mode**
- **Integrated Lotus-Intel-Microsoft Expanded Memory Specification (LIM EMS) Memory Controller. Supports EMS 4.0.**
- **Software Configurable Command Delays, Wait states and Memory Organization**
- **Optimized for OS/2 operation**
- **Shadow RAM for BIOS and video ROM to improve system performance**
- **Complete AT/286 system board requires only 28 logic components plus memory and processor**
- **Targeted at Desktop PC/ATs, Laptops and CMOS Industrial Control Applications**
- **Available as four CMOS 84-pin PLCC or 100-pin PFP components.**

The CS8221 PC/AT compatible NEAT CHIPSet™ is an enhanced, high performance 4 chip VLSI implementation (including the 82C206 IPC) of the control logic used on the IBM™ Personal Computer AT. The flexible architecture of the NEAT CHIPSet™ allows it to be used in any 80286 based system.

The CS 8221 NEAT CHIPSet™ provides a complete 286 PC/AT compatible system.

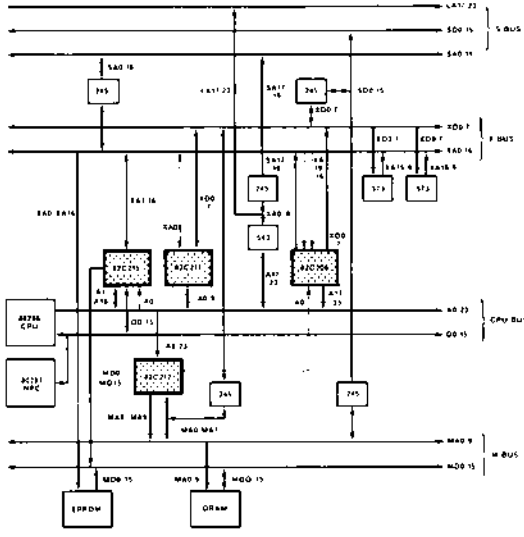



**Figure 1. NEAT System Block Diagram**

requiring only 24 logic components plus memory devices.

The CS8221 NEAT CHIPSet™ consists of the 82C211 CPU/Bus controller, the 82C212 Page/Interleave and EMS Memory controller, the 82C215 Data/Address buffer and the 82C206 Integrated Peripherals Controller (IPC).

The NEAT CHIPSet™ supports the local CPU bus, a 16 bit system memory bus, and the AT buses as shown in the NEAT System Block Diagram. The 82C211 provides synchronization and control signals for all buses. The 82C211 also provides an independent AT bus clock and allows for dynamic selection between the processor clock and the user selectable AT bus clock. Command delays and wait states are software configurable, providing flexibility for slow or fast peripheral boards.

The 82C212 Page/Interleave and EMS Memory controller provides an interleaved memory sub-system design with page mode operation. It supports up to 8 MB of on-board DRAM with combinations of 64Kbit, 256Kbit and 1Mbit DRAMs. The processor can operate at 16MHz with 0.5-0.7 wait state memory accesses, using 100 nsec DRAMs. This is possible through the Page Interleaved memory scheme. The Shadow RAM feature allows faster execution of code stored in EPROM, by down loading code from EPROM to RAM. The RAM then shadows the EPROM for further code execution. In a DOS environment, memory above 1Mb can be treated as LIM EMS memory.

The 82C215 Data/Address buffer provides the buffering and latching between the local CPU address bus and the Peripheral address bus. It also provides buffering between the local CPU data bus and the memory data bus. The parity bit generation and error detection logic resides in the 82C215.

The 82C206 Integrated Peripherals Controller is an integral part of the NEAT CHIPSet™. It is described in the 82C206 Integrated Peripherals Controller data book.

## System Overview

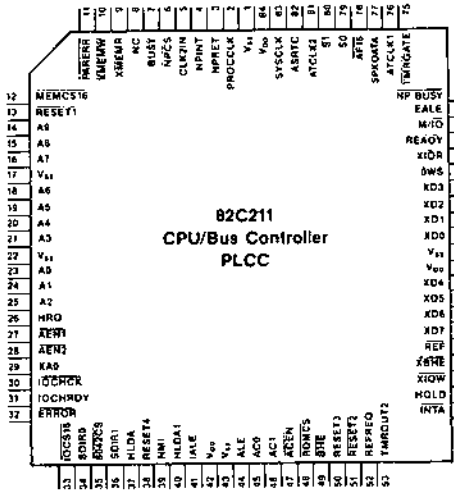
The CS8221 NEAT CHIPSet™ is designed for use in 12 to 16 MHz 80286 based systems and provides complete support for the IBM PC/AT bus. There are four buses supported by the CS8221 NEAT CHIPSet™ as shown in Figure 1: CPU local bus (A and D), system memory bus (MA and MD), I/O channel bus (SA and SD), and X bus (XA and XD). The system memory bus is used to interface the CPU to the DRAMs and EPROMs controlled by the 82C212. The I/O channel bus refers to the bus supporting the AT bus adapters which could be either 8 bit or 16 bit devices. The X bus refers to the peripheral bus to which the 82C206 IPC and other peripherals are attached in an IBM PC/AT.

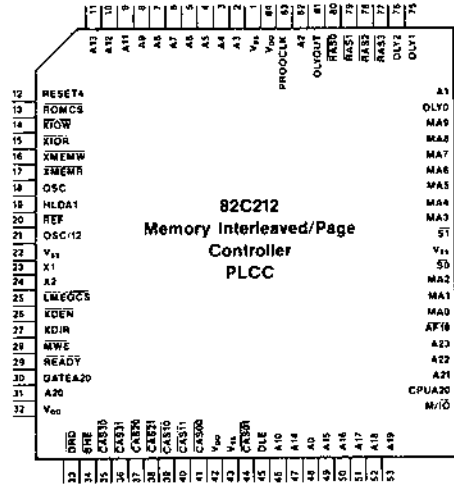
## Notation and Glossary

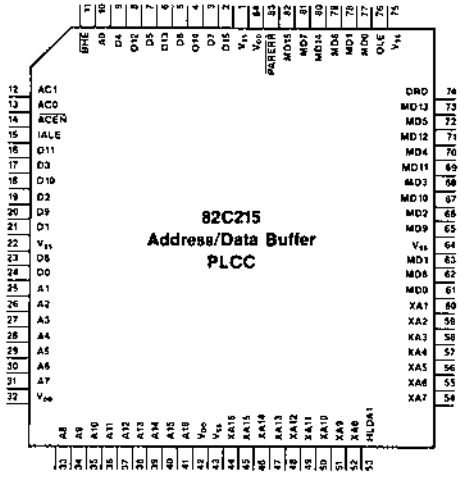
The following notations are used to refer to the configuration and diagnostics registers internal to the 82C211 and 82C212:

**REGnH** denotes the internal register of index n in hexadecimal notation.

**REGnH<x:y>** denotes the bit field from bits x to y of the internal register with index n in hexadecimal notation.


82C211
CPU/Bus Controller
PLCC
MEMCS16
RESET1
A9
A8
A7
A6
A5
A4
A3
A0
A1
A2
HRQ
AEN1
AEN2
KA9
IOCHCK
IOCHRDY
ERROR
IOCS16
SDIR0
SDIR1
HLDA
RESET4
HMI
HLDA1
IALE
ALE
AC0
AC1
ACEN
ROMCS
BHE
RESET3
RESET2
REFREQ
TMROUT2
NP BUSY
EALE
M/IO
READY
XIOR
DWS
XD3
XD2
XD1
XD0
XD4
XD5
XD6
XD7
REF
XMWE
XIOW
HOLD
INTA
HMREN
XMEMW
XMEMR
NC
BUSY
NPCS
CLK2IN
NPINT
NPRET
PROCCLK
SYSCLK
ABRTC
ATCLK2
SPKDATA
ATCLK1
TMRGATE


82C212
Memory Interleaved/Page
Controller
PLCC
RESET4
ROMCS
XIOW
XIOR
XMEMW
XMEMR
OSC
HLDA1
REF
OSC/12
X1
X2
LMEGCS
KDEN
KDIR
MWE
READY
GATEA20
A20
DRD
BHE
CAS30
CAS31
CAS20
CAS21
CAS10
CAS11
CAS00
DLE
A10
A14
A0
A15
A16
A17
A18
A19
A1
OLY0
MA9
MA8
MA7
MA6
MA5
MA4
MA3
S1
S0
MA2
MA1
MA0
AF16
A23
A22
A21
CPUA20
M/IO
A13
A12
A11
A9
A8
A7
A6
A5
A4
A3
PROCCLK
A2
OLYOUT
RAS0
RAS1
RAS2
RAS3
OLY2
OLY1


82C215
Address/Data Buffer
PLCC
BHE
A0
D4
D12
D5
D13
D6
D14
D7
D15
$V_{SS}$
$V_{DD}$
RQ/RER
MD15
MD7
MD14
MD6
MD1
MD0
OLE
$V_{SS}$
AC1
AC0
ACER
IALE
D11
D3
D10
D2
D9
D1
$V_{SS}$
D8
D0
A1
A2
A3
A4
A5
A6
A7
$V_{DD}$
A8
A9
A10
A11
A12
A13
A14
A15
A16
$V_{DD}$
$V_{SS}$
XA15
XA14
XA13
XA12
XA11
XA10
XA9
XA8
HLDA1
DRQ
MD13
MD5
MD12
MD4
MD11
MD3
MD10
MD2
MD9
$V_{SS}$
MD8
MD0
XA1
XA2
XA3
XA4
XA5
XA6
XA7

## 82C211 Pin Description

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| **Clocks** | | | |
| 5 | I | CLK2IN | CLOCK 2 input from a TTL crystal oscillator having a maximum of twice the rated frequency of the 80286 processor clock. |
| 2 | O | PROCCLK | PROCESSOR CLOCK output for the 80286 and the 82C212. It is derived from CLK2IN. It can also be programmed to be derived from ATCLK. |
| 76 | I | ATCLK1 | AT Bus Clock 1 input source from crystal or oscillator. This clock input is used for the AT bus operation and is only required if the AT bus state machine clock, BCLK (internal) will not be derived from CLK2IN. This clock input should be tied low if not used. Its frequency should be lower than CLK2IN. BCLK is the AT bus state machine clock and can be programmed to be equal to ATCLK. |
| 81 | O | ATCLK2 | AT Bus Clock 2 output is connected to the crystal (if a crystal is used to generate AT bus clock). A series damping resistor of 10 ohms should be used to reduce amplitude of the resonant circuit. It should be left open if a TTL oscillator is used. |
| 83 | O | SYSCLK | AT System Clock output is buffered to drive the SYSCLK line on the AT bus I/O channel. It is half the frequency of BCLK and should be between 6 and 8 MHz for maintaining correct AT I/O bus timing compatibility with the IBM™ PC/AT. |
| **Control** | | | |
| 13 | I | $\overline{\text{RESET1}}$ | RESET1 is an active low input generated by the power good signal of the power supply. When low, it activates RESET3 and RESET4. $\overline{\text{RESET1}}$ is latched internally. |
| 51 | I | $\overline{\text{RESET2}}$ | RESET2 is an active low input generated from the keyboard controller (8042/8742) for a "warm reset" not requiring the system power to be shut off. It forces a CPU reset by activating RESET3. |
| 38 | O | RESET4 | RESET4 is an active high output used to reset the AT bus, 82C206 IPC, 8042 keyboard controller, 82C212 memory controller. It is synchronized with the processor clock. |
| 50 | O | RESET3 | RESET3 is an active high output to the 80286 when $\overline{\text{RESET1}}$ or $\overline{\text{RESET2}}$ is active. It is also activated when shut-down condition in the CPU is detected. RESET3 will stay active for at least 16 PROCLK cycles. |

**82C211 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| **CPU Interface** | | | |
| 71 | I/O | $\overline{\text{READY}}$ | READY as an output, is driven low to terminate the current CPU cycle after IOCHRDY is high and $\overline{\text{OWS}}$ is high, or if "time out" condition is detected. During all other cycles, it is an input from the 82C212. It is an open collector output requiring an external pull-up resistor of 1KΩ and is connected to the 80286 $\overline{\text{READY}}$ pin. |
| 79, 80 | I | $\overline{\text{S0}}$, $\overline{\text{S1}}$ | STATUS is an active low input from the CPU. The status signals are used by the 82C211 to determine the state of the CPU. Pull up resistors of 10KΩ each should be provided. |
| 72 | I | M/$\overline{\text{IO}}$ | MEMORY INPUT/OUTPUT is the signal from the CPU. When high, it indicates a memory access, when low it indicates an I/O access. It is used to generate memory and I/O signals for the system. A 10KΩ pull up resistor is recommended. |
| 55 | O | HOLD | CPU HOLD REQUEST is an active high output to the CPU. It is activated during DMA, Master or refresh cycles. |
| 37 | I | HLDA | HOLD ACKNOWLEDGE is an active high input generated by the CPU to indicate to the requesting master that it has relinquished the bus. When active, it forces all commands ($\overline{\text{IOR}}$, $\overline{\text{IOW}}$, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{INTA}}$) to be tri-stated. |
| 49 | I/O | $\overline{\text{BHE}}$ | BYTE HIGH ENABLE is an active low signal which indicates the transfer of data on the upper byte of the data bus. In conjunction with A0, it is input during CPU cycles and in conjunction with XA0, it is output during DMA, MASTER cycles. A pull up resistor of 10KΩ is required. |
| 39 | O | NMI | NON MASKABLE INTERRUPT is an active high output to the NMI pin of the CPU and is generated by the 82C211 to invoke a non-maskable interrupt. |
| 41 | O | IALE | ADDRESS LATCH ENABLE (INTERNAL) is an active high output synchronized with PROCCLK and controls address latches used to hold addresses during bus cycles. It is not issued for halt bus cycles. |

**82C211 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| **I/O Channel Interface** | | | |
| 31 | I | IOCHRDY | I/O CHANNEL READY is an active high input from the AT bus. When low it indicates a not ready condition and inserts wait states in AT-I/O or AT-memory cycles. When high it allows termination of the current AT-bus cycle. A series damping resistor of 53Ω at the AT bus connector is recommended to limit the negative under shoot. A 1KΩ pull up resistor is required for this open collector line. |
| 30 | I | $\overline{\text{IOCHCK}}$ | I/O CHANNEL CHECK is an active low input from the AT bus causing an NMI to be generated if enabled. It is used to signal an I/O error condition from a device residing on the AT bus. A 10KΩ pull up resistor is required. |
| 11 | I | $\overline{\text{PARERR}}$ | PARITY ERROR is an active low input from the 82C215 which causes an NMI if enabled. It indicates a parity error in local system memory. |
| 44 | O | ALE | ADDRESS LATCH ENABLE is an active high output to the AT bus and is synchronized with the AT state machine clock. It controls the address latches used to hold the addresses during bus cycles. This signal should be buffered to drive the AT bus. |
| 73 | O | $\overline{\text{EALE}}$ | EXTERNAL ADDRESS LATCH ENABLE is an active low output used to latch the CPU A17-A23 address lines to the LA17-LA23 lines on the AT bus. |
| **DMA Interface** | | | |
| 40 | O | HLDA1 | HOLD ACKNOWLEDGE 1 is an active high output when a bus cycle is granted in response to HOLD REQUEST 1. |
| 26 | I | HRQ | HOLD REQUEST is an active high input when DMA/Master is requesting a bus cycle. For an AT compatible architecture, it should be connected to the HOLD REQUEST signal from DMA1 and DMA2. |
| 27 | I | $\overline{\text{AEN1}}$ | ADDRESS ENABLE 1 is an active low input from one of the two DMA controllers enabling the address latches for 8 bit DMA transfers. |
| 28 | I | $\overline{\text{AEN2}}$ | ADDRESS ENABLE 2 is an active low input from one of the two DMA controllers enabling the address latches for 16 bit DMA transfers. |
| 48 | I | $\overline{\text{ROMCS}}$ | ROM CHIP-SELECT is an active low input from the 82C212. It is used to disable parity checks for local ROM cycles. |

**82C211 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| **Bus Inputs** | | | |
| 12 | I | $\overline{\text{MEMCS16}}$ | MEMORY CHIP SELECT 16 is an active low input from the AT bus indicating a 16 bit memory transfer. If high it implies an 8 bit memory transfer. A pull up resistor of 330Ω is required. |
| 33 | I | $\overline{\text{IOCS16}}$ | I/O CHANNEL SELECT 16 is an active low input from the AT bus indicating a 16 bit I/O transfer. If high it implies an 8 bit I/O transfer. A pull up resistor of 330Ω is required. |
| 69 | I | $\overline{\text{0WS}}$ | ZERO WAIT STATES is an active low input from the AT bus, causing immediate termination of the current AT bus cycle. Memories requiring zero wait states use this line to speed up memory cycles. It requires a 330Ω pull up resistor. |
| **Device Decode** | | | |
| 35 | O | $\overline{\text{8042CS}}$ | 8042 CHIP SELECT is an active low signal for the keyboard controller chip select. |
| 82 | O | ASRTC | ADDRESS STROBE to Real Time Clock is an active high signal used on the 82C206. |
| **Refresh** | | | |
| 52 | I | REFREQ | REFRESH REQUEST is an active high input initiating a DRAM refresh sequence. It is generated by the 8254 compatible timer controller #1 of the 82C206 IPC in a PC/AT implementation. |
| 58 | I/O | $\overline{\text{REF}}$ | REFRESH is an active low signal. As an open drain output, it initiates a refresh cycle for the DRAMs. As an input, it can be used to force a refresh cycle from an I/O device. An external pull up of 620Ω is required. |
| **X Bus Interface** | | | |
| 9 | I/O | $\overline{\text{XMEMR}}$ | X BUS MEMORY READ is an active low control strobe directing memory to place data on the data bus. It is an output if the CPU is controlling the bus and is an input if a DMA controller is in control of the bus. |
| 10 | I/O | $\overline{\text{XMEMW}}$ | X BUS MEMORY WRITE is an active low control strobe directing memory to accept data from the data bus. It is an output if the CPU is controlling the bus and is an input if a DMA controller is in control of the bus. |

**82C211 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| 70 | I/O | $\overline{XIOR}$ | X BUS I/O READ is an active low strobe directing an I/O port to place data on the data bus. It is an output if the CPU is controlling the bus and is an input if a DMA controller is in control of the bus. |
| 56 | I/O | $\overline{XIOW}$ | X BUS I/O WRITE is an active low strobe directing an I/O port to accept data from the data bus. It is an output if the CPU is controlling the bus and is an input if a DMA controller is in control of the bus. |
| 57 | I/O | $\overline{XBHE}$ | X BYTE HIGH ENABLE is an active low signal indicating the high byte has valid data on the bus. It is an output when the CPU is in control of the bus and is an input when a DMA controller is in control of the bus. A 4.7KΩ pull-up resistor is required on this line. |
| 59-62<br>65-68 | I/O<br>I/O | XD<7:4><br>XD<0:3> | X DATA BUS bits <7:0> |
| 8 | — | NC | No Connect |
| 75 | O | TMRGATE | TIMER GATE is an active high output that enables the timer on the 8254 compatible counter timer in the 82C206 to enable the tone signal for the speaker. |
| 53 | I | TMROUT2 | TIMER OUT 2 is an active high input from the 8254 compatible counter timer in the 82C206 that can be read from port B. |
| 77 | O | SPKDATA | SPEAKER DATA is an active high output used to gate the 8254 compatible tone signal of the 82C206 to the speaker. |
| 54 | O | $\overline{INTA}$ | INTERRUPT ACKNOWLEDGE is an active low output to the 82C206 interrupt controller. It is also used to direct data from the X to S bus during an interrupt acknowledge cycle. |
| **Buffer Control** | | | |
| 34 | O | SDIR0 | SYSTEM BUS DIRECTION 0 for the low byte. A low sets the data path from the S bus to the M bus. A high sets the data path from the M bus to the S bus. |
| 36 | O | SDIR1 | SYSTEM BUS DIRECTION 1 for the high byte. A low sets the data path from the S bus to the M bus. A high sets the data path from the M bus to the S bus |
| 47 | O | $\overline{ACEN}$ | ACTION CODE ENABLE is an active low output that validates the action code signals AC<1, 0> that are used by the 82C215 address/data buffer. |

**82C211 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| 46, 45 | O | AC<1, 0> | ACTION CODE is a two bit encoded output command for bus size control and byte assembly operations performed in the 82C215. |
| **Memory Control** | | | |
| 78 | I | $\overline{AF16}$ | AF16 is an active low input indicating that the current cycle is a local bus cycle. A high indicates an AT bus cycle. A 10KΩ pull up resistor is required. |
| 23-25<br>18-21<br>14-18 | I/O | A<0:2><br>A<3:6><br>A<7:9> | ADDRESS lines A0-A9 are input from the CPU. These lines are output during refresh. A1 is used to detect shut down condition of the CPU. A0 is used to generate the enable signal for the data bus transceivers. |
| 29 | I/O | XA0 | ADDRESS line XA0 from the X bus. It is an output during CPU accesses on the X bus and is an input for 8 bit DMA cycles. |
| **CoProcessor Interface** | | | |
| 6 | O | $\overline{NPCS}$ | NUMERIC COPROCESSOR CHIP SELECT is an active low output signal used to select the internal registers of the 80287 NPX. |
| 7 | O | $\overline{BUSY}$ | BUSY is an active low output to the CPU initiated by the 80287 NPX, indicatig that it is busy. A 4.7KΩ pull up resistor is required. |
| 74 | I | $\overline{NPBUSY}$ | NUMERIC COPROCESSOR BUSY is an active low input from the NPX, indicating that it is currently executing a command. It is used to generate the BUSY signal to the CPU. A 4.7KΩ pull up resistor is required. |
| 32 | I | $\overline{ERROR}$ | ERROR is an active low input from the NPX indicating that an unmasked error condition exists. A 4.7KΩ pull up resistor is required. |
| 4 | O | NPINT | NUMERIC COPROCESSOR INTERRUPT is an active high output . It is an interrupt request from the 80287 and is connected to the IRQ13 line of the 82C206 IPC in a PC/AT environment. A 10KΩ pull up resistor is required. |

**82C211 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| 3 | O | NPRESET | NUMERICAL PROCESSOR RESET is an active high reset to the 80287. It is active when RESET4 is active or when a write operation is made to Port 0F1H. In the later case, it is active for the period of the command. |
| **Power Supplies** | | | |
| 42, 63, 84 | — | VDD | POWER SUPPLY. |
| 1, 17, 22 43, 64 | — | VSS | GROUND. |

## 82C212 Pin Description

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| **Clocks and Control** | | | |
| 83 | I | PROCCLK | PROCESSOR CLOCK input from the 82C211 |
| 23 | I | X1 | CRYSTAL 1 input from the 14.31818 MHz crystal. |
| 24 | O | X2 | CRYSTAL 2 output to the 14.31818 MHz crystal. |
| 18 | O | OSC | OSCILLATOR output for the system clock at 14.31818 MHz and has a drive capability of 24mA. |
| 21 | O | OSC/12 | OSCILLATOR divided by 12 is an output with a clock frequency equal to 1/12 of the crystal frequency across the X1, X2 pins. |
| 12 | I | RESET4 | RESET 4 is the active high reset input from the 82C211. It resets the configuration registers to their default values. When active, RAS<0:3> and CAS<00:31> remain high, OSC and OSC/12 remain inactive. |
| 20 | I | $\overline{REF}$ | REFRESH is an active low input for DRAM refresh control from the 82C211. It initiates a refresh cycle for the DRAMs. |
| 65, 63 | I | S<1, 0> | STATUS input lines from the CPU are active low. These lines are monitored to detect the start of a cycle. |
| 54 | I | M/$\overline{IO}$ | MEMORY I/O signal from the CPU. If high it indicates a memory cycle. If low, it indicates an I/O cycle. |
| 15 | I | $\overline{XIOR}$ | I/O READ command, input active low. |
| 14 | I | $\overline{XIOW}$ | I/O WRITE command, input active high. |
| 17 | I | $\overline{XMEMR}$ | X BUS MEMORY READ command, input active low. |
| 16 | I | $\overline{XMEMW}$ | X BUS MEMORY WRITE command, input active low. |
| 19 | I | HLDA1 | HOLD ACKNOWLEDGE 1 is an active high input from the 82C211. It is used to generate RAS and CAS signals for DMA cycles, in response to a hold request. |
| 13 | O | $\overline{ROMCS}$ | ROM CHIP SELECT is an active low chip select output to the BIOS EPROM. It can be connected to the output enable pin of the EPROM. |
| 48, 74, 82 | | A<0:2> | |
| 2-8 | | A<3:9> | |
| 46 | | A10 | |
| 9-11 | I | A<11:13> | ADDRESS input lines A<0:23> from the CPU local bus. |
| 47 | | A14 | |
| 49-53 | | A<15:19> | |
| 55-58 | | A<20:23> | |

**82C212 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| 34 | I | $\overline{BHE}$ | BYTE HIGH ENABLE is an active low input from the CPU for transfer of data on the upper byte. |
| 29 | I/O | $\overline{READY}$ | READY is the system ready signal to the CPU. It is an active low output after requested memory or I/O data transfer is completed. It is an input when the current bus cycle is an AT bus cycle and is an output for local memory and I/O cycles. |
| 59 | O | $\overline{AF16}$ | AF16 is an active low output asserted on local memory (EPROM or DRAM) cycles. It is high for all other cycles. This signal is sampled by the 82C211. |
| **DRAM Interface** | | | |
| 77-80 | O | $\overline{RAS}$<3:0> | ROW ADDRESS STROBES 3 to 0 are active low outputs used as $\overline{RAS}$ signals to the DRAMs for selecting different banks. $\overline{RAS3}$ selects the highest bank and $\overline{RAS0}$ selects the lowest bank. These signals should be buffered and line terminated with 75Ω resistors to reduce ringing before driving the DRAM RAS lines. |
| 41 | O | $\overline{CAS00}$ | COLUMN ADDRESS STROBE 00 is an active low output used to select the low byte DRAMs of bank 0. This signal should be line terminated with a 75Ω resistor to reduce ringing before driving the DRAM CAS line. |
| 44 | O | $\overline{CAS01}$ | COLUMN ADDRESS STROBE 01 is an active low output used to select the high byte DRAMs of bank 0. This signal should be line terminated with a 75Ω resistor to reduce ringing before driving the DRAM CAS line. |
| 39 | O | $\overline{CAS10}$ | COLUMN ADDRESS STROBE 10 is an active low output used to select the low byte DRAMs of bank 1. This signal should be line terminated with a 75Ω resistor to reduce ringing before driving the DRAM CAS line. |
| 40 | O | $\overline{CAS11}$ | COLUMN ADDRESS STROBE 11 is an active low output used to select the high byte DRAMs of bank 1. This signal should be line terminated with a 75Ω resistor to reduce ringing before driving the DRAM CAS line. |
| 37 | O | $\overline{CAS20}$ | COLUMN ADDRESS STROBE 20 is an active low output used to select the low byte DRAMs of bank 2. This signal should be line terminated with a 75Ω resistor to reduce ringing before driving the DRAM CAS line. |

**82C212 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| 38 | O | $\overline{CAS21}$ | COLUMN ADDRESS STROBE 21 is an active low output used to select the high byte DRAMs of bank 2. This signal should be line terminated with a 75Ω resistor to reduce ringing before driving the DRAM CAS line. |
| 35 | O | $\overline{CAS30}$ | COLUMN ADDRESS STROBE 30 is an active low output used to select the low byte DRAMs of bank 3. This signal should be line terminated with a 75Ω resistor to reduce ringing before driving the DRAM CAS line. |
| 36 | O | $\overline{CAS31}$ | COLUMN ADDRESS STROBE 31 is an active low output used to select the high byte DRAMs of bank 3. This signal should be line terminated with a 75Ω resistor to reduce ringing before driving the DRAM CAS line. |
| 28 | O | $\overline{MWE}$ | MEMORY WRITE ENABLE is an active low output for DRAM write enable. |
| 45 | O | DLE | DATA LATCH ENABLE is an active high output used to enable the local memory data buffer latch in the 82C215. |
| 33 | O | $\overline{DRD}$ | DATA READ is an active low output used to transfer data from the memory bus to the local CPU bus in the 82C215. If high it sets the data path from the local CPU bus to the memory bus. |
| 81 | O | DLYOUT | DELAY LINE OUT is an active high output to the delay line for generating the DRAM control signals. |
| 73, 75, 76 | I | DLY<0:2> | DELAY IN 0, 1, 2 are active high inputs from the first to third taps on the delay line used to generate DRAM control signals. |
| 26 | O | $\overline{XDEN}$ | X DATA BUFFER ENABLE is an active low output asserted during I/O accesses to locations 22H and 23H. These locations contain the index and data registers for the NEAT CHIPSet™. It is used to enable the buffers between the XD and MA buses for accessing the 82C212 internal registers. |
| 27 | O | $\overline{XDIR}$ | X BUS DIRECTION is used to control the drivers between the X and S buses. The driver should be used such that data flow is from the S to X bus when $\overline{XDIR}$ is high and in the other direction when $\overline{XDIR}$ is low. |
| 71-72 | O | MA<8:9> | MULTIPLEXED DRAM ADDRESS lines MA8, MA9. These lines should be buffered and line terminated with 75Ω resistors before driving the DRAM address lines. |

**82C212 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| 66-70<br>60-62 | I/O<br>I/O | MA<3:7><br>MA<0:2> | MULTIPLEXED DRAM ADDRESS lines MA0 to MA7. Also used as bi-directional lines to read/write to the internal registers of the 82C212. An external 74ALS245 buffer is required to isolate this path during normal DRAM operation. These lines should be buffered and line terminated with 75Ω resistors before driving the DRAM address lines. |
| **Miscellaneous** | | | |
| 31 | I/O | GA20 | ADDRESS line 20 is the gated A20 bit which is controlled by GATEA20. |
| 30 | I | GATEA20 | GATE ADDRESS 20 is an input used to force A20 low when GATEA20 is low. When high it propagates CPUA20 onto the A20 line. It is used to keep address under 1Mb during DOS operation. |
| 25 | O | $\overline{\text{LMEGCS}}$ | LOW MEG CHIP SELECT is an unlatched active low output asserted when the low Meg memory address space (0 to 1024 Kbytes) is accessed or during refresh cycles. It is used to disable $\overline{\text{SMEMR}}$ and $\overline{\text{SMEMW}}$ signals on the AT bus if accesses are made beyond the 1Mbyte address space to maintain PC and PC/XT compatibility. |
| **Power and Ground** | | | |
| 32, 42, 84 | — | VDD | POWER SUPPLY. |
| 1, 22, 43, 64 | — | VSS | GROUND. |

## 82C215 Pin Description

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| **Controls** | | | |
| 14 | I | $\overline{ACEN}$ | ACTION CODE ENABLE is an active low input from the 82C211 that validates the action codes. |
| 12, 13 | I | AC<1:0> | ACTION CODES input from the 82C211 are used for bus sizing and byte assembly operations. They are discussed in Section 1.2.4. |
| 76 | I | DLE | DATA LATCH ENABLE is an active high input from the 82C212 used to enable the local memory data buffer latch. |
| 74 | I | $\overline{DRD}$ | DATA READ is an active low input from the 82C212 used to transfer data from the M data bus to the CPU data bus. If high, it sets the data path from the CPU data bus to the M data bus. |
| 53 | I | HLDA1 | HOLD ACKNOWLEDGE 1 is an active high input from the 82C211 used for address and data direction control during DMA cycles. |
| 15 | I | IALE | ADDRESS LATCH ENABLE (INTERNAL) is an active high input from the 82C211 used to latch the CPU address lines on to the X address lines. |
| 11 | I | $\overline{BHE}$ | BYTE HIGH ENABLE is an active low input from the CPU. It is used to enable the high byte parity checking. |
| 10 | I | A0 | ADDRESS line A0 is input from the CPU. It is used to enable the low byte parity checking. |
| **Address** | | | |
| 25-31<br>33-41 | I/O<br>I/O | A<1:7><br>A<8:16> | ADDRESS lines A1-A16 from the CPU. They are input during CPU and refresh cycles and output during DMA/ Master cycles. |
| 44-52<br>54-60 | I/O<br>I/O | XA<16:8><br>XA<7:1> | X ADDRESS lines XA16-XA1 (latched) are connected to the peripheral bus in the IBM™ PC/AT architecture. |
| **Data** | | | |
| 2, 4, 6, 8, 16, 18, 20, 23, 3, 5, 7, 9, 17, 19, 21, 24 | I/O | D<15:0> | DATA lines D15-D0 from the CPU. |

**82C215 Pin Description** (Continued)

| Pin No. | Pin Type | Symbol | Description |
|---|---|---|---|
| 82, 80, 73, 71, 69, 67, 65, 62, 81, 79, 72, 70, 68, 66, 63, 61 | I/O | MD<15:0> | MEMORY DATA lines MD15-MD0 from the memory bus. |
| **Parity** | | | |
| 78, 77 | I/O | MP1, MP0 | MEMORY PARITY bits MP1, MP0 are the parity bits for the high and low order bytes of the system DRAMs. These lines are input during memory operations for parity error detection and are output during memory write operations for parity generation. |
| 83 | O | $\overline{\text{PARERR}}$ | PARITY ERROR is an active low output to the 82C211 which goes active upon detecting a parity error during a system memory read operation. It is used to generate a non-maskable interrupt to the CPU. |
| **Power and Ground** | | | |
| 32, 42, 84 | — | VDD | POWER |
| 1, 22, 43 64, 75 | — | VSS | GROUND |

# 1. 82C211 BUS CONTROLLER

## 1.1 Features

- Clock generation with software speed selection.
- Optional independent AT bus clock.
- CPU interface and bus control.
- Programmable command delays and wait state generation.
- Port B register.

## 1.2 Functional Description

The 82C211 Bus Controller consists of the following functional sub-modules as illustrated in figure 1.1:

- Reset and Shut down logic
- Clock generation and selection logic
- CPU state machine, AT bus state machine and bus arbitration logic
- Action Codes generation logic
- Port B register and NMI logic
- DMA and Refresh logic
- Numeric Coprocessor interface logic
- Configuration registers

### 1.2.1 Reset and Shut Down Logic

Two reset inputs RESET1 and RESET2 are provided on the 82C211 bus controller. RESET1 is the Power Good signal from the power supply. When RESET1 is active, the 82C211 asserts RESET3 and RESET4 for a system reset. RESET2 is generated from the 8042 (or 8742) keyboard controller when a "warm reset" is required. The warm reset activates RESET3 to reset the 80286 CPU.

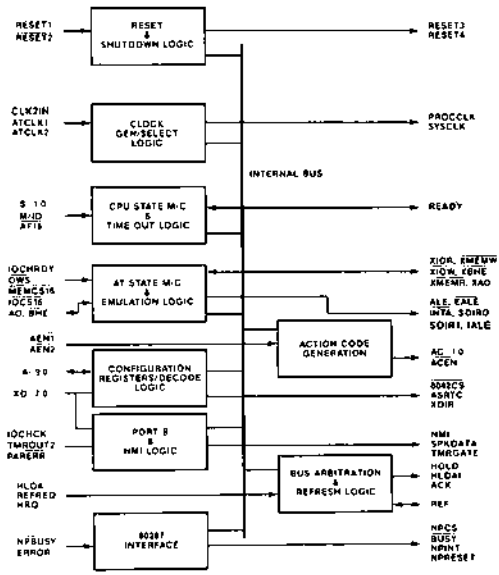



Figure 1.1 82C211 Block Diagram

RESET3 is also activated by the 82C211 when a shut down condition is detected in the CPU. Additionally, a low to high transition in REG60<5> causes RESET3 to be active after the current I/O command goes inactive. RESET3 is asserted for at least 16 PROCCLK cycles and then deasserted. RESET4 is used to reset the AT bus, 82C206 IPC, 8042 keyboard controller and the 82C212 memory controller. It is synchronized with respect to PROCCLK and is asserted as long as the Power Good signal is held low.

After a shut down condition is detected, RESET3 is asserted and held high for at least 16 PROCCLK cycles and then deasserted. RESET3 resulting from a shut down condition is synchronous with PROCCLK, ensuring proper CPU operation. Both RESET3 and RESET4 meet the setup and hold timing requirements of the 80286 CPU.

### 1.2.2 Clock Generation and Selection Logic

The 82C211 provides a flexible clock selection scheme as shown in Figure 1.2. It has two input clocks; CLK2IN and ATCLK. CLK2IN is driven from a TTL crystal oscillator, running at a maximum of twice the processor clock (PROCCLK) frequency. ATCLK is derived from a crystal. Typically, it should be of a lower frequency than CLK2IN. ATCLK and CLK2IN can be selected under program control.

The 82C211 generates processor clock, PROCCLK, for driving the CPU state machine and interface. SCLK (internal) is PROCCLK/2 and is in phase with the internal states of the 80286. BCLK (internal) is the AT bus state machine clock and is used for the AT bus interface. SYSCLK is the AT bus system clock and is always BCLK/2.

PROCCLK can be derived from CLK2IN or from ATCLK. In the synchronous mode, both PROCCLK and BCLK are derived from CLK2IN, so that the processor state machine and the AT bus state machine run synchronous. In the asynchronous mode, BCLK is generated from the ATCLK and PROCCLK is generated from CLK2IN or the ATCLK. In this case, the processor and AT bus state machines run asynchronous to each other. The following clock selections are possible:

**Synchronous mode**

1. PROCCLK = BCLK = CLK2IN
   SYSCLK = BCLK/2 = CLK2IN/2
2. PROCCLK = CLK2IN
   BCLK = CLK2IN/2
   SYSCLK = BCLK/2 = CLK2IN/4
3. PROCCLK = BCLK = CLK2IN/2
   SYSCLK = BCLK/2 = CLK2IN/4

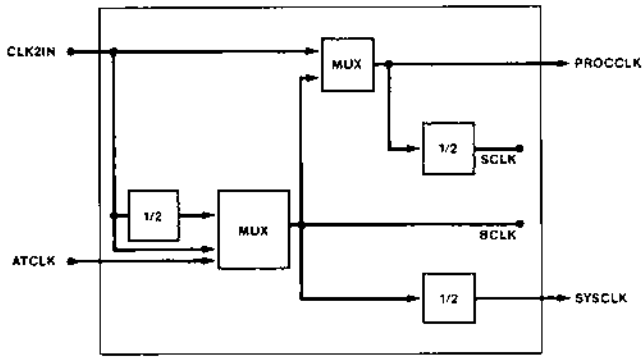



**Figure 1.2 Clock Selection Block Diagram**

**Asynchronous mode**

1. PROCCLK = CLK2IN
   BCLK = ATCLK
   SYSCLK = BCLK/2 = ATCLK/2
2. PROCCLK = ATCLK
   BCLK = ATCLK
   SYSCLK = BCLK/2 = ATCLK/2.

Under normal operation, CLK2IN should be selected as the processor clock (PROCCLK) to allow the processor to run at full speed. BCLK can either be a sub-division of CLK2IN or the ATCLK. ATCLK may be selected to generate PROCCLK only when it is desired to slow down the processor for timing dependent code execution. Once the options for clock switching are set, the switching occurs with clean transition in the asynchronous or synchronous mode. During clock switching, no phases of PROCCLK are less than the minimum value or greater than the maximum value specified for the 80286 CPU. The clock source selection is made by writing to REG62H<0:1> first and then to REG60H<4>, which default to: PROCCLK = CLK2IN, SYSCLK = CLK2IN/4.

Figures 1.3 and 1.4 illustrate the sequence of events that switch PROCCLK from high to low speed and from low to high speed, upon receiving a request from the configuration register. In Figure 1.3, the falling edge (A) of PROCCLK is used to latch the command inactive condition (1). On the falling edge (B), CLK2IN is disabled on the PROCCLK line. This ensures that clock switching will occur when PROCCLK is low. Once CLK2IN has been disabled, the first rising edge (C) of BCLK latches this condition as denoted by sequence (2). BCLK then enables itself on the PROCCLK line on the falling edge (D) as

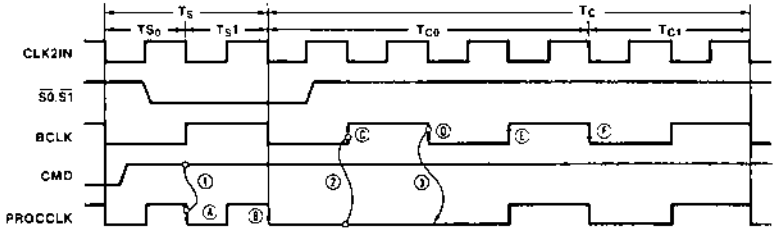



**Figure 1.3 Sequence Diagram for High to Low Frequency Transition**

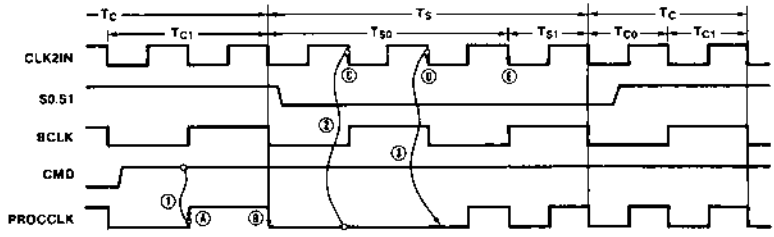



**Figure 1.4 Sequence Diagram for Low to High Frequency Transition**

denoted by sequence (3). This ensures a glitch free transition between the two clocks. It also does not violate the min and max 80286 CPU clock specifications. If BCLK is asynchronous with respect to CLK2IN, it is possible that sequence (2) could violate setup time requirements with respect to edge (C). In this case, edge (D) will register the state of PROCCLK as still being high in sequence (3). Hence, edge (E) samples PROCCLK to be low and edge (F) enables BCLK on the PROCCLK line. This case does not violate the min and max 80286 CPU clock specifications.

In Figure 1.4, the rising edge (A) of PROCCLK latches command inactive as denoted by sequence (1). Edge (B) disables BCLK on the PROCCLK line. In sequence (2), edge (C) of CLK2IN latches PROCCLK low. Edge (D) then enables CLK2IN on the PROCCLK line as denoted by sequence (3). If sequence (2) does not meet setup time requirements of edge (C), then the state of PROCCLK is sampled as being high in sequence (2). In this case, edge (D) samples PROCCLK low and edge (E) enables CLK2IN on the PROCCLK line. In this case also, PROCCLK does not violate the min and max 80286 CPU clock specifications.

### 1.2.3 CPU State Machine, Bus State Machine and Bus Arbitration

In order to extract maximum performance out of the 80286 on the system board, it is desirable to run the system board at the rated maximum CPU frequency. This frequency may be too fast for the slow AT bus. In order to overcome this problem, the 82C211 has two state machines: the CPU state machine which typically runs off CLK2IN, and the AT bus state machine which runs off BCLK. The two state machines maintain an asynchronous protocol under external mode operation.

#### CPU State Machine

Interface to the 80286 requires interpretation of the status lines $\overline{S0}$, $\overline{S1}$, M/$\overline{IO}$ during TS0 and the synchronization and generation of $\overline{READY}$ to the CPU upon completion of the requested operation. $\overline{IALE}$ is issued in response to the beginning of a new cycle in TS1 by the 82C211. If $\overline{AF16}$ is detected as being inactive at the end of the processor TS state, control is handed over to the AT bus state machine. The CPU state machine then waits for $\overline{READY}$ to be active to terminate the current cycle. All local memory cycles are 16 bit cycles. If $\overline{AF16}$ is asserted in response to a new CPU cycle and READY is not returned to the 82C211 within 128 clocks, and REG60H<2> is enabled, then an NMI is generated to signal bus time-out, if NMI has been enabled.

#### AT Bus State Machine

The AT bus state machine gains control when $\overline{AF16}$ is detected inactive by the CPU state machine. It uses BCLK which is twice the frequency of AT system clock SYSCLK. When ATCLK is selected as the source for BCLK, it also performs the necessary synchronization of control and status signals between the AT bus and the processor. The 82C211 supports 8 and 16 bit transfers between the processor and 8 or 16 bit memory or I/O devices located on the AT bus. The action codes AC0, AC1 qualified by $\overline{ACEN}$ are used for bus sizing and 8, 16 bit bus conversions by the 82C215. They are discussed in section 1.2.4.

The AT bus cycle is initiated by asserting ALE in AT-TS1. On the falling edge of ALE, $\overline{MEMCS16}$ is sampled for a memory cycle to determine the bus size. It then enters the command cycle AT-TC and provides the sequencing and timing signals for the AT bus cycle. For an I/O cycle, $\overline{IOCS16}$ is sampled in the middle of the processor TC state. These control signals emulate the lower speed AT bus signals. The command cycle is terminated when IOCHRDY is active on the AT bus and all programmed wait states have been executed.

It is possible to provide software selectable wait states and command delays to the AT state machine. Providing command delays causes the commands ($\overline{XMEMR}$ $\overline{XMEMW}$, $\overline{XIOR}$ or $\overline{XIOW}$)to be delayed from going active in BCLK steps. Providing wait states causes READY to be delayed to the CPU in steps of the AT command cycles (AT-TC). The defaults and settings are discussed in section 1.4.

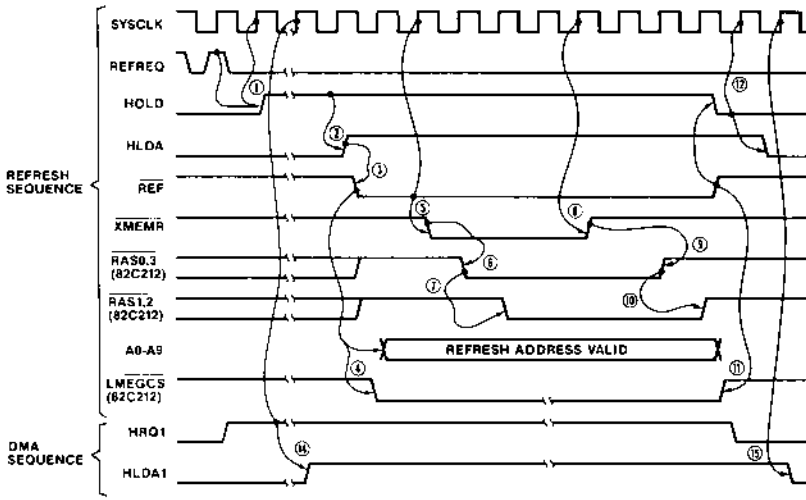



**Figure 1.5 Refresh/DMA Sequence**

**Bus Arbitration**

The 82C211 controls all bus activity and provides arbitration between the CPU, DMA/Master devices, and DRAM refresh logic. It handles HRQ and REFREQ by generating HOLD request to the CPU and arbitrating among these requests in a non-preemptive manner. The CPU relinquishes the bus by issuing HLDA. The 82C211 responds by issuing $\overline{REF}$ or HLDA1 depending on the requesting device. During a refresh cycle, the refresh logic has control of the bus until $\overline{REF}$ goes inactive. $\overline{XMEMR}$ is asserted low during a refresh cycle and the refresh address is provided on the A0-A9 address lines by the 82C211 to be used by the 82C212 memory controller. During a DMA cycle, the DMA controller has control of the bus until HRQ goes inactive. The 82C211 puts out the action codes for bus sizing. ALE, $\overline{EALE}$ and $\overline{ACEN}$ are active during DMA cycle.

Figure 1.5 is a sequence diagram for Refresh/DMA cycles. Upon receiving a refresh request (REFREQ) it is internally latched by the 82C211. On the first rising edge of SYSCLK, HOLD is output to the processor in sequence 1. Depending on the current activity of the processor, a hold acknowledge (HLDA) is issued by the processor in sequence 2, after a DMA latency time. The 82C211 responds with $\overline{REF}$ active in sequence 3. $\overline{LMEGCS}$ from the 82C212 goes active in sequence 4. $\overline{XMEMR}$ is asserted low on the second rising edge of SYSCLK after $\overline{REF}$ is low in sequence 5. The 82C212 pulls all its RAS lines (RAS0-RAS3) high when $\overline{REF}$ goes low. The RAS lines go active in sequences 6 and 7 when the refresh address is active on the A0-A9 lines of the 82C211. The 82C212 uses the A0-A9 lines to generate the refresh address on the MA0-MA9 address lines. $\overline{XMEMR}$ goes inactive in sequence 8 followed by the RAS lines going inactive in sequences 9, 10. $\overline{REF}$, $\overline{LMEGCS}$ and HOLD go inactive in sequence 11. Control is transferred to the CPU after HLDA goes inactive in sequence 12.

If a DMA device requests control of the bus,

the 82C211 receives HRQ1 active. After a DMA latency time, the CPU relinquishes the bus to the requesting device by issuing HLDA1 in sequence 14. HLDA1 is active as long as HRQ1 is active. Once the DMA device deasserts HRQ1, HLDA1 is deasserted by the 82C211 in sequence 15, to return control to the processor.

### 1.2.4 Action Codes Generation Logic

The AT state machine performs data conversion for CPU accesses to devices not on the CPU or Memory Bus.The AT bus conversions are performed for 16 to 8 bit read or write operations. Sixteen bit transfers to/from the CPU are broken into smaller 8 bit AT bus or peripheral bus reads or writes. The action codes are generated as shown in Table 1.1 to control the buffers in the 82C215. The action codes are in response to signals MEMCS16, IOCS16.

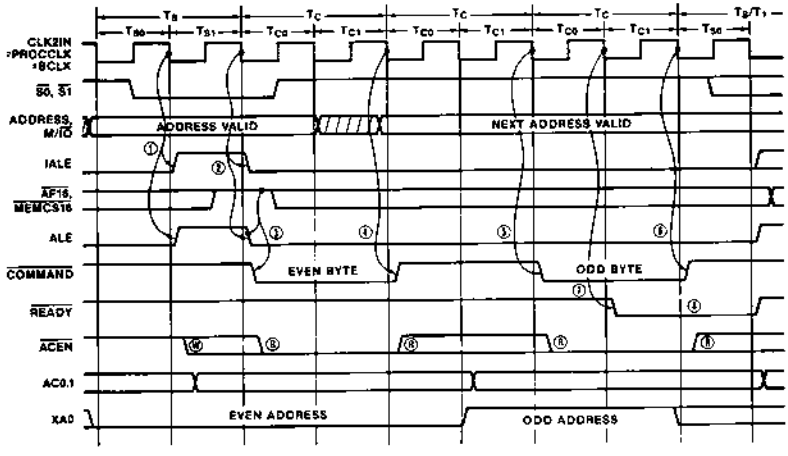
**Table 1.1**

**Action Codes Enable ($\overline{ACEN}$) Generation**

| Operation | $\overline{ACEN}$ |
|---|---|
| DMA/MASTER | 0 |
| CPU (local) | 1 |
| CPU (AT bus) | 0 for write<br>0 qualified by command for read and interrupt acknowledge cycles |
| REFRESH | 1 qualified by REF |

**AT-Bus CPU Cycles HLDA1 = 0**

| AC | Operation |
|---|---|
| 00 | 16 bit write and 8 bit write (low byte) |
| 01 | 16 bit read and 8 bit read (low byte) |
| 10 | 8 bit write (high byte) |
| 11 | 8 bit read (high byte) |




NOTE: W.S. = WAIT STATUS, C.D. = COMMAND DELAYS, R = READ CYCLE, W = WRITE CYCLE.

**Figure 1.6 Quick Mode Bus Conversion Cycle (0WS, 0CD)**

**DMA/MASTER Cycles, HLDA1 = 1**

| AC | Operation |
|---|---|
| 00 | MD bus tri-stated from the 82C215 for 16 bit and 8 (low byte) read/write operations |
| 01 | Reserved |
| 10 | High memory write MD0-7 to MD8-15 |
| 11 | High memory read MD8-15 to MD0-7 |

Figure 1.6 shows a sequence diagram for a data conversion cycle in Quick mode with zero wait states (0 W.S.) and zero command delays (0 C.D.). Quick mode is discussed in section 1.3.2. In Quick mode ALE is issued on the AT bus as shown in sequences 1 and 2. MEMCS16 from an external device is sampled high by the 82C211 in sequence 3, initiating a bus conversion cycle. The first command also goes active in sequence 3 for the first byte operation and is terminated in sequence 4. In order to provide sufficient back to back time between the two 8 bit cycles, the second byte command is issued two PROCCLKs later in sequence 5 and is terminated in sequence 6. No second ALE is issued for the second byte operation since only address line XA0 changes from zero to one. READY is asserted low in sequence 7 and is sampled low by the processor in sequence 8, to terminate the current cycle. ACEN and AC0, AC1 are issued by the 82C211 for bus conversion as shown.

### 1.2.5 Port B and NMI generation logic

The 82C211 provides access to Port B defined for the PC/AT as shown in Figure 1.7.

| IO ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| 61H | PCK | CHK | T20 | RFD | EIC | EPR | SPK | T2G | PORT B |

**Figure 1.7 Port B**

| Bits | Read/ Write | Function |
|---|---|---|
| 7 | R | PCK-System memory parity check |
| 6 | R | CHK-I/O channel check |
| 5 | R | T20-Timer 2 Out |
| 4 | R | RFD-Refresh Detect |
| 3 | R/W | EIC-Enable I/O channel check |
| 2 | R/W | ERP-Enable system memory parity check |
| 1 | R/W | SPK-Speaker Data |
| 0 | R/W | T2G-Timer 2 Gate (Speaker) |

**Table 1.2 Port B register definition**

The NMI sub-module performs the latching and enabling of I/O and parity error conditions, which will generate a non-maskable interrupt to the CPU if NMI is enabled. Reading Port B will indicate the source of the error condition (IOCK and PCHK). Enabling and disabling of NMI is accomplished by writing to I/O address 070H. On the rising edge of XIOW, NMI will be enabled if data bit 7 (XD7) is equal to 0 and will be disabled if XD7 is equal to 1.

### Numeric Coprocessor Interface

Incorporated in the 82C211 is the circuitary to interface an 80287 Numeric Coprocessor to 80286. The circuitary handles the decoding required for selecting and resetting the Numeric Coprocessor, handling NPBUSY and ERROR signals from the 80287 to the CPU, and generating interrupt signals for error handling.

The NPCS signal is active for I/O addresses 0F8H-0FFH, used to access the internal registers of the 80287. It is also active for I/O addresses 070H-NMI mask register, 0F0H-Clear Numeric Coprocessor BUSY signal, and 0F1H-Clear the Numerical Coprocessor and Numerical Coprocessor BUSY signal. While executing a task, the 80287 issues an NPBUSY

signal to the 82C211. Under normal operation, it is passed out to the CPU as $\overline{BUSY}$. If during this busy period, a numeric coprocessor error occurs, $\overline{ERROR}$ input to the 82C211 becomes active, resulting in latching of the BUSY* output and assertion of NPINT. Both signals stay active until cleared by an I/O write cycle to address 0F0H or 0F1H. A system reset clears both NPINT and $\overline{BUSY}$ latches in the 82C211. The 80287 is reset through the NPRESET output, which can be activated by a system reset or by performing a write operation to I/O port 0F1H.

### 1.3 Modes of Operation of the 82C211

The 82C211 has 4 modes of operation for different CPU and AT bus clock selections:

Normal mode
Quick mode
Delayed mode
External mode

#### 1.3.1 Normal mode

This mode is enabled by default (without writing to the internal registers of the 82C211). Under Normal mode:

PROCCLK = CLK2IN
BCLK = CLK2IN/2
SYSCLK = CLK2IN/4

Since the CPU state machine clock and the AT bus state machine clock are derived from CLK2IN, this is a synchronous mode. ALE and commands ($\overline{XMEMR}$, $\overline{XMEMW}$, $\overline{XIOR}$, $\overline{XIOW}$) are issued only for AT bus cycles and not for local cycles. If activated by default, I/O cycles will have one command delay, 8 bit AT memory cycles will have 4 wait states, 16 bit AT memory cycles will have 1 wait state.

Figure 1.8 shows the sequence diagram of a Normal mode local cycle followed by an AT bus cycle with zero wait states (0 W.S.) and

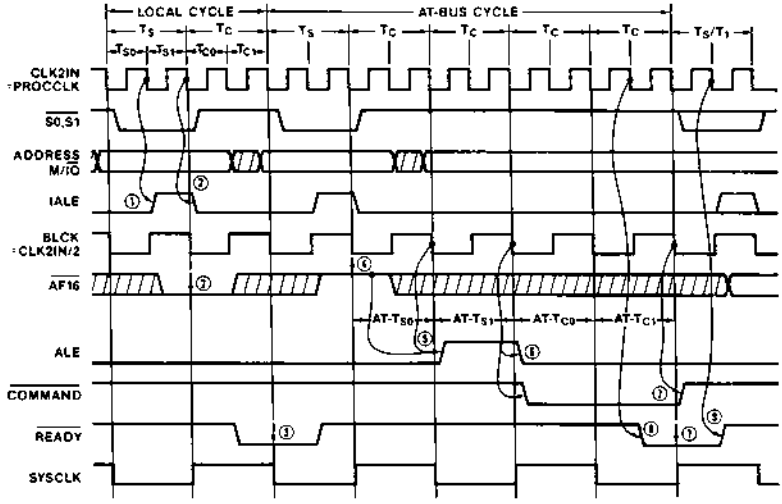
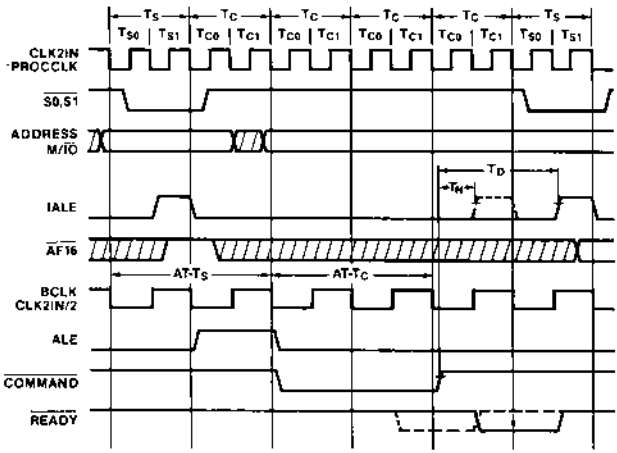



**Figure 1.8 Normal Mode Local Cycle Followed by AT Bus Cycle (0WS, 0CD)**




NOTE: TD : DELAYED HOLD TIME, TN : NORMAL HOLD TIME.

**Figure 1.9 Normal Mode AT Bus Cycle with Additional Hold Time (0WS, 0CD)**

zero command delays (0 C.D.). In sequences 1 and 2, IALE is generated from CLK2IN. AF16 is sampled to be low in sequence 2. ALE and AT buss commands (XIOR, XIOW, XMEMR, MEMW) are not generated since it is a local cycle. For a zero wait state cycle, ready is sampled low by the 80286 CPU in sequence 3 and the cycle is terminated. For the AT bus cycle, AF16 is sampled high in sequence 4. Control is transferred to the AT bus state machine. BCLK then generates the AT bus states. ALE is generated in sequences 5 and 6. The AT bus command is generated in sequences 6 and 7, for zero command delays programmed in the 82C211. For a zero wait state cycle, ready is asserted low as shown in sequences 8 and 9, to be sampled by the CPU in sequence 7. This terminates the AT bus cycle.

On the AT bus, certain slow peripherals require between 50 to 60 nanoseconds between command going inactive to the next ALE going active, to provide sufficient data recovery time. The sequence diagram in Figure 1.9 shows a Normal mode AT bus cycle with additional hold time. The dotted IALE signal would have been valid, if the additional hold time register had not been enabled in RA1<7>. Instead, IALE is delayed by one $T_C$ state of the processor by asserting READY one $T_C$ cycle later. The 82C212 provides an extended DLE to the 82C215 in this mode, so that data is available to the CPU during write cycles. If this mode was not invoked, then READY would have been asserted earlier as shown by the dotted line. In Delayed mode, the 82C211 provides an extended data hold time. This additional hold time can only be programmed in the Normal mode.

### 1.3.2 Quick mode

This mode is also a synchronous mode and is enabled by writing a zero to REG61<6> and the following clock selections have been made:

PROCCLK = BCLK = CLK2IN
SYSCLK = CLK2IN/2

In Quick mode, an ALE signal is generated

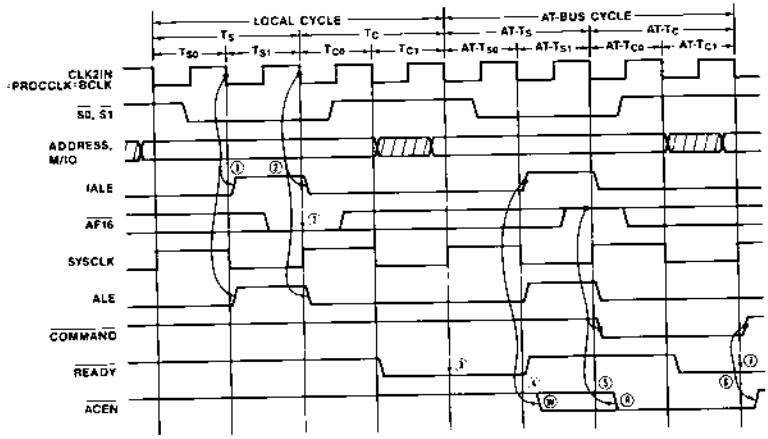



**Figure 1.10 Quick Mode Local Cycle Followed by AT Bus Cycle (0WS, 0CD)**

on the AT bus for both AT bus and local bus cycles. However, the commands (XMEMR, XMEMW, XIOR, XIOW) are not issued for local bus cycles.

The sequence diagram for a Quick mode local cycle followed by an AT bus cycle is shown in Figure 1.10. In this mode, both IALE and ALE are generated in sequences 1 and 2 for the local cycle. Hence, an ALE is issued on the AT bus for AT or non-AT bus cycles. The local cycle is terminated when READY is sampled low by the 80286 in sequence 3. For the AT bus cycle, the command is issued after AF16 is sampled high in sequence 5. For write cycles, ACEN is activated in sequence 4. For read cycles, ACEN is activated in sequence 5. If the next cycle is not an AT bus write cycle, then ACEN is negated in sequence 6. READY is sampled low by the 80286 in sequence 6, to terminate the cycle. As seen in Figure 1.10, the AT bus states coincide with the CPU states for AT bus cycles. Hence, Quick mode is performance efficient when switching between local and AT bus cycles. This mode is useful for high speed add-on cards such as Lazer Printer interface cards.

### 1.3.3 Delayed mode

This mode is another synchronous mode and is enabled when Quick mode is disabled and the following clock selections have been chosen made:

PROCCLK = CLK2IN
BCLK = CLK2IN
SYSCLK = CLK2IN/2

In Delayed mode, ALE and commands are issued only for AT bus cycles like in the Normal mode, except that BCLK = CLK2IN. ALE and commands are not issued for local cycles. Figure 1.11 shows a Delayed mode AT bus cycle. IALE is generated in sequences 1 and 2. ALE is asserted in sequence 3 after sampling AF16 high and it is deasserted in sequence 4. Hence the AT bus states, though synchronous, are delayed with respect to the processor states. Figure 1.11 is an example with two command delays and three wait states. The dotted lines A and B show command going active for 0 and 1 command delays. Sequence 5 shows command going active for programmed 2 command delays.

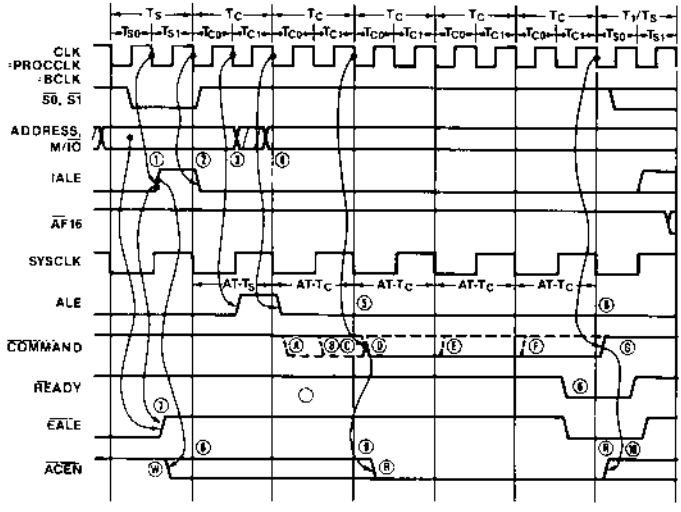



**Figure 1.11 Delayed Mode AT Bus Cycle (3WS, 2CD)**

Dotted lines D, E, F show command going inactive for 0, 1, 2 wait states. Sequence 6 shows command going inactive for programmed 3 wait states. READY is sampled by the 80286 in sequence 6 to terminate the current cycle. Since the AT bus states are delayed with respect to the processor states, the Local Address lines LA17-LA23 (typically un-latched) are not valid when ALE is active. In order to have the LA17-LA23 lines valid when ALE is active, they are latched by EALE as shown in sequence 7. Sequences 8, 9 show when ACEN is asserted for AT bus write (W) and read (R) cycles. ACEN is deasserted in sequence 10. This mode is useful for slow peripheral AT add-on cards.

### 1.3.4 External mode

This is an asynchronous mode and is enabled when ATCLK is selected as the source for BCLK. The following clock selections are required in this mode:

PROCCLK = CLK2IN
BCLK = ATCLK
SYSCLK = ATCLK/2

Since ATCLK is asynchronous to CLK2IN, the CPU state machine runs asynchronous to the AT bus state machine. ALE and commands (XMEMR, XMEMW, XIOR, XIOW) are issued only for AT bus cycles. These signals are inactive for local cycles. Figure 1.12 shows a sequence diagram for an External mode AT bus cycle. AF16 is sampled high in sequence 2 and is latched internally, using CLK2IN. The asynchronous BCLK samples this latched state on the next rising edge of BCLK. In the example shown, edge A samples the latched AF16 signal (internal) high. This causes the AT state machine to issue an ALE in sequences 3 and 4. For a zero command delay, zero wait states cycle, the command is issued on the AT bus in sequences 4 and 6, synchronized with BCLK. For write cycles, ACEN is asserted in sequence 1 and for read cycles, it is asserted in sequence 5. ACEN is deasserted in sequence 7. The command inactive state is sampled by CLK2IN on every rising edge. In this case, edge D of CLK2IN samples command high (sequence 8). It is followed by the assertion of READY in sequence 9, syn-

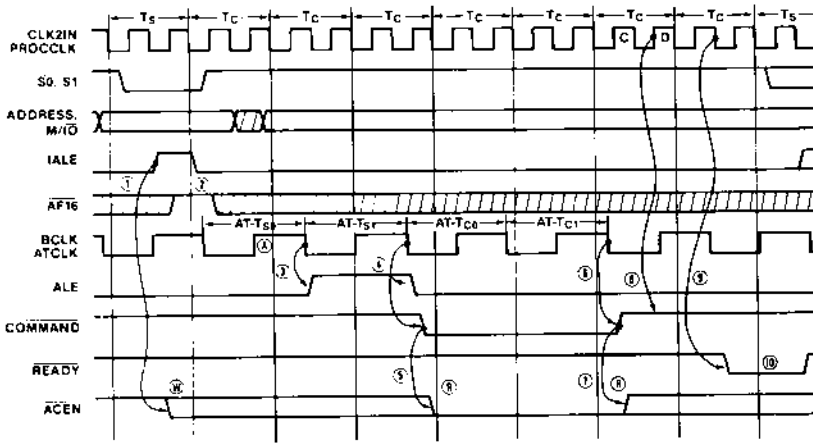



**Figure 1.12 External Mode AT Bus Cycle (0WS, 0CD)**

chronized with CLK2IN. The CPU samples READY low in sequence 10 and terminates the current cycle.

### 1.4 Configuration Registers

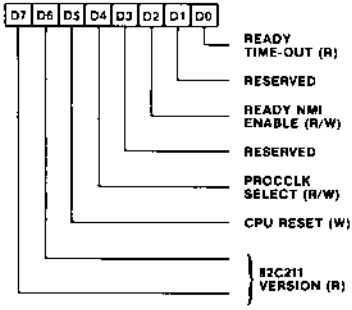
There are three bytes of configuration registers in the 82C211; RA0, RA1 and RA2. An indexing scheme is used to reduce the I/O ports required to access all the registers required for the NEAT CHIPSet. Port 22H is used as an indexing register and Port 23H is used as the data register. The index value is placed in port 22H to access a particular register and the data to be read from or written to that register is located in port 23H. Every access to port 23H must be preceded by a write of the index value to port 22H even if the same register data is being accessed again. All reserved bits are set to zero by default and when written to, must be set to zero. Table 1.3 lists the three registers:

**Table 1.3**

| Register Number | Register Name | Index |
|---|---|---|
| RA0 | PROCCLK Selector | 60H |
| RA1 | Command Delay | 61H |
| RA2 | Wait State/ BCLK Selector | 62H |

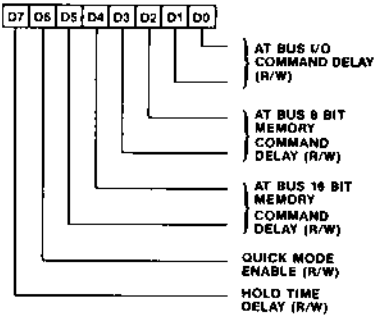
### 1.4.1 Register Description

**PROCCLK Register RA0**
Index register port: 22H
Data register port: 23H
Index: 60H



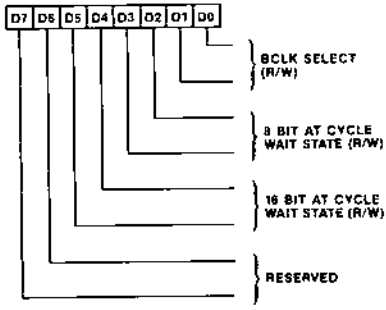

| Bits | Function |
|---|---|
| 7, 6 | 82C211 revision number. 00 is the initial number. |
| 5 | Alternate CPU reset. A low to high transition in this bit activates a CPU reset. Once active, it remains active for 16 PROCCLK cycles and then goes low. |
| 4 | Processor clock select is by default set to zero and selects PROCCLK = CLK2IN. If high, it selects PROCCLK = BCLK. |
| 3 | Reserved.* |
| 2 | Local bus READY timeout NMI enable. A one enables the NMI and a zero disables it. Default is 0 |
| 1 | Reserved.* |
| 0 | Local bus READY timeout. A one indicates that READY timeout has occurred 128 PROCCLK cycles after $\overline{AF16}$ has been asserted. A zero indicates that READY time out has not occurred. |

**Command Delay Register RA1**
Index register port: 22H
Data register port: 23H
Index: 61H




| Bits | Function |
|---|---|
| 1, 0 | AT Bus I/O cycle command delay. Specifies between 0 to 3 BCLK cycle command delays for AT I/O cycles. Default is 1. |
| 3, 2 | AT Bus 8 bit memory command delay. Specifies between 0 to 3 BCLK cycle command delays for 8 bit AT memory cycles. Default is 1. |
| 5, 4 | AT Bus 16 bit memory command delay. Specifies between 0 and 3 BCLK cycle command delays for 16 bit AT memory cycles. Default is 0 |
| 6 | Quick mode enable. A zero enables Quick mode and a one disables it. Default is 1. |
| 7 | Address hold time delay. A one enables extra address bus hold time and a zero disables it. Default is 0. |

**Wait States Register RA2**
Index register port: 22H
Data register port: 23H
Index: 62H




| Bits | Function |
|---|---|
| 1, 0 | Bus clock (BCLK) source select. Default is 00. |
| 00 | BCLK = CLK2IN/2 |
| 01 | BCLK = CLK2IN |
| 10 | BCLK = ATCLK |
| 11 | Reserved |
| 3, 2 | 8 bit AT cycle wait state generation. Default is 5. |
| 00 | 2 wait states |
| 01 | 3 wait states |
| 10 | 4 wait states |
| 11 | 5 wait states |
| 5, 4 | 16 bit AT cycle wait state generation. Default is 3. |
| 00 | 0 wait states |
| 01 | 1 wait state |
| 10 | 2 wait states |
| 11 | 3 wait states |
| 7, 6 | Reserved.* |

*The reserved bits are recommanded to be initialized to 1

### 1.5 Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | — | 7.0 | V |
| Input Voltage | $V_I$ | -0.5 | 5.5 | V |
| Output Voltage | $V_O$ | -0.5 | 5.5 | V |
| Operating Temperature | $T_{OP}$ | -25° | 85° | C |
| Storage Temperature | $T_{STG}$ | -40° | 125° | C |

**NOTE:** Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions

### 1.6 82C211 Operating Conditions

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.75 | 5.25 | V |
| Ambient Temperature | $T_A$ | 0° | 70° | C |

### 1.7 82C211 DC Characteristics

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | — | 0.8 | V |
| Input High Voltage | $V_{IH}$ | 2.0 | — | V |
| Output Low Voltage<br>$I_{OL}$ = 4mA | $V_{OL}$ | — | 0.45 | V |
| Output High Voltage<br>$I_{OH}$ = -4mA | $V_{OH}$ | 2.4 | — | V |
| Input Current<br>$0<V_{IN}<V_{CC}$ | $I_{IL}$ | — | ±10 | μA |
| Power Supply Current @ 16MHz | $I_{CC}$ | — | 50 | mA |
| Output High-Z Leakage Current<br>$0.45<V_{OUT}<V_{CC}$ | $I_{OZ1}$ | | ±10 | μA |
| PROCCLK Output Low Voltage<br>@ $I_{OL}$ = 5mA | $V_{OLC}$ | — | 0.45 | V |
| PROCCLK Output High Voltage<br>@ $I_{OH}$ = -1mA | $V_{OHC}$ | 4.0 | — | V |
| Standby Power Supply Current | $I_{CCSB}$ | — | 1.5 | mA |

## 1.8 82C211-12, 82C211-16 AC Characteristics

($T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ± 5%)

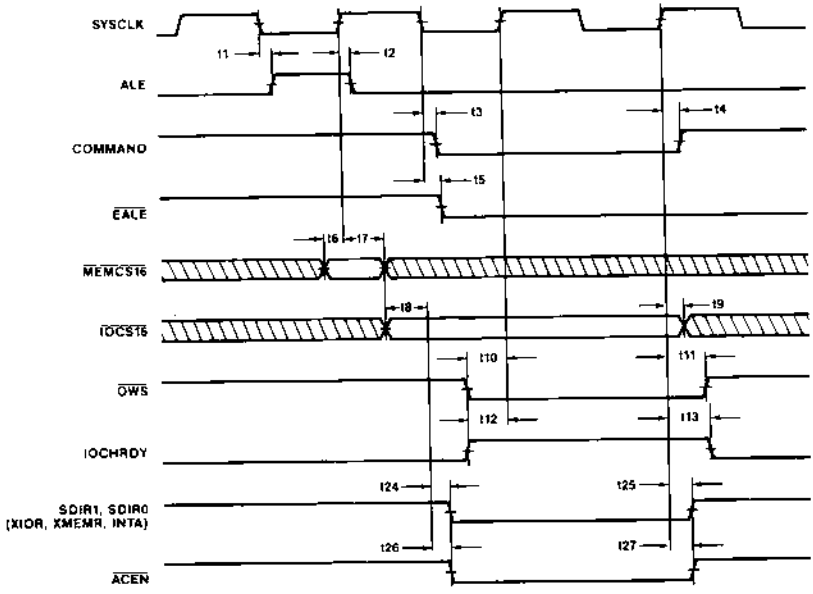
| Sym | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| t1 | ALE active delay from SYSCLKI | 1 | | 6 (10) | ns |
| t2 | ALE inactive delay from SYSCLKI | −1 | | 6 (10) | ns |
| t3 | COMMAND active delay from SYSCLKI | 0 | | 8 | ns |
| t4 | COMMAND inactive delay from SYSCLKI | 0 | | 6 | ns |
| t5 | $\overline{\text{EALE}}$ active delay from SYSCLKI | 0 | | 10 | ns |
| t6 | $\overline{\text{MEMCS16}}$ set-up time to SYSCLKI | 10 | | | ns |
| t7 | $\overline{\text{MEMCS16}}$ hold time to SYSCLKI | 4 | | | ns |
| t8 | $\overline{\text{IOCS16}}$ set-up time to SYSCLKI | 10 | | | ns |
| t9 | $\overline{\text{IOCS16}}$ hold time to SYSCLKI | 10 | | | ns |
| t10 | $\overline{\text{0WS}}$ set-up time to SYSCLKI | 9 | | | ns |
| t11 | $\overline{\text{0WS}}$ hold time to SYSCLKI | 4 | | | ns |
| t12 | IOCHRDY set-up time to SYSCLKI | 11 | | | ns |
| t13 | IOCHRDY hold time to SYSCLKI | 4 | | | ns |
| t14 | IALE active delay from PROCCLKI | 1 | | 10 | ns |
| t15 | IALE inactive delay from PROCCLKI | 1 | | 11 (16) | ns |
| t16 | $\overline{\text{AF16}}$ set-up time to PROCCLKI | 15(19) | | | ns |
| t17 | $\overline{\text{AF16}}$ hold time to PROCCLKI | 11(13) | | | ns |
| t18 | $\overline{\text{READY}}$ input set-up time to PROCCLKI | 11 | | | ns |
| t19 | $\overline{\text{READY}}$ input hold time PROCCLKI | 8 | | | ns |
| t20 | RESET3 active delay from PROCCLKI | 2 | | 12 | ns |
| t21 | RESET3 inactive delay from PROCCLKI | 2 | | 16 | ns |
| t22 | RESET4 active delay from PROCCLKI | 0 | | 8 | ns |
| t23 | RESET4 inactive delay from PROCCLKI | 1 | | 16 | ns |
| t24 | SDIR<1:0> active delay from SYSCLKI | 3 | | 11 | ns |
| t25 | SDIR<1:0> inactive delay from SYSCLKI | 1 | | 10 | ns |
| t26 | $\overline{\text{ACEN}}$ active delay from SYSCLKI | 0 | | 7 | ns |
| t27 | $\overline{\text{ACEN}}$ inactive delay from SYSCLKI | 0 | | 6 | ns |
| t32 | AC0 active delay from PROCCLKI | 6 | | 17 | ns |
| t33 | AC0 inactive delay from PROCCLKI | 6 | | 18 | ns |
| t34 | AC1 active delay from PROCCLKI | 7 | | 18 | ns |

**1.8 82C211-12, 82C211-16 AC Characteristics** (Continued)
($T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ± 5%)

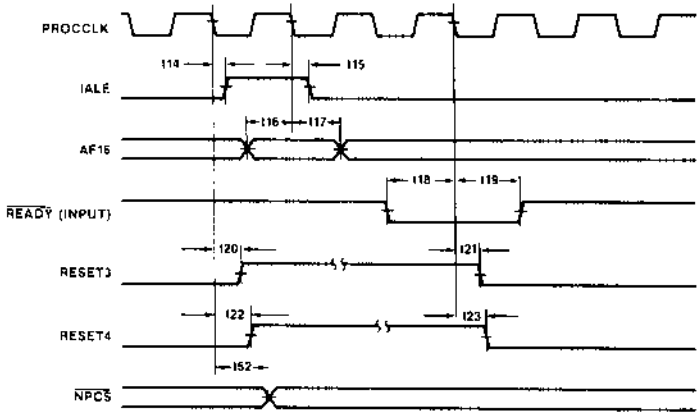
| Sym | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| t35 | AC1 active delay from PROCCLK↑ | 7 | | 18 | ns |
| t38 | Hold active delay from SYSCLK↑ | 0 | | 6 | ns |
| t39 | Hold inactive delay from SYSCLK↑ | 0 | | 6 | ns |
| t40 | $\overline{REF}$ delay from HLDA | 3 | | 14 | ns |
| t43 | $\overline{REF}$ inactive delay from SYSCLK↑ | 0 | | 6 | ns |
| t44 | XMEMR active delay from SYSCLK↑ | 1 | | 9 | ns |
| t45 | XMEMR inactive delay from SYSCLK↑ | 0 | | 5 | ns |
| t46 | HRQ1 set-up to SYSCLK↑ | 10 | | | ns |
| t47 | HRQ1 hold time to SYSCLK↑ | 4 | | | ns |
| t49 | HLDA1 active delay from HLDA↑ | 8 | | 17 | ns |
| t51 | HLDA1 inactive delay from HLDA↓ | 12 | | 20 | ns |
| t52 | $\overline{NPCS}$ active delay from PROCCLK↑ | 11 | | 21 | ns |
| t53 | Overlap of $\overline{NPBUSY}$ & $\overline{ERROR}$ (both low) | 8 | | | |
| t54 | NPINT delay from $\overline{NPBUSY}$, $\overline{ERROR}$ low | 7 | | 16 | ns |
| t55 | NPINT inactive delay from $\overline{ERROR}$↑ | 3 | | 11 | ns |
| t56 | $\overline{NPBUSY}$ active pulse width | 13 | | | |
| t57 | $\overline{ERROR}$ hold time with respect to $\overline{NPBUSY}$↑ | 0 | | | |
| t58 | $\overline{ERROR}$ set up time to $\overline{NPBUSY}$↑ | 3 | | | |
| t59 | $\overline{ERROR}$ min low pulse | 8 | | | |
| t60 | $\overline{BUSY}$ active delay from $\overline{NPBUSY}$↓ | 8 | | 18 | ns |
| t61 | $\overline{BUSY}$ inactive delay from $\overline{NPBUSY}$↑ | 8 | | 15 | ns |
| t62 | $\overline{BUSY}$ delay from $\overline{IOW}$ | 2 | | 12 | ns |
| t63 | NPRST active delay from $\overline{IALE}$ | 9 | | 19 | ns |
| t64 | NPRST inactive delay from $\overline{IALE}$ | 4 | | 15 | ns |

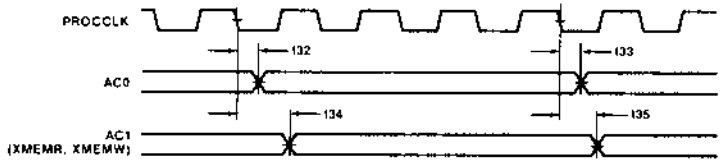
**Note:** Values inside ( ) are 12 MHz timing.

## 1.9 82C211 Timing Diagrams

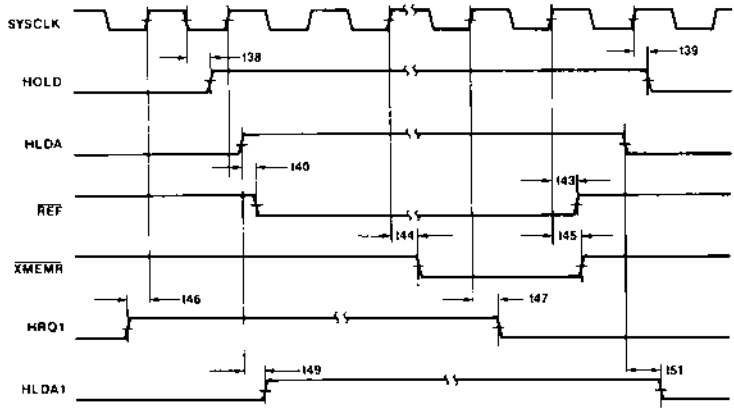


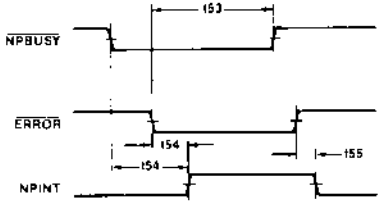
## 1.9 82C211 Timing Diagrams (Continued)



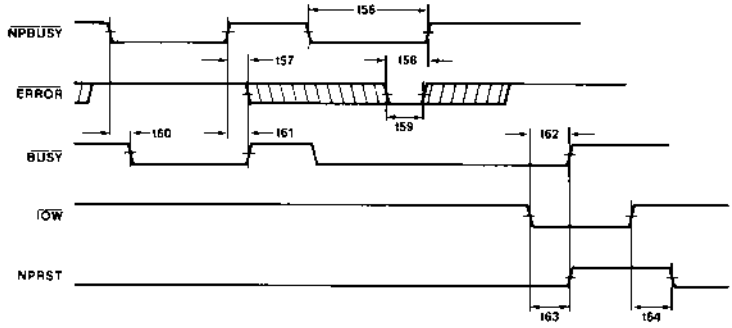



## 1.9 82C211 Timing Diagrams (Continued)



**1.9 82C211 Timing Diagrams** (Continued)



## 2 82C212 PAGE/INTERLEAVE AND EMS MEMORY CONTROLLER

### 2.1 Features

- Page mode access including single bank, 2 way and 4 way page interleaved, providing higher performance over conventional DRAM accessing schemes
- Supports 100ns DRAMs at 16MHz using page interleaved operation
- Supports up to 8Mbytes of on board memory
- Provides automatic remapping of RAM resident in 640K to 1Mbyte area to the top of the 1Mbyte address space.
- Supports Lotus Intel Microsoft-Expanded Memory System (LIM-EMS 4.0) address translation logic
- Shadow RAM feature for efficient Basic Input/Output System (BIOS) execution
- OS/2 optimization feature allows fast switching between protected and real mode
- Staggered refresh to reduce power supply noise

### 2.2 Overview

The 82C212 performs the memory control functions in the NEAT system, utilizing page mode access DRAMs. The various memory array configurations possible and Page/Interleaved mode operation are discussed in this section. Figure 2.1 is a block diagram of the 82C212 chip.

#### 2.2.1 Array Configuration

The 82C212 organizes memory as banks of 18 bit modules, consisting of 16 bits of data

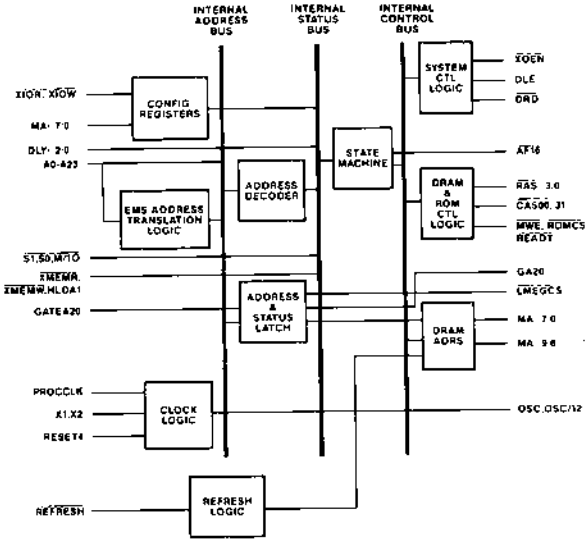



**Figure 2.1 82C212 Block Diagram**

and 2 bits of parity information. The 16 bits of data are split into high and low order bytes, with one parity bit for each byte. This configuration can be implemented by using eighteen 1-bit wide DRAMs or by using four 4-bit wide DRAMs for data with two 1-bit wide DRAMs for parity. The minimum configuration can be a single bank operating in non-interleaved mode or can be a pair of DRAM banks operating in two way interleaved mode. If the 82C212 uses a two way interleaving scheme, the DRAMs within a pair of banks must be identical. However, each bank of DRAM pairs can be different from other pairs. For example, Banks 0, 1 may have 256K by 1 bit DRAMs and Banks 2 and 3 could have 1M by 1bit DRAMs. A typical system may be shipped with one or two banks of smaller DRAM types (eg. 256K by 1 bit DRAMs) and later upgraded with additional pairs of banks of larger DRAMs (eg. 1M by 1 bit DRAMs).

### 2.2.2 Page/Interleaved Operation

The 82C212 uses a page/interleaved design that is different from most interleaved memory designs. Typical two way interleaving schemes use two banks of DRAMs with even word addresses on one bank and odd word addresses on the other bank. If memory accesses are sequential, the RAS* precharge time of one bank overlaps the access time of the other bank. Typically, programs consist of instruction fetches interspersed with operand accesses. The instruction fetches tend to be sequential and the operand accesses tend to be random.

Figure 2.2 is a sequence diagram for a memory interleaved scheme using two banks 0 and 1. The $\overline{RAS}$ signals of the two banks are interleaved so that the RAS precharge time ($T_{rp}$) of one bank is used for the $\overline{RAS}$ active time in the other bank. This requires sequential accesses to be alternating between the two banks. For non-sequential accesses, it is possible to get wait state accesses due to a 'miss'. Typically, this results in a 50% hit ratio (possible zero wait state accesses).

Figure 2.3 is a sequence diagram of a paged mode DRAM operation. In paged mode DRAMs, once a row access has been made, it

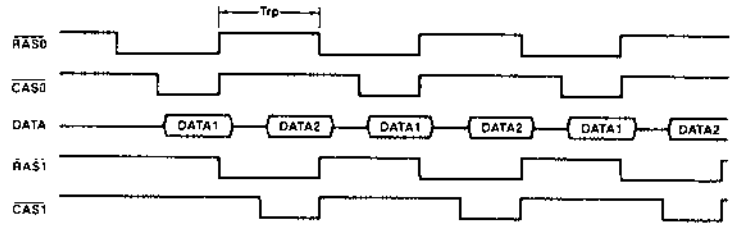



**Figure 2.2 DRAM Interleaved Operation**

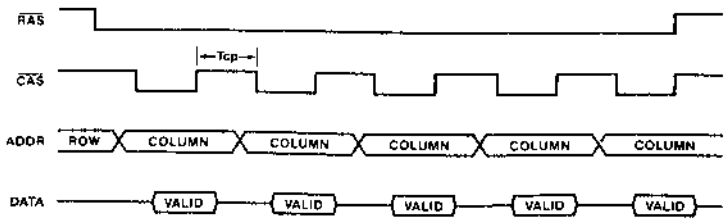



**Figure 2.3 DRAM Page Mode Operation**

is possible to access subsequent column addresses within that row, without the $\overline{RAS}$ precharge penalty. However, after a $\overline{RAS}$ active timeout, there is a $\overline{RAS}$ precharge period which typically occurs every 10 microseconds. Since the $\overline{CAS}$ precharge time $T_{cp}$ is small, it is possible to make fast random accesses within a selected row. Typically, page mode access times are half the normal DRAM access times. For 256K × 1 DRAMs, each row has 512 bits. If eighteen 256K × 1 bit DRAMs are used to implement a bank, a page would have 512 × 2 bytes (excluding 2 bits for parity) = 1 Kbytes. Thus paged mode DRAMs could be interleaved at 1 Kbyte boundaries rather than 2 byte boundaries as in the regular interleaved mode operation. Any access to the currently active $\overline{RAS}$ page would occur in a short page access time and any subsequent access could be anywhere in the same 1Kbyte boundary, without incurring any penalty due to $\overline{RAS}$ precharge. If memory is configured to take advantage of this DRAM organization, significantly better performance can be achieved over normal interleaving because:

1. Page mode access time is shorter than normal DRAM access time. This allows more time in the DRAM critical paths, to achieve penalty free accesses or 'hits'.
2. The possibility of the next access being fast is significantly higher than in a regular interleaving scheme. This is because instructions and data tend to cluster together by principle of locality of reference.

Figure 2.4 is a sequence diagram of a two way Page/Interleaved scheme using page mode DRAMs. As seen, it is possible to make zero wait state accesses between the two banks 0 and 1, by overlapping CAS precharge time of one bank with $\overline{CAS}$ active time of the other bank. The DRAM $\overline{RAS}$ lines for both banks can be held active till the $\overline{RAS}$ active time out period, at which time a $\overline{RAS}$ precharge for that bank is required. Typical hit ratios higher then 80% are possible using this scheme. With the 82C212 memory controller, using the page/interleaved scheme, 150 ns access time DRAMs can be used at 12MHz and 100 ns access time DRAMs at 16MHz.

82C212 supports both two and four way interleaved mode. If four way interleaved mode is used, the DRAMs used in the four banks must be identical. Table 2.0 shows the 0 wait state hit space for possible banks configurations.

### OS/2 Optimization

The NEAT architecture features OS/2 optimization using REG6F<1> of the 82C212 in conjunction with REG60<5> of the 82C211. OS/2 makes frequent DOS calls while operating in protected mode of the 80286 CPU. In order to service these DOS calls, the 80286 CPU has to switch from protected to real mode quickly. Typical PC/AT architectures require the processor to issue two commands to the 8042 (or 8742) keyboard controller in order to reset the processor (to switch it into protected mode) and to activate GATEA20.

REG60<5> of the 82C211 is to used to invoke a software reset to the 80286 processor and REG6F<1> is used to activate GATEA20. Since this involves two I/O writes, it is possible to execute a "Fast GATEA20". In an OS/2 environment, where frequent DOS calls are made, this feature provides significant performance improvement.

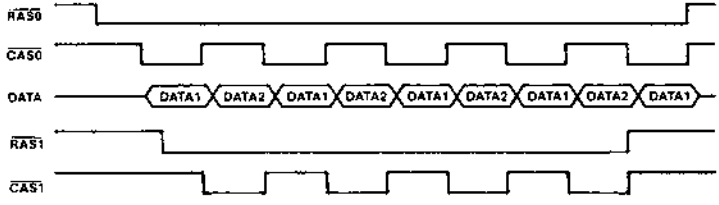



**Figure 2.4 DRAM Page/Interleave Operation**

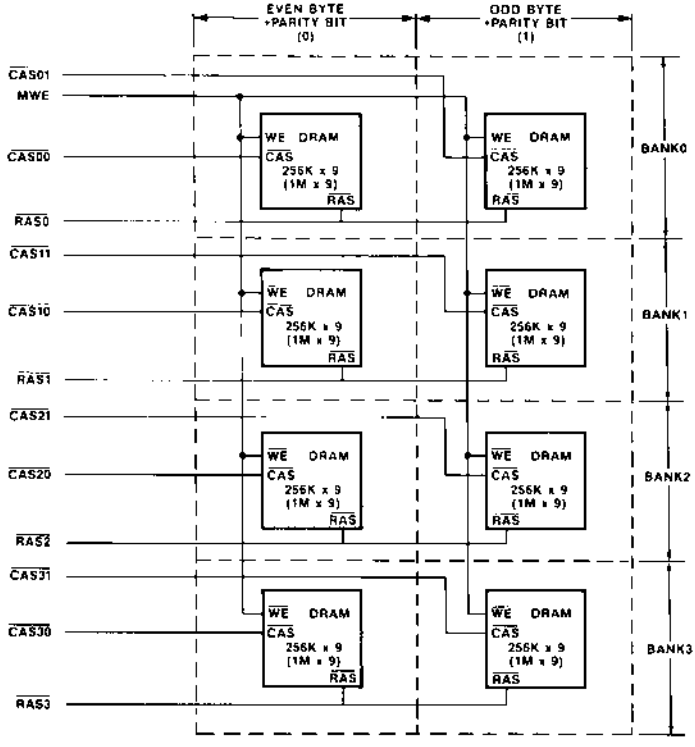



Figure 2.5 DRAM Organization

**Table 2.0 Average 0 Wait State Hit Space**

| DRAM Type | | | | | |
|---|---|---|---|---|---|
| Bank 0 | Bank 1 | Bank 2 | Bank 3 | Two Way Interleaved | Four Way Interleaved |
| 256K | 256K | 0 | 0 | 2K | NA |
| 256K | 256K | 256K | 256K | 2K | 4K |
| 256K | 256K | 1M | 1M | 3K | NA |
| 1M | 1M | 0 | 0 | 4K | NA |
| 1M | 1M | 1M | 1M | 4K | 8K |

## 2.3 Functional Description

Figure 2.1 is a block diagram of the 82C212 memory controller. It consists of the following sub-modules:

- EPROM and DRAM control logic
- System Control logic
- Memory Mapping and Refresh logic
- Oscillator clock generation logic
- Configuration registers

### 2.3.1 EPROM and DRAM Control Logic

The EPROM and DRAM control logic in the 82C212 is responsible for the generation of the $\overline{RAS}$, $\overline{CAS}$ and $\overline{MWE}$ signals for DRAM accesses and the generation of $\overline{ROMCS}$ for EPROM accesses. This sub-module also generates $\overline{READY}$ to the CPU upon completion of the desired local memory operation. The appropriate number of wait states are inserted, as programmed by software (or by default) in the wait state register of the 82C212. Figure 2.5 is a block diagram of the DRAM organization for the NEAT architecture. As seen, each $\overline{RAS}$ line drives each 256K × 18 bit bank (or 1M × 18 bit bank). The $\overline{CAS}$ lines are used to drive individual bytes within each bank. $\overline{MWE}$ is connected to each DRAM bank write enable input.

### 2.3.2 System Control Logic

This sub-module of the 82C212 generates $\overline{XDEN}$, DLE, $\overline{DRD}$, $\overline{AF16}$ for system control. $\overline{XDEN}$ is issued for I/O accesses to the internal registers of the 82C212. It is used to enable the XD0-7 lines onto the MA0-7 lines from an external buffer, for accessing the internal registers of the 82C212. The DLE and DRD signals are generated for enabling and controlling the direction of data between the CPU data bus and the memory data bus (MD bus). $\overline{AF16}$ is issued by the 82C212 state machine. It is active for local memory accesses and meets the set up and hold times with respect to PROCCLK for the 82C211.

### 2.3.3 Memory Mapping and Refresh logic

The 82C212 has an extensive set of memory mapping registers for various memory organizations. The registers are discussed in section 2.3.5. Through the memory mapping logic, for up to 1 Mbyte of system RAM, it is possible to map RAM that overlaps the EPROM area (640Kbyte-1Mbyte) above the 1Mbyte area, as shown in Figure 2.6. Hence, for 1Mbyte of on board RAM, the software can address it from 0 to 640 Kbytes and from 1 Mbyte to 1.384 Mbytes. The EPROM can be addressed from the 640 Kbyte area to the 1 Mbyte area.

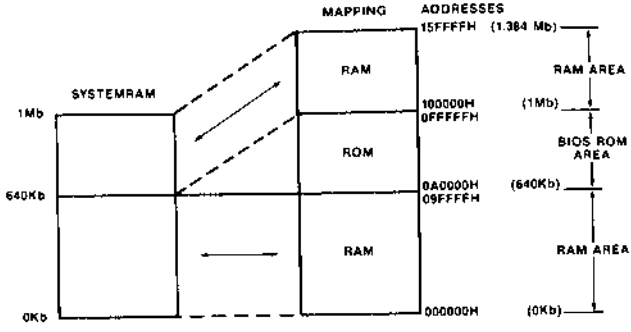



Figure 2.6 System RAM/ROM Mapping for 1MB System RAM

For normal mode of operation, only one bank of DRAMs may be used. However, for the page/interleaved mode of operation, RAM bank pairs must be used.

**Shadow RAM Feature**

For efficient execution of BIOS, it is preferable to execute BIOS code through RAM rather than through slower EPROMs. The 82C212 provides the shadow RAM feature which if enabled allows the BIOS code to be executed from system RAM resident at the same physical address as the BIOS EPROM. The software should transfer code stored in the BIOS EPROMs to the system RAM, before enabling the shadow RAM feature. This feature significantly improves the performance in BIOS-call intensive applications. Performance improvements as high as 300 to 400% have been observed in benckmark tests on the shadow RAM. The shadow RAM feature is invoked by enabling the corresponding bits in the ROM enable register and the RAM mapping register.

If more than 1 Mbyte of system RAM exists, it is mapped as shown in Figure 2.7, if the shadow RAM feature is not invoked. This means that RAM in the 640 Kbyte to 1 Mbyte area cannot be accessed. If the shadow RAM feature is used, then the RAM is mapped as

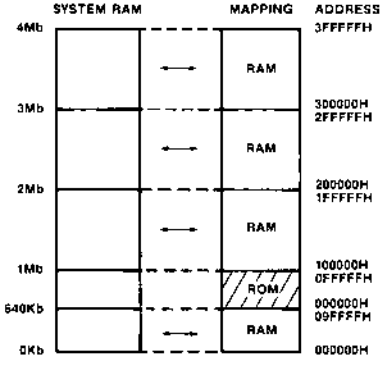



**Figure 2.7 RAM/ROM Mapping Without Shadow RAM (More Than 1MB of RAM)**

shown in Figure 2.8, overlapping or Shadowing the EPROM area. In both cases, for accesses beyond the 1 Mbyte address range, the processor is switched from real to protected mode from BIOS.

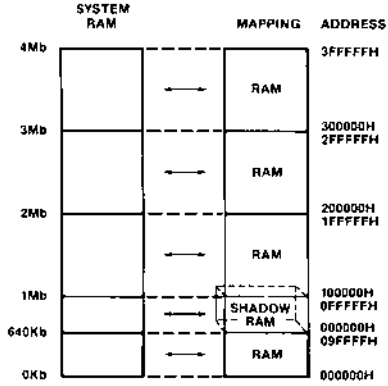



**Figure 2.8 RAM Mapping with Shadow RAM (More Than 1MB of RAM)**

**EMS Address Translation Logic**

Expanded Memory System or EMS is a memory mapping scheme used to map a 64 Kbyte block of memory in the EPROM area D0000H-DFFFFH to anywhere in the 1 Mbyte-8 Mbyte area. This 64 Kbyte memory block is segmented into four 16 Kbyte pages. Through a translation table, each 16 Kbyte segment can be mapped anywhere in the 1 Mbyte to 8 Mbyte area. Since the 82C212 uses the translation table in the EMS mode, address lines A14 to A22 are translated by the appropriate EMS mapping register. Hence, this scheme does not require switching between user and protected mode. Figure 2.9 shows the EMS organization with a possible translation scheme. It is possible for the 82C212 to map this 64 Kbyte block to anywhere in the 0 to 8 Mbyte area. However, it is desirable to map this block above the 1 Mbyte area in order to not use the RAM space in the 0 to 640 Kbyte area. Although the EMS scheme translates the 64 Kbyte block in the D0000H-DFFFFH

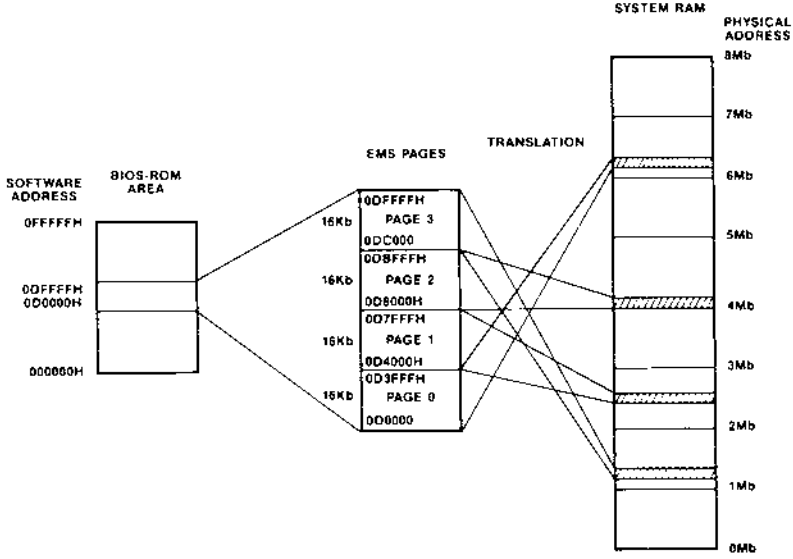



**Figure 2.9 EMS Mapping**

area, it is possible to select a 64 Kbyte block from any other area.

### Refresh Logic

During a refresh cycle, the 82C211 puts out the refresh address on the A0-A9 address lines and asserts the $\overline{REF}$ signal low to the 82C212. The 82C212 uses these signals to generate the refresh address on the MA0-MA9 address lines, the $\overline{RAS}$ signals and $\overline{LMEGCS}$. Figure 1.5 is a sequence diagram for a refresh cycle. As seen, the 82C212 performs a staggered mode refresh to reduce the power supply noise generated during $\overline{RAS}$ switching. Prior to a refresh, all $\overline{RAS}$ lines are pulled high to ensure $\overline{RAS}$ precharge. Following this, $\overline{RAS0}$ and $\overline{RAS3}$ are asserted low. $\overline{RAS1}$ and $\overline{RAS2}$ are staggered by one delay unit using an external delay line, with respect to $\overline{RAS0}$ and $\overline{RAS3}$. The $\overline{RAS0}$-$\overline{RAS3}$, $\overline{RAS1}$-$\overline{RAS2}$ bundling is provided so that staggering is effective for a minimal 2 bank or a full 4 bank configuration.

### Memory Configurations

It is possible to use 1Mbit or 256K bit (and in one case, 64K bit) DRAMs for system memory in the NEAT CHIPSet™. Each memory bank can be implemented with eighteen 1 bit wide DRAMs or four 4 bit wide DRAMs with two 1 bit wide DRAMs. Possible configurations for onboard memory are listed in Table 2.1. Each bank is 16 bits wide plus two bits for parity.

Table 2.1

| | DRAM Type | | | | Total | EMS |
|---|---|---|---|---|---|---|
| | Bank0 | Bank1 | Bank2 | Bank3 | Memory | Range |
| 1 | 0 | 0 | 0 | 0 | disable | 0 |
| 2 | 256K | 0 | 0 | 0 | 512Kb | 0 |
| 3 | 1M | 0 | 0 | 0 | 2Mb | 1Mb to 2Mb |
| 4 | 256K | 64K | 0 | 0 | 640Kb | 0 |
| 5 | 256K | 256K | 0 | 0 | 1Mb | 1Mb to 1.384Mb |
| 6 | 1M | 1M | 0 | 0 | 4Mb | 1Mb to 4Mb |
| 7 | 256K | 256K | 256K | 0 | 1.5Mb | 1Mb to 1.5Mb |
| 8 | 256K | 256K | 1M | 0 | 3Mb | 1Mb to 3Mb |
| 9 | 1M | 1M | 1M | 0 | 6Mb | 1Mb to 6Mb |
| 10 | 256K | 64K | 256K | 256K | 1.64Mb | 1Mb to 1.64Mb |
| 11 | 256K | 256K | 256K | 256K | 2Mb | 1Mb to 2Mb |
| 12 | 256K | 64K | 1M | 1M | 4.64Mb | 1Mb to 4.64Mb |
| 13 | 256K | 256K | 1M | 1M | 5Mb | 1Mb to 5Mb |
| 14 | 1M | 1M | 1M | 1M | 8Mb | 1Mb to 8Mb |

Page/interleaving is possible for only those combinations with similar pairs of DRAMs. In table 2.1, page/interleaving is possible with combinations 5, 6, 11, 13 and 14.

## 2.4 Clock Generation Logic

The 82C212 has an oscillator circuit which uses a 14.31818 MHz crystal to generate the OSC and OSC/12 clocks. The 1.19381 MHz OSC/12 clock is used internally to generate the $\overline{RAS}$ timeout clocks, one for each bank. $\overline{RAS}$ is deasserted for each bank when its $\overline{RAS}$ time out counter times out after about 10 microseconds.

## 2.5 Configuration Registers

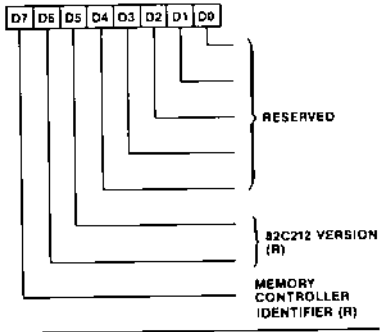
There are twelve configuration and diagnostics registers in the 82C212, RB0-RB11. These are accessed through IO ports 22H and 23H normally found in the interrupt controller module of the 82C206 IPC. An indexing scheme is used to reduce the number of I/O addresses required to access all of the registers needed to configure and control the memory controller. Port 22H is used as an index register that points to the required data value accessed through port 23H. A write of the index value for the required data is performed to location 22H. This is then decoded and controls the multiplexers gating the appropriate register to the output bus. Every access to port 23H must be preceded by a write of the index value to port 22H even if the same data register is being accessed again. All bits marked as Reserved are set to zero by default and must be maintained that way during write operations. Table 2.2 lists these registers.

**Table 2.2**

| Register Number | Register Name | Index |
|---|---|---|
| RB0 | Version | 64H |
| RB1 | ROM Configuration | 65H |
| RB2 | Memory Enable-1 | 66H |
| RB3 | Memory Enable-2 | 67H |
| RB4 | Memory Enable-3 | 68H |
| RB5 | Memory Enable-4 | 69H |
| RB6 | Bank 0/1 Enable | 6AH |
| RB7 | DRAM Configuration | 6BH |
| RB8 | Bank 2/3 Enable | 6CH |
| RB9 | EMS Base Address | 6DH |
| RB10 | EMS Address Extension | 6EH |
| RB11 | Miscellaneous | 6FH |

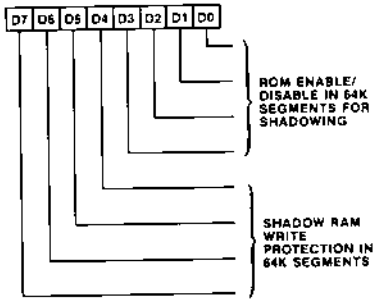
### 2.5.1 Register Description

**Version Register RB0**
Index register port: 22H
Data register port: 23H
Index: 64H



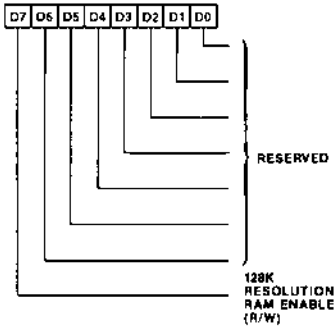

| Bits | Function |
|---|---|
| 7 | NEAT memory controller identifier. 0 = 82C212 |
| 6, 5 | 82C212 revision number. 00 = initial revision number |
| 4-0 | Reserved and default to 0' |

**ROM Configuration Register RB1**
Index register port: 22H
Data register port: 23H (R/W)
Index: 65H



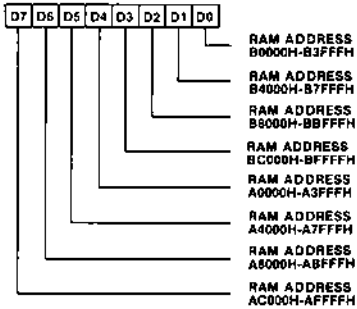

| Bits | Function |
|---|---|
| 0 | ROM at F0000H-FFFFFH (BIOS). Default = 0 = ROM enabled. ROMCS is generated. |
| 1 | ROM at E0000H-EFFFFH. Default = 1 = ROM disabled. Shadow RAM enabled. ROMCS is not generated unless bit is set to 0. |
| 2 | ROM at D0000H-DFFFFH. Default = 1 = ROM disabled. Shadow RAM enabled. ROMCS is not generated unless bit is set to 0. |
| 3 | ROM at C0000H-CFFFFH (EGA). Default = 1 = ROM disabled. Shadow RAM enabled. ROMCS is not generated unless bit is set to 0. |
| 4 | Shadow RAM at F0000H-FFFFFH in Read/Write mode. 0 = Read/Write (default). 1 = Read only (Write protected). |
| 5 | Shadow RAM at E0000H-EFFFFH in Read/Write mode. 0 = Read/Write (default). 1 = Read only (Write protected). |
| 6 | Shadow RAM at D0000H-DFFFFH in Read/Write mode. 0 = Read/Write (default). 1 = Read only (Write protected). |
| 7 | Shadow RAM at C0000H-CFFFFH in Read/Write mode. 0 = Read/Write (default). 1 = Read only (Write protected). |

**Memory Enable-1 Register RB2**
Index register port: 22H
Data register port: 23H
Index: 66H



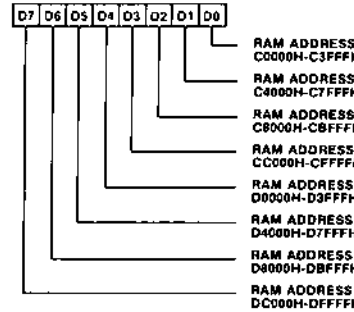

| Bits | Function |
|---|---|
| 0-6 | Reserved and default to 0' |
| 7 | Address map RAM on system board in 80000H-9FFFFH area. 0 = Address is on the I/O channel (Default), 1 = Address is on the system board and is put out by the 82C212. |

**Memory Enable Register-2 RB3**
Index register port: 22H
Data register port: 23H (R/W)
Index: 67H




| Bits | Function |
|---|---|
| 0 | Enable Shadow RAM in B0000H-B3FFFH area. Disable = 0 Enable = 1. |
| 1 | Enable Shadow RAM in B4000H-B7FFFH rea. Disable = 0 Enable = 1. |
| 2 | Enable Shadow RAM in B8000H-BBFFFH area. Disable = 0 Enable = 1. |
| 3 | Enable Shadow RAM in BC000H-BFFFFH area. Disable = 0 Enable = 1. |
| 4 | Enable Shadow RAM in A0000H-A3FFFH area. Disable = 0 Enable = 1. |
| 5 | Enable Shadow RAM in A4000H-A7FFFH area. Disable = 0 Enable = 1. |
| 6 | Enable Shadow RAM in A8000H-ABFFFH area. Disable = 0 Enable = 1. |
| 7 | Enable Shadow RAM in AC000H-AFFFFH area. Disable = 0 Enable = 1. |

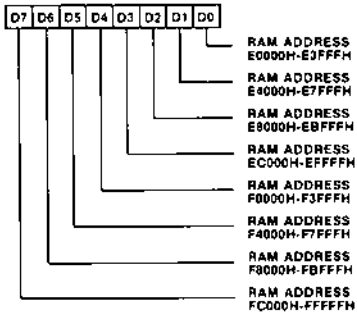
**Memory Enable-3 Register RB4**
Index register port: 22H
Data register port: 23H (R/W)
Index: 68H




| Bits | Function |
|---|---|
| 0 | Enable Shadow RAM in C0000H-C3FFFH area. Disable = 0 Enable = 1. |
| 1 | Enable Shadow RAM in C4000H-C7FFFH area. Disable = 0 Enable = 1. |

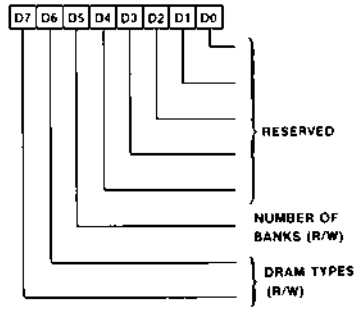
| | |
|---|---|
| 2 | Enable Shadow RAM in C8000H-CBFFFH area. Disable = 0 Enable = 1. |
| 3 | Enable Shadow RAM in CC000H-CFFFFH area. Disable = 0 Enable = 1. |
| 4 | Enable Shadow RAM in D0000H-D3FFFH area. Disable = 0 Enable = 1. |
| 5 | Enable Shadow RAM in D4000H-D7FFFH area. Disable = 0 Enable = 1. |
| 6 | Enable Shadow RAM in D8000H-DBFFFH area. Disable = 0 Enable = 1. |
| 7 | Enable Shadow RAM in DC000H-DFFFFH area. Disable = 0 Enable = 1. |

**Memory Enable-4 Register (RB5)**
Index register port: 22H
Data register port: 23H (R/W)
Index: 69H




| Bits | Function |
|---|---|
| 0 | Enable Shadow RAM in E0000H-E3FFFH area. Disable = 0 Enable = 1. |
| 1 | Enable Shadow RAM in E4000H-E7FFFH area. Disable = 0 Enable = 1. |
| 2 | Enable Shadow RAM in E8000H-EBFFFH area. Disable = 0 Enable = 1. |
| 3 | Enable Shadow RAM in EC000H-EFFFFH area. Disable = 0 Enable = 1. |
| 4 | Enable Shadow RAM in F0000H-F3FFFH area. Disable = 0 Enable = 1. |
| 5 | Enable Shadow RAM in F4000H-F7FFFH area. Disable = 0 Enable = 1. |
| 6 | Enable Shadow RAM in F8000H-FBFFFH area. Disable = 0 Enable = 1. |
| 7 | Enable Shadow RAM in FC000H-FFFFFH area. Disable = 0 Enable = 1. |

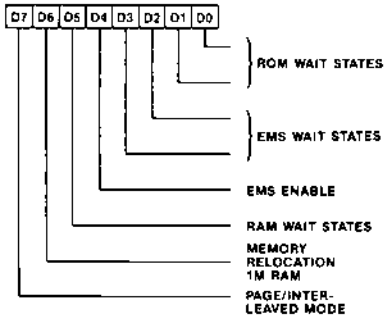
**Bank 0/1 Enable Register RB6**
Index register port: 22H
Data register port: 23H
Index: 6AH




| Bits | Function |
|---|---|
| 0-4 | Reserved and default to 0* |
| 5 | Number of RAM banks used. 0 = one bank, non-interleaved mode (Default), 1 = two banks |
| 7, 6 | These bits contain the information for the DRAM types used on the system board. POST/BIOS should use the DRAM configuration data stored in the CMOS RAM of the 82C206 IPC. |

| 7 | 6 | DRAM Types |
|---|---|---|
| 0 | 0 | Disabled |
| 0 | 1 | 256K and 64K bit DRAMs used (for 640 Kbyte combination only) |
| 1 | 0 | 256K bit DRAMs used (Default) |
| 1 | 1 | 1M bit DRAMs used |

**DRAM Configuration Register RB7**
Index register port: 22H
Data register port: 23H (R/W)
Index: 6BH




| Bits | Function |
|---|---|
| 1, 0 | ROM access wait states control. |

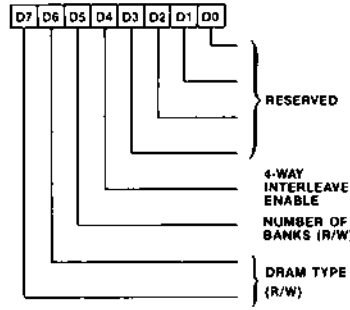
| 1 | 0 | Wait States |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 (Default) |

| Bits | Function |
|---|---|
| 3, 2 | EMS memory access wait states. |

| 3 | 2 | Wait States |
|---|---|---|
| 0 | 0 | 0 |

| Bits | Function |
|---|---|
| 4 | EMS enable bit.If set to 0, EMS is disabled (Default). If set to 1, EMS is enabled. |
| 5 | RAM access wait states. If set to 0, accesses have 0 wait state. If set to 1 (Default), accesses will have 1 wait state. |
| 6 | 640Kbyte to 1Mbyte RAM relocation bit. A zero does not relocate local RAM. A one (Default) relocates local RAM from 0A0000-0FFFFF to 100000H-15FFFFH, provided total local RAM is 1 Mbyte only. |
| 7 | Page/Interleaved mode enable. A 0 disables the page/interleaved mode, allowing useage of normal mode for the DRAMs (Default). A 1 enables page/interleaved mode for the DRAMs. |

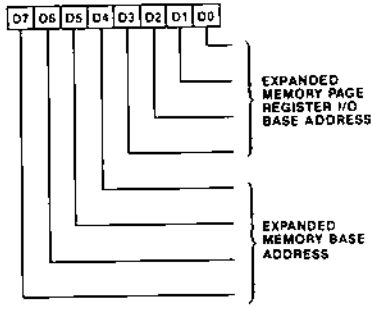
**Bank 2/3 Enable Register RB8**
Index register port: 22H
Data register port: 23H
Index: 6CH




| Bits | Function |
|---|---|
| 0-3 | Reserved and default to 0* |
| 4 | A zero enable the 2-way page interleaved mode. A one (Default) enables the 4-way page interleaved mode if all 4 banks are the same DRAM devices. |
| 5 | Number of local RAM banks used. 0 = one bank used, non-interleaved mode only (Default). 1 = two banks used. |
| 7, 6 | These bits indicate the local DRAM type as listed: |

| 7 | 6 | DRAM Type |
|---|---|---|
| 0 | 0 | none (Default) |
| 0 | 1 | Reserved |
| 1 | 0 | 256 Kbit |
| 1 | 1 | 1 Mbit |

**EMS Base Address Register RB9**
Index register port: 22H
Data register port: 23H (R/W)
Index: 6DH



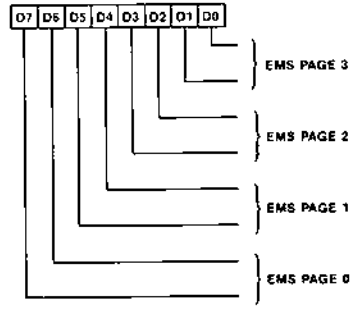

| Bits | Function |
|---|---|
| 0-3 | These bits are used for the EMS page register I/O base address. The bits are encoded as follows, with unused combinations being reserved: |

| 3 | 2 | 1 | 0 | I/O Base |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 208H/209H |
| 0 | 0 | 0 | 1 | 218H/219H |
| 0 | 1 | 0 | 1 | 258H/259H |
| 0 | 1 | 1 | 0 | 268H/269H |
| 1 | 0 | 1 | 0 | 2A8H/2A9H |
| 1 | 0 | 1 | 1 | 2B8H/2B9H |
| 1 | 1 | 1 | 0 | 2E8H/2E9H |

| Bits | Function |
|---|---|
| 7-4 | These bits are used for selecting the expanded memory base addresses. They are encoded as follows, with all unused combinations being reserved: |

| 7 | 6 | 5 | 4 | EMS Base Addresses |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | C0000H, C4000H, C8000H, CC000H |
| 0 | 0 | 0 | 1 | C4000H, C8000H, CC000H, D0000H |
| 0 | 0 | 1 | 0 | C8000H, CC000H, D0000H, D4000H |
| 0 | 0 | 1 | 1 | CC000H, D0000H, D4000H, D8000H |
| 0 | 1 | 0 | 0 | D0000H, D4000H, D8000H, DC000H |
| 0 | 1 | 0 | 1 | D4000H, D8000H, DC000H, E0000H |
| 0 | 1 | 1 | 0 | D8000H, DC000H, E0000H, E4000H |
| 0 | 1 | 1 | 1 | DC000H, E0000H, E4000H, E8000H |
| 1 | 0 | 0 | 0 | E0000H, E4000H, E8000H, EC000H |

**EMS Address Extention Register RB10**
Index register port: 22H
Data register port: 23H (R/W)
Index: 6EH




| Bits | Function |
|---|---|
| 1(A22) 0(A21) | EMS Page 3 address extension bits. |

| 1 | 0 | Block of EMS Memory |
|---|---|---|
| 0 | 0 | 0 Mbyte to 2 Mbyte |
| 0 | 1 | 2 Mbyte to 4 Mbyte |
| 1 | 0 | 4 Mbyte to 6 Mbyte |
| 1 | 1 | 6 Mbyte to 8 Mbyte |

| Bits | Function |
|---|---|
| 3(A22) 2(A21) | EMS Page 2 address extension bits. |

| 3 | 2 | Block of EMS Memory |
|---|---|---|
| 0 | 0 | 0 Mbyte to 2 Mbyte |
| 0 | 1 | 2 Mbyte to 4 Mbyte |
| 1 | 0 | 4 Mbyte to 6 Mbyte |
| 1 | 1 | 6 Mbyte to 8 Mbyte |

| | |
|---|---|
| 5(A22)<br>4(A21) | EMS Page 1 address extension bits. |

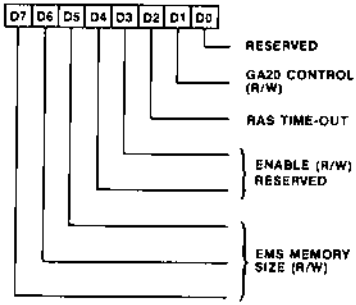
| 5 | 4 | Block of EMS Memory |
|---|---|---|
| 0 | 0 | 0 Mbyte to 2 Mbyte |
| 0 | 1 | 2 Mbyte to 4 Mbyte |
| 1 | 0 | 4 Mbyte to 6 Mbyte |
| 1 | 1 | 6 Mbyte to 8 Mbyte |

| | |
|---|---|
| 7(A22)<br>6(A21) | EMS Page 0 address extension bits. |

| 7 | 6 | Block of EMS Memory |
|---|---|---|
| 0 | 0 | 0 Mbyte to 2 Mbyte |
| 0 | 1 | 2 Mbyte to 4 Mbyte |
| 1 | 0 | 4 Mbyte to 6 Mbyte |
| 1 | 1 | 6 Mbyte to 8 Mbyte |

Address lines A22 and A21 are used in EMS Address translation logic.

**Miscellaneous Register RB12**
Index register port: 22H
Data register port: 23H
Index: 6FH




| Bits | Function |
|---|---|
| 0 | Reserved and default to 0.* |
| 1 | This bit is used for Address line A20 control and provides OS/2 optimization while switching between real and protected modes. If the bit is set to 0 it enables CPUA20 onto A20. The bit default to 1 and sets A20 = 0. |
| 2 | This bit is used to enable the RAS time-out counter for page mode operation. The counter is disabled if set to 0 (Default) and is enabled if set to 1. |
| 3, 4 | Reserved and default to 1 (bit 4), 0 (bit 3). |
| 7-5 | These bits are used to set the EMS memory space according to the following coding: |

| 7 | 6 | 5 | EMS Memory Size |
|---|---|---|---|
| 0 | 0 | 0 | less than 1 Mbyte |
| 0 | 0 | 1 | 1 Mbyte |
| 0 | 1 | 0 | 2 Mbytes |
| 0 | 1 | 1 | 3 Mbytes |
| 1 | 0 | 0 | 4 Mbytes |
| 1 | 0 | 1 | 5 Mbytes |
| 1 | 1 | 0 | 6 Mbytes |
| 1 | 1 | 1 | 7 Mbytes |

**EMS Page Registers**

| | |
|---|---|
| Page 0 | 2X8/2X9H |
| Page 1 | 42X8/42X9H |
| Page 2 | 82X8/82X9H |
| Page 3 | C2X8/C2X9H |

| Bits | Function |
|---|---|
| 0-6 | 0 - A14<br>1 - A15<br>2 - A16<br>3 - A17<br>4 - A18<br>5 - A19<br>6 - A20 |
| 7 | 0 - page disable<br>1 - page enable |

X can be 0, 1, 5, 6, A, B, E

*The reserved bits are recommanded to be initialized to 1.

## 2.6 Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | — | 7.0 | V |
| Input Voltage | $V_I$ | -0.5 | 5.5 | V |
| Output Voltage | $V_O$ | -0.5 | 5.5 | V |
| Operating Temperature | $T_{OP}$ | -25° | 85° | C |
| Storage Temperature | $T_{STG}$ | -40° | 125° | C |

**NOTE:** Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

## 2.7 82C212 Operating Conditions

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.75 | 5.25 | V |
| Ambient Temperature | $T_A$ | 0° | 70° | C |

## 2.8 82C212 DC Characteristics

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | — | 0.8 | V |
| Input High Voltage | $V_{IH}$ | 2.0 | — | V |
| Output Low Voltage $I_{OL}$ = 4mA | $V_{OL}$ | — | 0.45 | V |
| Output High Voltage $I_{OH}$ = -4mA | $V_{OH}$ | 2.4 | — | V |
| Input Low Current $0<V_{IN}<V_{CC}$ | $I_{IL}$ | — | +10 | μA |
| Power Supply Current @ 16MHz | $I_{CC}$ | — | 75 | mA |
| Output High-Z Leakage Current $0.45<V_{OUT}<V_{CC}$ | $I_{OZ1}$ | | +10 | μA |
| Standby Power Supply Current | $I_{CCSB}$ | — | 1.0 | mA |

## 2.9 82C212-12, 82C212-16 AC Characteristics

($T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ± 5%)

| Sym | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| t1 | $\overline{RAS}_i$ active delay from CLK2↓ | 11 | | 16 | ns |
| t2 | $\overline{RAS}_i$ inactive delay from CLK2↓ | 15 | | 25 | ns |
| t3 | DLYOUT active delay from $\overline{RAS}_i$↓ | 0 | | 4 | ns |
| t4 | DLYOUT inactive delay from $\overline{RAS}_i$↑ | 0 | | 6 | ns |
| t5 | Column address stable from DLY0↑ | 8 | | 18 | ns |
| t6 | Column address hold from DLY0↓ | 6 | | | ns |
| t7 | $\overline{CAS}_i$ active delay from DLY1↑ | 7 | | 14 | ns |
| t8 | $\overline{CAS}_i$ inactive delay from DLY1↓ | 11 | | 18 | ns |
| t9 | $\overline{AF16}$ active delay from CLK2↓ | 7 | | 16(19) | ns |
| t10 | $\overline{AF16}$ inactive delay from CLK2↓ | 8 | | 18(21) | ns |
| t11 | $\overline{READY}$ active delay from CLK2↓ | 15 | | 25 | ns |
| t12 | $\overline{READY}$ inactive delay from CLK2↓ | 11 | | 20 | ns |
| t13 | $\overline{DRD}$ active delay from CLK2↓ | 10 | | 19 | ns |
| t14 | $\overline{DRD}$ hold from DLE↓ | 13 | | | ns |
| t15 | DLE active delay from $\overline{DLY1}$↑ | 6 | | 16 | ns |
| t16 | DLE inactive delay from CLK2↓ | 9 | | 18 | ns |
| t17 | $\overline{LMEGCS}$ active from CLK2↓ | 12 | | 21 | ns |
| t18 | $\overline{LMEGCS}$ inactive from CLK2↓ | 11 | | 20 | ns |
| t19 | $\overline{GA20}$ valid delay from CPU <A20> valid | 7 | | 16 (20) | ns |
| t20 | $\overline{GA20}$ invalid delay from CPU <A20> invalid | 4 | | 12 (16) | ns |
| t22 | $\overline{MWE}$ active delay from CLK2↓ | 11 | | 20 | ns |
| t23 | $\overline{MWE}$ inactive delay from CLK2↑ | 4 | | 12 | ns |
| t26 | $\overline{CAS}_i$ active delay from CLK2↓ | 10 | | 19 (25) | ns |
| t27 | $\overline{CAS}_i$ inactive delay from CLK2↓ | 11 | | 21(26) | ns |
| t28 | $\overline{DRD}$ inactive delay from CLK2↓ | 12 | | 23 | ns |
| t29 | $\overline{CAS}_i$ inactive delay from DLE inactive | 2 | | | ns |
| t30 | $\overline{RAS}_i$ active delay from CLK2↓ | 10.5 | | 16 | ns |
| t31 | Row address set up time to $\overline{RAS}_i$↓ | 8 | | | ns |
| t32 | Row address hold time from CLK2↓ | 6 | | 22 | ns |
| t33 | $\overline{RAS}_i$ inactive delay from CLK2↓ | 15 | | 25 | ns |

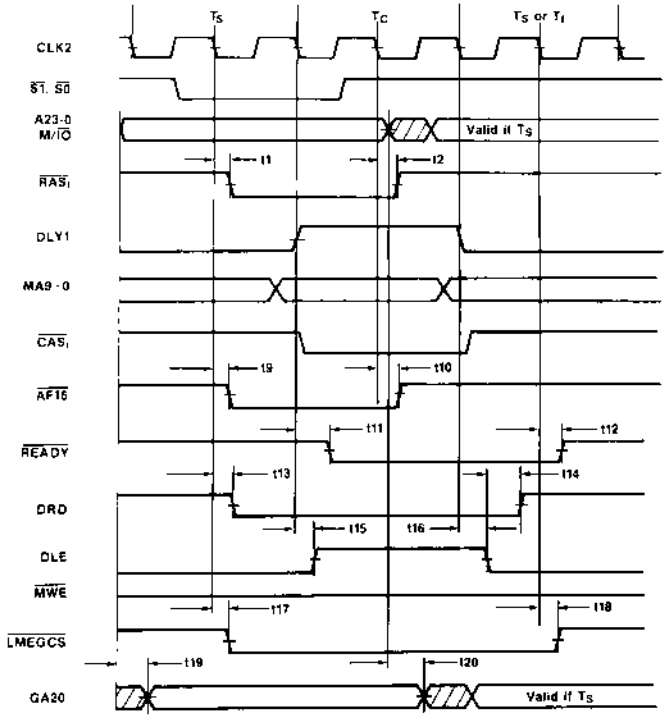
## 2.9 82C212-12, 82C212-16 AC Characteristics (Continued)

($T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ± 5%)

| Sym | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| t34 | $\overline{RAS}$, precharge time (Interleaved Mode) | | 4 × CLK2 | | |
| t35 | $\overline{ROMCS}$ active from CLK2↓ | 11 | | 20 | ns |
| t36 | $\overline{ROMCS}$ inactive from CLK2↑ | 10 | | 20 | ns |
| t37 | DLE hold time from $\overline{DRD}$ | 0 | | 7 | ns |
| t38 | $\overline{RAS_{0-3}}$ inactive from $\overline{REF}$↓ | 13 | | 24 | ns |
| t39 | $\overline{RAS_{0,3}}$ active from $\overline{XMEMR}$↓ | 9 | | 17 | ns |
| t40 | $\overline{RAS_{0,3}}$ inactive from $\overline{XMEMR}$↑ | 10 | | 19 | ns |
| t41 | $\overline{RAS_{1,2}}$ active from $\overline{RAS_{0,3}}$↓ | 7 | | 15 | ns |
| t42 | $\overline{RAS_{1,2}}$ inactive from $\overline{RAS_{0,3}}$↑ | 11 | | 20 | ns |
| t43 | Address setup time from $\overline{XMEMR}$↓ | 10 | | | ns |
| t44 | Address hold time from $\overline{REF}$↑ | 4 | | | ns |
| t45 | Refresh address delay | 0 | | | ns |
| t47 | $\overline{LMEGCS}$ delay from $\overline{REF}$↓ | 8 | | 16 | ns |
| t48 | $\overline{LMEGCS}$ delay from $\overline{REF}$↑ | 10 | | 19 | ns |
| t49 | $\overline{RAS_{0-3}}$ inactive from HLDA1↑ | 11 | | 20 | ns |
| t50 | $\overline{RAS}$, active from command active | 10 | | 18 | ns |
| t51 | $\overline{RAS}$, inactive from command inactive | 12 | | 21 | ns |
| t54 | Column address stable from DLY0↑ | 9 | | 18 | ns |
| t55 | $\overline{CAS}$, active delay from DLY1↑ (while XMEMW active) | 6 | | 14 | ns |
| t56 | $\overline{CAS}$, inactive delay from command inactive | 9 | | 18 | ns |
| t57 | $\overline{AF16}$ active from command active | 9 | | 17 | ns |
| t58 | $\overline{AF16}$ inactive from command inactive | 6 | | 14 | ns |

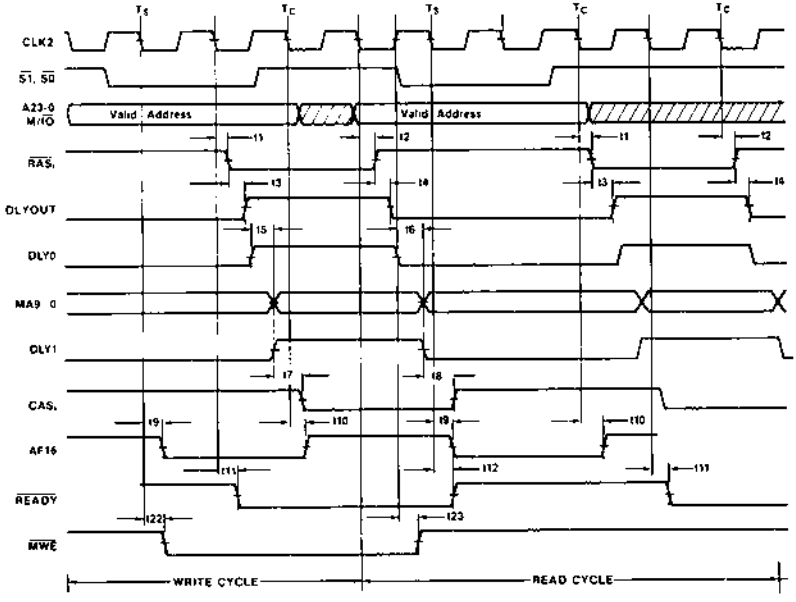
**Note:** Value inside ( ) are 12 MHz timing.

## 2.10 82C212 Timing Diagrams



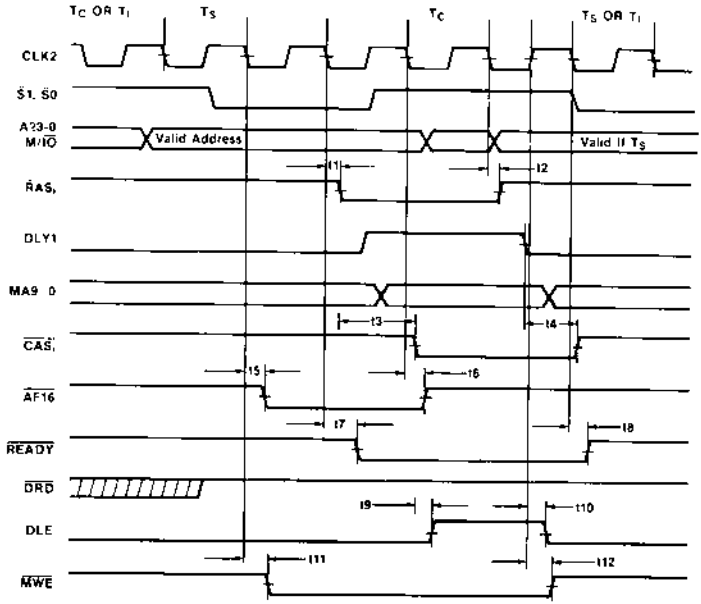

Non-Interleave Mode—Read, 0WS

## 2.10 82C212 Timing Diagrams (Continued)



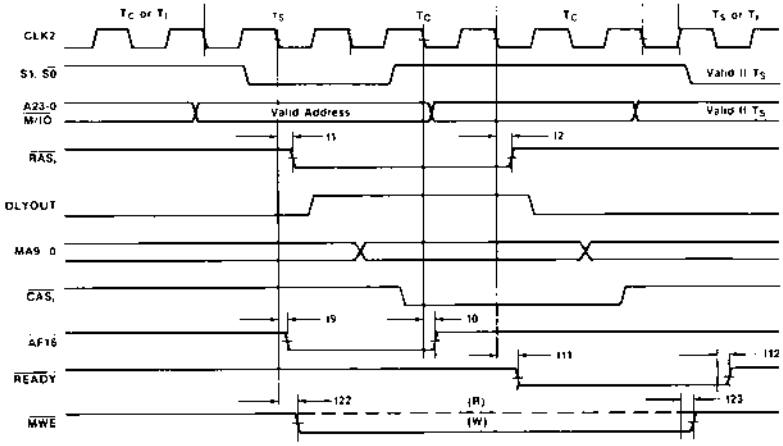

**Non-Interleave Mode—Write Followed by Read, 0WS**

## 2.10 82C212 Timing Diagrams (Continued)



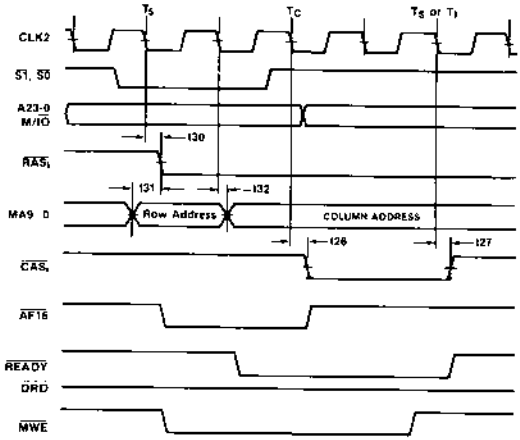

**Non-Interleave Mode—0WS, Write**

## 2.10 82C212 Timing Diagrams (Continued)



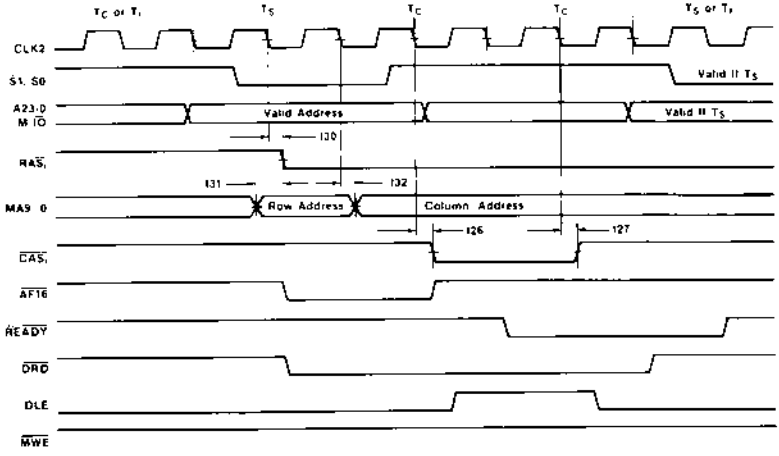

**Non-Interleave Mode—1WS, Read, Write**

## 2.10 82C212 Timing Diagrams (Continued)



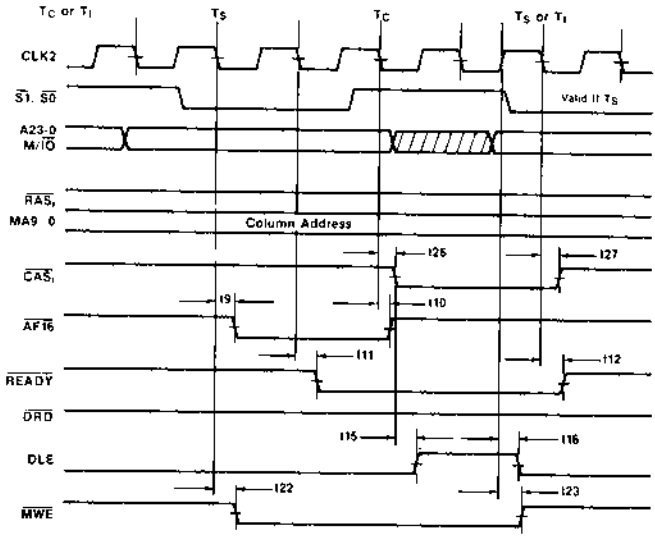

**Interleave Mode—Write Cycle with RAS Being Inactive, 0WS**

## 2.10 82C212 Timing Diagrams (Continued)



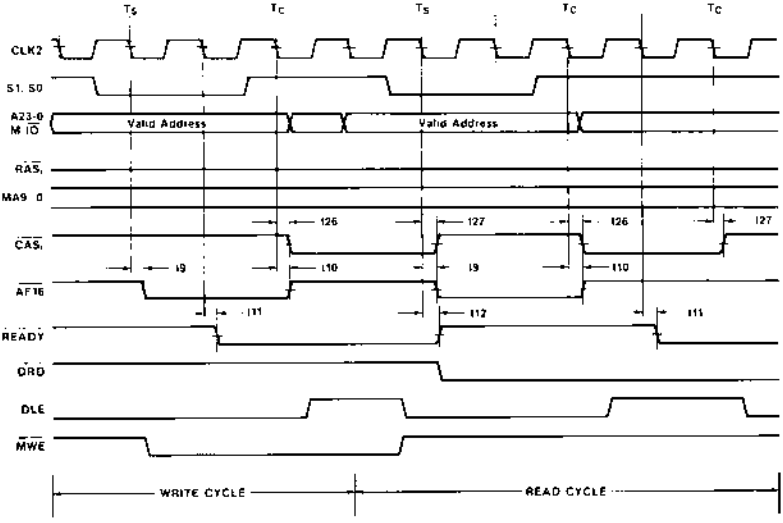

**Interleave Mode—Read Cycle with RAS Being Inactive, 0WS**

## 2.10 82C212 Timing Diagrams (Continued)



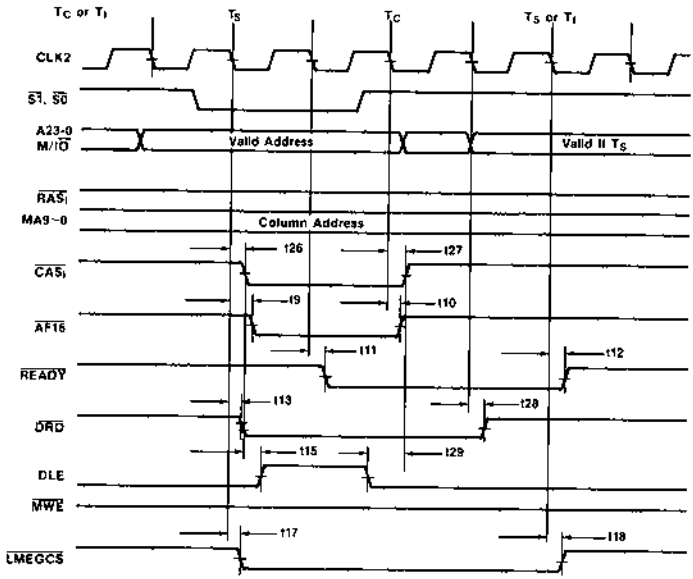

**Interleave Mode—Write, 0WS (RAS active)**

## 2.10 82C212 Timing Diagrams (Continued)



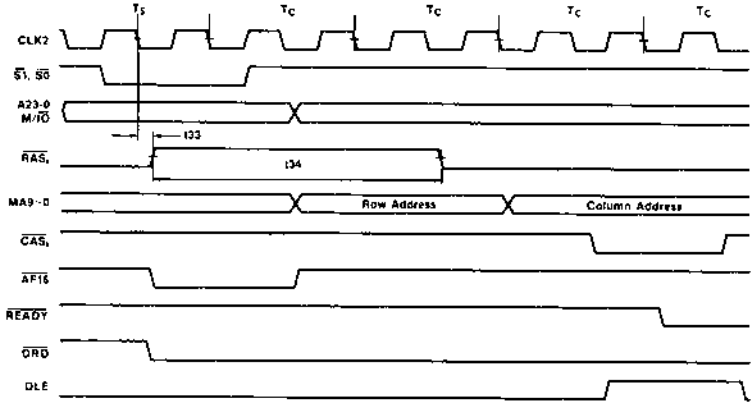

**Interleave Mode—Read After Write, 0WS (RAS active)**

## 2.10 82C212 Timing Diagrams (Continued)



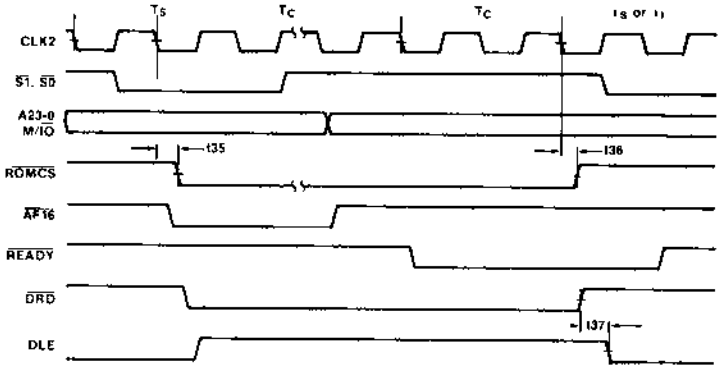

**Interleave Mode—Read, 0WS (RAS active)**

## 2.10 82C212 Timing Diagrams (Continued)



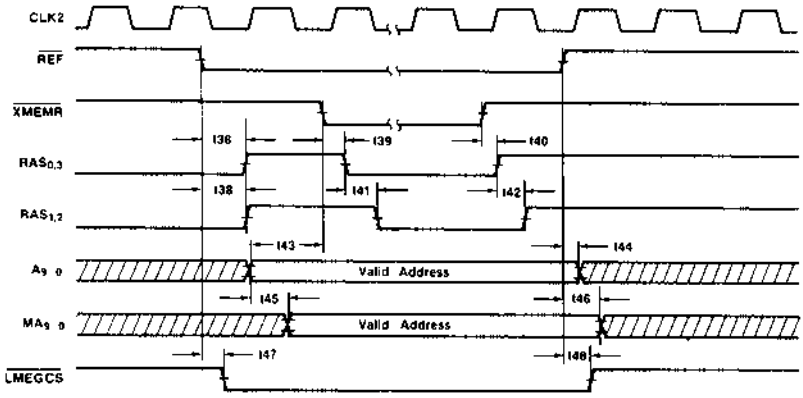

**Interleave Mode—Read Miss Cycle**

## 2.10 82C212 Timing Diagrams (Continued)



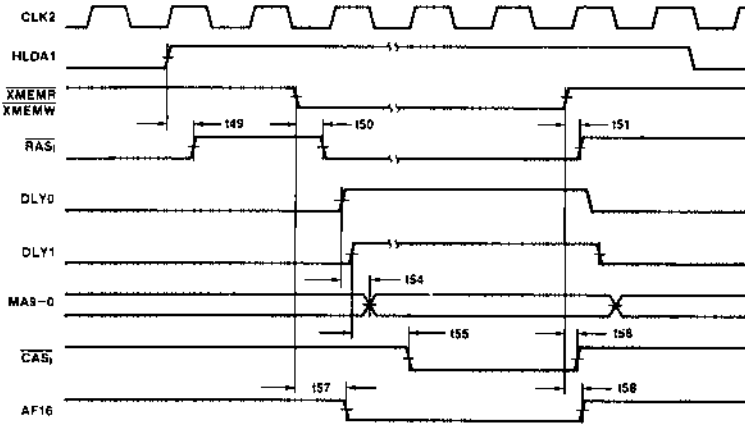

**ROM Read Cycle**

## 2.10 82C212 Timing Diagrams (Continued)




Refresh Cycle

## 2.10 82C212 Timing Diagrams (Continued)




**DMA Cycle**

# 3 82C215 DATA/ADDRESS BUFFER

## 3.1 Features

- Bus Conversion logic for 16 bit to 8 bit transfers
- Parity generation/detection logic

## 3.2 Functional Description

Figure 3.1 is a block diagram of the 82C215 Data/Address buffer. It consists of four modules:

- Address buffers and latches
- Data buffers and latches
- Bus conversion logic
- Parity generation/detection logic

### 3.2.1 Address Buffers and Latches

The 82C215 provides the address buffering between the CPU address lines A1-A16 and the XA1-XA16 lines. These buffers drive 4 mA output low currents ($I_{OL}$). The CPU address lines are latched by IALE to generate the X-Address lines when HLDA is inactive.

### 3.2.2 Data Buffers and Latches

The 82C215 provides the buffering between the CPU data bus (D0-D15) and the memory data bus (MD0-MD15). The D0-D15 lines drive 4 mA output low currents ($I_{OL}$). The MD0-MD15 lines drive 8 mA $I_{OL}$. The enable signal for the latch between the Memory Data bus and the CPU Data bus is controlled by $\overline{DRD}$, HLDA and the action codes. This allows 16 bit reads from 8 bit peripherals controlled by the 82C211.

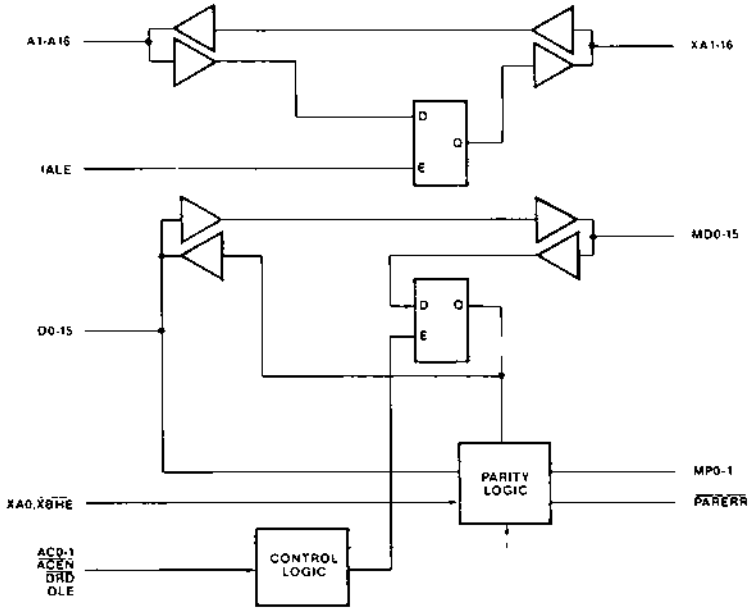



Figure 3.1 82C215 Block Diagram

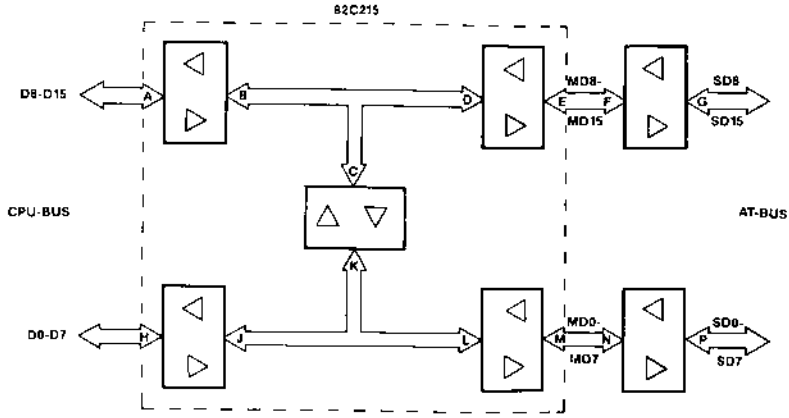



**Figure 3.2 Bus Conversion Data Paths**

### 3.3.3 Bus Conversion Logic

The 82C215 provides data bus conversion when the 16 bit CPU reads from or writes to 8 bit devices. It also provides bus conversion for Master/DMA cycles. There are six possible cases, as seen in Table 3.1 in conjunction with Figure 3.2. These conversions are controlled by the action codes which are qualified by ACEN from the 82C211.

### 3.3.4 Parity Generation/Detection Logic

For local RAM write cycles, the 82C215 generates even parity for each of the two bytes of the data word. These valid even parity bits are written to the parity bits MP0, MP1 in the local DRAMs. During a local memory read cycle, the 82C215 checks for even parity for each MD byte read. If the parity is detected as being odd, the 82C215 flags a parity error on the PARERR output line to the 82C211. The 82C211 distinguishes between local ROM and RAM cycles before sampling PARERR.

Table 3.1

| AC1 | AC0 | Cycle | Operation | Data Path |
|---|---|---|---|---|
| 0 | 0 | CPU | 16 bit write | A-B-D-E-F-G and H-J-L-M-N-P |
| 0 | 0 | CPU | 8 bit LO write | H-J-L-M-N-P |
| 0 | 1 | CPU | 16 bit read | G-F-E-D-B-A and P-N-M-L-J-H |
| 0 | 1 | CPU | 8 bit LO read | P-N-M-L-J-H |
| 1 | 0 | CPU | 8 bit HI write | A-B-C-K-L-M-N-P |
| 1 | 1 | CPU | 8 bit HI read | P-N-M-L-K-C-B-A |
| 1 | 0 | DMA/MASTER | 8 bit HI write | P-N-M-L-K-C-D-E-F-G |
| 1 | 1 | DMA/MASTER | 8 bit HI read | G-F-E-D-C-K-L-M-N-P |

### 3.4 Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | — | 7.0 | V |
| Input Voltage | $V_I$ | -0.5 | 5.5 | V |
| Output Voltage | $V_O$ | -0.5 | 5.5 | V |
| Operating Temperature | $T_{OP}$ | -25° | 85° | C |
| Storage Temperature | $T_{STG}$ | -40° | 125° | C |

**NOTE:** Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

### 3.5 82C215 Operating Conditions

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.75 | 5.25 | V |
| Ambient Temperature | $T_A$ | 0° | 70° | C |

### 3.6 82C215 DC Characteristics

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | — | 0.8 | V |
| Input High Voltage | $V_{IH}$ | 2.0 | — | V |
| Output Low Voltage<br>$I_{OL}$ = 4mA | $V_{OL}$ | — | 0.45 | V |
| Output High Voltage<br>$I_{OH}$ = -4mA | $V_{OH}$ | 2.4 | — | V |
| Input Current<br>$0<V_{IN}<V_{CC}$ | $I_{IL}$ | — | ±10 | μA |
| Power Supply Current @ 16MHz | $I_{CC}$ | — | 80 | mA |
| Output High-Z Leakage Current<br>$0.45<V_{OUT}<V_{CC}$ | $I_{OZ1}$ | | ±10 | μA |
| Standby Power Supply Current | $I_{CCSB}$ | — | 1.0 | mA |

### 3.7 82C215-12, 82C215-16 AC Characteristics

($T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ± 5%)

| Sym | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| t1 | MD bus 3-stated after $\overline{DRD}$ active | 7.5 | | 24 | ns |
| t2 | MD bus valid to D bus valid | 8 | | 18.5 | ns |
| t3a | MD bus being driven after $\overline{DRD}$ inactive | 7.5 | | 28 | ns |
| t3b | MP0, MP1 being driven after $\overline{DRD}$ inactive | 6 | | 23 | ns |
| t4 | D bus invalid after $\overline{DRD}$ inactive | 4 | | 13 | ns |
| t5 | D bus 3-stated after $\overline{DRD}$ inactive | 6 | | 15 | ns |
| t6 | D bus valid to MD bus valid | 11 | | 19 | ns |
| t7 | D bus valid to MP1, MP0 valid | 11 | | 20 | ns |
| t8 | $\overline{ACEN}$ active to D bus valid | 16 | | 27 | ns |
| t9 | AC code valid to MD bus valid | 10 | | 19 | ns |
| t10 | AC code invalid to MD bus invalid | 11 | | 20 | ns |
| t11 | DLE inactive to $\overline{PARERR}$ enabled | 17 | | 30 | ns |
| t12 | $\overline{DRD}$ inactive to $\overline{PARERR}$ disabled | 17 | | 28 | ns |
| t13 | IALE active to XA bus valid | 11 | | 19 | ns |

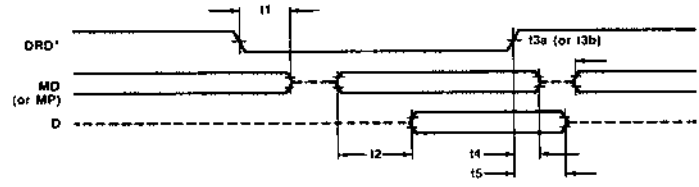
### 3.7 82C215-12, 82C215-16 AC Characteristics (Continued)

($T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ± 5%)

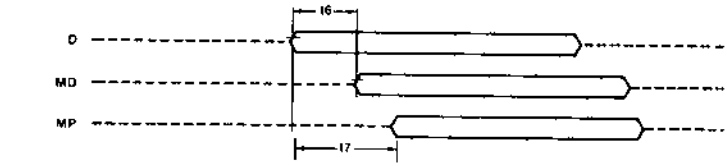
| Sym | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| t14 | XA bus valid to A bus valid | 7 | | 16 (19) | ns |
| t15 | MD, MP setup time to DLE trailing edge | 0.0 | | | ns |
| t16 | MD, MP hold time from DLE trailing edge | 6.0 | | | ns |
| t17 | $\overline{DRD}$ setup time to DLE trailing edge | 12 | | | ns |
| t19 | MD bus hold time from $\overline{ACEN}$ trailing edge | 7.5 | | | ns |
| t20 | MD bus valid to MP valid during DMA memory write cycle | 14 | | 24 | ns |
| t21 | MD high byte valid to MD low byte valid during DMA high memory read cycle | 10 | | 19 | ns |
| t22 | AC code valid to MD high byte valid during DMA high memory write cycle | 9 | | 18 | ns |
| t23 | AC code valid to MP valid during DMA high memory write cycle | 17 | | 28 | ns |

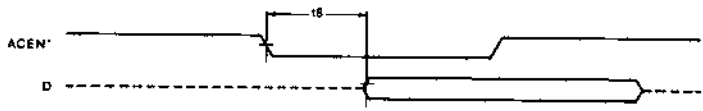
**Note:** Values inside ( ) are 12 MHz timing.

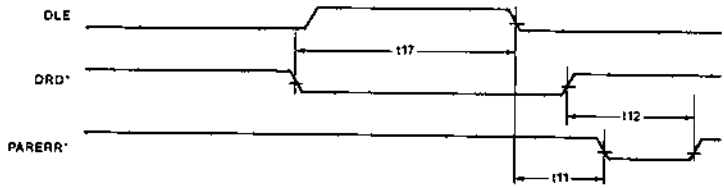
### 3.8 82C215 Timing Diagrams

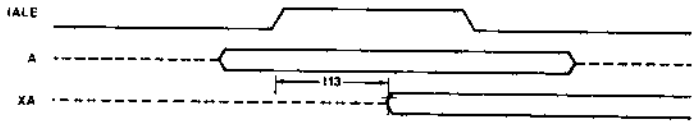


### 3.8 82C215 Timing Diagrams (Continued)

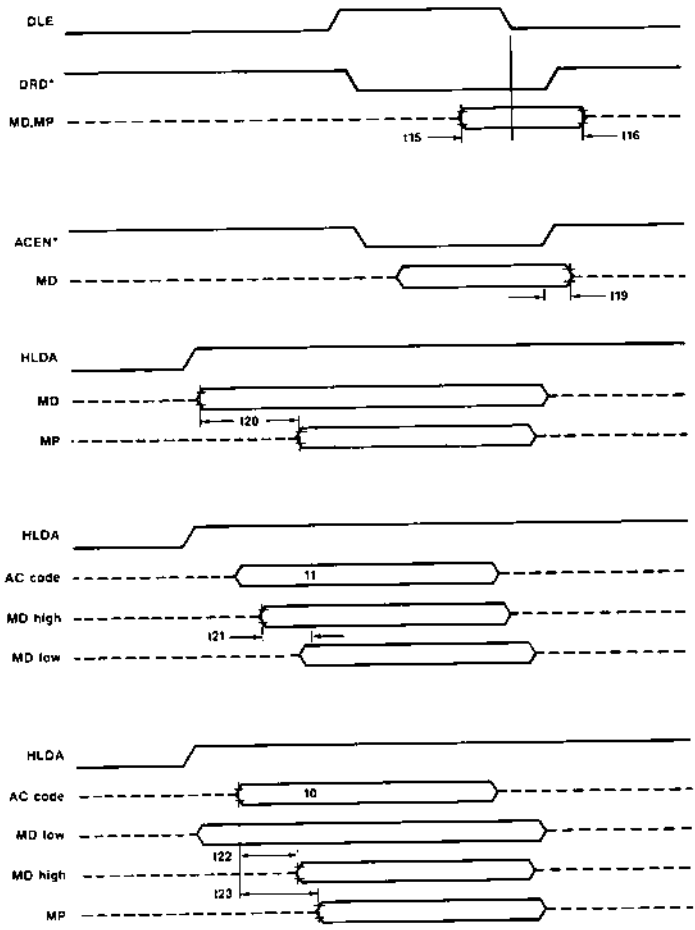


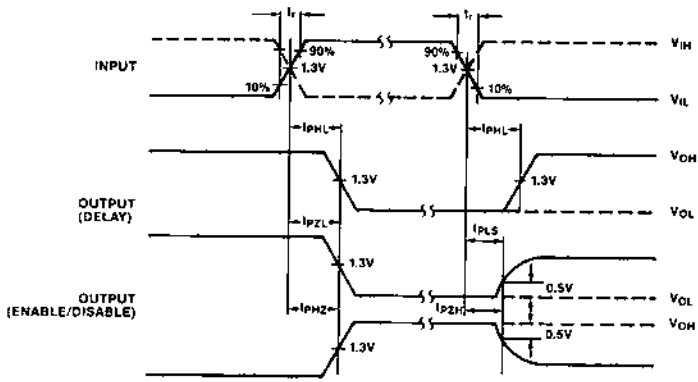



## 3.8 82C215 Timing Diagrams (Continued)



**Load Circuit Measurement Conditions**

| Parameter | Output Type | Symbol | $C_L$(pF) | $R_1$ (Ω) | $R_L$ (Ω) | $SW_1$ | $SW_2$ |
|---|---|---|---|---|---|---|---|
| Propagation Delay Time | Totem pole 3-state Bidirectional | $t_{PLH}$ $t_{PHL}$ | 50 | — | 1.0K | OFF | ON |
| Propagation Delay Time | Open drain or Open Collector | $t_{PLH}$ $t_{PHL}$ | 50 | 0.5K | — | ON | OFF |
| Disable Time | 3-state Bidirectional | $t_{PLZ}$ $t_{PHZ}$ | 5 | 0.5K | 1.0K | ON OFF | ON |
| Enable Time | 3-state Bidirectional | $t_{PZL}$ $t_{PZH}$ | 50 | 0.5K | 1.0K | ON OFF | ON ON |



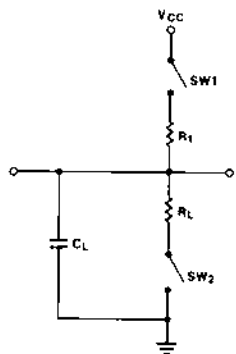
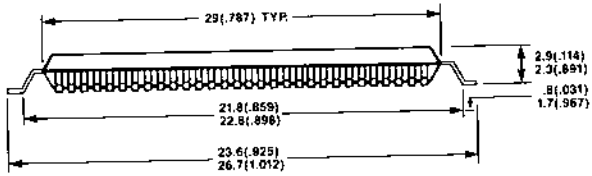
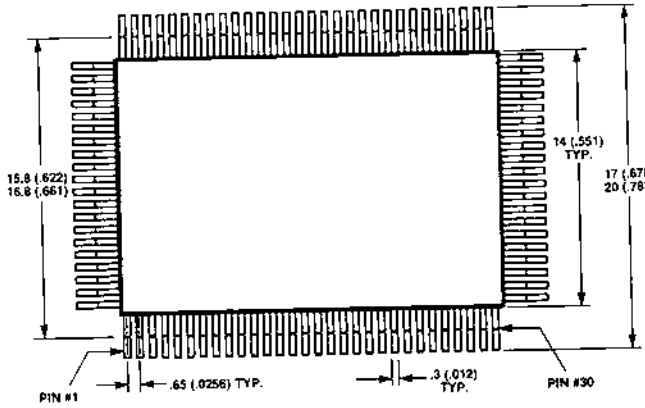




**Figure 10. Load Circuit and AC Characteristics Measurement Waveform**

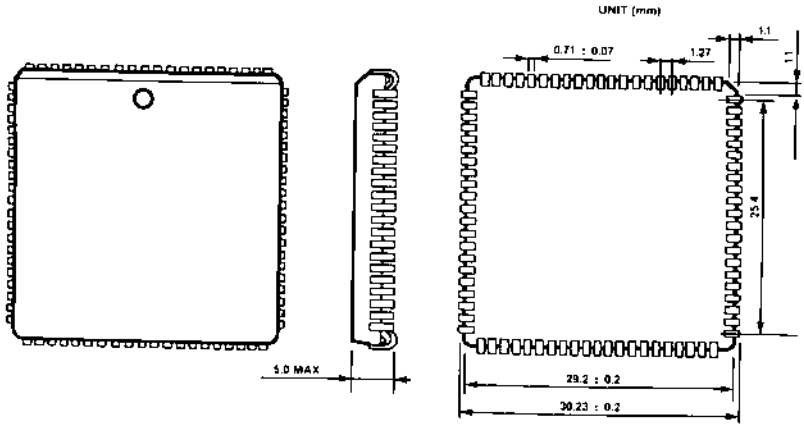
## 100-PIN PLASTIC FLAT PACKAGE




ALL DIMENSIONS IN MILLIMETERS (INCHES).

## 84-PIN PLASTIC LEADED CHIP CARRIER




### Ordering Information

| Order Number | Package Type |
|---|---|
| P82C211/212/215/206 | PLCC-84 pins |
| F82C211/212/215/206 | PFP-100 pins |

**Note:**
1. PLCC = Plastic Leaded Chip Carrier
   PFP = Plastic Flat Pack

NOTES

NOTES

NOTES

## CANADA DISTRIBUTORS

**Electro Source, Inc.**
39 Robertson Rd., Ste. 233
The Bell Mews Mall
Nepean, Ontario
Canada K2H 8R2
Phone: 613-726-1452

**Electro Source, Inc.**
230 Galaxy Blvd.
Suite 303
Rexdale, Ontario
Canada M9W 5R8
Phone: 416-675-4490

**Electro Source, Inc.**
6600 TransCanada Hwy.
Suite 510
Pointe Claire, Quebec
Canada H9R 4S2
Phone: 514-694-0404

**ITT Rae Electronics**
300 North Riverimede Road
Concord (Toronto) Ontario
Canada L4K 2Z4
Phone: 416-736-1144

**Valtrie Marketing**
910 Roundtree Dairy Road
Unit 12
Woodbridge, Ontario
Canada L4L4B
Phone: 416-851-0355

## U.S. DISTRIBUTORS

**ALABAMA**

**Quality Components**
4900 University Square
Suite 20
Huntsville, AL 35816
Phone: 205-830-1881

**Hall-Mark**
4900 Bradford Drive
Huntsville, AL 35816
Phone: 205-837-8700

**ARIZONA**

**Anthem**
1727 East Webber Drive
Tempe, AZ 85281
Phone: 602-966-6600

**Hall-Mark**
4040 E. Raymond
Phoenix, AZ 85040
Phone: 602-437-1200

**CALIFORNIA**

**Anthem**
20640 Bahama Street
Chatsworth, CA 91311
Phone: 818-700-1000

**Anthem**
One Oldfield Drive
Irvine, CA 92718-2809
Phone: 714-768-4444

**Anthem**
4700 Northgate Boulevard
Sacramento, CA 95834
Phone: 916-922-6800

**Anthem**
9369 Carroll Park Drive
San Diego, CA 92121
Phone: 619-453-9005

**Anthem**
10400 East Brokaw
San Jose, CA 95131
Phone: 408-295-4200

**Hall-Mark**
8130 Remmet Avenue
Canoga Park, CA 91304
Phone: 818-716-7300

**Hall-Mark**
6341 Auburn Blvd., Suite D
Citrus Heights, CA 95610
Phone: 916-722-8600

**Hall-Mark**
3878 Ruffin Rd., Suite B
San Diego, CA 92123
Phone: 619-268-1201

**Hall-Mark**
1110 Ringwood Ct.
San Jose, CA 95131
Phone: 408-946-0900

**Hall-Mark**
19220 S. Normandie Avenue
Torrance, CA 90502
Phone: 213-217-8400

**Hall-Mark**
14831 Franklin Avenue
Tustin, CA 92680
Phone: 714-669-4700

**COLORADO**

**Anthem**
373 Inverness Dr. South
Englewood, CO 80112
Phone: 303-790-4500

**Hall-Mark**
6950 S. Tucson Way
Englewood, CO 80112
Phone: 303-790-1662

**CONNECTICUT**

**Lionex**
170 Research Parkway
Meriden, CT 06450
Phone: 203-237-2282

**Hall-Mark**
33 Village Lane
Wallingford, CT 06492
Phone: 203-269-0100

**FLORIDA**

**Hall-Mark**
15302 Roosevelt Blvd.
Suite 303
Clearwater, FL 33520
Phone: 813-530-4543

**Hall-Mark**
7648 Southland Blvd.
Suite 100
Orlando, FL 32809
Phone: 305-855-4020

**Hall-Mark**
3161 S.W. 15th Street
Pompano Beach, FL
33069-4806
Phone: 305-971-9280

**Quality Components**
Florida
Phone: 800-241-0037

**GEORGIA**

**Hall-Mark**
6410 Atlantic Blvd.
Suite 115
Norcross, GA 30071
Phone: 404-447-8000

**Quality Components**
6145 North Bell Pkwy. Suite 8
Norcross, GA 30071
Phone: 404-449-9508

**ILLINOIS**

**Anthem**
180 Crossen
Elkgrove, IL 60007
Phone: 312-640-6066

**Hall-Mark/N.C. Regional Systems Warehouse**
210 Mittel Drive
Wooddale, IL 60191
Phone: 312-680-3800

**INDIANA**
**Hall-Mark**
4275 W. 96th Street
Indianapolis, IN 46268
Phone: 317-872-8875
800-423-6638 (INDIANA)
800-772-0112 (KENTUCKY)

**KANSAS**
**Hall-Mark**
10809 Lakeview Drive
Lenexa, KS 66215
Phone: 913-888-4747

**MASSACHUSETTS**
**Hall-Mark**
6 Cook Street
Billerica, MA 01821
Boston 617-935-9777
Phone: 617-667-0902

**Lionex**
36 Jonspin Road
Wilmington, MA 01887
Phone: 617-657-5170

**MARYLAND**
**Hall-Mark/Baltimore**
10240 Old Columbia Road
Columbia, MD 21046
Phone: 301-988-9800

**Lionex**
9020A Mondenhall Court
Columbia, MD 21045
Phone: 301-964-0040

**MICHIGAN**
**Hall-Mark**
38027 Schoolcraft
Livonia, MI 45810
Phone: 313-462-1205

**MINNESOTA**
**Anthem**
10025 Valley View Rd. #160
Eden Prairie, MN 55344
Phone: 612-944-5454

**Hall-Mark**
10300 Valley View
Eden Prairie, MN 55344
Phone: 612-941-2600

**MISSOURI**
**Hall-Mark**
13750 Shoreline Drive
Earth City, MO 63045
Phone: 314-291-5350

**NEW MEXICO**
**Hall-Mark**
2715 Braidbent Pkwy. NE.
Albuquerque, NM 87107
Phone: 505-344-7341

**NORTH CAROLINA**
**Hall Mark**
5237 N. Blvd.
Raleigh, NC 27604
Phone: 919-872-0712

**Quality Components**
2940-15 Trawick Road
Raleigh, NC 27604
Phone: 919-876-7767

**NEW JERSEY**
**Lionex**
311 Route 46 West
Fairfield, NJ 07006
Phone: 201-227-7960

**Hall-Mark**
107 Fairfield Road Ste. 1B
Fairfield, NJ 07006
Phone: 201-575-4415

**Hall-Mark**
1000 Midlantic Drive
Mt. Laurel, NJ 08054
Phone: 609-235-1900

**Hall-Mark**
10 Old Bloomfield Avenue
Pinebrook, NJ 07058
Phone: 201-882-9773

**NEW YORK**
**Hall-Mark**
101 Comac Loop
RonKonKoma, NY 11779
Phone: 516-737-0600

**Lionex**
400 Oser Avenue
Hauppauge, NY 11787
Phone: 516-273-1660

**OHIO**
**Hall-Mark**
5821 Harper Road
Solon, OH 44139
Phone: 216-349-4632

**Hall-Mark**
400 E. Wilson Bridge Road
Suite 5
Worthington, OH 43085
Phone: 614-888-3313

**OKLAHOMA**
**Hall-Mark**
2500 No. Hemlock Lane
Broken Arrow, OK 74012
Phone: 1-800-327-9989

**Quality Components**
9934 E. 21st Street South
Tulsa, OK 74129
Phone: 918-664-8812

**OREGON**
**Anthem**
9705 SW Sunshine Cl. #900
Beaverton, OR 97005
Phone: 503-643-1114

**PENNSYLVANIA**
**Lionex**
101 Rock Road
Horsham, PA 19044
Phone: 215-443-5150

**TEXAS**
**Hall-Mark**
12211 Technology Blvd.
Austin, TX 78727
Phone: 512-258-8848

**Hall-Mark**
11420 Page Mill Road
Dallas TX 75243
Phone: 214-553-4300

**Hall-Mark**
8000 Westglen
Houston, TX 77063
Phone: 713-781-6100

**Quality Components**
4257 Kellway Circle
Addison, TX 75001
Phone: 214-733-4300

**Quality Components**
2120-M Braker Lane
Austin, TX 78758
Phone: 512-835-0220

**Quality Components**
1005 Industrial Boulevard
Sugar Land, TX 77478
Phone: 713-240-2255

**UTAH**
**Anthem**
1615 West 2200 South
Salt Lake City, UT 84119
Phone: 801-973-8555

UTAH (con't)
**Hall-Mark**
2265 S. 1300 West
West Valley, UT 84119
Phone: 801-972-1008

WASHINGTON
**Anthem**
5020 148th Avenue N.E.
Redmond, WA 98052
Phone: 206-881-0850

WISCONSIN
**Hall-Mark**
16255 W. Lincoln Avenue
New Berlin, WI 53151
Phone: 414-797-7844

## FAR EAST DISTRIBUTORS

**American MITAC Corporation**
3385 Viso Court
Santa Clara, CA 95054
U.S.A.
Phone: 408-988-0258
Telex: 9103382201 MECTEL
Fax: 408-980-9742

AUSTRALIA
**R&D Electronics**
4 Florence Street
Burwood, Victoria
Australia 3125
Phone: 61-3-288 8911
Fax: 61-3-2889168

HONG KONG
**Wong's Kong King Ltd.**
8/F Sime Darby Ind. Bldg.
420 Kwun Tong Road
Kwun Tong, Hong Kong
Phone: 852 3-450121
Telex: 36810 WKKL HX
Fax: 852 3-7551128

**Technology Research Co.**
4/F, Block C, Watson's Estate
North Point, Hong Kong
Phone: 011852 5-8073323
Telex: 80554 TRC HX
Fax: 852 5-8073031

INDIA
**Silicon Electronics**
3350 Scott Blvd. #1201
Santa Clara, CA 95054
U.S.A.
Phone: 408-988-4408

ISRAEL
**Hitek Ltd.**
5 Haarad St.
TEL-AVIV, ISRAEL
Phone: 972 03/472005
Telex: 922371984HTK1

JAPAN
**ASCII Corporation**
SAT-1 Bldg., 3F
2-20-4, Minami Aoyamo
Minato-ku
Tokyo 107 Japan
Phone: 03-470-0486
Telex: J28764ASCII
Fax: 03-740-0522

KOREA
**Kortronics Enterprises**
Rm. 307 9-Dong B-Block
#604-1 Guro-Dong, Guro-Gu
Seoul, Korea
Phone: 82 2 635-1043
Fax: 82 2 675-0514

SINGAPORE
**Chartered Telmos Design PTE Ltd.**
249 Jalan Boonlay
Singapore 261
Phone: 656607359
Fax: 652614913

TAIWAN, R.O.C.
**Chips & Technologies, Inc. c/o UTC**
8th Floor
687 Ming Sheng E., Rd. Rm. 1
Taipei, Taiwan, R.O.C.
Phone: 886 250 18170 Ext. 204
Fax: 886 27175595

## EUROPEAN DISTRIBUTORS

BELGIUM
**Auriema Belgium S.A./N.V.**
Rue Brogniezstraat 172-A
B-1070 Bruxelles
Brussels
Phone: (02) 523-62-95
Telex: 21646

FINLAND
**OY Fintronic AB**
Melkonkatu 24A
SF-00210
Helsinki, Finland
Phone: 358 06926022
Telex: 857124224 FTRON SF
Fax: 358 0 674886

FRANCE
**A2M**
6, Av. du General De Gaulle
78150 Le Chesnay
France
Phone: 33 39.54.91.13
Telex: 842698376 F
Fax: 331 39.54.30.61

GERMANY
**Rein Elektronik GmbH**
Loetscher Weg 66
Postfach 5160
D-4054 Nettetal 1
West Germany
Phone: 49 (02153) 733-0
Telex: 841854203B REIN D
(or 854251B REIN D)
Fax: 49 02153-733110

ITALY
**Eledra S.p.A.**
Via G. Watt 37
20143 Milano
Viale Elvezia 18
Italy
Phone: 39 (02 81.82.1)
Telex: 843332332
Fax: 39 (02) 81.82.211

NETHERLANDS
**Auriema Nederland B.V.**
Doornakkersweg 26
5642 MP Eindhoven
Netherlands
Phone: 31 (0) 40-816565
Telex: 84451992
Fax: 31 (0) 40-811815

SPAIN
**Compania Electronica de Tecnicas Aplicadas, S.A. (Comelta) (Main Branch)**
Emilio Munoz, num. 41
nave 1-1-2
28037 Madrid, Spain
Phone: 34 754 30 01
Telex: 83142007 CETA E

**SPAIN (cont'd)**
**Compania Electronica de Tecnicas Aplicadas, S.A. (Comelta)**
Pedro IV, num. 84-5
planta
08005 Barcelona, Spain
Phone: 300 77 12 (8 lineas)
Telex: 83151934 CETA E

**SWEDEN (Nordic Countries)**

**Nordisk Elektronik A.B. (Main Branch)**
Torshamnsgatan 39, 7th Floor
Box 36 S-164 93 Kista
Sweden
Phone: 46 08 703 46 30
Fax: 46 08 703 98 45
Telex: 85410547 NORTRON S

**Nordisk Eletronik A/S**
P.O. Box 123
Smedsvingen 4
1364 Hvalstad
Norway
Phone: 47 02 84 62 10
Fax: 47 02 84 65 45
Telex: 85677546 NENASN

**Nordisk Elektronik A/S**
Transformervej 17
DK-2730 Herlev
Denmark
Telex: 85535200 NORDEL DK

**SWITZERLAND**
**DataComp**
Silbernstrasse 10
CH-9853 Diotikon
Switzerland
Phone: 41 01 740 51 40
Telex: 827750 DACO
Fax: 41 1-7413423

**UNITED KINGDOM**
**Katakana Limited**
Manhattan House
Bridge Road
Maidenhead, Berkshire
SL6 8DB
United Kingdom
Phone: Maidenhead 44 (0628) 75641
Telex: 846775 KATKAN
Fax: 44 (0628) 782812

## CANADA SALES REPRESENTATIVES

**Electro Source, Inc.**
39 Robertson Rd, Ste. 233
The Bell Mews Mall
Nepean, Ontario
Canada K2H 8R2
Phone: 613-726-1452

**Electro Source, Inc.**
230 Galaxy Blvd.
Suite 303
Rexdale, Ontario
Canada M9W 5R8
Phone: 416-675-4490

**Electro Source, Inc.**
6600 TransCanada Hwy.
Suite 510
Pointe Claire, Quebec
Canada H9R 4S2
Phone: 514-694-0404

**ITT Rae Electronics**
300 North Rivermede Road
Concord (Toronto) Ontario
Canada L4K 2Z4
Phone: 416-851-0355

**Valtrie Marketing**
910 Roundtree Dairy Road
Unit 12
Woodbraidge, Ontario
Canada L4L4B
Phone: 416-851-0355

## U.S. SALES REPRESENTATIVES

**ALABAMA**
**The Novus Group, Inc.**
2905 Westcorp Blvd.
Suite 120
Huntsville, AL 35805
Phone: 205-534-0044

**ARIZONA**
**Reptronix**
237-C Eubank Blvd. NE
Albuquerque, NM 871213
Phone: 505-292-1718

**Reptronix**
4625 So. Lakeshore Dr.
Tempe, AZ 85282
Phone: 602-964-2362

**CALIFORNIA**
**Chips & Technologies, Inc.**
18201 Von Karman Ave.
Suite 310
Irvine, CA 92715
Phone: 714-852-8721

**Chips & Technologies, Inc.**
2055 Gateway Place
Suite 220
San Jose, CA 95110
Phone: 408-437-8877

**Magna Sales**
2935 Humphrey Road
Loomis, CA 95650
Phone: 408-727-8753

**Magna Sales**
3333 Bowers Avenue
Suite 251
Santa Clara, CA 95054
Phone: 408-727-8753

**S.C. Cubed**
468 Pensfield Place
Suite 101A
Thousand Oaks, CA 91360
Phone: 805-496-7307

**S.C. Cubed**
17862 17th St. East Building
Suite 207
Tustin, CA 92680
Phone: 714-731-9206

**COLORADO**
**Wescom Marketing, Inc.**
4851 Independence Street
Suite 159
Wheat Ridge, CO 80033
Phone: 303-422-8957

**FLORIDA**
**Dyne-A-Mark Corporation**
500 E. Semoran Blvd. Ste. 15A
Casselberry, FL 32707

**Dyne-A-Mark Corporation**
573 South Duncan Avenue
Clearwater, FL 33516
Phone: 813-441-4702
Tampa: 813-223-7969

**Dyne-A-Mark Corporation**
1001 Northwest 62nd Street
Suite 108
Ft. Lauderdale, FL 33309
Phone: 305-771-6501

**Dyne-A-Mark Corporation**
P.O. Box 33
235 S. Mailland Ave.
Suite 204
Maitland, FL 32751
Phone: 305-629-5557

**GEORGIA**
**Chips & Technologies, Inc.**
136 Mae Belle Way
Lawrenceville, GA 30244
Phone: 404-921-0292
Fax: 404-921-0292

**The Novus Group, Inc.**
4556 Canda Drive
Liburn, GA 30247
Phone: 404-381-1015

**ILLINOIS**
**Micro-Tex, Inc.**
2400 West Central Road
Hoffman Estates, IL 60196
Phone: 312-382-3001

**INDIANA**
**Giesting & Associates**
101 East Carmel Drive
Suite 210
Carmel, IN 46032
Phone: 317-844-5222

**Giesting & Associates**
1246 Sowles Bay Road
RR#2 Box 505
Angola, IN 46703
Phone: 219-833-1960

**MARYLAND**
**Micro-Comp, Inc.**
1421 South Calon Ave.
Baltimore, MD 21227-1082
Phone: 301-644-5700

**MASSACHUSETTS**
**Chips & Technologies, Inc.**
One Wall Street
Burlington Office Park
Burlington, MA 01803
Phone: 617-273-3500

**Mill-Bern Associates, Inc.**
2 Mack Road
Woburn, MA 01801
Phone: 617-932-3311

**MICHIGAN**
**Giesting & Associates**
5654 Wendzel Drive
Coloma, MI 49038
Phone: 616-468-4200

**Giesting & Associates**
21999 Farmington Road
Suite 400
Farmington Hills, MI 48024
Phone: 313-478-8106

**Giesting & Associates**
34441 Eight Mile Road
Suite 113
Livonia, MI 48152
Phone: 313-478-8106

**MINNESOTA**
**High Technology Sales Assoc.**
11415 Valley View Road
Eden Prairie, MN 55344
Phone: 612-944-7274

**NEW JERSEY**
**T.A.I.**
12 South Blackhorse Pike
Bellmawr, NJ 08031
Phone: NJ: 609-933-2600
PA: 215-627-6615

**NEW MEXICO**
**Reptronix**
237-C Eubank Blvd. NE
Albuquerque, NM 87123
Phone: 505-292-1718

**NEW YORK**
**ERA, Incorporated**
351 Veterans Memorial Hwy.
Commack, NY 11725
Phone: 516-543-0510

**L-Mar Associates**
349 W. Commercial St.
Suite 2285
Rochester, NY 14445
Phone: 716-381-9100

**NORTH CAROLINA**
**The Novus Group, Inc.**
5337 Trestlewood Lane
Raleigh, NC 27610
Phone: 919-833-7771

**OHIO**
**Giesting & Associates**
2854 Blue Rock Road
P.O. Box 39398
Cincinnati, OH 45239
Phone: 513-385-1105

**Giesting & Associates**
26250 Euclid Avenue
Suite 525
Cleveland, OH 44132
Phone: 216-261-9705

**Giesting & Associates**
8843 Washington Colony Drive
Dayton, OH 45459
Phone: 513-433-5832

**OREGON**
**L-Squared Limited**
15234 NW Greenbrier Pkwy.
Beaverton, OR 97006
Phone: 503-629-8555

**PENNSYLVANIA**
**Giesting & Associates**
471 Walnut Street
Pittsburgh, PA 15238
Phone: 412-963-5832

**TEXAS**
**OM Sales**
13915 Burnet Road
Suite 301
Austin, TX 78728
Phone: 512-388-1151

**Chips & Technologies, Inc.**
15415 Katy Freeway
Suite 209
Houston, TX 77095
Phone: 713-579-9633

**OM Sales**
10500 Richmond Avenue
Suite 115
Houston, TX 77042
Phone: 713-789-4426

**OM Sales**
2323 N. Central Expwy.
Suite 150
Richardson, TX 76080
Phone: 214-690-6746

**UTAH**
**Wescom Marketing, Inc.**
3499 S. Main
Salt Lake City, UT 84114
Phone: 801-269-0419

**WASHINGTON**
**L-Squared Limited**
105 Central Way
Suite 203
Kirkland, WA 98033
Phone: 206-827-8555

**WISCONSIN**
**Micro-Tex, Inc.**
22660 Broadway
Suite 3B
Waukesha, WI 53186
Phone: 414-542-5352

CHIPS

Chips and Technologies, Incorporated
3050 Zanker Road, San Jose, CA 95134 408-434-0600 Telex 272929 CHIP UR

IBM, AT, XT, PS/2, Enhanced Graphics Adapter, Color Graphics Adapter, Monochrome Adapter, IBM Color Display, IBM Monochrome Display are trademarks of International Business Machines.

Intel, iAPX 286 are trademarks of Intel Corporation.

MOTOROLA is a trademark of Motorola.

Hercules Graphics is a trademark of Hercules Computer Technology.

Lotus is a trademark of Lotus Corporation.
Microsoft is a trademark of Microsoft.

CHIPSet, CHIPSpak, CHIPSport, SharpScan EGA NEAT are trademarks of Chips and Technologies, Inc.

Copyright© 1985, 1986, 1987 Chips and Technologies, Inc.

Chips and Technologies, Inc. makes no warranty for the use of its products and bears no responsibility for any errors which may appear in this document.

Chips and Techonologies, Inc. retains the right to make changes to these specifications at any time without notice.

FUJITSU

October 1986
Edition 2.0

# MBL8042H/N

## NMOS Universal Peripheral Interface 8-Bit Microcomputer

### Description

The MBL8042 Universal Peripheral Interface is a single-chip 8-bit microcomputer based on an 8-bit parallel microprocessor chip.

The MBL8042 is fabricated with an N-channel silicon-gate MOS process. The MBL8042 has a 2K x 8-bit ROM for program memory, a 128 x 8-bit RAM for data memory, 18 I/O ports, an 8-bit timer/counter and clock generator on the chip, and is powered by single +5V supply.

The MBL8042 is designed to operate as a slave processor, which receives commands and data from the master processor, controls peripheral devices and transfers input data from peripheral devices to the master processor. By using the MBL8042 an intelligent peripheral controller can be designed freely.

Ceramic DIP
DIP-40C-A01

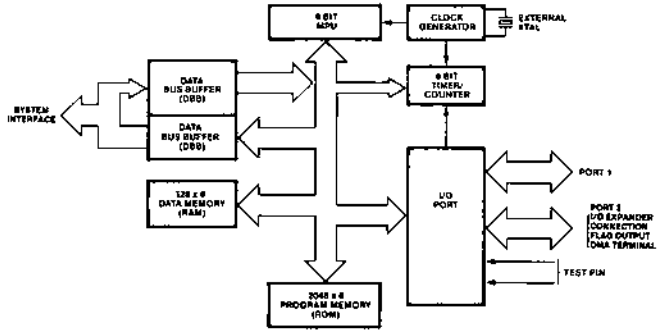
Plastic DIP
DIP-40P-M01

### Features

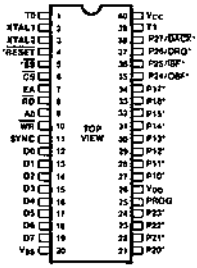
- Processor:
  8-bit parallel processing
- Register:
  One 8-bit Status Register (for interface with master processor)
  Two 8-bit Data Bus Buffer Registers (for Input/Output)
- Memory
  — 2K x 8 bit ROM (for program memory)
  — 128 x 8 bit RAM (for data memory)
- I/O:
  One 8-bit Bidirectional Data Bus
  Two 8-bit Bidirectional I/O Ports
  Two Test Inputs
- Clock Source:
  Clock Generator (with External Crystal Resonator) or External Clock
- 8-Bit Interval Timer/Event Counter
- Low-power Standby Operation Capability
- Power-on Reset Capability (with External Capacitor)
- Instruction Set:
  93 Instructions
  (217 Instruction Codes)
  — 1-byte Instruction (about 70%), 2-byte Instruction (about 30%)
  — 1-cycle or 2-cycle Instruction (1 cycle = 2.5μs at 6MHz XTAL)
- Technology:
  N-channel Silicon-gate E/D MOS Process
- Two Package Options:
  Standard 40-pin Ceramic (Suffix-C) or Plastic DIP (Suffix-P)
- Equivalent:
  Intel 8042

Portions reprinted by permission of Intel Corporation. Copyright © 1985 Intel Corporation
Compilation and additional materials Copyright © 1985 by Fujitsu Limited, Tokyo, Japan, and Fujitsu Microelectronics, Inc., Santa Clara, California, U.S.A. Fujitsu Limited is a licensee of Intel Corporation and authorized to produce alternate source products.

## Block Diagram




## Pin Assignment




*These pins are internally pulled up

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

## Pin Descriptions

| Pin No. | Name | Symbol | Description |
|---|---|---|---|
| 1 | Test 0 | $T_0$ | Conditional Input for Conditional Branch |
| 2 | Crystal 1 | XTAL 1 | Input pin for an internal Clock Generator connected to external crystal. Also, this pin can be used as input from an external clock source. |
| 3 | Crystal 2 | XTAL 2 | Input pin for an internal Clock Generater connected to external crystal. (Note: The XTAL 1 and XTAL 2 input levels are not TTL compatible). |
| 4 | Reset | $\overline{RESET}$ | Resets and forces the MPU to be initialized (Note: This input level is not TTL compatible) |
| 5 | Single Step | $\overline{SS}$ | Input pin used for single step operation. |
| 6 | Chip Select | $\overline{CS}$ | Input pin used for the master processor to select the UPI. |
| 7 | External Address | EA | Input pin used for controlling program memory access. Holding EA high forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. |
| 8 | Read Strobe | $\overline{RD}$ | Strobe input enables the MBL8042 to read contents of the Data Bus Buffer register or Status register. |
| 9 | Address "0" | $A_0$ | Address input to read/write data or read/write commands<br>$A_0$ = "L" indicates data read or write<br>$A_0$ = "H" indicates status read or command write |
| 10 | Write Strobe | $\overline{WR}$ | Strobe input enables the MBL8042 to write data into its Data Buffer register. |
| 11 | Sync | SYNC | A clock output pin indicating the MBL8042 instruction cycle. This pin is used when a synchronization signal is required for external circuits. |
| 12 thru 19 | Data Bus | $DB_0$ thru $DB_7$ | 8-bit bidirectional I/O port used to interface the MBL8042 to the master processor |
| 20 | Ground | $V_{SS}$ | Ground terminal. |
| 21 thru 24 | Port 2 | $P2_0$ thru $P2_3$ | Lower 4 bits of the quasi-bidirectional I/O port (Port 2). These function as interface port with the I/O expander (MBL8243) when an expansion I/O executes instruction During single step operation upper 3 bits of the program fetch address are output on P20, P21, P22. |
| 25 | Program | PROG | A strobe signal output pin for an I/O expander (MBL8243) used, when performing an expansion I/O instruction. |
| 26 | Power Supply | $V_{DD}$ | Power supply pin (+ 5V) for internal RAM. |
| 27 thru 34 | Port 1 | $P1_0$ thru $P1_7$ | Quasi-bidirectional I/O ports (Port 1). During single step operation, the next program fetch address (Lower 8 bits) is output |
| 35 thru 38 | Port 2 | $P2_4$ thru $P2_7$ | Upper 4 bits of the quasi-bidirectional I/O port (port 2). These function as the flag output pins ($P2_4$ and $P2_5$) and DMA pins ($P2_6$ and $P2_7$) according to instructions |
| 39 | Test 1 | $T_1$ | This pin has the following functions according to instruction<br>1. Event Input pin for the Event Counter<br>2. Condition Input pin for Conditional Branch |
| 40 | Power Supply | $V_{CC}$ | Power supply pin (+ 5V). |

4

## System Interface

The master processor and MBL8042 are interfaced through the data bus buffer

MBL8042 has 2 internal DBB (Data Bus Buffer) registers. The register to be accessed is determined by the address line and strobe signal.

Flag 1 (F1) is set when a command is written ($A_0$ = 1), and reset when data is written ($A_0$ = 0).

The master processor can read only data from the output DBB register, and cannot read and check data or commands which the master processor has written itself.

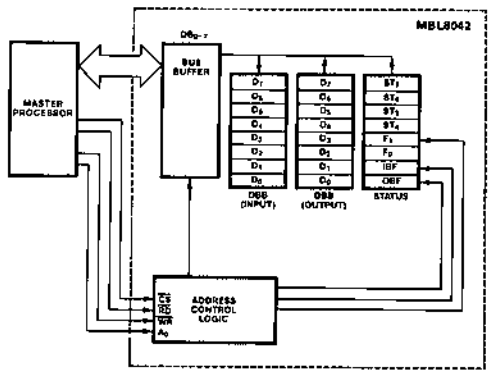
When MBL8042 writes data to the output DBB with the OUT DBB, A instruction, OBF is set

When DBB is read ($\overline{CS}$ = RD = $A_0$ = 0, $\overline{WR}$ = 1) by the master processor, OBF is reset. IBF is set when the master processor writes to the DBB, and reset when MBL8042 reads data from the DBB with IN A, DBB instruction.

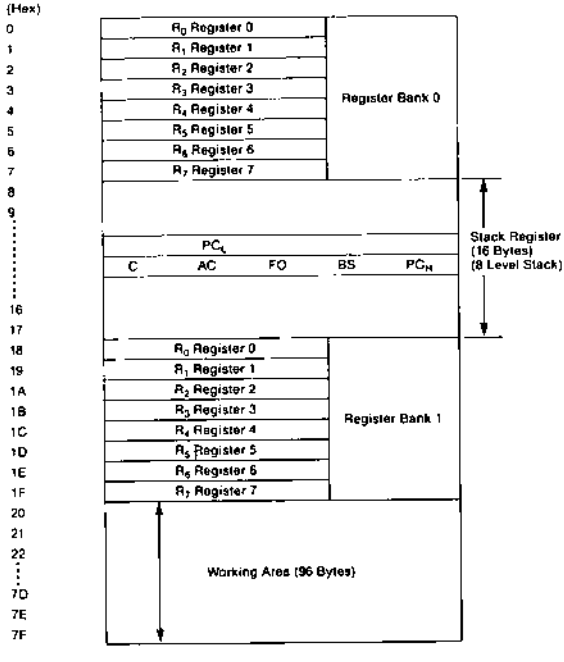
The internal status of the MBL8042 does not change when the status register contents are read out

| $\overline{CS}$ | $\overline{RD}$ | $\overline{WR}$ | $A_0$ | Description |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | Read DBB (Output) register. |
| 0 | 0 | 1 | 1 | Read Status Register. |
| 0 | 1 | 0 | 0 | Write DBB (Input) register (Data) |
| 0 | 1 | 0 | 1 | Write DBB (Input) register (Command). |
| 1 | x | x | x | Invalid. |

## Interface between MBL8042 and Master Processor



**Resident Data Memory Map (RAM)**




**Status Register (PSW)**

The Status Register is an 8-bit register configured as shown in the following figure. The upper four bits are used for flags to indicate the status of the MPU and when a sub-routine call or an interrupt occurs, the contents of the program counter is transferred to one of the 8 register pairs of the Stack Register as determined by the lower three bits of the Status Register. The remaining one bit is an unused bit.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| C | AC | $F_0$ | BS | 1 | $SP_2$ | $SP_1$ | $SP_0$ |
| ← Flags → | | | | (Unused Bit) | ← Stack Pointer → | | |

**Flags**

C (Carry): When an overflow occurs in the Accumulator, this bit is set to "1".

AC (Auxiliary Carry): When an overflow occurs from Bit 3 to Bit 4 in the accumulator, this bit is set to "1".

$F_0$ (User Flag): This flag can be controlled as a user flag by the proper instruction.

BS (Bank Select): This flag can be controlled to select a Register Bank by an instruction. When BS = 0, Register Bank 0 is selected. When BS = 1, the Register Bank 1 is selected.

**Stack Register (8 Level Capability)**

The Stack Register has 16 bytes of memory area in the built-in RAM. The stack Register consists of eight levels, i.e. a Stack level consists of two bytes as shown below.

SP (Stack Pointer). In the diagram below, "SP" indicates a Stack Pointer address to be used for the next sub-routine call or interrupt. "SP" is given an 8-bit code from the lower three bits of Status Register as follows:

$SP = 00001\underbrace{SP_2SP_1SP_0}_{\text{Status Register Bits 0 to 2}}$

$PC_n$ (Program Counter): "$PC_n$" indicates the contents of the n-th bit in the Program Counter.

**Interrupt Processing (IBF Interrupt, Timer/Counter Interrupt)**

There are two types of interrupt: the IBF interrupt and Timer/Counter interrupt.

If an interrupt occurs when the system is in "interrupt enable" status, the interrupt flag is set as soon as the current instruction is completed.

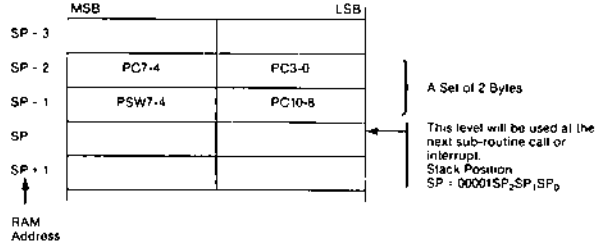
When the interrupt processing begins, the Status and Program Counter contents are first stored in the stack. Then, operation jumps to Address 3 in the case of the IBF interrupt and Address 7 in the case of a timer interrupt.

After the interrupt has been processed by a user program and RETR (Return and Restore Status) instruction has been executed, the Status and Program Counter contents stored in the stack are restored, the interrupt flag is reset and the system is ready to accept the next interrupt request.

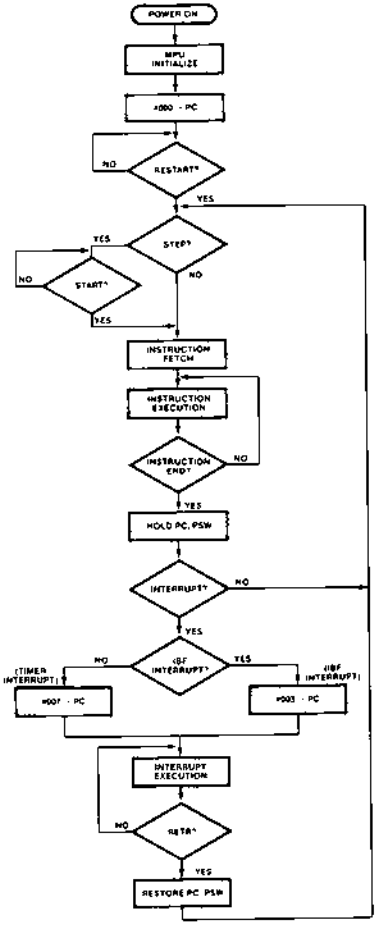
A Timer/Counter interrupt request occurs when the Timer/Counter overflow flag is set due to Timer/Counter overflow.

However, since the Timer/Counter interrupt request is masked by the IBF interrupt request, IBF interrupt has first priority.

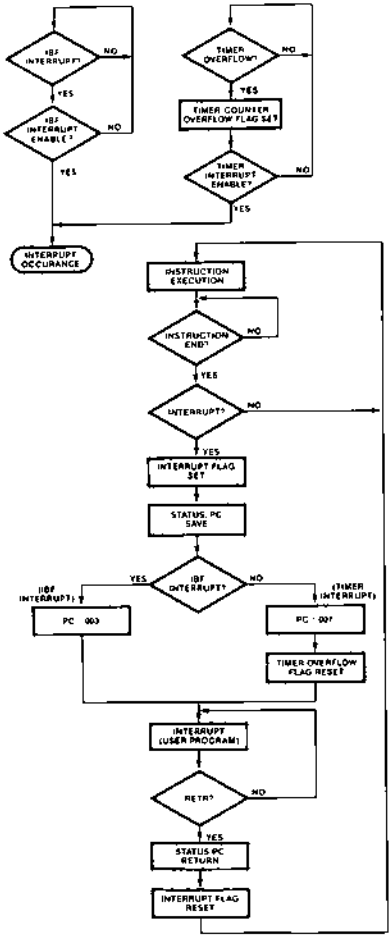
The Timer/Counter interrupt is enabled after the IBF interrupt has been executed and the system has become ready to receive the next interrupt request.



## Operation Flow Chart



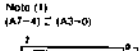
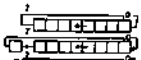
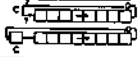
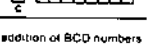

## Interrupt Flow Chart




4

## Instruction Set Summary

### Accumulator

| Operation | Mnemonic | OP Code | Byte | Cycle | Flag C | Flag AC | Note |
|---|---|---|---|---|---|---|---|
| Add register to A | ADD A, Rr | 6X | 1 | 1 | * | * | (A) ← (A) + (Rr) |
| Add data memory to A | ADD A, @R0 | 60 | 1 | 1 | * | * | (A) ← (A) + ((R0)) |
| | ADD A, @R1 | 61 | 1 | 1 | * | * | (A) ← (A) + ((R1)) |
| Add immediate to A | ADD A, #data | 03 | 2 | 2 | * | * | (A) ← (A) + data |
| Add register to A with Carry | ADDC A, Rr | 7X | 1 | 1 | * | * | (A) ← (A) + (Rr) + C |
| Add data memory to A with Carry | ADDC A, @R0 | 70 | 1 | 1 | * | * | (A) ← (A) + ((R0)) + C |
| | ADDC A, @R1 | 71 | 1 | 1 | * | * | (A) ← (A) + ((R1)) + C |
| Add immediate to A with Carry | ADDC A, #data | 13 | 2 | 2 | * | * | (A) ← (A) + data + C |
| AND register to A | ANL A, Rr | 5X | 1 | 1 | — | — | (A) ← (A) AND (Rr) |
| AND data memory to A | ANL A, @R0 | 50 | 1 | 1 | — | — | (A) ← (A) AND ((R0)) |
| | ANL A, @R1 | 51 | 1 | 1 | — | — | (A) ← (A) AND ((R1)) |
| AND immediate to A | ANL A, #data | 53 | 2 | 2 | — | — | (A) ← (A) AND data |
| OR register to A | ORL A, Rr | 4X | 1 | 1 | — | — | (A) ← (A) OR (Rr) |
| OR data memory to A | ORL A, @R0 | 40 | 1 | 1 | — | — | (A) ← (A) OR ((R0)) |
| | ORL A, @R1 | 41 | 1 | 1 | — | — | (A) ← (A) OR ((R1)) |
| OR immediate to A | ORL A, #data | 43 | 2 | 2 | — | — | (A) ← (A) OR data |
| Exclusive OR register to A | XRL A, Rr | DX | 1 | 1 | — | — | (A) ← (A) XOR (Rr) |
| Exclusive OR data memory to A | XRL A, @R0 | D0 | 1 | 1 | — | — | (A) ← (A) XOR ((R0)) |
| | XRL A, @R1 | D1 | 1 | 1 | — | — | (A) ← (A) XOR ((R1)) |
| Exclusive OR immediate to A | XRL A, #data | D3 | 2 | 2 | — | — | (A) ← (A) XOR data |
| Increment A | INC A | 17 | 1 | 1 | — | — | (A) ← (A) + 1 |
| Decrement A | DEC A | 07 | 1 | 1 | — | — | (A) ← (A) - 1 |
| Clear A | CLR A | 27 | 1 | 1 | — | — | (A) ← 0 |
| Complement A | CPL A | 37 | 1 | 1 | — | — | (A) ← $(\bar{A})$ |
| Decimal Adjust A | DA A | 57 | 1 | 1 | * | — | Note (1) |
| Swap nibbles of A | SWAP A | 47 | 1 | 1 | — | — | (A7~4) ⇄ (A3~0) |
| Rotate A Left | RL A | E7 | 1 | 1 | — | — |  |
| Rotate A Left through Carry | RLC A | F7 | 1 | 1 | * | — |  |
| Rotate A Right | RR A | 77 | 1 | 1 | — | — |  |
| Rotate A Right through Carry | RRC A | 67 | 1 | 1 | * | — |  |

**Note 1:** The accumulator value is adjusted to form BCD digits following the binary addition of BCD numbers
Operation Code X, Table 3
Flag* This flag is set or reset in the state after executed instruction

### Input/Output

| Operation | Mnemonic | OP Code | Byte | Cycle | Flag C | Flag AC | Note |
|---|---|---|---|---|---|---|---|
| Input port to A | IN A, P1 | 09 | 1 | 2 | — | — | (A) ← (P1) |
| | IN A, P2 | 0A | 1 | 2 | — | — | (A) ← (P2) |
| Output A to port | OUTL P1, A | 39 | 1 | 2 | — | — | (P1) ← (A) |
| | OUTL P2, A | 3A | 1 | 2 | — | — | (P2) ← (A) |
| AND immediate to port | ANL P1, #data | 99 | 2 | 2 | — | — | (P1) ← (P1) AND data |
| | ANL P2, #data | 9A | 2 | 2 | — | — | (P2) ← (P2) AND data |
| OR immediate to port | ORL P1, #data | 89 | 2 | 2 | — | — | (P1) ← (P1) OR data |
| | ORL P2, #data | 8A | 2 | 2 | — | — | (P2) ← (P2) OR data |
| Input DBB to A, clear IBF | IN A, DBB | 22 | 1 | 1 | — | — | (A) ← (DBB), (IBF) ← 0 |
| Output A to DBB, set OBF | OUT DBB, A | 02 | 1 | 1 | — | — | (DBB) ← (A), (OBF) ← 1 |
| A7~4 to bits 7~4 of Status | MOV STS, A | 90 | 1 | 1 | — | — | (STS7~4) ← (A7~4) |
| Input Expander port to A | MOVD A, $P_p$ | 0X | 1 | 2 | — | — | (A3~0) ← ($P_p$), (A7~4) ← 0 |
| Output A to Expander port | MOVD $P_p$, A | 3X | 1 | 2 | — | — | ($P_p$) ← (A3~0) |
| AND A to Expander port | ANLD $P_p$, A | 9X | 1 | 2 | — | — | ($P_p$) ← ($P_p$) AND (A3~0) |
| OR A to Expander port | ORLD $P_p$, A | 8X | 1 | 2 | — | — | ($P_p$) ← ($P_p$) OR (A3~0) |

Operation Code X, Table 2

## Instruction Set Summary
(Continued)

### Data Moves

| Operation | Mnemonic | OP Code | Byte | Cycle | Flag C | Flag AC | Note |
|---|---|---|---|---|---|---|---|
| Move register to A | MOV A, Rr | FX | 1 | 1 | — | — | (A) ← (Rr) |
| Move data memory to A | MOV A, @R0 | F0 | 1 | 1 | — | — | (A) ← ((R0)) |
| | MOV A, @R1 | F1 | 1 | 1 | — | — | (A) ← ((R1)) |
| Move immediate to A | MOV A, #data | 23 | 2 | 2 | — | — | (A) ← data |
| Move A to register | MOV Rr, A | AX | 1 | 1 | — | — | (Rr) ← (A) |
| Move A to data memory | MOV @R0, A | A0 | 1 | 1 | — | — | ((R0)) ← (A) |
| | MOV @R1, A | A1 | 1 | 1 | — | — | ((R1)) ← (A) |
| Move immediate to register | MOV Rr, #data | BX | 2 | 2 | — | — | (Rr) ← data |
| Move immediate to data memory | MOV @R0, #data | B0 | 2 | 2 | — | — | ((R0)) ← data |
| | MOV @R1, #data | B1 | 2 | 2 | — | — | ((R1)) ← data |
| Move PSW to A | MOV A, PSW | C7 | 1 | 1 | — | — | (A) ← (PSW) |
| Move A to PSW | MOV PSW, A | D7 | 1 | 1 | * | * | (PSW) ← (A) |
| Exchange A and register | XCH A, Rr | 2X | 1 | 1 | — | — | (A) ⇄ (Rr) |
| Exchange A and data memory | XCH A, @R0 | 20 | 1 | 1 | — | — | (A) ⇄ ((R0)) |
| | XCH A, @R1 | 21 | 1 | 1 | — | — | (A) ⇄ ((R1)) |
| Exchange digit of A and data memory | XCHD A, @R0 | 30 | 1 | 1 | — | — | (A3-0) ⇄ ((R0)3-0) |
| | XCHD A, @R1 | 31 | 1 | 1 | — | — | (A3-0) ⇄ ((R1)3-0) |
| Move to A from current page | MOVP A, @A | A3 | 1 | 2 | — | — | (A) ← ((A)) within page |
| Move to A from Page 3 | MOVP3 A, @A | E3 | 1 | 2 | — | — | (A) ← ((A)) within page 3 |

Operation Code X: Table 1
Flag*: This flag is set or reset in the state after executed instruction

### Timer/Counter

| Operation | Mnemonic | OP Code | Byte | Cycle | Flag C | Flag AC | Note |
|---|---|---|---|---|---|---|---|
| Read Timer/Counter | MOV A, T | 42 | 1 | 1 | — | — | (A) ← (T) |
| Load Timer/Counter | MOV T, A | 62 | 1 | 1 | — | — | (T) ← (A) |
| Start Timer | STRT T | 55 | 1 | 1 | — | — | |
| Start Counter | STRT CNT | 45 | 1 | 1 | — | — | |
| Stop Timer/Counter | STOP TCNT | 65 | 1 | 1 | — | — | |
| Enable Timer/Counter Interrupt | EN TCNTI | 25 | 1 | 1 | — | — | |
| Disable Timer/Counter Interrupt | DIS TCNTI | 35 | 1 | 1 | — | — | |

### Control

| Operation | Mnemonic | OP Code | Byte | Cycle | Flag C | Flag AC | Note |
|---|---|---|---|---|---|---|---|
| Enable DMA Handshake Lines | EN DMA | E5 | 1 | 1 | — | — | |
| Enable IBF Interrupt | EN I | 05 | 1 | 1 | — | — | |
| Disable IBF Interrupt | DIS I | 15 | 1 | 1 | — | — | |
| Enable Master Interrupts | EN FLAGS | F5 | 1 | 1 | — | — | |
| Select register bank 0 | SEL RB0 | C5 | 1 | 1 | — | — | (BS) ← 0 |
| Select register bank 1 | SEL RB1 | D5 | 1 | 1 | — | — | (BS) ← 1 |
| No Operation | NOP | 00 | 1 | 1 | — | — | |

4

## Instruction Set Summary
(Continued)

### Register

| Operation | Mnemonic | OP Code | Byte | Cycle | Flag C | Flag AC | Note |
|---|---|---|---|---|---|---|---|
| Increment register | INC Rr | 1X | 1 | 1 | — | — | (Rr) ← (Rr) + 1 |
| Increment data memory | INC @R0 | 10 | 1 | 1 | — | — | ((R0)) ← ((R0)) + 1 |
| | INC @R1 | 11 | 1 | 1 | — | — | ((R1)) ← ((R1)) + 1 |
| Decrement register | DEC Rr | CX | 1 | 1 | — | — | (Rr) ← (Rr) - 1 |

Operation Code X: Table 1

### Subroutine

| Operation | Mnemonic | OP Code | Byte | Cycle | Flag C | Flag AC | Note |
|---|---|---|---|---|---|---|---|
| Jump to Subroutine | CALL addr | %4 | 2 | 2 | — | — | Note (2) |
| Return | RET | 83 | 1 | 2 | — | — | Note (3) |
| Return and restore status | RETR | 93 | 1 | 2 | * | * | Note (4) |

Operation Code %: Table 3
Flag*: This flag is set or reset in the state after executed instruction

### Flags

| Operation | Mnemonic | OP Code | Byte | Cycle | Flag C | Flag AC | Note |
|---|---|---|---|---|---|---|---|
| Clear Carry | CLR C | 97 | 1 | 1 | 0 | — | (C) ← 0 |
| Complement Carry | CPL C | A7 | 1 | 1 | CP | — | (C) ← $(\overline{C})$ |
| Clear Flag 0 | CLR F0 | 85 | 1 | 1 | — | — | (F0) ← 0 |
| Complement Flag 0 | CPL F0 | 95 | 1 | 1 | — | — | (F0) ← $(\overline{F0})$ |
| Clear Flag 1 | CLR F1 | A5 | 1 | 1 | — | — | (F1) ← 0 |
| Complement Flag 1 | CPL F1 | B5 | 1 | 1 | — | — | (F1) ← $(\overline{F1})$ |

Flag Z: Reset CP: Invert

### Branch

| Operation | Mnemonic | OP Code | Byte | Cycle | Flag C | Flag AC | Note |
|---|---|---|---|---|---|---|---|
| Jump unconditional | JMP addr | %4 | 2 | 2 | — | — | Unconditional Branch |
| Jump indirect | JMPP @A | B3 | 1 | 2 | — | — | Unconditional Branch Note (5) |
| Decrement register and jump | DJNZ Rr,addr | Ex | 2 | 2 | — | — | (Rr) ≠ 0 Note (6) |
| Jump on Carry = 1 | JC addr | F6 | 2 | 2 | — | — | (C) = 1 |
| Jump on Carry = 0 | JNC addr | E6 | 2 | 2 | — | — | (C) = 0 |
| Jump on A Zero | JZ addr | C6 | 2 | 2 | — | — | (A) = 0 |
| Jump on A not Zero | JNZ addr | 96 | 2 | 2 | — | — | (A) ≠ 0 |
| Jump on T0 = 1 | JT0 addr | 36 | 2 | 2 | — | — | (T0) = H |
| Jump on T0 = 0 | JNT0 addr | 26 | 2 | 2 | — | — | (T0) = L |
| Jump on T1 = 1 | JT1 addr | 56 | 2 | 2 | — | — | (T1) = H |
| Jump on T1 = 0 | JNT1 addr | 46 | 2 | 2 | — | — | (T1) = L |
| Jump on F0 = 1 | JF0 addr | B6 | 2 | 2 | — | — | (F0) = 1 |
| Jump on F1 = 1 | JF1 addr | 76 | 2 | 2 | — | — | (F1) = 1 |
| Jump on Timer Flag = 1, Clear Flag | JTF addr | 16 | 2 | 2 | — | — | (TF) = 1 |
| Jump on IBF Flag = 0 | JNIBF addr | D6 | 2 | 2 | — | — | (IBF) = 0 |
| Jump on OBF Flag = 1 | JOBF addr | 86 | 2 | 2 | — | — | (OBF) = 1 |
| Jump on Accumulator Bit | JBb addr | %2 | 2 | 2 | — | — | (Ab) = 1 |

Operation Code X: Table 1
% Table 3

Note 2: Call addr
((SP)) ← (PC), (PSW7~4)
(SP) ← (SP) + 1
(PC10 ~ 8) ← $A_H$
(PC7~0) ← $A_L$

Note 3: RET
(SP) ← (SP) - 1
(PC) ← ((SP))

Note 4: RETR
(SP) ← (SP) - 1
(PC) ← ((SP))
(PSW7~4) ← ((SP))

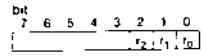
Note 5: JMPP @
(PC7~0) ← ((A))

Note 6: DJNZ Rr, addr
(Rr) ← (Rr) - 1
if (Rr) ≠ 0 (PC7~0) ← addr
if (Rr) = 0 Execute next instruction

## Instruction Set Summary
(Continued)

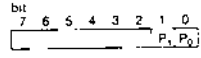
**OP Code Of Register Access (Table 1)**

| Mnemonic | Rr | R0 | R1 | R2 | R3 | R4 | R5 | R6 | R7 |
|---|---|---|---|---|---|---|---|---|---|
| ADD A,Rr | | 68 | 69 | 6A | 6B | 6C | 6D | 6E | 6F |
| ADDC A,Rr | | 78 | 79 | 7A | 7B | 7C | 7D | 7E | 7F |
| ANL A,Rr | | 58 | 59 | 5A | 5B | 5C | 5D | 5E | 5F |
| DEC Rr | | C8 | C9 | CA | CB | CC | CD | CE | CF |
| DJNZ Rr addr | | E8 | E9 | EA | EB | EC | ED | EE | EF |
| INC Rr | | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |
| MOV A,Rr | | F8 | F9 | FA | FB | FC | FD | FE | FF |
| MOV Rr,A | | A8 | A9 | AA | AB | AC | AD | AE | AF |
| MOV Rr, #data | | B8 | B9 | BA | BB | BC | BD | BE | BF |
| ORL A, Rr | | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F |
| XCH A,Rr | | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F |
| XRL A,Rr | | D8 | D9 | DA | DB | DC | DD | DE | DF |

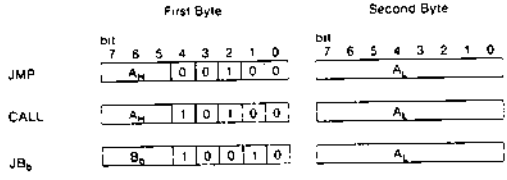



**OP Code Of Expander (Table 2)**

| Mnemonic | PP | P4 | P5 | P6 | P7 |
|---|---|---|---|---|---|
| ANLD $P_p$, A | | 9C | 9D | 9E | 9F |
| MOVD A, $P_p$ | | 0C | 0D | 0E | 0F |
| MOVD $P_p$, A | | 3C | 3D | 3E | 3F |
| ORLD $P_p$, A | | 8C | 8D | 8E | 8F |




**OP Code Of JMP, CALL, JBb (Table 3)**




$A_H$: Address $A_{10}$, $A_9$, $A_8$
$A_L$: Address $A_7$ to $A_0$
$B_b$: b-th Bit on Accumulator

4

## Instruction Codes

| H \ L | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | NOP | | OUT DBB,A | ADD A, # | JMP 0 * * | EN I | | DEC A | | IN A, P1 | IN A, P2 | | MOVD A, P4 | MOVD A, P5 | MOVD A, P6 | MOVD A, P7 |
| 1 | INC @R0 | INC @R1 | JB0 addr | ADDC A, # | CALL 0 * * | DIS I | JTF addr | INC A | INC R0 | INC R1 | INC R2 | INC R3 | INC R4 | INC R5 | INC R6 | INC R7 |
| 2 | XCH A, @R0 | XCH A, @R1 | IN A, DBB | MOV A, # | JMP 1 * * | EN TCNTI | JNT0 addr | CLR A | XCH A, R0 | XCH A, R1 | XCH A, R2 | XCH A, R3 | XCH A, R4 | XCH A, R5 | XCH A, R6 | XCH A, R7 |
| 3 | XCHD A, @R0 | XCHD A, @R1 | JB1 addr | | CALL 1 * * | DIS TCNTI | JT0 addr | CPL A | | OUTL P1, A | OUTL P2, A | | MOVD P4, A | MOVD P5, A | MOVD P6, A | MOVD P7, A |
| 4 | ORL A, @R0 | ORL A, @R1 | MOV A, T | ORL A, # | JMP 2 * * | STRT CNT | JNT1 addr | SWAP A | ORL A, R0 | ORL A, R1 | ORL A, R2 | ORL A, R3 | ORL A, R4 | ORL A, R5 | ORL A, R6 | ORL A, R7 |
| 5 | ANL A, @R0 | ANL A, @R1 | JB2 addr | ANL A, # | CALL 2 * * | STRT T | JT1 addr | DA A | ANL A, R0 | ANL A, R1 | ANL A, R2 | ANL A, R3 | ANL A, R4 | ANL A, R5 | ANL A, R6 | ANL A, R7 |
| 6 | ADD A, @R0 | ADD A, @R1 | MOV T, A | | JMP 3 * * | STOP TCNT | | RRC A | ADD A, R0 | ADD A, R1 | ADD A, R2 | ADD A, R3 | ADD A, R4 | ADD A, R5 | ADD A, R6 | ADD A, R7 |
| 7 | ADDC A, @R0 | ADDC A, @R1 | JB3 addr | | CALL 3 * * | | JF1 addr | RR A | ADDC A, R0 | ADDC A, R1 | ADDC A, R2 | ADDC A, R3 | ADDC A, R4 | ADDC A, R5 | ADDC A, R6 | ADDC A, R7 |
| 8 | | | | RET | JMP 4 * * | CLR F0 | JOBF addr | | | ORL P1, # | ORL P2, # | | ORLD P4, A | ORLD P5, A | ORLD P6, A | ORLD P7, A |
| 9 | MOV STS, A | | JB4 addr | RETR | CALL 4 * * | CPL F0 | JNZ addr | CLR C | | ANL P1, # | ANL P2, # | | ANLD P4, A | ANLD P5, A | ANLD P6, A | ANLD P7, A |
| A | MOV @R0, A | MOV @R1, A | | MOVP A, @A | JMP 5 * * | CLR F1 | | CPL C | MOV R0, A | MOV R1, A | MOV R2, A | MOV R3, A | MOV R4, A | MOV R5, A | MOV R6, A | MOV R7, A |
| B | MOV @R0, # | MOV @R1, # | JB5 addr | JMPP @A | CALL 5 * * | CPL F1 | JF0 addr | | MOV R0, # | MOV R1, # | MOV R2, # | MOV R3, # | MOV R4, # | MOV R5, # | MOV R6, # | MOV R7, # |
| C | | | | | JMP 6 * * | SEL RB0 | JZ addr | MOV A, PSW | DEC R0 | DEC R1 | DEC R2 | DEC R3 | DEC R4 | DEC R5 | DEC R6 | DEC R7 |
| D | XRL A, @R0 | XRL A, @R1 | JB6 addr | XRL A, # | CALL 6 * * | SEL RB1 | JNIBF addr | MOV PSW, A | XRL A, R0 | XRL A, R1 | XRL A, R2 | XRL A, R3 | XRL A, R4 | XRL A, R5 | XRL A, R6 | XRL A, R7 |
| E | | | | MOVP3 A, @A | JMP 7 * * | EN DMA | JNC addr | RL A | DJNZ R0, addr | DJNZ R1, addr | DJNZ R2, addr | DJNZ R3, addr | DJNZ R4, addr | DJNZ R5, addr | DJNZ R6, addr | DJNZ R7, addr |
| F | MOV A, @R0 | MOV A, @R1 | JB7 addr | | CALL 7 * * | EN FLAGS | JC addr | RLC A | MOV A, R0 | MOV A, R1 | MOV A, R2 | MOV A, R3 | MOV A, R4 | MOV A, R5 | MOV A, R6 | MOV A, R7 |

* Immediate data

1 Byte, 1 Cycle Instruction

1 Byte, 2 Cycle Instruction

2 Byte, 2 Cycle Instruction

## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$, $V_{DD}$ | -0.3 to +7.0 | V |
| Input Voltage | $V_{IN}$ | -0.3 to +7.0 | V |
| Operating Temperature | $T_A$ | 0 to +70 | °C |
| Storage Temperature | $T_{stg}$ | -55 to +150 | °C |
| Power Dissipation | $P_D$ | 1.5 | W |

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational specifications of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Recommended Operating Conditions

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$, $V_{DD}$ | +5.0 ±10% | V |
| | $V_{SS}$ | 0 | V |
| Operating Temperature | | 0 to +70 | °C |

## DC Characteristics

($T_A$ = 0°C to +70°C, $V_{CC}$ = $V_{DD}$ = 5.0V ± 10%, $V_{SS}$ = 0V)

| Parameter | | Symbol | Test Conditions | Value Min. | Value Max. | Unit |
|---|---|---|---|---|---|---|
| Input Low Voltage | All Except XTAL1, 2, $\overline{RESET}$ | $V_{IL}$ | | -0.3 | 0.8 | V |
| | XTAL1,2, $\overline{RESET}$ | $V_{IL1}$ | | -0.3 | 0.6 | V |
| Input High Voltage | All Except XTAL1, 2, $\overline{RESET}$ | $V_{IH}$ | | 2.0 | $V_{CC}$ | V |
| | XTAL1,2, $\overline{RESET}$ | $V_{IH1}$ | | 3.8 | $V_{CC}$ | V |
| Output Low Voltage | $DB_0$ to $DB_7$ | $V_{OL}$ | $I_{OL}$ = 2.0mA | | 0.45 | V |
| | P10-P17, P20-P27 SYNC | $V_{OL1}$ | $I_{OL}$ = 1.6mA | | 0.45 | V |
| | PROG | $V_{OL2}$ | $I_{OL}$ = 1.0mA | | 0.45 | V |
| Output High Voltage | $DB_0$ to $DB_7$ | $V_{OH}$ | $I_{OH}$ = -400μA | 2.4 | | |
| | All other outputs | $V_{OH1}$ | $I_{OH}$ = -50μA | 2.4 | | |
| Input Leakage Current | $T_0$, $T_1$, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, $A_0$, EA | $I_{IL}$ | $V_{SS} \leq V_{IN} \leq V_{CC}$ | | ±10 | μA |
| Output Leakage Current | $DB_0$ to $DB_7$ (High Z State) | $I_{OL}$ | $V_{SS}$+0.45V ≤ $V_{IN} \leq V_{CC}$ | | ±10 | μA |
| Input Low Current | $P1_0$ to $P1_7$, $P2_0$ to $P2_7$ | $I_{LI}$ | $V_{IL}$ = 0.8V | | 0.5 | mA |
| | $\overline{RESET}$, $\overline{SS}$ | $I_{LI1}$ | $V_{IL}$ = 0.8V | | 0.2 | mA |
| $V_{DD}$ Supply Current | | $I_{DD}$ | | | 15 | mA |
| Supply Current | | $I_{CC}$ + $I_{DD}$ | | | 125 | mA |

4

## AC Characteristics

($T_A$ = 0°C to +70°C, $V_{CC}$ = $V_{DD}$ = 5.0V ± 10%, $V_{SS}$ = 0V)

**Data Bus Buffer Register Read (Refer to the Fig. 1)**

| Parameter | | Symbol | Test Conditions | Value Min. | Value Max. | Unit |
|---|---|---|---|---|---|---|
| $\overline{CS}$, $A_0$ Setup Time (to $\overline{RD}$) | | $t_{AR}$ | | 0 | | ns |
| $\overline{CS}$, $A_0$ Hold Time (from $\overline{RD}$) | | $t_{RA}$ | | 0 | | ns |
| $\overline{RD}$ Pulse Width | | $t_{RR}$ | | 160 | | ns |
| Data Delay Time (from $\overline{CS}$, $A_0$) | | $t_{AD}$ | $C_L$ = 150pF | | 130 | ns |
| Data Delay Time (from $\overline{RD}$) | | $t_{RD}$ | $C_L$ = 150pF | | 130 | ns |
| Data Floating Time (from $\overline{RD}$) | | $t_{DF}$ | | | 85 | ns |
| Cycle Time | MBL8042N | $t_{CY}$ | * | 2.5 | 15.0 | μs |
| | MBL8042H | | ** | 1.25 | 15.0 | μs |

*$t_{CY}$ = 2.50μs at 6MHz XTAL (N version)
**$t_{CY}$ = 1.25μs at 12MHz XTAL (H version)

**Data Bus Buffer Register Write (Refer to the Fig. 2)**

| Parameter | Symbol | Test Conditions | Value Min. | Value Max. | Unit |
|---|---|---|---|---|---|
| $\overline{CS}$, $A_0$ Setup Time (to $\overline{WR}$) | $t_{AW}$ | | 0 | | ns |
| $\overline{CS}$, $A_0$ Hold Time (from $\overline{WR}$) | $t_{WA}$ | | 0 | | ns |
| $\overline{WR}$ Pulse Width | $t_{WW}$ | | 160 | | ns |
| Data Setup Time (to $\overline{WR}$) | $t_{DW}$ | | 130 | | ns |
| Data Hold Time (from $\overline{WR}$) | $t_{WD}$ | | 0 | | ns |

**Port 2 (Refer to the Fig. 3)***

| Parameter | Symbol | MBL8042N Min. | MBL8042N Max. | MBL8042H Min. | MBL8042H Max. | Unit |
|---|---|---|---|---|---|---|
| Port Control Setup before Falling Edge of PROG Time (to PROG) | $t_{CP}$ | 100 | | 110 | | ns |
| Port Control Hold after Falling Edge of PROG Time (from PROG) | $t_{PC}$ | 60 | | 100 | | ns |
| Output Data Setup Time (to PROG) | $t_{DP}$ | 200 | | 250 | | ns |
| Output Data Hold Time (from PROG) | $t_{PD}$ | 20 | | 65 | | ns |
| Input Data Hold Time (from PROG) | $t_{PF}$ | 0 | 150 | 0 | 150 | ns |
| PROG Time P2 Input Must be Valid | $t_{PR}$ | | 650 | | 810 | ns |
| PROG Pulse Width | $t_{PP}$ | 700 | | 1200 | | ns |

*at 6MHz XTAL for N version
at 12MHz XTAL for H version

## AC Characteristics
(Continued)

**DMA Characteristics (Refer to the Fig. 4)**

| Parameter | Symbol | Test Conditions | Value Min. | Value Max. | Unit |
|---|---|---|---|---|---|
| $\overline{DACK}$ Setup Time (to $\overline{RD}$, $\overline{WR}$) | $t_{ACC}$ | | 0 | | ns |
| $\overline{DACK}$ Hold Time (from $\overline{RD}$, $\overline{WR}$) | $t_{CAC}$ | | 0 | | ns |
| Input Data Delay Time (from $\overline{DACK}$) | $t_{ACD}$ | $C_L$ = 150pF | | 130 | ns |
| DRQ Clear Time (from $\overline{RD}$, $\overline{WR}$) | $t_{CRQ}$ | | | 100 | ns |

AC Test Conditions
$V_{IL}$ = 0.8V (All except XTAL1, 2, $\overline{RESET}$)
= 0.6V (XTAL1, 2, $\overline{RESET}$)
$V_{IH}$ = 2.0V (All except XTAL1, 2, $\overline{RESET}$)
= 3.8V (XTAL1, 2, $\overline{RESET}$)
$V_{OL}$ = 0.45V
$V_{OH}$ = 2.4V

Output Load
D0-D7 $C_L$ = 150pF
All other outputs $C_L$ = 80pF

## Timing Diagram

**Figure 1. Data Bus Buffer (DBB) Read Operation**

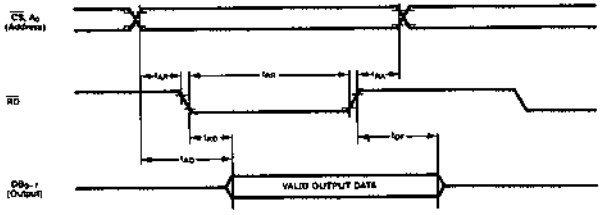
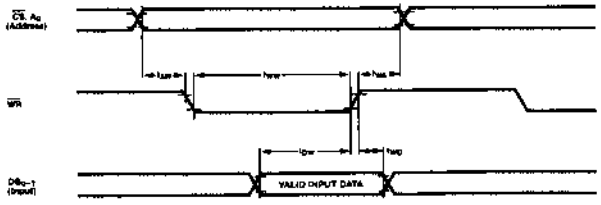



**Figure 2. Data Bus Buffer (DBB) Write Operation**




4

## Timing Diagram
(Continued)

Figure 3. Port 2 (Lower 4 Bits) Operation in Connection with I/O Expander

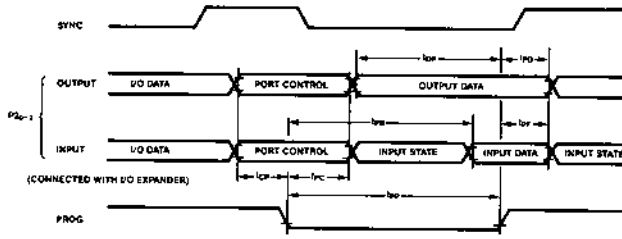
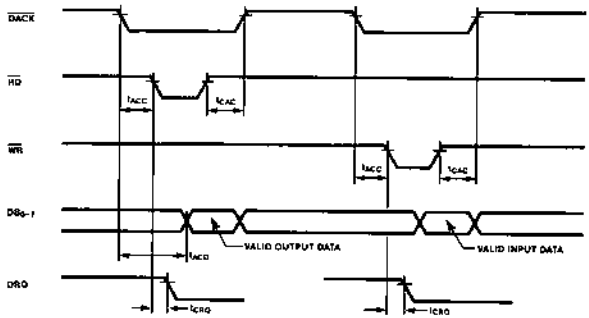
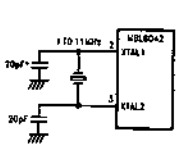



Figure 4. DMA Operation



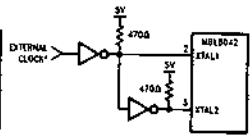

## Oscillation Circuits

Crystal Oscillator




* Including stray capacitances

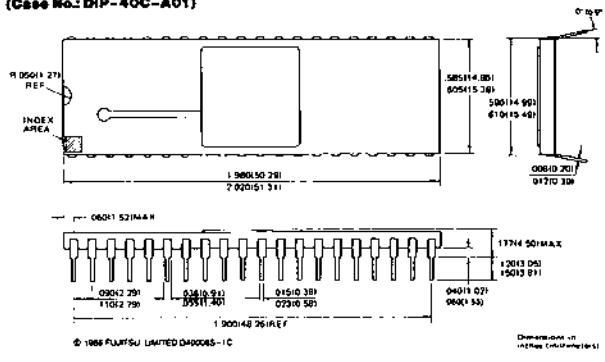
External Clock Driver



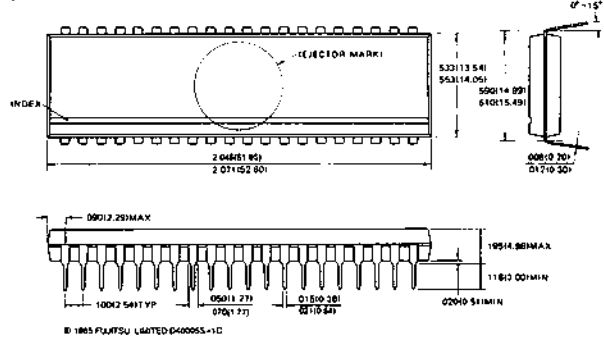

* Both high and low times should be more than 35 % of the cycle time, and rise and fall times should be less than 20 ns

**Package Dimensions**
Dimensions in inches
(millimeters)

**40-Lead Ceramic**
**(Metal Seal)**
**Dual In-Line Package**
**(Case No.: DIP-40C-A01)**




**40-Lead Plastic**
**Dual In-Lane Package**
**(Case No.: DIP-40P-M01)**



Power Supply

3000 NL IMC AT1043 Power Supply

# 3000 NL IMC AT1043 Power Supply
## Contents

**Section** **Page**

**Circuit Description**


General ..... 1
AC Input Circuit ..... 1
Inverter ..... 1
Feedback Circuit and +5 Volt Output ..... 2
+12 Volt Output ..... 3
Overcurrent Protection ..... 4
Overvoltage Protection ..... 4
-12 and -5 Volt Outputs ..... 5
AC Low Detection ..... 5
+5 Volt Undervoltage Detection ..... 5
Power Good Startup ..... 5

## Circuit Description:

### General

The IMC power supply consists of two printed circuit boards which are subsequently mounted in a chassis assembly. An IEC connector, an on/off switch and an input voltage range switch are mounted on the chassis.

### AC Input Circuit

Incoming AC power enters the power unit via the IEC connector and the double pole switch and is fused by F1 (mounted on the small EMI board). Inrush current limiting is provided by means of thermistor RT1. Conducted EMI is kept within the class B limits of the FCC/VDE by means of the filter comprising inductors L1,L2,L3 and capacitors C1,C2,C3,C4.

The output of the EMI filter is fed to a bridge rectifier consisting of CR1,CR2,CR3,CR4, whose output is smoothed in the two series bulk capacitors C5 and C6 mounted on the main board. For 200-265 volt operation the rectifiers are used in the bridge configuration. For 100-132 volt operation select switch S2 is closed, which connects the neutral AC line direct to the center point of C5 and C6 allowing CR1 and CR3 to function as a voltage doubler. The subsequent circuitry, therefore, sees a similar DC voltage across C5 and C6 irrespective of which input voltage range the unit is operating in.

### The Inverter

Discontinuous mode flyback topology is utilized in the inverter circuit, transistor Q5 being the inverter power switch. Transformer T1 is the inverter transformer, and 1-2 is the primary winding. As a flyback circuit can generate peak voltages in access of 400 volts it is essential to ensure that the current in the switch has decayed to a sufficently low voltage before the voltage exceeds the reverse biased safe operating range. This is achieved by means of the snubber circuit C7,CR5 and R7 and R8. In addition, winding 3-4 is a clamp winding which returns the energy in the leakage inductance back to the bulk capacitors via diode CR6 and thus limits the peak collector voltage. The primary and clamp windings are tightly coupled, but there is some leakage inductance between them, which is handled by an additional snubber circuit C8 and R9,10,11,12.

Reverse bias for the switch transistor Q5 is obtained by means of the diodes CR11,CR12,CR13, capacitor C12 and resistor R23 in the emitter circuit. Resistors R21,22 monitor the current through the switch transistor and allow turn off if a safe value is exceeded.

The inverter circuit is self-oscillating, base drive being obtained from winding 5-6 on T1. This is fed via inductor L4 and resistor R26 to control the magnitude of the longer conduction periods. Resistors R2,R3,R4 provide starting bias for the inverter and C13 prevents this starting bias from being loaded down by the drive circuit and also provides a timing function when the inverter is operating in a short circuit mode. Zener diode CR17 prevents excessive voltage being developed across C13. The secondary winding on L4 is used to ensure that L4 is discharged during the flyback portion of the cycle.

Transistors Q3 and Q4 are an NPN-PNP regenerative pair whose function is to terminate a forward conduction cycle in Q5 through by-passing the base drive current to ground upon receipt of a pulse from the feedback transformer T3. Q3 and Q4 are also fired by means of zener diode CR30 in the event of a large current flowing in the emitter circuit of Q5, and, in addition, by the voltage developed across the resistors R24 and R25, and across the current monitoring resistors R21 and R22. Resistor R27 provides a feed forward signal to reduce the current limit point at high line.

The forward conduction cycle may also be terminated by an additional NPN-PNP pair, Q1,and Q2, which trigger Q3 and Q4 upon receiving a signal from the current transformer T2. The purpose of this is described later.

**Feedback Circuit and +5 Volt Output**

The feedback loop for the inverter operates around the +5 volt output. Secondary winding 9-10 of T1 drives the schottky dual rectifier CR20, having both elements in parallel to handle the current. Capacitors C19,C20,C21 and C22 provide the required energy storage and ripple current handling capacity for this output. Inductor L5 and capacitors C23 and C24 provide additional ripple reduction of the output voltage. Resistor R30 is included to monitor output current.

U5 is a TL431 shunt regulator chip which is used to control the feedback loop. Resistors R55,R56,R57 and R58 attenuate the 5 volt output so that at the wiper of R57 the voltage is equal to the reference voltage of U5, 2.5 volts. Any deviation of the output from the required 5 volts will then result in an amplified error signal appearing across resistor R53. Resistor R54 and capacitors C36,C37 and C38 are included to shape the frequency response of the overall feedback loop. During the flyback portion of the inverter cycle capacitor C35 is charged to a more positive value than the cut-off voltage of the base of Q8 by means of resistor R50 connected to the +5 volt secondary winding of T1. As the flyback phase ends C13 then discharges through R50 and resistors R52 and R72. The rate at which this discharge takes place will depend upon the amplified error signal at the output of U5. Once C13 has discharged sufficently transistor Q8 will conduct and transmit a pulse via T3 to the NPN-PNP pair Q3 and Q4 which will terminate the forward stroke of the inverter. The error signal, therefore, controls the "on" period of the inverter. This method of control results in some variation of frequency with variation in load and line.

**+12 Volt Output**

Secondary winding 7-8 of T1 together with rectifier CR20 and capacitors C25 and C26 develop a voltage which is subsequently independently regulated to provide +12 volts. Darlington transistor Q6 is the linear regulating transistor, and is driven directly from the pin 8 output of the op-amp U3. Zener diode CR23 provides an independent reference which is connected to the inverting input pin 9 of U3. R44, R45 and R46 provide an attenuator to reduce the output voltage to the level of the reference voltage at the wiper of R45, which is connected to the non-inverting input, pin 10 of U3. C29 and C31 stabilize the feedback loop of the linear regulator. Capacitors C32 and C34 provide the required low impedance to enable the loop to be stabilized irrespective of load impedance. C30 is a local decoupling capacitor for the chip bias. Resistor R41 provides a means of monitoring the load current of the +12 volt output.

**Overcurrent Protection**

Over-current protection for the +5 and +12 volt rails is similar. Consider the +5 volt output. Resistors R31 and R32 attenuate the upstream voltage across R30 such that during normal operation the voltage at the junction of R31 and R32 is less than the voltage at the downstream side of R30. This voltage difference is applied to the differential inputs of op amp U3 at pins 2 and 3 in such a manner that the output of U3 pin 1 is normally high. In the event of a current overload the voltage at the junction of R31 and R32 will increase above that of the downstream end of R30 and the output of U3 pin 1 will go low. This will cause transistor Q7 to conduct and fire SCR Q10, which is connected in series with the primary of the current transformer T2 across the unregulated +12 volt output. The current in T2 will initiate turn off of the forward cycle and in addition the high load current causing a change in the charge on C12 and C13. This will result in the unit firing for a few cycles and then being quiescent for a period, that is the output will vary, resulting in a low average current flowing in the load and power supply circuits.

Overcurrent outputs at pins 1 and 14 of U3, representing the +5 and +12 volt rails, are "ORed" by diodes CR24 and CR25 so that a current overload in either rail may initiate the variable mode. Also ORed with this signal are the outputs from pin 7 of U3 via diode CR26, and pin 13 of U4, which as an open collecter comparator does not need an ORing diode. These two circuits provide overtemperature protection by varing, the temperature sensing elements being PTC thermistors RT2 and RT3 which are mounted on the heatsinks of the +5 volt rectifier CR20 and the +12 volt linear regulator Q6.

**Overvoltage Protection**

Overvoltage protection for the +5 volt output is given by zener diode CR22 and diode CR21, which in the event of an overvoltage condition will directly fire the gate of SCR Q10. As the +12 volt unregulated line is piggy-backed on the +5 volt rail this reduces both rails to a safe value.

### -12 Volt and -5 Volt Outputs

The -12 volt and -5 volt outputs are both developed from a common winding 11-12 on T1, which is rectified and smoothed by CR18 and C14. The resulting DC is independently regulated by monolithic TO220 regulator U1 to provide the -12 volt output, and the -12 volt rail is then re-regulated by another regulator U2 to provide the -5 volt output. Both of these outputs are independently and individually overload protected.

### AC Low Detection

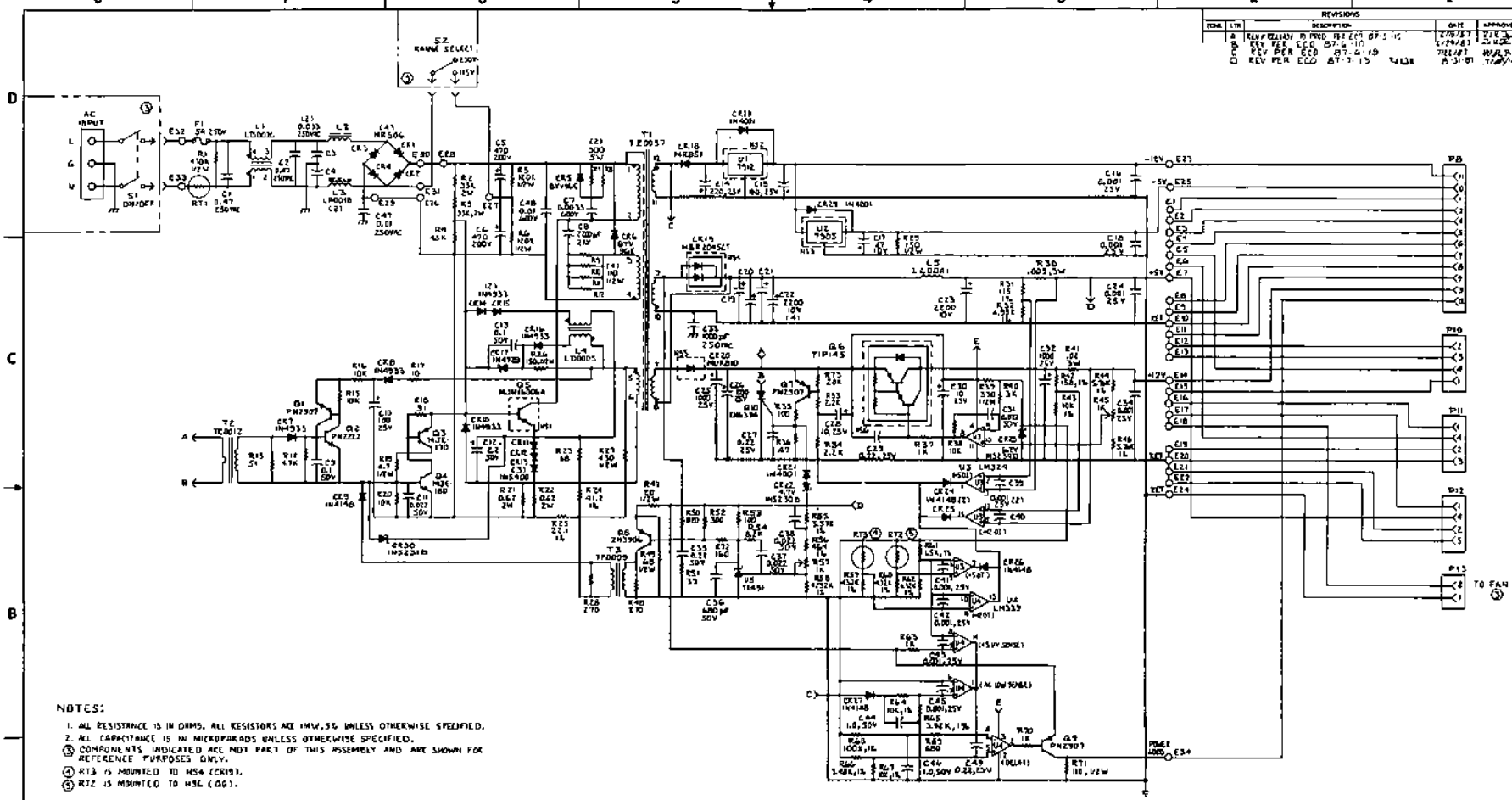
Sensing of low AC line is accomplished by modeling the voltage on the bulk storage capacitors by rectifying the voltage appearing on winding 11-12 of T1 during the forward stroke of the inverter using rectifier CR27 and capacitor C65. Resistors R64 and R65 compare the resulting voltage with the reference voltage from CR23, and in the event that the measured voltage is low, pin 1 of comparator U4 will go low. This in turn will cause pin 2 of U4 to go high, turning off Q9 and resulting in the Power Good signal falling to zero.

### +5 Volt Undervoltage Detection

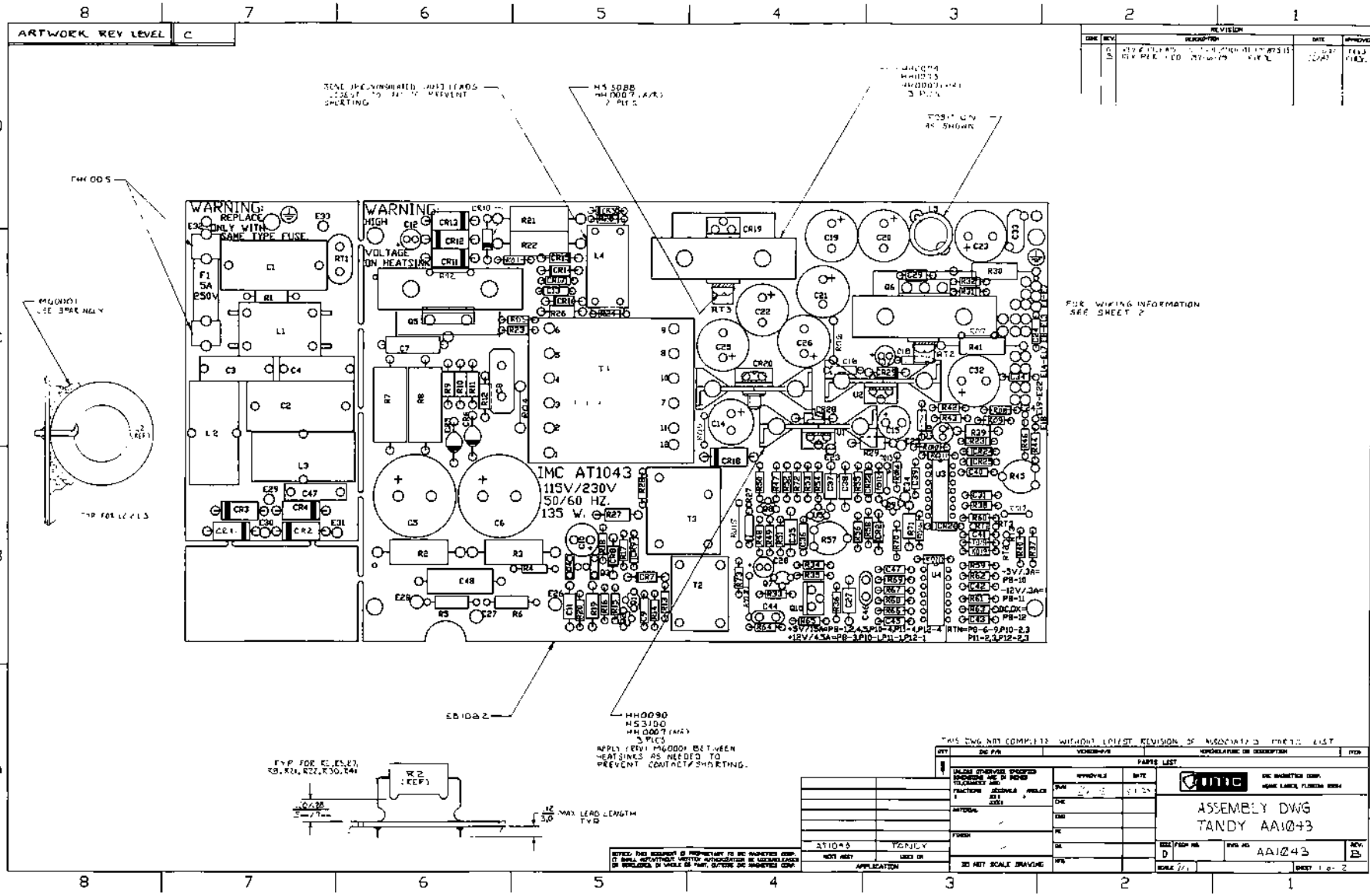
Resistors R51 and R52 attenuate the reference and this voltage is then compared with the +5 volt rail at pins 8 and 9 of comparator U4. If the +5 volt output is low then pin 14 of U4 will go low, pin 2 will be driven high and the Power Good signal will go low.

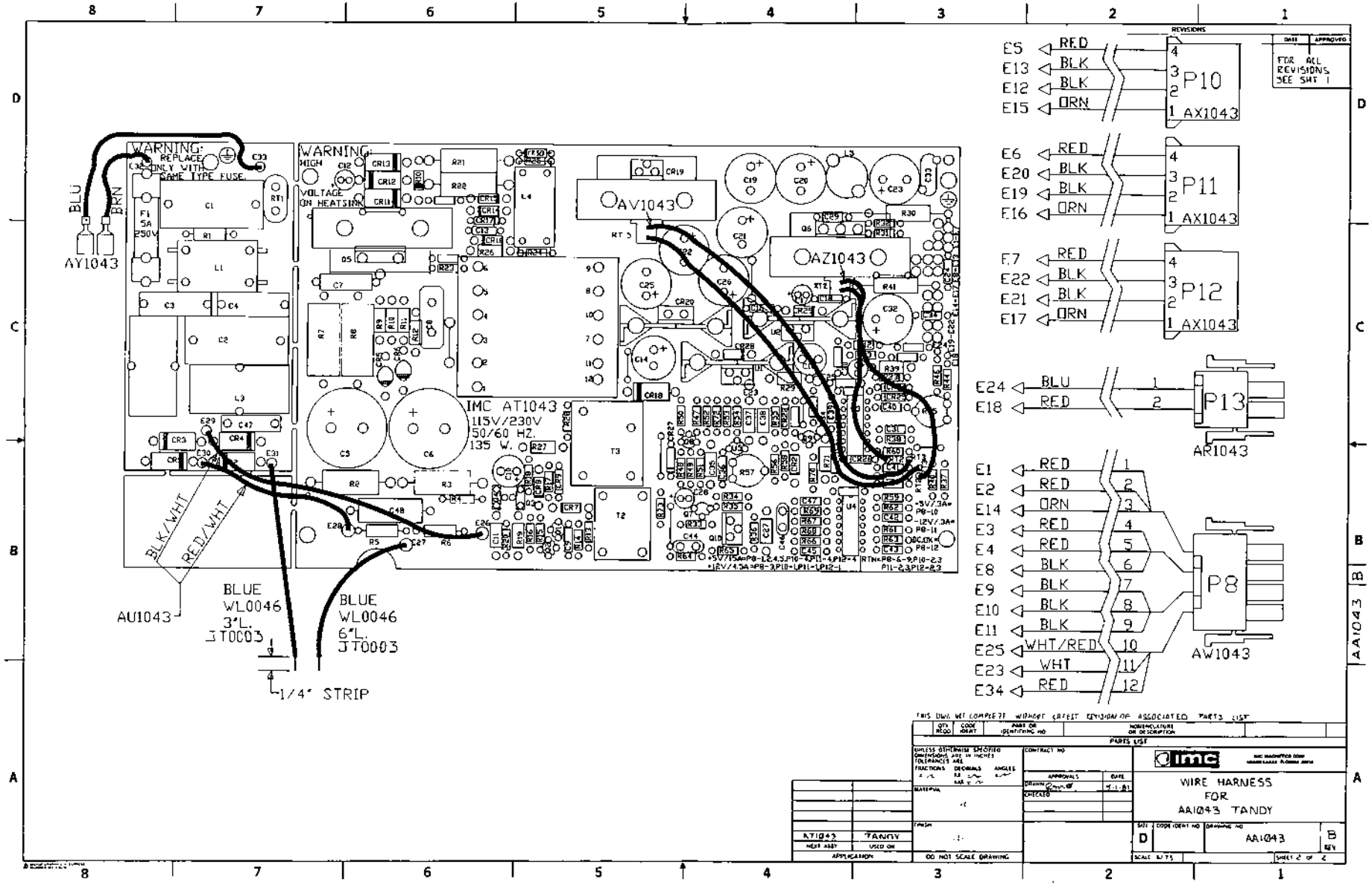
### Power Good Start Up

During the start up condition, capacitors C46,C49 and the associated resistors delay the transition of pin 2 of U4 to a low condition, thus delaying the assertion of Power Good until all rails have had time to become established.




| LAST USED | C49 | CR30 | E31 | F1 | L5 | P13 | Q10 | RT3 | RT3 | S2 | T3 | HS6 | U5 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NOT USED | | | | | | P1-7,9 | | | | | | | |


ARTWORK REV LEVEL C
WARNING: REPLACE ONLY WITH SAME TYPE FUSE.
WARNING: HIGH VOLTAGE ON HEATSINK
IMC AT1043
115V/230V
50/60 HZ.
135 W.
FOR WIRING INFORMATION SEE SHEET 2
ASSEMBLY DWG
TANDY AA1043
AA1043
B


WARNING: REPLACE ONLY WITH SAME TYPE FUSE.
WARNING HIGH VOLTAGE ON HEATSINK
AY1043
BLU
BRN
AV1043
AZ1043
IMC AT1043
115V/230V
50/60 HZ.
135 W.
BLK/WHT
RED/WHT
AU1043
BLUE
WL0046
3"L.
JT0003
BLUE
WL0046
6"L.
JT0003
1/4" STRIP
E5 RED
E13 BLK
E12 BLK
E15 ORN
P10
AX1043
E6 RED
E20 BLK
E19 BLK
E16 ORN
P11
AX1043
E7 RED
E22 BLK
E21 BLK
E17 ORN
P12
AX1043
E24 BLU
E18 RED
P13
AR1043
E1 RED
E2 RED
E14 ORN
E3 RED
E4 RED
E8 BLK
E9 BLK
E10 BLK
E11 BLK
E25 WHT/RED
E23 WHT
E34 RED
P8
AW1043
REVISIONS
FOR ALL REVISIONS SEE SHT 1
PARTS LIST
WIRE HARNESS
FOR
AA1043 TANDY
AA1043
B
SHEET 2 OF 2
AT1043
TANDY
DO NOT SCALE DRAWING

Keyboard

FUJITSU KEYBOARD
ASSEMBLY # N860-4703-T

## 1.0 GENERAL

The keyboard is a direct, plug-compatible replacement for the Enhanced Keyboard for the IBM PC, XT, and AT personal computer. No software modification or special interface is needed by the user.

## 2.0 SCOPE

This specification describes the functional, mechanical, electrical, environmental, and reliability characteristics of the FUJITSU N860-4703-T Keyboard assembly.

The keyboard is encoded in such a way as to produce a unique output code for each key that is pressed and/or released. The communication with the host computer is a synchronous serial link. The Key Layout, Switch Encoding and Serial Communication are all compatible with the IBM PC, XT and AT.

## 3.0 MECHANICAL SPECIFICATION

### 3.1 Key Layout, Legends, and Colors

Figure 1 shows keytop layout, appropriate legends and keytop colors. The keys are numbered from left to right starting with the spacebar row (Row A) and ending with the function key row (Row F).

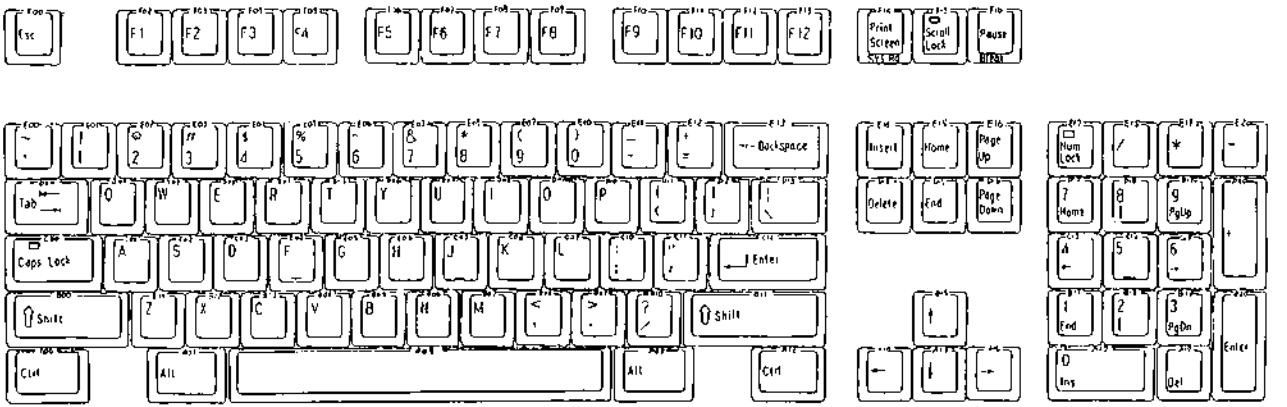

Esc
F1
F2
F3
F4
F5
F6
F7
F8
F9
F10
F11
F12
Print Screen
Scroll Lock
Pause
Backspace
Tab
Caps Lock
Enter
Shift
Shift
Ctrl
Alt
Alt
Ctrl
Insert
Home
Page Up
Delete
End
Page Down
Num Lock
Home
PgUp
End
PgDn
Ins
Del
Enter

FIGURE 1

## 3.2 KEYSWITCH

3.2.1 Total Travel: 0.150", +/- 0.020" (3.8, +/-0.5mm)

3.2.2 FORCE: All keyswitches shall utilize a 2.0 ounce (+/- 0.9 oz) operating force. This is accomplished using both a rubber keyswitch membrane and springs.

3.2.3 BREAKOVER FEEDBACK: The keyswitches utilize a tactile feedback to assure the operator that the key has been fully pressed.

# 4.0 FUNCTIONAL REQUIREMENTS

## 4.1 SCAN CODES

The keyboard generates a unique Hex scan code for each keyswitch that is pressed (make code) and released (break code). For the AT Mode, the break code is the same as the make code preceded by "F0" Hex. Example: The make code for the "ESC" key is 76 Hex and the break code is two bytes, F0 76 Hex. For the XT Mode, the break code is 80 Hex, plus the make code. Example: The make code for the "ESC" key is 01 Hex and the break code is 81 Hex. The keyswitch-to-scan-code (make and break codes) assignments, Standard ASCII Codes, and Extended ASCII Codes are listed on the following pages.

# KEYBOARD SCAN CODES

| Key # | Key Descript. | AT Mode Make Code | AT Mode Break Code | XT Mode Make Code | XT Mode Break Code | Standard ASCII (Scancode/ASCII code) Norm | Shift | Ctrl | Alt | Extended ASCII (Scancode/ASCII code) Norm | Shift | Ctrl | Alt |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Esc | 76 | F076 | 01 | 81 | 011B | 011B | 011B | ----- | 011B | 011B | 011B | 0100 |
| 2 | F1 | 05 | F005 | 3B | BB | 3B00 | 5400 | 5E00 | 6800 | 3B00 | 5400 | 5E00 | 6800 |
| 3 | F2 | 06 | F006 | 3C | BC | 3C00 | 5500 | 5F00 | 6900 | 3C00 | 5500 | 5F00 | 6900 |
| 4 | F3 | 04 | F004 | 3D | BD | 3D00 | 5600 | 6000 | 6A00 | 3D00 | 5600 | 6000 | 6A00 |
| 5 | F4 | 0C | F00C | 3E | BE | 3E00 | 5700 | 6100 | 6B00 | 3E00 | 5700 | 6100 | 6B00 |
| 6 | F5 | 03 | F003 | 3F | BF | 3F00 | 5800 | 6200 | 6C00 | 3F00 | 5800 | 6200 | 6C00 |
| 7 | F6 | 0B | F00B | 40 | C0 | 4000 | 5900 | 6300 | 6D00 | 4000 | 5900 | 6300 | 6D00 |
| 8 | F7 | 83 | F083 | 41 | C1 | 4100 | 5A00 | 6400 | 6E00 | 4100 | 5A00 | 6400 | 6E00 |
| 9 | F8 | 0A | F00A | 42 | C2 | 4200 | 5B00 | 6500 | 6F00 | 4200 | 5B00 | 6500 | 6F00 |
| 10 | F9 | 01 | F001 | 43 | C3 | 4300 | 5C00 | 6600 | 7000 | 4300 | 5C00 | 6600 | 7000 |
| 11 | F10 | 09 | F009 | 44 | C4 | 4400 | 5D00 | 6700 | 7100 | 4400 | 5D00 | 6700 | 7100 |
| 12 | F11 | 78 | F078 | 57 | D7 | ----- | ----- | ----- | ----- | 8500 | 8700 | 8900 | 8B00 |
| 13 | F12 | 07 | F007 | 58 | D8 | ----- | ----- | ----- | ----- | 8600 | 8800 | 8A00 | 8C00 |
| 14 | Print Scrn | E07C | E0F07C | E02AE037 | E0B7E0AA | Note[1] | Note[1] | 7200 | ----- | Note[1] | Note[1] | 7200 | ----- |
| 15 | Scroll Lock | 7E | F07E | 46 | C6 | Note[2] | Note[2] | ------ | Note[2] | Note[2] | Note[2] | ----- | Note[2] |
| 16 | Pause Break | E11477 | E1F014F077 | E11D45 | E19DC5 | Note[3] | Note[3] | Note[4] | Note[3] | Note[3] | Note[3] | Note[4] | Note[3] |
| 17 | ~ or \ | 0E | F00E | 29 | A9 | 2960 | 297E | ----- | ----- | 6000 | 7E00 | ----- | 2900 |
| 18 | ! or 1 | 16 | F016 | 02 | 82 | 0231 | 0221 | ----- | 7800 | 0231 | 0221 | ----- | 7800 |

TABLE 1

# KEYBOARD SCAN CODES

| Key # | Key Descript. | AT Mode Make Code | AT Mode Break Code | XT Mode Make Code | XT Mode Break Code | Standard ASCII (Scancode/ASCII code) Norm | Standard ASCII Shift | Standard ASCII Ctrl | Standard ASCII Alt | Extended ASCII (Scancode/ASCII code) Norm | Extended ASCII Shift | Extended ASCII Ctrl | Extended ASCII Alt |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 19 | @ or 2 | 1E | F01E | 03 | 83 | 0332 | 0340 | 0300 | 7900 | 0332 | 0340 | 0300 | 7900 |
| 20 | # or 3 | 26 | F026 | 04 | 84 | 0433 | 0423 | ----- | 7A00 | 0433 | 0423 | ----- | 7A00 |
| 21 | $ or 4 | 25 | F025 | 05 | 85 | 0534 | 0524 | ----- | 7B00 | 0534 | 0524 | ----- | 7B00 |
| 22 | % or 5 | 2E | F02E | 06 | 86 | 0635 | 0625 | ----- | 7C00 | 0635 | 0625 | ----- | 7C00 |
| 23 | ^ or 6 | 36 | F036 | 07 | 87 | 0736 | 075E | 071E | 7D00 | 0736 | 075E | 071E | 7D00 |
| 24 | & or 7 | 3D | F03D | 08 | 88 | 0837 | 0826 | ----- | 7E00 | 0837 | 0826 | ----- | 7E00 |
| 25 | * or 8 | 3E | F03E | 09 | 89 | 0938 | 092A | ----- | 7F00 | 0938 | 092A | ----- | 7F00 |
| 26 | ( or 9 | 46 | F046 | 0A | 8A | 0A39 | 0A28 | ----- | 8000 | 0A39 | 0A28 | ----- | 8000 |
| 27 | ) or 0 | 45 | F045 | 0B | 8B | 0B34 | 0B29 | ----- | 8100 | 0B34 | 0B29 | ----- | 8100 |
| 28 | _ or - | 4E | F04E | 0C | 8C | 0C2D | 0C5F | 0C1F | 8200 | 0C2D | 0C5F | 0C1F | 8200 |
| 29 | + or = | 55 | F055 | 0D | 8D | 0D3D | 0D2B | ----- | 8300 | 0D3D | 0D2B | ----- | 8300 |
| 30 | Backspace | 66 | F066 | 0E | 8E | 0E08 | 0E08 | 0E7F | ----- | 0E08 | 0E08 | 0E7F | 0E00 |
| 31 | Insert | E070 | E0F070 | E02AE052 | E0D2E0AA | 5200 | 5200 | ----- | ----- | 52E0 | 52E0 | 92E0 | A200 |
| 32 | Home | E06C | E0F06C | E02AE047 | E0C7E0AA | 4700 | 4700 | 7700 | ----- | 47E0 | 47E0 | 77E0 | 9700 |
| 33 | Pg Up | E07D | E0F07D | E02AE049 | E0C9E0AA | 4900 | 4900 | 8400 | ----- | 49E0 | 49E0 | 84E0 | 9900 |
| 34 | Num Lock | 77 | F077 | 45 | C5 | Note[5] | Note[5] | ----- | Note[5] | Note[5] | Note[5] | ---- | Note[5] |
| 35 | / | E04A | E0F04A | E035 | E0B5 | 352F | 352F | ----- | ----- | E02F | E02F | 9500 | A400 |
| 36 | * | 7C | F07C | 37 | B7 | 372A | 372A | ----- | ----- | 372A | 372A | 9600 | 3700 |
| 37 | - | 7B | F07B | 4A | CA | 4A2D | 4A2D | ----- | ----- | 4A2D | 4A2D | 8E00 | 4A00 |

# KEYBOARD SCAN CODES

| Key # | Key Descript. | AT Mode Make Code | AT Mode Break Code | XT Mode Make Code | XT Mode Break Code | Standard ASCII (Scancode/ASCII code) Norm | Shift | Ctrl | Alt | Extended ASCII (Scancode/ASCII code) Norm | Shift | Ctrl | Alt |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 38 | Tab | 0D | F00D | 0F | 8F | 0F90 | 0F00 | ----- | ----- | 0F09 | 0F00 | 9400 | A500 |
| 39 | Q or q | 15 | F015 | 10 | 90 | 1071 | 1051 | 1011 | 1000 | 1071 | 1051 | 1011 | 1000 |
| 40 | W or w | 1D | F01D | 11 | 91 | 1177 | 1157 | 1117 | 1100 | 1177 | 1157 | 1117 | 1100 |
| 41 | E or e | 24 | F024 | 12 | 92 | 1265 | 1245 | 1205 | 1200 | 1265 | 1245 | 1205 | 1200 |
| 42 | R or r | 2D | F02D | 13 | 93 | 1372 | 1352 | 1312 | 1300 | 1372 | 1352 | 1312 | 1300 |
| 43 | T or t | 2C | F02C | 14 | 94 | 1474 | 1454 | 1414 | 1400 | 1474 | 1454 | 1414 | 1400 |
| 44 | Y or y | 35 | F035 | 15 | 95 | 1579 | 1559 | 1519 | 1500 | 1579 | 1559 | 1519 | 1500 |
| 45 | U or u | 3C | F03C | 16 | 96 | 1675 | 1655 | 1615 | 1600 | 1675 | 1655 | 1615 | 1600 |
| 46 | I or i | 43 | F043 | 17 | 97 | 1769 | 1749 | 1709 | 1700 | 1769 | 1749 | 1709 | 1700 |
| 47 | O or o | 44 | F044 | 18 | 98 | 186F | 184F | 180F | 1800 | 186F | 184F | 180F | 1800 |
| 48 | P or p | 4D | F04D | 19 | 99 | 1970 | 1950 | 1910 | 1900 | 1970 | 1950 | 1910 | 1900 |
| 49 | { or [ | 54 | D054 | 1A | 9A | 1A5B | 1A7B | 1A1B | ----- | 1A5B | 1A7B | 1A1B | 1A00 |
| 50 | } or ] | 5B | F05B | 1B | 9B | 1B5D | 1B7D | 1B1D | ----- | 1B5D | 1B7D | 1B1D | 1B00 |
| 51 | \| or \ | 5D | F05D | 2B | AB | 2B5C | 2B7C | 2B1C | ----- | 2B5C | 2B7C | 2B1C | 2B00 |
| 52 | Delete | E071 | E0F071 | E02AE053 | E0D3E0AA | 5300 | 5300 | ----- | ----- | 53E0 | 53E0 | 93E0 | A300 |
| 53 | End | E069 | E0F069 | E02AE04F | E0CFE0AA | 4F00 | 4F00 | 7500 | ----- | 4FE0 | 4FE0 | 75E0 | 9F00 |
| 54 | Page Down | E07A | E0F07A | E02AE051 | E0D1E0AA | 5100 | 5100 | 7600 | ----- | 51E0 | 51E0 | 76E0 | A100 |
| 55 | 7 or Home | 6C | F06C | 47 | C7 | 4700 | 4737 | 7700 | Note[6] | 4700 | 4737 | 7700 | Note[6] |
| 56 | 8 | 75 | F075 | 48 | C8 | 4800 | 4838 | ---- | Note[6] | 4800 | 4838 | 8D00 | Note[6] |
| 57 | 9 or Page Up | 7D | F07D | 49 | C9 | 4900 | 4939 | 8400 | Note[6] | 4900 | 4939 | 8400 | Note[6] |

# KEYBOARD SCAN CODES

| Key # | Key Descript. | AT Mode Make Code | AT Mode Break Code | XT Mode Make Code | XT Mode Break Code | Standard ASCII (Scancode/ASCII code) Norm | Shift | Ctrl | Alt | Extended ASCII (Scancode/ASCII code) Norm | Shift | Ctrl | Alt |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 58 | + | 79 | F079 | 4E | CE | 4E2B | 4E2B | ---- | ---- | 4E2B | 4E2B | 9000 | 4E00 |
| 59 | Caps Lock | 58 | F058 | 3A | BA | Note[7] | Note[7] | ---- | Note[7] | Note[7] | Note[7] | ---- | Note[7] |
| 60 | A or a | 1C | F01C | 1E | 9E | 1E61 | 1E41 | 1E01 | 1E00 | 1E61 | 1E41 | 1E01 | 1E00 |
| 61 | S or s | 1B | F01B | 1F | 9F | 1F73 | 1F53 | 1F13 | 1F00 | 1F73 | 1F53 | 1F13 | 1F00 |
| 62 | D or d | 23 | F023 | 20 | A0 | 2064 | 2044 | 2004 | 2000 | 2064 | 2044 | 2004 | 2000 |
| 63 | F or f | 2B | F02B | 21 | A1 | 2166 | 2146 | 2106 | 2100 | 2166 | 2146 | 2106 | 2100 |
| 64 | G or g | 34 | F034 | 22 | A2 | 2267 | 2247 | 2207 | 2200 | 2267 | 2247 | 2207 | 2200 |
| 65 | H or h | 33 | F033 | 23 | A3 | 2368 | 2348 | 2308 | 2300 | 2368 | 2348 | 2308 | 2300 |
| 66 | J or j | 3B | F03B | 24 | A4 | 246A | 244A | 240A | 2400 | 246A | 244A | 240A | 2400 |
| 67 | K or k | 42 | F042 | 25 | A5 | 256B | 254B | 250B | 2500 | 256B | 254B | 250B | 2500 |
| 68 | L or l | 4B | F04B | 26 | A6 | 266C | 264C | 260C | 2600 | 266C | 264C | 260C | 2600 |
| 69 | : or ; | 4C | F04C | 27 | A7 | 273B | 273A | ---- | ---- | 273B | 273A | ---- | 2700 |
| 70 | " or ' | 52 | F052 | 28 | A8 | 2827 | 2822 | ---- | ---- | 2827 | 2822 | ---- | 2800 |
| 71 | Enter | 5A | F05A | 1C | 9C | 1C0D | 1C0D | 1C0A | ---- | 1C0D | 1C0D | 1C0A | 1C00 |
| 72 | 4 | 6B | F06B | 4B | CB | 4B00 | 4B34 | 7300 | Note[6] | 4B00 | 4B34 | 7300 | Note[6] |
| 73 | 5 | 73 | F073 | 4C | CC | ----- | 4C35 | --- | Note[6] | 4C00 | 4C35 | 8F00 | Note[6] |
| 74 | 6 | 74 | F074 | 4D | CD | 4D00 | 4D36 | 7400 | Note[6] | 4D00 | 4D36 | 7400 | Note[6] |

# KEYBOARD SCAN CODES

| Key # | Key Descript. | AT Mode Make Code | AT Mode Break Code | XT Mode Make Code | XT Mode Break Code | Standard ASCII (Scancode/ASCII code) Norm | Standard ASCII Shift | Standard ASCII Ctrl | Standard ASCII Alt | Extended ASCII (Scancode/ASCII code) Norm | Extended ASCII Shift | Extended ASCII Ctrl | Extended ASCII Alt |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 76 | Left Shift | 12 | F012 | 2A | AA | Note[8] | Note[8] | Note[8] | Note[8] | Note[8] | Note[8] | Note[8] | Note[8] |
| 77 | Z or z | 1A | F01A | 2C | AC | 2C7A | 2C5A | 2C1A | 2C00 | 2C7A | 2C5A | 2C1A | 2C00 |
| 78 | X or x | 22 | F022 | 2D | AD | 2D78 | 2D58 | 2D18 | 2000 | 2D78 | 2D58 | 2D18 | 2000 |
| 79 | C or c | 21 | F021 | 2E | AE | 2E63 | 2E43 | 2E03 | 2E00 | 2E63 | 2E43 | 2E03 | 2E00 |
| 80 | V or v | 2A | F02A | 2F | AF | 2F76 | 2F56 | 2F16 | 2F00 | 2F76 | 2F56 | 2F16 | 2F00 |
| 81 | B or b | 32 | F032 | 30 | B0 | 3062 | 3042 | 3002 | 3000 | 3062 | 3042 | 3002 | 3000 |
| 82 | N or n | 31 | F031 | 31 | B1 | 316E | 314E | 310E | 3100 | 316E | 314E | 310E | 3100 |
| 83 | M or m | 3A | F03A | 32 | B2 | 326D | 324D | 320D | 3200 | 326D | 324D | 320D | 3200 |
| 84 | < or , | 41 | F041 | 33 | B3 | 332C | 333C | ----- | ----- | 332C | 333C | ----- | 3300 |
| 85 | > or . | 49 | F049 | 34 | B4 | 342E | 343E | ----- | ----- | 342E | 343E | ----- | 3400 |
| 86 | ? or / | 4A | F04A | 35 | B5 | 352F | 353F | ----- | ----- | 352F | 353F | ----- | 3500 |
| 87 | Right Shift | 59 | F059 | 36 | B6 | Note[8] | Note[8] | Note[8] | Note[8] | Note[8] | Note[8] | Note[8] | Note[8] |
| 88 | Up Arrow | E075 | E0F075 | E02AE048 | E0C8E0AA | 4800 | 4800 | ----- | ---- | 48E0 | 48E0 | 8DE0 | 9800 |
| 89 | 1 or End | 69 | F069 | 4F | CF | 4F00 | 4F31 | 7500 | Note[6] | 4F00 | 4F31 | 7500 | Note[6] |
| 90 | 2 | 72 | F072 | 50 | D0 | 5000 | 5032 | ---- | Note[6] | 5000 | 5032 | 9100 | Note[6] |
| 91 | 3 or Pg Dn | 7A | F07A | 51 | D1 | 5100 | 5133 | 7600 | Note[6] | 5100 | 5133 | 7600 | Note[6] |
| 92 | Left Ctrl | 14 | F014 | 1D | 9D | Note[9] | Note[9] | Note[9] | Note[9] | Note[9] | Note[9] | Note[9] | Note[9] |
| 93 | Left Alt | 11 | F011 | 38 | B8 | Note[10] | Note[10] | Note[10] | Note[10] | Note[10] | Note[10] | Note[10] | Note[10] |
| 94 | Space | 29 | F029 | 39 | B9 | 3920 | 3920 | 3920 | 3920 | 3920 | 3920 | 3920 | 3920 |

# KEYBOARD SCAN CODES

| Key # | Key Descript. | AT Mode Make Code | AT Mode Break Code | XT Mode Make Code | XT Mode Break Code | Standard ASCII (Scancode/ASCII code) Norm | Standard ASCII Shift | Standard ASCII Ctrl | Standard ASCII Alt | Extended ASCII (Scancode/ASCII code) Norm | Extended ASCII Shift | Extended ASCII Ctrl | Extended ASCII Alt |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 95 | Right Alt | E011 | E0F011 | E038 | E0B8 | Note[10] | Note[10] | Note[10] | Note[10] | Note[10] | Note[10] | Note[10] | Note[10] |
| 96 | Right Ctrl | E014 | E0F014 | E01D | E09D | Note | Note | Note | Note | Note | Note | Note | Note |
| 97 | Left Arrow | E06B | E0F06B | E02AE04B | E0CBE0AA | 4B00 | 4B00 | 7300 | ---- | 4BE0 | 4BE0 | 73E0 | 9B00 |
| 98 | Down Arrow | E072 | E0F072 | E02AE050 | E0D0E0AA | 5000 | 5000 | ---- | ---- | 50E0 | 50E0 | 91E0 | A000 |
| 99 | Right Arrow | E074 | E0F074 | E024E04D | E0CDE0AA | 4D00 | 4000 | 7400 | ---- | 4DE0 | 4DE0 | 74E0 | 9D00 |
| 100 | 0 or Ins | 70 | F070 | 52 | D2 | 5200 | 5230 | ---- | Note[6] | 5200 | 52311 | 9200 | Note[6] |
| 101 | . or Del | 71 | F071 | 53 | D3 | 5300 | 532E | ---- | ---- | 5300 | 532E | 9300 | ---- |
| 102 | Enter | E05A | E0F05A | E01C | E09C | 1C0D | 1C0D | 1C0A | ---- | E00D | E00D | E00A | A600 |

## NOTES

Note1 —INT 05H is invoked and a screen dump is performed
Note2 —the scroll lock active bit is toggled
Note3 —the pause state is initiated
Note4 —INT 1BH is invoked
Note5 —the numlock active bit is toggled
Note6 —ALT num pad generates raw ascii code of typed number
Note7 —the caps lock active bit is toggled
Note8 —hold shift lock active until key is released
Note9 —hold control shift active until key is released
Note10—hold alternate shift active until key is released

## 5.0 PROTOCOL

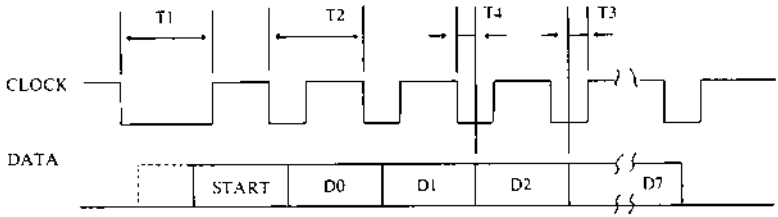
### 5.0.1 COMMUNICATION MODE 1 (PC/XT Mode)

The keyboard communicates with the host computer using a synchronous serial protocol at approximately 9600BPS. One start bit, eight data bits, no stop bit, and no parity are used to make up the nine bit data word. When no communications are in progress, the keyboard holds the data line low and the clock line high.

Before starting a transmission, the keyboard lowers the clock line as a Request To Send (RTS). The state of the data line is then checked. If the host system is holding the data line low, transmissions are disabled. The keyboard will retain the keycode for the pressed key in its buffer until the clock and data lines return to the idle state. The keyboard then resumes scanning the keyboard matrix until transmissions are enabled.

When transmissions are enabled, 100 to 250 microseconds after the keyboard drives the clock line low, the keyboard transmits its data in the previously described format. Data is valid during the time the clock line is high and for a minimum of 10 microseconds after the falling edge of the clock line. See Figure 2 for a timing diagram.

< KEYBOARD DATA OUTPUT-XT MODE >



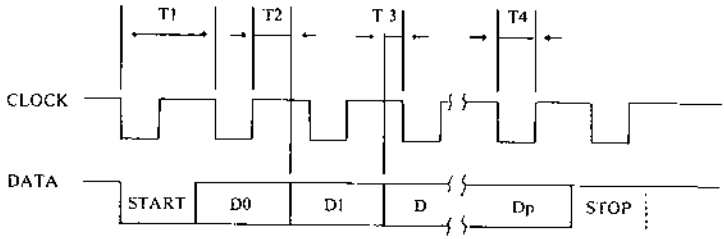

T1 ; 100 – 250μs (CHECKING TIME OF DATA OUTPUT READY OR PROHIBITION)
T2 ; 104μs ± 20%
T3 ; 10μs MIN.
T4 ; 10μs MIN.

FIGURE 2

5.0.2 COMMUNICATION MODE 2 (AT MODE)

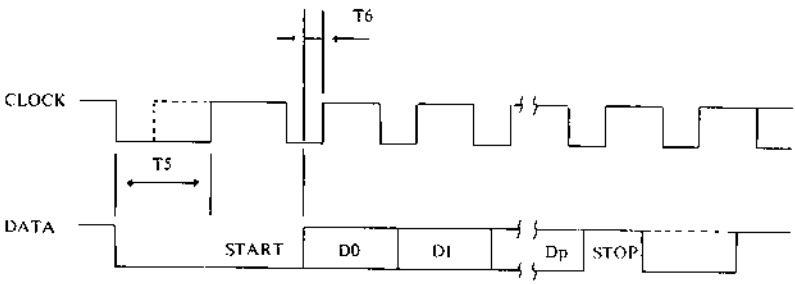
The keyboard communicates with the host computer using a synchronous serial protocol at approximately 9600BPS. One start bit, eight data bits, odd parity, and one stop bit form the eleven bit data word. This communication is bi-directional, with the keyboard clocking all data transfers. When no communications are in progress, the data and clock lines are high, indicating an idle state.

< KEYBOARD DATA OUTPUT-AT MODE > Figure 3A




T1 ; 104μs ±20%
T2 ; 20μs MIN.
T3 ; 20μs MIN.
T4 ; 35μs ±20%

< KEYBOARD DATA INPUT-AT MODE > Figure 3B




T5 ; 60μs MIN. (WAITING TIME FOR HOST DATA OUTPUT)
T6 ; 5μs MIN.

FIGURE 3

Before starting a transmission, the keyboard checks the status of the clock and data lines. Transmissions are disabled if the clock line is low and the code for the pressed key is held in the keyboard buffer until transmissions are enabled. If the clock line is high and the data line is low, the host system is sending a Request To Send (RTS), and the code for the pressed key is stored in the buffer.

When transmissions are enabled and no RTS is detected from the host system, both clock and data line will be high. The keyboard starts a transmission by sending a low start bit, followed by the rest of the data word. Data is valid 20 microseconds minimum prior to the falling edge of the clock. See Figure 3 for timing diagram.

During the transmission of a data word, the keyboard periodically checks the state of the clock line. If the clock line is low during these checks prior to the rising edge of the parity bit, a data collision occurs. When a data collision occurs, the keyboard stops transmitting, returns the code for the pressed key to the keyboard buffer, and prepares to respond to actions requested by the host system.

## 5.1 COMMANDS FROM THE KEYBOARD TO THE HOST SYSTEM

### Keyboard Buffer Overrun — AT and XT Modes

This buffer can store up to sixteen codes for pressed keys. When this buffer is full and the seventeenth code is received, this code is replaced by an Overrun Code. The following chart shows the Overrun Codes for each mode.

| | |
|---|---|
| XT Mode | FF Hex |
| AT Mode | 00 Hex |

Codes received after this code are lost until the keyboard clears additional space in the keyboard buffer.

Self Test Passed -- AA Hex AT and XT Modes

The keyboard issues this command upon successful completion of the keyboard self test. The self test consists of the following.

XT MODE

1. Memory is cleared.
2. Keyboard buffer is cleared.
3. ROM checksum is read and compared.
4. RAM is tested.
5. Self test completion code is output.
6. AA Hex is output to indicate successful self test.
7. FC Hex is output to indicate a defect in the self test.

AT MODE

1. ROM checksum is read and compared.
2. RAM is tested.
3. AA Hex is output to indicate successful self test.
4. FC Hex is output to indicate a defect in the self test.

This self test is initiated by the host system reset (Ctrl, Alt, Delete) or by Power-on Reset. Upon successful completion of the Self Test during Power-on Reset, the keyboard is set to XT mode if the keyboard detects a low level on the data line for more than 10 microseconds after 5 microseconds from the falling edge of the clock line. If this condition is not met, the keyboard is placed in the AT Mode, and Typematic Rate and Delay are set to the following defaults:

Typematic Rate 10.9 cps
Delay 500 milliseconds

ECHO -- EE Hex AT and XT Modes

The Echo Command (EE Hex) is sent in response to an Echo Command from the host system instead of the normal Acknowledge (ACK) for diagnostic purposes.

Acknowledge -- FA Hex AT Mode

The keyboard sends an Acknowledge (FA Hex) in response to a valid command from the host system, with the exceptions of the Resend and Echo commands.

Resend -- FE Hex  AT and XT Modes

The keyboard issues a Resend (FE Hex) in response to inputs which have parity errors, framing errors, or invalid data received from the host system.

KEYBOARD BUFFER OVERRUN — AT and XT Modes

When the 16-character keyboard buffer receives the 17th character, an overflow condition occurs. This condition is communicated to the host system by transmitting the Keyboard buffer Overrun (FF Hex for XT Mode, 00 Hex for AT Mode) to the host system.

## 5.2 COMMANDS FROM THE HOST SYSTEM TO THE KEYBOARD

Prior to sending commands to the keyboard, the host system must first check to see if the keyboard is sending data. If the keyboard is transmitting, and the data is past the parity bit, the host system must accept the data prior to initiating its own transmission.

If the keyboard's data has not yet reached the tenth clock pulse (Parity Bit), or is not transmitting data, the host system assumes control by lowering the clock line for a minimum of 60 microseconds, then releasing the clock line after clamping the data line low to indicate a start bit. The keyboard will respond with an RTS within 5 microseconds by clocking the start bit into the keyboard. The keyboard continues to clock data as shown in the timing diagram (Figure 3B). The host system must ensure that the data is valid prior to the rising edge and after the falling edge of the keyboard clock pulse.

After the parity bit, the host system should raise the data line to indicate a stop bit. The keyboard checks for a logical high stop bit, then clamps the data line low prior to clock in the stop bit. This signals the host system that the keyboard received the data correctly (Acknowledge). If the host system has not raised the data line to indicate a stop bit, a framing error results and the keyboard continues to clock data until the data line is raised by the host system. Upon receiving either a framing or parity error, the keyboard issues a RESEND to the host system.

All commands from the host system require a response from the keyboard. The keyboard will respond to these commands within 20 microseconds.

The following commands may be sent to the keyboard at any time, following the protocol described for the AT Mode. These commands are valid only in the AT Mode. During the reset command, the keyboard will not respond within 20 microseconds as described above.

RESET — FF Hex

Upon receiving this command, the keyboard transmits an Acknowledge to the host system. The keyboard then waits for the host system to accept the Acknowledge response. The host system will accept the Acknowledge by raising the clock and data lines for a minimum of 500 microseconds.

The keyboard then executes the self test routine similar to the Power-On Reset, and is placed in its default state.

RESEND — FE Hex

Upon receiving this command, the keyboard will transmit the last byte of data sent to the host system.

SET DEFAULT — F6 Hex

This command resets the keyboard to the Power-Up default state. The keyboard responds with an Acknowledge, clears the output buffer, sets the scanset to AT Mode, sets the default typematic rate and delay, and continues to scan the matrix.

DEFAULT DISABLE — F5 Hex

This command is similar to the Set Default command, except the keyboard stops scanning the matrix and waits for further instructions to be sent by the host system.

ENABLE -- F4 Hex

Upon receipt of this command the keyboard responds with an Acknowledge, clears the output buffer, and starts scanning the matrix.

SET TYPEMATIC RATE/DELAY — F3 Hex

This command consists of one command byte and one parameter byte. The keyboard Acknowledges the command byte, stops scanning the matrix, and waits for the parameter byte. Upon receiving the parameter byte, the keyboard sends an Acknowledge, sets the typematic rate and delay as indicated in Table 2, and continues scanning the matrix.

If another command is received instead of the parameter byte, the set typematic rate/delay function ends with no change to the existing rate or delay parameters. The new command is processed and the keyboard continues scanning the matrix.

The parameter byte consists of an eight-bit word with bit 7 (most significant bit) always being set. Bits 0-4 set the typematic rate and bits 5-6 set the delay.

Example

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | Parameter Byte |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit Number |

The above example shows the default 10.9 cps typematic rate and 500 microsecond delay. Bits 0-4 (010111) correspond to the rate of 10.9 cps shown on Table 2 ii and bits 5-6 (01) correspond to the 500 microsecond delay shown in Table 2 i.

See Table 2 for Typematic Rate/Delay values other than the default settings.

i) Delay

| Bit 6 5 | Delay ms |
|---|---|
| 0 0 | 250 |
| 0 1 | 500 |
| 1 0 | 750 |
| 1 0 | 1000 |

ii) Rate

| Bit 4 | 3 | 2 | 1 | 0 | Rate (CPS) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 30.0 |
| 0 | 0 | 0 | 0 | 1 | 26.7 |
| 0 | 0 | 0 | 1 | 0 | 24.0 |
| 0 | 0 | 0 | 1 | 1 | 21.8 |
| 0 | 0 | 1 | 0 | 0 | 20.0 |
| 0 | 0 | 1 | 0 | 1 | 18.5 |
| 0 | 0 | 1 | 1 | 0 | 17.1 |
| 0 | 0 | 1 | 1 | 1 | 16.0 |
| 0 | 1 | 0 | 0 | 0 | 15.0 |
| 0 | 1 | 0 | 0 | 1 | 13.3 |
| 0 | 1 | 0 | 1 | 0 | 12.0 |
| 0 | 1 | 0 | 1 | 1 | 10.9 |
| 0 | 1 | 1 | 0 | 0 | 10.0 |
| 0 | 1 | 1 | 0 | 1 | 9.2 |
| 0 | 1 | 1 | 1 | 0 | 8.6 |
| 0 | 1 | 1 | 1 | 1 | 8.0 |

| Bit 4 | 3 | 2 | 1 | 0 | Rate (CPS) |
|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 7.5 |
| 1 | 0 | 0 | 0 | 1 | 6.7 |
| 1 | 0 | 0 | 1 | 0 | 6.0 |
| 1 | 0 | 0 | 1 | 1 | 5.5 |
| 1 | 0 | 1 | 0 | 0 | 5.0 |
| 1 | 0 | 1 | 0 | 1 | 4.6 |
| 1 | 0 | 1 | 1 | 0 | 4.3 |
| 1 | 0 | 1 | 1 | 1 | 4.0 |
| 1 | 1 | 0 | 0 | 0 | 3.7 |
| 1 | 1 | 0 | 0 | 1 | 3.3 |
| 1 | 1 | 0 | 1 | 0 | 3.0 |
| 1 | 1 | 0 | 1 | 1 | 2.7 |
| 1 | 1 | 1 | 0 | 0 | 2.5 |
| 1 | 1 | 1 | 0 | 1 | 2.3 |
| 1 | 1 | 1 | 1 | 0 | 2.1 |
| 1 | 1 | 1 | 1 | 1 | 2.0 |

TABLE 2

ECHO — FE Hex

This command is provided for diagnostic purposes. The keyboard shall respond with EE Hex, instead of Acknowledge, and continue scanning the matrix.

SET/RESET STATUS INDICATORS — ED Hex

This command consists of one command byte and one parameter byte. The keyboard Acknowledges the command byte, stops scanning the matrix, and waits for the parameter byte. Upon receiving the parameter byte, the keyboard sends an Acknowledge, sets the status indicators, and starts scanning the matrix.

If another command is received instead of the parameter byte, the keyboard disregards the Set/Reset Status Indicators command without changing the present status of the indicators, processes the new command, and starts scanning the matrix.

The parameter byte is an eight-bit word with bits 3-7 always set to low. Bit 0 is the Scroll Lock Indicator, bit 1 is the Num Lock Indicator, and bit 2 is the Caps Lock Indicator. A high in each individual bit indicates that Indicator is active and the indicator lamp should be on.

Example

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | PARAMETER BYTE |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | BIT NUMBER |

The above example shows the power-on default of the Tandy 3000 NL. Bit 1 is high indicating Num Lock is active and the Num Lock indicator lamp is on.

READ KEYBOARD ID — F2 Hex

This command causes the keyboard to return two identification bytes AB83 Hex. The keyboard responds with an Acknowledge to the command and stops scanning the matrix. The keyboard then transmits the keyboard ID AB83 Hex and resumes scanning the matrix.

SET/READ SCAN SET — F0 Hex

This command is used to select one of three Scan Sets or to tell the host system which Scan Set is currently being used. This command consists of a command byte and a parameter byte. Upon receiving this command, the keyboard sends an Acknowledge to the host system and waits for the parameter byte. When the keyboard receives the parameter byte, it responds with an Acknowledge.

A parameter byte of 00 Hex will cause the keyboard to transmit the Hex value for the Scan Set currently in use. A parameter byte of 01 Hex selects the Scan Set 1 (XT Scan Codes), 02 Hex selects Scan Set 2 (Default AT Scan Codes), and 03 Hex selects Scan Set 3 (Special AT Scan Codes -- See Table 3 for Scan Codes and Default Key State Information). The keyboard resumes scanning the matrix.

TABLE 3

| KEY DESCRIPTION | MAKE CODE | BREAK CODE | DEFAULT KEY STATE |
|---|---|---|---|
| Esc | 08 | F0 08 | Make Only |
| F1 | 07 | F0 07 | Make Only |
| F2 | 0F | F0 0F | Make Only |
| F3 | 17 | F0 17 | Make Only |
| F4 | 1F | F0 1F | Make Only |
| F5 | 27 | F0 27 | Make Only |
| F6 | 2F | F0 2F | Make Only |
| F7 | 37 | F0 37 | Make Only |
| F8 | 3F | F0 3F | Make Only |
| F9 | 47 | F0 47 | Make Only |
| F10 | 4F | F0 4F | Make Only |
| F11 | 56 | F0 56 | Make Only |
| F12 | 5E | F0 5E | Make Only |
| Print Scrn | 57 | F0 57 | Make Only |
| Scroll Lock | 5F | F0 5F | Make Only |
| Pause or Break | 62 | F0 62 | Make Only |
| ` | 0E | F0 0E | Typematic |
| 1 | 16 | F0 16 | Typematic |
| 2 | 1E | F0 1E | Typematic |
| 3 | 26 | F0 26 | Typematic |
| 4 | 25 | F0 25 | Typematic |
| 5 | 2E | F0 2E | Typematic |
| 6 | 36 | F0 36 | Typematic |
| 7 | 3D | F0 3D | Typematic |
| 8 | 3E | F0 3E | Typematic |
| 9 | 46 | F0 46 | Typematic |
| 0 | 45 | F0 45 | Typematic |
| - | 4E | F0 4E | Typematic |
| = | 55 | F0 55 | Typematic |
| Backspace | 66 | F0 66 | Make Only |
| Insert cursor pad | 67 | F0 67 | Make Only |
| Home cursor pad | 6E | F0 6E | Make Only |
| Page Up cursor pad | 6F | F0 6F | Make Only |
| Num Lock | 76 | F0 76 | Make Only |
| / number pad | 77 | F0 77 | Make Only |
| * number pad | 7E | F0 7E | Make Only |
| - number pad | 84 | F0 84 | Make Only |
| Tab | 0D | F0 0D | Typematic |
| q | 15 | F0 15 | Typematic |
| w | 1D | F0 1D | Typematic |
| e | 24 | F0 24 | Typematic |
| r | 2D | F0 2D | Typematic |
| t | 2C | F0 2C | Typematic |
| y | 35 | F0 35 | Typematic |
| u | 3C | F0 3C | Typematic |
| i | 43 | F0 43 | Typematic |
| o | 44 | F0 44 | Typematic |
| p | 4D | F0 4D | Typematic |
| [ | 54 | F0 54 | Typematic |
| ] | 5B | F0 5B | Typematic |

| | | | |
|---|---|---|---|
| | 5C | F0 5C | Typematic |
| Delete cursor pad | 64 | F0 64 | Typematic |
| Home cursor pad | 65 | F0 65 | Make Only |
| Page Up cursor pad | 6D | F0 6D | Make Only |
| 7 number pad | 6C | F0 6C | Make Only |
| 8 number pad | 75 | F0 75 | Make Only |
| 9 number pad | 7D | F0 7D | Make Only |
| + number pad | 7C | F0 7C | Make Only |
| Caps Lock | 14 | F0 14 | Make/Break |
| a | 1C | F0 1C | Typematic |
| s | 1B | F0 1B | Typematic |
| d | 23 | F0 23 | Typematic |
| f | 2B | F0 2B | Typematic |
| g | 34 | F0 34 | Typematic |
| h | 33 | F0 33 | Typematic |
| j | 3B | F0 3B | Typematic |
| k | 42 | F0 42 | Typematic |
| l | 4B | F0 4B | Typematic |
| ; | 4C | F0 4C | Typematic |
| ' | 52 | F0 52 | Typematic |
| Enter | 5A | F0 5A | Typematic |
| 4 number pad | 6B | F0 6B | Make Only |
| 5 number pad | 73 | F0 73 | Make Only |
| 6 number pad | 74 | F0 74 | Make Only |
| Left Shift | 12 | F0 12 | Make/Break |
| z | 1A | F0 1A | Typematic |
| x | 22 | F0 22 | Typematic |
| c | 21 | F0 21 | Typematic |
| v | 2A | F0 2A | Typematic |
| b | 32 | F0 32 | Typematic |
| n | 31 | F0 31 | Typematic |
| m | 3A | F0 3A | Typematic |
| , | 41 | F0 41 | Typematic |
| . | 49 | F0 49 | Typematic |
| Right Shift | 59 | F0 59 | Make/Break |
| Up Arrow cursor pad | 63 | F0 63 | Typematic |
| 1 number pad | 69 | F0 69 | Make Only |
| 2 number pad | 72 | F0 72 | Make Only |
| 3 number pad | 7A | F0 7A | Make Only |
| Enter number pad | 79 | F0 79 | Make Only |
| Left Ctrl | 11 | F0 11 | Make/Break |
| Left Alt | 19 | F0 19 | Make/Break |
| Spacebar | 29 | F0 29 | Typematic |
| Right Alt | 39 | F0 39 | Make Only |
| Right Ctrl | 58 | F0 58 | Make Only |
| Left Arrow cursor | 61 | F0 61 | Typematic |
| Down Arrow | 60 | F0 60 | Typematic |
| Right Arrow | 6A | F0 6A | Typematic |
| Ins number pad | 70 | F0 70 | Make Only |
| Del number pad | 71 | F0 71 | Make Only |

SET ALL KEYS -- TYPEMATIC — F7 Hex

SET ALL KEYS — MAKE/BREAK — F8 Hex

SET ALL KEYS -- MAKE ONLY -- F9 Hex

SET ALL KEYS — TYPEMATIC/MAKE/BREAK — FA Hex

These commands affect Scan Set 3 only, but may be sent using any Scan Set. The keyboard responds with an Acknowledge, clears the output buffer, sets all keys to the function requested by the command, and continues scanning the matrix if it was previously enabled.

SET SINGLE KEY -- TYPEMATIC -- FB Hex

SET SINGLE KEY -- MAKE/BREAK — FC Hex

SET SINGLE KEY -- MAKE ONLY -- FD Hex

These commands consist of a command byte and a parameter byte. The keyboard responds to the command byte with an Acknowledge and waits for the parameter byte. The parameter byte is the scan code from Scan Set 3 for the key to be changed. Upon receiving the parameter byte, the keyboard sets the selected key to the function selected by the command byte, and continues to scan the matrix if it was previously enabled. These commands affect only Scan Set 3 operation, but may be sent using any Scan Set.

## 5.3 KEY ROLLOVER

The keyboard incorporates N-Key Rollover in software to avoid loss of keystroke data during high speed entry. N-Key Rollover is defined as all keys pressed and released will be output in the proper sequence. However, when the keyboard detects more than four keys pressed during a scan of the matrix, the keyboard does not output the keycodes until one or more of the keys are released. If the released key was not properly detected as a pressed key, an error condition occurs and the keyboard issues an buffer overrun code to the host system.

## 5.4 AUTOREPEAT

The power-on default condition will cause the last key pressed to repeat at 10.9 characters-per-second after a 500 millisecond delay. This may be changed by the system when the keyboard is using the AT Communications Mode.

## 5.5 BUFFERING

The keyboard is capable of storing 16 scan codes in a first in/ first out (FIFO) circular buffer. When the buffer overflows, the last code is replaced by a Hex 00, in AT Mode and a Hex FF, in XT Mode.

## 5.6 STATUS INDICATORS

Three LED Status Indicators are provided: Num Lock, Caps Lock, and Scroll Lock.

These indicators are located in the keytop of each respective key. The keyboard will power up with all indicators OFF, except when the host system (such as the Tandy 3000 NL) sets them to ON.

# 6.0 ELECTRICAL REQUIREMENTS

The interface consists of two bi-directional lines, clock and data, which are controlled by 74LS125 equivalent buffers. The keyboard side is terminated by 2200 Ohm resistors. All voltage levels are TTL compatible and the keyboard drivers are capable of sinking 20 mA minimum including the current sourced by the pullup resistors on the keyboard.

## 6.1 CONNECTOR

The connector is a 5-pin DIN connector. Connections are shown in the following table.

Table 4

| PIN # | SIGNAL |
|---|---|
| 1 | CLOCK |
| 2 | DATA |
| 3 | NO CONNECTION |
| 4 | LOGIC GROUND |
| 5 | +5 VOLTS DC |

## 6.2 CHASSIS GROUND

Chassis ground is isolated from logic ground.

## 6.3 POWER REQUIREMENTS

The keyboard requires 5 Volts DC, +/-5%, at 500 milliamps (max).

# 7.0 ENVIRONMENTAL REQUIREMENTS

## 7.1 TEMPERATURE

OPERATING.....0 to 50 degrees C
NON-OPERATING.....-20 to 60 degrees C

## 7.2 RELATIVE HUMIDITY

20% to 90% non-condensing

## 7.3 SHOCK

Operating and non-operating.....10G 11 mS duration

## 7.4 VIBRATION

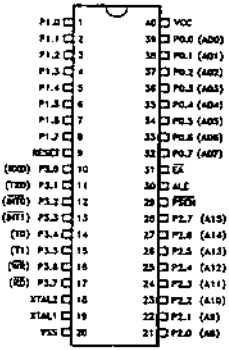
Operating and non-operating.....0.3 mm amplitude 10 to 55 Hz

# 8.0 RELIABILITY

## 8.1 SWITCH LIFE

Switch life of the keyboard is a minimum of 20 million cycles.

## Pin Connections




| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | | | |
| | | | | | | |
| | | | | | | |

## PIN DESCRIPTION

### $V_{SS}$
Circuit ground potential.

### $V_{CC}$
+5V power supply during operation, programming and verification.

### Port 0
Port 0 is an 8-bit open drain bidirectional I/O port.

It is also the multiplexed low-order address and data bus when using external memory. It is used for data input and output during programming and verification. Port 0 can sink/source two TTL loads.

### Port 1
Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during programming and verification. Port 1 can sink/source one TTL load.

### Port 2
Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order 8 bits of address when accessing external memory. It is used for the high-order address and the control signals during programming and verification. Port 2 can sink/source one TTL load.

### Port 3
Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a special function must be programmed to a one (1) for that function to operate. Port 3 can sink/source one TTL load. The special functions are assigned to the pins of Port 3, as follows:

- RXD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous).
- TXD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous).
- $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0.
- $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1.
- T0 (P3.4). Input to counter 0.
- T1 (P3.5). Input to counter 1.
- $\overline{WR}$ (P3.6). The write control signal latches the data byte from Port 0 into the External Data Memory.
- $\overline{RD}$ (P3.7). The read control signal enables External Data Memory to Port 0.

### RST/$V_{PD}$
A low to high transition on this pin (at approximately 3V) resets the 8051. If $V_{PD}$ is held within its spec (approximately +5V), while $V_{CC}$ drops below spec, $V_{PD}$ will provide standby power to the RAM. When $V_{PD}$ is low, the RAM's current is drawn from $V_{CC}$. A small internal resistor permits power-on reset using only a capacitor connected to $V_{CC}$.

### ALE/PROG
Provides Address Latch Enable output used for latching the address into external memory during normal operation. Receives the program pulse input during EPROM programming.

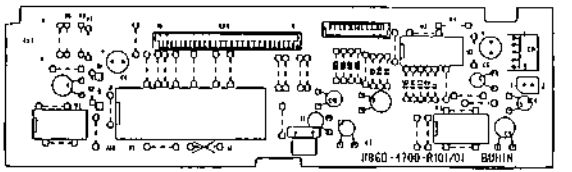
### $\overline{PSEN}$
The Program Store Enable output is a control signal that enables the external Program Memory to the bus during normal fetch operations.

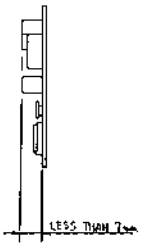
### $\overline{EA}$/$V_{DD}$
When held at a TTL high level, the 8051 executes instructions from the internal ROM/EPROM when the PC is less than 4096. When held at a TTL low level, the 8051 fetches all instuctions from external Program Memory. The pin also receives the 21V EPROM programming supply voltage.

### XTAL1
Input to the oscillator's high gain amplifier. A crystal or external source can be used.

### XTAL2
Output from the oscillator's amplifier. Required when a crystal is used.

| DATE | DOCUMENT CONTROL SECTION |
|---|---|
| | → |



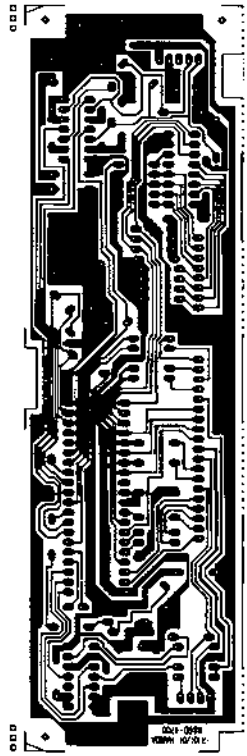




NOTE

1. CAPACITORS AND RESONATOR (X1) TO BE BENT AS ABOVE DRAWING AFTER MOUNTED.
   CAPACITOR (C6) TO BE NOT BENT.
2. CONNECTORS (CN1,CN2,CN3 ) TO BE NOT FLOATED.
3. JUMPER WIRE J2 TO BE NOT MOUNTED.
4. JUMPER WIRE IS 30 POSITIONS (CONTAIN J1)
5. COMPONENTS HEIGHT IS LESS THAN 7mm.

| | | | |
|---|---|---|---|
| FUJITSU LIMITED | PCB ASSEMBLE | J860-4703-P101/01 | 6 |

B13 FOX4-49025




DOCUMENT CONTROL SECTION

DATE

TITLE P.C.B Akiyoshi

PART NO. N86D-4700-Q101/01

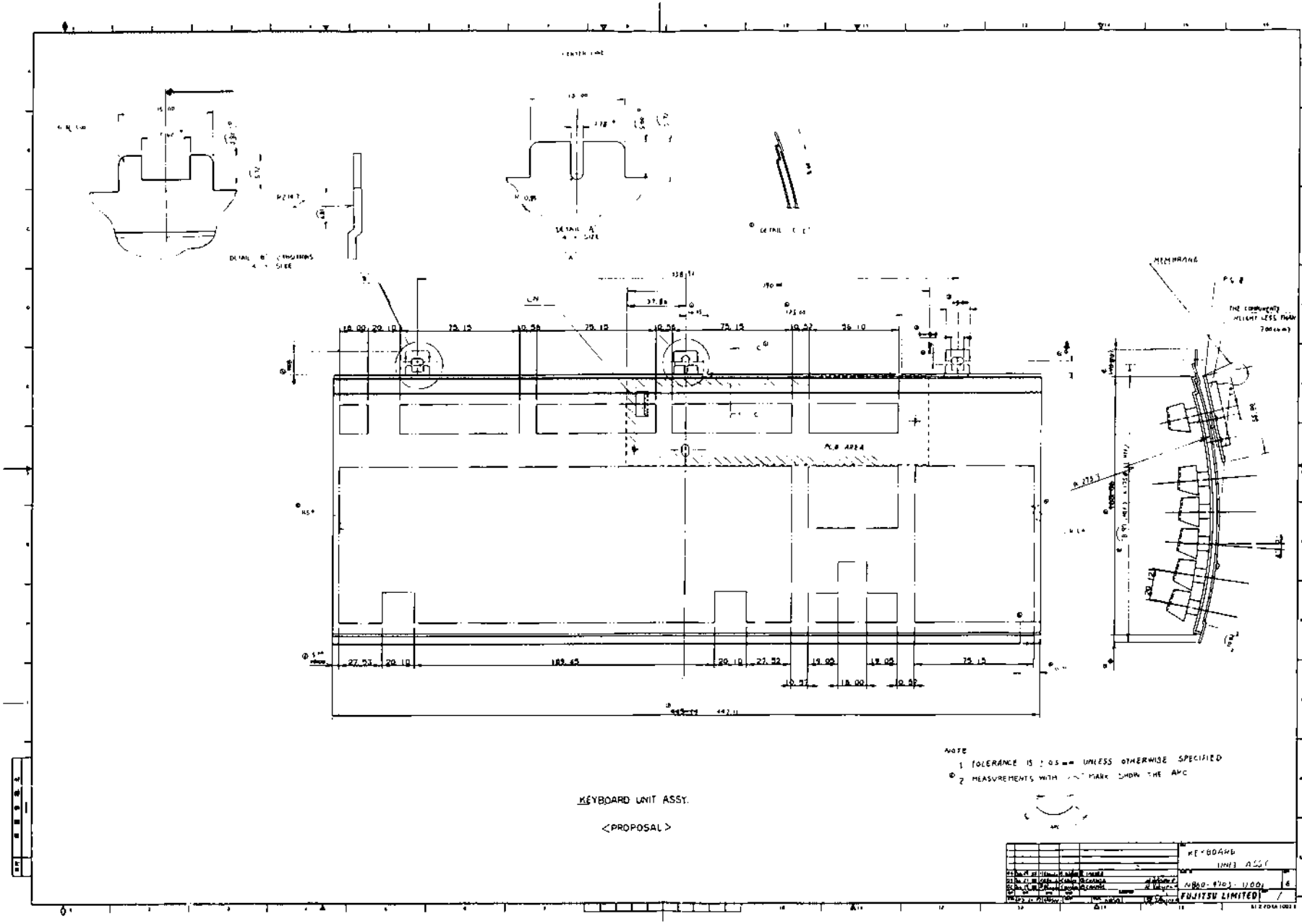
SHEET 6

FUJITSU LIMITED

DRAWN S. Wada

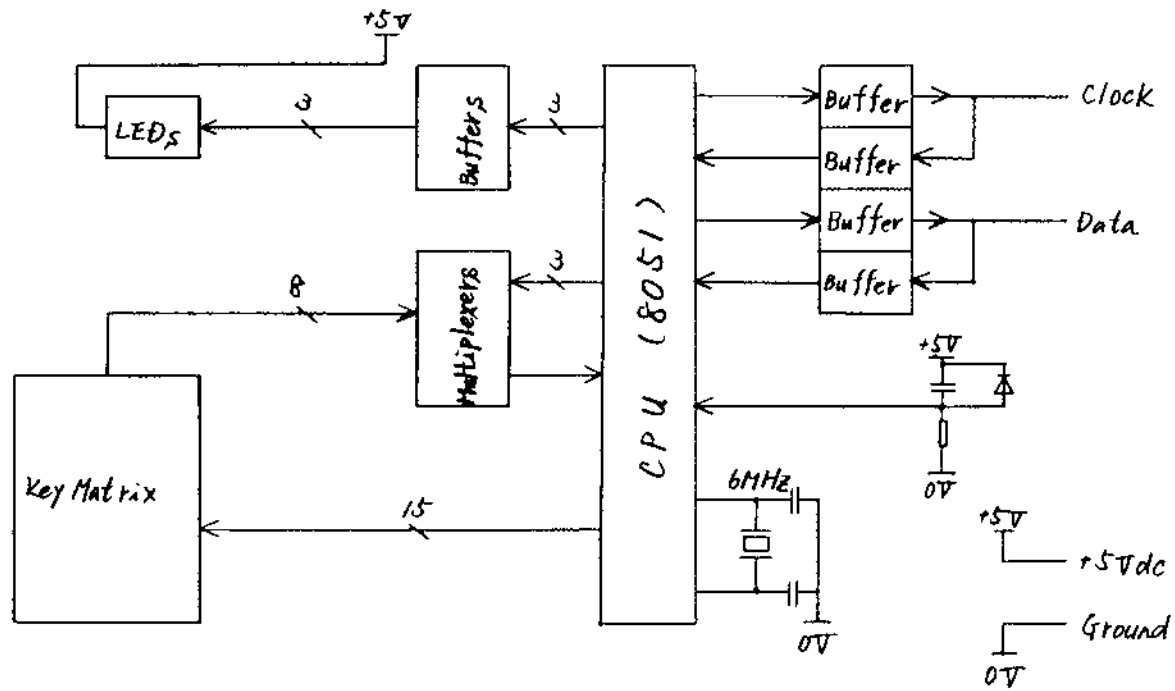
APPR. H. Sakaguchi

61.3 FDXA-4902-5




KEYBOARD UNIT ASSY.

<PROPOSAL>




| 日付 | 原図管理元 |
|---|---|
| | → |

| 項目 | 寸法区分 | 0.5 ~ 30 | ~ 120 | ~ 315 | ~ 1000 | ~ 2000 |
|---|---|---|---|---|---|---|
| 機械・板金加工 | 中心距離（金属） | ±0.1 | ±0.15 | ±0.2 | ±0.3 | ±0.5 |
| | 中心距離（樹脂）<br>一般寸法（金属） | ±0.15 | ±0.25 | ±0.4 | ±0.5 | ±0.7 |
| | 一般寸法（樹脂），組立寸法，曲げ寸法（反手方向315以下） | ±0.2 | ±0.3 | ±0.5 | ±0.8 | ±1.2 |

| 材質 | FN111-10 | FN111-11 | FN111-12 | FN111-13 | FN111-14 |
|---|---|---|---|---|---|
| 材質 | （ ） | 金属地板，アルミニウム合金鋳物（金・砂型），ガラス加工，鋼鉄，鋼合金鋳物，ゴム成形・加工，スポンジ成形・加工 | | プラスチックモールド | ダイカスト |

| 材料 | | 処理 | |
|---|---|---|---|
| 名称 | BLOCK DIAGRAM | 尺度 | : |
| 図番 | 4700 | 提出先 | |
| 富士通株式会社 | | ページ | 1 |

| 版 | 年月日 | 設計 | 調査 | 変更内容 | 設計 | 調査 | 承認 |
|---|---|---|---|---|---|---|---|
| | | | | | 87.04.08 | | |

61.2 FDXA-4006-5

| | | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| X14 | 9 | A00 | | | | | A12 | | |
| X2 | 10 | | | B00 | B11 | | | | |
| X13 | 11 | A01 | C12' | B00' | | | | | |
| X6 | 12 | B01 | B02 | B03 | B04 | B05 | B06 | B07 | B08 |
| X8 | 14 | F00 | F02 | F03 | F04 | F05 | F06 | F07 | F08 |
| X10 | 15 | E00 | E01 | E02 | E03 | E04 | E05 | E06 | E07 |
| X12 | 16 | D00 | D01 | D02 | D03 | D04 | D05 | D06 | D07 |
| X5 | 17 | C01 | C02 | C03 | C04 | C05 | C06 | C07 | C08 |
| X9 | 20 | D10 | F09 | F10 | F11 | F12 | F13 | F15 | F16 |
| X11 | 21 | E08 | E09 | E10 | E11 | E12 | E13 | D08 | D09 |
| X1 | 23 | E15 | E16 | F14 | C00 | A09 | E17 | B20 | E18 |
| X3 | 24 | D11 | D12 | D13 | D17 | D18 | D19 | E19 | E20 |
| X4 | 25 | C09 | C10 | C11 | C12 | C17 | C18 | C19 | D20 |
| X7 | 26 | B09 | B10 | A05 | A17 | A19 | B17 | B18 | B19 |
| X0 | 27 | A14 | A15 | A16 | B15 | D14 | D15 | D16 | E14 |

Vcc ○ 18

L1 ○ 13 Caps

L3 ○ 19 Scroll

L2 ○ 22 Num

原図管理元

日付

| 版 | 年月日 | 設計 | 調査 | 変更内容 |
|---|---|---|---|---|
| 設計 | May.20.88 | Y.Ishida | 調査 | 承認 |

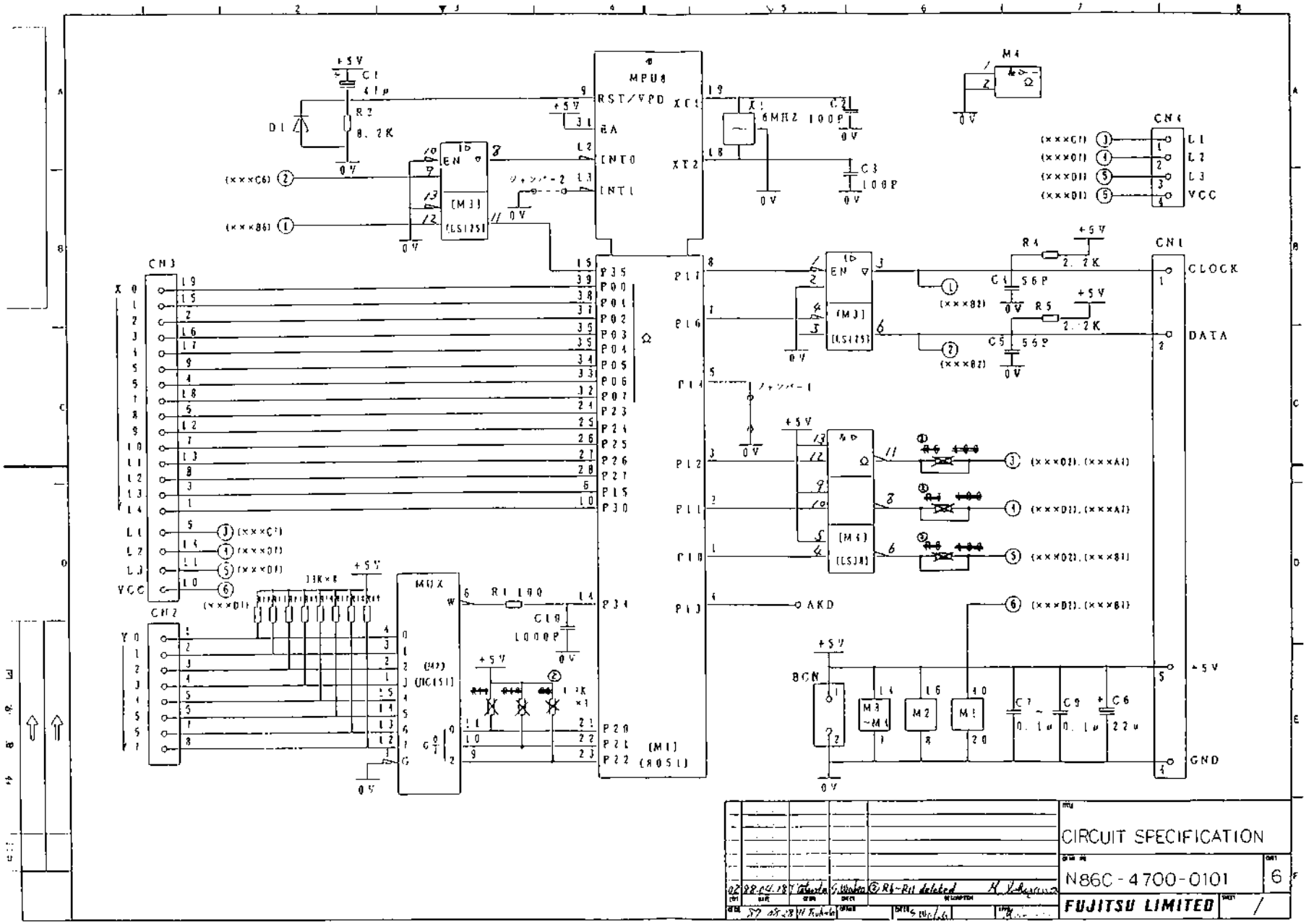
名称 CIRCUIT SPECIFICATION

図番 N86C-4700-0001 提出先 6

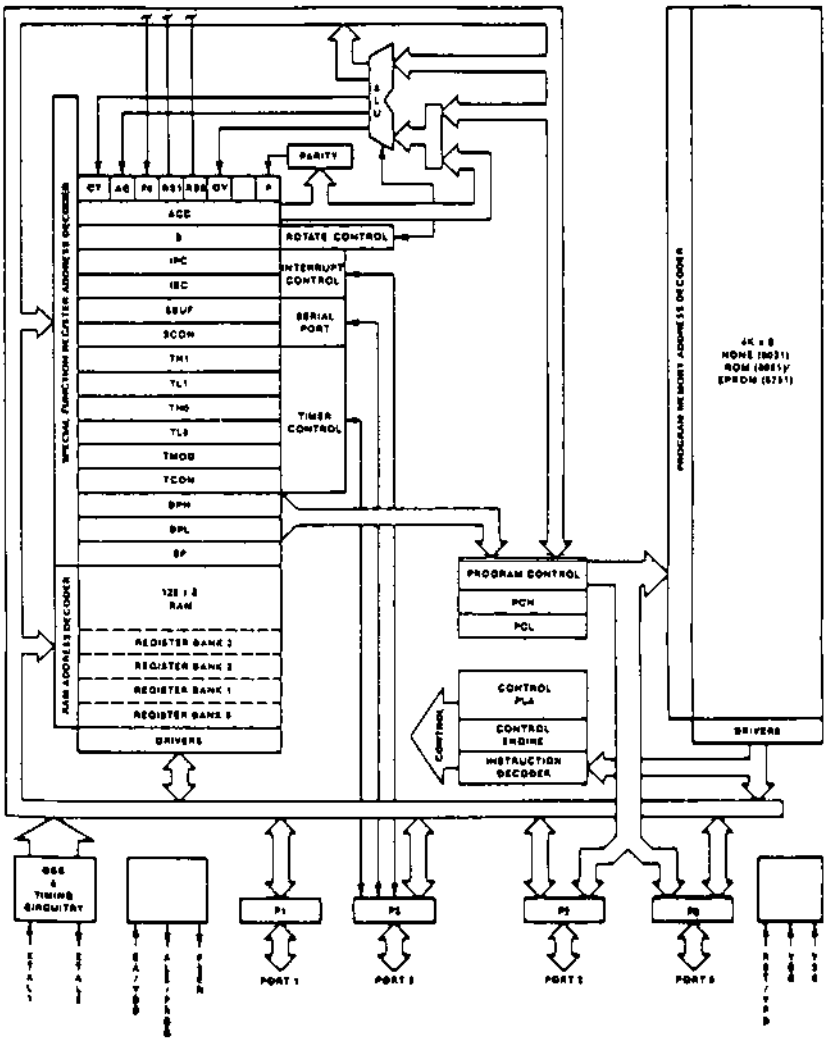
富士通株式会社 シート /

3

61.3. FDXA-4003-5


MPU8
RST/VPP
XC1
XT2
EA
INT0
INT1
P35
P00
P01
P02
P03
P04
P05
P06
P07
P23
P24
P25
P26
P27
P15
P30
P34
P20
P21
P22
P17
P16
P14
P12
P11
P10
P13
AKD
(M1)
(8051)
X1
6MHZ
C1
41μ
R2
8.2K
D1
C2
100P
C3
100P
M4
CN4
CN1
CN2
CN3
CLOCK
DATA
GND
+5V
0V
R4
2.2K
R5
2.2K
C4
56P
C5
56P
R1 100
C10
1000P
MUX
(M2)
(MC151)
BGN
M3
M2
M1
C7
0.1μ
C9
0.1μ
C6
22μ
CIRCUIT SPECIFICATION
N86C-4700-0101
6
FUJITSU LIMITED

Block Diagram




DOCUMENT CONTROL SECTION

DATE

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | |
| | | | | | | | | | | | |
| | | | | | | | | | | | |
| EDIT. | DATE | DESIG. | CHECK | DESCRIPTION | | | | | | | |
| DESIG. | | | CHECK | | | | | APPR. | | | |

TITLE CUSTOM IC PIN SIGNAL AND FUNCTION

DRAW. NO.

CUST.

FUJITSU LIMITED

3/3

61.3. FDXA-4902-5

Disk Drive

# SONY

MECHATRONIC PRODUCTS GROUP

PART NO. : 00-0074

REVISION : 11-88

ISSUE DATE : June 30, 88

## Product Specifications

MODEL NAME :

8790145 (MP-F17W-70D)

## *** Table of Contents ***


1. Description

2. Specifications

   2.1 Configuration

   2.2 Physical Dimensions

   2.3 Weight

   2.4 Performance

      2.4.1 Capacity
      2.4.2 Transfer Rate
      2.4.3 Access Time
      2.4.4 Functional
      2.4.5 Reliability

   2.5 Input Power Requirements

      2.5.1 Power Consumption
      2.5.2 Supply Voltages
      2.5.3 Current Profile

   2.6 Environmental Limits and Orientation

      2.6.1 Temperature
      2.6.2 Humidity
      2.6.3 Vibration
      2.6.4 Shock
      2.6.5 Orientation

3. Interface

   3.1 Pin Assignment

      3.1.1 Signal Connector
      3.1.2 Signal Connector Pin Assignment

   3.2 DC Characteristics of Interface Signals

      3.2.1 Output Signals from Drive
      3.2.2 Inputs Signal to Drive

3.3 Signal Definitions

3.3.1 DRIVE SELECT 0,1,2,3
3.3.2 MOTOR ON
3.3.3 STEP
3.3.4 DIRECTION
3.3.5 HEAD SELECT
3.3.6 WRITE GATE
3.3.7 WRITE DATA
3.3.8 INDEX
3.3.9 TRACK 00
3.3.10 WRITE PROTECT
3.3.11 READ DATA
3.3.12 DISK CHANGE

3.4 Timing Requirements

3.4.1 Head Access
3.4.2 TRACK 00 Signal
3.4.3 Write Data Timing
3.4.4 Read Data Timing
3.4.5 Index Pulse
3.4.6 Disk Change

3.5 Power on and Power off Requirements

3.5.1 Data Protection
3.5.2 Power Supply Sequencing

3.6 Disk Motor Rotation and Disk Insertion.

3.7 Power-On Reset Timing

4. High Density Read/Write Mode Switch

5. Safety

6. Power On Initialization

## 1. Description

This document describes the specifications of the SONY 3.5" Micro Floppy Disk Drive, the MP-F17W-70D that is designed for general applications, even for lap-top computers. It features a low profile, a low power cunsumption, single power voltage, a light weight, ruggedness, high reliability and easiness to use.

## 2. Specifications

### 2.1 Configuration

The drive consists of Read/Write heads, head positioning mechanism, disk motor, interface logic circuit and Read/Write circuit.

### 2.2 Physical Dimensions

The detailed physical dimensions are shown in Figure 2.1.
The main dimensions are:

1) Height : 25.4 mm (1.0 inch)
2) Width : 101.6 mm (4.0 inches)
3) Depth : 150.0 mm (5.9 inches)
(excluding a front panel thickness)

### 2.3 Weight

Weight : 425 g (0.94 pound)

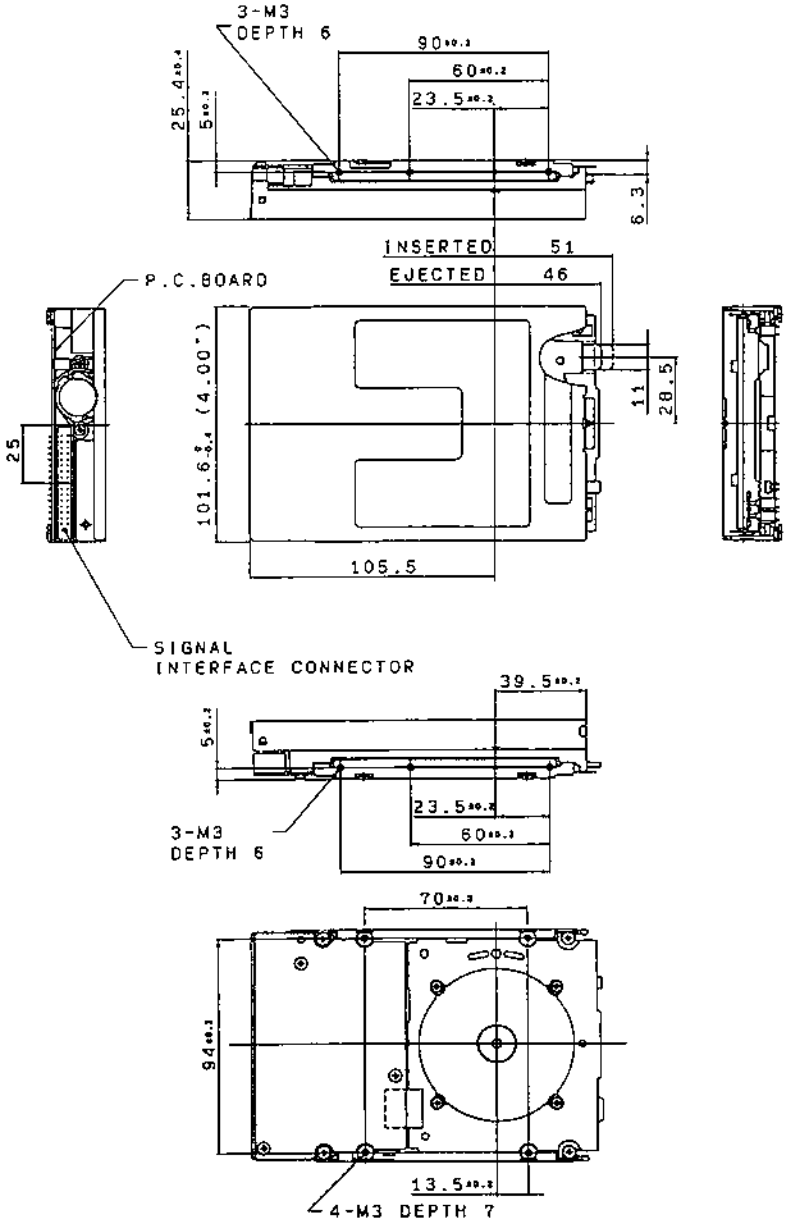
### 2.4 Performance

#### 2.4.1 Recording Capacity (unformatted, MFM)

| 2MB mode | 1MB mode |
|---|---|
| 2.0 Mbytes/disk | 1.0 Mbytes/disk |
| 1.0 Mbytes/surface | 0.5 Mbytes/surface |

#### 2.4.2 Transfer Rate

Burst transfer rate : 500 Kbits/sec for MFM in a 2MB mode
250 Kbits/sec for MFM in a 1MB mode




MP-F11W / F17W-70D OUTLINE DIMENSIONS

2.4.3 Access Time

a. Track to Track Slew Rate : 3 msec min.

b. Head Settling Time : 15 msec max.

c. Motor Start Time : 500 msec max.

2.4.4 Functional

a. Rotation Speed : 300 rpm
The continuous speed variation is within ±1.0%.
The instantanuous speed variation is within ±0.9%.

b. Recording Density : 17434 BPI in a 2MB mode.
(Side 1, Trach 79) 8717 BPI in a 1MB mode.

c. Track Density : 135 TPI

d. Number of Cylinders : 80

e. Number of Tracks : 160

f. R/W Heads : 2

2.4.5 Reliability

a. Mean Time Between Failures (MTBF) : 30,000 POH

b. Mean Time to Repair (MTTR) : 30 minutes

c. Preventive Maintenance (PM) : Not Required

d. Components life : 5 years or 15,000 POH

e. Error Rate :

1. Soft Read Error : Less than 1 per $10^9$ bits read

2. Hard Read Error : Less than 1 per $10^{12}$ bits read

3. Seek Error : Less than 1 per $10^6$ seeks

## 2.5 Input Power Requirements

### 2.5.1 Power Consumption

| | |
|---|---|
| Standby | 0.1 W max. |
| Operation (read/write mode) | 1.1 W typ. |

### 2.5.2 Supply Voltages

| Voltage | Max. Ripple | Current |
|---|---|---|
| +5.0V ±10% | 0.1Vpp | 20 mA max. (Standby)<br>220 mA Typ. (Read/Write)<br>680 mA max. (Motor starts)<br>890 mA max. (Step during motor rotates) |

### 2.5.3 Current Profile

See FIgure 2.2

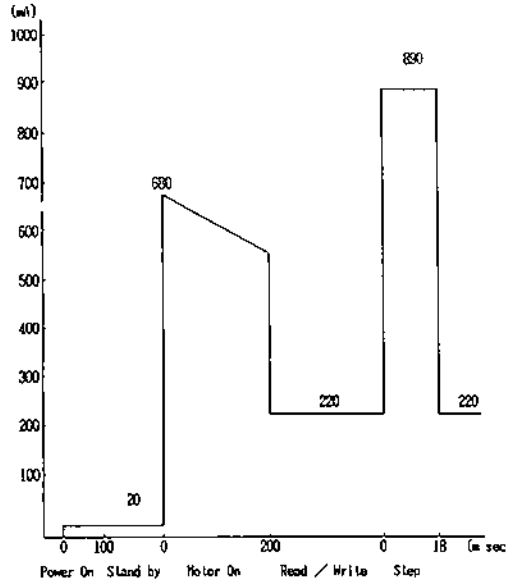



Figure 2.2. Current Profile

## 2.6 Environmental Limits

### 2.6.1 Temperature Range

| | | |
|---|---|---|
| Operating | : 5°C to 50°C ambient | (40°F to 122°F) |
| Transportation | : -40°C to 60°C | (-40°F to 140°F) |
| Storage | : -20°C to 60°C | (-20°F to 140°F) |

### 2.6.2 Humidity Range

Operating : 8% to 80% relative humidity with a wet bulb temperature of 29°C (85F) and no condensation.

Transportation and Storage : 5% to 95% relative humidity with a wet bulb temperature of 29°C (85F) and no condensation.

### 2.6.3 Vibration

Operating : The unit can perform Read/Write operations without errors at continuous vibration from 10 to 500 Hz at a maximum of 0.5G along each of the two mutually perpendicular axes.

Transportation and Storage : The unit can withstand continuous vibration from 10 to 500 Hz with a maximum level of 2.0G along each of the three mutually perpendicular axes without any degradation of any characteristics below the performance specifications.

### 2.6.4 Shock

Operating : The unit can withstand a shock of 5.0G shock for 11 msec with a 1/2 sine wave shape in each of the two mutually perpendicular axis while performing normal read/write functions without damage or any loss of data.

Transportation and Storage : The unit when unpacked can withstand an 11 msec with a 1/2 sine wave shock of 70G on any of the three mutually perpendicular axis.

### 2.6.5 Orientation

The drive can be set horizontal or vertical including a top-loading. The detail orientations are shown in Figure 2.3.

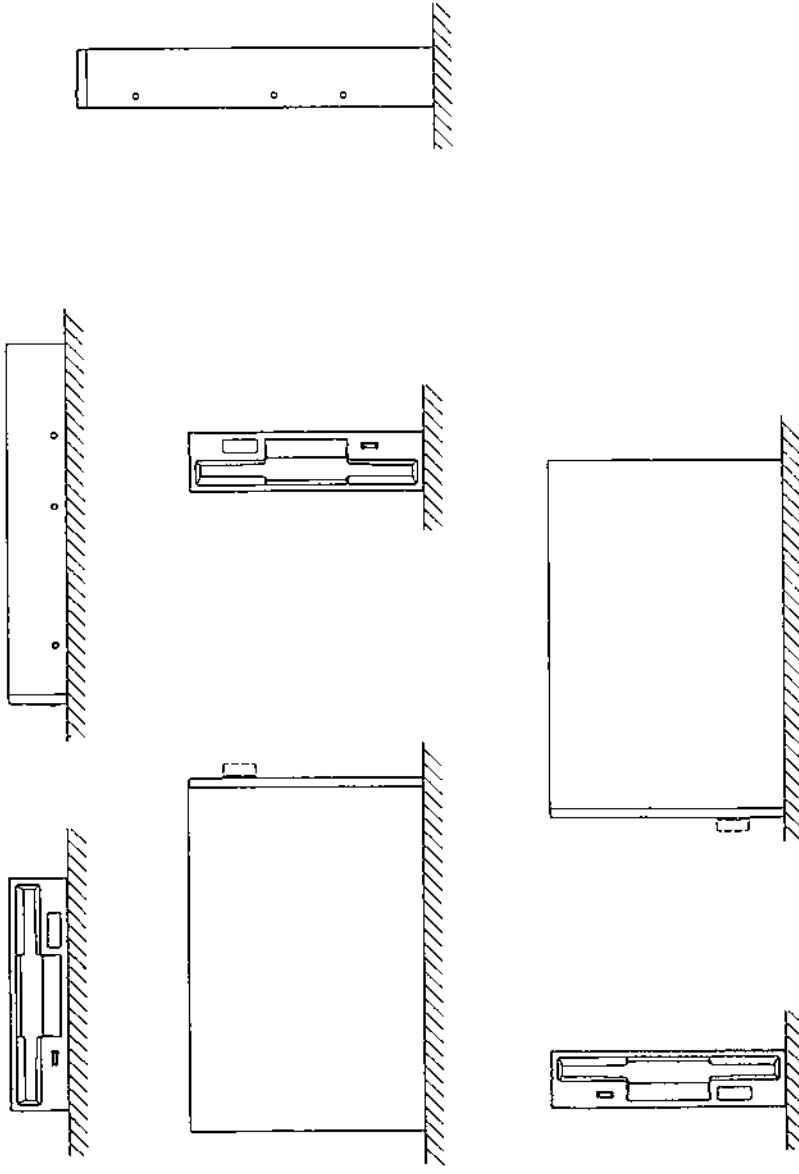


Figure 2.3. Orientations

## 3. Signal Interface

### 3.1 Connector and Pin Assignments

#### 3.1.1 Signal connector

Receptacle : 3M 3414-6500xx or equivalent

Cable : 3M 3365/34 or equivalent

#### 3.1.2 Signal Connector Pin Assignment

| PIN | SIGNAL DESCRIPTION | PIN | SIGNAL DESCRIPTION |
|---|---|---|---|
| 1 | N.C. | 2 | N.C. |
| 3 | N.C. | 4 | N.C. |
| 5 | + 5V | 6 | DRIVE SELECT 3 |
| 7 | + 5V | 8 | INDEX |
| 9 | + 5V | 10 | DRIVE SELECT 0 |
| 11 | + 5V | 12 | DRIVE SELECT 1 |
| 13 | RETURN | 14 | DRIVE SELECT 2 |
| 15 | RETURN | 16 | MOTOR ON |
| 17 | RETURN | 18 | DIRECTION |
| 19 | RETURN | 20 | STEP |
| 21 | RETURN | 22 | WRITE DATA |
| 23 | RETURN | 24 | WRITE GATE |
| 25 | RETURN | 26 | TRACK 00 |
| 27 | RETURN | 28 | WRITE PROTECT |
| 29 | N.C. | 30 | READ DATA |
| 31 | N.C. | 32 | HEAD SELECT |
| 33 | N.C. | 34 | DISK CHANGE |

## 3.2 DC Characteristics of Interface Signals

### 3.2.1 Output Signal from Drive

C-MOS Open Drain Driver is used for the Output.

Output voltage (VOH) : Open
Output voltage (VOL) : 0.4 V max.
Output current (IOL) : 48 mA max.

### 3.2.2 Input Signal to Drive

Input voltage (VIH) : 2.2 V min.
Input voltage (VIL) : 0.8 V max.

### 3.2.3 Recommended Circuit for Signal Interface

The detail interface circuits are shown in Figure 3.1.

A 1K ohm pull-up resister can be put on each output line from the drive. The recommended cable length is 1.5 m (4.92ft.) or less.

Recommended driver ICs : 7406, 7438 or equivalent.

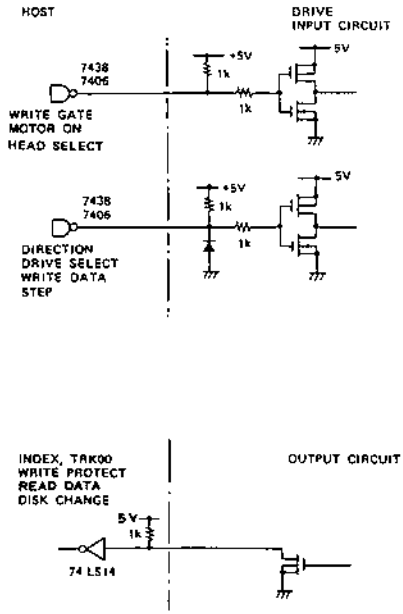



Figure 3.1. Interface Circuits

## 3.3 Signal Definitions

### 3.3.1 DRIVE SELECT 0,1,2,3

The SELECT lines are used to enable or disable all other interface lines except a MOTOR ON line. When the SELECT line is true (low), the drive is enabled and is considered active. When the SELECT line is false (high), all controlled inputs except the MOTOR ON line are ignored and all output lines are disabled.

N.B. IN USE (LED) lamp

When a drive is selected, the IN USE lamp on the selected drive is turned on, and when a drive is not selected, it is turned off.

### 3.3.2 MOTOR ON

When this input is true (low), the spindle motor will start to run. When this line is made false (high), the spindle motor will decelerate and stop. Even if the MOTOR ON signal is low (true), the spindle motor will not rotate until a disk is inserted. If the MOTOR ON signal becomes false during either a write or erase operation, the disk motor will not stop rotating until both the ERASE GATE signal and the WRITE GATE signal become high (false).

### 3.3.3 STEP

When a drive is selected, a true (low) pulse on this line will cause the read/write heads to move to the adjacent track. The direction of the head movement is determined by the DIRECTION input at the trailing edge of the pulse.
The step operation can be performed even if there is no disk inserted in the drive.

### 3.3.4 DIRECTION

When a drive is selected, a false (high) level on this input will cause a STEP input to move the read/write head away from the disk spindle. A true (low) level will cause a STEP input to move the read/write head toward the drive spindle.

### 3.3.5 HEAD SELECT

When a drive is selected, a true (low) level on this input will cause Head 1 (upper) to be selected. A false (high) level on this input will cause Head 0 (lower) to be selected. If the HEAD SELECT signal changes during either write or erase operation, the head will not be changed until both ERASE GATE and WRITE GATE signal become high (false).

### 3.3.6 WRITE GATE

When a drive is selected and this line is made true (low), the write current circuit is enabled and information in the WRITE DATA input may be written.

### 3.3.7 WRITE DATA

If a drive is selected, and the WRITE GATE is true (low), a true pulse (low) on the WRITE DATA line will cause a bit to be written on the disk. Pulses on this line will be neglected when WRITE GATE is false (high). No pre-compensation is required.

### 3.3.8 INDEX

When the drive is selected, a true (low) pulse is generated on this line by each revolution of the spindle.

### 3.3.9 TRACK 00

This line is true (low) when the drive is selected and the Read/Write head is positioned on track 00.

### 3.3.10 WRITE PROTECT

If a write-protect disk or no disk is inserted while a drive is selected, this line will be true (low) and the drive will not be able to write data.

### 3.3.11 READ DATA

When the drive is selected, a true (low) pulse is generated on this line every time a bit is detected.

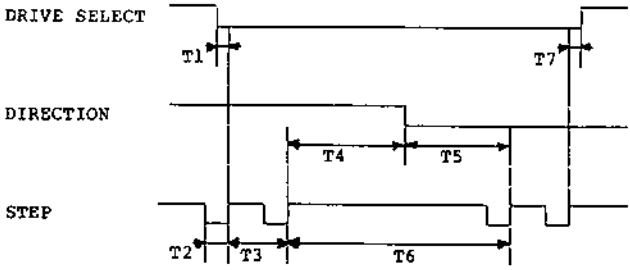
### 3.3.12 DISK CHANGE

This line is true (low) whenever a disk is removed from the drive. The line will remain true (low) until both the following conditions have been met:

1. A disk is inserted.
2. A STEP pulse has been received when the drive is selected.

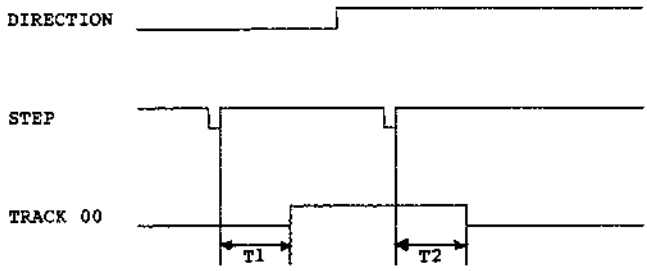
## 3.4 Timing Requirements

### 3.4.1 Head Access




| | | |
|---|---|---|
| T1 | : | 0.5 usec min. |
| T2 | : | 0.5 usec min. |
| T3 | : | 3.0 msec min. |
| T4 | : | 0.5 usec min. |
| T5 | : | 0.5 usec min. |
| T6 | : | 18 msec min. |
| T7 | : | 0.5 usec min. |

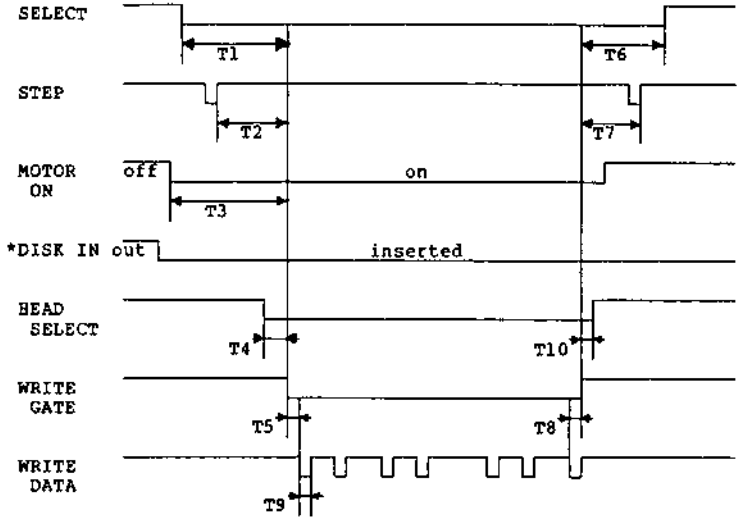
### 3.4.2 TRACK 00 Signal




T1 : 2.9 msec max.

T2 : 2.9 msec max.

### 3.4.3 Write Data Timing

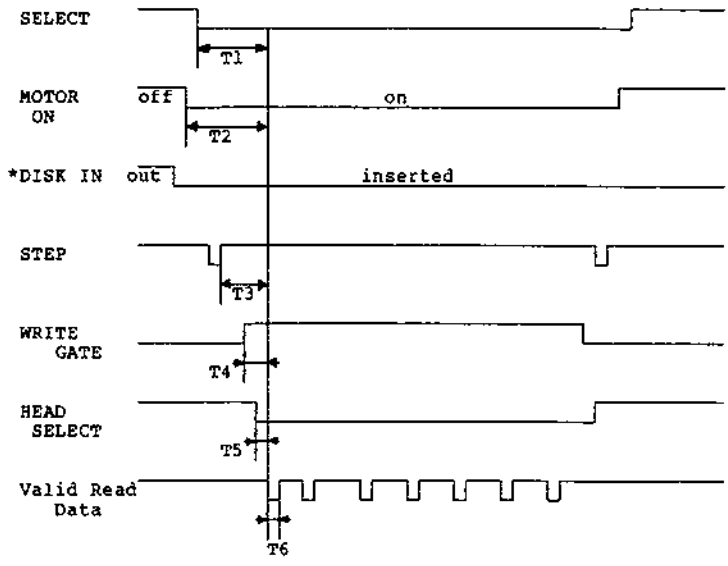



| | | | | | |
|---|---|---|---|---|---|
| T1 | : | 0.5 usec min. | T6 | : | 0.5 usec min. |
| T2 | : | 18 msec min. | T7 | : | 585 usec min. |
| T3 | : | 500 msec min. | T8 | : | 4 usec max.<br>(8 usec max.) |
| T4 | : | 100 usec min. | T9 | : | 150 ns min., 1000 ns max.<br>(150 ns min., 2000 ns max.) |
| T5 | : | 4 usec max.<br>(8 usec max.) | T10 | : | See 3.3.5 |

***NB.** All figures in parenthesis are for a 1MB mode only.

*DISK IN, the disk-in sensor signal inside the drive, is low when a disk is inserted in the drive.

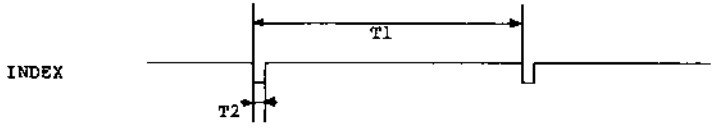
### 3.4.4 Read Data Timing




| | | | | | |
|---|---|---|---|---|---|
| T1 | : | 0.5 usec max. | T4 | : | 615 usec max |
| T2 | : | 500 msec max. | T5 | : | 100 usec max |
| T3 | : | 18 msec max. | T6 | : | 350 nsec min., 550 nsec max. |

*DISK IN, the disk-in sensor signal inside the drive, is low when a disk is inserted in the drive.

### 3.4.5 Index Pulse

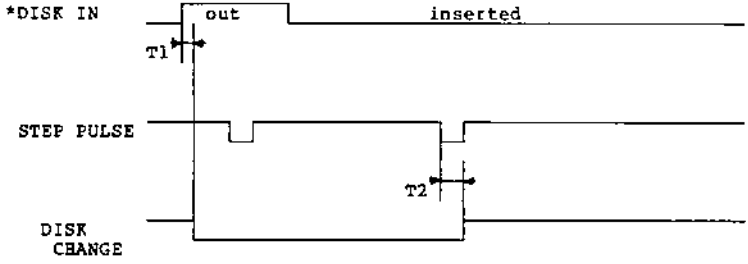



T1* : 198 msec min., 202 msec max.

T2 : 1.5 msec min., 1.7 msec max.

*When the disk motor rotation is at the steady state.

### 3.4.6 Disk Change




T1 : 0.5 usec max. T2 : 1.0 usec max.

*DISK IN, the disk-in sensor signal inside the drive, is low when a disk is inserted in the drive.

### 3.5 Power On and Power off Requirements

#### 3.5.1 Data Protection

Turning power on or off will not cause any damage to recorded data on the disk as long as the drive is not in the midst of writing when the power is shut off or supplied.

#### 3.5.2 Power Supply Sequencing

When the power is turned on, no special power supply sequencing is required. When the power is turned off, the power supply must fall monotonically to zero volt.

### 3.6 Power-On Reset Timing

A drive will be ready in 100 msec after power on. It takes up to 100 msec to reset the control IC of the drive.

## 4. Safety

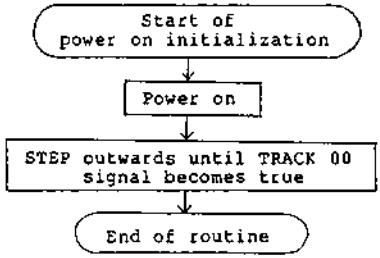
The drive will meet the following product safety regulations:

U.L. 478
C.S.A. C.22.2, No.154

5. Power On Initialization

In order to reduce the peak current requirement when drives are used in a daisy chain, the MP-F17W-70D has been designed not to seek track 00 automatically. If all the drives connected in the daisy chain sought trach 00 simultaneously, this would place a significant power drain on the host system.
Thus, the host system must perform the following routine just after power on in order to reset the track counter inside the drive.

Power on initialization



SONY

MECHATRONIC PRODUCTS GROUP

PART NO. : 061

REVISION : 11-88

ISSUE DATE : Mar. 4, 88

# OEM MANUAL

MODEL NAME :

MP-F11W / MP-F17W

*** Table of Contents ***

1. INTRODUCTION
   1-1. Purpose
   1-2. General description

2. MECHANISM
   2-1. Chassis
   2-2. Cassette compartment mechanism
   2-3. Disk chucking and disk rotation mechanism
   2-4. Magnetic head carriage
   2-5. Head positioning mechanism
   2-6. Detection mechanism

3. ELECTRONICS
   3-1. Read/write circuit
   3-2. Control circuit
   3-3. Spindle motor driver circuit
   3-4. Stepping motor driver circuit

4. SPECIFICATIONS
   4-1. Drive performance
   4-2. Dimensional data

5. INTERFACE DESCRIPTION
   5-1. Host system interface
   5-2. Signal interface

6. EJECT BUTTON, INDICATOR AND SELECT SWITCH
   6-1. Eject button
   6-2. Indicator
   6-3. Drive select switch

7. OPERATION
   7-1. Disk cartridge description
   7-2. Disk cartridge preparation for write protection
   7-3. Operation
   7-4. Disk precaution

8. ORIENTATION AND INSTALLATION
   8-1. Orientation
   8-2. Installation

9. ERROR DETECTION AND CORRECTION
   9-1. Write error
   9-2. Read error

# 1. INTRODUCTION

## 1-1. Purpose

This material provides the information necessary to interface the MP-F11W/MP-F17W Micro Floppydisk drive to a floppy disk controller.

## 1-2. General description

The SONY Micro Floppydisk Drive represents a technological break through offering extreme lightweight, compactness, (101.6mm wide by 25.4mm high by 150.0mm deep, weighting 425g) that provides a versatile data storage component for the systems designer.

SONY's leadership in high-density recording techniques, perfected in video technology, enabled SONY engineers to develop the 3.5" Micro Floppydisk standard. Yet an unformatted, storage capacity of 1MBytes (MP-F11W, double density), 2MBytes (MP-F17W high density) in 135 tracks per inch provides that of conventional 5.25" disks or more.

A semi-rigid protective shell provides protection unique to the Micro Floppydisk. When the disk is inserted into or taken out of the drive, its shutter automatically opens and closes to protect the disk from dust, dirt, fingerprints and other foreign objects that might degrade performance. A metal centering hub allows positioning with greater ease and more positive accuracy in over 30,000 disk interchanges.

The SONY proprietary read/write and tunnel erase head, developed using video techniques, is positioned by a precision stepper motor assembly, providing fast access while maintaining high positioning accuracy. High coercivity media accomplishes high data integrity with the SONY high density head.

The SONY Micro Floppydisk drive is interface signal-compatible with conventional 5" floppydisk drives. Accordingly, popular FDC chips such as Western Digital FD1WDs, NEC μPD765 series can be used.

Whether your application is small business systems, test instruments, personal computers or any related application, you will find that the Micro Floppydisk drive will offer a whole new range of possibilities.

The Micro Floppydisk drive offers the following features :

* 3.5" floppy disk media with automatic shutter mechanism
* Large capacity ..... 1MB(MP-F11W) / 2MB(MP-F17W)
* Small footprint
* Light weight
* Low power consumption
* High track density ..... 135 TPI
* High reliability ..... MTBF 30,000POHs
* High transfer rate ..... 250Kbps(1MB), 500Kbps(2MB)

## 2. MECHANISM

The mechanism mounted on the chassis consists of a cassette compartment mechanism, a disk chucking and disk rotation mechanism, magnetic heads and carriage, a head positioning mechanism, some detectors, and so on.

### 2-1. Chassis

The chassis made of aluminum diecast is strong, highly durable, and precision-manufactured. This is the base structure for mounting most of mechanisms and printed circuit board.

### 2-2. Cassette compartment mechanism

The cassette compartment mechanism precisely positions the cassette on chassis by one touch operation. The mechanism is designed that the cassette is ejected easily as well.

### 2-3. Disk chucking and disk rotation mechanism

The disk chucking mechanism is mounted on the top of the thin brushless direct drive DC motor. The disk chucking mechanism precisely positions a disk and drives it.

The disk rotation mechanism directly mouted in a chassis consists of a printed circuit board for drive control, a rotor magnet, a rotor yoke, a stator yoke, and so on.

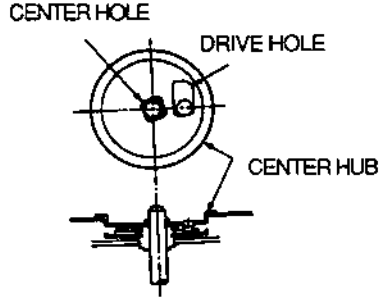



Fig. 2-1 Chucking Mechanism

## 2-4. Magnetic heads and head carriage

The tunnel erase type head with narrow track width is developed to attain a 135 TPI track density. The head is designed for higher Read signal quality. The head surface is treated for less the disk wear and the head wear. The head comprises a read/write gap to read and write data and two erase gaps to erase the recorded track edge immediately after recording. The heads and the carriage are very impotant parts in the MFDD, so they are especially precision-assembled.

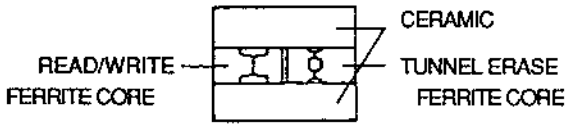



Fig. 2-2 Magnetic Head

## 2-5. Head positioning mechanism

The head positioning mechanism consists of a stepping motor, a lead screw, a bearing, and a guide shaft. The head carriage is held with the guide shaft and the lead screw with stepping motor. The 4-phase stepping motor rotates 2 micro steps (18°X 2) per track.

## 2-6. Detection mechanism

a) Write protect

The micro switch is mounted on the printed circuit board to detect the position of the write protect tab on the disk. If a write-protected disk is inserted and the micro switch is not pushed down, the recording/erasing power is not supplied and the data is protected from an erroneous writing command.

b) Track 00

The mechanism consists of a photo-interrupter to detect the outermost track position (Track 00). The head carriage is not moved more outer track, after the MFDD detects the Track 00. So, the head and head positioning mechanism do not get damaged.

c) Index

Since the MFDD is designed to make the spindle motor and the disk be fixed in the same corresponding position, the Index pluse is generated by the spindle motor circuit.

d) Disk-in

If the cassette pushes the micro switch on the printed circuit board, it is detected that the cassette is inserted.

e) Density select (Only for MP-F17Ws)

The micro switch is mounted on the printed circuit board to detect the hole of the high density disk. If a high density cassette is inserted and the micro switch is not pushed, the MFDD works in high density mode. If a nomal density disk is inserted and the micro switch is pushed down, the MFDD works in normal density mode.

## 3. ELECTRONICS

The electronics of the MFDD consists of a read/write circuit, a control circuit and some drivers, and so forth. The electronic circuits are mounted on two printed circuit boards (Motor and Logic boards).

### 3-1. Read/write circuit

The read/write circuit consists of a read circuit, a write circuit, and a power on detection circuit. These circuits are mostly included in a read/write amplifier LSI(bipolar) on the Logic board.

### 3-2. Control circuit

The control circuit consists of an input and output interface circuit, a spindle motor control circuit, a stepping motor control circuit, a sensor circuit, and a function control circuit. These circuits are mostly included in a control LSI(C-MOS) on the Logic board.

### 3-3. Spindle motor driver circuit

This circuit consists of a three phase spindle motor driver, a rotation speed detector, a rotation phase detector, and a current limiter. These circuits are mostly included in a spindle motor driver IC(bipolar) on the Motor board.

### 3-4. Stepping motor driver circuit

This circuit consists of two bridge driver circuits. The IC is made by the bipolar process, which is mounted in the Logic board.

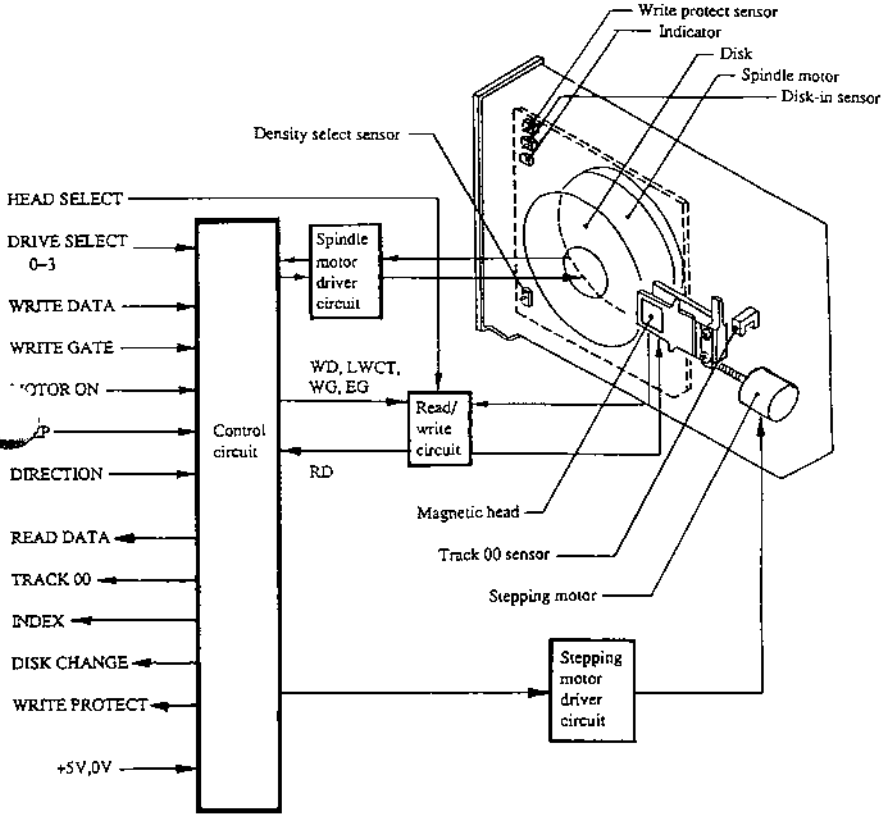



Fig. 3-1 General Block Diagram

# 4. SPECIFICATIONS

## 4-1. Drive performance

Table 4-1 lists performance specifications for the SONY Micro Floppydisk drive.

TABLE 4-1 Performance Specifications

| Specification | MP-F11W | MP-F17W (2MB mode) |
|---|---|---|
| CAPACITY | | |
| Unformatted per disk | 1MB for MFM | 2MB for MFM |
| Unformatted per track | 6.25KB for MFM | 12.5KB for MFM |
| Recording density | 8,717BPI | 17,434BPI |
| Burst transfer rate | 250Kbits/sec | 500Kbits/sec |
| ACCESS TIME | | |
| Track to track | 3msec | |
| Settling Time | 15msec | |
| FUNCTIONAL | | |
| Rotational speed | 300rpm | |
| Track density | 135TPI | |
| Cylinders | 80 | |
| Tracks | 160 | |
| R/W heads | 2 | |
| Encoding method | MFM or FM | |
| POWER CONSUMPTION | | |
| Read/Write mode | 220mA | |
| Standby mode | 20mA(TTL I/F), 6mA(C-MOS I/F) | |

**4-2. Dimensional data**

Table 4-2 lists the dimensional data for the Micro Floppydisk drive.

TABLE 4-2 Dimensional Data

| Physical Dimension | Value |
|---|---|
| Height | 25.4 mm |
| Width | 101.6 mm |
| Depth | 150.0 mm |
| Weight | 425 g |

## 5. INTERFACE DESCRIPTION

### 5-1. Host system interface

The SONY Micro Floppydisk drive is compatible with conventional floppy disk controllers. The interface consists of 15 signal lines for data, control and hand-shaking (see Figure 5-1, details will appear in a product specification of each mode).

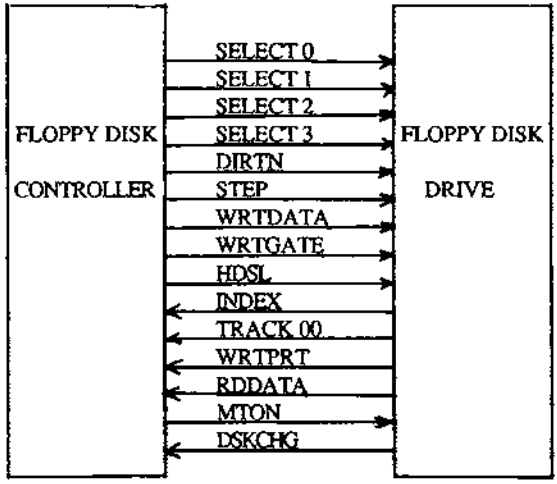



Fig. 5-1 Interface Signal Diagram

## 5-2. Signal interface

The drive has 15 interface signals. Ten signals are input to the drive, and six are output.

Table 5-2 MNEMONIC

| SIGNAL DESCRIPTION | MNEMONIC |
|---|---|
| DRIVE SELECT 0 | SELECT 0 |
| DRIVE SELECT 1 | SELECT 1 |
| DRIVE SELECT 2 | SELECT 2 |
| DRIVE SELECT 3 | SELECT 3 |
| DIRECTION SELECT | DIRTN |
| STEP | STEP |
| WRITE DATA | WRTDATA |
| WRITE GATE | WRTGATE |
| HEAD SELECT | HDSL |
| INDEX | INDEX |
| TRACK00 | TRK00 |
| WRITE PROTECT | WRTPRT |
| READ DATA | RDDATA |
| MOTOR ON | MTON |
| DISK CHANGE | DSKCHG |

## 6. EJECT BUTTON, INDICATOR AND SELECT SWITCH

### 6-1. Eject button

The eject button (see Fig. 6-1) is used to remove a disk cartridge from the unit. Depression of the eject button causes the disk cartridge in the unit to be ejected.

### 6-2. Indicator

The activity indicator (see Fig. 6-1) indicates that a drive is selected.

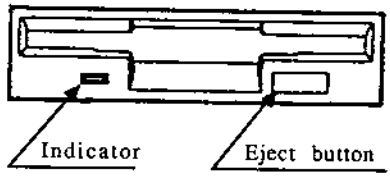



Fig. 6-1 Front Bezel

**6-3. Drive select switch**

Drive Select switch located next to a power connector on the rear side is used to designate drive0 up to drive3 in a daisy chain application. Usually, this switch is set to drive 1 in shipping from the drive factory.

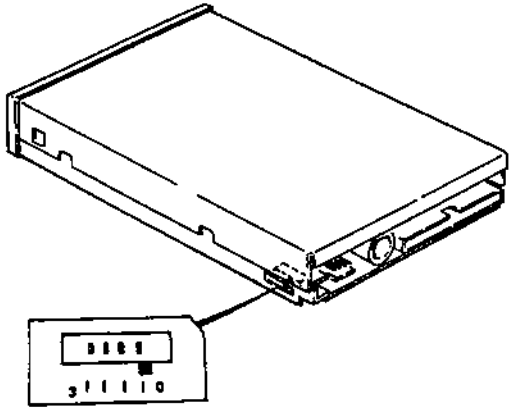



Fig. 6-2 Drive Select Switch

# SECTION 4
# PART REPLACEMENT

## 4-1 COVER ASS'Y REPLACEMENT

### 4-1-1 Removal

a. Insert your finger into the rear right side portion of the Cover Ass'y as shown in Fig. 4-1, and dislocate the Cover Ass'y from the hook while applying some force to the direction marked with arrow. The whole Cover Ass'y can be taken out.

### 4-1-2 Installation

a. Match the projection located in the front side of the Cover Ass'y with square hole of the front panel ass'y and then put the rear of the Cover Ass'y into the proper position. (Refer to Fig. 4-1)

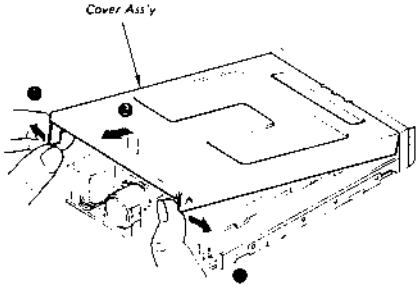



*Fig. 4-1 Cover Ass'y Replacement*

## 4-2 FRONT PANEL ASS'Y AND EJECT BUTTON REPLACEMENT

### 4-2-1 Removal

a. Remove the cover ass'y. (Refer to 4-1)

b. Push slightly the plastic hinges located on each of right and left sides with (-) shaped screw driver through the square hole of upper cover, and pull it slowly toward you. (Refer to Fig. 4-2)

c. Dislocate the Eject Button from the hook of the slide plate.

### 4-2-2 Installation

a. Hang the Eject Button to the hook of slide plate as shown Fig. 4-2.

b. Install the Front Panel Ass'y into the metal frame by sliding in the hook located on each side of the Front Panel Ass'y.

c. Make sure that protuberances of LED and the Eject Button are properly located in the recess and square hole of the Front Panel Ass'y.

d. Install the cover ass'y. (Refer to 4-1)

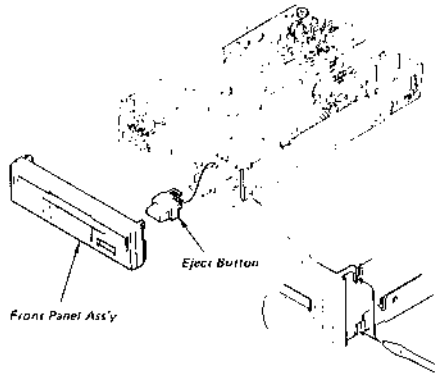



*Fig. 4-2 Front Panel Ass'y Replacement*

## 4-3 LG-2 MOUNTED BOARD REPLACEMENT

### 4-3-1 Removal

a. Remove the cover ass'y. (Refer to 4-1)

b. Disconnect the all connectors. (CN102 for stepping motor, CN104 for 00 sensor, CN105 and CN106 for head carriage ass'y)

c. Desolder the jumper cable (CN1) on MT-2 mounted board with soldering iron.

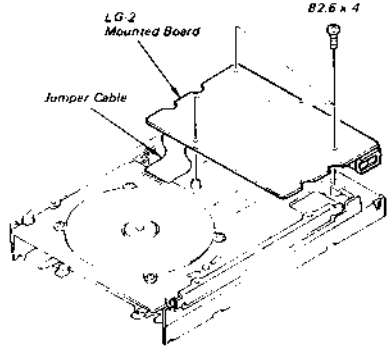



*Fig. 4-3 LG-2 Mounted Board Replacement*

d. Remove the three screws (B2.6x4) securing the LG-2 Mounted Board and then remove the LG-2 Mounted Board. (Refer to Fig. 4-3)

**4-3-2 Installation**

a. Solder the jumper cable to the CN1 of MT-2 mounted board.

b. Install the LG-2 Mounted Board with three screws (B2.6x4).

c. Connect the all connectors.

d. Perform the Radial Alignment and TRK00 sensor Adjustment. (Refer to 5-1)

e. Install the cover ass'y. (Refer to 4-1)

## 4-4 MT-2 MOUNTED BOARD REPLACEMENT

**4-4-1 Removal**

a. Desolder the jumper cable on MT-2 Mounted Board with soldering iron.

b. Remove the four screws (P2.6x4) securing the Stator Yoke Ass'y and then remove the Stator Yoke Ass'y. (Refer to Fig. 4-4)

c. Disconnect the connector CN2 (hall IC ass'y) and then remove the MT-2 Mounted Board.

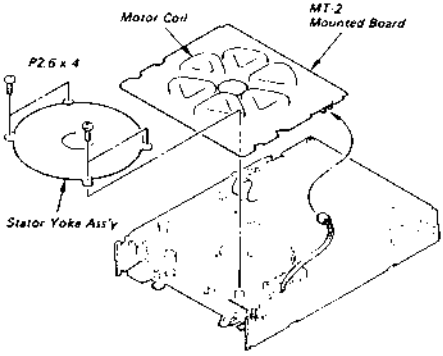



*Fig. 4-4 MT-2 Mounted Board Replacement*

**4-4-2 Installation**

a. Connect the connector CN2 (hall IC ass'y) onto the MT-2 Mounted Board.

b. Solder the Jumper Cable to CN1 of MT-2 Mounted Board.

c. Match the hole of the MT-2 Mounted Board with the emboss of the chassis ass'y.

d. Install the Stator Yoke Ass'y on MT-2 Mounted Board with four screws (P2.6x4), not to damage to six motor coils for disk motor. (Refer to Fig. 4-4)

## 4-5 HALL IC ASS'Y REPLACEMENT

**4-5-1 Removal**

a. Remove the four screws (P2.6x4) securing the stator yoke ass'y and then remove the stator yoke ass'y. (Refer to Fig. 4-4)

b. Disconnect the connector CN2 (Hall IC Ass'y).

c. Remove the screw (PSW2x5/LR PSW2x5) securing the Hall IC Ass'y and then remove the Hall IC Ass'y. (Refer to Fig. 4-5)

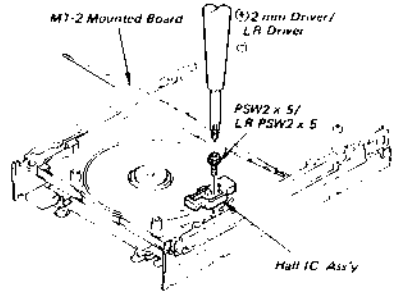



*Fig. 4-5 Hall IC Ass'y Replacement*

**4-5-2 Installation**

a. Fasten loosely the Hall IC Ass'y with a screw (PSW2x5/LR PSW2x5). But this screw must not be tightened for later adjustment.

b. Connect the connector CN2 (Hall IC Ass'y) onto the MT-2 mounted board.

c. Match the hole of the MT-2 mounted board with the emboss of the chassis ass'y.

d. Install the stator yoke ass'y on MT-2 mounted board with four screws (P2.6x4), not to damage to six motor coils for disk motor. (Refer to Fig. 4-4)

e. Perform the Index phase adjustment. (Refer to 5-3)

## 4-6 CASSETTE HOLDER ASS'Y REPLACEMENT

### 4-6-1 Removal

a. Connect the drive to the MFD Function Checker II (Refer to Fig. 2-14), move the head to the TRK00 and then disconnect the drive from MFD Function Checker II.

b. Remove the cover ass'y. (Refer to 4-1)

c. Remove the front panel ass'y and eject button. (Refer to 4-2)

d. Be careful not to apply the excessive force to the head carriage ass'y. While pushing the eject lever, take the Cassette Holder Ass'y. (Refer to Fig. 4-6)

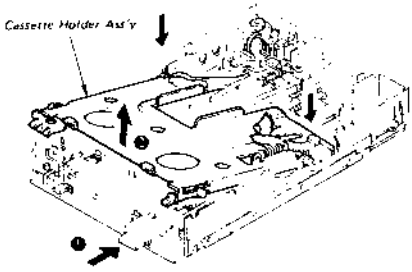



*Fig. 4-6 Cassette Holder Ass'y Replacement*

### 4-6-2 Installation

a. Insert carefully the Cassette Holder Ass'y underneath the arm of the head carriage ass'y, then set the holder into the location shown by arrow as shown in Fig. 4-6, while pushing the eject lever.

b. Install the front panel ass'y and eject button. (Refer to 4-2)

c. Install the cover ass'y. (Refer to 4-1)

## 4-7 SLIDE PLATE ASS'Y REPLACEMENT

### 4-7-1 Removal

a. Remove the cover ass'y. (Refer to 4-1)

b. Remove the front panel ass'y and eject button. (Refer to 4-2)

c. Remove the cassette holder ass'y. (Refer to 4-6)

d. Slide the trigger arm to set the Disk In-mode as shown in Fig. 4-7.

e. Remove the one end of Tension Springs on chassis ass'y and then take the Slide Plate Ass'y. (Refer to Fig. 4-7)

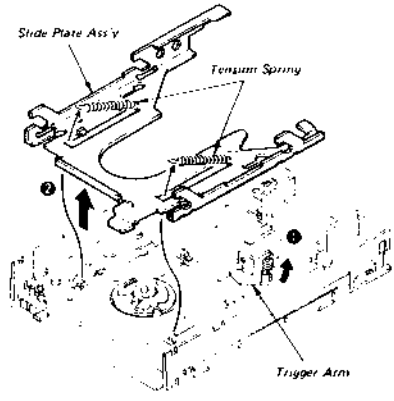



*Fig. 4-7 Slide Plate Ass'y Replacement*

### 4-7-2 Installation

a. While pushing the trigger arm, set the Slide Plate Ass'y into the location shown in Fig. 4-7.

b. Hang the Tension Springs on hook of chassis ass'y.

c. Push the Slide Plate Ass'y, while pushing the trigger arm back side. (This stays "disk-in mode")

d. Install the cassette holder ass'y. (Refer to 4-6)

e. Install the front panel ass'y and eject button. (Refer to 4-2)

f. Install the cover ass'y. (Refer to 4-1)

g. Make the head clean. (Refer to 5-4)

## 4-8 00 SENSOR REPLACEMENT

### 4-8-1 Removal

a. Connect the drive to the MFD Function Checker II as shown in Fig. 2-14, move the head to TRK79 and then disconnect the drive from the MFD Function Checker II.

b. Remove the cover ass'y. (Refer to 4-1)

c. Disconnect the connector CN104 (00 Sensor) from the LG-2 mounted board.

d. Remove the screw (PSW2.6x6) securing the 00 Sensor and remove 00 Sensor. (Refer to Fig. 4-8)

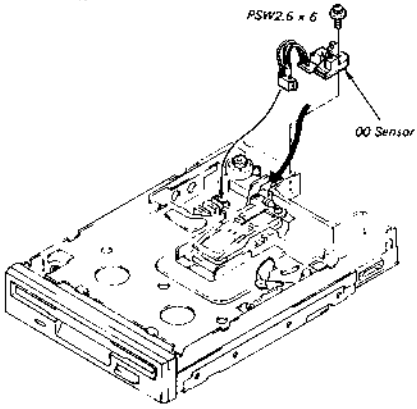



*Fig. 4-8 00 Sensor Replacement*

### 4-8-2 Installation

a. Install the 00 Sensor with a screw (PSW2.6x6).

b. Connect the CN104 connector onto the LG-2 mounted board.

c. Perform the radial alignment and TRK00 sensor adjustment. (Refer to 5-1)

d. Install the cover ass'y. (Refer to 4-1)

## 4-9 HEAD CARRIAGE ASS'Y REPLACEMENT

### 4-9-1 Removal

a. Remove the cover ass'y. (Refer to 4-1)

b. Remove the front panel ass'y and eject button. (Refer to 4-2)

c. Remove the cassette holder ass'y. (Refer to 4-6)

d. Disconnect the connectors CN105 and CN106 (flexible boards) from the LG-2 mounted board.

e. Remove the screw (P2.6x4) securing the Guide Retainer and then remove the Guide Retainer, Head Carriage Ass'y and Slide Guide Shaft. (Refer to Fig. 4-9)

### 4-9-2 Installation

Note: Apply Sony oil to the Guide Shaft before installation. Apply Sony oil to the openings of Head Carriage Ass'y using the bamboo stick.

a. Pass the Guide Shaft through the opening of Head Carriage Ass'y.

Note: The spring of Head Carriage Ass'y, that is located in around shaft hole, should be installed inside so that the Guide Shaft is forced outwardly by the spring force, as shown in Fig. 4-9.

b. Put the Head Carriage Ass'y and the Slide Guide Shaft in place, and install the guide retainer with a screw (P2.6x4). (Refer to Fig. 4-9)

c. Connect the flexible boards to CN105 and CN106 on the LG-2 mounted board.

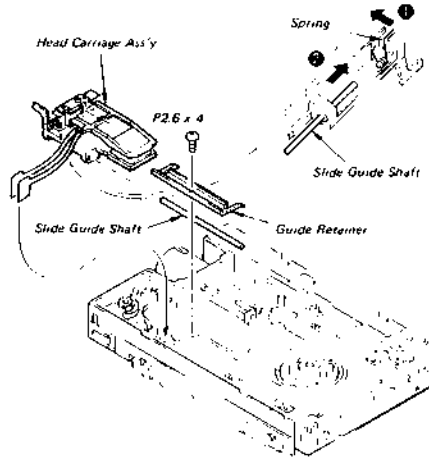



*Fig. 4-9 Head Carriage Ass'y Replacement*

d. Install the cassette holder ass'y. (Refer to 4-6)

e. Install the front panel ass'y and eject button. (Refer to 4-2)

f. Perform the radial alignment and TRK00 sensor adjustment. (Refer to 5-1)

g. Perform the head compliance. (Refer to 5-2)

h. Install the cover ass'y. (Refer to 4-1)

i. Make the head clean. (Refer to 5-4)

## 4-10 STEPPING MOTOR ASS'Y (ROTOR ASS'Y AND STATOR ASS'Y) REPLACEMENT

### 4-10-1 Removal

a. Remove the cover ass'y. (Refer to 4-1)

b. Remove the front panel ass'y and eject button. (Refer to 4-2)

c. Remove the cassette holder ass'y. (Refer to 4-6)

d. Disconnect the connector CN102 (Stator Ass'y) from the LG-2 mounted board.

e. Remove the three screws (B2.6x4) securing LG-2 mounted board so that removal of Stator Ass'y can be easily performed.

f. Remove the two screws (PSW2.6x5) securing the Stator Ass'y and then remove the Stator Ass'y and steel ball. (Refer to Fig. 4-10)

g. Wipe away the grease applied around lead screw with soft cloth before removal of Stator Ass'y and Rotor Ass'y, not to leave the grease in the chass'y hole during the removal.

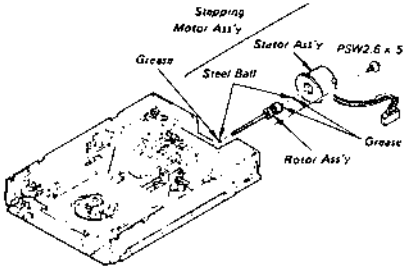



*Fig. 4-10 Stepping Motor Ass'y (Stator Ass'y and Rotor Ass'y) Replacement*

h. While twisting Rotor Ass'y, separate the Rotor Ass'y from the needle pin of head carriage ass'y.

i. Take the steel ball from the hole of chassis ass'y.

### 4-10-2 Installation

Note: The stepping motor must be replaced with the whole ass'y, since the wrong combination (Rotor Ass'y and Stator Ass'y) in the ass'y causes the mulfunction.

Note: Apply Molykote Grease (EM101) (same quantity of match tip) on whole area of lead screw and two steel balls before the installation.

a. Insert the steel ball into hole of the chassis ass'y.

b. While lifting the head carriage ass'y a little, insert the lead screw of the Rotor Ass'y between the needle and plate spring of head carriage ass'y.

c. Insert the steel ball into hole of Rotor Ass'y.

d. Fasten loosely the Stator Ass'y with two screws (PSW2.6x5). But these screws must not be tightened for later adjustment.

e. Connect the connector CN102 (Rotor Ass'y) onto the LG-2 mounted board.

f. Install the cassette holder ass'y. (Refer to 4-6)

g. Install the front panel ass'y and eject button. (Refer to 4-2)

h. Perform the radial alignment and TRK00 sensor adjustment. (Refer to 5-1)

i. Install the cover ass'y. (Refer to 4-1)

j. Make the head clean. (Refer to 5-4)

## 4-11 OIL DAMPER REPLACEMENT

### 4-11-1 Removal

a. Remove the cover ass'y. (Refer to 4-1)

b. Remove one screw (P2x5) securing the Damper to chassy ass'y.

c. Lift up the Damper and take it out. (Refer to Fig. 4-11)

### 4-11-2 Installation

a. Insert one end of the Damper (small hole) into the boss.

b. Align the Damper gear with the teeth portion of the slide plate ass'y.

c. Secure the Damper with the screw (P2x5).

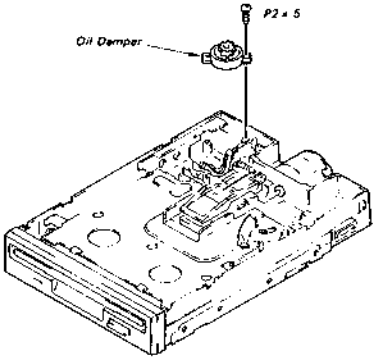



*Fig. 4-11 Oil Damper Replacement*

## 4-12 COMBINATION OF HEAD CARRIAGE ASS'Y AND LG-2 MOUNTED BOARD

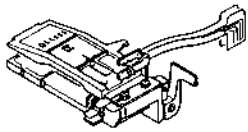
This drive has two types of combination, consisting of Head Carriage Ass'y and LG-2 Mounted Board. We call them as "high current type" and "low current type" for easy reference. The combination must not be mixed up, otherwise the unit may not satisfy the original specification.

a. "High current type"

Marking on Head Carriage Ass'y

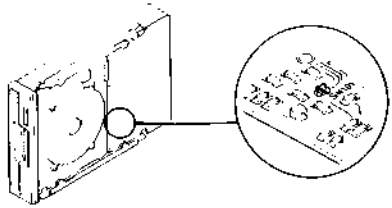
The letter must be "Q" in the first wording on the ass'y.

Parts No.; A-8010-249-A



Setting of SH101

If SH101 is not shorted with soldering, short SH101 with a soldering. As the result, R178 (33K) is connected in parallel to other resistors R155/R156.

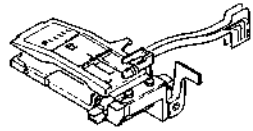


b. "Low currency type"

Marking on Head Carriage Ass'y

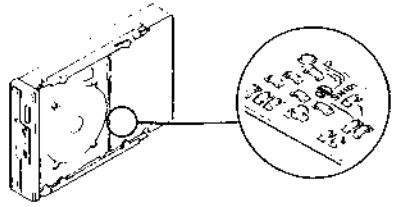
The letter must be "P" in the first wording on the ass'y.

Parts No.; A-8010-248-A



Setting of SH101

If SH101 is shorted with soldering, remove soldering. As the result, R178 (33K) is disconnected.



## 6-2. MECHANICAL PARTS LIST

Note: 1. Parts printed in **Bold-Face type** are normally stocked for replacement purposes. The remaining parts shown in this list are not normally required for routine service work. Orders for parts not shown in **Bold-Face type** will be processed, but allow for additional delivery time.

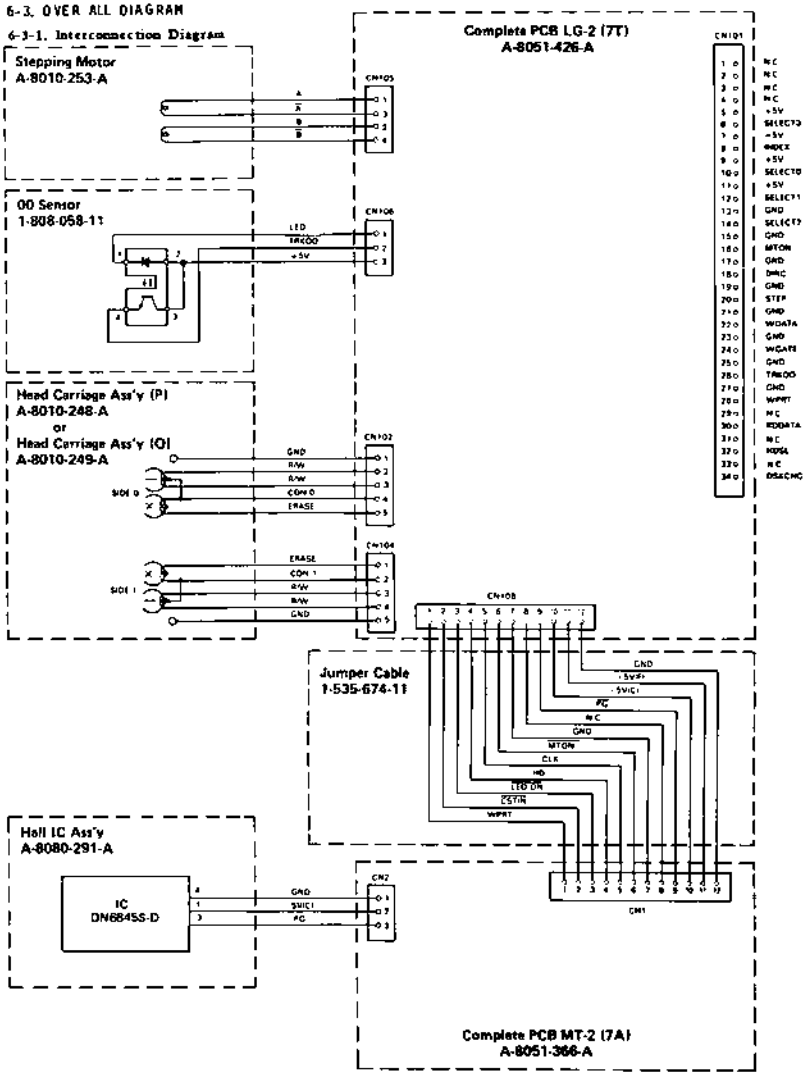
2. The screws and washers may be supplied with the substitution that is similar to ones listed because of part-standardization program in SONY.

3. Before part's ordering or replacement, refer to section 4-12 "Combination of Head Carriage Ass'y and LG-2 Mounted Board".

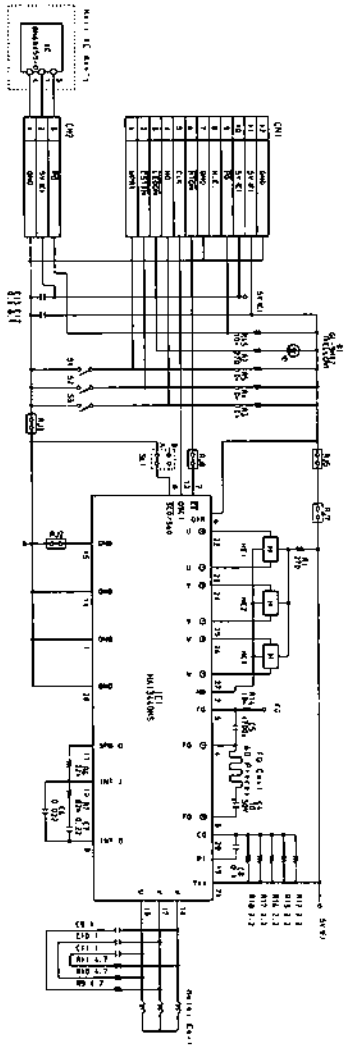
| No. | Parts No. | Description |
|---|---|---|
| **1** | **A-8010-248-A** | **Head Carriage Ass'y (P) (Refer to Note 3)** |
| | **A-8010-249-A** | **Head Carriage Ass'y (Q) (Refer to Note 3)** |
| **2** | **A-8010-283-A** | **Cassette Holder Ass'y** |
| **3** | **A-8010-253-A** | **Stepping Motor Ass'y** |
| **4** | **4-613-114-01** | **Tension Spring** |
| 5 | A-8010-234-A | Slide Plate Ass'y |
| **6** | **4-613-132-01** | **Tension Spring** |
| 7 | A-8051-426-A | LG-2 (7T) Mounted Board (Refer to Note 3) |
| **8** | **A-8051-366-A** | **MT-2 (7A) Mounted Board** |
| 9 | A-8080-291-A | Hall IC Ass'y |
| **10** | **8-759-404-25** | **DN6845S-D** |
| 11 | 4-613-138-11 | Stator Yoke |
| **12** | **1-808-058-11** | **DD Sensor** |
| 13 | 4-606-001-11 | Slide Guide Shaft |
| 14 | 4-613-103-01 | Trigger Arm |
| 15 | 4-613-104-01 | Spring |
| 16 | 4-613-105-01 | Guide Retainer |
| 17 | X-4613-105-1 | Bracket Ass'y (Left) |
| 18 | X-4613-106-1 | Bracket Ass'y (Right) |
| **19** | **4-613-145-02** | **Cover** |
| **20** | **3-701-428-01** | **Special Screw +B 2.6x4** |
| **21** | **3-712-786-01** | **Oil Damper** |
| | 7-621-255-35 | Screw +P 2x5 |
| | 7-621-259-25 | Screw +P 2.6x4 |
| | 7-621-775-20 | Screw +B 2.6x5 |
| | 4-613-717-01 | Screw LR PSW 2x5 |
| | 7-621-759-35 | Screw PSW 2.6x5 |
| | | (Serial No. 7,500,000 thru 7,502,220) |
| | 4-614-322-01 | Screw LR PSW 2.6x5 |
| | | (Serial No. 7,502,221 thru 7,600,000) |
| | 7-621-759-45 | Screw +PSW 2.6x6 |
| | 7-623-923-11 | Nylone Washer 2.6 |

## 6-3. OVER ALL DIAGRAM

### 6-3-1. Interconnection Diagram



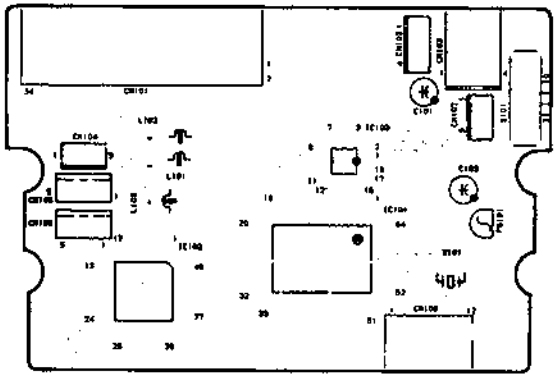
6-4-2. Circuit Diagram on MT-2 (7A)



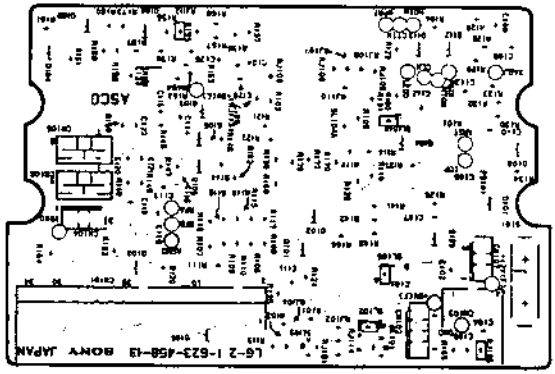
## 6-5. PARTS LAYOUT

### 6-5-1. Parts Layout on LG-2 (7T)

- Component Side -

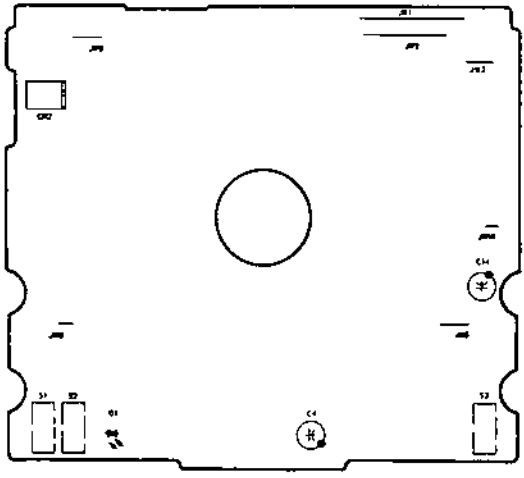


- Pattern Side -

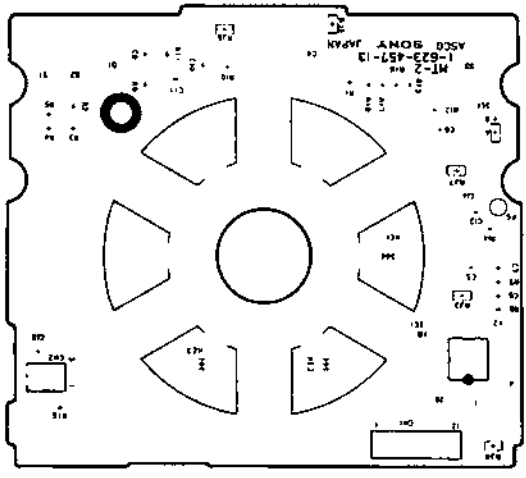


6-5-2. Parts Layout on MT-2 (7A)

- Component Side -



- Pattern Side -



## 6-6. ELECTRIC PARTS

### 6-6-1. ELECTRIC PARTS LIST

Note: 1. All capacitors are in micro farads unless otherwise specified.

2. All inductors are in micro henries unless otherwise specified.

3. All resistors are in ohms.

4. "CHIP" stands for chip component.

| Ref. No. | Parts No. | Description | | | |
|---|---|---|---|---|---|
| LC-2 (7T) MOUNTED BOARD | | | | | |
| **CAPACITORS** | | | | | |
| C101 | 1-126-154-11 | ELECT | 47 | 20% | 6.3V |
| C102 | 1-163-038-00 | CERAMIC CHIP | 0.1 | | 25V |
| C106 | 1-163-038-00 | CERAMIC CHIP | 0.1 | | 25V |
| C107 | 1-163-809-11 | CERAMIC CHIP | 0.047 | 10% | 25V |
| C108 | 1-163-038-00 | CERAMIC CHIP | 0.1 | | 25V |
| C109 | 1-163-038-00 | CERAMIC CHIP | 0.1 | | 25V |
| C110 | 1-163-038-00 | CERAMIC CHIP | 0.1 | | 25V |
| C111 | 1-163-809-11 | CERAMIC CHIP | 0.047 | 10% | 25V |
| C112 | 1-163-241-11 | CERAMIC CHIP | 39PF | 5% | 50V |
| C113 | 1-163-241-11 | CERAMIC CHIP | 39PF | 5% | 50V |
| C114 | 1-163-017-00 | CERAMIC CHIP | 0.0047 | 10% | 50V |
| C115 | 1-163-013-00 | CERAMIC CHIP | 0.0022 | 10% | 50V |
| C116 | 1-163-145-00 | CERAMIC CHIP | 0.0015 | 5% | 50V |
| C117 | 1-163-145-00 | CERAMIC CHIP | 0.0015 | 5% | 50V |
| C118 | 1-163-129-00 | CERAMIC CHIP | 330PF | 5% | 50V |
| C119 | 1-163-129-00 | CERAMIC CHIP | 330PF | 5% | 50V |
| C120 | 1-163-809-11 | CERAMIC CHIP | 0.047 | 10% | 25V |
| C121 | 1-163-809-11 | CERAMIC CHIP | 0.047 | 10% | 25V |
| C122 | 1-163-809-11 | CERAMIC CHIP | 0.047 | 10% | 25V |
| C123 | 1-163-038-00 | CERAMIC CHIP | 0.1 | | 25V |
| C124 | 1-163-809-11 | CERAMIC CHIP | 0.047 | 10% | 25V |
| C125 | 1-163-809-11 | CERAMIC CHIP | 0.047 | 10% | 25V |
| C126 | 1-163-038-00 | CERAMIC CHIP | 0.1 | | 25V |
| **CONNECTORS** | | | | | |
| CN101 | 1-564-941-11 | HEADER, CONNECTOR 34P | | | |
| CN102 | 1-564-003-00 | PIN, CONNECTOR 4P | | | |
| CN104 | 1-564-002-00 | PIN, CONNECTOR 3P | | | |
| CN105 | 1-562-787-21 | CONNECTOR, FLEXIBLE 5P | | | |
| CN106 | 1-562-787-21 | CONNECTOR, FLEXIBLE 5P | | | |
| CN108 | 1-535-674-11 | JUMPER CABLE | | | |
| **ICS** | | | | | |
| IC101 | 8-752-325-50 | CXD1142Q | | | |
| IC102 | 8-752-033-09 | CXA1286Q-Z | | | |
| IC103 | 8-759-305-19 | HA13421AMP | | | |
| **COILS** | | | | | |
| L101 | 1-408-795-21 | INDUCTOR CHIP 33D | | | |
| L102 | 1-408-795-21 | INDUCTOR CHIP 33D | | | |
| L103 | 1-408-783-00 | INDUCTOR CHIP 33 | | | |
| **RESISTORS** | | | | | |
| R101 | 1-216-049-00 | METAL CHIP | 1K | 5% | 1/10W |
| R105 | 1-216-049-00 | METAL CHIP | 1K | 5% | 1/10W |
| R106 | 1-216-049-00 | METAL CHIP | 1K | 5% | 1/10W |
| R107 | 1-216-049-00 | METAL CHIP | 1K | 5% | 1/10W |
| R108 | 1-216-049-00 | METAL CHIP | 1K | 5% | 1/10W |
| R109 | 1-216-049-00 | METAL CHIP | 1K | 5% | 1/10W |
| R110 | 1-216-049-00 | METAL CHIP | 1K | 5% | 1/10W |
| R111 | 1-216-049-00 | METAL CHIP | 1K | 5% | 1/10W |
| R112 | 1-216-049-00 | METAL CHIP | 1K | 5% | 1/10W |
| R114 | 1-216-049-00 | METAL CHIP | 1K | 5% | 1/10W |
| R115 | 1-216-049-00 | METAL CHIP | 1K | 5% | 1/10W |
| R116 | 1-216-049-00 | METAL CHIP | 1K | 5% | 1/10W |
| R117 | 1-216-049-00 | METAL CHIP | 1K | 5% | 1/10W |
| R118 | 1-216-049-00 | METAL CHIP | 1K | 5% | 1/10W |
| R119 | 1-216-049-00 | METAL CHIP | 1K | 5% | 1/10W |
| R120 | 1-216-049-00 | METAL CHIP | 1K | 5% | 1/10W |
| R122 | 1-216-085-00 | METAL CHIP | 33K | 5% | 1/10W |
| R124 | 1-216-073-00 | METAL CHIP | 10K | 5% | 1/10W |
| R125 | 1-216-045-00 | METAL CHIP | 680 | 5% | 1/10W |
| R126 | 1-216-073-00 | METAL CHIP | 10K | 5% | 1/10W |
| R127 | 1-216-045-00 | METAL CHIP | 680 | 5% | 1/10W |
| R128 | 1-216-085-00 | METAL CHIP | 33K | 5% | 1/10W |
| R129 | 1-216-085-00 | METAL CHIP | 33K | 5% | 1/10W |
| R130 | 1-216-119-00 | METAL CHIP | 820K | 5% | 1/10W |
| R131 | 1-216-073-00 | METAL CHIP | 10K | 5% | 1/10W |
| R132 | 1-216-073-00 | METAL CHIP | 10K | 5% | 1/10W |
| R133 | 1-216-049-00 | METAL CHIP | 1K | 5% | 1/10W |
| R134 | 1-216-097-00 | METAL CHIP | 100K | 5% | 1/10W |
| R136 | 1-216-059-00 | METAL CHIP | 2.7K | 5% | 1/10W |
| R138 | 1-216-059-00 | METAL CHIP | 2.7K | 5% | 1/10W |
| R139 | 1-216-166-00 | METAL CHIP | 47 | 5% | 1/8W |
| R140 | 1-216-166-00 | METAL CHIP | 47 | 5% | 1/8W |
| R141 | 1-216-166-00 | METAL CHIP | 47 | 5% | 1/8W |
| R142 | 1-216-166-00 | METAL CHIP | 47 | 5% | 1/8W |
| R143 | 1-216-166-00 | METAL CHIP | 47 | 5% | 1/8W |
| R144 | 1-216-097-00 | METAL CHIP | 100K | 5% | 1/10W |
| R145 | 1-216-023-00 | METAL CHIP | 82 | 5% | 1/10W |
| R146 | 1-216-121-00 | METAL CHIP | 1M | 5% | 1/10W |
| R147 | 1-216-049-00 | METAL CHIP | 1K | 5% | 1/10W |
| R148 | 1-216-041-00 | METAL CHIP | 470 | 5% | 1/10W |
| R149 | 1-216-041-00 | METAL CHIP | 470 | 5% | 1/10W |
| R150 | 1-216-077-00 | METAL CHIP | 15K | 5% | 1/10W |
| R151 | 1-216-071-00 | METAL CHIP | 8.2K | 5% | 1/10W |
| R152 | 1-216-077-00 | METAL CHIP | 15K | 5% | 1/10W |
| R153 | 1-216-748-11 | METAL CHIP | 39K | 1% | 1/10W |
| R154 | 1-216-748-11 | METAL CHIP | 39K | 1% | 1/10W |
| R155 | 1-216-092-00 | METAL CHIP | 56K | 5% | 1/10W |
| R156 | 1-216-069-00 | METAL CHIP | 6.8K | 5% | 1/10W |
| R157 | 1-216-069-00 | METAL CHIP | 6.8K | 5% | 1/10W |
| R158 | 1-216-083-00 | METAL CHIP | 27K | 5% | 1/10W |

| Ref. No. | Parts No. | Description | | | |
|---|---|---|---|---|---|
| R159 | 1-216-081-00 | METAL CHIP | 22K | 5% | 1/10W |
| R160 | 1-216-097-00 | METAL CHIP | 100K | 5% | 1/10W |
| R161 | 1-216-047-00 | METAL CHIP | 820 | 5% | 1/10W |
| R163 | 1-216-073-00 | METAL CHIP | 10K | 5% | 1/10W |
| R164 | 1-216-180-00 | METAL CHIP | 180 | 5% | 1/8W |
| R168 | 1-216-089-00 | METAL CHIP | 47K | 5% | 1/10W |
| R170 | 1-216-089-00 | METAL CHIP | 47K | 5% | 1/10W |
| R173 | 1-216-097-00 | METAL CHIP | 100K | 5% | 1/10W |
| R176 | 1-216-073-00 | METAL CHIP | 10K | 5% | 1/10W |
| R177 | 1-216-073-00 | METAL CHIP | 10K | 5% | 1/10W |
| R178 | 1-216-085-00 | METAL CHIP | 33K | 5% | 1/10W |
| R180 | 1-216-073-00 | METAL CHIP | 10K | 5% | 1/10W |
| RJ105 | 1-216-295-00 | METAL CHIP | 0 | 5% | 1/10W |
| RJ112 | 1-216-295-00 | METAL CHIP | 0 | 5% | 1/10W |
| SLA105 | 1-216-295-00 | METAL CHIP | 0 | 5% | 1/10W |
| SLB102 | 1-216-295-00 | METAL CHIP | 0 | 5% | 1/10W |
| SLB103 | 1-216-295-00 | METAL CHIP | 0 | 5% | 1/10W |
| SLB104 | 1-216-295-00 | METAL CHIP | 0 | 5% | 1/10W |

**TRANSISTORS**

| | | |
|---|---|---|
| Q101 | 8-729-162-44 | 2SB624-BV4 (CHIP) |
| Q102 | 8-729-900-53 | DTC114EK (CHIP) |
| Q103 | 8-729-162-44 | 2SB624-BV4 (CHIP) |
| Q104 | 8-729-900-53 | DTC114EK (CHIP) |
| Q105 | 8-729-900-53 | DTC114EK (CHIP) |
| Q106 | 8-729-900-53 | DTC114EK (CHIP) |
| Q107 | 8-729-109-42 | 2SK94-X2 (CHIP) |
| Q108 | 8-729-109-42 | 2SK94-X2 (CHIP) |
| Q109 | 8-729-109-42 | 2SK94-X2 (CHIP) |

**DIODES**

| | | |
|---|---|---|
| D101 | 8-719-100-03 | 1S2835 (CHIP) |
| D102 | 8-719-100-03 | 1S2835 (CHIP) |
| D103 | 8-719-100-05 | 1S2837 (CHIP) |
| D104 | 8-719-100-05 | 1S2837 (CHIP) |
| D106 | 8-719-100-03 | 1S2835 (CHIP) |

**IC LINK**

| | | |
|---|---|---|
| PS101 | 1-532-727-11 | IC LINK |

**SWITCH**

| | | |
|---|---|---|
| S101 | 1-554-644-00 | SWITCH, SLIDE |

**OSCILLATOR**

| | | |
|---|---|---|
| X101 | 1-567-912-11 | OSCILLATOR, CERAMIC (4.91M) |

MT-2 (7A) MOUNTED BOARD

**CAPACITORS**

| | | | | | |
|---|---|---|---|---|---|
| C4 | 1-124-261-00 | ELECT | 10 | 20% | 50V |
| C5 | 1-163-017-00 | CERAMIC CHIP | 0.0047 | 10% | 50V |
| C6 | 1-163-037-11 | CERAMIC CHIP | 0.022 | 10% | 25V |
| C7 | 1-163-081-00 | CERAMIC CHIP | 0.22 | | 25V |
| C8 | 1-163-038-00 | CERAMIC CHIP | 0.1 | | 25V |
| C9 | 1-162-638-11 | CERAMIC CHIP | 1 | | 16V |
| C10 | 1-162-638-11 | CERAMIC CHIP | 1 | | 16V |
| C11 | 1-162-638-11 | CERAMIC CHIP | 1 | | 16V |
| C12 | 1-163-038-00 | CERAMIC CHIP | 0.1 | | 25V |
| C13 | 1-163-038-00 | CERAMIC CHIP | 0.1 | | 25V |

| Ref. No. | Parts No. | Description | | | |
|---|---|---|---|---|---|
| | | **RESISTORS** | | | |
| R1 | 1-216-035-00 | METAL CHIP | 270 | 5% | 1/10W |
| R2 | 1-216-184-00 | METAL CHIP | 270 | 5% | 1/8W |
| R3 | 1-216-073-00 | METAL CHIP | 10K | 5% | 1/10W |
| R4 | 1-216-073-00 | METAL CHIP | 10K | 5% | 1/10W |
| R5 | 1-216-073-00 | METAL CHIP | 10K | 5% | 1/10W |
| R6 | 1-216-081-00 | METAL CHIP | 22K | 5% | 1/10W |
| R7 | 1-216-095-00 | METAL CHIP | 82K | 5% | 1/10W |
| R9 | 1-216-142-00 | METAL CHIP | 4.7 | 5% | 1/8W |
| R10 | 1-216-142-00 | METAL CHIP | 4.7 | 5% | 1/8W |
| R11 | 1-216-142-00 | METAL CHIP | 4.7 | 5% | 1/8W |
| R12 | 1-216-298-00 | METAL CHIP | 2.2 | 5% | 1/10W |
| R13 | 1-216-298-00 | METAL CHIP | 2.2 | 5% | 1/10W |
| R14 | 1-216-073-00 | METAL CHIP | 10K | 5% | 1/10W |
| R15 | 1-216-073-00 | METAL CHIP | 10K | 5% | 1/10W |
| R16 | 1-216-298-00 | METAL CHIP | 2.2 | 5% | 1/10W |
| R17 | 1-216-298-00 | METAL CHIP | 2.2 | 5% | 1/10W |
| R18 | 1-216-298-00 | METAL CHIP | 2.2 | 5% | 1/10W |
| RJ2 | 1-216-296-00 | METAL CHIP | 0 | 5% | 1/8W |
| RJ3 | 1-216-295-00 | METAL CHIP | 0 | 5% | 1/10W |
| RJ5 | 1-216-295-00 | METAL CHIP | 0 | 5% | 1/10W |
| RJ7 | 1-216-296-00 | METAL CHIP | 0 | 5% | 1/8W |
| | (Serial No. 1,027,501 and higher) | | | | |
| RJ8 | 1-216-295-00 | METAL CHIP | 0 | 5% | 1/10W |
| SLA1 | 1-216-295-00 | METAL CHIP | 0 | 5% | 1/10W |

**CONNECTOR**

| | | |
|---|---|---|
| CN2 | 1-566-427-11 | PIN, CONNECTOR 3P |

**DIODE**

| | | |
|---|---|---|
| D1 | 8-719-904-92 | GL-9HY2 (Yellow) |

**IC**

| | | |
|---|---|---|
| IC1 | 8-759-305-25 | HA13440MS |

**SWITCHES**

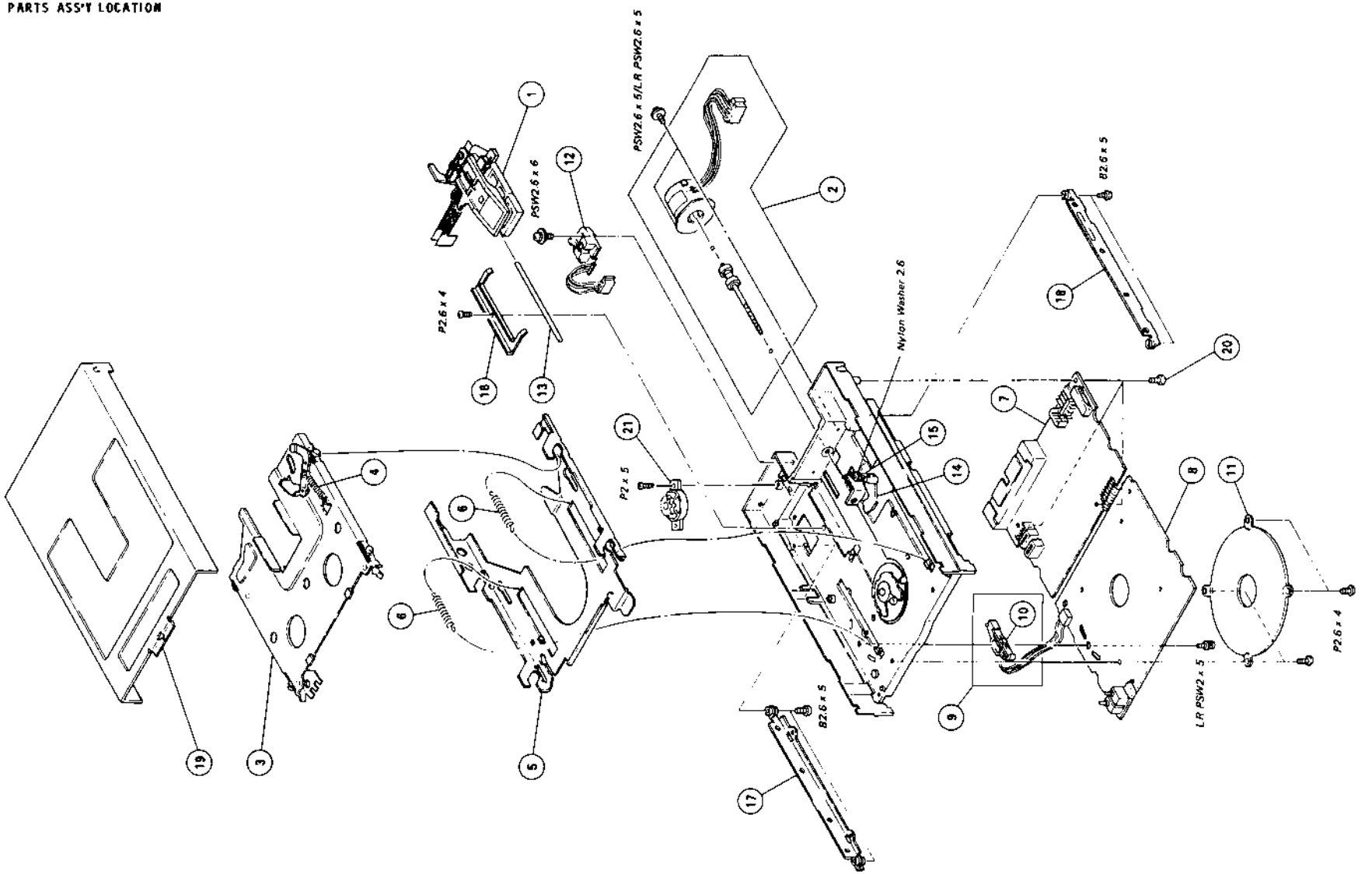
| | | |
|---|---|---|
| S1 | 1-571-237-11 | SWITCH, MICRO |
| S2 | 1-571-237-11 | SWITCH, MICRO |
| S3 | 1-571-237-11 | SWITCH, MICRO |

# SECTION 6

## PARTS LOCATION AND LIST

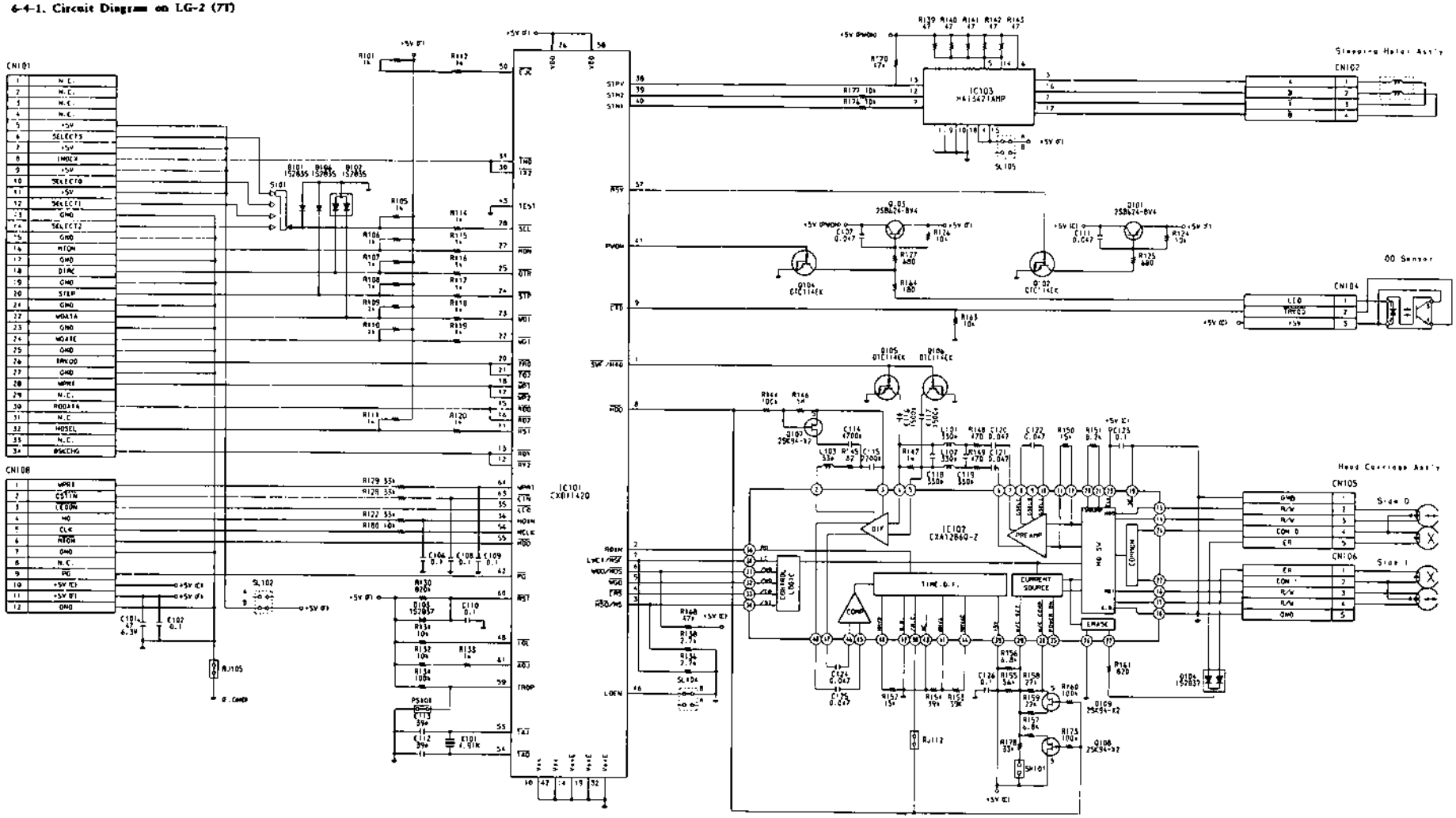
(Serial No. 7,500,001 thru 7,600,000)

6-1. PARTS ASS'Y LOCATION



## 6-4. CIRCUIT DIAGRAM

### 6-4-1. Circuit Diagram on LG-2 (7T)



Software

# SOFTWARE

# Software Contents

## BIOS Services


Device I/O Services ..... 1
Video Display ..... 3
Equipment ..... 14
Memory Size ..... 15
Floppy Diskette Drive I/O Support ..... 16
Floppy Disk Parameter Pointer ..... 23
Hard Disk Support ..... 24
Hard Disk Parameter Pointer ..... 33
Serial Communications ..... 34
Multi-Tasking Support ..... 37
Keyboard ..... 45
Line Printer ..... 50
System Clock ..... 52


## MS-DOS Memory Map


High-Level Memory Map ..... 57
Interrupt Vector Table ..... 58
ROM BIOS Data Area ..... 60
MS-DOS and BASIC Data Area ..... 65


## Keyboard ASCII and Scan Codes


Keyboard ASCII and Scan Codes ..... 67

# Tandy 3000 NL BIOS Services

## Device I/O Services

The BIOS (Basic Input/Output System) is the lowest-level interface between other software (application programs and the operating system itself) and the hardware. The BIOS routines provide various device input/output services, as well as boot strap, and print screen, and other services. Some of the services that BIOS provides, such as the graphics routines, are not available through the operating system,

All calls to the BIOS are made through software interrupts (that is, by means of assembly-language "INT x" instructions). Each I/O device is provided with a software interrupt, that transfers execution to the routine.

Entry parameters to BIOS routines are normally passed in CPU registers. Similarly, exit parameters are generally returned from these routines to the caller in CPU registers. To ensure BIOS compatibility with other machines, the register usage and conventions are, for the most part, identical.

The following pages describe the entry and exit requirements for each BIOS routine. To execute a BIOS call, load the registers as indicated under the "Entry Condition Banner." (Register AH contains the function number in cases where a single interrupt can perform more than one operation.) Then issue the interrupt given for the call. For example, the following can be used to read a character from the keyboard:

```
MOV AH,0
INT 16H
```

Upon return, AL contains the ASCII character and AH contains the keyboard scan code.

**Note:** All registers except those used to return parameters to the caller are saved and restored by the BIOS routines.

Following is a quick reference list of software interrupts for all device I/O and system status services.

| Service | Software Interrupts |
|---|---|
| Video Display | 10 hex (16 dec) |
| Equipment | 11 hex (17 dec) |
| Memory Size | 12 hex (18 dec) |
| Floppy Disk | 13 hex (19 dec) |
| Hard Disk | 13 hex (19 dec) |
| Serial Communications | 14 hex (20 dec) |
| Multi-Tasking Support | 15 hex (21 dec) |
| Joystick | 15 hex (21 dec) |
| Microsecond Delay | 15 hex (21 dec) |
| Extended Memory | 15 hex (21 dec) |
| Virtual Mode | 15 hex (21 dec) |
| Keyboard | 16 hex (22 dec) |
| Line Printer | 17 hex (23 dec) |
| System Clock | 1A hex (26 dec) |
| Floppy Disk Parameter | 1E hex (30 dec) |
| Hard Disk 0 Parameter | 41 hex (65 dec) |
| Hard Disk 1 Parameter | 46 hex (70 dec) |

# Video Display

These routines provide an interface to the video display, which is the half of the console (CON) device that is for output. MS-DOS considers the video display to be the default standard output (STDOUT) device.

**Software Interrupt:** 10 hex (16 dec)

**Function Summary:**

**Control Routines:**

| | | |
|---|---|---|
| AH = | 00H | Set CRT mode |
| AH = | 01H | Set cursor type |
| AH = | 02H | Set cursor position |
| AH = | 03H | Get cursor position |
| AH = | 04H | Read light pen position |
| AH = | 05H | Select active page |
| AH = | 06H | Scroll active page up |
| AH = | 07H | Scroll active page down |

**Text Routines:**

| | | |
|---|---|---|
| AH = | 08H | Read attribute/character |
| AH = | 09H | Write attribute/character |
| AH = | 0AH | Write character only |

**Graphics Routines:**

| | | |
|---|---|---|
| AH = | 0BH | Set color palette |
| AH = | 0CH | Write dot |
| AH = | 0DH | Read dot |

**Other Routines:**

| | | |
|---|---|---|
| AH = | 0EH | Write TTY* to active page |
| AH = | 0FH | Get CRT mode |
| AH = | 13H | Write string |

*Screen width is determined by the mode previously set. Some control characters (ASCII 00H-1FH) perform the usual special terminal function. These include (but are not limited to) BEL (07H), BS (08H), LF (0AH), and CR (0DH).

Note that AX is modified on all video calls.

**Function Descriptions:**

# Set CRT Mode

Set CRT mode.

# Entry Conditions:

AH = 00H
AL = mode value, as follows:

Alpha Modes

| | |
|---|---|
| AL = 0 | 40 x 25 monochrome |
| AL = 1 | 40 x 25 color |
| AL = 2 | 80 x 25 monochrome |
| AL = 3 | 80 x 25 color |

Graphics Modes

| | |
|---|---|
| AL = 4 | 320 x 200 color graphics |
| AL = 5 | 320 x 200 monochrome graphics |
| AL = 6 | 640 x 200 monochrome graphics |
| AL = 7 | 80 x 25 monochrome with mono text adapter |

## Set Cursor Type

Set the cursor type and attribute.

## Entry Conditions:

AH = 01H
CH = bit values:
Setting bits 5-6 causes an invisible or erratically blinking cursor
Bits 4-0 point to the start line for cursor within character cell
CL = bit values:
Bits 4-0 point to the end line for cursor within character cell

## Set Cursor Position

Write (set) cursor position.

## Entry Conditions:

AH = 02H
BH = page number (must be 0 for graphics modes or when used with mono text adapter)
DH = row (0 = top row)
DL = column (0 = leftmost position)

## Get Cursor Position

Read (get) cursor position.

## Entry Conditions:

AH = 03H
BH = page number (must be 0 for graphics modes or when used with mono text adapter)

## Exit Conditions:

DH = row of current cursor position (0 represents top row)
DL = column of current cursor position (0 represents leftmost column)
CH = cursor type currently set
Bits 4-0 point to the start line for cursor within character cell
CL = bit values:
Bits 4-0 point to the end line for cursor within character cell

## Read Light Pen Position

Reads light pen position.

## Entry Conditions:

AH = 04H

## Exit Conditions:

AH = 0 light pen switch not activated
1 light pen values in registers
DH = row of current light pen position (0 represents top row)
DL = column of current light pen position (0 represents leftmost column)
CH = raster line (0-199) of current light pen position
BX = pixel column (0-319 or 0-639) of current light pen position

## Select Active Page

Select active display page (valid with color graphics adapter in alpha mode).

## Entry Conditions:

AH = 05H
AL = display page
(0 through 7 valid for video modes 0 and 1)
(0 through 3 valid for video modes 2 and 3)

## Scroll Up

Scroll active page up.

## Entry Conditions:

AH = 06H
AL = number of lines to scroll; this number of lines will be blank at the bottom of the window. (0 means blank entire window)
CH = row of upper left corner of scroll window
CL = column of upper left corner of scroll window
DH = row of lower right corner of scroll window
DL = column of lower right corner of scroll window
BH = attribute (alpha modes) or color (graphics modes) to be used on blank line

**Attributes:**

BH = attribute

Alpha modes (0, 1, 2, 3) and monochrome mode (7):

Bits 2, 1, 0 = foreground color (alpha)
In mono, 0 = black, 1 = underline, 7 = white.
Bit 3 = foreground intensity
Bits 6, 5, 4 = background color
In mono, 7 = white, other values = black.
Bit 7 = blink

Select foreground color 0 - 15 and background color 0 - 7 from background color list of Set Color Palette (AH = 11).

**Sample Attributes**

| Attribute | Alpha Modes | Mono Mode |
|---|---|---|
| 07H | White on Black | Normal Text |
| 0FH | Bright White on Black | High Intensity Text |
| 87H | Blinking White on Black | Blinking Text |
| 8FH | Blinking Bright White on Black | High Intensity Blinking Text |
| 70H | Black on White | Reverse Video |
| F0H | Black on Blinking White | Blinking Reverse Video |
| 01H | Blue on Black | Underline Text |
| 09H | Bright Blue on Black | High Intensity Underline Text |
| 00H | Black on Black | Invisible |

**Color (Graphics Mode):**

BH = color palette index

The color is selected from the current palette based on the color palette index. In Modes 4 and 5, BH can be 0-3. In Mode 6, BH can be 0 or 1. All unused bits are zero. See default palettes of Set Color Palette (AH = 11).

## Scroll Down

Scroll active page down.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 07H |
| AL | = | number of lines to scroll; this number of lines will be blank at the top of the window (0 means blank entire window) |
| CH | = | row of upper left corner of scroll window |
| CL | = | column of upper left corner of scroll window |
| DH | = | row of lower right corner of scroll window |
| DL | = | column of lower right corner of scroll window |
| BH | = | attribute (alpha modes) or color (graphics modes) to be used on a blank line |

See Scroll Up (AH = 06H) for attribute values and Set Color Palette (AH = 0BH) for color values.

## Read Attribute or Color/Character

Read a character and its attribute or color at the current cursor position.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 08H |
| BH | = | display page number (not used in graphics modes or with mono text adapter) |

## Exit Conditions:

| | | |
|---|---|---|
| AL | = | character read |
| AH | = | attribute or color of character (alpha modes only) |

## Write Attribute Or Color/Character

Write a character and its attribute or color at the current cursor position.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 09H |
| BH | = | display page number (not used in graphics modes) |
| CX | = | number of characters to write |
| AL | = | character to write |
| BL | = | attribute of character (for alpha modes) or color of character (for graphics modes). In graphics modes, Bit 7 of BL is set, the color of the character is XOR'ed with the currently displayed color value where the character will be printed. See Scroll Up (AH = 06H) for attribute values and Set Color Palette (AH = 0BH) for color values. |

## Write Character Only

Write character only at current cursor position.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 0AH |
| BH | = | display page number (valid for alpha modes only) |
| CX | = | number of characters to write |
| AL | = | character to write |
| BL | = | color of character (graphics modes only) |

## Set Color Palette

Select the color palette.

## Entry Conditions:

| | | | |
|---|---|---|---|
| AH | = | 0BH | |
| BH | = | 0 | Set background color to color value in BL. Color values are:<br>0 = black 8 = dark gray<br>1 = blue 9 = light blue<br>2 = green 10 = light green<br>3 = cyan 11 = light cyan<br>4 = red 12 = light red<br>5 = magenta 13 = light magenta<br>6 = yellow 14 = yellow<br>7 = gray 15 = white |
| BH | = | 1 | Set default palette to the number (0 or 1) in BL. |

In black and white modes:

| | | |
|---|---|---|
| BL | = | 0: 1 for white |
| BL | = | 1: 1 for black |

In 4 color graphics modes:

| | | |
|---|---|---|
| BL | = | 0 (1 = green/2 = red/3 = yellow) |
| BL | = | 1 (1 = cyan/2 = magenta/3 = white) |

In 16 color graphics modes:

(1 = blue/2 = green/3 = cyan/4 = red/5 = magenta/6 = yellow/7 = light gray/8 = dark gray/9 = light blue/10 = light green/11 = light cyan/12 = light red/13 = light magenta/14 = yellow/15 = white)

**Note:** For alpha modes, Palette Entry 0 indicates the border color. For graphics mode, Palette Entry 0 indicates the border and the background colors.

**Note:** Some colors may not appear the same on all monitors (e.g., yellow can appear brown).

## Write Dot

Write a pixel (dot).

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 0CH |
| DX | = | row number (0 to 199) |
| CX | = | column number (0 to 319 or 639) |
| AL | = | color value (When Bit 7 of AL is set, the resultant color value of the dot is the exclusive OR of the current position's dot color value and the value in AL.) |

## Read Dot

Read a pixel (dot).

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 0DH |
| DX | = | row number (0 to 199) |
| CX | = | column number (0 to 319 or 639) |

## Exit Conditions:

| | | |
|---|---|---|
| AL | = | color value of dot read |

## Write TTY

Write a character in teletype fashion. (Control characters are interpreted in the normal manner.)

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 0EH |
| AL | = | character to write |
| BL | = | foreground color (graphics mode) |

## Get CRT Mode

Get the current video mode.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 0FH |

## Exit Conditions:

| | | |
|---|---|---|
| AL | = | current video mode. See Set CRT Mode (AH = 00H) for values |
| AH | = | number of columns on screen |
| BH | = | current active display page |

## Write String

Write a string of characters.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 13H |
| ES:BP | = | pointer to the string of characters to be written |
| CX | = | number of characters in the string to display |
| DX | = | starting cursor position (DH = row, DL = column) |
| BH | = | page number (for alpha modes) |
| BL | = | attribute for characters (If attributes are not in the string, see below) |
| AL | 0 = | Cursor is not moved, string is characters only, attribute is in BL |
| | 1 = | Cursor is moved to the next character position after the last character written, string is characters only, attribute is in BL |
| | 2 = | Cursor is not moved, string has alternating characters and attributes |
| | 3 = | Cursor is moved to the next character position after the last character written, string has alternating characters and attributes |

# Equipment

This service returns the equipment flag (hardware configuration of the computer system) in the AX register.

**Software Interrupt:** 11 hex (17 dec)

The equipment flag returned in the AX register has the following meanings for each bit:

| | | |
|---|---|---|
| Reset = | the indicated equipment is not in the system | |
| Set = | the indicated equipment is in the system | |
| Bit 0 | diskette installed | |
| Bit 1 | math coprocessor | |
| Bit 3,2 | not used | |
| Bit 5,4 | initial video mode | |
| | 01 = | 40 x 25 BW on color graphics adapter |
| | 10 = | 80 x 25 BW on color graphics adapter |
| | 11 = | 80 x 25 BW on monochrome text adapter |
| Bit 7,6 | number of diskette drives (only if Bit 0 = 1) | |
| | 00 = | 1 |
| | 01 = | 2 |
| Bit 8 | not used | |
| Bit 11,10,9 | number of RS-232 cards | |
| Bit 12 | not used | |
| Bit 13 | not used | |
| Bit 15,14 | number of printers | |

## Memory Size

This service returns the total number of kilobytes of RAM in the computer system (contiguous starting from address 0) in the AX register. The maximum value returned is 640 (280 hex).

**Software Interrupt:** 12 hex (18 dec)

# Floppy Diskette Drive I/O Support

These routines provide a means to control diskette drive operation.

**Software Interrupt:** 13 hex (19 dec)

**Function Summary:**

| | | | |
|---|---|---|---|
| AH | = | 00H | Reset all disks |
| AH | = | 01H | Return status of last disk operation |
| AH | = | 02H | Read sectors from disk |
| AH | = | 03H | Write sectors to disk |
| AH | = | 04H | Verify sectors on disk |
| AH | = | 05H | Format track on disk |
| AH | = | 08H | Read drive parameters |
| AH | = | 15H | Read disk type |
| AH | = | 16H | Get diskette change line status |
| AH | = | 17H | Set diskette type for format |
| AH | = | 18H | Set media type for format |

**Function Descriptions:**

## Reset All Disks

Resets the floppy diskette system, reset associated hardware, and recalibrate all drives.

## Entry Conditions:

AH = 00H

## Exit Conditions:

See the following section, "Exits From All Floppy Disk Calls."

## Return Status of Last Diskette Operation

Return the status of the last diskette operation in AH.

## Entry Conditions:

AH = 01H
DL = 80H

## Exit Conditions:

See the following section, "Exits From All Floppy Disk Calls."

## Read Sectors From Disk

Read the specified sectors from disk into RAM.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 02H |
| DL | = | drive number (0-1) |
| DH | = | head number (0-1) |
| CH | = | track number (0-79) |
| CL | = | sector number (1-18) |
| AL | = | number of sectors to read (1-18) |
| ES:BX | = | pointer to disk buffer |

## Exit Conditions:

See the following section, "Exits From All Floppy Disk Calls."

## Write Sectors To Disk

Write the specified sectors from RAM to disk.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 03H |
| DL | = | drive number (0-1) |
| DH | = | head number (0-1) |
| CH | = | track number (0-79) |
| CL | = | sector number (1-18) |
| AL | = | number of sectors to write (1-18) |
| ES:BX | = | pointer to disk buffer |

## Exit Conditions:

See the following section, "Exits From All Floppy Disk Calls."

## Verify Sectors On Disk

Verify the specified sectors.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 04H |
| DL | = | drive number (0-1) |
| DH | = | head number (0-1) |
| CH | = | track number (0-79) |
| CL | = | sector number (1-18) |
| AL | = | number of sectors to verify (1-18) |

## Exit Conditions:

See the following section, "Exits From All Floppy Disk Calls."

## Format Track On Disk

Format the specified track.

**Note:** Function Call 23 must be performed before using this routine.

To format 360K diskettes, the gap length for format and end of track parameters of the Floppy Disk Parameter table (INT 1EH) must be changed. These parameters should be restored when formatting is complete.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 05H |
| DL | = | drive number (0-1) |
| DH | = | head number (0-1) |
| CH | = | track number (0-79) |
| AL | = | number of sectors per track (used only for DMA bound check) |
| ES:BX | = | pointer to sector format table consisting of four bytes per sector:<br>The first byte is the track number<br>The second byte is the head number<br>The third byte is the sector number<br>The fourth byte is the sector size code:<br>00 = 128 bytes/sector<br>01 = 256 bytes/sector<br>02 = 512 bytes/sector<br>03 = 1024 bytes/sector |

For Track 0, Head 1, on a nine-sector/track diskette formatted with an interleave of 1 (256 bytes/sector) the table would be:

00H,01H,01H,02H, 00H,01H,02H,02H, 00H,01H,03H,02H
00H,01H,04H,02H, 00H,01H,05H,02H, 00H,01H,06H,02H
00H,01H,07H,02H, 00H,01H,08H,02H, 00H,01H,09H,02H

## Exit Conditions:

See the following section, "Exits From All Floppy Disk Calls."

# Read Drive Parameters

Read parameter table for the selected drive.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 08H |
| DL | = | drive number (0-1) |

## Exit Conditions:

| | | |
|---|---|---|
| ES:DI | = | Floppy Disk Parameter table |
| CH | = | maximum number of tracks (low 8 bits of 10-bit value) |
| CL | = | Bits 7-6: Maximum number of tracks (high 2 bits of 10-bit value)<br>Bits 5-0: Maximum sectors per track |
| DH | = | maximum head number |
| DL | = | number of disk drives installed |
| BH | = | 0 |
| BL | = | Bits 7-4: 0<br>Bits 3-3: Drive type value in CMOS:<br>0 Drive type known but CMOS type is invalid, CMOS is not present, CMOS battery discharged or CMOS checksum invalid<br>1 360K, 5-1/4", 40 track<br>2 1.2 Mb, 5-1/4", 80 track<br>3 720K, 3-1/2", 80 track<br>4 1.44 Mb, 3-1/2", 80 track |

## Read Disk Type

Return the disk type.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 15H |
| DL | = | drive number (0-1) |

## Exit Conditions:

| | | |
|---|---|---|
| [C] | = | Error (possibly no drive installed) |
| [NC] | = | Operation successful. Status in AH |
| AH | 0 | = not present |
| | 1 | = diskette with no change line |
| | 2 | = diskette with change line |
| | 3 | = hard disk |

## Get Disk Change Line Status

Test to see if diskette has changed.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 16H |
| DL | = | drive number (0-1) |

## Exit Conditions:

| | | |
|---|---|---|
| AH | 00 = | [NC] diskette has not changed |
| | 06 = | [C] diskette has changed |

Also, see the following section called "Exits From All Floppy Disk Calls."

## Set Disk Type For Format

Set the diskette type for the next FORMAT command.

## Entry Conditions:

| | | | |
|---|---|---|---|
| AH | = | 17H | |
| AL | | 00 = | not used |
| | | 01 = | 360K media in a 360K drive |
| | | 02 = | 360K media in a 1.2M drive |
| | | 03 = | 1.2M media in a 1.2M drive, or 1.44M media in a 1.44M drive |
| | | 04 = | 720K disk in 720K drive |
| DL | = | drive number (0-1) | |

## Exit Conditions:

See the following section, "Exits From All Floppy Disk Calls."

## Set Media Type for Format

Set the media type for the selected drive.

## Entry Conditions:

| | | | |
|---|---|---|---|
| AH | = | 18H | |
| DL | = | drive number (0-1) | |
| CH | = | number of tracks (low 8 bits of 10-bit value) | |
| CL | = | Bits 7-6: | Number of tracks (high 2 bits of 10-bit value) |
| | | Bits 5-0: | Sectors per track |

## Exit Conditions:

| | | |
|---|---|---|
| ES:DI | = | Floppy Disk Parameter table |

Also, see the following section, "Exits From All Floppy Disk Calls."

## Exits From All Floppy Disk Calls

| | | | |
|---|---|---|---|
| [NC] | = | operation was successful (AH = 00H) | |
| [C] | = | operation failed | |
| AH | | 01H = | Bad command or parameter |
| | | 02H = | Address mark not found |
| | | 03H = | Write protected |
| | | 04H = | Sector not found |
| | | 06H = | Diskette has changed |
| | | 08H = | DMA overrun error |
| | | 09H = | DMA boundary error |
| | | 10H = | Bad CRC on disk read |
| | | 20H = | Controller failed |
| | | 40H = | Seek failed |
| | | 80H = | Device timeout |

# Floppy Disk Parameter Pointer

This is a double word pointer to the current floppy disk parameter block.

**Software Interrupt:** 1E hex (30 dec)

To change the way the floppy disk driver operates, build another parameter block and load the segment and offset of this parameter block into the software interrupt 1E hex vector area.

The layout of the Floppy Disk Parameter table is:

| Offset | Length | Description |
|---|---|---|
| 0 | 1 byte | First specify byte |
| 1 | 1 byte | Second specify byte |
| 2 | 1 byte | Number of ticks to wait before turning disk drive motor off |
| 3 | 1 byte | Number of bytes per sector:<br>0 = 128 bytes per sector<br>1 = 256 bytes per sector<br>2 = 512 bytes per sector<br>3 = 1024 bytes per sector |
| 4 | 1 byte | Sectors per track |
| 5 | 1 byte | Gap length |
| 6 | 1 byte | Data transfer length |
| 7 | 1 byte | Gap length for format |
| 8 | 1 byte | Fill byte for format |
| 9 | 1 byte | Head settle time (milliseconds) |
| 10 | 1 byte | Motor startup time (increments of 1/8 second) |

## Hard Disk Support

The following routines provide access to Hard Disk operations.

**Software Interrupt:** 13 hex (19 dec)

**Function Summary:**

| | | | |
|---|---|---|---|
| AH | = | 00H | Reset all disks |
| AH | = | 01H | Return status of last disk operation |
| AH | = | 02H | Read sectors from disk |
| AH | = | 03H | Write sectors to disk |
| AH | = | 04H | Verify sectors on disk |
| AH | = | 05H | Format track on disk |
| AH | = | 06H | Unused |
| AH | = | 07H | Unused |
| AH | = | 08H | Return current hard disk parameters |
| AH | = | 09H | Initialize hard disk parameters |
| AH | = | 0AH | Read long |
| AH | = | 0BH | Write long |
| AH | = | 0CH | Perform seek on hard disk |
| AH | = | 0DH | Reset hard disk |
| AH | = | 0EH | Unused |
| AH | = | 0FH | Unused |
| AH | = | 10H | Test for hard disk ready |
| AH | = | 11H | Recalibrate hard disk |
| AH | = | 12H | Unused |
| AH | = | 13H | Unused |
| AH | = | 14H | Controller internal diagnostic |
| AH | = | 15H | Read disk type |

## Reset Hard Disks

Reset the hard disk system. Reset associated hardware, and recalibrate all drives.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 00H |
| DL | = | drive number (80H-81H) |

## Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

## Return Status of Last Hard Disk Operation

Return the status of the last hard disk operation in AL.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 01H |
| DL | = | 80H |

## Exit Conditions:

| | | |
|---|---|---|
| AL | = | status of the last operation. See the following section, "Exits From All Hard Disk Calls," for values. |

## Read Sectors From Disk

Read the specified sectors from disk into RAM.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 02H |
| DL | = | drive number (80H-81H) |
| DH | = | head number (0-15) |
| CH | = | least significant part of cylinder number (0-1023) (See CL Bits 7, 6) |
| CL Bits 7, 6 | = | most significant part of cylinder number |
| CL Bits 5-0 | = | sector number (1-17) |
| AL | = | number of sectors to read (1-80H) |
| ES:BX | = | pointer to disk buffer |

## Exit Conditions:

See the following section named "Exits From All Hard Disk Calls."

## Write Sectors To Disk

Write the specified sectors from RAM to disk.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 03H |
| DL | = | drive number (80H-81H) |
| DH | = | head number (0-15) |
| CH | = | least significant part of cylinder number (0-1023) (See CL Bits 7, 6) |
| CL Bits 7, 6 | = | most significant part of cylinder number |
| CL Bits 5-0 | = | sector number (1-17) |
| AL | = | number of sectors to write (1-80 hex) |
| ES:BX | = | pointer to disk buffer |

## Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

## Verify Sectors On Disk

Verify the specified sectors.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 04H |
| DL | = | drive number (80H-81H) |
| DH | = | head number (0-15) |
| CH | = | least significant part of cylinder number (0-1023) (See CL Bits 7, 6) |
| CL Bits 7, 6 | = | most significant part of cylinder number |
| CL Bits 5-0 | = | sector number (1-17) |
| AL | = | number of sectors to verify (1-80 hex) |

## Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

## Format Track On Disk

Format the specified track.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 05H |
| DL | = | drive number (80H-81H) |
| DH | = | head number (0-15) |
| CH | = | least significant part of cylinder number (0-1023) (See CL Bits 7, 6) |
| CL Bits 7, 6 | = | most significant part of cylinder number |
| ES:BX | = | pointer to sector format table consisting of two bytes for each sector. The first byte is 00 for a good sector, and 80H for a bad sector. The second byte is the sector number. For a 17-sector track with an interleave of 2, the table is: |

00H,01H, 00H,0AH, 00H,02H, 00H,0BH, 00H,03H, 00H,0CH, 00H,04H, 00H,0DH, 00H,05H, 00H,0EH, 00H,06H, 00H,0FH, 00H,07H, 00H,10H, 00H,08H, 00H,11H, 00H,09H

## Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

## Return Current Hard Disk Parameters

Return the current parameter values for the specified hard disk.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 08H |
| DL | = | drive number (80H-81H) |

## Exit Conditions:

| | | |
|---|---|---|
| DL | = | number of hard disk drives attached |
| DH | = | maximum usable value for head number |
| CH | = | least significant part of maximum usable value for cylinder number |
| CL Bits 7, 6 | = | most significant part of maximum usable value for cylinder number |
| CL Bits 5-0 | = | maximum usable value for sector number |

See also the following section, "Exits From All Hard Disk Calls."

## Initialize Hard Disk Parameters

Initialize the hard disk parameters for the specified hard disk. The values are taken from the current drive parameter table pointed to by INT 41H for Drive 80H, and INT 46H for Drive 81H.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 09H |
| DL | = | drive number (80H-81H) |

## Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

## Read Long

Read specified sectors and four ECC bytes per sector from disk to RAM.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 0AH |
| DL | = | drive number (80H-81H) |
| DH | = | head number (0-15) |
| CH | = | least significant part of cylinder number (0-1023). (See CL Bits 7, 6) |
| CL Bits 7, 6 | = | most significant part of cylinder number |
| CL Bits 5-0 | = | sector number (1 -17) |
| AL | = | number of sectors to read (1-79 hex) |
| ES:BX | = | pointer to disk buffer |

## Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

## Write Long

Write specified sectors plus four ECC bytes per sector from RAM to disk.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 0BH |
| DL | = | drive number (80H-81H) |
| DH | = | head number (0-15) |
| CH | = | least significant part of cylinder number (0-1023). (See CL Bits 7, 6) |
| CL Bits 7, 6 | = | most significant part of cylinder number |
| CL Bits 5-0 | = | sector number (1 -17) |
| AL | = | number of sectors to write (1-79 hex) |
| ES:BX | = | pointer to disk buffer |

## Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

## Perform Seek On Hard Disk

Seek to the specified hard disk track.

## Entry Conditions

| | | |
|---|---|---|
| AH | = | 0CH |
| DL | = | drive number (80H-81H) |
| DH | = | head number (0-15) |
| CH | = | least significant part of cylinder number (0-1023). (See CL Bits 7, 6) |
| CL Bits 7, 6 | = | most significant part of cylinder number |
| ES:BX | = | pointer to disk buffer |

## Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

## Reset Hard Disk

Reset the hard disk system. Reset associated hardware, and recalibrate all hard disk drives.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 0DH |
| DL | = | drive number (80H-81H) |

## Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

## Test For Hard Disk Ready

Check to see if the specified hard disk drive is ready.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 10H |
| DL | = | drive number (80H-81H) |

## Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

## Recalibrate Hard Disk

Recalibrate the specified hard disk drive.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 11H |
| DL | = | drive number (80H-81H) |

## Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

## Controller Internal Diagnostic

Perform internal diagnostic on the hard disk controller.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 14H |
| DL | = | drive number (80H-81H) |

## Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

## Read Disk Type

Return the disk type and the number of sectors available on the hard disk.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 15H |
| DL | = | drive number (80H-81H) |

## Exit Conditions:

| | | | |
|---|---|---|---|
| AH | 0 | = | Not present |
| | 3 | = | Hard disk drive |
| CX:DX | = | | Number of sectors available on the hard disk. (Assumes 512 byte sectors) |

### Exits From All Hard Disk Calls

| | | |
|---|---|---|
| [NC] | | = operation was successful (AH = 00H) |
| [C] | | = operation failed |
| AH | 01H | = Bad command or parameter |
| | 02H | = Address mark not found |
| | 03H | = Write protect error |
| | 04H | = Sector not found |
| | 05H | = Reset failed |
| | 07H | = Drive parameter command failed |
| | 08H | = DMA overrun |
| | 09H | = DMA boundary error |
| | 0AH | = Bad sector flag detected |
| | 0BH | = Bad cylinder detected |
| | 0DH | = Invalid number of sectors on format |
| | 0EH | = Control data address mark detected |
| | 0FH | = DMA arbitration level out of range |
| | 10H | = Bad ECC on disk read |
| | 11H | = Data corrected during read |
| | 20H | = Controller failed |
| | 40H | = Seek failed |
| | 80H | = Device timeout |
| | AAH | = Drive not ready |
| | BBH | = Undefined error occurred |
| | CCH | = Write error |

## Hard Disk Parameter Pointer

This is a double word pointer to the hard disk parameter block.

**Software Interrupt:** 41 hex (65 dec) for hard disk 0

**Software Interrupt:** 46 hex (70 dec) for hard disk 1

Characteristics of the hard disk is stored in the Hard Disk Parameter table. To read the values, load the segment and offset stored at the appropriate software interrupt vector area. For hard disk 0, use interrupt 41 hex; for hard disk 1, use interrupt 46 hex.

The layout of the Hard Disk Parameter table is:

| Offset | Length | Description |
|---|---|---|
| 0 | 2 bytes | Maximum number of cylinders |
| 2 | 1 byte | Maximum number of heads |
| 3 | 2 bytes | Not used |
| 5 | 2 bytes | Starting Write Precompensation Cylinder |
| 7 | 1 byte | Not used |
| 8 | 1 byte | Control byte: |
| | | Bit 7: Disable retries |
| | | -or- |
| | | Bit 6: Disable retries |
| | | Bit 5: Defect Map Present at Maximum Cylinders + 1 |
| | | Bit 3: More than 8 heads |
| 9 | 1 byte | Not used |
| 10 | 1 byte | Not used |
| 11 | 1 byte | Not used |
| 12 | 2 bytes | Landing zone |
| 14 | 2 bytes | Sectors per track |
| 15 | 1 byte | Reserved |

# Serial Communications

These routines provide asynchronous byte stream I/O to and from the RS-232C serial communications port.

**Software Interrupt:** 14 hex (20 dec)

**Function Summary:**

| | | | |
|---|---|---|---|
| AH | = | 00H | Initialize comm port |
| AH | = | 01H | Transmit character |
| AH | = | 02H | Receive character |
| AH | = | 03H | Get current comm status |
| DX | = | Communications port number (0 or 1) | |

**Function Descriptions:**

## Initialize Comm Port

Initialize the communication port according to the parameters in AL and DX.

## Entry Conditions:

| | | |
|---|---|---|
| DX | = | Communications port number (0 or 1) |
| AL | = | RS-232C parameters, as follows: |
| AH | = | 00H |

| 7 6 5 | 4 3 | 2 | 1 0 |
|---|---|---|---|
| Baud Rate | Parity | Stop Bits | Word Length |

| | | | |
|---|---|---|---|
| 000 = 110 baud | x0 = none | 0 = 1 bit | 10 = 7 bits |
| 001 = 150 baud | 01 = odd | 1 = 2 bits | 11 = 8 bits |
| 010 = 300 baud | 11 = even | | |
| 011 = 600 baud | | | |
| 100 = 1200 baud | | | |
| 101 = 2400 baud | | | |
| 110 = 4800 baud | | | |
| 111 = 9600 baud | | | |

## Exit Conditions:

| | | |
|---|---|---|
| AX | = | RS-232 status; see "Get Current Comm Status" (AH = 03H) |

## Transmit Character

Transmit (output) the character in AL

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 01H |
| AL | = | character to transmit |
| DX | = | port number (0 or 1) |

## Exit Conditions:

| | | |
|---|---|---|
| AH | = | RS-232 status; see "Get Current Comm Status (AH = 03H). If Bit 7 is set, the routine is unable to transmit the character because of a timeout error. |

AL is preserved.

## Receive Character

Receive (input) a character in AL (wait for a character, if necessary). On exit, AH contains the RS-232 status, except that only the error bits (1, 2, 3, 4, 7) can be set; the timeout Bit (7), if set, indicates that data set ready was not received. Thus, AH is nonzero only when an error occurs. If bit 7 is set, the other bit values are not meaningful.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 02H |
| DX | = | port number (0 or 1) |

## Exit Conditions:

| | | |
|---|---|---|
| AL | = | character received |
| AH | = | RS-232 status; see "Get Current Comm Status" (AH = 03H) |

## Get Current Comm Status

Read the communication status in AX.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 03H |
| DX | = | port number (0 or 1) |

## Exit Conditions:

| | | |
|---|---|---|
| AH | = | RS-232 status, as follows (set = true): |
| | | Bit 0 = data ready |
| | | Bit 1 = overrun error |
| | | Bit 2 = parity error |
| | | Bit 3 = framing error |
| | | Bit 4 = break detect |
| | | Bit 5 = transmitter holding register empty |
| | | Bit 6 = transmitter shift register empty |
| | | Bit 7 = timeout occurred |
| AL | = | modem status, as follows (set = true): |
| | | Bit 0 = delta clear to send |
| | | Bit 1 = delta data set ready |
| | | Bit 2 = trailing edge ring detector |
| | | Bit 3 = delta receive line signal detect |
| | | Bit 4 = clear to send |
| | | Bit 5 = data set ready |
| | | Bit 6 = ring indicator |
| | | Bit 7 = receive line signal detect |

# Multi-Tasking Support

Hooks, Joystick Support, Microsecond Delay, 80286 Virtual Mode Support, Extended Memory Support.

**Software Interrupt:** 15 hex (21 dec)

**Function Summary:**

| | | |
|---|---|---|
| AH | = 80H | Device Open |
| AH | = 81H | Device Close |
| AH | = 82H | Program Terminate |
| AH | = 83H | Event Wait |
| AH | = 84H | Joystick Support |
| AH | = 85H | System Request Key Support |
| AH | = 86H | Wait |
| AH | = 87H | Move Block of Memory |
| AH | = 88H | Extended Memory Size |
| AH | = 89H | Processor to Virtual Mode |
| AH | = 90H | Device Busy Wait Loop |
| AH | = 91H | Interrupt Complete |
| AH | = C0H | System Configuration Parameters |

**Function Descriptions:**

## Device Open
## Entry Conditions:

AH = 80H
BX = Device ID
CX = Process ID

**Exit Conditions:** None

## Device Close
## Entry Conditions:

AH = 81H
BX = Device ID
CX = Process ID

**Exit Conditions:** None

## Program Terminate
## Entry Conditions:

AH = 82H
BX = Device ID

**Exit Conditions:** None

## Event Wait
## Entry Conditions:

| | | |
|---|---|---|
| AH = 83H | | |
| AL = 0 | | Set interval |
| ES:BX | = | Pointer to a byte in caller's memory that has the sign bit set after the time interval expires |
| CX,DX | = | The number of microseconds to elapse before the high order byte in the caller's memory pointed to by ES:BX is set. Granularity is 976 microseconds |
| AL = 1 | | Cancel event wait |

**Exit Conditions:** None

## Joystick Support
## Entry Conditions:

| | |
|---|---|
| AH = 84H | |
| DX = 0 | Read the current joystick button setting. On return, AL contains the button settings in Bits 4-7 |
| Bit 4: | Joystick A, Button 1 |
| Bit 5: | Joystick A, Button 2 |
| Bit 6: | Joystick A, Button 1 |
| Bit 7: | Joystick B, Button 2 |
| DX = 1 | Read the resistive inputs of the game adapter. The following values are returned: |
| | AX = Joystick A x value |
| | BX = Joystick A y value |
| | CX = Joystick B x value |
| | DX = Joystick B y value |

## System Request Key Support
## Entry Conditions:

AH = 85H

## Exit Conditions:

| | | |
|---|---|---|
| AL | = 0 | Sys Req key pressed |
| AL | = 1 | Sys Req key released |

## Wait

Wait indicated number of microseconds.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = 86H | Wait indicated number of microseconds |
| CX,DX | = | Number of microseconds to wait before returning. Granularity is 976 microseconds |

## Exit Conditions:

| | | |
|---|---|---|
| [C] | = | Successful wait |
| [NC] | = | Wait function already in progress |

## Move Block of Memory

Transfers the contents of a block of memory from memory addressed above 1024K to memory addressed below 1024K. This uses the 80286 processor "protected" mode.

## Entry Conditions:

AH = 87H

ES:SI = A pointer to a Global Descriptor Table (GDT) as defined in the following table. The calling program must have previously set up this table

CX = Number of 16-bit words to be transferred. The source and destination global descriptors must contain a length field of at least (2 * CX - 1)

| GDT: | Descriptor | Usage (each entry is 8 bytes) |
|---|---|---|
| | 0 | Dummy |
| | 1 | Segment address of this GDT |
| | 2 | Pointer to area from which to move data |
| | 3 | Pointer to segment to receive the data |
| | 4 | BIOS code segment descriptor |
| | 5 | BIOS stack segment descriptor |

## Exit Conditions:

AH = 0 Operation successful
AH = 1 RAM parity error
AH = 2 Exception interrupt occurred
AH = 3 Gating of address line 20H failed
Carry flag set if error
Zero flag set if successful

## Extended Memory Size

Returns the amount of extended memory starting at address 1024K.

## Entry Conditions:

AH = 88H

## Exit Conditions:

AX = Amount of contiguous available memory in kilobytes starting at address 1024K

## Processor to Virtual Mode

Set the 80286 processor into protected virtual memory mode.

## Entry Conditions:

AH = 89H

ES:SI = Pointer to a Global Descriptor Table (GDT) set up by the calling program as defined in the following table

BH = Offset within the Interrupt Descriptor Table (IDT) that contains the first eight interrupts

BL = Offset within the Interrupt Descriptor Table that contains the second eight hardware interrupts

| GDT: | Descriptor | Usage (each entry is 8 bytes) |
|---|---|---|
| | 0 | Dummy |
| | 1 | Segment address of this GDT |
| | 2 | Pointer to the IDT |
| | 3 | Pointer to user's data segment |
| | 4 | Pointer to user's extra segment |
| | 5 | Pointer to user's stack segment |
| | 6 | Pointer to user's code segment |
| | 7 | Pointer to BIOS code segment |

## Exit Conditions:

AH = 0 Operation successful

**Note:** All segment registers are changed, AX and BP registers modified.

## Device Busy Wait Loop
## Entry Conditions:

| | | | | |
|---|---|---|---|---|
| AH | = | 90H | | |
| AL | = | Type code groups | | |
| | | 00H - 7FH | = | Non re-entrant devices |
| | | 80H - BFH | = | Re-entrant devices. ES:BX points to data block |
| | | C0H - FFH | = | Wait only |

**Exit Conditions:** None

## Interrupt Complete
## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 91H |
| AL | = | Type code (See function AH = 90H) |

**Exit Conditions:** None

## System Configuration Parameters

Returns pointer to system description vector in ROM.

## Entry Conditions:

AH = C0H

## Exit Conditions:

AH = 00H
ES:BX = Pointer to system descriptor vector

System Descriptor:

| Offset | Length | Description |
|---|---|---|
| 0 | 2 bytes | Byte count of data the follows; minimum length is 8 |
| 2 | 1 byte | Model byte |
| 3 | 1 byte | Sub-Model byte |
| 4 | 1 byte | BIOS revision level (00 is first release) |
| 5 | 1 byte | Feature information byte 1:<br>Bit 7: Hard Disk BIOS uses DMA channel 3<br>Bit 6: 2nd interrupt chip present<br>Bit 5: Real-time clock present<br>Bit 4: Keyboard intercept sequence (INT 15H) called in keyboard interrupt (INT 09H)<br>Bit 3: Wait for external event supported<br>Bit 2: Extended BIOS area is allocated<br>Bit 1: Micro Channel implemented<br>Bit 0: Reserved |
| 6 | 4 bytes | Feature information byte 2-5 - reserved |

# Keyboard

The following routines provide access to keyboard functions.

**Software Interrupt:** 16 hex (22 dec)

**Function Summary:**

| | | |
|---|---|---|
| AH = | 00H | Read Keyboard Input |
| AH = | 01H | Read Keyboard Status |
| AH = | 02H | Read Shift Status |
| AH = | 03H | Set Typematic Rate |
| AH = | 05H | Stuff Keyboard Buffer |
| AH = | 10H | Read Extended Keyboard Input |
| AH = | 11H | Read Extended Keyboard Status |
| AH = | 12H | Read Extended Shift Status |

**Function Descriptions:**

# Read Keyboard

Read the next character typed at the keyboard. Return the ASCII value of the character and the keyboard scan code, removing the entry from the keyboard buffer (destructive read). Control returns when a keystroke is available.

# Entry Conditions:

AH = 00H

# Exit Conditions:

AL = ASCII value of character
AH = keyboard scan code

## Scan Keyboard

Set up the zero flag (Z flag) to indicate whether a character is available to be read from the keyboard or not. If a character is available, return the ASCII value of the character and the keyboard scan code. The entry remains in the keyboard buffer (non-destructive read).

## Entry Conditions:

AH = 01H

## Exit Conditions:

| | | |
|---|---|---|
| Z = | 1 | no character is available |
| Z = | 0 | a character is available, in which case:<br>AL = ASCII value of character<br>AH = keyboard scan code |

## Get Shift Status

Return the current shift status.

## Entry Conditions:

AH = 02H

## Exit Conditions:

AL = current shift status (bit settings: set = true, reset = false)

- Bit 0 = RIGHT SHIFT key pressed
- Bit 1 = LEFT SHIFT key pressed
- Bit 2 = CTRL (control) key pressed
- Bit 3 = ALT (alternate mode) key pressed
- Bit 4 = SCROLL state active
- Bit 5 = NUMBER lock engaged
- Bit 6 = CAPS lock engaged
- Bit 7 = INSERT state active

## Set Typematic Rate
## Entry Conditions:

AH = 03H
AL = 05H
BL = Typematic rate (00 - 1F hex)
BH = Typematic delay (00 - 3 hex)

## Exit Conditions: None

## Stuff Keyboard Buffer
## Entry Conditions:

AH = 05H
CH = Scan Code to Place in Keyboard Buffer
CL = ASCII Character to Place in Keyboard Buffer

## Exit Conditions:

AL = 0 Store is Successful
AL = 1 Store is Unsuccessful
CY = 1 Error

## Read Extended Keyboard Input

Control is returned when a keystroke is available. The keystroke is removed from the buffer.

## Entry Conditions:

AH = 10H

## Exit Conditions:

AL = ASCII Character
AH = Scan Code

## Read Extended Keyboard Status

Includes extended read interface for extended keyboard.

## Entry Conditions:

AH = 11H

## Exit Conditions:

| | | |
|---|---|---|
| Z | = 1 | No Character Available |
| Z | = 0 | Character Available, in which case: |
| | | AL = ASCII Character |
| | | AH = Scan Code |

**Note:** The keystroke is not removed from the buffer.

## Read Extended Shift Status
## Entry Conditions:

AH = 12H

## Exit Conditions:

AL = Shift Status Byte — Bit = true, (on or depressed)
— Bit = false (or off)

Bit 0 = Right Shift key
Bit 1 = Left Shift key
Bit 2 = Ctrl (control) key
Bit 3 = Alt (alternate mode) key
Bit 4 = Scroll Lock
Bit 5 = Num Lock
Bit 6 = Caps Lock
Bit 7 = Ins(ert)

AH = Extended Shift Status —
Bit = 1 — currently depressed
Bit = 0 — not currently depressed

Bit 0 = Left Ctrl key
Bit 1 = Left Alt key
Bit 2 = Right Ctrl key
Bit 3 = Right Alt key
Bit 4 = Scroll Lock key
Bit 5 = Num Lock key
Bit 6 = Caps Lock key
Bit 7 = SysRq key

## Line Printer

These routines provide an interface to the parallel line printer.

**Software Interrupt:** 17 hex (23 dec)

**Function Summary:**

| | | | |
|---|---|---|---|
| AH | = | 00H | Print character |
| AH | = | 01H | Initialize printer port |
| AH | = | 02H | Get current printer status |

**Function Descriptions:**

## Print Character

Print a character.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 00H |
| AL | = | character to be printed |
| DX | = | printer to be used (0-2) |

## Exit Conditions:

| | | |
|---|---|---|
| AH | = | printer status; See the following section "Get Current Printer Status (AH = 02H). If Bit 0 is set, the character could not be printed because of a timeout error |

## Initialize Printer Port

Initialize the printer port.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 01H |
| DX | = | printer to be used (0-2) |

## Exit Conditions:

AH = printer status; See the following section "Get Current Printer Status" (AH = 02H)

## Get Current Printer Status

Read the printer status in AH.

## Entry Conditions:

AH = 02H

## Exit Conditions:

AH = printer status, as follows (set = true):

Bit 0 = timeout occurred
Bit 1 = [unused]
Bit 2 = [unused]
Bit 3 = I/O error
Bit 4 = selected
Bit 5 = out of paper
Bit 6 = acknowledge
Bit 7 = not busy

(Note: If printer port specified by DX does not exist, the status value is not meaningful.)

# System Clock

These routines provide the means of reading and setting the system clock tick counter, the CMOS real-time clock, and the system alarm function.

**Software Interrupt:** 1A hex (26 dec)

**Function Summary:**

| | | |
|---|---|---|
| AH = | 00H | Read system clock |
| AH = | 01H | Set system clock |
| AH = | 02H | Read CMOS time of day |
| AH = | 03H | Set CMOS time of day |
| AH = | 04H | Read CMOS date |
| AH = | 05H | Set CMOS date |
| AH = | 06H | Set the alarm |
| AH = | 07H | Reset the alarm |
| AL = | 80H | Set up sound multiplexer |

**Function Descriptions:**

# Read System Clock

Read the system clock value kept in RAM.

**Note:** The clock runs at a rate of 1,193,180/65,536 per second. (About 18.2 ticks per second.) 24 hours equals 1800BOH ticks.

# Entry Conditions:

AH = 00H

# Exit Conditions:

| | | |
|---|---|---|
| AL | = | If the timer has not exceeded 24 hours since the last time this function was called, AL contains 0, otherwise it contains a non-zero value |
| CX | = | high (most significant) portion of clock count |
| DX | = | low (least significant) portion of clock count |

## Set System Clock

Set the system clock value kept in RAM.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 01H |
| CX | = | high (most significant) portion of clock count |
| DX | = | low (least significant) portion of clock count |

## Read CMOS Time Of Day

Read the time of day kept in CMOS.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 02H |

## Exit Conditions:

| | | |
|---|---|---|
| CH | = | hours in BCD |
| CL | = | minutes in BCD |
| DH | = | seconds in BCD |
| DL | = | daylight savings time (1 = yes, 0 = no) |

## Set CMOS Time Of Day

Set the time of day kept in CMOS.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 03H |
| CH | = | hours in BCD |
| CL | = | minutes in BCD |
| DH | = | seconds in BCD |
| DL | = | If daylight savings time, 1. Otherwise 0 |

## Read CMOS Date

Read the date kept in CMOS

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 04H |

## Exit Conditions:

| | | |
|---|---|---|
| CH | = | century in BCD |
| CL | = | year in BCD |
| DH | = | month in BCD |
| DL | = | day in BCD |

## Set CMOS Date

Set the date kept in CMOS

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 05H |
| CH | = | century in BCD |
| CL | = | year in BCD |
| DH | = | month in BCD |
| DL | = | day in BCD |

## Set The Alarm

Set the alarm function to generate an INT 4AH at the specified time. The user must provide an alarm routine and initialize the vector for interrupt 4AH to point to this routine.

## Entry Conditions:

| | | |
|---|---|---|
| AH | = | 06H |
| CH | = | hours in BCD |
| CL | = | minutes in BCD |
| DH | = | seconds in BCD |

## Exit Conditions:

| | | |
|---|---|---|
| [NC] | = | CMOS clock operating correctly, and no other alarm is currently in process |
| [C] | = | An alarm is currently in progress, or the CMOS clock is not operating correctly |

## Reset The Alarm

Reset the alarm function set by Function 6.

## Entry Conditions:

AH = 07H

## Exit Conditions: None

# MS-DOS Memory Map

## High-Level Memory Map

| HEX ADDRESS 0-16 MEG | DESCRIPTION |
|---|---|
| 000000 | Interrupt Vector Table (INTs 00h - FFh) |
| 000400 | ROM BIOS Data Area |
| 000500 | MS-DOS & BASIC Data Area |
| 000600 | RESERVED |
| 000700 | MS-DOS interface drivers to ROM BIOS I/O routines (IBMBIO.COM) |
| Note 1 | MS-DOS interrupt handler service routines (INT 21h functions) |
| Note 1 | MS-DOS structures, buffers, stack space and installable device drivers |
| Note 1 | Resident portion of command interpreter (COMMAND. COM), Interrupt handlers for INT 22h (terminate), INT 23h (Control-Break), INT 24h (Critical Error) and code to reload the transient portion of COMMAND.COM. |
| Note 1 | Transient Program Area. Used by external commands and utilities. |
| Note 1 | Transient portion of COMMAND.COM Command interpreter, internal commands, batch processor, external command loader. |
| Note 2 | End of conventional RAM |
| 0A0000 | RESERVED for EGA type display buffer |
| 0B0000 | RESERVED for MDPA type display buffer |
| 0B8000 | RESERVED for CGA type display buffer |
| 0C0000 | RESERVED for ROM BIOS extensions on I/O adapters |
| 0F8000 | ROM BIOS Initialization Diagnostic Routines |
| 100000 | Extended (upper Meg) RAM |
| FF8000 | Duplicated code assignment of addresses 0F8000-0FFFFF |

**Notes:**

1 These addresses are not absolute as they depend on the hardware installed and/or the software driver configuration. But the relative order of these items is preserved.

2 The Transient Program Area extends to all of the conventional RAM installed. Maximum of 640K.

# Interrupt Vector Table

| HEX ADDRESS SEQ. OFFSET | INTERRUPT NUMBER | DESCRIPTION |
|---|---|---|
| 0:0 | 00 | Divide by zero (CPU generated) |
| 0:4 | 01 | Single Step (CPU generated) |
| 0:8 | 02 | Non-Maskable Interrupt (H/W generated) |
| 0:C | 03 | Softare Break Point Interrupt |
| 0:10 | 04 | Arithmetic Overflow (CPU generated) |
| 0:14 | 05 | Print Screen |
| 0:18 | 06 | Invalid Op-code Exception (CPU generated) |
| 0:1C | 07 | Processor Extension not available Exception (CPU generated) |
| 0:20 | 08 | Timer Clock Tick (H/W generated IRQ0) |
| 0:24 | 09 | Keyboard (H/W generated IRQ1) |
| 0:28 | 0A | I/O Channel available (H/W generated IRQ9) re-directed from Slave Interrupt Controller |
| 0:30 | 0B | I/O Channel available, usually secondary serial communications (H/W generated IRQ3) |
| 0:34 | 0C | I/O Channel available, usually primary serial communications (H/W generated IRQ4) |
| 0:2C | 0D | I/O Channel available (H/W generated IRQ5) hard disk |
| 0:38 | 0E | Floppy Disk (H/W generated IRQ6) |
| 0:3C | 0F | Printer (H/W generated IRQ7) |
| 0:40 | 10 | Video BIOS I/O Call |
| 0:44 | 11 | BIOS Equipment Check I/O Call |
| 0:48 | 12 | BIOS Memory Size I/O Call |
| 0:4C | 13 | Diskette and Hard Disk BIOS I/O Call |
| 0:50 | 14 | RS-232 Communications BIOS I/O Call |
| 0:54 | 15 | I/O Systems BIOS Extension Call |
| 0:58 | 16 | Keyboard BIOS I/O Call |
| 0:5C | 17 | Printer BIOS I/O Call |
| 0:60 | 18 | Boot Stap Loader Failure Hook |
| 0:64 | 19 | Boot Strap Loader |
| 0:68 | 1A | Time Date BIOS I/O Call |
| 0:6C | 1B | Keyboard Control-Break Hook |
| 0:70 | 1C | Timer Clock Tick Hook |
| 0:74 | 1D | Video Display Parameters Pointer |
| 0:78 | 1E | Floppy Diskette Parameters Pointer |
| 0:7C | 1F | Video Graphics Characters Pointer (Characters 128-255 only) |

# Interrupt Vector Table

| HEX ADDRESS SEQ. OFFSET | INTERRUPT NUMBER | DESCRIPTION |
|---|---|---|
| 0:80 | 20 | MS-DOS Program Terminate |
| 0:84 | 21 | MS-DOS Functions I/O Call |
| 0:88 | 22 | MS-DOS Programs' Terminate Routine |
| 0:8C | 23 | MS-DOS Programs' Control-Break Exit Routine |
| 0:90 | 24 | MS-DOS Programs' Critical Error Routine |
| 0:94 | 25 | MS-DOS Absolute Disk Read Call |
| 0:98 | 26 | MS-DOS Absolute Disk Write Call |
| 0:9C | 27 | MS-DOS Terminate and Stay Resident Call |
| 0:A0 | 28-3F | RESERVED for MS-DOS |
| 0:CC | 33 | RESERVED for Mouse Driver |
| 0:100 | 40 | Re-vectored Diskette BIOS INT 13h I/O Call when Fixed Disk is Present |
| 0:104 | 41 | Fixed Disk Drive #1 parameters pointer |
| 0:108 | 42 | Re-vectored Video BIOS INT 10h I/O Call when optional video ROM, is present. |
| 0:10C | 43 | EGA Video Display parameters |
| 0:110 | 44-45 | RESERVED for BIOS |
| 0:118 | 46 | Fixed Disk Drive #2 parameters pointer |
| 0:11C | 47-5F | RESERVED |
| 0:180 | 60-66 | RESERVED |
| 0:19C | 67 | RESERVED for Lotus/Intel/Microsoft Expanded Memory Manager Support |
| 0:1A0 | 68-6F | Not Used |
| 0:1C0 | 70 | Real-time Clock (H/W generated IRQ8) |
| 0:1C4 | 71 | Re-direction of old PC style INT 0Ah (IRQ2) |
| 0:1C8 | 72 | I/O Channel Available (H/W generated IRQ 10) |
| 0:1CC | 73 | I/O Channel Available (H/W generated IRQ 11) |
| 0:1D0 | 74 | I/O Channel Available (H/W generated IRQ 12) |
| 0:1D4 | 75 | Numeric Coprocessor (H/W generated IRQ 13) |
| 0:1D8 | 76 | Fixed Disk (H/W generated IRQ 14) |
| 0:1DC | 77 | I/O Channel Available (H/W generated IRQ 15) |
| 0:1E0 | 78-7F | Not Used |
| 0:200 | 80-85 | RESERVED by BASIC |
| 0:218 | 86-F0 | Used by BASIC |
| 0:3C4 | F1-FF | Not Used |

# ROM BIOS Data Area

| STARTING ADDRESS | LENGTH IN BYTES | DESCRIPTION |
|---|---|---|
| 40:0 | 8 | RS-232 Communications Adapter Installed Base Address Table (max. of 4 entries) |
| 40:8 | 8 | Parallel Printer Adapter Installed Base Address Table (max. of 4 entries) |
| 40:10 | 2 | Installed Equipment Flag (same as INT 11h return word) |
| 40:12 | 1 | Initialization/Diagnostic scratch byte |
| 40:13 | 2 | System Memory Size in kilobytes (640K max.) |
| 40:15 | 2 | Initialization/Diagnostic scratch word |
| 40:17 | 1 | Primary Keyboard Shift Status |

| Bit | Description |
|---|---|
| 7 | 1 = Insert state is on |
| 6 | 1 = Caps Lock state is on |
| 5 | 1 = Num Lock state is on |
| 4 | 1 = Scroll Lock state is on |
| 3 | 1 = Alt key is depressed |
| 2 | 1 = Ctrl key is depressed |
| 1 | 1 = Left Shift key is depressed |
| 0 | 1 = Right Shift key is depressed |

| | | |
|---|---|---|
| 40:18 | 1 | Secondary Keyboard Shift Status |

| Bit | Description |
|---|---|
| 7 | 1 = Insert key is depressed |
| 6 | 1 = Caps Lock key is depressed |
| 5 | 1 = Num Lock key is depressed |
| 4 | 1 = Scroll Lock key is depressed |
| 3 | 1 = Suspend Mode is active |
| 2 | 1 = Sys Req key is depressed |
| 1 | 1 = Left Alt key is depressed |
| 0 | 1 = Left Ctrl key is depressed |

| | | |
|---|---|---|
| 40:19 | 1 | Alt-numpad accumulator |
| 40:1A | 2 | Keyboard Buffer Head pointer |

# ROM BIOS Data Area

| STARTING ADDRESS | LENGTH IN BYTES | DESCRIPTION |
|---|---|---|
| 40:1C | 2 | Keyboard Buffer Tail pointer |
| 40:1E | 20h | 16 entry Keyboard Buffer |
| 40:3E | 1 | Floppy Disk Recalibration Status |

| Bit | Description |
|---|---|
| 7 | 1 = Floppy disk operation completed |
| 6-2 | Not Used |
| 1 | 0 = Floppy Drive 1 needs re-calibration |
| 0 | 0 = Floppy Drive 0 needs re-calibration |

| | | |
|---|---|---|
| 40:3F | 1 | Floppy Disk Motor On Status |

| Bit | Description |
|---|---|
| 7 | Write/Read Operation |
| 6 | Not Used |
| 5,4 | 00 = Drive 0 selected<br>01 = Drive 1 selected |
| 3,2 | Not Used |
| 1 | 1 = Drive 1 motor on |
| 0 | 0 = Drive 0 motor on |

| | | |
|---|---|---|
| 40:40 | 1 | Floppy disk motor on Time-out Value-Timer Clock ticks left until diskette motors are turned off |
| 40:41 | 7 | Floppy Disk S/W Status of last floppy disk INT 13h I/O operation |
| 40:42 | 7 | Floppy Disk Controller Status Byte Area |
| 40:49 | 1 | Current BIOS video mode |
| 40:4A | 2 | Current BIOS video screen column width |
| 40:4C | 2 | Current BIOS video screen buffer length in bytes |
| 40:4E | 2 | Current BIOS video display page starting offset address |
| 40:50 | 10h | Row/Column cursor coordinates for each of up to 8 display pages |
| 40:60 | 2 | Current BIOS video cursor type |
| 40:62 | 1 | Current BIOS video display page |
| 40:63 | 2 | Base I/O port address of the active display card |
| 40:65 | 1 | Copy of value written to Mode Selected Register |
| 40:66 | 1 | Copy of value written to Color Palette Register |

# ROM BIOS Data Area

| STARTING ADDRESS | LENGTH IN BYTES | DESCRIPTION |
|---|---|---|
| 40:67 | 4 | ROM initialization code optional ROM offset/ segment address storage |
| 40:6B | 1 | Last unexpected hardware interrupt that occurred or FFh if it was an unexpected software interrupt |
| 40:6C | 2 | Least significant word of Timer Clock Tick count |
| 40:6F | 2 | Most significant word of Timer Clock Tick count |
| 40:70 | 1 | 24-hour Timer Clock Tick rollover counter. |
| 40:71 | 1 | Keyboard Control-Break flag |
| | | Bit — Description |
| | | 7 — 1 = Keyboard Break |
| | | 6-0 — Not Used |
| 40:72 | 2 | Warm Restart flag<br>= 1234h, if it's a warm start<br>= anything else if it's a cold boot |
| 40:74 | 1 | Hard Disk S/W status of last INT 13h I/O operation |
| 40:75 | 1 | # of Hard Disk attached to system |
| 40:76 | 1 | Copy of Hard Disk control byte |
| 40:77 | 1 | Hard Disk port offset |
| 40:78 | 4 | Parallel Printer time-out table (max. of 4 entries) |
| 40:7C | 4 | RS-232 Communications time-out table (max. of 4 entries) |
| 40:80 | 2 | Keyboard buffer start offset location pointer (offset from 40:0) |
| 40:82 | 2 | Keyboard buffer end offset location pointer (offset from 40:0) |
| 40:84 | 1 | EGA # of CRT Rows — 1 |
| 40:85 | 2 | EGA # of bytes/character in EGA Font Table |

# ROM BIOS Data Area

| STARTING ADDRESS | LENGTH IN BYTES | DESCRIPTION |
|---|---|---|
| 40:87 | 1 | EGA Miscellaneous Information Byte 1 |

| Bit | Description |
|---|---|
| 7 | High bit of video mode, 1 = don't clear buffer display |
| 6,5 | EGA memory size in 64K chunks<br>00 = 64K, 01 = 128K, 10 = 192K, 11 = 256K |
| 4 | RESERVED |
| 3 | 0 = EGA active, 1 = not active |
| 2 | 0 = Write to CRT anytime<br>1 = Wait for display enable |
| 1 | 0 = Color monitor attached to EGA card<br>1 = Monochrome monitor attached to EGA card |
| 0 | 0 = Emulate cursor type |

| | | |
|---|---|---|
| 40:88 | 1 | EGA Miscellaneous Information Byte 2 |

| Bit | Description |
|---|---|
| 7-4 | EGA Feature Bits |
| 30 | EGA DIP switches |

| | | |
|---|---|---|
| 40:89 | 2 | RESERVED |
| 40:8B | 1 | Last floppy disk rate selected |
| 40:8C | 1 | Hard disk status register copy |
| 40:8D | 1 | Hard disk error register copy |
| 40:8E | 1 | Hard disk interrupt flag |
| 40:8F | 1 | Multi-rate floppy disk controller flag |

| Bit | Description |
|---|---|
| 7-1 | RESERVED |
| 0 | Always = 1 |

| | | |
|---|---|---|
| 40:90 | 2 | Floppy drive 0/1 Media State Table |
| 40:92 | 2 | Floppy drive 0/1 Operation State Table |
| 40:94 | 2 | Floppy drive 0/1 Current Track Table |

# ROM BIOS Data Area

| STARTING ADDRESS | LENGTH IN BYTES | DESCRIPTION |
|---|---|---|
| 40:96 | 1 | Enhanced Keyboard Flags |

| Bit | Description |
|---|---|
| 7 | 1 = Read ID bytes command in progress |
| 6 | 1 = First of ID bytes was last |
| 5 | 1 = Force Num Lock if 101-keyboard |
| 4 | 1 = 101-key keyboard is attached |
| 3 | 1 = Right ALT key is depressed |
| 2 | 1 = Right Ctrl key is depressed |
| 1 | 1 = Keyboard controller E0 command was last |
| 0 | 1 = Keyboard controller E1 command was last |

| | | |
|---|---|---|
| 40:97 | 1 | Keyboard LED and Flags data area |

| Bit | Description |
|---|---|
| 7 | 1 = Indicates 3 failures of sending data to keyboard |
| 6 | 1 = LED Update in progress |
| 5 | 1 = Re-send received from keyboard |
| 4 | 1 = Acknowledge received from keyboard |
| 3 | 1 = Not Used (Must be 0) |
| 2 | 1 = Caps Lock LED is on |
| 1 | 1 = Num Lock LED is on |
| 0 | 1 = Scroll Lock LED is on |

| | | |
|---|---|---|
| 40:98 | 2 | Real-time Clock user wait flag offset address |
| 40:9A | 2 | Real-time Clock user wait flag segment address |
| 40:9C | 2 | Real-time Clock wait count low word |
| 40:9E | 2 | Real-time Clock wait count high word |
| 40:A0 | 1 | Real-time Clock wait active flag |
| 40:A1 | 7 | RESERVED |
| 40:A8 | 4 | EGA-pointer to table of EGA pointers |
| 40:AC | 9 | RESERVED |
| 40:B5 | 1 | Tandy Information Flag |

| Bit | Description |
|---|---|
| 7-1 | RESERVED |
| 0 | Floppy Swap Drive Flag<br>= 1, swap drives<br>= 0, don't swap drives<br>Note: Valid for 2 floppy drive systems only |

| | | |
|---|---|---|
| 40:B6 | 4Ah | RESERVED |

# MS-DOS & BASIC Data Area

| STARTING ADDRESS | LENGTH IN BYTES | DESCRIPTION |
|---|---|---|
| 50:0 | 1 | Print Screen Status Flag<br>= 0, Print Screen not active or successful<br>= 1, Print Screen in progress<br>= FFh, Print Screen encountered error |
| 50:1 | 3 | RESERVED |
| 50:4 | 1 | MS-DOS Single Floppy Drive Mode Status Byte<br>= 0, Logical drive A: last accessed<br>= 1, Logical drive B: last accessed |
| 50:5 | FBh | RESERVED |

# Keyboard ASCII and Scan Codes

The table in this appendix lists the keys on the Tandy 3000 NL keyboard in the key number order, along with the hardware scan codes and ASCII code they generate. For each key, the following entries are given:

*Hardware Keyboard Make Code*

A one byte value which the keyboard unit presents to the keyboard controller when a key is pressed. This value uniquely identifies the physical key on the keyboard.

*Hardware Keyboard Break Code*

A two byte value which the keyboard unit presents to the keyboard controller when a key is released. This value uniquely identifies the physical key on the keyboard.

*Keyboard Interrupt Make Code*

A value or values which the keyboard controller presents to the CPU when a key is pressed. This value (scan code) can be from one to four bytes in length and uniquely identifies the physical key on the keyboard.

*Keyboard Interrupt Break Code*

A value or values which the keyboard controller presents to the CPU when a key is released. This value (scan code) can be from one to four bytes in length and uniquely identifies the physical key on the keyboard.

*Standard ASCII Codes*

A value which the Keyboard BIOS Services return when the extended keyboard functions are called.

*Extended ASCII Codes*

A value which the Keyboard BIOS Services return when the extended keyboard functions are called.

*Normal (Norm)*

The normal ASCII value that is returned when a key is depressed by itself.

*Shift*

The ASCII value that is returned when a key is pressed along with either of the 'Ctrl' keys.

*Control (Ctrl)*

The ASCII value that is returned when a key is pressed along with either of the 'Ctrl' keys

*Alternate (Alt)*

The ASCII value that is returned when a key is pressed along with either of the 'Alt' keys.

*Key #*

The numbered key order of the keyboard.

*Key Description*

The physical keyboard legend enscribed on the key

The following special symbols appear in the table:

**Note#** No ASCII code is generated but the special function described at the end of the table is performed.

_____ This key combination does not generate an ASCII code and no special function is performed.

**Note:** All numeric values in the table are expressed in hexadecimal.

# KEYBOARD SCAN CODES

| Key # | Key Descript. | Hardware Kybrd Make Code | Hardware Kybrd Break Code | Kybrd Interrupt Make Code | Kybrd Interrupt Break Code | Standard ASCII (Scancode/ASCII code) Norm | Standard ASCII Shift | Standard ASCII Ctrl | Standard ASCII Alt | Extended ASCII (Scancode/ASCII code) Norm | Extended ASCII Shift | Extended ASCII Ctrl | Extended ASCII Alt |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Esc | 76 | F076 | 01 | 81 | 011B | 011B | 011B | ----- | 011B | 011B | 011B | 0100 |
| 2 | F1 | 05 | F005 | 3B | BB | 3B00 | 5400 | 5E00 | 6800 | 3B00 | 5400 | 5E00 | 6800 |
| 3 | F2 | 06 | F006 | 3C | BC | 3C00 | 5500 | 5F00 | 6900 | 3C00 | 5500 | 5F00 | 6900 |
| 4 | F3 | 04 | F004 | 3D | BD | 3D00 | 5600 | 6000 | 6A00 | 3D00 | 5600 | 6000 | 6A00 |
| 5 | F4 | 0C | F00C | 3E | BE | 3E00 | 5700 | 6100 | 6B00 | 3E00 | 5700 | 6100 | 6B00 |
| 6 | F5 | 03 | F003 | 3F | BF | 3F00 | 5800 | 6200 | 6C00 | 3F00 | 5800 | 6200 | 6C00 |
| 7 | F6 | 0B | F00B | 40 | C0 | 4000 | 5900 | 6300 | 6D00 | 4000 | 5900 | 6300 | 6D00 |
| 8 | F7 | 83 | F083 | 41 | C1 | 4100 | 5A00 | 6400 | 6E00 | 4100 | 5A00 | 6400 | 6E00 |
| 9 | F8 | 0A | F00A | 42 | C2 | 4200 | 5B00 | 6500 | 6F00 | 4200 | 5B00 | 6500 | 6F00 |
| 10 | F9 | 01 | F001 | 43 | C3 | 4300 | 5C00 | 6600 | 7000 | 4300 | 5C00 | 6600 | 7000 |
| 11 | F10 | 09 | F009 | 44 | C4 | 4400 | 5D00 | 6700 | 7100 | 4400 | 5D00 | 6700 | 7100 |
| 12 | F11 | 78 | F078 | 57 | D7 | ----- | ----- | ----- | ----- | 8500 | 8700 | 8900 | 8B00 |
| 13 | F12 | 07 | F007 | 58 | D8 | ----- | ----- | ----- | ----- | 8600 | 8800 | 8A00 | 8C00 |
| 14 | Print Scrn | E07C | E0F07C | E02AE037 | E0B7E0AA | Note[1] | Note[1] | 7200 | ----- | Note[1] | Note[1] | 7200 | ----- |
| 15 | Scroll Lock | 7E | F07E | 46 | C6 | Note[2] | Note[2] | ------ | Note[2] | Note[2] | Note[2] | ----- | Note[2] |
| 16 | Pause Break | E11477 | E1F014F077 | E11D45 | E19DC5 | Note[3] | Note[3] | Note[4] | Note[3] | Note[3] | Note[3] | Note[4] | Note[3] |
| 17 | ~ or \ | 0E | F00E | 29 | A9 | 2960 | 297E | ----- | ----- | 6000 | 7E00 | ----- | 2900 |
| 18 | ! or \| | 16 | F016 | 02 | 82 | 0231 | 0221 | ----- | 7800 | 0231 | 0221 | ----- | 7800 |

# KEYBOARD SCAN CODES

| Key # | Key Descript. | Hardware Kybrd Make Code | Hardware Kybrd Break Code | Kybrd Interrupt Make Code | Kybrd Interrupt Break Code | Standard ASCII (Scancode/ASCII code) Norm | Standard ASCII Shift | Standard ASCII Ctrl | Standard ASCII Alt | Extended ASCII (Scancode/ASCII code) Norm | Extended ASCII Shift | Extended ASCII Ctrl | Extended ASCII Alt |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 19 | @ or 2 | 1E | F01E | 03 | 83 | 0332 | 0340 | 0300 | 7900 | 0332 | 0340 | 0300 | 7900 |
| 20 | # or 3 | 26 | F026 | 04 | 84 | 0433 | 0423 | ----- | 7A00 | 0433 | 0423 | ----- | 7A00 |
| 21 | $ or 4 | 25 | F025 | 05 | 85 | 0534 | 0524 | ----- | 7B00 | 0534 | 0524 | ----- | 7B00 |
| 22 | % or 5 | 2E | F02E | 06 | 86 | 0635 | 0625 | ----- | 7C00 | 0635 | 0625 | ----- | 7C00 |
| 23 | ^ or 6 | 36 | F036 | 07 | 87 | 0736 | 075E | 071E | 7D00 | 0736 | 075E | 071E | 7D00 |
| 24 | & or 7 | 3D | F03D | 08 | 88 | 0837 | 0826 | ----- | 7E00 | 0837 | 0826 | ----- | 7E00 |
| 25 | * or 8 | 3E | F03E | 09 | 89 | 0938 | 092A | ----- | 7F00 | 0938 | 092A | ----- | 7F00 |
| 26 | ( or 9 | 46 | F046 | 0A | 8A | 0A39 | 0A28 | ----- | 8000 | 0A39 | 0A28 | ----- | 8000 |
| 27 | ) or 0 | 45 | F045 | 0B | 8B | 0B34 | 0B29 | ----- | 8100 | 0B34 | 0B29 | ----- | 8100 |
| 28 | _ or - | 4E | F04E | 0C | 8C | 0C2D | 0C5F | 0C1F | 8200 | 0C2D | 0C5F | 0C1F | 8200 |
| 29 | + or = | 55 | F055 | 0D | 8D | 0D3D | 0D2B | ----- | 8300 | 0D3D | 0D2B | ----- | 8300 |
| 30 | Backspace | 66 | F066 | 0E | 8E | 0E08 | 0E08 | 0E7F | ----- | 0E08 | 0E08 | 0E7F | 0E00 |
| 31 | Insert | E070 | E0F070 | E02AE052 | E0D2E0AA | 5200 | 5200 | ----- | ----- | 52E0 | 52E0 | 92E0 | A200 |
| 32 | Home | E06C | E0F06C | E02AE047 | E0C7E0AA | 4700 | 4700 | 7700 | ----- | 47E0 | 47E0 | 77E0 | 9700 |
| 33 | Pg Up | E07D | E0F07D | E02AE049 | E0C9E0AA | 4900 | 4900 | 8400 | ----- | 49E0 | 49E0 | 84E0 | 9900 |
| 34 | Num Lock | 77 | F077 | 45 | C5 | Note[5] | Note[5] | ----- | Note[5] | Note[5] | Note[5] | ---- | Note[5] |
| 35 | / | E04A | E0F04A | E035 | E0B5 | 352F | 352F | ----- | ----- | E02F | E02F | 9500 | A400 |
| 36 | * | 7C | F07C | 37 | B7 | 372A | 372A | ----- | ----- | 372A | 372A | 9600 | 3700 |
| 37 | - | 7B | F07B | 4A | CA | 4A2D | 4A2D | ----- | ----- | 4A2D | 4A2D | 8E00 | 4A00 |

# KEYBOARD SCAN CODES

| Key # | Key Descript. | Hardware Kybrd Make Code | Hardware Kybrd Break Code | Kybrd Interrupt Make Code | Kybrd Interrupt Break Code | Standard ASCII (Scancode/ASCII code) Norm | Standard ASCII Shift | Standard ASCII Ctrl | Standard ASCII Alt | Extended ASCII (Scancode/ASCII code) Norm | Extended ASCII Shift | Extended ASCII Ctrl | Extended ASCII Alt |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 38 | Tab | 0D | F00D | 0F | 8F | 0F90 | 0F00 | ----- | ----- | 0F09 | 0F00 | 9400 | A500 |
| 39 | Q or q | 15 | F015 | 10 | 90 | 1071 | 1051 | 1011 | 1000 | 1071 | 1051 | 1011 | 1000 |
| 40 | W or w | 1D | F01D | 11 | 91 | 1177 | 1157 | 1117 | 1100 | 1177 | 1157 | 1117 | 1100 |
| 41 | E or e | 24 | F024 | 12 | 92 | 1265 | 1245 | 1205 | 1200 | 1265 | 1245 | 1205 | 1200 |
| 42 | R or r | 2D | F02D | 13 | 93 | 1372 | 1352 | 1312 | 1300 | 1372 | 1352 | 1312 | 1300 |
| 43 | T or t | 2C | F02C | 14 | 94 | 1474 | 1454 | 1414 | 1400 | 1474 | 1454 | 1414 | 1400 |
| 44 | Y or y | 35 | F035 | 15 | 95 | 1579 | 1559 | 1519 | 1500 | 1579 | 1559 | 1519 | 1500 |
| 45 | U or u | 3C | F03C | 16 | 96 | 1675 | 1655 | 1615 | 1600 | 1675 | 1655 | 1615 | 1600 |
| 46 | I or i | 43 | F043 | 17 | 97 | 1769 | 1749 | 1709 | 1700 | 1769 | 1749 | 1709 | 1700 |
| 47 | O or o | 44 | F044 | 18 | 98 | 186F | 184F | 180F | 1800 | 186F | 184F | 180F | 1800 |
| 48 | P or p | 4D | F04D | 19 | 99 | 1970 | 1950 | 1910 | 1900 | 1970 | 1950 | 1910 | 1900 |
| 49 | { or [ | 54 | D054 | 1A | 9A | 1A5B | 1A7B | 1A1B | ----- | 1A5B | 1A7B | 1A1B | 1A00 |
| 50 | } or ] | 5B | F05B | 1B | 9B | 1B5D | 1B7D | 1B1D | ----- | 1B5D | 1B7D | 1B1D | 1B00 |
| 51 | \| or \ | 5D | F05D | 2B | AB | 2B5C | 2B7C | 2B1C | ----- | 2B5C | 2B7C | 2B1C | 2B00 |
| 52 | Delete | E071 | E0F071 | E02AE053 | E0D3E0AA | 5300 | 5300 | ----- | ----- | 53E0 | 53E0 | 93E0 | A300 |
| 53 | End | E069 | E0F069 | E02AE04F | E0CFE0AA | 4F00 | 4F00 | 7500 | ----- | 4FE0 | 4FE0 | 75E0 | 9F00 |
| 54 | Page Down | E07A | E0F07A | E02AE051 | E0D1E0AA | 5100 | 5100 | 7600 | ----- | 51E0 | 51E0 | 76E0 | A100 |
| 55 | 7 or Home | 6C | F06C | 47 | C7 | 4700 | 4737 | 7700 | Note[6] | 4700 | 4737 | 7700 | Note[6] |
| 56 | 8 | 75 | F075 | 48 | C8 | 4800 | 4838 | ---- | Note[6] | 4800 | 4838 | 8D00 | Note[6] |
| 57 | 9 or Page Up | 7D | F07D | 49 | C9 | 4900 | 4939 | 8400 | Note[6] | 4900 | 4939 | 8400 | Note[6] |

# KEYBOARD SCAN CODES

| Key # | Key Descript. | Hardware Kybrd Make Code | Hardware Kybrd Break Code | Kybrd Interrupt Make Code | Kybrd Interrupt Break Code | Standard ASCII (Scancode/ASCII code) Norm | Standard ASCII Shift | Standard ASCII Ctrl | Standard ASCII Alt | Extended ASCII (Scancode/ASCII code) Norm | Extended ASCII Shift | Extended ASCII Ctrl | Extended ASCII Alt |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 58 | + | 79 | F079 | 4E | CE | 4E2B | 4E2B | ---- | ---- | 4E2B | 4E2B | 9000 | 4E00 |
| 59 | Caps Lock | 58 | F058 | 3A | BA | Note[7] | Note[7] | ---- | Note[7] | Note[7] | Note[7] | ---- | Note[7] |
| 60 | A or a | 1C | F01C | 1E | 9E | 1E61 | 1E41 | 1E01 | 1E00 | 1E61 | 1E41 | 1E01 | 1E00 |
| 61 | S or s | 1B | F01B | 1F | 9F | 1F73 | 1F53 | 1F13 | 1F00 | 1F73 | 1F53 | 1F13 | 1F00 |
| 62 | D or d | 23 | F023 | 20 | A0 | 2064 | 2044 | 2004 | 2000 | 2064 | 2044 | 2004 | 2000 |
| 63 | F or f | 2B | F02B | 21 | A1 | 2166 | 2146 | 2106 | 2100 | 2166 | 2146 | 2106 | 2100 |
| 64 | G or g | 34 | F034 | 22 | A2 | 2267 | 2247 | 2207 | 2200 | 2267 | 2247 | 2207 | 2200 |
| 65 | H or h | 33 | F033 | 23 | A3 | 2368 | 2348 | 2308 | 2300 | 2368 | 2348 | 2308 | 2300 |
| 66 | J or j | 3B | F03B | 24 | A4 | 246A | 244A | 240A | 2400 | 246A | 244A | 240A | 2400 |
| 67 | K or k | 42 | F042 | 25 | A5 | 256B | 254B | 250B | 2500 | 256B | 254B | 250B | 2500 |
| 68 | L or l | 4B | F04B | 26 | A6 | 266C | 264C | 260C | 2600 | 266C | 264C | 260C | 2600 |
| 69 | : or ; | 4C | F04C | 27 | A7 | 273B | 273A | ---- | ---- | 273B | 273A | ---- | 2700 |
| 70 | " or ' | 52 | F052 | 28 | A8 | 2827 | 2822 | ---- | ---- | 2827 | 2822 | ---- | 2800 |
| 71 | Enter | 5A | F05A | 1C | 9C | 1C0D | 1C0D | 1C0A | ---- | 1C0D | 1C0D | 1C0A | 1C00 |
| 72 | 4 | 6B | F06B | 4B | CB | 4B00 | 4B34 | 7300 | Note[6] | 4B00 | 4B34 | 7300 | Note[6] |
| 73 | 5 | 73 | F073 | 4C | CC | ----- | 4C35 | --- | Note[6] | 4C00 | 4C35 | 8F00 | Note[6] |
| 74 | 6 | 74 | F074 | 4D | CD | 4D00 | 4D36 | 7400 | Note[6] | 4D00 | 4D36 | 7400 | Note[6] |

# KEYBOARD SCAN CODES

| Key # | Key Descript. | Hardware Kybrd Make Code | Hardware Kybrd Break Code | Kybrd Interrupt Make Code | Kybrd Interrupt Break Code | Standard ASCII (Scancode/ASCII code) Norm | Standard ASCII Shift | Standard ASCII Ctrl | Standard ASCII Alt | Extended ASCII (Scancode/ASCII code) Norm | Extended ASCII Shift | Extended ASCII Ctrl | Extended ASCII Alt |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 76 | Left Shift | 12 | F012 | 2A | AA | Note[8] | Note[8] | Note[8] | Note[8] | Note[8] | Note[8] | Note[8] | Note[8] |
| 77 | Z or z | 1A | F01A | 2C | AC | 2C7A | 2C5A | 2C1A | 2C00 | 2C7A | 2C5A | 2C1A | 2C00 |
| 78 | X or x | 22 | F022 | 2D | AD | 2D78 | 2D58 | 2D18 | 2000 | 2D78 | 2D58 | 2D18 | 2000 |
| 79 | C or c | 21 | F021 | 2E | AE | 2E63 | 2E43 | 2E03 | 2E00 | 2E63 | 2E43 | 2E03 | 2E00 |
| 80 | V or v | 2A | F02A | 2F | AF | 2F76 | 2F56 | 2F16 | 2F00 | 2F76 | 2F56 | 2F16 | 2F00 |
| 81 | B or b | 32 | F032 | 30 | B0 | 3062 | 3042 | 3002 | 3000 | 3062 | 3042 | 3002 | 3000 |
| 82 | N or n | 31 | F031 | 31 | B1 | 316E | 314E | 310E | 3100 | 316E | 314E | 310E | 3100 |
| 83 | M or m | 3A | F03A | 32 | B2 | 326D | 324D | 320D | 3200 | 326D | 324D | 320D | 3200 |
| 84 | < or , | 41 | F041 | 33 | B3 | 332C | 333C | ----- | ----- | 332C | 333C | ----- | 3300 |
| 85 | > or . | 49 | F049 | 34 | B4 | 342E | 343E | ----- | ----- | 342E | 343E | ----- | 3400 |
| 86 | ? or / | 4A | F04A | 35 | B5 | 352F | 353F | ----- | ----- | 352F | 353F | ----- | 3500 |
| 87 | Right Shift | 59 | F059 | 36 | B6 | Note[8] | Note[8] | Note[8] | Note[8] | Note[8] | Note[8] | Note[8] | Note[8] |
| 88 | Up Arrow | E075 | E0F075 | E02AE048 | E0C8E0AA | 4800 | 4800 | ----- | ---- | 48E0 | 48E0 | 8DE0 | 9800 |
| 89 | 1 or End | 69 | F069 | 4F | CF | 4F00 | 4F31 | 7500 | Note[6] | 4F00 | 4F31 | 7500 | Note[6] |
| 90 | 2 | 72 | F072 | 50 | D0 | 5000 | 5032 | ---- | Note[6] | 5000 | 5032 | 9100 | Note[6] |
| 91 | 3 or Pg Dn | 7A | F07A | 51 | D1 | 5100 | 5133 | 7600 | Note[6] | 5100 | 5133 | 7600 | Note[6] |
| 92 | Left Ctrl | 14 | F014 | 1D | 9D | Note[9] | Note[9] | Note[9] | Note[9] | Note[9] | Note[9] | Note[9] | Note[9] |
| 93 | Left Alt | 11 | F011 | 38 | B8 | Note[10] | Note[10] | Note[10] | Note[10] | Note[10] | Note[10] | Note[10] | Note[10] |
| 94 | Space | 29 | F029 | 39 | B9 | 3920 | 3920 | 3920 | 3920 | 3920 | 3920 | 3920 | 3920 |

# KEYBOARD SCAN CODES

| Key # | Key Descript. | Hardware Kybrd Make Code | Hardware Kybrd Break Code | Kybrd Interrupt Make Code | Kybrd Interrupt Break Code | Standard ASCII (Scancode/ASCII code) Norm | Standard ASCII Shift | Standard ASCII Ctrl | Standard ASCII Alt | Extended ASCII (Scancode/ASCII code) Norm | Extended ASCII Shift | Extended ASCII Ctrl | Extended ASCII Alt |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 95 | Right Alt | E011 | E0F011 | E038 | E0B8 | Note[9,10] | Note[9,10] | Note[9,10] | Note[9,10] | Note[9,10] | Note[9,10] | Note[9,10] | Note[9,10] |
| 96 | Right Ctrl | E014 | E0F014 | E01D | E09D | Note[9] | Note[9] | Note[9] | Note[9] | Note[9] | Note[9] | Note[9] | Note[9] |
| 97 | Left Arrow | E06B | E0F06B | E02AE04B | E0CBE0AA | 4B00 | 4B00 | 7300 | ----- | 4BE0 | 4BE0 | 73E0 | 9B00 |
| 98 | Down Arrow | E072 | E0F072 | E02AE050 | E0D0E0AA | 5000 | 5000 | ----- | ----- | 50E0 | 50E0 | 91E0 | A000 |
| 99 | Right Arrow | E074 | E0F074 | E024E04D | E0CDE0AA | 4D00 | 4000 | 7400 | ---- | 4DE0 | 4DE0 | 74E0 | 9D00 |
| 100 | 0 or Ins | 70 | F070 | 52 | D2 | 5200 | 5230 | ---- | Note[6] | 5200 | 523H | 9200 | Note[6] |
| 101 | . or Del | 71 | F071 | 53 | D3 | 5300 | 532E | ---- | ---- | 5300 | 532E | 9300 | ----- |
| 102 | Enter | E05A | E0F05A | E01C | E09C | 1C0D | 1C0D | 1C0A | ---- | E00D | E00D | E00A | A600 |

## NOTES

Note1 —INT 05H is invoked and a screen dump is performed
Note2 —the scroll lock active bit is toggled
Note3 —the pause state is initiated
Note4 —INT 1BH is invoked
Note5 —the numlock active bit is toggled
Note6 —ALT num pad generates raw ascii code of typed number
Note7 —the caps lock active bit is toggled
Note8 —hold shift lock active until key is released
Note9 —hold control shift active until key is released
Note10—hold alternate shift active until key is released

RADIO SHACK
A Division of Tandy Corporation
Fort Worth, Texas 76102

10/83-5Co 874-3081 Printed in U.S.A.