

Ready 5000

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READY



**Tandy 3000**  
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**DETAIL DESIGN SPECIFICATION**

**TANDY MODEL 3000 COMPUTER**



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## 1.0 SCOPE

The purpose of this specification is to serve as the detailed specification guide for the TANDY Model 3000 computer. The system is composed of four buses; 80286 LOCAL BUS, LOCAL MEMORY BUS, SYSTEM I/O (AT) BUS, and the BUFFERED PERIPHERAL BUS.

Each bus has timing associated with the devices being accessed. For instance, the 80286 LOCAL BUS typically operates with one wait state, its bandwidth is 90 % utilized by the CPU, operates asynchronous to the math coprocessor (optional), and operates synchronous to the other buses.

The LOCAL MEMORY BUS consists of two banks of DRAMS. This bus can support to 1MB of memory using 256K x 1 DRAMS. At this time the basic configuration of this bus will consist of one bank of 256K x 1 DRAMS and be upgradable to only 640KB by populating the second bank with 64K x 1 DRAMS. The bandwidth of this bus is 5.3MB/sec, and requires the use of DRAMS with a maximum access time of 150ns.

The SYSTEM I/O (AT) BUS provides system expansion through 10 I/O peripheral card slots (2 PC compatible and 8 AT compatible) internal to the cabinet. The bandwidth of this bus is the same as the 80286 LOCAL BUS or the MEMORY BUS, and incorporates variable wait states to service some option cards.

The BUFFERED PERIPHERAL BUS is an extension of the SYSTEM I/O (AT) BUS, but supports DMA operations, provides counters and timers, interrupt requests, I/O decoding, keyboard logic, speaker logic, and a real time clock with RAM.

## 1.1 PRODUCT BRIEF

**TANDY DESK TOP PC/AT PRODUCT BRIEF****FEATURES:**

- o Low Entry Cost Advanced PC
- o 8MHz 16-Bit 80286 with on Chip Memory Management and Protection
- o Standard 512KB Memory
  - Expandable to 640KB on Board
  - Bus Addressing Supports to 16MB Memory
- o Standard High Capacity 5-1/4" Slim Line Floppy Disk Drive
  - Selectable 1.2MB or 720KB Formats Allows Compatibility with IBM-AT or Tandy 2000
  - Channel for Additional Internal Floppy Disk Drive for either a 360KB, 720KB, or 1.2MB Format
- o Channel for optional Hard Disk Drive
- o Ten IBM-AT Compatible Slots for Standard Peripherals and Additional Memory expansion (8-Slots Open)
- o True Software Compatibility with the IBM-AT in the Single User MS-DOS Mode or Multi-User Protected Mode
- o Standard Real Time Clock with CMOS Ram and Battery Backup
- o Standard Serial/Parallel Adapter (Uses one I/O Slot)
- o Standard PC/AT Compatible Keyboard
- o Support for Optional Math Co-processor

**PHYSICAL DIMENSIONS**

Height 6.5 inches  
Width 19.0 inches  
Depth 18.0 inches

**HEAT OUTPUT**

850 BTU/hr.

**NOISE LEVEL**

42 decibels

**OPERATING TEMPERATURE**

55 - 85 degrees Fahrenheit  
13 - 29 degrees Celsius

## 2.0 FUNCTIONAL DESCRIPTION

### 2.1 80286 Local Bus

This bus consists of the 80286 CPU and the 80287 Co-Processor. There are no buffers between the two. This bus connects memory and I/O resources to the 80286 processor, using 24 address lines, 16 data lines, and a number of status and control signals. All resources other than the 80287 are buffered to this bus.

#### 2.1.1 82284 Clock Generator

This 18-pin dip generates the clock, ready, and reset signals required for the 80286 processors and support components.

#### 2.1.2 82288 Bus Controller

This 20-pin dip is used to provide address latch control, and command outputs based on the 80286 status lines.

#### 2.1.3 80287 Numeric Processor Extension (Optional)

This 40-pin dip works in parallel with the 80286 CPU. This parallel operation decreases operating time by allowing the coprocessor to execute mathematical calculations independent of the CPU. This device performs high-speed arithmetic, logarithmic functions, and trigonometric operations with seven numeric data types divided into the following three classes:

- \* Binary integers (three types)
- \* Decimal integers (one type)
- \* Real numbers (three types)

## 2.2 System Memory

## 2.2.1 Memory Configuration

The real address mode is defaulted to at power up, and has a maximum directly addressable range of 1 megabyte.

The protected address mode of the CPU has a maximum directly accessible range of 16 megabytes, and a virtual addressable range of 4 gigabytes. In this mode, memory configuration below the 1 megabyte region remains mapped the same as in real address mode. The on-board ROM locations 0E0000H thru OFFFFH are duplicated at addresses FE0000H thru FFFFFH.

FFFFFH	BOOT ROM IMAGE	16.0 Meg
FF8000h	EXPANSION BIOS ROM IMAGE	
FE0000h	UNUSED	15.9 Meg
F00000h		15.0 Meg
14 MEGABYTE EXPANSION RAM ON SYSTEM I/O BUS		PROTECTED MEMORY MODE
100000h		1.0 Meg
OFFFFFh	BOOT ROM	
OF8000h	EXPANSION BIOS ROM	
OE0000h		896 K
PERIPHERAL MEMORY AREA		REAL MEMORY MODE
OC0000h		768 K
VIDEO MEMORY AREA		
OA0000h		640 K
128K ON-BOARD EXPANSION		
OB0000h		512 K
512K ON-BOARD MEMORY		
OC00000h		000 K

### 2.2.2 ROM Subsystem

The on-board ROM subsystem consists of four ROM/EPROM modules; the code for odd and even addresses reside in separate modules, and is not parity checked. Each module can support to 32KB of data for a total of 128KB. The BIOS (Basic Input Output System) resides in 64KB allowing a 64KB expansion range. The ROM is assigned at the top of the first and last 1 megabyte address space (0E0000 and FE0000 HEX)

### 2.2.3 RAM Subsystem

The system RAM consists of two divisions; the on board system memory (Standard 512 kilobytes of DRAM upgradable to 640 kilobytes), and the SYSTEM I/O (AT) BUS memory options.

Memory refresh requests one memory cycle every 15 microseconds through channel 1 of the counter/timer subsystem. The RAM initialization program initializes channel 1 of the counter/timer subsystem to the rate generation mode, with a period of 15 microseconds, and then performs a memory read operation to any memory location. The memory must be accessed or refreshed eight times before it can be used.

### 2.2.4 Parity Control

All dynamic memory utilizes odd parity. Parity can be disabled by the CPU. There is one parity bit per byte of DRAM - for both upper and lower banks of memory.

## 2.3 System I/O (AT) Bus

This bus is a 100% compatible IBM-AT bus. It has an open-bus structure which will allow multiple microprocessors to share the systems resources. A total of ten expansion cards are supported. Although all of these slots can support some PC compatible boards, two are dedicated for this use. Some of the functions supported by this bus are:

- \* 24-bit memory addressing.
- \* 8 or 16 bit data accesses.
- \* I/O addressing range of 100 to 3FF hex.
- \* Interrupts and DMA support.
- \* I/O wait state generation.
- \* Refresh of system memory.

### 2.3.1 Floppy Disk Controller

This controller resides on the I/O (AT) bus and is an integral part of the Fixed Disk controller. It supports two 5-1/4" drives (one standard) through an internal, daisy-chained, flat cable. The controller will support 160K, 320K, and 1.2M byte formats. The interface is buffered on the I/O bus and uses the system board's DMA for block data transfers. An interrupt is used to indicate when an operation is complete or that a status condition requires the CPU's attention.

### 2.3.2 Fixed Disk Controller

This controller is integrated with the Floppy Disk controller. It is 100% PC AT compatible. The controller is based on Western Digital's WD1010 and on a self-adjusting Data Separator WD10C20. The controller board supports up to 16 read/write heads per drive, 1024 cylinders per drive, and two Winchester disk drives.

### 2.3.3 Memory Expansion Board

These optional boards may be configured as 512KB, 1MB, 1.5MB or 2MB. All Memory Expansion boards must be configured on contiguous boundaries. These boards have a 16-bit data path, parity checking, and an addressable range of 16MB. Refresh of the DRAMs is accomplished by the main PCB. Memory limitation is determined by the available option slots.

### 2.3.4 Serial/Parallel I/O

This standard Serial/Parallel card is 100% compatible with the IBM-AT.

#### SERIAL PORT

The serial portion of this board supports the EIA RS-232C interface standard through a 9-pin D-shell connector (a 9-pin to 25-pin adapter cable is used to complete the EIA RS-232C interface) located on the rear of the board for external chassis access (the serial port is fully programmable, and supports asynchronous communications).

The onboard universal asynchronous receiver transmitter adds and removes start, parity, and stop bits (five, six, seven, and eight bit characters with 1, 1.5, or 2 stop bits are supported). The onboard programmable baud-rate generator supports operation from 50 to 9600 baud. A prioritized interrupt scheme controls transmit, receive, error, line status, and data set interrupts.

#### Serial Port Controller (NS16450) Specifications

**Clear-to-Send (CTS):** signal is bit 4 of the modem status register - bit 0 (DCTS) of the modem status register indicates a state change of CTS. If the modem status interrupt is enabled, and the CTS changes state, an interrupt is generated.

**Data Set Ready (DSR):** signal is bit 5 of the modem status register and indicates the modem or data set is ready to establish communications link and transfer data with the controller - bit 1 (DDSR) of the modem status register indicates a state change of DSR. If the modem status interrupt is enabled, and the DSR changes state, an interrupt is generated.

### 2.3.5 Monochrome Display Adapter

The controller used for this option is the TANDY Catalog # 25-3040 Monochrome Display Adapter. This adapter uses the TANDY VM-3 Monochrome Monitor catalog # 25-3010. This card is 100% compatible with this or the IBM AT product.

### 2.3.6 Color/Graphics Monitor Adapter

The controller used for the 320 x 200 resolution option is the TANDY Catalog # 25-3043 Graphics Display Adapter. This adapter uses the TANDY CM-2 Color Monitor catalog # 26-3212 or the TANDY VM-3 Monochrome Monitor catalog # 25-3010. This card is 100% compatible with this or the IBM AT product.

The controller used for the 640 x 200 resolution option is the TANDY Catalog # 25-3044 Graphics Master Adapter. This adapter uses the TANDY CM-2 Color Monitor catalog # 26-3212.

This card is 100% hardware compatible with this or the IBM AT product. It is not software compatible with any IBM high resolution graphics cards.

## 2.4 Buffered Peripheral Bus

### 2.4.1 System Interrupts

The 80286 microprocessor NMI (non maskable interrupt) and two 8259A interrupt controller chips together provide the system with a total of 16 levels of interrupts. Note that any or all interrupt levels may be masked, including the CPU's NMI. The following table shows the interrupt level assignments in decreasing order of priority (note that interrupts 8 thru 15 are accessed thru interrupt 2).

<u>INTERRUPT</u>	<u>DEVICE</u>	<u>FUNCTION</u>
NMI	CPU's	Parity of I/O Channel Check
IRQ0	Controller 1	Timer Output 0
IRQ1	Controller 1	Keyboard (Output Buffer Full)
IRQ2	Controller 1	IRQ8 thru IRQ15
IRQ3	Controller 1	Serial Port 2
IRQ4	Controller 1	Serial Port 1
IRQ5	Controller 1	Parallel Port 2
IRQ6	Controller 1	Diskette Controller
IRQ7	Controller 1	Parallel Port 1
IRQ8	Controller 2	Real Time Clock Interrupt
IRQ9	Controller 2	Software Redirected to INT DAH (IRQ2)
IRQ10	Controller 2	Reserved
IRQ11	Controller 2	Reserved
IRQ12	Controller 2	Reserved
IRQ13	Controller 2	Coprocessor
IRQ14	Controller 2	Fixed Disk Controller
IRQ15	Controller 2	Reserved

### 2.4.2 Direct Memory Access

The system supports 7 DMA channels, using two 8237A-5 DMA controller chips (each chip has four channels, but channel 4 of controller 2 is used to cascade the two DMA chips).

DMA controller 1 contains channels 0 thru 3, and supports 8 bit data transfers between 8 bit I/O adapters and 8 or 16 bit system memory (each channel can transfer data throughout the 16 megabyte system address space in 64 kilobyte blocks).

DMA controller 2 contains channels 5 thru 7, and supports 16 bit data transfers between 16 bit I/O adapters and 16 bit system memory (each channel can transfer data throughout the 16 megabyte system address space in 128 kilobyte blocks, but not on odd byte boundaries).

<u>HEX ADDRESS</u>	<u>COMMAND CODES</u>	<u>DMA CONTROLLER</u>
000	CH0 base and current address	1
002	CH0 base and current word count	1
004	CH1 base and current address	1
006	CH1 base and current word count	1
008	CH2 base and current address	1
00A	CH2 base and current word count	1
00C	CH3 base and current address	1
00E	CH3 base and current word count	1
010	Read Status Reg/Write Command Reg	1
012	Write Request Register	1
014	Write Single Mask Register Bit	1
016	Write Mode Register	1
018	Clear Byte Pointer Flip-Flop	1
01A	Read Temporary Reg/Write Master Clear	1
01C	Clear Mask Register	1
01E	Write All Mask Register	1
0C0	CH4 base and current address	2
0C2	CH4 base and current word count	2
0C4	CH5 base and current address	2
0C6	CH5 base and current word count	2
0C8	CH6 base and current address	2
0CA	CH6 base and current word count	2
0CC	CH7 base and current address	2
0CE	CH7 base and current word count	2
0D0	Read Status Reg/Write Command Reg	2
0D2	Write Request Register	2
0D4	Write Single Mask Register Bit	2
0D6	Write Mode Register	2
0D8	Clear Byte Pointer Flip-Flop	2
0DA	Read Temporary Reg/Write Master Clear	2
0DC	Clear Mask Register	2
0DE	Write All Mask Register	2

## 2.4.2 Direct Memory Access — CONTINUED

Addresses for all DMA channels do not increase or decrease through page boundaries (64 kilobyte for channels 0 thru 3 and 128 kilobyte for channel 5 thru 7). Address generation for DMA channels are as follows in the next table:

PAGE <u>REGISTER</u>	I/O HEX <u>ADDRESS</u>	PAGE <u>ADDRESS</u>	DMA OUTPUT <u>ADDRESS</u>
DMA CHANNEL 0	0087	A23<---->A16	A15<---->A0
DMA CHANNEL 1	0083	A23<---->A16	A15<---->A0
DMA CHANNEL 2	0081	A23<---->A16	A15<---->A0
DMA CHANNEL 3	0082	A23<---->A16	A15<---->A0
DMA CHANNEL 5	008B	A23<---->A17	A16<---->A1
DMA CHANNEL 6	0089	A23<---->A17	A16<---->A1
DMA CHANNEL 7	008A	A23<---->A17	A16<---->A1
REFRESH	008F		

NOTE: For channels 0 thru 3 -- byte high enable (BHE) = A0 inverted  
For channels 5 thru 7 -- BHE and A0 are forced to a logic 0.

## 2.4.3 I/O Decode

The following table is a condensed map of the I/O address map (each address range is expanded within the sections listed under the heading 'SEE SECTION').

<u>HEX RANGE</u>	<u>DEVICE</u>	<u>SEE SECTION</u>
000 - 01F	DMA controller 1 (8237A-5)	2.4.2
020 - 03F	Interrupt controller 1, Master (8259A)	2.4.1
040 - 05F	Timer (8254.2)	2.4.5
060 - 06F	(keyboard) 8042	2.4.7
070 - 07F	Real time clock/NMI mask/(MC146818)	2.4.6
080 - 09F	DMA page register (74LS612)	2.4.4
0A0 - 0BF	Interrupt controller 2 (8259A)	2.4.1
0C0 - 0DF	DMA controller 2 (8237A-5)	2.4.2
0E0 - 0EF	UNDEFINED	
0F0	Clear Math Coprocessor Busy	2.1.3
0F1	Reset Math Coprocessor	2.1.3
0F8 - OFF	Math Coprocessor	2.1.3
100 - 1EF	UNDEFINED	
1F0 - 1F8	Fixed Disk	2.3.1
1F9 - 1FF	UNDEFINED	
200 - 207	Game I/O	2.3.2
278 - 27F	Parallel printer port 2	2.3.3
280 - 2F7	UNDEFINED	
2F8 - 2FF	Serial Port 2	2.3.3
300 - 31F	Prototype card	2.3.6
320 - 35F	UNDEFINED	
360 - 36F	Reserved	
370 - 377	UNDEFINED	
378 - 37F	Parallel printer port 1	2.3.3
380 - 38F	SDLC, bisynchronous 2	2.3.3
390 - 39F	UNDEFINED	
3A0 - 3AF	Bisynchronous 1	2.3.3
3B0 - 3BF	Monochrome Display/Printer Adapter	2.3.4
3C0 - 3CF	Reserved	
3D0 - 3DF	Color/Graphics Monitor Adapter	2.3.5
3E0 - 3EF	UNDEFINED	
3F0 - 3F7	Diskette controller	2.3.1
3F8 - 3FF	Serial port 1	2.3.3

#### 2.4.4 DMA Paged Memory Mapper

The memory mapper is used to expand the DMA's memory address capability by eight bits. Four bits of the memory address are used to select one of 16 map registers that contain 8 bits each. These 8 bits are presented to the system memory address bus through the map output buffers along with the user memory address bits from the DMA. However, addressable memory space without reloading the map registers is the same as would be available with the memory mapper left out. The addressable memory space is increased only by periodically reloading the map registers from the data bus.

The memory mapper has four modes of operation (read, write, map and pass). Data may be read from or loaded into the map register selected by the register select inputs (RS0 thru RS3), under control of R/W\* whenever chip select (CS\*) is low.

#### 2.4.5 System Timers

The system has an INTEL 8254-2 counter/timer chip (three programmable counter/timers in one chip). This chip is a programmable interval counter/timer that system programs treat as an arrangement of four external I/O ports; three ports are treated as counters, and the fourth is a control register for mode programming. The following table describes each channel control and output as follows (NOTE: channel 1 is programmed as a rate generator to produce a 15 microsecond period signal):

CHANNEL	SIGNAL NAME	DESCRIPTION
0		SYSTEM TIMER
0	GATE 0	TIED ON
0	CLK IN 0	1.190 MHz OSC
0	CLK OUT 0	8259A IRQ0
1		REFRESH REQUEST GENERATOR
1	GATE 1	TIED ON
1	CLK IN 1	1.190 MHz OSC
1	CLK OUT 1	REQUEST REFRESH CYCLE
2		TONE GENERATION FOR SPEAKER
2	GATE 2	CONTROLLED BY BIT 0 OF PORT 61H PPI BIT
2	CLK IN 2	1.190 MHz OSC
2	CLK OUT 2	USED TO DRIVE THE SPEAKER

## 2.4.6 Real Time Clock

The MC146818 Real Time Clock combines four features on the chip: a complete time of day clock with alarm (not used), a one hundred year calendar, a programmable periodic interrupt and square wave generator, and 64 bytes of general purpose low power static RAM (this RAM is battery backed up, and 50 bytes of this RAM are available for system configuration programmable uses). The setup program initializes registers A,B,C, and D, when the time and date are set. Interrupt 1A is the BIOS interface to read/set the time and date; it initializes the status bytes the same as the Setup program.

<u>HEX ADDRESS</u>	<u>DESCRIPTION</u>
00	* Seconds
01	* Seconds Alarm
02	* Minutes
03	* Minutes Alarm
04	* Hours
05	* Hours Alarm
06	* Day of the Week
07	* Date of the Month
08	* Month
09	* Year
0A	* Register A
0B	* Register B
0C	* Register C
0D	* Register D
0E	* Diagnostic status byte
0F	* Shutdown status byte
10	Diskette drive type byte - drives A and B
11	Reserved
12	Fixed disk type byte - drives C and D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2 - byte CMOS checksum
30	* Low expansion memory byte
31	* High expansion memory byte
32	* Date century byte
33	* Information flags (set during power on)
34-3F	Reserved

\* These bytes are excluded from the checksum calculation and are not part of the configuration record.

## 2.4.6 Real Time Clock -- CONTINUED

## STATUS REGISTER A

**BIT 7** - a 1 indicates the time update cycle is in progress, and a 0 indicates the current date and time is available to read.

**BITS 6-4** - these bits are used to select the frequency divider stage based on the time base used; 000 selects 4.194304 megahertz, 001 selects 1.048576 megahertz, default 010 selects 32.768 kilohertz time base, 110 and 111 select any frequency, and other combinations are used for test purposes.

**BITS 3-0** - these bits are used to select the frequency divider output as shown in the next table; default 0110 selects 1.024 kilohertz square wave output frequency and a 976.562 microsecond periodic interrupt rate (PIR) for a 32.768 kilohertz time base.

<b>BITS 3-0</b>	<b>TIME BASE CODE 000 OR 001</b>		<b>TIME BASE CODE 010 (DEFAULT)</b>	
	<u>PIR</u>	<u>OUTPUT FREQ</u>	<u>PIR</u>	<u>OUTPUT FREQ</u>
0000	none	none	none	none
0001	30.517 us	32.768 KHz	3,906.250 us	256.000 Hz
0010	61.035 us	16.384 KHz	7,812.500 us	128.000 Hz
0011	122.070 us	8.192 KHz	122.070 us	8.192 KHz
0100	244.141 us	4.096 KHz	244.141 us	4.096 KHz
0101	488.281 us	2.048 KHz	488.281 us	2.048 KHz
0110	976.562 us	1.024 KHz	976.562 us	1.024 KHz
0111	1,953.125 us	512.000 Hz	1,953.125 us	512.000 Hz
1000	3,906.250 us	256.000 Hz	3,906.250 us	256.000 Hz
1001	7,812.500 us	128.000 Hz	7,812.500 us	128.000 Hz
1010	15.625 ms	64.000 Hz	15.625 ms	64.000 Hz
1011	31.250 ms	32.000 Hz	31.250 ms	32.000 Hz
1100	62.500 ms	16.000 Hz	62.500 ms	16.000 Hz
1101	125.000 ms	8.000 Hz	125.000 ms	8.000 Hz
1110	250.000 ms	4.000 Hz	250.000 ms	4.000 Hz
1111	500.000 ms	2.000 Hz	500.000 ms	2.000 Hz

## 2.4.6 Real Time Clock -- CONTINUED

### STATUS REGISTER B

BIT 7 - a 1 aborts any update cycle in progress and the program can initialize the 14 time bytes without any further updates occurring until a 0 is written to this bit (a 0 updates the cycle normally by advancing the counts at one per second).

BIT 6 - is a read/write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in REGISTER A; 1 enables the interrupt, and 0 (default) disables the interrupt.

BIT 5 - a 1 enables the alarm interrupt, and a 0 disables it; system default is 0.

BIT 4 - a 1 enables the update ended interrupt, and a 0 disables it; system default is 0.

BIT 3 - a 1 enables the square wave frequency as set by the rate selection bits in REGISTER A, and a 0 disables it; system default is 0.

BIT 2 - indicated whether the time and date calendar updates are to use binary or binary coded decimal formats; 1 indicates binary, and 0 (default) indicates binary coded decimal.

BIT 1 - establishes whether the hours byte is in the 24 hour or 12 hour mode; 1 indicates the 24 hour mode, and 0 indicates the 12 hour mode (default is 0).

BIT 0 - a 1 enables daylight savings, and a 0 disables daylight savings (standard time); system default is 0.

### STATUS REGISTER C

BITS 7-4 - are flag bits (IRQF, PF, AF, UF in descending order) which are read only, but are updated when bits 6-4 of REGISTER B are enabled.

BITS 3-0 - are RESERVED.

### STATUS REGISTER D

BIT 7 - is a read only bit, which is updated when the real time clock has lost power; 1 indicates power on the real time clock, and 0 indicates that the real time clock has lost power.

BITS 6-0 - are RESERVED.

#### 2.4.6 Real Time Clock -- CONTINUED

##### DIAGNOSTIC STATUS BYTE

BIT 7 - indicates loss of power on the real time clock when 1, and a 0 indicates that the chip has not lost power.

BIT 6 - is a checksum status indicator; 0 indicates that the checksum is good, and 1 indicates it is bad.

BIT 5 - is a check, at power on time, of the equipment byte of the configuration record; 0 indicates that the configuration information is valid, and 1 indicates it is invalid. Note: power on checks require at least one diskette drive to be installed (bit 0 of the equipment byte set to 1), and the actual display hardware in the system (primary display adapter setting in the configuration record matches the system board's display switch setting).

BIT 4 - a 1 indicates, that the power on check determined the memory size is different from the configuration record, and a 0 indicates a memory size match.

BIT 3 - a 0 indicates that the adapter and drive are functioning properly and the system can attempt a boot up, however, a 1 indicates that the adapter and/or drive C failed initialization, preventing the system from attempting a boot up.

BIT 2 - is a post validity check; 0 indicates that the time is valid, and 1 indicates that the time is invalid.

BITS 1 and 0 - are RESERVED.

##### SHUTDOWN STATUS BYTE

The bits in this byte are defined by the power on diagnostics in the BIOS Listing.

##### DISKETTE DRIVE TYPE BYTE

BITS 7-4 - indicate type of first diskette drive installed; 0000 = no drive is present, 0001 = double sided diskette drive (48 TPI), 0010 = high capacity diskette drive (96 TPI), and 0011 thru 1111 are reserved.

BITS 3-0 - indicate type of second diskette drive installed; 0000 = no drive is present, 0001 = double sided diskette drive (48 TPI), 0010 = high capacity diskette drive (96 TPI), and 0011 thru 1111 are reserved.

## 2.4.6 Real Time Clock -- CONTINUED

## FIXED DISK TYPE BYTE

**BITS 7-4** - indicate type of first fixed disk drive (drive C) installed; 0000 = no drive is present, 0001 thru 1111 = define type 1 thru type 15 (15 is reserved and set to 0) of fixed disk drive.

**BITS 3-0** - indicate type of second fixed disk drive (drive D) installed; 0000 = no drive is present, 0001 thru 1111 = define type 1 thru type 15 (15 is reserved and set to 0) of fixed disk drive.

<u>TYPE</u>	<u>CYLINDERS</u>	<u>HEADS</u>	<u>WRITE PRE-COMP</u>	<u>LANDING ZONE</u>
1	306	4	128	305
2	615	4	300	615
3	615	6	300	615
4	940	8	512	940
5	940	6	512	940
6	615	4	NONE	615
7	462	8	256	511
8	733	5	NONE	733
9	900	15	NONE	901
10	820	3	NONE	820
11	855	5	NONE	855
12	855	7	NONE	855
13	306	8	128	319
14	733	7	NONE	733
15	---	-	---	---

## EQUIPMENT BYTE

**BITS 7-6** - indicate the number of diskette drives installed; 00 = 1 drive, 01 = 2 drives, and 10 and 11 are reserved.

**BITS 5-4** - indicate primary display; 00 = reserved, 01 = primary display is attached to the color/graphics monitor adapter in the 40 column mode, 10 = primary display is attached to the color/graphics monitor adapter in the 80 column mode, and 11 = primary display is attached to the monochrome display and printer adapter.

**BITS 3-2** - not used.

**BIT 1** - indicates if the math coprocessor is present; 0 = not installed, and 1 = installed.

**BIT 0** - indicates if diskette drives are installed if set.

#### 2.4.6 Real Time Clock -- CONTINUED

##### LOW AND HIGH BASE MEMORY BYTES (15H and 16H)

**BITS 7-0** - of 15H indicates low byte base size, and 16H indicates high byte base size; valid sizes 0100H = 256 kilobytes of system RAM, 0200H = 512 kilobytes of system RAM, and 0280H = 640 kilobytes 512 kilobytes if system RAM and the IBM-AT 128 kilobyte memory expansion option.

##### LOW AND HIGH MEMORY EXPANSION BYTES (17H and 18H)

**BITS 7-0** - of 17H indicates low byte base size, and 18H indicates high byte base size; valid sizes 0200H = 512 kilobytes I/O adapter RAM, 0400H = 1024 kilobytes I/O adapter RAM (2 adapter cards), and 0600H to 3C00H = 1536 kilobytes I/O adapter (3 adapters) to 15360 kilobytes I/O adapter (15 megabytes maximum).

##### CHECKSUM BYTES (2EH and 2FH)

**BITS 7-0** - of 2EH indicates low byte of CHECKSUM, and 2FH indicates high byte of CHECKSUM.

##### LOW AND HIGH EXPANSION MEMORY BYTES (30H and 31H)

**BITS 7-0** - of 30H indicates low byte expansion size, and 31H indicates high byte expansion size; valid sizes 0200H = 512 kilobytes I/O adapter RAM, 0400H = 1024 kilobytes I/O adapter RAM (2 adapter cards), and 0600H to 3C00H = 1536 kilobytes I/O adapter (3 adapters) to 15360 kilobytes I/O adapter (15 megabytes maximum).

##### DATE CENTURY BYTE

**BITS 7-0** - indicate BCD value for the century (BIOS interface to read and set).

##### INFORMATION FLAG BYTE

**BIT 7** - if set indicates IBM-AT 128 kilobyte memory expansion option is installed.

**BIT 6** - is used by the setup utility to put out a first used message after initial setup.

**BITS 5-0** - are RESERVED.

#### 2.4.7 Keyboard Control

The keyboard controller is a single-chip microcomputer (INTEL 8042), which is programmed to be IBM-AT keyboard compatible, with a serial interface. This controller communicates with the keyboard through the status register, an input buffer, and an output buffer; the controller has two byte wide I/O ports and two test inputs (the test inputs are used to read the state of the clock line and the data line).

The keyboard controller receives serial data from the keyboard, checks the parity of the data, translates scan codes, and presents the data to the system as a byte of data in its output buffer; the controller will interrupt the CPU when data is placed in its output buffer.

Data is sent to the keyboard by writing to the keyboard controller's input buffer (the status register contains bits that indicate if an error was detected while receiving the data). Bytes of data are serialized and sent to the keyboard, with odd parity bits automatically inserted; the keyboard is required to acknowledge all data transmissions, and the acknowledgment separates byte transmissions.

The keyboard sends serial format data to the controller, using an 11 bit frame (data sent is synchronized by a clock supplied by the keyboard); the first bit is a start bit, and is followed by eight data bits, an odd parity bit, and a stop bit. At the end of a transmission, the keyboard controller disables the interface until the system accepts the byte. For a received byte of data with a parity error, a resend command is automatically sent to the keyboard. Whenever the keyboard controller is unable to receive the data correctly, FFH is placed in its output buffer, and the parity bit in the status register is set to 1, indicating a receive parity error. The keyboard controller will also time a byte of data from the keyboard, and if the byte transmission does not end within 2 milliseconds, FFH is placed in the keyboard controller's output buffer, and the receive time out bit in the status register is set (no retries will be attempted on a receive time out error).

For scan codes, which are received from the keyboard, the keyboard controller converts these codes to system scan codes before they are put into the controller's output buffer.

Data is sent to the keyboard in the same serial format used to receive data from the keyboard; a parity bit is automatically inserted by the keyboard controller. If the keyboard does not start clocking the data out of the keyboard controller within 15 milliseconds, or completes that clocking within 2 milliseconds, FEH is placed in the keyboard controller's output buffer, and the transmit time out error bit is set in the status register. If the response contains a parity error, FEH is placed in the keyboard controller's output buffer, and the transmit time out and parity error bits are set in the status register. The keyboard controller is programmed to a set time limit for the keyboard to respond; if 25 milliseconds are exceeded, the keyboard controller places FEH in its output buffer and sets the transmit an receive time out error bits in the status register (no retries are made by the keyboard controller for any transmission error).

## 2.4.7 Keyboard Control -- CONTINUED

The following figure shows the conversion between scan codes, and the key relation on the keyboard.

<u>KB SCAN CODE</u>	<u>SYSTEM SCAN CODE</u>	<u>KEY</u>	<u>KEY DESCRIPTION</u>
00	FF		
76	01	90	ESC
16	02	2	! or 1
1E	03	3	@ or 2
26	04	4	# or 3
25	05	5	\$ or 4
2E	06	6	% or 5
36	07	7	^ or 6
3D	08	8	& or 7
3E	09	9	* or 8
46	0A	10	( or 9
45	0B	11	) or 0
4E	0C	12	_ or -
55	0D	13	+ or =
66	0E	15	backspace
0D	0F	16	tab function
15	10	17	Q or q
1D	11	18	W or w
24	12	19	E or e
2D	13	20	R or r
2C	14	21	T or t
35	15	22	Y or y
3C	16	23	U or u
43	17	24	I or i
44	18	25	O or o
4D	19	26	P or p
54	1A	27	{ or [
5B	1B	28	} or ]
5A	1C	43	carriage return
14	1D	30	Cntl
1C	1E	31	A or a
1B	1F	32	S or s
23	20	33	D or d
2B	21	34	F or f
34	22	35	G or g
33	23	36	H or h
3B	24	37	J or j
42	25	38	K or k
4B	26	39	L or l
4C	27	40	: or ;
52	28	41	" or "
0E	29	1	- or `
12	2A	44	shift
5D	2B	14	\ or \
1A	2C	46	Z or z
22	2D	47	X or x

## 2.4.7 Keyboard Control -- CONTINUED

<u>KB SCAN CODE</u>	<u>SYSTEM SCAN CODE</u>	<u>KEY</u>	<u>KEY DESCRIPTION</u>
21	2E	48	C or c
2A	2F	49	V or v
32	30	50	B or b
31	31	51	N or n
3A	32	52	M or m
41	33	53	< or ,
49	34	54	> or .
4A	35	55	? or /
59	36	57	shift
7C	37	106	PrtSc or *
11	38	58	Alt
29	39	61	space
58	3A	64	Caps Lock
05	3B	70	F1
06	3C	65	F2
04	3D	71	F3
0C	3E	66	F4
03	3F	72	F5
0B	40	67	F6
02 or 83	41	73	F7
0A	42	68	F8
01	43	74	F9
09	44	69	F1
77	45	95	Num Lock
7E	46	100	Scroll Lock or Break
6C	47	91	7 or Home
75	48	96	8 or up cursor
7D	49	101	9 or Pg Up
7B	4A	107	-
6B	4B	92	4 or left cursor
73	4C	97	S
74	4D	102	6 or right cursor
79	4E	108	+
69	4F	93	1 or End
72	50	98	2 or down cursor
7A	51	103	3 or Pg Dn
70	52	99	0 or INS
71	53	104	. or DEL
7F or 84	54	105	SYS REQ
60	55	R	reserved
61	56	R	reserved
78	57	R	reserved
07	58	R	reserved
0F	59	R	reserved
17	5A	R	reserved
1F	5B	R	reserved
27	5C	R	reserved
2F	5D	R	reserved

## 2.4.7 Keyboard Control -- CONTINUED

<u>KB SCAN CODE</u>	<u>SYSTEM SCAN CODE</u>	<u>KEY</u>	<u>KEY DESCRIPTION</u>
37	5E	R	reserved
3F	5F	R	reserved
47	60	R	reserved
4F	61	R	reserved
56	62	R	reserved
5E	63	R	reserved
08	64	R	reserved
10	65	R	reserved
18	66	R	reserved
20	67	R	reserved
28	68	R	reserved
30	69	R	reserved
38	6A	R	reserved
40	6B	R	reserved
48	6C	R	reserved
50	6D	R	reserved
57	6E	R	reserved
6F	6F	R	reserved
13	70	R	reserved
19	71	R	reserved
39	72	R	reserved
51	73	R	reserved
53	74	R	reserved
5C	75	R	reserved
5F	76	R	reserved
62	77	R	reserved
63	78	R	reserved
64	79	R	reserved
65	7A	R	reserved
67	7B	R	reserved
68	7C	R	reserved
6A	7D	R	reserved
6D	7E	R	reserved
6E	7F	R	reserved

## 2.4.8 Speaker

The system unit has a 2.25 inch permanent magnet speaker which can be driven from: the I/O port output bit, the counter/timer clock out, or both.

## 3.0 INTERFACE REQUIREMENTS

## 3.1 System I/O (AT) Bus

This section identifies the I/O interface requirements for both the PC compatible option cards and the AT compatible option cards. Out of the 8 expansion slots available, only 2 are reserved for PC compatibility; all 8 slots have a 62 pin connector socket, and 6 have an additional 36 pin connector socket (used on AT compatible cards only).

## 3.1.1 PC Interface Compatibility

The following connector pin assignment is used on both the PC and AT option slots; this connector socket has 62 pins.

PIN	SIGNAL NAME	I/O	PIN	SIGNAL NAME	I/O
A1	-I/O CH CK	I	B1	GND	GROUND
A2	SD7	I/O	B2	RESET DRV	I
A3	SD6	I/O	B3	+5 VDC	POWER
A4	SD5	I/O	B4	IRQ9	I
A5	SD4	I/O	B5	-5 VDC	POWER
A6	SD3	I/O	B6	DRQ2	I
A7	SD2	I/O	B7	-12 VDC	POWER
A8	SD1	I/O	B8	OWS	I
A9	SD0	I/O	B9	+12 VDC	POWER
A10	-I/O CH RDY	I	B10	GND	GROUND
A11	AEN	O	B11	-SMEMW	I
A12	SA19	I/O	B12	-SMEMR	I
A13	SA18	I/O	B13	-IOW	I/O
A14	SA17	I/O	B14	-IOR	I/O
A15	SA16	I/O	B15	-DACK3	I
A16	SA15	I/O	B16	DRQ3	I
A17	SA14	I/O	B17	-DACK1	I
A18	SA13	I/O	B18	DRQ1	I
A19	SA12	I/O	B19	-REFRESH	I/O
A20	SA11	I/O	B20	CLK	I
A21	SA10	I/O	B21	IRQ7	I
A22	SA9	I/O	B22	IRQ6	I
A23	SA8	I/O	B23	IRQ5	I
A24	SA7	I/O	B24	IRQ4	I
A25	SA6	I/O	B25	IRQ3	I
A26	SA5	I/O	B26	-DACK2	I
A27	SA4	I/O	B27	T/C	I
A28	SA3	I/O	B28	BALE	I
A29	SA2	I/O	B29	+5 VDC	POWER
A30	SA1	I/O	B30	OSC	I
A31	SA0	I/O	B31	GND	GROUND

### 3.1.2 AT Interface Compatibility

The following connector pin assignment is used on the AT compatible option slots only; this connector socket has 36 pins.

<u>PIN</u>	<u>SIGNAL NAME</u>	<u>I/O</u>	<u>PIN</u>	<u>SIGNAL NAME</u>	<u>I/O</u>
C1	SBRE	I/O	D1	-MEM CS16	I
C2	LA23	I/O	D2	-I/O CS16	I
C3	LA22	I/O	D3	IRQ10	I
C4	LA21	I/O	D4	IRQ11	I
C5	LA20	I/O	D5	IRQ12	I
C6	LA19	I/O	D6	IRQ15	I
C7	LA18	I/O	D7	IRQ14	I
C8	LA17	I/O	D8	-DACK0	O
C9	-MEMR	I/O	D9	DRQ0	I
C10	-MEMW	I/O	D10	-DACK5	O
C11	SD08	I/O	D11	DRQ5	I
C12	SD09	I/O	D12	-DACK6	O
C13	SD10	I/O	D13	DRQ6	I
C14	SD11	I/O	D14	-DACK7	O
C15	SD12	I/O	D15	DRQ7	I
C16	SD13	I/O	D16	+5 VDC	POWER
C17	SD14	I/O	D17	-MASTER	I
C18	SD15	I/O	D18	GND	GROUND

### 3.1.3 System I/O (AT) Bus Signal Description

The following signal descriptions for the System I/O Bus, are for both PC and AT compatible option cards (differentiation is presented in the compatibility sections above). Note, that all signal lines are TTL compatible levels, and that I/O adapters should be designed with a maximum of two low power Shottky (LS) loads per line.

\* **CLK** -- (clock) signal (8 megahertz, 50 % duty cycle signal) is used only for synchronization, and is not intended for uses requiring a fixed frequency.

\* **SA0 thru SA19** -- are 20 address lines used to address memory and I/O devices within the system. They are gated on the system bus when the signal 'BALE' is high and are latched on the falling edge of 'BALE'. Generation of these signals are by the CPU or a DMA controller, but other microprocessors or DMA controller that reside on the bus may drive the address lines.

\* **LA17 thru LA23** -- signals (unlatched) are used in conjunction with SA0 thru SA19 to address memory and I/O devices within the system; they give the system up to 16 megabytes of addressability (Validity of these signals are when 'BALE' is high; they are not latched during CPU cycles, and therefore do not stay valid for the whole cycle). Their main purpose is to generate memory decodes for 1 wait-state memory cycles; the decodes should be latched by I/O adapter on the falling edge of 'BALE'. These signals may be driven by other microprocessors or DMA controllers that reside on the bus.

\* **BALE** (buffered) -- is an address latch enable generated by the 82288 bus controller; it is used to latch valid addresses and memory decodes from the CPU, and is used as a valid CPU or DMA (forced high during DMA cycles) address indicator, in conjunction with AEN.

\* **AEN** -- (address enable) is used to remove the CPU and other devices from the bus to allow DMA transfers to take place. During AEN active, the DMA controller has control of the address bus, the data bus READ command lines, and the WRITE command lines.

\* **S00 thru S015** -- signals provide bus bits 0 thru 15 for the CPU, memory and I/O devices (D0 is the least significant bit and D15 is the most significant bit). All 8-bit devices on the bus should use D0 thru D7 for communications to the CPU (D8 thru D15 will be gated to D0 thru D7 during transfers to these devices, to provide 2 byte wide transfers per 16-bit transfer), while 16-bit devices will use D0 thru D15.

\* **RESET DRV** -- signal (active high) is used to reset or initialize the system logic during power-up time, or during a low line voltage outage.

## 3.1.3 System I/O (AT) Bus Signal Description -- CONTINUED

\* -I/O CH CK -- signal indicates an uncorrectable system error when active. The -I/O channel check provides the system board with parity information about memory or devices on the bus.

\* I/O CH RDY -- signal is used to lengthen I/O or memory cycles when driven low by the active device (this signal should not be held low for more than 2.5 microseconds). Any slow device using this line should drive it low immediately upon detecting its valid address and a READ or WRITE command.

\* IRQ3 THRU IRQ15 -- signals (active high, and must remain high until the CPU acknowledges it) are used to signal the CPU that an I/O device needs attention (these interrupt requests are prioritized in descending order 9 thru 15, and 3 thru 7). Interrupt 13 is used on the system board and is not available on the bus, and interrupt 8 is used for the real time clock.

\* -IOR -- is a read signal (active low) that instructs an I/O device to drive its data onto the data bus. This line may be driven by the CPU or the DMA controller resident on the bus.

\* -IOW -- is a write signal (active low) that instructs an I/O device to read the data bus. This line may be driven by the CPU or the DMA controller resident on the bus.

\* -MEMR -- memory read signal (active low) is active on all memory read cycles (may be driven by any microprocessor or DMA in the system), and instructs the memory devices to drive data onto the data bus. The address lines must be valid on the bus for one system clock period before driving this signal active.

\* -SMEMR -- is an active signal (active low) only when the memory decode is within the low 1 megabyte range. This signal is derived from the '-MEMR' signal active and the decode of the low 1 megabyte of memory.

\* -MEMW -- memory write signal (active low) is active on all memory read cycles (may be driven by any microprocessor or DMA in the system), and instructs the memory devices to store present data onto the data bus. The address lines must be valid on the bus for one system clock period before driving this signal active.

\* -SMEMW -- is an active signal (active low) only when the memory decode is within the low 1 megabyte range. This signal is derived from the '-MEMR' signal active and the decode of the low 1 megabyte of memory.

## 3.1.3 System I/O (AT) Bus Signal Description -- CONTINUED

\* **DRQ0 THRU DRQ7** -- DMA requests are asynchronous, and are used by peripheral devices to gain DMA service or control of the system; they are prioritized in descending order from DRQ0 thru DRQ7. A request is generated by driving a DRQ line active high, and holding it until the corresponding DACK (acknowledge line) signal goes active. DRQ0 thru DRQ3 will perform 8 bit transfers, and DRQ5 thru DRQ7 will perform 16 bit transfers; DRQ4 is used on the system board and is not available on the bus.

\* **DACK0 THRU DACK7** -- DMA acknowledge signals (active low) are used to acknowledge DMA requests (DRQ0 thru DRQ7); DACK4 is used on the system board and is not available on the bus.

\* **REFRESH** -- signal is used to indicate a refresh cycle, and can be driven by a microprocessor on the bus.

\* **T/C** -- terminal count signal provides a pulse when the terminal count for any DMA channel is reached.

\* **SBHE** -- system bus high enable indicates data transfer on the upper byte of the data bus (SD8 thru SD15); 16 bit devices use this signal to condition data bus buffers tied to SD8 thru SD15.

\* **-MASTER** -- signal is used in conjunction with a DRQ line to gain control of the system; if this signal is held low for more than 15 microseconds, system memory may be lost because of a lack of refresh. A processor or DMA controller on the bus may issue a DRQ to a DMA channel in cascade mode and receive a '-DACK'; reception of the '-DACK' will allow the microprocessor to pull the '-MASTER' line low, which will allow it to control the system address, data, and control lines (condition known as tri-state). After '-MASTER' is low, the processor must wait one system clock period before driving the address and data lines, and two clock periods before issuing a READ or WRITE command.

\* **-MEM CS16** -- (not) memory 16 bit chip select (derived from the decode of LA17 thru LA23), signals the system board if the present data transfer is a 1 wait-state, 16 bit, memory cycle. Note, this signal is active low, and should be driven with an open collector or tri-state driver capable of sinking 20 milliamperes of current.

\* **-I/O CS16** -- (not) I/O 16 bit chip select (derived from an address decode), signals the system board that the present data transfer is a 16 bit, 1 wait-state, I/O cycle. Note, this signal is active low, and should be driven with an open collector or tri-state driver capable of sinking 20 milliamperes of current.

\* **OSC** -- oscillator signal is a high speed clock with a 70 nanosecond period (14.31818 megahertz), asynchronous with the system clock, and has a 50 % duty cycle.

## 3.1.3 System I/O (AT) Bus Signal Description -- CONTINUED

\* OWS -- signal indicates to the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16 bit device without wait cycles, the 'OWS' signal is derived from an address decode gated with a READ or WRITE command. In order to run a memory cycle to an 8 bit device with a minimum of two wait states, the 'OWS' signal is driven active one system clock after the READ or WRITE command is active gated with the address decode for the device (memory read and write commands to an 8 bit device are active on the falling edge of the system clock). Note, this signal is active low, and should be driven with an open collector or tri-state driver capable of sinking 20 milliamperes of current.

THEORY OF OPERATION

TANDY MODEL 3000 COMPUTER  
MAIN LOGIC BOARD ASSEMBLY



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III)	PCB LAYOUT AND SILKSCREEN	



## 1.0 DETAILED DESIGNS

### 1.1 Clock Circuits

The system clock logics are derived from the INTEL 82284 chip (U42, sheet 4 of the schematics). This device uses an external 16MHZ parallel resonant, fundamental mode crystal, Y2, which is the source of all system timing. This clock, called PRCLK, is synchronized with processor status signal S1 by U36/A (sheet 3), and is then divided by two to 8MHz by U29/A which provides the system and peripheral clocks called SCLK(H) and SCLK(L). PCLK(H) and PCLK(L) are also derived by dividing the PRCLK by two but they are not synchronized with S1. PCLK(H) and PCLK(L) are the 8042 CPU (U6, sheet 12) clocks which require a clocked setup time prior to reset going away. The processor status signal S1 is valid after reset and so cannot be used to synchronize the 8042 clock. The DMA clock, signal DMACLK, is derived by dividing the SCLK by two to 4MHz.

An 8284 INTEL clock device (U47, sheet 3) provides two clocks which are not synchronous to any of the above clocks. One of the clocks is the OSC clock used by the I/O channel only which has a period of 70ns (14.31818 MHZ). The other clock is derived by dividing the 8284 osc output by two to 1.19MHz and is used for the system timer chip (8253, U4, sheet 11). The CMOS real time clock controller uses a 32.768KHZ crystal (Y1, sheet 11) configured with a CMOS driver.

### 1.2 Wait State and Conversion Control

These logics allow compatibility with 8-bit PC type option boards using 8 or 16-data bit CPU instructions.

All 8-bit data references to 8-bit devices have four wait states inserted, resulting in a 1000-nanosecond microprocessor cycle (assuming 8MHz CPU). CPU odd memory byte location references (BHE active low and A0 inactive high) to 8-bit devices are transferred onto the upper eight bit data bus D8-D16 for a read command and the lower eight bit data bus D0-D8 for a write command cycle.

All 16-bit CPU references to 8-bit devices have 10 wait states inserted, resulting in a 2000-nanosecond microprocessor cycle time. During a CPU read operation the hardware allows transfers of the first 8 data bits through a normal CPU cycle with four wait states inserted; these first 8-bits are latched and held in the 74ALS646 bus transceiver (U82, sheet 4) until the second eight data bits are transferred. The second eight bit transfer continues to wait the CPU by inserting four more wait states. The 82288 bus controller (U49, sheet 9) is temporarily tri-stated to end the first transfer and then released to allow regeneration of the control signals for the second transfer. The second transfer gates the next lower eight bits onto the upper data bus bits D8 - D16, and then releases the CPU to complete the cycle. A similar process takes place for a CPU write operation except data is transferred from the CPU's upper eight bit data bus onto the lower eight bit data bus during the second write cycle.

## 1.2 Wait State and Conversion Control (continued)

Following are the equations for the 16L8A PAL which senses and controls the transfer logics:

```
/*********************************************
/* Allowable Target Device Types: 16L8          */
/********************************************

/** Inputs **/

PIN 1 = RAS ; /* MEMORY READ OR WRITE */
PIN 2 = !MWT ; /* MEMORY WRITE */
PIN 3 = !IOR ; /* I/O READ */
PIN 4 = AIOW ; /* I/O WRITE */
PIN 5 = Q1 ; /* ONE WAIT STATE */
PIN 6 = !IOS16 ; /* 16-BIT DATA PATH (I/O) */
PIN 7 = !AEN1 ; /* DMA CNTRL 1 ENABLED */
PIN 8 = !AEN2 ; /* DMA CNTRL 2 ENABLED */
PIN 9 = Q4 ; /* FOUR WAIT STATES */
PIN 11 = SYS16 ; /* 16-BIT DATA PATH (MEMORY) */
PIN 13 = !RESOWS ; /* RESET OR NO WAIT STATES */

/** Outputs **/

PIN 12 = !END ; /* RESET READY LOGICS */
PIN 14 = !DMAEN ; /* AEN1 OR AEN2 */
PIN 15 = !XAO ; /* BUFFERED ADDRESS */
PIN 16 = !XBHE ; /* BUFFERED ADDRESS SELECT */
PIN 17 = !GATE ; /* DO-D7 TO D8-D15 OR VICE VERSA */
PIN 18 = !DIR ; /* DIR OF DATA DURING GATE */
PIN 19 = !CONV ; /* 16-BIT DATA TO/FROM 8-BIT DATA*/

/** Declarations and Intermediate Variable Definitions **/

/** Logic Equations **/


CONV = RAS & Q1 & XBHE & XAO & !AEN1 & !AEN2 & !SYS16 #
      IOR & Q1 & XBHE & XAO & !AEN1 & !AEN2 & !IOS16 #
      AIOW & Q1 & XBHE & XAO & !AEN1 & !AEN2 & !IOS16;

DIR = !MWT & RAS & AEN1 #
      MWT & XBHE & !AEN1 & !AEN2 #
      AIOW & XBHE & !AEN1 & !AEN2;

GATE = MWT & XBHE & !XAO & !AEN1 & !AEN2 & !SYS16 #
      RAS & XBHE & AEN1 & SYS16 #
      RAS & XBHE & !XAO & !AEN1 & !AEN2 & !SYS16 #
      IOR & !IOS16 & !AEN1 & !AEN2 & !XAO & XBHE #
      AIOW & !IOS16 & !AEN1 & !AEN2 & !XAO & XBHE #
      IOR & AEN1 & !IOS16 & XBHE;
```

## 1.2 Wait State and Conversion Control (continued)

```
XBHE = !XA0 & AEN1 # AEN2;  
XBHE.OE= DMAEN;  
  
XA0 = AEN2;  
XA0.OE = AEN2;  
  
DMAEN = AEN1 #  
AEN2;  
  
END = RAS & RESOWS #  
AIOW & RESOWS #  
Q4 #  
IOR & Q1 & IOS16 #  
AIOW & Q1 & IOS16 #  
RAS & Q1 & SYS16;
```

### 1.3 Shut Down Control

Shutdown occurs when a severe error is detected that prevents further instruction processing by the CPU. The shutdown logics (U57/A, U45/A/B, U46/B, U23/A, U35/D, sheet 3) decode a shutdown condition only (See INTEL 80286 Hardware Reference Manual for halt conditions). A shutdown bus operation is detected when S1, S0, A1 and COD/INTA are low and M/I/O is high. Upon detecting this condition the hardware resets the CPU only using signal RESCPU, thereby allowing all other hardware (including memory) to retain their previous values.

### 2.0 80286 Local Bus

#### 2.1 82288 Bus Controller

This 20-pin dip (U42, sheet 4) is used to provide address latch control, and command outputs based on the 80286 status lines. The INTEL Hardware Reference manual contains the functional description. The use of this device in the TANDY Model 3000 project differs from the INTEL spec in that CEN/AEN is used in conjunction with the conversion logics to tri-state the 82288 outputs during the second half cycle of a eight-bit to 16-bit transfer. The outputs are also tri-stated during a DMA transfer by asserting the MB pin high.

#### 2.2 80287 Numeric Processor Extension

The 80287 (U78, sheet 4) operates at 1/3 the frequency of the microprocessor clock. It is configured as an I/O device having ports 00F8h, 00FAh, and 00FCh. A 16L8A PAL device (U70, sheet 4) is used to interface the 80287 to the CPU. This PAL provides the I/O decode [NPCS(L)], the 80287 Reset, the 286BUSY signal, and Interrupt Request 13.

```
*****  
/* Allowable Target Device Types:16L8 */  
*****  
  
/** Inputs **/  
  
PIN 1 =RESET ; /* */  
PIN 2 =!ERROR ; /* */  
PIN 3 =!BUSY ; /* */  
PIN 4 =XA0 ; /* */  
PIN 5 =XA3 ; /* */  
PIN 6 =!XLOW ; /* */  
PIN 7 =SMIO ; /* */  
PIN 8 =!CS287 ; /* */  
PIN 9 =!INTA ; /* */
```

## 2.2 80287 Numeric Processor Extension (continued)

```
/** Outputs */
PIN 12 =!NPCS ; /* */
PIN 13 =L ; /* */
PIN 14 =M ; /* */
PIN 15 =N ; /* */
PIN 16 =O ; /* */
PIN 17 =287RESET ; /* */
PIN 18 =IRQ13 ; /* */
PIN 19 =!287BUSY ; /* */

/** Declarations and Intermediate Variable Definitions **/

/** Logic Equations */
NPCS = XA3 & CS287 & !SMIO & !INTA;
!IRQ13 = !ERROR #
        !BUSY & !IRQ13;
!287RESET = !RESET & SMIO #
            !RESET & XA3 #
            !RESET & !XA0 #
            !RESET & !XIOW #
            !RESET & !CS287 #
            !RESET & INTA;
287BUSY = BUSY #
        !N;
!N = O & !N & !M #
        L;
!M = O & !M #
        L #
        !IRQ13;
!L = !O #
        M & !L #
        !IRQ13;
!O = 287RESET #
        !XA3 & !XIOW & !SMIO & CS287 & !INTA;
```

## 3.0 Local Memory Bus

## 3.1 Memory Decode Prom

Memory is decoded with the use of a 512 x 8 byte 28S42 PROM. (U63, sheet 7). The data outputs are latched through a 74LS573 (U64, sheet 7) by either ALE or HLDA(H). The inputs to the PROM include A17 thru A23, RFRSH(H), and RAMSEL(L). Address bits A17 thru A23 allow a decode resolution to 128KB to allow a memory configuration of 0-640KB. The RAMSEL(L) signal allows an upgrade option of 128KB from 512K-640KB when asserted low. Asserted high allows only 512KB. The RFRSH(H) signal asserts RAS0, RAS1, Fl6, and MEGCS(L) in order to refresh all memory in the system in parallel. Fl6 is used to signify a 16-bit data width and that no command delays are needed. MEGCS(L) drives the SMWT and SMRD control signals onto the peripheral bus during the low one megabyte range only.

The following table includes the CPU address translated to the PROM address, the data values of the PROM at those address's and the function of the data values:

CPU ADDR	PROM ADDR	DATA	FUNCTION
000000-07FFFF	000-003	91H	0-512K MEMORY
080000-09FFFF	004	61H	512K-640K MEMORY
0A0000-0DFFFF	005-006	37H	PERIPHERAL MEMORY
0E0000-0FFFFFF	007	30H	PROM
FE0000-FFFFFFF	07F	30H	PROM
000000-07FFFF	100-103	91H	0-512K MEMORY
080000-0DFFFF	104-106	37H	LOW MEG CS ONLY
0E0000-0FFFFFF	107	30H	PROM
FE0000-FFFFFFF	17F	30H	PROM
000000-000100	180	FlH	REFRESH & LOW MEG CS
000000-000100	080	FlH	REFRESH & LOW MEG CS

All remaining PROM address space must be programmed with a data value of 3FH.

The following table is a bit definition of the 28S42 ROM outputs. The active output polarities are indicated with (H) for active high state or (L) for active low.

D7	RAS0(H)
D6	RAS1(H)
D5	CAS0(L)
D4	CAS1(L)
D3	LOW MB MEMORY(L)
D2	MEMORY SELECT(L)
D1	16-BIT DATA(L)
D0	ROM SELECT(L)

### 3.2 ROM Subsystem

There are four ROM modules on the main PCB. Two are used for the BIOS and two are left for optional expansion. The basic configuration is jumper selected for 27128K-bit (16K by 8 bits) ROM's occupying U59 and U61 (sheet 6). In this configuration the jumpers are placed between E5 & E9 and E7 & E11 (sheet 6) and use address A15 to select between the BIOS ROM's or the optional ROM. The BIOS ROM starting address location is 0E8000H or FE8000H while the optional starting address location is 0E0000H or FE0000H.

To expand to 27256K-bit (32K by 8 bit) ROM's requires the jumpers to be placed between E6 & E10, and E8 & E12. This places the starting locations of the ROM's to 0F0000H or FF0000H for the BIOS and 0E0000H or FE0000H for the optional ROM.

NOTE: All four ROM modules must be of the same type i.e., four 27128's or four 27256's.

The maximum Rom access time is calculated as follows:

375ns	cycle time
-	0ns CPU address delay
-	78ns ALE
-	20ns ALS573 output from ALE (sheet 7)
-	11ns ALS04
-	8ns AL500 to chip select on the ROM's
-	10ns data thru ALS245 (sheet 6)
-	10ns data thru ALS245 (sheet 4)
-	10ns CPU data setup time
-	27ns bus capacitance
201ns	ROM access (NOTE: address decode determines access time separate from mem read. Memory read controls output enable)

### 3.3 RAM Subsystem

The decoding for the RAM is explained in section 3.1. The control logics uses a 200ns, 40ns/step, 5-tap delay line (U67,sheet 7) along with the decode, XAO and XBHE. The two RAS's (one per bank) are the "OR" condition of the memory read or memory write control lines "AND'd" with a valid decode. CAS is asserted 80ns after RAS and steered to a row of DRAM with a valid range decode, XBHE and XAO. There are four CAS's, each controlling a 9-bit memory array. The total RAS time is 200ns, and CAS time is 120ns. RAS precharge time is 175ns. Refresh occurs every 15us under a CPU hold cycle (sheet 12) by driving the memory read control line (sheet 9) qualified with a valid RFRSH request. CAS is not asserted during refresh.

### 3.4 Parity Control

The parity control logics is located on sheet 7 of the schematics. These logics consist of four DRAM chips (U99, U108, U117, U126) and two 74F280 parity generator/checker devices (U62, U71) which outputs are selected by XAO or XBHE. A valid memory cycle is selected by OR'ing the CAS decode output lines allowing parity to be latched in a 74F74 flip-flop (U26/A) with XMRD. The parity DRAM control is accomplished with the same timing as explained in section 3.3.

#### 4.0 Buffered Peripheral Bus

##### 4.1 System Interrupts

Two cascaded 8259 interrupt controller chips (U2 and U3, sheet 11) along with the CPU NMI provide 16 levels of interrupts. The 8259's prioritize all incoming interrupts, interrupt the CPU and respond to a CPU interrupt acknowledge by placing a vectored address on the data bus. The CPU interrupt acknowledge cycle is comprised of two back to back hardware interrupt-acknowledge cycles. The first cycle allows the 8259's to resolve the source of the interrupt by driving the cascade address lines to the slave and the second cycle allows the CPU to read the pre-programmed vector off the data bus from the interrupt controller. The basic timing of these devices can be found in the INTEL 8259A specifications. These controllers reside on the XDATA bus.

##### 4.2 Direct Memory Access

Section 2.4.2 contains the functional description of the DMA controllers (U21 and U22, sheet 10). There are two 16-bit 4-channel LSI DMA devices and one memory page mapper (U20, sheet 10) used to obtain the upper eight address lines. DMA controller U22 is cascaded to DMA controller U21 by means of DREQ0. This allows four DMA channels on U21 and three DMA channels on U22. Refer to the INTEL 8237 reference manual for the basic timing.

##### 4.3 I/O Decode

I/O decode is comprised of an 74ALS138 three to eight decoder (U55, sheet 5 and a 74S288 32 x 8 ROM (U1, sheet 11). The 74ALS138 is strictly an address decode of address lines XA5 thru XA9 with no CPU control lines. System control lines MASTR and HLDA are used to disable decode output during a CPU hold acknowledge cycle when there is no I/O bus master, and to enable the decode output when there is an I/O bus master controlling the system bus. All I/O control lines are decoded by the peripheral device with the exception of the 74S288 ROM decodes. The 74S288 ROM decodes the PPICS signal from the ALS138 along with XA0, XA4, XIOR, and XIOW to obtain the NMI CS, KEYBD I/O, Real Time CMOS clock, and peripheral register select.

##### 4.4 Real Time Clock

The Real Time Clock consist of a Motorola CMOS MC146818 device (U5, sheet 11), a lithium battery back-up and a battery interface circuit (sheet 11). Power is supplied by VCC through a two stage transistor circuit when power is on and above approximately 3.0v. When the voltage drops below this level power is supplied through CR1 & CR2 by the lithium battery. These two diodes isolate the battery from any voltage spikes or high DC levels on VCC. During power down, the total drain on the battery equals 50ua (146818 max) plus 14.5ua (MC14069) for a total of 64.5ua.

## 5.0 MAIN LOGIC TIMING DIAGRAMS

### 5.1 SCOPE

Three important timing diagrams relevant to the TANDY model 3000 computer are included in this section.

### 5.2 CLOCK TIMING

The TANDY Model 3000 computer clock generation timing is indicated on Page 11. Clock generation and timing is discussed in Section 1.1.

of important note is signal ENAS(L) which is SI(L) synchronized to PROC CLK(1), called PRCLK(L) on the schematic. ENAS is used to allow generation of SYSCLK(H), called SCLK(H) on the schematic, which is one-half the rate of PROC CLK(1), or 8 MHZ, and also synchronized to PROC CLK(1).

DMA CLK(H), called DMACLK on the schematic, is SYS CLK(H) divided by two.

### 5.3 REFRESH TIMING

The diagram on Page 12 illustrates the REFRESH CYCLE timing.

Dynamic RAM refresh is required once every 15uS. The refresh request is generated by a timer IC (U4, sheet 11) OUT1. The refresh request is synchronized to the rising edge of DMACLK(L) to generate a CPU HRQ (CPU Hold REQuest).

Once the HOLD is acknowledged a "dummy" memory READ cycle is initiated. However, while RAS is allowed to pass to the RAM chips, CAS is inhibited. This produces a RAS-only memory access, or a REFRESH cycle.

During the time the refresh is taking place the processor is generating Ti cycles (indicating that it is working internally), Th cycles (indicating that the processor is holding), or both, depending on the actual instruction currently being executed by the processor.

Once the "dummy" cycle is complete the CPU HRQ line is brought inactive. This is recognized by the CPU, the hold acknowledge is dropped, and the processor continues processing normally.

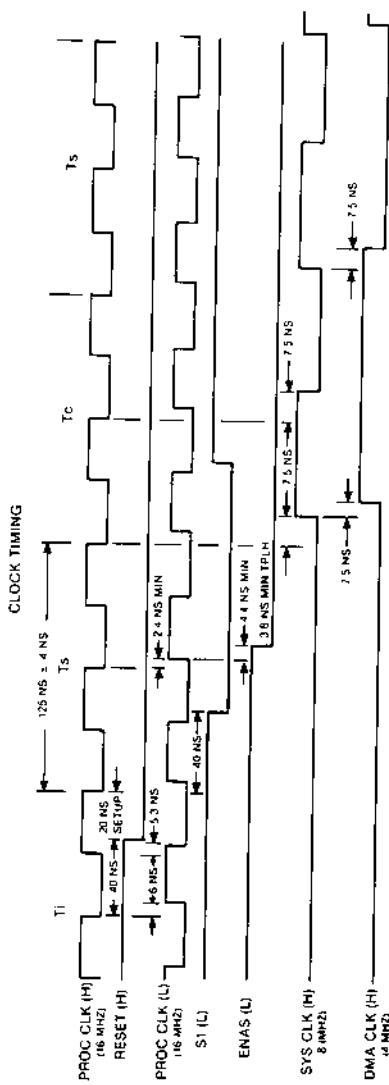
#### 5.4 INTERRUPT ACKNOWLEDGE CYCLE

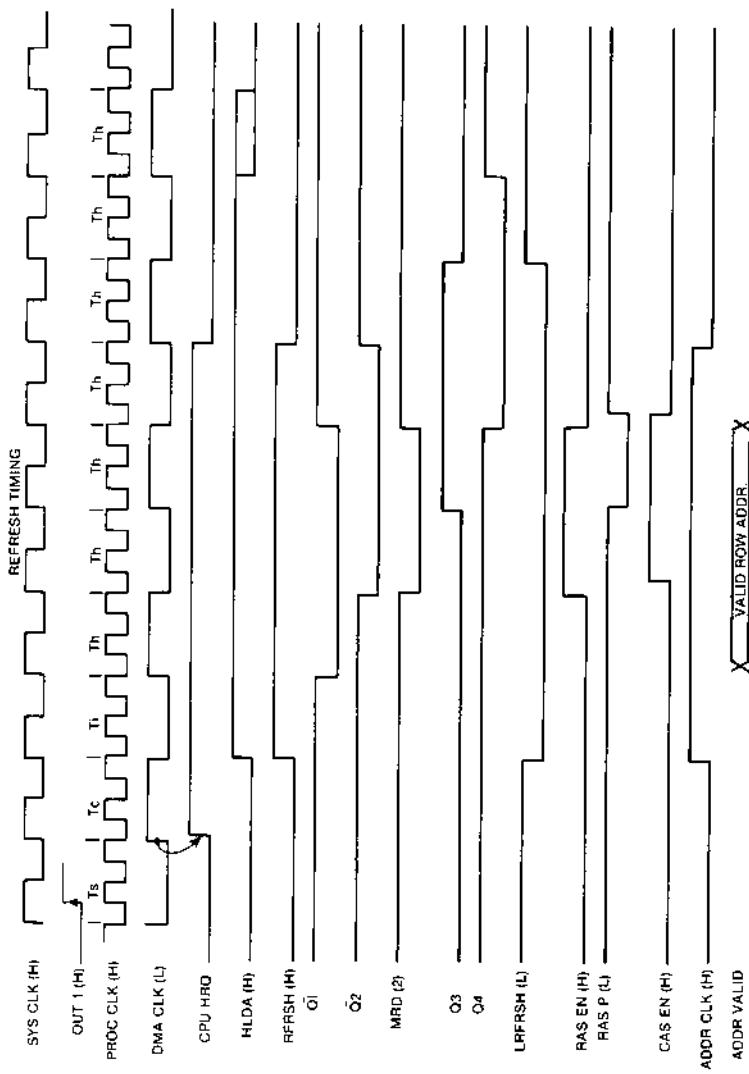
The diagram on Page 13 indicates the INTERRUPT ACKNOWLEDGE (INTA) cycle.

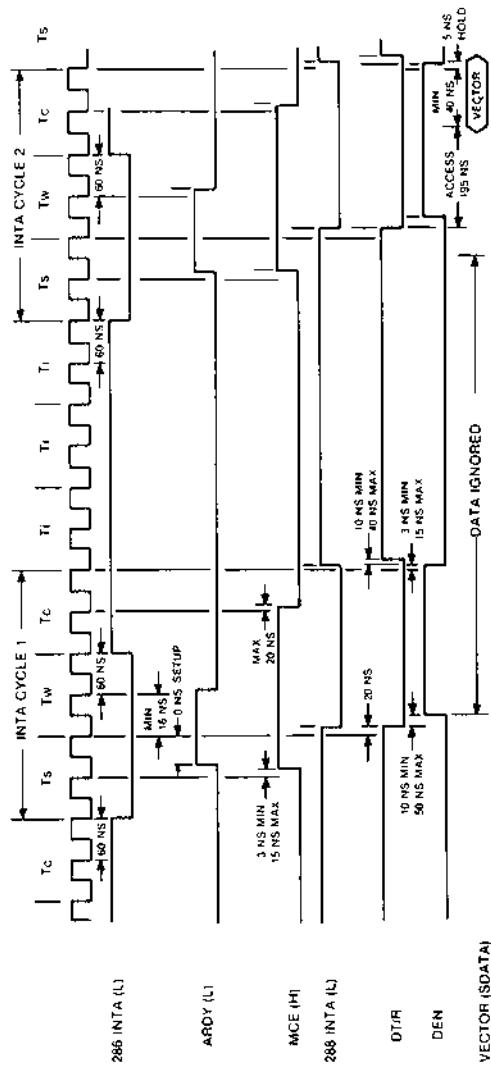
Of primary importance in this diagram is the fact that there are TWO Interrupt Acknowledge cycles for every interrupt generated by the 8259 Interrupt controllers (U2 and U3, sheet 11).

The first INTA cycle is used to indicate to the 8259s that the processor has recognized the attempt to interrupt. This first cycle is used by the 8259 to arbitrate their internal priority settings. Notice that any data appearing on the data lines at this time is ignored by the processor.

The second INTA cycle signals the interrupting 8259 to place an interrupt VECTOR on the data bus during this time. The processor reads this vector and uses it as an offset into a pre-programmed table of interrupts to determine where in memory the necessary interrupt handler routine is located. This routine is then executed by the processor.







TIMING SHOWN IS NOT ACTUAL TIMING.  
IT REFLECTS WORST CASE REQUIREMENTS ONLY

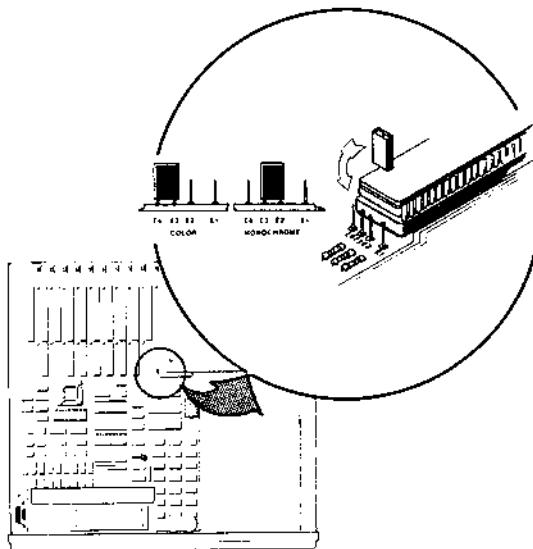
## 6.0 UPGRADES, JUMPER SETTINGS AND ALIGNMENTS

The following text describes the available jumper setting options and adjustments available on the TANDY Model 3000 computer.

### 6.1 COLOR / MONOCHROME SETTING

The TANDY Model 3000 is set at the factory for a monochrome video display card and monitor. Before installing a COLOR video display card, you must reposition a wire jumper on the computer's main logic board.

The color / monochrome jumper is located between the Serial / Parallel Adapter card (in Slot 10) and the front corner of the power supply chassis. (See the following illustration.)



To reach the jumper, you must remove the serial / Parallel Adapter Card in Slot 10.

The video display jumpers consists of three (3) pins.

JUMPER E2 - E3    MONOCHROME MONITOR [factory default setting]

JUMPER E3 - E4    COLOR MONITOR [user selectable option]

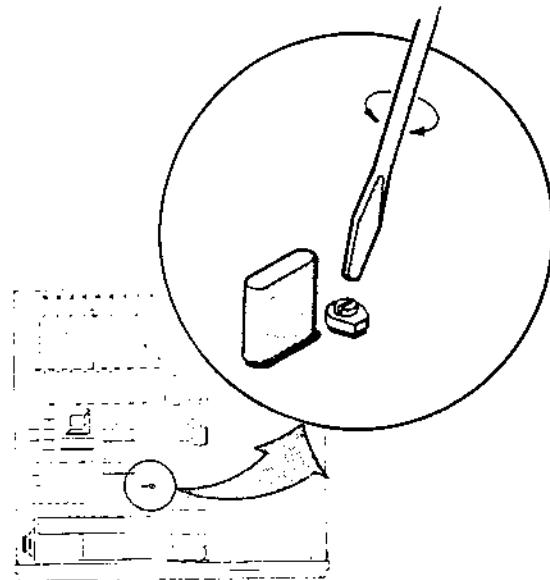
## 6.2 COLOR BURST CLOCK ADJUSTMENT

If a color video board is installed and a composite video monitor or color television is attached but no color is visible on the monitor it may be necessary to adjust the tunable capacitor on the Main Logic board.

Remove the TANDY Model 3000 computer's cover, then connect the color monitor or color television to the computer. Turn on both the computer and the monitor.

Adjust the Color Burst Clock adjustment until color is displayed on the monitor. (See the following illustration.)

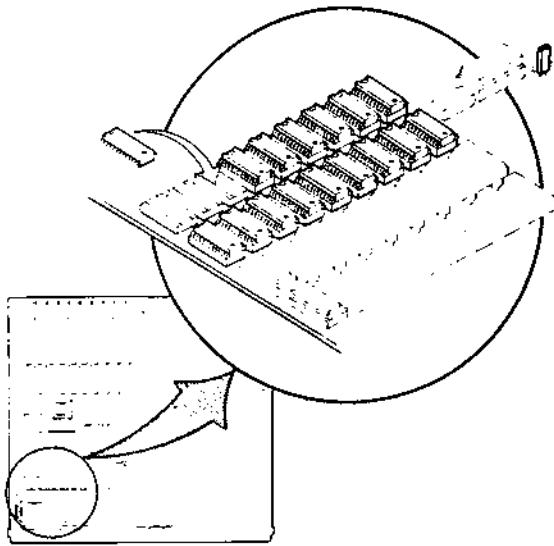
NOTE: You **MUST** use a plastic tuning tool for this adjustment.



### 6.3 RAM UPGRADE OPTION

The TANDY Model 3000 computer can support an optional 128K Memory Upgrade to bring the total RAM on the Main Logic board to 640K.

1. Remove the computer's cover.
2. The 18 empty RAM sockets are located behind the fan on the left front section of the Main Logic board. (See illustration below.) To gain access to these sockets you must first remove all cards present in Expansion lots 1 through 5. Take care not to damage or apply strain to any interconnecting cables.
3. Note the notch or dot at one end of the RAM chips. Install each chip into its socket with the notch or dot on the chip facing toward the slots at the rear of the system unit. (See illustration below.)
4. Install the supplied jumper across pins E13 and E14 on the Main Logic board. (See illustration below.)
5. Reinstall all cards removed from Slots 1 through 5. Verify proper operation using available diagnostics.



#### 6.4 ROM UPGRADE OPTION

The TANDY Model 3000 computer can support two different ROM configurations.

The first is two (2) 27128-type (16K by 8 bit) ROMs. Four (4) ROM locations are available; two are used. The remaining two are for expansion. Using this option there is 64K of ROM space available with 32K used.

The second option is for 27256-type (32K by 8 bit) ROMs. In this case there would be a total ROM address space of 128K available.

To support the 27128-type ROMs requires the following jumpers:

JUMPER E5 - E9      JUMPER E7 - E11      [factory default setting]

If 27256-type ROMs are to be installed then the following jumpers are required:

JUMPER E6 - E10      JUMPER E8 - E12

In either case all four ROMs must be of the same type.



Tandy 3000 Main Logic Sub Assembly

Symbol	Description	Part No.
	Tandy 3000 M/L	AX-0204
	T3000 PCB Rev. A (10.9" x 16" 4 Layer)	8709635A
C1,2,1A,2A,35 C3-8,10-13, 15-22,25,26, 28-34,39-43, 45,46-51,57-67, 70-73,77-80, 86-88,107-113, 127-132	Capacitor 47 PF $\pm 10\%$ 50V RAD Capacitor 0.1 UF Mono AX.	CF-1366 CC-104JJLA
C9,24,36-38,52, 53,68,69,74-76, 81-83,93,94,96, 105,106,114, 123,124-126, 141,142,151,152	Capacitor 10 UF $\pm 20\%$ 16V Rad.	CC-106MDAP
C14	Capacitor 27 PF $\pm 15\%$ 50V	CC-270KJCP
C23	Capacitor .01 UF 20% 50V C. Disc	CC-103JJCP
C27	Capacitor 4700 PF 80% 50V RAD	CC-472QJCP
C35	Capacitor .01 UF 10% 50V AX.	CC-103KJLA
C44	Capacitor Variable, 6-70 PF	ACF-7364
C54,89-92,97- 104,115-122, 133-140,143-149	Capacitor .33 UF $\pm 80-50\%$ 50V	CC-334ZJLA
C55	Capacitor 33 PF $\pm 10\%$ 50V RAD	CC-330KJCP
C56	Capacitor 15 PF $\pm 5\%$ 50V RAD	CC-150DJCP
C84,85,95	Capacitor .047 UF 10% 50V Mono	CC-473KJLA
C150	Capacitor .001 UF 50V 10%	CC-102JJCP
CR1-4	Diode IN4148	DX-0022
E1-14	Staking Pin	AHB-9682
FBL,2	Ferrite Bead	ACA-8242

Symbol	Description	Part No.
J1-10	Connector, 62PB	AJ-5954
J12-17,19	Connector, 36PB	8519258
J21,25	Connector, 4-Pin Header	AJ-7521
J22	Connector, 8-Pin DIN	AJ-7550
J23	Connector, 12-Pin Mate-N-Lock	AJ-1079
J24	Connector, 5-Pin Header	AJ-1078
R1,2	Resistor 470 Ohm 1/4 Watt 5%	N-0169EEC
R3,4,18	Resistor Car F 1K Ohm 1/4 Watt 5%	N-0196EEC
R6	Resistor 150 Ohm 1/4 Watt 5%	N-0142EEC
R7,14-17,21, 25,27-30,100	Resistor Car F 10K Ohm 1/4 Watt 5%	N-0281EEC
R8	Resistor 47 Ohm 1/4 Watt 5%	N-0099EEC
R9,11-13,19	Resistor 300 Ohm 1/4 Watt 5%	N-0158EEC
R10,24,101	Resistor 4.7K Ohm 1/4 Watt 5%	N-0247EEC
R20	Resistor 910 Ohm 1/4 Watt 5%	N-0192EEC
R22,23	Resistor 510 Ohm 1/4 Watt 5%	N-0173EEC
R26	Resistor Car F 51K Ohm 1/4 Watt 5%	N-0344EEC
R93	Resistor 2.2 Meg Ohm 1/4 Watt 5%	N-0454EEC
R102	Resistor 18 Ohm 1/4 Watt 5%	8207027
R103,R104	Resistor 27 Ohm 1/4 Watt 5%	N-0082EEC
RP1,3-7	Resistor Pak 10K Ohm 10-Pin SIP	ARX-0239
RP2,8	Resistor PAK 33 Ohm 10-Pin SIP	ARX-0048
RP9,10	Resistor PAK 33 Ohm 16-Pin DIP	ARX-0390
U1,99-134	Socket 16-Pin DIP	AJ-6581
U2,3,58-61	Socket 28-Pin DIP	AJ-6758
U4	Socket 24-Pin DIP	AJ-5044
U5	IC 146818	MX-5697
U6,21,22,78	Socket 40-Pin DIP	AJ-6580
U7	IC 14069	MX-5425
U8,9,12,17,36 45,46	IC 74ALS74	MX-5689
U10	IC 74LS51	MX-5572
U11	IC 74F11	MX-4979
U13	IC 74F04	MX-5953
U14,26,44,54	IC 74F74	MX-5936
U15	IC 74ALS175	MX-5692
U16,66,94	IC 74ALS244	MX-5853
U18,35,73	IC 74ALS04	MX-5522
U19,41,65,72	IC 74F08	MX-5954
U20	IC 74LS612	MX-5698
U23,69	IC 74ALS00	MX-5445
U24	IC 74ALS10 14-Pin	MX-5527

Symbol	Description	Part No.
U25,39	IC 74ALS02	MX-5498
U27,30	IC 74F175	MX-2118
U28,50	IC 74F174	MX-4983
U29	IC 74ALS112	8015112
U31	IC 75477	MX-6111
U32,33,64,85-87	IC 74ALS573	MX-5694
U34	IC 7407	AMX-4628
U37,84	IC 74LS245	AMX-4470
U38,49,63,70	Socket 20-Pin DIP	AJ-6760
U40	IC 74LS125	AMX-4640
U42,47	Socket 18-Pin DIP	AJ-6701
U43,96	IC 74ALS08	MX-5523
U48,53	IC 74ALS32	MX-5688
U51	IC 74F00	MX-6085
U52,68,75,76	IC 74F10	MX-3023
U55	IC 74ALS138	MX-5691
U56	IC 74F257	MX-6083
U57	IC 74ALS27	MX-5542
U62,71	IC 74F280	MX-5435
U67	IC PE21213 Delay Line 200 NS	AMX-5706
U74,98	IC 74S51 Dual AOI Gate	MX-5727
U77	Socket 68-Pin, JADEC "A"	AJ-7539
U79-81,83,88, 89,93	IC 74ALS245	MX-5693
U82	IC 74AS646	MX-5696
U90,91	IC 74F158	MX-2132
U95	IC 74LS590	MX-5695
U97	IC 74S04	AMX-4945
Q1	Transistor 2N3904	AMX-3583
Q2	Transistor 2N3906	AMX-3584
Y1	Crystal 32.768 KHz	MX-1113
Y2	Crystal 16 MHz	MX-0094
Y3	Crystal 14.318 MHz	MX-0095

**Tandy 3000 Main Logic Main Assembly**

Symbol	Description	Part No.
	Tandy 3000 Main Assembly	889AZ01
	Tandy 3000 Subassembly	AX-0204
	Jumper Plug	AJ-6908
U1	IC 74S288	MX-5701
U2,3	IC 8259A	MX-6001
U4	IC 8254-2	8048284
U6	IC 8042	8040041
U21,22	IC 8237A-5	MX-6778
U38	IC 16L8A PAL	MX-5737
U42	IC 82284-8	MX-5909
U47	IC 8284A	MX-5911
U49	IC 82288-8	MX-5910
U59	IC 27128 EPROM 200 NS	MX-4975
U61	IC 27128 EPROM 200 NS	MX-4976
U63	IC 28S42 512 X 8 PROM	MX-5265
U70	IC 16L8A PAL	MX-5787
U77	IC 80286-8	MX-5908
U117-134	TMS4256-15NL 256K X 1 DRAM 150NS	MX-6796

Tandy 3000

Chassis Subassembly

Item	Quan	Description	Part No.
1	1	Weldment, Chassis, Main	AZ-1002
2	1	Chassis, Main	
3	1	Support, Rear, Option Card	
4	1	Panel, Connector, Keyboard	
5	1	Bracket, Card Support	
6	1	Support, Front, Option Card	AHC-0191
7	4	Clip	8559073
8	7	Panel, Option Slot Cover	AZ-1010
9	1	Panel, Serial/Parallel	AZ-1004
10	1	Panel, Memory	AZ-1008
11	5	Feet	AF-0010
12	1	Fan Assembly, DC 12V	AM-4026
13	1	Connector	AJ-1080
14	2	Pins	AJ-1081
15	1	Filter, Fan	AHC-0190
16	4	Screw, #6-32 x 1/2	AHD-1815
17	4	Nut, Keps #6	AHD-7159
18	1	Loop, 5/8" x 3", White	
19	1	Hook, 5/8" x 1", White	
20	1	Speaker	AS-4001
21	1	Cable, Speaker	
22	15	Screw, #6-32 x 5/16 High Performance Thread Forming W/Torque Setting Serrations	AHD-2746
24	7	Screw, #6-32 x 1/4 H.P. Thread Form.	AHD-2618
25	3	Rivet	
26	1	Cable, Floppy Signal	AW-1066
27	1	Guide, Card, Option	ART-0204
28	1	Guide, Air Flow	
29	1	Battery Assembly, 6V	
30	1	Panel, Option Bd. Multiuser	ACS-0020
31	1	Clamp, Multiuser	

Final Assembly

Item	Quan	Description	Part No.
1	1	Chassis Subassembly	
2	1	Case, Top	AZ-1005
3	1	Bezel, Front	AZ-1006
4	1	Spring	ARB-1001
5	1	Retainer, Shaft	
6	5	Screw, #6 x 3/8 Plastite, PPHD	AHD-1552
7	1	Button, Reset	AK-1001
8	2	LED	AL-0020
9	2	Lens	AG-0002
10	2	LED Holder	
11	3	Screw, #8-32 x 1/2 PPHD	AHD-1553
12	1	Power Cord	AW-3329
13	1	Bezel, Disk Drive Door	AZ-1007
14	1	Switch, Reset	AS-1010
15	1	Toroid	
16	2	Pin, Guide	
17	1	Cable, Ground Outlet	
18	1	Cable, Ground Inlet	
19	1	Harness, Power/Reset/LED	AW-1062

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MODEL 3000 KEYBOARD SECTION

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IV. Parts List



## **I** KEYBOARD THEORY OF OPERATION

### **1 Description**

The TANDY Model 3000 system keyboard is a low profile, 84 key, detachable, IBM-AT compatible keyboard, using an 8049 microprocessor, clocked by a 6 MHz crystal oscillator.

### **2 Interface**

The keyboard has a bidirectional serial interface through a 5 pin DIN connector (pin 1 = clock, pin 2 = data, pin 3 = spare, pin 4 = ground, and pin 5 = +5 VDC; see Figure 5).

**CLOCK AND DATA SIGNALS:** When the keyboard sends data to the system through the 8049's P16 (see keyboard schematic), or receives commands through the 8049's INT\* line, it generates the clock signal through P17 to time the data; the system can prevent the keyboard from sending by forcing the clock line to a logic 0 level, sensed on the 8049 T1 input. During basic assurance test, the keyboard allows the clock and data lines to go to a logic 1 level. Data/command transmission from/to the keyboard consists of 11-bit serial data streams; bit 1 = 0 start bit, bits 2 thru 9 = data bits 0 thru 7, bit 10 = odd parity bit, and bit 11 = stop bit.

**KEYBOARD DATA OUTPUT:** When the clock and data lines are both high (this is a request to transmit from the keyboard), the keyboard sends the 11 bit serial transmission; data will be valid before the falling edge, and beyond the rising edge of the clock (see Figure 2). The clock line is checked for a logic 1 level at least every 60 milliseconds, and if it goes low before the 10th bit is sent (system override has occurred), the keyboard buffer returns the data and clock lines to a logic 1 level, otherwise, the transmission is completed. When the clock line is low, data is stored in the keyboard buffer, otherwise, the keyboard is either idle or receiving data or commands.

**KEYBOARD DATA INPUT:** When the clock line is high and the data line is low (this is a request to send to the keyboard; see Figure 3), the keyboard will count 10 bits and then force the data line low and will count one more bit (this action signals the system that the keyboard has received its transmission; the clock line will be checked for a low level no less than 60 millisecond intervals by the keyboard. Each transmission to the keyboard requires a response form the keyboard before the next communication can take place; the keyboard will respond within 20 milliseconds, unless prevented by a held-lo clock signal from the system. If the keyboard response is invalid or has a parity error, the system sends the command or data again; a resend command should not be sent in this case.

### **3 Sequencing Key Code Scanning**

Based on the programmed 8049 counter outputs (P20-P22), the keyboard detects all keys pressed through the 8049 D80-DB7 and P24-P26 inputs, and sends their scan codes to the interface in correct sequence, regardless of the number of keys held down (keystrokes entered while the interface is inhibited will be lost, and not stored; see Figures 6-7).

#### 4 Keyboard Buffer

The keyboard has a 16 character FIFO buffer contained in 8049 RAM (the 17th key stroke will be replaced with the overrun code 00H, and additional keystrokes will be lost).

#### 5 Power on Reset

This function has an operational time span of a minimum of .3 seconds, and a maximum of .9 seconds, asserted at Pin 4 of the 8049.

#### 6 Basic Assurance Test

This function is executed immediately after the power on reset, and lasts for .6 to .9 seconds; a successful test will send a AAH to the system, and an unsuccessful test will send FCH. The successful test defaults to typematic and make/break mode.

#### 7 Commands

**RESET (FFH):** The keyboard acknowledges a reset by raising the clock and data lines for a minimum of 500 microseconds (the keyboard is disabled from the reset until the acknowledge is accepted or until another command overrides the reset), and then perform a basic assurance test.

**RESEND (FEH):** The keyboard acknowledges this command by resending the previous output again unless the previous output was a resend, which means it will resend the byte which precedes the resend. The keyboard will issue a resend command following receipt of an invalid input, or any input with incorrect parity.

**NO-OPERATION (NOP, FDH thru F7H and F2H thru EPH):** These commands are acknowledged, but unused.

**SET DEFAULT (F6H):** The keyboard responds with an acknowledge, clears its output buffer, sets default conditions, and continues scanning, if the keyboard was previously enabled.

**ENABLE (F4H):** The keyboard responds with an acknowledge, clears its buffer, and starts scanning.

**SET TYPEMATIC RATE/DELAY (F3):** The keyboard responds with an acknowledge, stops scanning, waits for the rate parameter, acknowledges the rate parameter, sets the rate and delay, and continues scanning, if the keyboard was enabled. If a command is received instead of the rate parameter, the function ends with no change to the existing rate and the new command is processed; the scanning is disabled.

**ECHO (EEH):** If enabled, the keyboard responds by issuing a EEH response, and continues scanning.

## 7 Commands (continued)

**SET/RESET MODE INDICATORS (EDH):** The keyboard responds with an acknowledge, disables scanning, and waits for the option byte. Upon receipt of the byte, the keyboard responds with an acknowledge, sets the indicators, and continues scanning if the keyboard is enabled. If another command is received in place of the option byte, execution of the function is stopped with no change to the indicator states, and the new command is processed, and scanning is resumed.

**ACK (FAR):** The keyboard issues an acknowledge response to any valid input other than an echo or resend command; if the keyboard is interrupted, while sending an acknowledge, the acknowledge is discarded and the new command is acted upon.

## 8 Keys

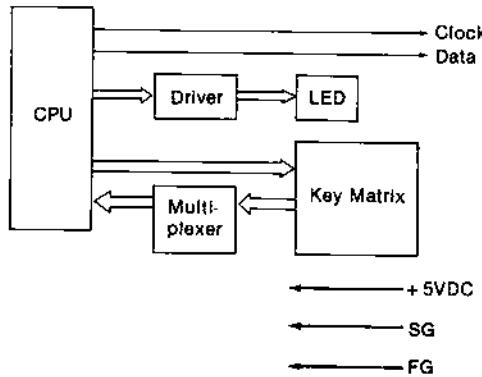
All keys are classified as make/break, which means when a key is pressed, the keyboard sends a make code, and when released, it sends a make code preceded by FOH (the keys are IBM typematic, which means when held down, they will continue to send make codes until released; only the first make code will be stored in the keyboard buffer). The typematic rate and delay parameter are determined by the value of the byte following the command; bit 7 is always 0, bits 6 and 5 serve as the delay parameter (delay = 1 plus the binary value of bits 6 and 5 multiplied by 250 milliseconds +/- 20 %), and bits 4 thru 0 are the rate parameter as shown in the table below.

<u>BIT</u>	<u>RATE</u>	<u>BIT</u>	<u>RATE</u>	<u>BIT</u>	<u>RATE</u>	<u>BIT</u>	<u>RATE</u>
00000	30.0	00100	20.0	01000	15.0	01100	10.0
00001	26.7	00101	18.5	01001	13.3	01101	9.2
00010	24.0	00110	17.1	01010	12.0	01110	8.6
00011	21.8	00111	16.0	01011	10.9	01111	8.0
10000	7.5	10100	5.0	11000	3.7	11100	2.5
10001	6.7	10101	4.6	11001	3.3	11101	2.3
10010	6.0	10110	4.3	11010	3.0	11110	2.1
10011	5.5	10111	4.0	11011	2.7	11111	2.0

## 8 Keys (continued)

**KEY SCAN CODES:** Each key is assigned a unique 8 bit, make, scan code, which is sent when the key is pressed; the following table and figure indicate the key number scan code. (See the keyboard layout and code table for appropriate key position, and the keyboard section of the design detail specification for translated system codes.)

<u>KEY</u>	<u>CODE</u>										
1	0E	15	66	30	14	46	1A	65	06	95	77
2	16	16	0D	31	1C	47	22	66	0C	96	75
3	1E	17	15	32	1B	48	21	67	0B	97	73
4	26	18	1D	33	23	49	2A	68	0A	98	72
5	25	19	24	34	2B	50	32	69	09	99	70
6	2E	20	2D	35	34	51	31	70	05	100	7E
7	36	21	2C	36	33	52	3A	71	04	101	7D
8	3D	22	35	37	3B	53	41	72	03	102	74
9	3E	23	3C	38	42	54	49	73	02	103	7A
10	46	24	43	39	4B	55	4A	74	01	104	71
11	45	25	44	40	4C	57	59	90	76	105	7F
12	4E	26	4D	41	52	58	11	91	6C	106	7C
13	55	27	54	43	5A	61	29	92	6B	107	7B
14	50	28	5B	44	12	64	58	93	69	108	79



**Figure 1 Keyboard Block Diagram**

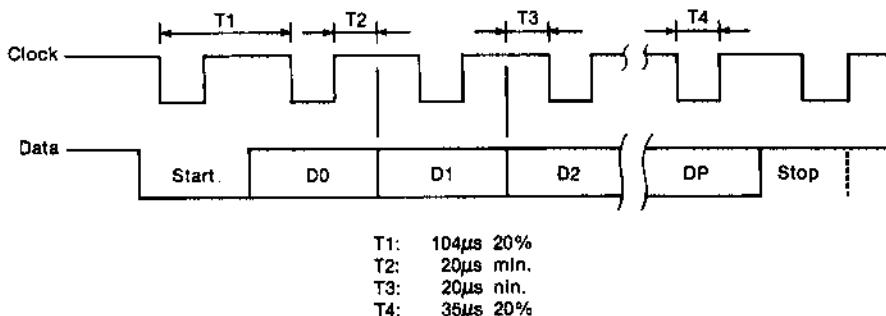


Figure 2 Keyboard Data Output

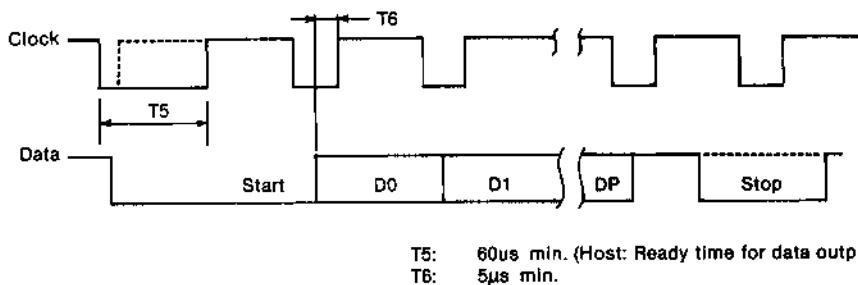
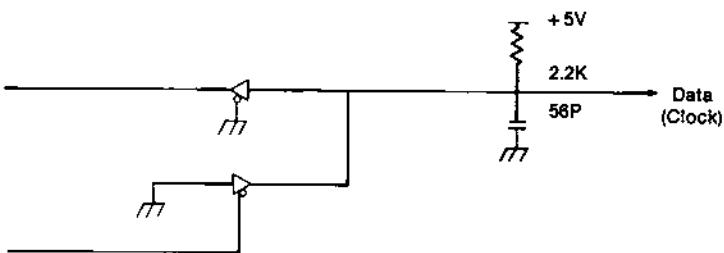
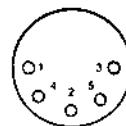


Figure 3 Keyboard Data Input

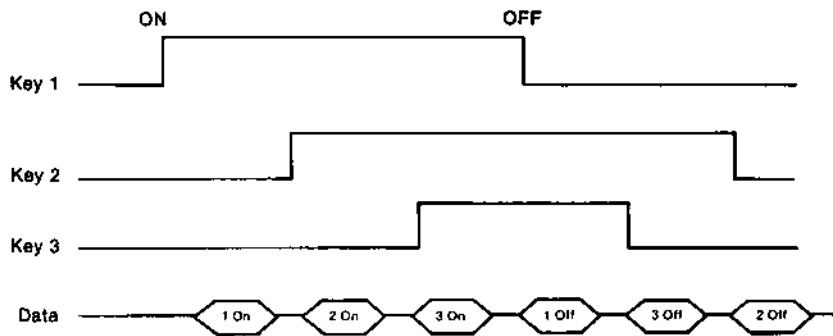


**Figure 4 Interface Circuit Specification**

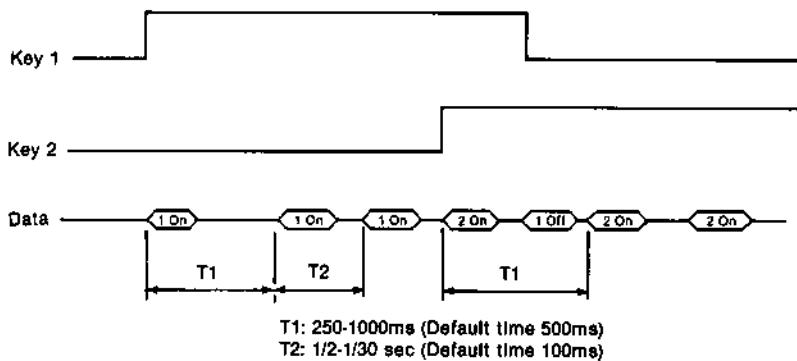
NO	SIGNAL
1	CLOCK
2	Data
3	
4	Ground (SG)
5	5 Vdc
—	Ground (FG)



**Figure 5 DIN Connector**



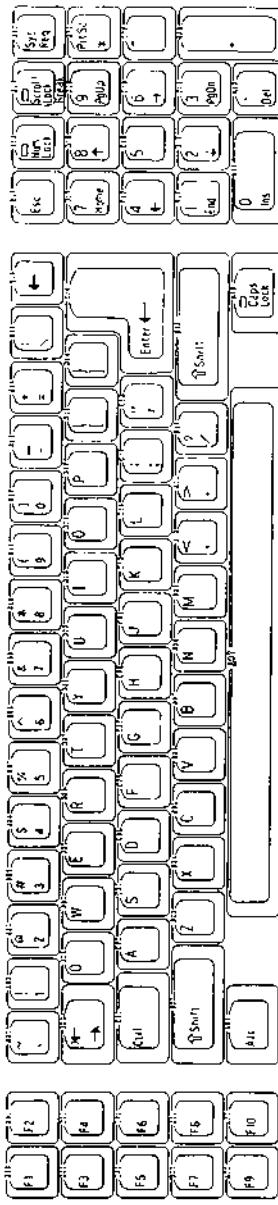
**Figure 6 Key Code Sending Sequence**



**Figure 7 Typermatic Cycle**

ECONOMIC TABLE

四



MODEL 3000 KEYBOARD LAYOUT

**Keyboard Subassembly**

Item	Quan	Description	Part No.
1	1	Keyboard, Encoded	AXX-0244
2	1	Key Cap Set (International)	8590202
3	1	Keyboard (Canada)	8790559

**THEORY OF OPERATION**

**TANDY MODEL 3000  
2 MEGABYTE MEMORY UPGRADE BOARD**



TANDY MODEL 3000  
2 MEGABYTE MEMORY UPGRADE BOARD

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**Tandy Model 3000  
2 Megabyte Memory Upgrade Board**

## 1.0 THEORY OF OPERATION

### 1.1 OVERVIEW

The Tandy Model 3000 2 Megabyte Memory Upgrade Board supports up to 2 megabytes of memory per board, in 512 Kilobyte (1/2 Megabyte) steps. This memory is in addition to the fully upgraded main logic board, which contains 64K of memory. Using the 2 Megabyte memory upgrade the Tandy Model 3000 can support up to 16 megabytes of memory. However, expansion memory above the 1 megabyte base memory can only be accessed from the 80286 processor's Protected Operation Mode.

The 2 Megabyte Memory Upgrade option allows both 8-bit and 16-bit operation in the memory address space 100000h - EFFFFFh available to the 80286 processor in the Protected Mode. One WAIT state is generated per access. Odd parity generation and checking is used for memory integrity. The 2 Megabyte Memory Upgrades must be installed contiguously, beginning at address 100000h.

The 2 Megabyte Memory Upgrade option is populated with 256K-by-1 bit dynamic RAM (DRAM) chips of 150 nanosecond access time.

### 1.2 INTERFACING

The 2 Megabyte Memory Upgrade interface to the Tandy Model 3000 requires both the IBM PC compatible expansion connector (62 pins) and the IBM AT compatible expansion slot (36 connector).

The 62 pin IBM PC compatible expansion connector provides most of the necessary signals to operate the expansion memory.

Low order address lines	SA0 - SA19
Low order data lines	SD0 - SD7
Refresh control	RFSH*
Parity error check	IOCHK*
Address latch control	BALE
RESET	RESETDRV

The 36 pin IBM AT compatible expansion slot provides the necessary signals to allow the extended addressing and 16-bit data path compatibility.

High order address lines	LA20 - LA23
High order data lines	SD9 - SD15
8 bit access control	SBRE
16-bit WAIT control	MEM16*
READ and WRITE control	MEMR*, MEMW*

## 1.2 INTERFACING (continued)

Power supply distribution is handled by both expansion slots

Supply Voltage	SVIN1, SVIN2, SVIN3
Ground	GND

## 1.3 THEORY OF OPERATION

The 2 Megabyte Memory Expansion board is arranged as 4 banks, each bank consisting of 512 Kilobytes of DRAM. The banks are numbered "A" through "D". Schematic Pages 4, 5, 6 and 7 detail the RAM banks. Note that each bank is in parallel with the others, and that any individual bank is selected by asserting the appropriate RAS line (RASA - RASC) at the appropriate time. Upper or lower byte access is controlled by assertion of the appropriate CAS signal.

Address and data line buffering is handled by the circuitry contained on Page 3 of the schematic. Data transfers are handled by U93 and U97. These chips are in turn controlled by SBHE and BA0, respectively. SBHE and BA0 indicate how a transfer is to take place, in accordance with the following table:

SBHE	BA0	FUNCTION
0	0	16-bit transfer
0	1	8-bit transfer on UPPER data bits (SD8 - SD15)
1	0	8-bit transfer on LOWER data bits (SD0 - SD7)
1	1	No data transferred

Odd parity is generated during a WRITE operation by U88 and U91. Odd parity is checked during READ operation by the same chips. During a READ operation the odd parity outputs (pin 6) should always be HIGH. A LOW on the parity outputs during a READ operation indicates a parity error.

RAS/CAS multiplexing of the address lines during a memory access (READ or WRITE) is handled by U95, U96 and parts of U78 and U83. Sixteen address lines, SA1 through SA16, are handled by these two chips. However, the 256K DRAMs used require 18 address lines. U78 and U83 form a simple address multiplexer to handle SA17 and SA18.

Due to the number of ICs to be driven by the address lines (72 to be exact) an increased drive capacity is needed on the RAM chip address lines. U78, U84 and U89 are included to drive the RAM chip address lines. Increased drive for the WRITE line (BMEMW\*) is provided by U74. Resistor packs RP1, RP2, RP3, RP6 and RP7 are included to reduce overshoot, undershoot, and ringing on the address and write lines.

Memory timing and bank selection are handled by the circuitry found on Page 2 of the schematic diagram. The upper 4 address lines (LA20 - LA23) are used for bank selection. The desired bank is indicated by proper setting of DIP switch S1 [See Memory Expansion Board Switch Settings] and is decoded by U81, U85, and U94.

The switch and decoding systems allows the Memory Expansion Board to be populated with .5 Meg, 1 Meg, 1.5 Meg, or 2 Meg of memory. The board may be selected to appear at any 1 megabyte boundary above the 1 megabyte base memory. Memory must be installed contiguously; there can be no empty "blocks" between memory banks.

Decoding of proper RAS and CAS enable signals is handled by IFL chip U86. U86 also produces signal T/R used to control the direction of data flow through data buffers U93 and U97. Also produced by U86 is signal MEM16. This signal is used to indicate that the desired access requires one (1) WAIT cycle and has a 16-bit data path available. MEM16 controls part of U80 to produce signal MEM16\* which indicates to the processor control circuitry that a one WAIT state 16-bit data path memory access is in progress.

A memory access is indicated by any activity on MEMW\* or MEMR\*. This activity is detected by part of U75, which produces signal MEMCYCLE. MEMCYCLE is used to qualify the RAS and CAS steering buffers U73, U75, U77 and U79. When MEMCYCLE goes active HIGH the correct RAS\* signal will begin, as decoded by U86.

MEMCYCLE also starts a signal traveling through delay line U76. After 40 nanoseconds signal ADDRMUX is generated to switch the RAS/CAS address multiplexers U95 and U96. After 80 nanoseconds signal T80 is generated which activates the proper CAS\* signal as decoded by U86.

Part of U79 decodes the time that T80, T160 and T200 all become HIGH. This happens at 200 nanoseconds after MEMCYCLE becomes active. Signal SYNC is asserted LOW and stops the generation of the RAS\* signals. The remaining system timing is generated by the device generating the memory access (usually the microprocessor).

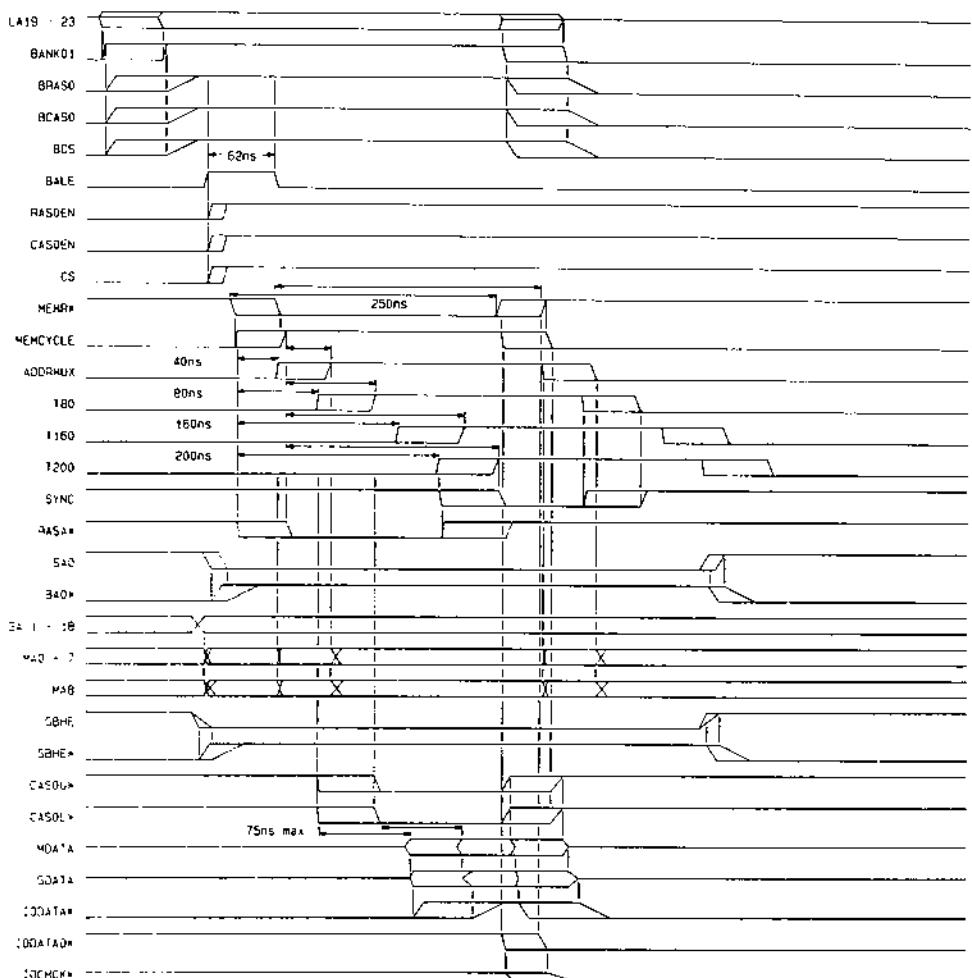
Parity error checking is handled by IFL chip U90 and parts of U87, U92 and U98. U90 decodes if a parity error has been produced, and if so which in which bank. An appropriate signal, IODATA0\* - IODATA3\*, is produced, and the signal is clocked through latches U87 and U92 on the trailing (rising) edge of BMEMR\*. A parity error will cause the latch to become CLEARED. The necessary section of U98 will be enabled, bringing IOCHK\* LOW, indicating a parity error has occurred. Latches U87 and U92 are SET before the next memory cycle occurs, and parity is not checked during a refresh cycle.

#### 1.4 TIMING DIAGRAMS

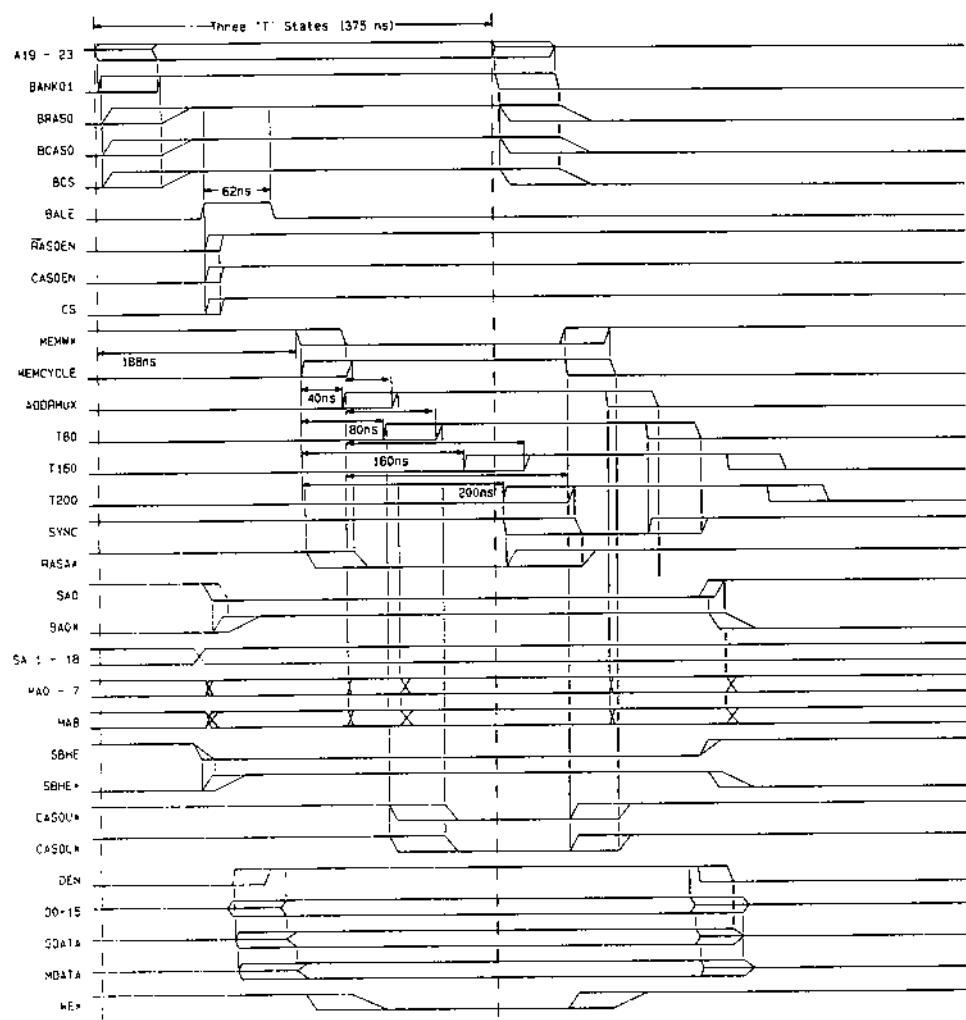
Timing diagrams have been included to exactly describe the signal relationships during a READ or WRITE cycle. Of particular note are the length of the access cycle and the time required during an access.

Because of the MEM16\* signal the processor control section introduces one processor clock (125 nanosecond) WAIT state during any access to this board. This results in a three "T" state (375 nanosecond) access. This allows the use of 150 nanosecond access time memory devices.

READ cycle timing is quite critical. WRITE cycle timing is more relaxed.



READ TIMING



WRITE TIMING

## Memory Expansion Board Dip Switch Settings

1. Set dip switches 5 and 6 On (0) or Off (1) as follows:

Dip  
Switches  
5, 6 and 8

On On Off If only bank 0 contains memory chips.  
Off On Off If banks 0 and 1 contain memory chips.  
On Off Off If banks 0,1 and 2 contain memory chips.  
Off Off Off If banks 0,1,2 and 3 contain memory chips.

Note: Dip switch 7 is not used.

Note: Dip switch 8 is used to disable the first 512K memory on the first board installed (Address 1.0MB thru 1.5MB) for other options which use this address space. To select this option configure dip switch 8 to the "On" position, on the first memory board installed only.

2. Set the start address of memory bank 0 by setting dip switches 1-4 On (0) or Off (1). The dip switches are to be set on 1 megabyte boundaries depending upon whether the Memory Expansion board is the 1st, 2nd, 3rd... or last (7th), Memory Expansion board in the computer.

	Dip Switches				Start Address of Bank 0	Start Address of Bank 1	Start Address of Bank 2	Start Address of Bank 3
	1	2	3	4				
1st Brd.	Off	On	On	On	100000	180000	200000	280000
2nd Brd.	Off	Off	On	On	300000	380000	400000	480000
3rd Brd.	Off	On	Off	On	500000	580000	600000	680000
4th Brd.	Off	Off	Off	On	700000	780000	800000	880000
5th Brd.	Off	On	On	Off	900000	980000	A00000	A80000
6th Brd.	Off	Off	On	Off	B00000	B80000	C00000	C80000
7th Brd.	Off	On	Off	Off	D00000	D80000	E00000	E80000



**Tandy 3000 Memory/Option Sub Assembly**

Symbol	Description	Part No.
	T3000 Memory/Option Sub Assembly	8898936
	T3000 Memory/Option PCB REV. "A" (13" X 4.5" 4 Layer)	8709644A
C1-72	Capacitor .33 UF 50V 80/20 Mono Ax	CC-334ZJLA
C73-81,105,107	Capacitor 10 UF 16V Rad.	CC-106MDAP
C82-104,106	Capacitor .1 UF 50V 80/20 Mono Ax.	CC-104JJLA
C108-110	Capacitor .01 UF 50V +20% Mono Ax	CC-103KJLA
FBl-3	Resistor 0 Ohm	AJ-6814
R1	Resistor 4.7K Ohm 1/4W 5%	N-0247EEC
RPl-3	Resistor Pack 33 Ohm 5R 10-Pin SIP	ARK-0048
RP4,5,8	Resistor Pack 10K Ohm 9R 10-Pin SIP	ARK-0239
RP6,7	Resistor Pack 33 Ohm 8R 16-Pin DIP	ARK-0390
S1	Switch 8PST DIP	8489004
U1-72	Socket 16-Pin DIP	AJ-6581
U73,77	IC 74F20	8015020
U74,84,89	IC 74F244	8015244
U75,79	IC 74F10	MX-3023
U76	IC Delay Line	8429010
U78	IC 74F02	8015002
U80,98	IC 74LS125	AMX-4640
U81	IC 74LS283	8020283
U82	IC 74ALS573	MX-5694
U83	IC 74F08	MX-5954
U85,94	IC 74F85 or SUB 74S85	8015085
U86,90	Socket 20-Pin DIP	AJ-6760
U87,92	IC 74F74	MX-5936
U88,91	IC 74F280	MX-5435
U93,97	IC 74ALS245	MX-5693
U95,96	IC 74F158	MX-2132
U99	IC 74F00	MX-6085

Tandy 3000 Memory/Option Main Assembly

Symbol	Description	Part No.
	Tandy 3000 Memory/Option Main Assembly	
	T3000 Memory/Option Sub Assembly	8898936
	Panel - Memory Combo	AZ-1008
U86,90	82S153A 10 NS	8075153
U1 728	IC 256K Dram	MX-6796

Tandy 3000 Memory/Option Sub Assembly - REV. B

Symbol	Description	Part No.
	T3000 Memory/Option Sub Assembly	8898936B
	T3000 Memory/Option PCB REV. "B" (13" X 4.5" 4 Layer)	8709644B
C1-72 C73,80,81,101- 108	Capacitor .33 UF 50V 80/20 Mono Ax	8374334
	Capacitor 10 UF 16V Rad.	8326101
C74-79,82-100	Capacitor .1 UF 50V 80/20 Mono Ax.	8374104
R1	Resistor 4.7K Ohm 1/4W 5%	8207247
RPl,4,6	Resistor Pack 33 Ohm 5R 10-Pin SIP	8290057
RP2,3	Resistor Pack 33 Ohm 8R 16-Pin DIP	8290044
RP5,7,8	Resistor Pack 10K Ohm 9R 10-Pin SIP	8290010
S1	Switch 8PST DIP	8489004
U1-72,99	Socket 16-Pin DIP	8509003
U73,75,98	IC 74F244	8015244
U74,76	IC 74F20	8015020
U78,81,97,98, 102	Socket 20-Pin DIP	8509009
U77	IC 74ALS573	8025573
U79,84	IC 74F10	8015010
U80	IC Delay Line	8429010
U82	IC 74F00	8015000
U83,89	IC (Spares)	
U85	IC 74F02	8015002
U86	IC 74LS283	8020283
U87,96	IC 74LS125	8020125
U88	IC 74F32	8015032
U90,92	IC 74F280	8015280
U91	IC 74F08	8015008
U93,99	IC 74F85 or SUB 74S85	8015085
U94,95	IC 74F158	8015158
U97,102	IC 74ALS245	8025245
U100,101	IC 74F74	8015074

**Tandy 3000 Memory/Option Main Assembly**

Symbol	Description	Part No.
	Tandy 3000 Memory/Option Main Assembly	
	T3000 Memory/Option Sub Assembly	8898936B
	Panel - Memory Combo	8729557
U1-72 U78,81	IC 256K Dram 825153A 10 NS	8049008 8042153

TABLE OF CONTENTS  
MODEL 3000 SERIAL/PARALLEL OPTION CARD SECTION

I. Theory of Operation

Overview (Not Available)

II. Jumper Settings

III. Schematics

IV. Parts List

V. PCB Layout



## Jumper Settings on the optional Serial/Parallel Board

1. Check the position of the Baud-Rate Generator jumper. It is set at the factory to connect pins E1 and E3 for the USA Standard. To set the Baud-Rate Generator to the International Standard connect pins E1 and E2 with the jumper that connected E1 and E3. Then connect pins E3 and E4 with a second jumper.
2. If you are installing this board in the Tandy 3000, install a jumper on E5 and E6 to set the parallel port as Port 2 (LPT2). Install a jumper on E8 and E9 to set the serial port as Port 2 (COM2).
3. If you are installing this board in the Tandy 1000 or Tandy 1200, install a jumper on E5 and E6 to set the parallel port as Port 2. If a serial board is not already installed we suggest that you set the jumper on E9 and E10 to set the serial port as Port 1 (COM1).

Note: The parallel port can be set as Port 1 (LPT1) by moving the jumper to connect pins E6 and E7.

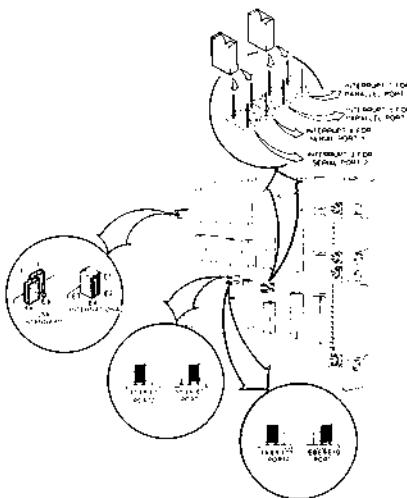


Figure 1 Jumper Settings on the optional Serial/Parallel Board.

**Note:** In order to resolve interrupt conflicts with other boards disable the corresponding interrupt on the Rev. B Serial/Parallel board by removing the jumper from the corresponding interrupt staking pins as follows:

Interrupt	Staking Pins	Port
7	E11 ~ E12	Parallel 1 *
5	E13 ~ E14	Parallel 2
4	E15 ~ E16	Serial 1 *
3	E17 ~ E18	Serial 2

On the optional Serial/Parallel Board only one parallel or serial port can be jumpered at any given time.

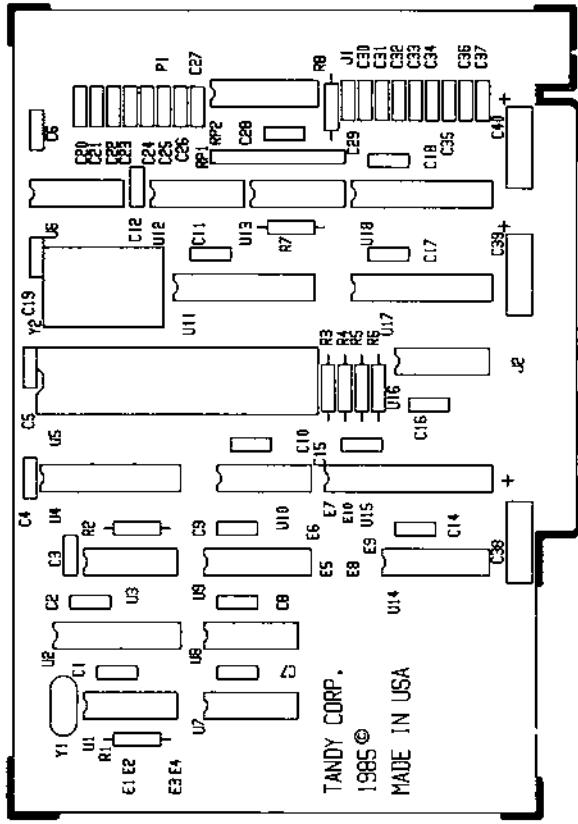
Tandy 3000 Serial/Parallel Sub Assy.

Symbol	Description	Part No.
	Tandy 3000 Serial/Parallel Sub Assy. T3000 Serial/Parallel PCB REV.PP2 (6" X 4.25" : 4 Layer)	88898921B 8709643B
C1-12,14-19,28	Capacitor 0.1 UF 50V +80/-20% Mono Ax.	8374104
C38-40	Capacitor 10 UF 16V Elect. Ax.	8316101
C20-27	Capacitor 330 PF 50V 10 <sup>t</sup> C Disc	8371334
C29-37	Capacitor 2200 PF 50V 20% Mono Ax.	8372224
E1-18	Staking Pin	8529014
J1	Connector 25 Position Shielded D Sub Fem.	8519270
P1	Connector 9 Position Shielded D Sub Male	8519269
P1,J1 (2 ea.)	Screw 4-40 x 3/8 (For use w/ alternate J1/P1)	8569002
P1,J1 (2 ea.)	Nut 4-40 Keps (For use w/ alternate J1/P1)	8579003
R1-3,5,6	Resistor 4.7K Ohm 1/4 Watt 5%	8207247
R4,7	Resistor 750 Ohm 1/4 Watt 5%	8207175
R8	Resistor 27 Ohm 1/4 Watt 5%	8207027
RPL	Resistor Pack 4.7K 9COM 10-Pin SIP	8294247
RP2	Resistor Pack 27 Ohm 8R 16-Pin DIP	8290027
U1	IC 74LS00	8020000
U2	Socket 18-Pin DIP (LS=.300)	8509006
U3	IC 74LS125	8020125
U4	IC 74LS240	8020240
U5	Socket 40-Pin DIP	8509002
U6	IC MC1488	8050188
U7,12	IC MC1489	8050189
U8	IC 74LS21	8020021
U9	IC 74LS174	8020174
U10,16	IC 74LS04	8020004
U11	IC 74LS244	8020244
U13	IC 74LS05	8020005
U14	IC 74LS155	8020155
U15	Socket 24-Pin DIP	8509029
U17	IC 74LS374	8020374
U18	IC 74LS245	8020245
Y1	Crystal 5.0688 MHz	8409005
Y2	Oscillator 1.8432 MHz	8409054

Tandy 3000 Serial/Parallel Main Assy.

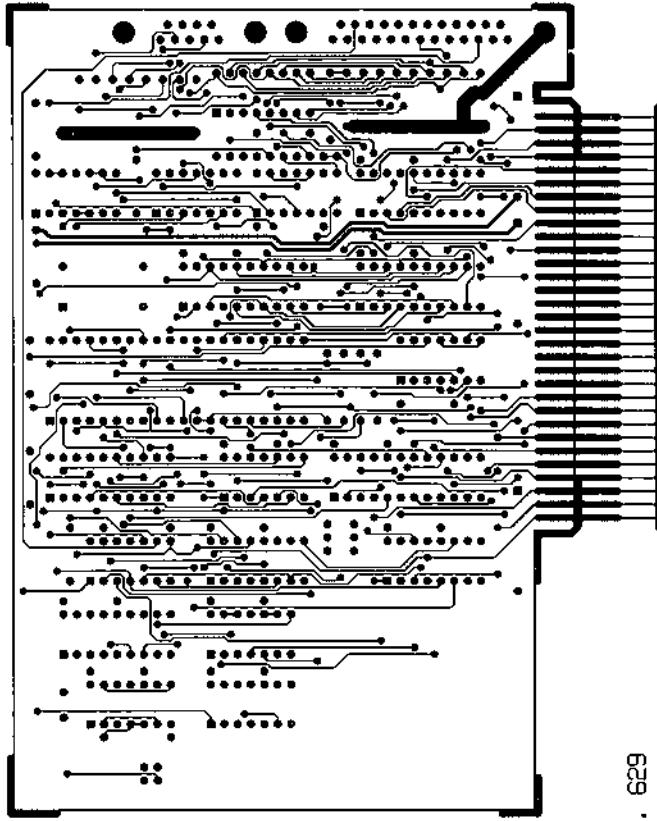
Symbol	Description	Part No.
	Tandy 3000 Serial/Parallel Main Assy.	
	Tandy 3000 Serial/Parallel Subassembly.	8898921B
U2	WD1943	8040943
U5	IC NS16450	8040450
U15	IC 20L8 PAL	8041208

SILKSCREEN



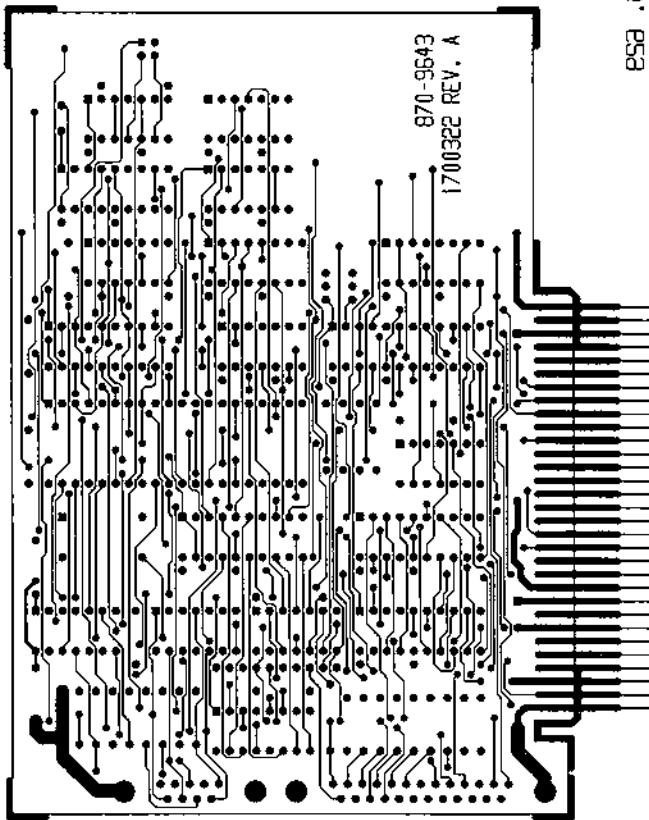
PROJ. 629  
SERIAL/PARALLEL BD.  
1700322 REV. A B/7/85

COMPONENT-SIDE LAYER 1



PROJ. 629  
SERIAL/PARALLEL BD.  
1700322 REV. A 8/7/85

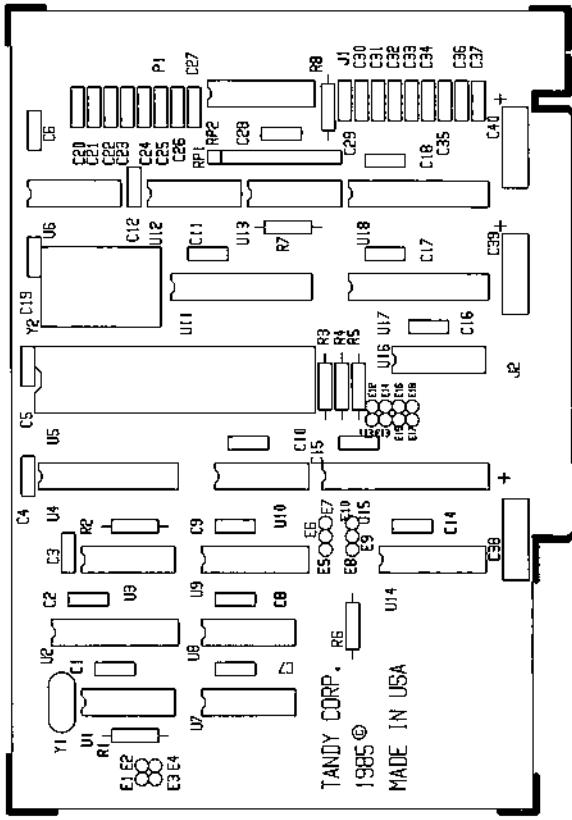
SOLDER-SIDE LAYER 4



28V128 PARALLEL DB.  
SERIAL DB.  
1700322 REV. A  
870-9643

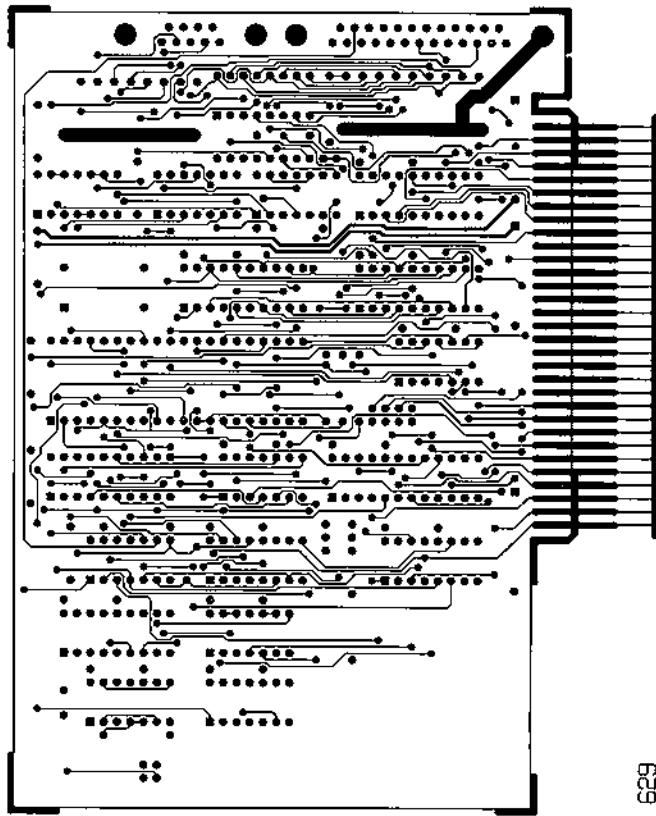


SILKSCREEN



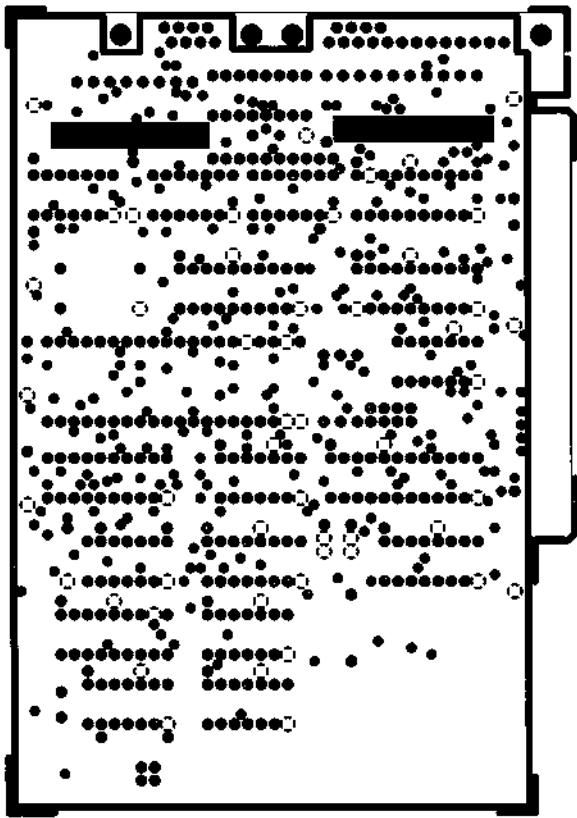
PROJ. 629  
SERIAL/PARALLEL BD.  
1700322 REV. B 12-7-85

COMPONENT-SIDE LAYER 1



PROJ. 629  
SERIAL/PARALLEL BD.  
1700322 REV. B 12-7-85

GROUND-PLANE LAYER 2



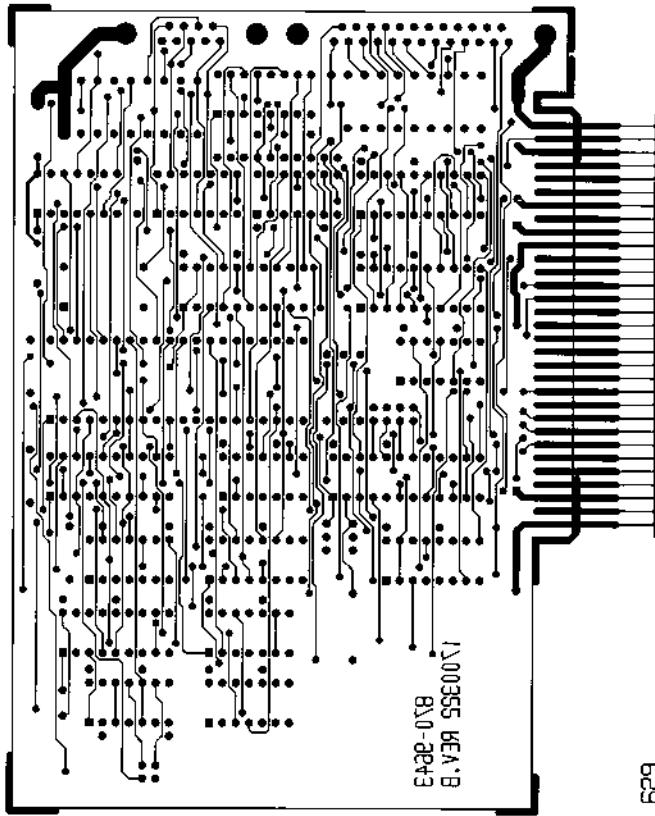
PROJ. 629  
SERIAL/PARALLEL BD.  
1700322 REV. B 12-7-85

+SV/PWR-PLANE LAYER 3



PROJ. 629  
SERIAL/PARALLEL BD.  
1700322 REV. B 12-7-85

SOURCE-SIDE LAYER 4



PROJ. 629  
SERIAL/PARALLEL BD.  
1700322 REV. B 12-7-85



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\*  
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\*  
\*        Floppy Disk Controller        \*  
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\*  
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## **Tandy 3000 floppy disk controller**

The Tandy 3000 Floppy Disk controller uses Western Digital uPD765 and WD16C92 technology for reliable operation of both the standard or high density floppy drives. This board supports up to two floppy drives installed in the Tandy 3000.

<b>Contents</b>	<b>Section</b>
Normal jumper settings	1
Schematics & Component layout	2
Pal Equations PAL16L8	3
Parts list	4

Refer to the Chip Data section for information on the  
WD16C92

November 15, 1985



\*\*\*\*\*  
\* \*  
\* \*  
\*       Floppy Disk Controller      \*  
\*    \*  
\*       Section I                        \*  
\*    \*  
\*       Jumper settings                \*  
\*    \*  
\*\*\*\*\*



## FLOPPY DISK CONTROLLER JUMPERS

1. E1 jumpered to E2\*      primary host bus address effective (3Fx)  
E3 jumpered to E2      secondary host bus address effective (37x)
2. E4 jumpered to E5\*      board operational  
E6 jumpered to E5      board disabled (will not respond to host bus)
3. E7 jumpered to E8\*      single speed drive (01 data rate = 300 Kbs)  
E9 jumpered to E8      dual speed drive (01 data rate = 250 Kbs)

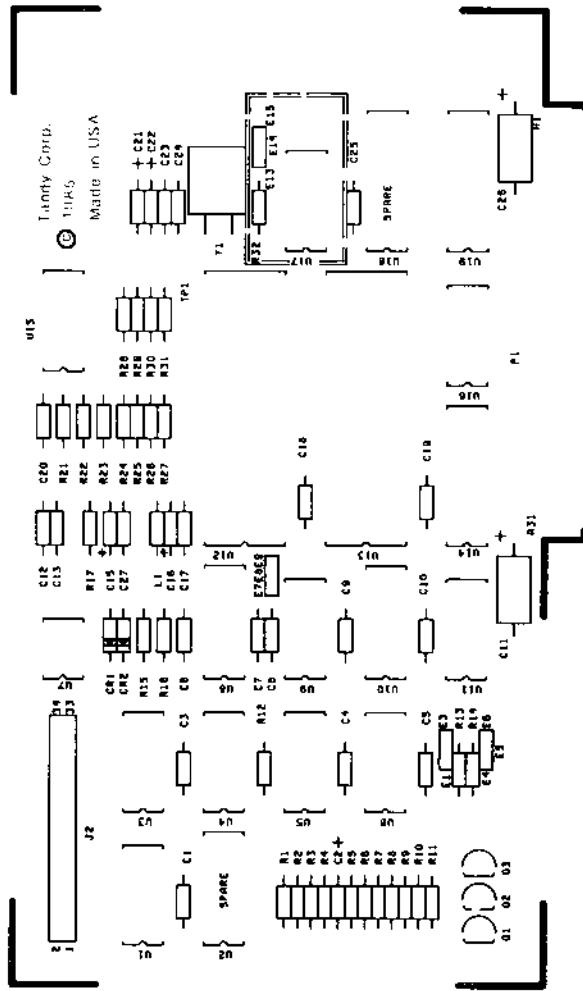
\* "Normal" jumper positions. These functions are also valid if no jumpers are installed.



\*\*\*\*\*  
\* \* \* \* \*  
\* \* \* \* \*  
\* \* \* Floppy Disk Controller \*  
\* \* \* \* \*  
\* \* \* Section 2 \*  
\* \* \* \* \*  
\* \* \* Schematics & Component layout \*  
\* \* \* \* \*  
\*\*\*\*\*

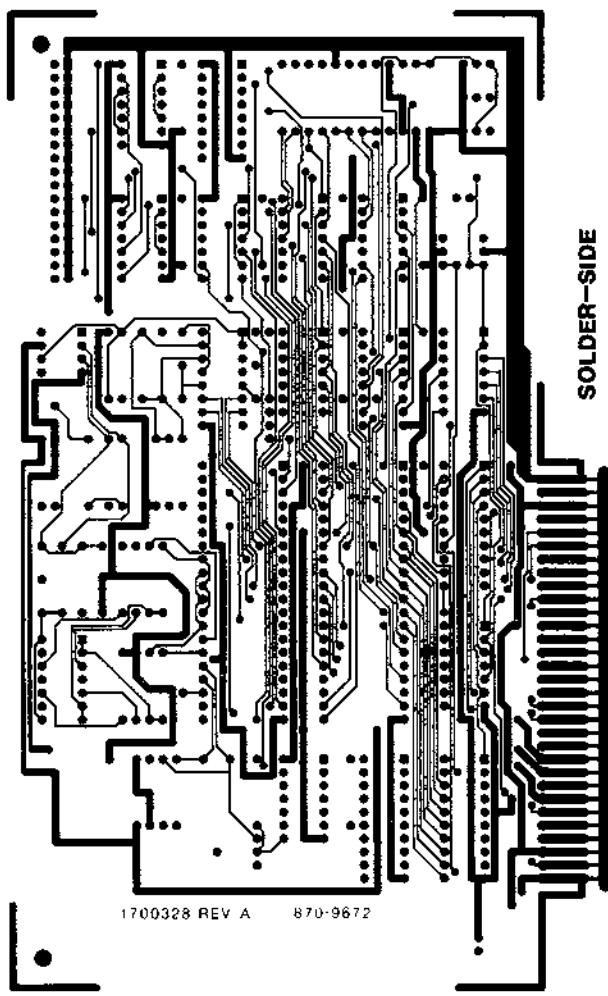


1700328 REV A

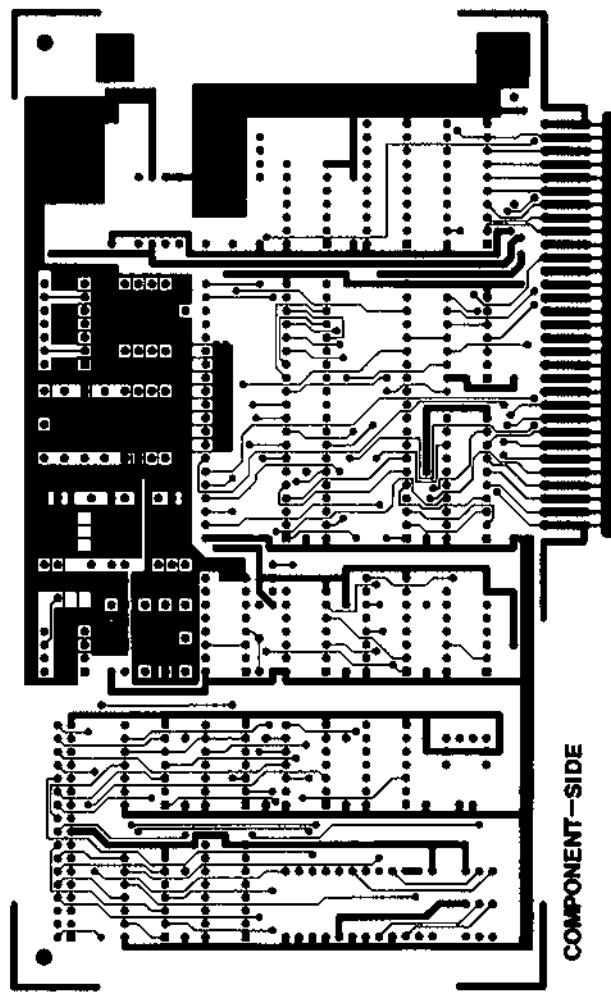


## SILKSCREEN

A V3R 8550011



1700328 REV A



COMPONENT-SIDE



\*\*\*\*\*  
\* \* \* \* \*  
\* \* \* \* \*  
\* \* \* Floppy Disk Controller \* \*  
\* \* \* \* \*  
\* \* \* Section 3 \* \*  
\* \* \* \* \*  
\* \* \* PAL Equations PAL16L8 \* \*  
\* \* \* \* \*  
\*\*\*\*\*

November 15, 1985



```
/********************************************/  
/* THIS IS THE SET OF EQUATIONS USED FOR GENERATING THE */  
/* CONTROL SIGNALS FOR THE WD FLOPPY DISK CONTROLLER */  
/* OPTION CARD. */  
/* TARGET DEVICE(S): CUPL -JFX PALL6L8 A:FLOPWD */  
/********************************************/  
  
/*INPUTS*/  
  
pin 1 = aen;  
pin 2 = iow;  
pin 3 = ior;  
pin 4 = sa0;  
pin 5 = sal;  
pin 6 = sa2;  
pin 7 = sa3;  
pin 8 = sa7;  
pin 9 = sax;  
pin 11 = dchg;  
pin 13 = dack;  
pin 14 = asel;  
  
/*OUTPUTS*/  
  
pin 12 = !selfc;  
pin 15 = !oen;  
pin 16 = !csel;  
pin 17 = !ldfcr;  
pin 18 = !ldccr;  
pin 19 = sd07;  
  
/*OUTPUT EQUATIONS*/  
  
!sd07 = !dchg;  
sd07.oe = oen;  
ldccr = !sax & !sa0 & sal & !sa2 & !sa3 & sa7 & !aen &  
       !iow & asel  
     # !sax & !sa0 & sal & !sa2 & !sa3 & !sa7 & !aen &  
       !iow & !asel;  
ldfcr = !sax & sa0 & sal & sa2 & !sa3 & sa7 & !aen & !iow  
       & asel  
     # !sax & sa0 & sal & sa2 & !sa3 & !sa7 & !aen & !iow  
       & !asel;  
csel = !dack  
      # ldfcr  
      # ldccr  
      # !sax & !sal & sa2 & !sa3 & sa7 & !aen & asel  
      # !sax & !sal & sa2 & !sa3 & !sa7 & !aen & !asel;  
oen = !sax & sa0 & sal & sa2 & !sa3 & sa7 & !aen & !ior  
     & asel  
   # !sax & sa0 & sal & sa2 & !sa3 & !sa7 & !aen & !ior  
     & !asel;  
selfc = !sax & !sal & sa2 & !sa3 & sa7 & !aen & asel  
      # !sax & !sal & sa2 & !sa3 & !sa7 & !aen & !asel;
```

Date 07/29/85  
Assembly floppy address decoder  
Location ul5

===== Expanded Product Terms =====

csel ->  
    !dack  
    # ldfcr  
    # ldccr  
    # !aen & asel & !sal & sa2 & !sa3 & sa7 & !sax  
    # !aen & !asel & !sal & sa2 & !sa3 & !sa7 & !sax

ldccr ->  
    !aen & asel & !iow & !sa0 & sal & !sa2 & !sa3 &  
    sa7 & !sax  
    # !aen & !asel & !iow & !sa0 & sal & !sa2 & !sa3 &  
    !sa7 & !sax

ldfcr ->  
    !aen & asel & !iow & sa0 & sal & sa2 & !sa3 & sa7  
    & !sax  
    # !aen & !asel & !iow & sa0 & sal & sa2 & !sa3 &  
    !sa7 & !sax

oen ->  
    !aen & asel & !ior & sa0 & sal & sa2 & !sa3 & sa7  
    & !sax  
    # !aen & !asel & !ior & sa0 & sal & sa2 & !sa3 &  
    !sa7 & !sax

sd07 ->  
    !dchg

sd07,oe ->  
    oen

selfc ->  
    !aen & asel & !sal & sa2 & !sa3 & sa7 & !sax  
    # !aen & !asel & !sal & sa2 & !sa3 & !sa7 & !sax

asel.oe ->  
    0

csel.oe ->  
    1

dack.oe ->  
0

ldccr.oe ->  
1

ldfcr.oe ->  
1

oen.oe ->  
1

selfc.oe ->  
1

Symbol Table

Pol	Name	Ext	Pin	Type	Used	Max
	aen		1	V	-	-
!	asel		14	V	-	-
!	csel		16	V	5	7
!	dack		13	V	-	-
	dchg		11	V	-	-
!	ior		3	V	-	-
!	iow		2	V	-	-
!	ldccr		18	V	2	7
!	ldfcr		17	V	2	7
!	oen		15	V	2	7
	sa0		4	V	-	-
	sa1		5	V	-	-
	sa2		6	V	-	-
	sa3		7	V	-	-
	sa7		8	V	-	-
	sax		9	V	-	-
	sd07		19	V	1	7
!	sd07	oe	19	X	1	1
!	selfc		12	V	2	7
	asel	oe	14	D	1	1
	csel	oe	16	D	1	1
	dack	oe	13	D	1	1
	ldccr	oe	18	D	1	1
	ldfcr	oe	17	D	1	1
	oen	oe	15	D	1	1
	selfc	oe	12	D	1	1

LEGEND D : default var    F : field    I : intermediate var  
 U : undefined            V : var        X : extended var  
 N : node                M : extended node

## Fuse Plot

```

Pin #19
0000 -----
0032 -----
0064 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0096 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0128 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0160 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0192 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0224 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

Pin #18
0256 -----
0288 -x-x-----x-x-----x-xx-x-----x-
0320 -x-x-----x-x-----x-x-x-x-----x-
0352 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0384 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0416 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0448 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0480 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

Pin #17
0512 -----
0544 -x-x-----x-x-----x-xx-x-----x-
0576 -x-x-----x-x-----x-x-x-x-----x-
0608 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0640 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0672 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0704 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0736 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

Pin #16
0768 -----
0800 -----x-----
0832 -----
0864 -----
0896 -----x-----x-----x-x-----x-
0928 -----x-----x-x-----x-x-x-----x-
0960 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0992 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

Pin #15
1024 -----
1056 -----x-x-----x-x-----x-xx-x-----x-
1088 -----x-x-----x-x-----x-x-x-x-----x-
1120 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1152 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1184 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1216 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1248 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

```

Pin #14

1280 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx  
1312 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx  
1344 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx  
1376 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx  
1408 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx  
1440 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx  
1472 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx  
1504 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

Pin #13

1536 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx  
1568 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx  
1600 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx  
1632 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx  
1664 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx  
1696 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx  
1728 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx  
1760 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

Pin #12

1792 -----  
1824 ---x-----x-x-----xx-x---x--  
1856 ---x-----x-x-----x-x-x---x--  
1888 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx  
1920 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx  
1952 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx  
1984 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx  
2016 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

LEGEND X : fuse not blown

- : fuse blown





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\* \* \* \* \*  
\* \* \* \* \*  
\* \* \* Floppy Disk Controller \* \*  
\* \* \* \* \*  
\* \* \* Section 4 \* \*  
\* \* \* \* \*  
\* \* \* Parts list \* \*  
\* \* \* \* \*  
\*\*\*\*\*



Tandy 3000 Floppy Disk Controller Sub Assembly

Symbol	Description	Part No.
	Tandy 3000 Floppy Disk Controller Sub Assembly	AX-0203
	T3000 FDC PCB, Rev. A	8709672A
C1,3-5,8-10,12, 13,17-29	Capacitor .1 UF 50V 80/20% Mono Ax CC-104JJLA	
C2	Capacitor 4.7 UF 15V 20% Tant Ax. CC-475MDTA	
C6	Capacitor 180 PF 50V 5% Mono Ax. CC-181JJLA	
C7	Capacitor 220 PF 50V 5% Mono Ax. CC-473KJLA	
C11,26	Capacitor 2.2 UF 16V 20% Elect Ax. CC-225WDAA	
C15	Capacitor 2.2 UF 10V 10% Tant Ax. CC-225KCTA	
C16,21,22	Capacitor 1 UF 20V 10% Tant Ax. CC-105KETA	
C20	Capacitor .01 UF 50V 10% Mono Ax. CC-221JJLA	
C23,24	Capacitor 10 PF 50V 5% Mono Ax. CC-111JJLA	
C27	Capacitor .047 UF 50V 10% Mono Ax. CC-103KJLA	
CR1,2	Diode 1N4148	DX-0022
E1-9	Staking Pin	AHB-9682
J2	Connector 34-Pin Post Header	AJ-7286
L1	Inductor 4.7 uH 10%	ACA-8332
Q1-3	Transistor 2N3904	AMX-3583
R1-4,12	Resistor 150 Ohm 1/4W 5%	N-0142EEC
R5	Resistor 27K Ohm 1/4W 5%	N-0316EEC
R6,8,9	Resistor 1.2K Ohm 1/4W 5%	N-0199EEC
R7	Resistor 220 Ohm 1/4W 5%	N-0149EEC
R10	Resistor 487 Ohm 1/8W 1%	N-0810BBE
R11,22,23	Resistor 100 Ohm 1/8W 1%	N-0132BBE
R13,14	Resistor 4.7K Ohm 1/4W 5%	N-0247EEC
R15	Resistor 1K Ohm 1/8W 1%	N-0196BEE
R16	Resistor 499 Ohm 1/8W 1%	N-0833BBE
R17	Resistor 332 Ohm 1/8W 1%	N-0792BBE
R21	Resistor 220 Ohm 1/8W 1%	N-0146BEE
R24,25,28,29	Resistor 100 Ohm 1/4W 5%	N-0132EEC
R26,27,30,31	Resistor 1.21K Ohm 1/8W 1%	N-0546BBE

Tandy 3000 Floppy Disk Controller Main Assy

Symbol	Description	Part No.
Tandy 3000 Floppy Disk Controller Main Assy		
U12	T3000 FDC Sub Assembly	AX-0203
U13	IC WD16C92	MX-5912
U14	IC UPD765A	MX-5934
	IC 16L8A PAL	MX-6980
Symbol	Description	Part No.
U1,3,4	IC 7438	AMX-5709
U5,6	IC 74LS14	MX-6181
U7	IC TL087CP	MX-4967
U8	IC 74LS629	AMX-4663
U9	IC 74LS00	MX-3479
U10	IC 74LS174	AMX-3565
U11	IC 74LS30	AMX-3556
U12,13	Socket, 40-Pin DIP	AJ-6580
U14	Socket, 20-Pin DIP	AJ-6760
U15	IC MPQ6700 ARY	MX-5731
U16	IC 74LS08	AMX-3698
U19	IC 74LS245	AMX-4470
Y1	Crystal 24 MHz (Fundamental)	MX-1286

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\*      1.2 Meg. Floppy Disk Drive      \*  
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\*  
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**High Density 1.2 Meg. Mitsubishi M4854-3S and MF504A-3 drives**

The Tandy 3000 uses the Mitsubishi M4854-3S and MF504A-3 flexible disk drives with a capacity of 1.2 Meg. These high performance double sided 5.25" drives can run normal density or high density media. These drives can be configured to run 300 rpm (40 or 80 cylinders, or 360 rpm high density 80 cylinders. The drives are normally run in the Tandy 3000 in the high density 96 tpi (80 cylinders) mode but can read or write to any compatable 5.25" diskette.

The following pages contain the specifications for your reference in maintenance, troubleshooting and repair of the drives.

Contents	Section
M4854-3S Normal Jumper Settings	1
M4854-3S Schematics and Component Layout	2
M4854-3S Maintenance Manual	3
M4854-3S Standard Specifications	4
M4854-3S Parts List	5
MF504A-3 Normal Jumper Settings	6
MF504A-3 Schematics and Component Layout	7
MF504A-3 Maintenance Manual	8
MF504A-3 Technical Manual	9
MF504A-3 Standard Specifications	10
M4854-3S Parts List	11

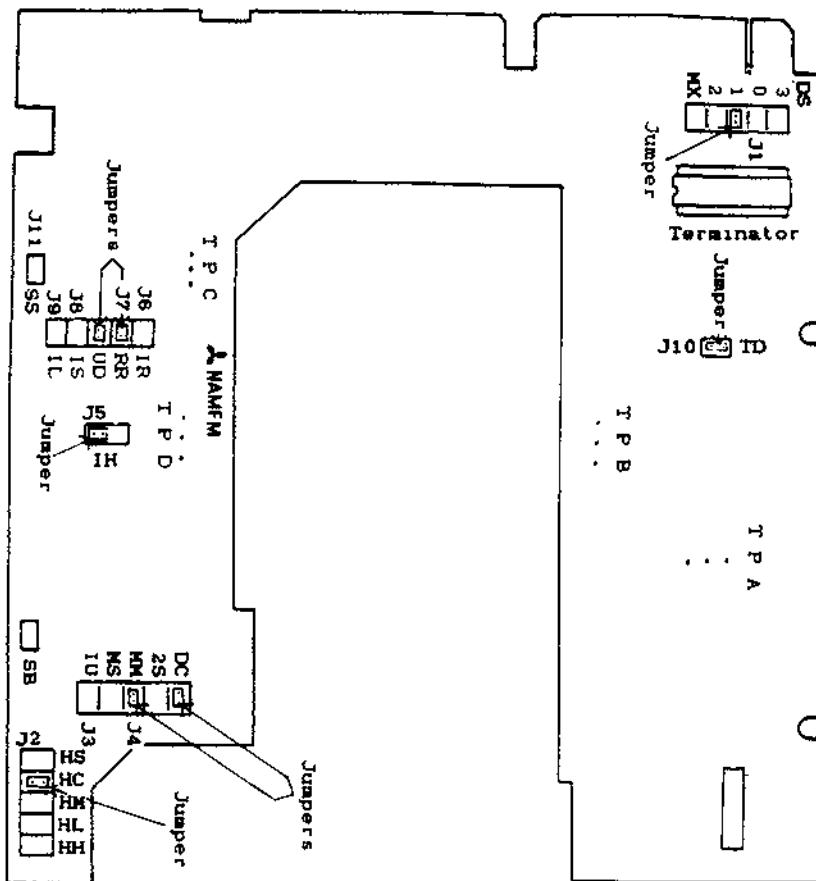


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\* \*  
\* \*  
\* 1.2 Meg. Floppy Disk Drive \*  
\* \*  
\* Section 1 \*  
\* \*  
\* Jumper settings \*  
\* \*  
\*\*\*\*\*



## 1.2 Meg Disk Drive Servo/Logic Board Jumper Settings

1. If the drive is a Mitsubishi Model 4854 be sure that HC, DC, MM, DSL, RR, UD, SB, TD and 11H on the drive servo/logic board are jumpered.



**Figure 1**  
**Drive logic board**



\*\*\*\*\*  
\* \* \* \* \*  
\* \* \* \* \*  
\*      1.2 Meg. Floppy Disk Drive      \*  
\* \* \* \* \*  
\*              Section 2      \*  
\* \* \* \* \*  
\*      Schematics & Component layout      \*  
\* \* \* \* \*  
\*\*\*\*\*



**DISK DRIVE  
SCHEMATICS AND  
LOGIC MANUAL**

M4854-347USA

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\* 1.2 Meg. Floppy Disk Drive \*  
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\* Section 3 \*  
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\* Maintenance manual \*  
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Maintenance Manual was not available at time of printing



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\* 1.2 Meg. Floppy Disk Drive  
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\* Section 4  
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\* Standard specifications  
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**5.25 INCH FLEXIBLE DISK DRIVE  
STANDARD SPECIFICATIONS  
M4854-347USA**

 MITSUBISHI ELECTRIC CORPORATION



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## CHAPTER 1 INTRODUCTION

The Mitsubishi M4854-3S Flexible Disk Drive is a high performance double side Disk Drive designed for use with standard 5.25 inch diskettes. This device can perform read/write operation both with high density and normal density media.

### 1.1 General Description

1. Use of high density disk with the M4854-3S Flexible Disk Drive allows for a formatted memory capacity exceeding 1Mb, a format compatible with an 8 inch floppy disk drive. It is also a magnetic disk drive which makes possible both read and write operations with normal density media used up to now. However, 48TPI normal density media can read and write, but only 96TPI drive can read the revised data.
2. Input pin 2 is used for switching between high density and normal density media. This allows the rotational speed to be switched between 360 rpm when high density is selected, and 300 rpm when normal density is selected. The READ/WRITE circuit is also switched at the same time.
3. When normal density has been selected, the setting can be performed so that only the READ/WRITE circuit is switched, while the rotation remains at 360 rpm.
4. A wide variety of user options makes it possible for this device to be used in various operations.
5. Half height (41 mm) dimension of conventional model and two M4854-3S units can be fit into the industry standard size for one 5-1/4 inch flexible disk drive.
6. Ejector for the diskette provides ease-of use in the handling the diskette.
7. The soft-toch, circular gimbal-supported magnetic head provides stable contact with the medium.

- 8. A high-precision stepping motor and steel bands are used in a combination for the magnetic head position mechanism to achieve a fast 3 ms access time between tracks.
- 9. Compact Brushless D.C. Motor gives maintenance free.
- 10. Stable media interchangeability by keeping enough window time margin at off-track in a wide range of ambient conditions.
- 11. Low power consumption can be achieved by a diskette detection function.
- 12. Dynamic clamping function provides high reliability of diskette centering in order to avoid possible mis-clamping.

## 1.2 Specifications

### 1.2.1 Performance specifications (Table 1-1)

			high density media		normal density media				
Encoding method			FM	MFM	FM	MFM			
Transfer rate (Kbits/s)			250	500	(150)/125	(300)/250			
Memory capacity	Unformatted	Track (K bytes)	5.208	10.416	3.125	6.25			
		Disk (K bytes)	833	1666	500	1000			
		Sector (K bytes)	0.128	0.256					
		Track (K bytes)	3.328	6.656					
	Formatted	Disk (K bytes)	532.48	1064.96					
		Sector (K bytes)	0.256	0.512	0.128	0.256			
		Track (K bytes)	3.840	7.680	2.048	4.096			
		Disk (K bytes)	614.40	1228.80	327.68	655.36			
		Sector (K bytes)	0.512	1.024					
		Track (K bytes)	4.096	8.192					
		Disk (K bytes)	655.36	1310.72					
Recording density			BPI	4935	9870	2961			
Magnetic flux reversal density			FCI	9870	9870	5922			
Number of tracks				160	160/80				
Track density			TPI		96	96/48			
Number of cylinders				80	80/40				
Track radius	00 Track	Side 0		57.150 mm (2.2500 in)					
		Side 1		55.033 mm (2.1667 in)					
	79 Track	Side 0		36.248 mm (1.4271 in)					
		Side 1		34.131 mm (1.3438 in)					
Rotation speed				360 rpm	(360)/300 rpm				
Motor starting time				500msec or less	(500)/400msec or less				
Average latency time				83.3msec	(83.3)/100msec				
Rotation speed change time (360rpm - 300rpm)				400msec or less					
1 Track Access time				3msec					
Settling time				15msec or less					
Average Access time				94msec					

Note: ( ) of normal density media is 360 rpm selected.

1.2.2 Physical specifications (Table 1-2)

<b>DC power requirements</b>	
+5V	+5V + 5%, 0.5 A typical 0.7 A max
+12V	+12V + 5%, 0.7 A typical (seeking) 1.0 A max (Spindle motor operating)
<b>Operating environmental conditions</b>	
Ambient temperature	5°C to 43°C (41°F to 109.4°F)
Relative humidity	20% to 80% (Maximum wet bulb temperature: 29°C (85°F))
<b>Non-operating environmental conditions</b>	
Ambient temperature	-20°C to 51°C (-4°F to 125°F)
Relative humidity	5% to 95%
<b>Heat dissipation</b>	9.7 Watts Continuous seek(typical) 5 Watts Standby (typical) 4 Watts Motor off (typical)
<b>Physical dimensions</b>	(Except for front panel)
Height	41 mm (1.62 in)
Width	146 mm (5.75 in)
Depth	195 mm (7.7 in)
<b>Front panel dimensions</b>	42 x 148.0 mm (1.65 x 5.83 in)
<b>Weight</b>	1.3 kg (2.9 lbs)

### 1.2.3 Reliability specifications (Table 1-3)

MTBF	10,000 POH or more
MTTR	30 minutes
Unit life	5 years or 20,000 POH whichever comes first
Media life	
Rotational life	$3.5 \times 10^6$ pass/track or more
Error rate	
Soft read error	$10^{-9}$ bit (Two retries)
Hard read error	$10^{-12}$ bit
Seek error	$10^{-4}$ seek

Table 1-3. Table of reliability specification.

## CHAPTER 2 OPERATION OF MAJOR COMPONENTS

### 2.1 System Operation

The M4854-3S Flexible Disk Drive consists of a medium rotating mechanism, two read/write heads, an actuator to position the read/write heads on tracks, and electronic circuits to read and write data, and to drive these components.

The rotation mechanism clamps the medium inserted into the drive to the spindle, which is directly coupled to the DC brushless direct-drive motor, and rotates it at 360 rpm or 300 rpm. The positioning actuator moves the read/write head over the desired track of the medium. Then, read or write data.

### 2.2 Electronic Circuits

The electronic circuits to drive the individual mechanisms of the M4854-3S are located on a single printed-circuit board, which consists of the following circuits:

- o Line driver and receiver that exchange signals with the host system
- o Drive selection circuit
- o Index detection circuit
- o Head positioning actuator drive circuit
- o Head loading solenoid drive circuit
- o Read/write circuit
- o Write protect circuit
- o Track 00 detection circuit
- o Drive ready detection circuit
- o Head selection circuit
- o In use and panel indicator LED drive circuit

The spindle motor driving circuit is within the PCB that is integrated with the motor. It consists of a rotation speed control servo circuit, motor driving circuit, speed detecting device, and hall detecting device.

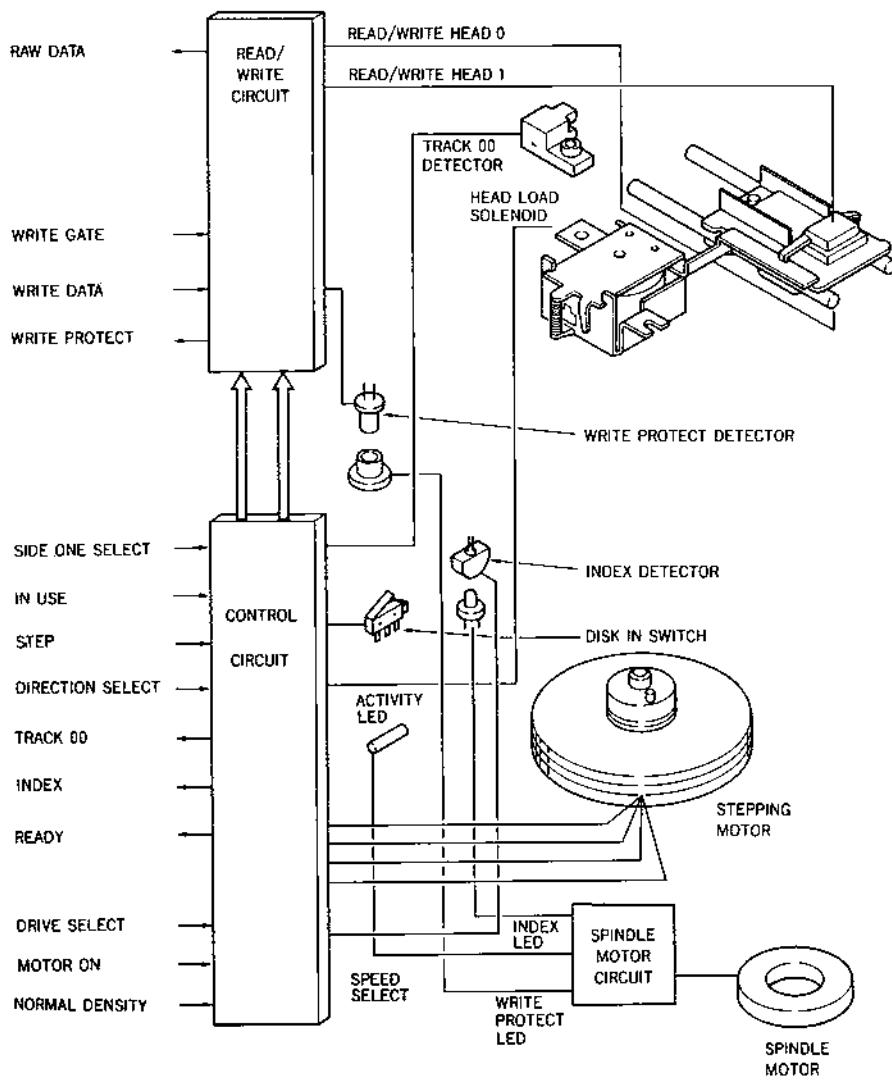


Fig. 1 Functional View

## 2.3 Rotation Mechanism

The diskette rotation mechanism used the DC brushless direct-drive motor to directly rotate the spindle at 360 rpm or 300 rpm.

## 2.4 Positioning Mechanism

The positioning mechanism positions the read/write heads as described below.

The head carriage assembly is fastened to the steel band secured around the capstan of a stepping motor; a 1.8° turn of the stepping motor moves the read/write head one track in the designated direction, thus positioning the read/write head.

This drive system is temperature compensated to minimize read/write head deviations from the disk tracks caused by ambient temperature change.

## 2.5 Read/Write Heads

The read/write heads are MnZn magnetic ferrite.

Each read/write head has three ferrite head cores, consisting read/write core and erase cores on both sides of the read/write core to erase the space between tracks (tunnel erase).

The two read/write heads, which are located face-to-face with a disk between them, are mounted on compliant, gimbal springs so that the heads track the disk with good contact to enable maximum reproduction of the signals from the disk. The high surface tracking ability of the gimbal keeps the disk free of stress, and thus improves diskette life.

## CHAPTER 3 ELECTRICAL INTERFACE

There are two kinds of electrical interfaces: Signal interface and DC power interface.

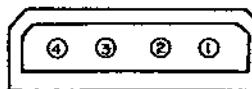
The signal interface sends and receives control signals and read/write data between the M4854-3S and the host system via the J1/P1 connector.

The DC power interface drives the spindle drive motor of the disk drive, and supplies power to the electronic circuits and the stepping motor which drives the read/write head positioning mechanism via the J2/P2 connector.

The signals and pin arrangement of these two types of interfaces are shown in Tables 3-1 and 3-2.

Table 3-1 DC Power Connector Pin Arrangement (J2/P2)

Source voltage	Pin number	Remarks
+12 V DC	1	
+12 V DC return	2	
+5 V return	3	
+5 V DC	4	



P2 connector

Table 3-2 Signal Connector Pin Arrangement (J1/P1)

Signal	Signal Pin Number	Ground Return Pin Number
NORMAL DENSITY *1	2	1
IN USE *2	4	3
DRIVE SELECT 3	6	5
INDEX	8	7
DRIVE SELECT 0	10	9
DRIVE SELECT 1	12	11
DRIVE SELECT 2	14	13
MOTOR ON	16	15
DIRECTION SELECT	18	17
STEP	20	19
WRITE DATA	22	21
WRITE GATE	24	23
TRACK Q0	26	25
WRITE PROTECT	28	27
READ DATA	30	29
SIDE ONE SELECT	32	31
READY *3	34	33

\*1: This line is used for switching between high and normal density.

\*2: The line can be used as HEAD LOAD instead of IN USE with the jumper plug setting on the PCB.

\*3: This line can be used as HOLD READY and DISK CHANGE instead of READY with the jumper setting on the PCB.

### 3.1 Signal Interface

The signal interface is classified into control signals and data signals. These interface signal lines are all at TTL levels. The meanings and characteristics of the signal levels are as follows:

- o True = Logical "0" = VL 0 V to +0.4V  
Iin 40 mA maximum
- o False = Logical "1" = VH +2.5 V to +5.25 V  
Iin 0 mA
- o Input impedance = 150 Ohms

#### 3.1.1 Cabling method and input line termination

The drive uses a daisy chain system of cable connections. A single ribbon cable or twisted-pair cable may be fitted with multiple connectors to permit connection of up to four drives.

The connected drives are multiplex-controlled by drive select lines, and any one of the drives can be accessed.

The cabling method and input line termination are shown in Fig. 3-1. A maximum of eight input signal lines, plus the drive select lines, may be terminated at the disk drive proper operation of the drives requires termination at or near the drive connected to the end of the interface cable farthest from the host system.

The drive has detachable terminator modules on the printed-circuit board to terminate these input signal lines.

When a drive is shipped from the factory, its terminators are installed on the printed-circuit board.

Keep the terminators connected in the drive that is connected to the end of the interface cable, and disconnect the terminators in all the other drives.

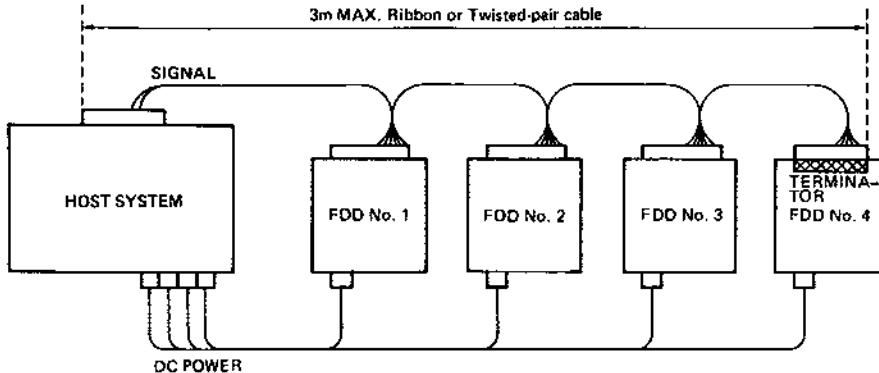


Fig. 3-1 Cabling Method (Sketch)

### 3.1.2 Line driver and line receiver

The recommended interface line driver and line receiver circuits for the host system and the drives are shown in Fig. 3-2.

It is suggested that a Schmitt trigger circuit with a hysteresis characteristic at the switching level be used for the line receiver to improve the noise resistance of the interface lines.

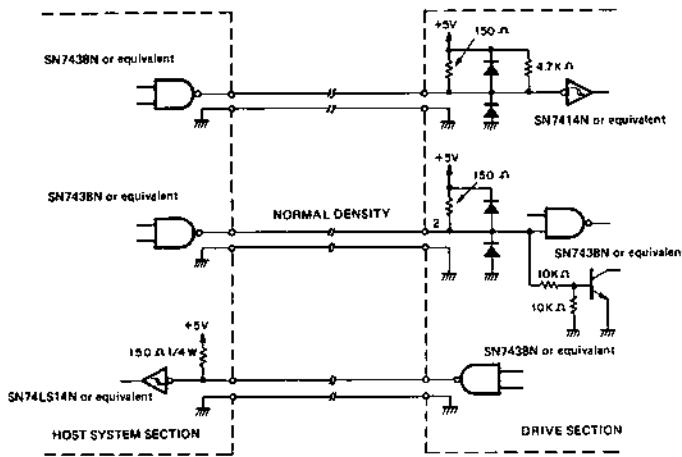


Fig. 3-2 Recommended Line Driver and Line Receiver Circuits

### 3.1.3 Short plug

The short plug sets the conditions for selecting the drive, starting the spindle motor, lighting the LED of the panel indicator and sending the ready signal.

The following is the explanation of features of the short plug.

#### (1) Drive selection conditions DS0-3, MX (location A6 of PCB)

##### 1.1) DS0-3

If multiple connection is made with the system and the drive, by short-circuiting one of the DS0-3, the corresponding DRIVE SELECT line will select the drive with the logical "0" only, and input signals can be received.

For example, the drive that has had its DS0-3 short-circuited, will be selected when DRIVE SELECT 0 line is at logical "0".

##### 1.2) MX

When all of DS0-3 has been opened and MX short-circuited, the drive will always be selected regardless of the DRIVE SELECT line of the interface. However, in this case the control of the panel indicator LED can only be done with the IN USE signal. Furthermore, the power of the spindle motor cannot be controlled by DRIVE SELECT 0-3. Therefore it is necessary to revise the conditions to another.

\* DS1 is short-circuited at the factory before delivery.  
Resetting is necessary in order to use another drive number.

##### 1.3) The terminator of the DRIVE SELECT line conditions selection TD (Location D6 of PCB)

When TD is open, the terminator of the DRIVE SELECT line can be separated.

\* TD is shorted when the unit is shipped from the factory.

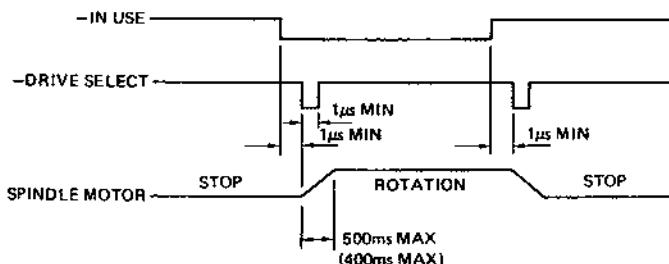
- 2) Head loading conditions selections HS, HM, HC, HL, (location J1 of PCB), & J2.
- 2.1) HS  
In the case HS is short-circuited, the head will be loaded by DRIVE SELECT 0 - 3.
- 2.2) HM  
In the case HM is short-circuited, the head will be loaded by the MOTOR ON signal.
- 2.3) HC  
In the case HC is short-circuited, the head will always be loaded regardless of the interface input signal.
- 2.4) HL  
In the case HL is short-circuited, the IN USE input signal (Pin 4 of connector J1/P1) and the DRIVE SELECT signal of the head will be loaded a logical "0". The logical product for all of the conditions for the above is taken by the HOLD READY conditions listed later on and the head code will be controlled. HS is short-circuited at the factory before delivery.

- (3) Spindle MOTOR ON conditions selection MM, MS (location H1 of PCB)

The conditions for Spindle MOTOR ON conditions are selected by the combination of opening and short-circuiting of MM and MS.

Short plug		Refer to	Notes
MS	MM		
open	short	3.1	Before delivery
short	open	3.2	
open	open	3.3	
short	short	3.4	

- 3.1) Power of the spindle motor is controlled by the MOTOR ON signal.
- 3.2) Power of the spindle motor is controlled by the drive select conditions that have been selected by DRIVE SELECT 0-3 signal.
- 3.3) Power of the spindle motor is controlled by the logic sum of the DRIVE SELECT 0-3 signals and MOTOR ON signal.
- 3.4) Power of the spindle motor is controlled by latching the IN USE signal with the reading edge of the DRIVE SELECT signal. At this time, the short plug IU will be short-circuited.



(Note) : The figures in brackets ( ) are for when the unit is at 300 rpm.

Fig. 5 Spindle mo-or on/off timing  
(IN USE latching)

- (4) Ready transmission selection conditions DC, 2S  
 (location H1 of PCB) RR (location D1 of PCB)

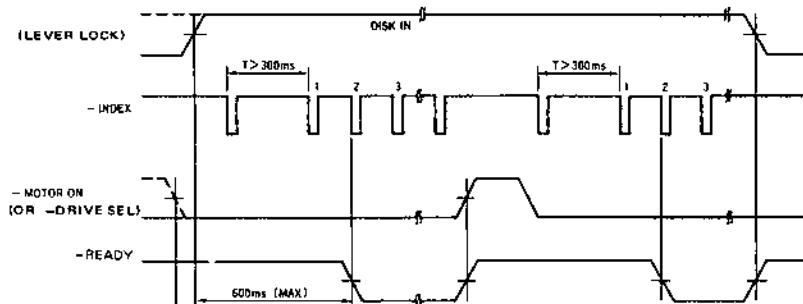
The ready transmission conditions below can be selected with the combination of opening and short-circuiting of DC and 2S.

Short plug		Refer to	Notes
DC	2S		
open	open	4.1	
open	short	4.2	
short	short	4.3	
short	open	4.4	Before delivery

#### 4.1) Standard READY

With the standard READY signal, after detection for a disk rotation period of less than 300 ms, the INDEX signal is detected by two pulses and a READY signal is sent to the interface. A maximum of 600 ms is required for the output of the READY signal.

The READY signal interrupts disk rotation and renders it NOT READY for all conditions.



Standard READY timeing

#### 4.2) Hold ready

Indicates that the diskette is inserted and the lever is locked. This ready is set within 600 ms from when the lever is locked. When the lever is cancelled, reset starts. In order to perform read/write operations, since ready will be held even if the Spindle motor is turned off, a minimum of 500 ms should be allowed to pass after the spindle MOTOR ON signal (DRIVE SELECT signal in the case when spindle MOTOR ON is done with DRIVE SELECT 0-3) is sent.

#### 4.3) Disk change

Indicates that the lever is cancelled immediately after POWER ON. After the lever has been locked, this signal will be cancelled with the trailing edge of the first DRIVE SELECT signal and will not change with any DRIVE SELECT signal afterwards.

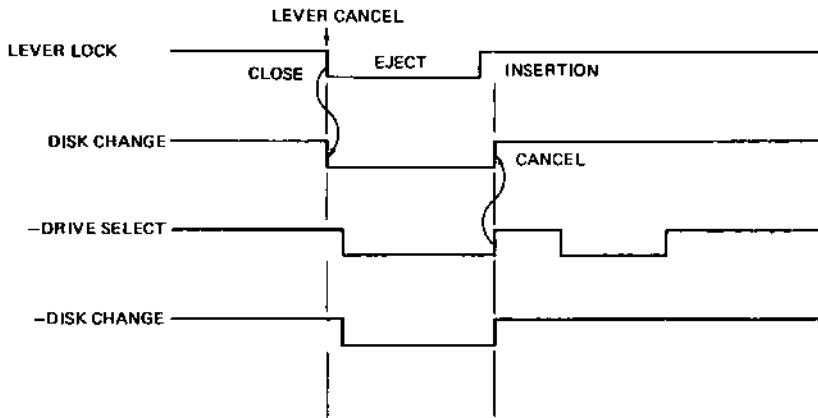


Fig. 6 Disk Change Timing

#### 4.4) Diskette change

This signal becomes active or logic low (logical "0") when the drive door has been disturbed (opened) and reset to the inactive state when the door is closed and a step pulse has been received by the drive.

#### 4.5) RR

In the case RR is short-circuited, the ready signal will be output after the logic product and the DRIVE SELECT signal will be taken.

In the case RR is open, this logic product will be deleted and the DRIVE SELECT signal and ready signal will be outputted regardlessly.

\* RR is shorted when the unit is shipped from the factory.

- (5) Head unloading conditions selection UD (location b1 of PCB). In the case UD is open, maintain the head loading mode until the disk rotates 3 to 4 times after the head loading signal becomes inactive. In the case UD is short-circuited, perform the head load operation that is synchronized with the head loading signals. UD is opened at the factory before delivery.
- (6) Panel indicator LED lighting conditions selection IU (location H1 of PCB) J3; IH (location E1 of PCB) J5; IR, IS, IL (location D1 of PCB) J6, J8, J9. Shown in Table 9.
- (7) Normal density condition selection SS (D1 on the PCB) J11; SB (G1 on the PCB)  
When SS is shorted and SB is open, the rpm of motor is set to 360 rpm by logical "1" of the NORMAL DENSITY signal, and the read/write circuitry is set for the use of high density media. The rpm of the motor is set to 300 rpm by logical "0" of the NORMAL DENSITY signal, and the read/write circuitry is set for the use of normal density media.  
When SS is open and SB is shorted, the rpm is not changed by the NORMAL DENSITY signal, but the read/write circuitry is adjusted as above. Logical "0" of the NORMAL DENSITY signal allows the use of normal density media with a transfer speed of 300 kb/sec. SS is shorted and SB is open when the unit is shipped from the factory.

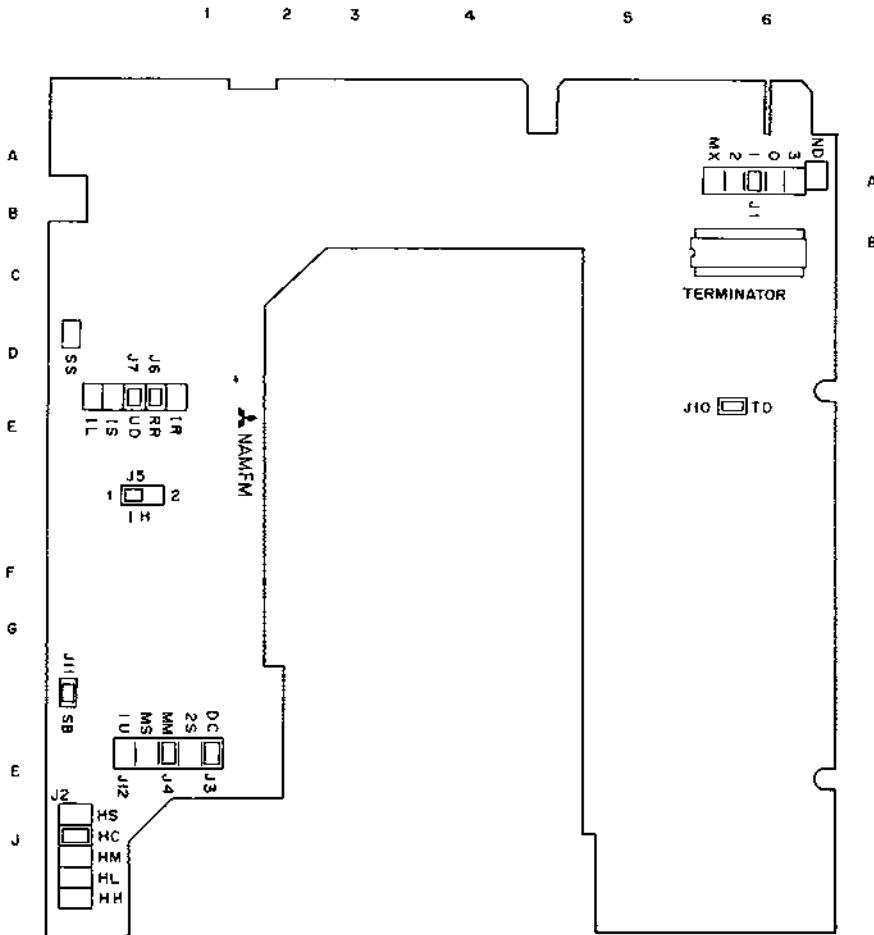
Table 9. Panel indicator LED lighting conditions

J 3	J 5	J 6	J 8	J 9	LED lighting conditions
[I U] Note 1	[I IH 2] Note 2	[I R]	[I S]	[I L]	If the IN USE signal is active, latching and lighting will be initiated with the reading edge of the DRIVE SELECT signal. Afterwards the LED will remain lighted even after the DRIVE SELECT signal is active. By inputting the DRIVE SELECT signal once again when the IN USE signal is inactive, the latching will be cancelled and the LED will go out with this reading edge. Furthermore, these lighting conditions become effective only when the drive is READY. (Note 4) This setting will be done at the factory before delivery.
[I U]	[I IH 2]	I R	[I S]	[I L]	The READY conditions will be cancelled from the above lighting conditions.
[I U]	[I IH 2]	[I R] or I R	[I S]	[I L]	LED will light with the logic sum of the DRIVE SELECT signal and the lighting conditions by the latching listed above. When the IR is short-circuited, the LED will light at the READY mode and logic product and will be delayed when IR is open. (The same is with the following.)
[I U]	[I IH 2]	[I R] or I R	[I S]	[I L]	The LED will light with the logic sum of the DRIVE SELECT and IN USE signals.
[I U]	[I IH 2]	[I R] or I R	[I S]	[I L]	The LED will light with the IN USE signal.
[I U]	[I IH 2]	[I R] or I R	[I S]	Note 3	The LED will light with the DRIVE SELECT signal.
-	[I IH 2]	-	-		The LED will light at head loading mode.
[I U]	[I IH 2]	-	[I S]	-	The LED will not light.

- Note 1. The enclosed names are those shorted by jumper plugs. Those not enclosed are open.
2. [I IH 2] indicates that side 1 is shorted by the insertion of a plug. [I IH 2] indicates that side 2 is shorted.
3. - indicates that the lighting conditions will not change whether open or short-circuited.
4. When the lighting conditions are included in the ready conditions, stand-by or hold ready transmission conditions are to be used.

Object	Name	Contents	Setting when shipped from the factory	Plug number																		
Selection of drive select	[DS0]	Drive select 0	<table border="1"> <tr><td>DS</td><td>○</td><td>○</td></tr> <tr><td>3</td><td>○</td><td>○</td></tr> <tr><td>0</td><td>○</td><td>○</td></tr> <tr><td>1</td><td>○</td><td>○</td></tr> <tr><td>2</td><td>○</td><td>○</td></tr> <tr><td>MX</td><td>○</td><td>○</td></tr> </table>	DS	○	○	3	○	○	0	○	○	1	○	○	2	○	○	MX	○	○	J1
DS	○	○																				
3	○	○																				
0	○	○																				
1	○	○																				
2	○	○																				
MX	○	○																				
[DS1]	Drive select 1																					
[DS2]	Drive select 2																					
[DS3]	Drive select 3																					
[MX]	The drive select which is usually set																					
[TD]	Connection to the terminator resistance of the DRIVE SELECT signal	[○ ○] TD	J10																			
Selection of head loading conditions	[HS]	Head loading by the DRIVE SELECT signal	<table border="1"> <tr><td>HS</td><td>○</td><td>○</td></tr> <tr><td>HC</td><td>○</td><td>○</td></tr> <tr><td>HM</td><td>○</td><td>○</td></tr> <tr><td>HL</td><td>○</td><td>○</td></tr> <tr><td>HH</td><td>○</td><td>○</td></tr> </table>	HS	○	○	HC	○	○	HM	○	○	HL	○	○	HH	○	○	J2			
HS	○	○																				
HC	○	○																				
HM	○	○																				
HL	○	○																				
HH	○	○																				
[HM]	Head loading by the MOTOR ON signal																					
[HC]	Normal head loading																					
[HL]	Head loading by the IN USE signal																					
[HH]	(not used)																					
Selection of MOTOR ON conditions	[MM MS]	Motor started by the MOTOR ON signal	<table border="1"> <tr><td>MM</td><td>○</td><td>○</td></tr> <tr><td>MS</td><td>○</td><td>○</td></tr> </table>	MM	○	○	MS	○	○	J4												
MM	○	○																				
MS	○	○																				
[MM MS]	Motor started by the DRIVE SELECT signal																					
[MM MS]	Motor started by the MOTOR ON signal or DRIVE SELECT signal																					
[MM MS IU]	Motor started by the IN USE signal latched by DRIVE SELECT signal																					
Selection of the signal transmitted from pin 34 of the interface (Connector P1)	DC 2S	STANDARD READY is sent	<table border="1"> <tr><td>DC</td><td>○</td><td>○</td></tr> <tr><td>2S</td><td>○</td><td>○</td></tr> <tr><td>MM</td><td>○</td><td>○</td></tr> <tr><td>MS</td><td>○</td><td>○</td></tr> <tr><td>IU</td><td>○</td><td>○</td></tr> </table>	DC	○	○	2S	○	○	MM	○	○	MS	○	○	IU	○	○	J3			
DC	○	○																				
2S	○	○																				
MM	○	○																				
MS	○	○																				
IU	○	○																				
DC 2S	HOLE READY is sent																					
DC 2S	DISK CHANGE is sent																					
DC 2S	(not used)																					
Gate selection for the above transmission signal	[RR]	Gated by DRIVE SELECT signal	<table border="1"> <tr><td>○</td><td>○</td><td>RR</td></tr> </table>	○	○	RR	J7															
○	○	RR																				
RR	Transmitted as is																					
Head unload condition selection	[UD]	Head unload delay released	<table border="1"> <tr><td>○</td><td>○</td><td>UD</td></tr> </table>	○	○	UD	-															
○	○	UD																				
UD	Head load mode is kept for 3 ... revolutions																					
Normal density condition selection	[SS SB]	360 rpm when high density is specified 300 rpm when normal density is specified	<table border="1"> <tr><td>○</td><td>○</td><td>SS</td></tr> </table>	○	○	SS	J11															
○	○	SS																				
SS SB	360 rpm for both high and normal density																					

Note 1 : [ ] means the plug position when shipped from factory.



Printed-Circuit Board Trace Location

### 3.1.4 Input signal lines

The disk drive has 12 input signal lines. Input signals can be classified into two types: One is multiplexed in a multi-drive system; and the other performs a multiplex operation.

The multiplexing signals are as follows:

- o DRIVE SELECT 0
- o DRIVE SELECT 1
- o DRIVE SELECT 2
- o DRIVE SELECT 3

#### (1) DRIVE SELECT 0 to DRIVE SELECT 3

When these drive select lines are at logical "0" level, a multiplexed I/O lines become active to enable read/write operation. These four separate input signal lines, drive select 0 to drive select 3, are provided for connecting four drives to one system and mutually multiplexing them. Jumper pins DS0, DS1, DS2, and DS3 on the printed-circuit board are used to select drive to be made active, corresponding to each of the DRIVE SELECT lines, and specify which of the drives is active.

\* DS1 is shorted before shipment from the factory, so this setting must be changed when establishing other select lines.

#### (2) SIDE ONE SELECT

This interface line is used to select which of the two sides of the deskette should be read/write operations. When this line is at logical "1," the side 0 head is selected; or when it is at logical "0," the side 1 head is selected. If the polarity of the side one select signal is reversed, delay read/write operation by more than 100  $\mu$ s before execution.

Upon completion of a write operation, reverse the polarity of the side one select signal after a delay of 590  $\mu$ s (\*1). The heads are tunnel type, with a physical core gap deviation between the read/write head and the erase heads so with no

delay, non-erased areas would be generated on the diskette due to a timing difference between the write data area and the erase area during write operation. This is prevented by delaying the erase current ON/OFF time of a few hundred microseconds within the disk drive. Therefore, the head select must not be reversed during this delay time. Also, the track access action must not be permitted for 590  $\mu$ s.

(\*1)

\*1: The interval is 1000  $\mu$ s when normal density at 300 rpm is specified.

(3) DIRECTION SELECT

This interface line controls the direction. (inward or outward) in which the read/write head should be moved when a step signal pulse is applied.

If the signal is at logical "1", the read/write head moves from the center of the diskette outward; if it is at logical "0", the head moves inward.

(4) STEP

This interface line is a pulse signal for moving the read/write head in the direction defined by the direction select line. The read/write head moves by one track each time a signal logical "1", and the step operation starts with the trailing edge of a negative-going pulse (reversal from logical "0" to logical "1").

The direction select line must be reversed more than 1  $\mu$ s before the trailing edge of the step pulse.

(5) WRITE GATE

When this interface line goes to logical "0", the write drive becomes active and the data given to the write data line is written on the selected side of the diskette. When it becomes Logical "1," the write drive becomes inactive and the read data logic is enabled. However, the protected read data is

output 590  $\mu$ s (\*1) after the write drive become inactive.  
Refer to CHAPTER 4 for the timing.

\*1: The interval is 1000  $\mu$ s when normal density at 300 rpm is specified.

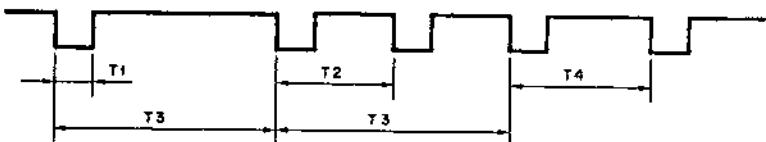
(6) WRITE DATA

Data to written on the diskette is sent to this interface line.

This line is normally at logical "1", and reverses the write current at the leading edge of a negative-going data pulse (reversal from logical "1" to logical "0") to write data bits.

This line is enabled when the write gate goes to logical "0", Fig. 3-3 shows the write data timing.

(Note: The interval is 1000  $\mu$ s when normal density at 300 rpm is specified.)



	MFM			
	FM			
	T1	T2	T3	T4
High density, 360 rpm	150 to 1100ns	$2.00\mu s \pm 10ns$	$4.00\mu s \pm 20ns$	$3.00\mu s \pm 15ns$
Normal density, 300 rpm	150 to 2100ns	$4.00\mu s \pm 20ns$	$8.00\mu s \pm 40ns$	$6.00\mu s \pm 30ns$
Normal density, 360 rpm	150 to 1800ns	$3.33\mu s \pm 17ns$	$6.67\mu s \pm 33ns$	$5.00\mu s \pm 25ns$

Fig. 3-3 Write Data Timing (FM, MFM Encoding)

(7) IN USE

An LED indicator on the front panel lights when this interface line goes to logical "0", The LED is also lit by the drive select.

(8) MOTOR ON

This interface line starts the spindle motor when it goes to logical "0." The write gate does not go to logical "0" until more than 500 ms (the interval is 400 ms for 300 rpm) after the motor-on line goes logical "0".

The motor-on line goes logical "1" to stop the motor and keep it off while the drive is out of operation, thus prolonging motor life.

(9) NORMAL DENSITY

This interface line selects whether read/write operations are set for high density or normal density media. Logical "1" corresponds to high density, and logical "0" corresponds to normal density.

When the normal density condition selection plugs SS (shorted) and SB (open) are used to switch the RPM, read/write operations are performed after a wait of more than 400 ms after transmission of this NORMAL DENSITY signal, during which time the RPM is stabilized. When the RPM is switched, write operations always begin after the read/write head moves to track 00. This erase power delay of a few hundred microseconds, which is generated within the drive, is necessary for switching when the head is moved to track 00 or when the power is turned on. When the normal density condition selection plug SS is open and SB is closed, the RPM is always 360 rpm, and there is no waiting, and no need to move the head to track 00.

### 3.1.5 Output signal lines

The drive has five standard output signal lines.

(1) INDEX

This interface line is normally logical "1" but sends a logical "0" output pulse 3.5 ms wide each time the diskette makes one revolution.

This signal signifies the start of a track on the rotating diskette. The index signal timing is shown in Fig. 3-4.

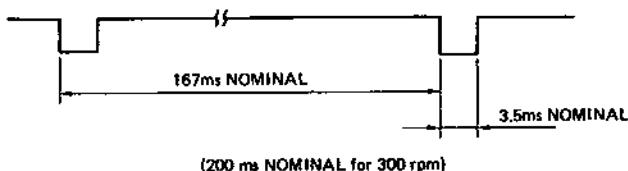


Fig. 3-4 Index Timing

(2) TRACK 00

When this interface line is at logical "0", it indicates that a read/write head of the selected drive is positioned on track 00. If the output of the selected drive is at logical "1", it indicates that the read/write head is positioned on a track other than track 00.

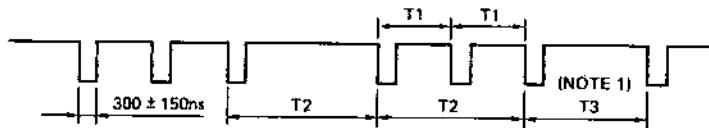
(3) READY

This interface line is logical "1" when the lever is cancelled. The line goes logical "0" (ready) if an index pluse is detected twice or more when the index hole is correctly detected, and the DC power (+5V and +12V) supplied after a diskette is inserted into the drive and the lever is locked.

(4) READ DATA

This interface line reads the data stored on the diskette with the read/write heads, and outputs raw data (combined clock and data signals) converted into pulse signals by an electronic circuit.

The read data line is normally logical "1" but it sends a logical "0" (negative-going) output pulse during a read operation. Fig. 3-5 shows allowable limits on timing variations with the usual diskette and bit shifts.



	MFM		
	FM		
	T1	T2	T3
High density, 360 rpm	$2.00\mu s \pm 400\text{ns}$	$4.00\mu s \pm 800\text{ns}$	$3.00\mu s \pm 600\text{ns}$
Normal density, 300 rpm	$4.00\mu s \pm 800\text{ns}$	$8.00\mu s \pm 1600\text{ns}$	$6.00\mu s \pm 1200\text{ns}$
Normal density, 360 rpm	$3.33\mu s \pm 667\text{ns}$	$6.67\mu s \pm 1333\text{ns}$	$5.00\mu s \pm 1000\text{ns}$

Note : Jitter caused by change in revolution speed are not considered in the above.

Fig. 3-5 Read Data Timing (FM, MFM Encoding)

#### (5) WRITE PROTECT

This interface signal notifies the host system of the insertion of a diskette with a write protect notch into the drive. The signal goes to logical "0" when a write-protected diskette is inserted into the drive. When the signal is at logical "0", write on the diskette is inhibited even if the write gate line becomes active.

#### 3.2 Power Interface

The disk drive requires two types of DC power supplies.

One is +12V DC, which drives the drive motor to rotate the disk. It is supplied to the stepping motor and the read/write circuit. The other is +5V DC, which is used for the logic circuit and the read/write circuit.

#### NOTE

The index LED is driven by the +12V DC.

### 3.2.1 DC power

DC power is supplied via connector J2/P2 on the back of the printed-circuit board. The specifications of the two DC voltages are shown in Table 3-3. The pin arrangement of connector J2/P2 is shown in Table 3-1.

Table 3-3 DC Power Specifications

DC voltage	Voltage variation	Current	Maximum ripple voltage (peak-to-peak)
+5 V DC	$\pm 0.25$ V ( $\pm 5\%$ )	0.7 A maximum 0.5 A typical	50 mV
+12 V DC	$\pm 0.6$ V ( $\pm 5\%$ )	1.3 A MAX (Spindle motor operating) 0.5 A typical at seek	100 mV

## CHAPTER 4 FUNCTIONAL OPERATION

### 4.1 Power On Sequencing

No read/write operation may be performed during the period of 100 ms or more from the start of DC power supply until the control signal stabilizes. And after the period of 600 ms from the Motor On, the drive comes to ready.

The read/write head may have been positioned on an incorrect track after switching the DC power on, so before starting a read/write operation, be sure to perform the step out operation until a track 00 signal is output to the interface line, and thus correctly position the read/write head.

### 4.2 Drive Selection

The disk drive daisy chain cabling system permits connection of multiple drives to a single cable.

These drives are selected when the drive select lines on the drive side become active. Only the drive whose drive select line is active sends and receives signals to and from the host system. The select lines on the drive must have different numbers if two or more drives are connected. If the same number is assigned, an operation error occurs due to interference among the interface output signals of the drives themselves.

### 4.3 Positioning Operation

The seek operation which moves the read/write head to the desired track selects a direction, inward or outward, depending on the polarity of the direction select signal, and moves the head by the step signal. If access to a track two or more tracks away is required, step signal are continuously sent until the head moves to the desired track.

Head movement starts with the trailing edge of the step pulse. Fig. 4-1 shows the operation timing.

#### 4.4 Side One Selection

The read/write heads located on both sides of the diskette are selected by the side one select signal. When the side one select line is high, the Side 0 head is selected. When it is low, the Side 1 head is selected.

#### 4.5 Read Operation

The required timing for read operations is shown in Fig. 4-1 and 3-5. These timing specifications are necessary for accurate read operation.

Two modes of encoding, FM and MFM, are used for the data stored on media. FM is used for single-density read, and MFM for double-density read.

A comparison of the FM and MFM encoding modes is shown in Fig. 4-3.

#### 4.6 Write Operation

The requiring timing for write operation is shown in Fig. 3-3 and 4-1.

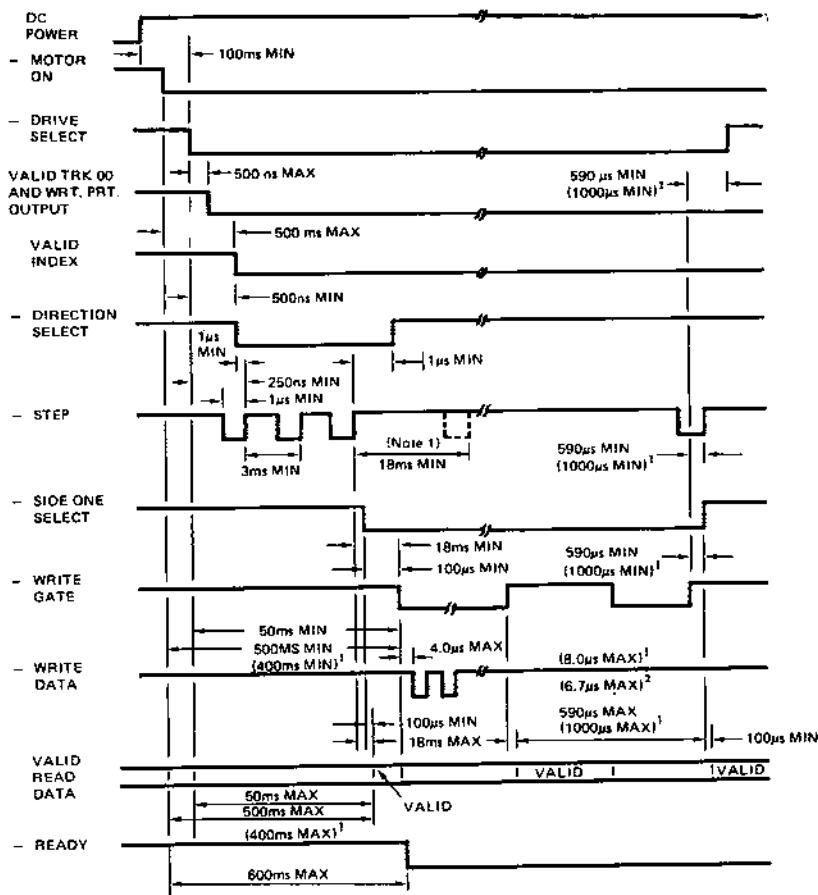
These timing specifications must be strictly observed to ensure an accurate write operation.

Write data can be encoded by either FM or MFM. The disk drive has good contact stability of the read/write heads on the medium and employs high-performance read/write heads, so no precompensation is necessary for correcting the bit shift effect when writing data in the MFM mode (double density).

In case of applying write precompensation, smaller compensation is recommended such as 150ns or smaller.

#### 4.7 READY and dynamic clamp functions

Refer to Fig. 4-2 for standard ready, hold ready, and the timing of the dynamic clamp.

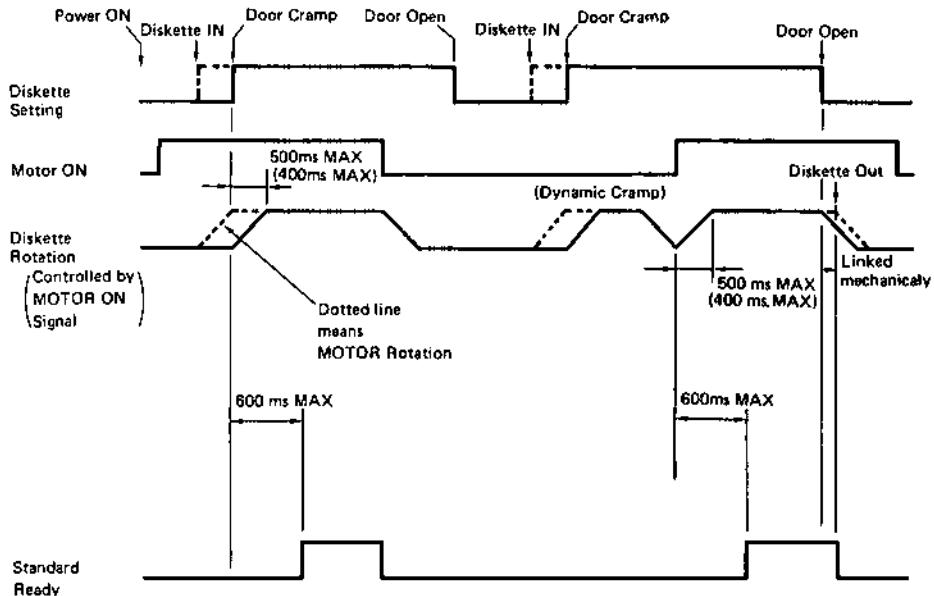


Note 1: When reversing direction, issue a next step pulse after more than 18 ms from the step pulse before inversion.

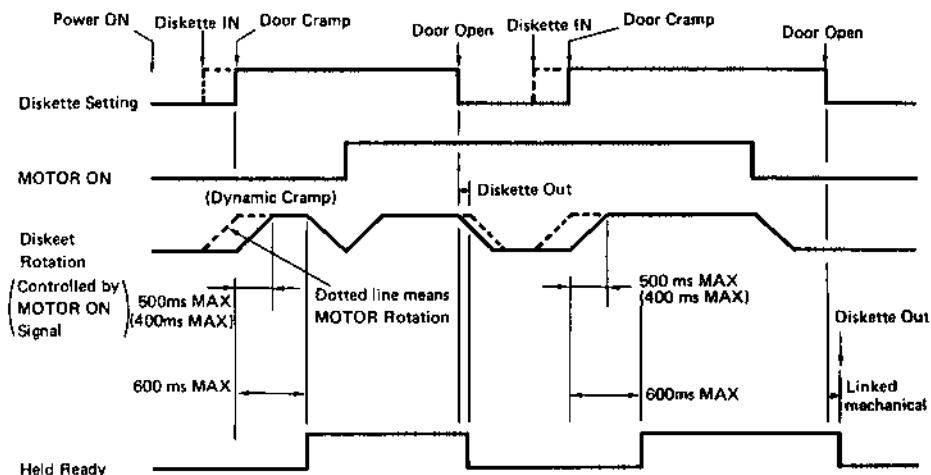
Note 2: The figures in brackets ( )<sup>1</sup> are for when the unit is specified for normal density at 300 rpm.  
The figures in brackets ( )<sup>2</sup> are for when the unit is specified for normal density at 360 rpm.

Fig. 4-1 Control and Data Timing

(1) Standard Ready, Dynamic Cramp



(2) Held Ready, Dynamic Cramp



Note 1: The figures in brackets ( ) are for when the unit is specified for 300 rpm.

Fig. 4-2 Ready and Dynamic Cramp Timing

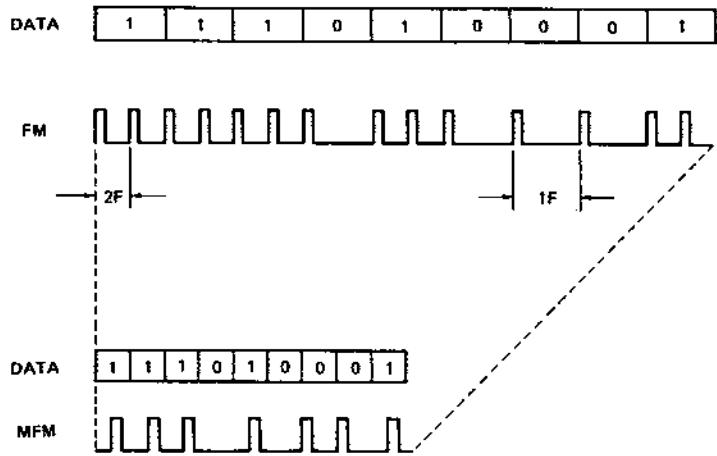


Fig. 4-3 Comparison of FM and MFM Encoding Systems

## CHAPTER 5 PHYSICAL INTERFACE

Electronic interfaces between the disk drive and the host system are accomplished with three connectors. Connector J1 is for the signal interfaces, connector J2 for the DC power supplies, and connector J7 for frame grounding. The connectors used for the disk drive and recommended mating connectors are described below.

### 5.1 Signal Connectors

J1 is a card-edge type, 34-pin (for both sides, or 17 pins for a single side) connector with even-numbered pins (2, 4, to 34) on the parts side and odd-numbered pins (1, 3, to 33) on the soldered side.

A key slot is provided between pins 4 and 6 for the polarity reversal prevention.

The dimensions of J1 are shown in Fig. 5-1.

Recommended Pl connectors that mate with J1 are shown in Tables 5-1 and 5-2.

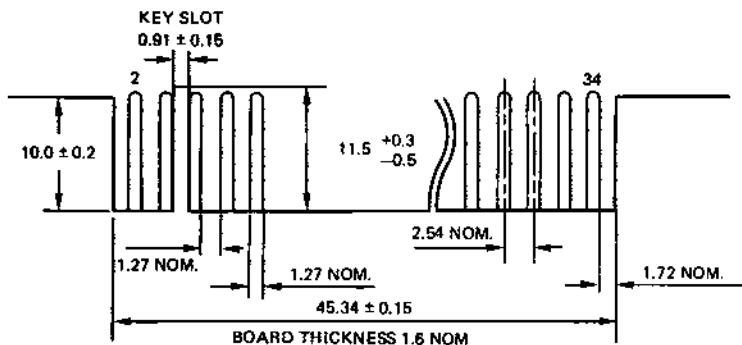


Fig. 5-1 Connector J1 Dimensions (mm) and Pin Numbers

Table 5-1 Connectors for Twisted-Pair Cable (Pl)

Parts	Crimp Type	Solder Type
	AMP P/N	AMP P/N
Housing	583717-5	583717-5
Contact	1-583616-1	583854-3
Polarity key	583274-1	583274-1
Crimping tool	90268-1	-
Extraction tool	91073-1	91073-1
Twisted-pair cable (3 m max.)	AWG 26	AWG 26

Table 5-2 Connector for Flat Cable (Pl)

Parts	3M P/N
Connector	3463-0001
Polarity key	3439-0000
Crimping tools	Press 3440
	Locator plate 3443-11
	Platen 3442-3
Flat cable (3 m max.)	3365/34

Items that can be used in conjunction with a connector for the flat cable.

Parts	HIROSE P/N
Connector	HIF5D-34DA-2.54R
Polarity key	CR7C-GPIN

(Items such as a fusing tool. For details refer to the manufacturers of the connector.)

## 5.2 DC Power Connector (J2/P2)

P2 is a four-pin DC power connector made by AMP, located on the back of the printed-circuit board. Pin 4 on connector P2 is located closest to J1/P1; the arrangement of the pins as viewed from the side is shown in Fig. 5-2.

The connectors on the drive side and cable side are shown in Table 5-3.

Table 5-3 DC Power Connectors

Parts	J2 (Cable Side)	P2 (Drive Side)
	AMP P/N	AMP P/N
Housing	1-480424-0	172349-1
Contact (4 pins)	60619-1	-
Crimp tool	90124-2	-
Extraction tool	1-305183-2	-
Cable (3 m MAX.)	AWG 18	-

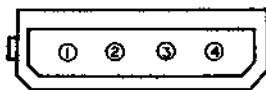


Fig. 5-2 Connector P2

## 5.3 Frame Ground Connector (J7/P7)

FASTON Terminal	Crimp Terminal
AMP P/N 60920-1	AMP P/N 60972-1

## 5.4 Interface Connector Physical Location

Fig. 5-3 shows the physical locations of the interface connectors.

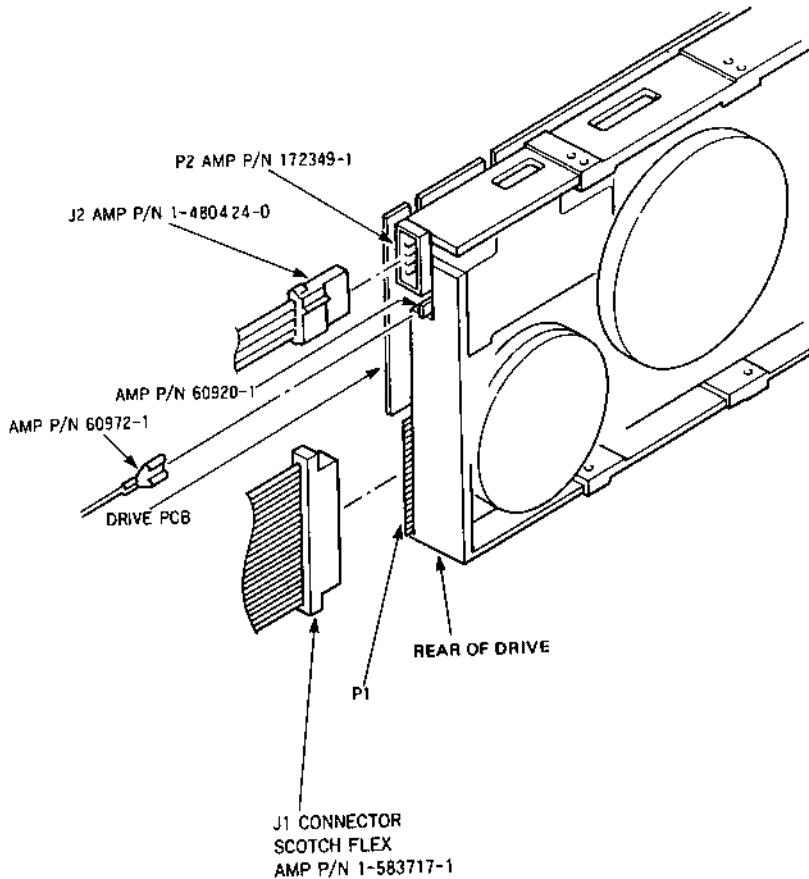


Fig. 5-3 Location of Interface Connectors

## CHAPTER 6 DRIVE PHYSICAL SPECIFICATIONS

### 6.1 Installation Direction

Install the Mini Flexible disk drive in the directions shown in Fig. 6-1.

The slant mount should be within 10 degrees.

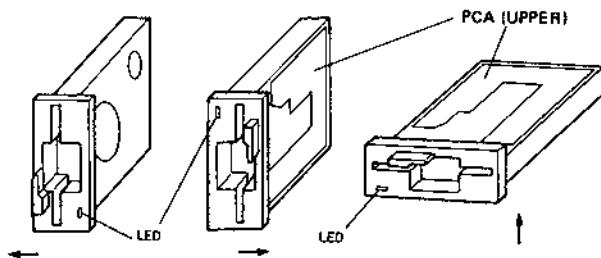


Fig. 6-1 Disk Drive Installation Directions

### 6.2 Dimensions of disk drive

See Fig. 6-2.

### 6.3 Dimensions of Front Panel

See Fig. 6-3.

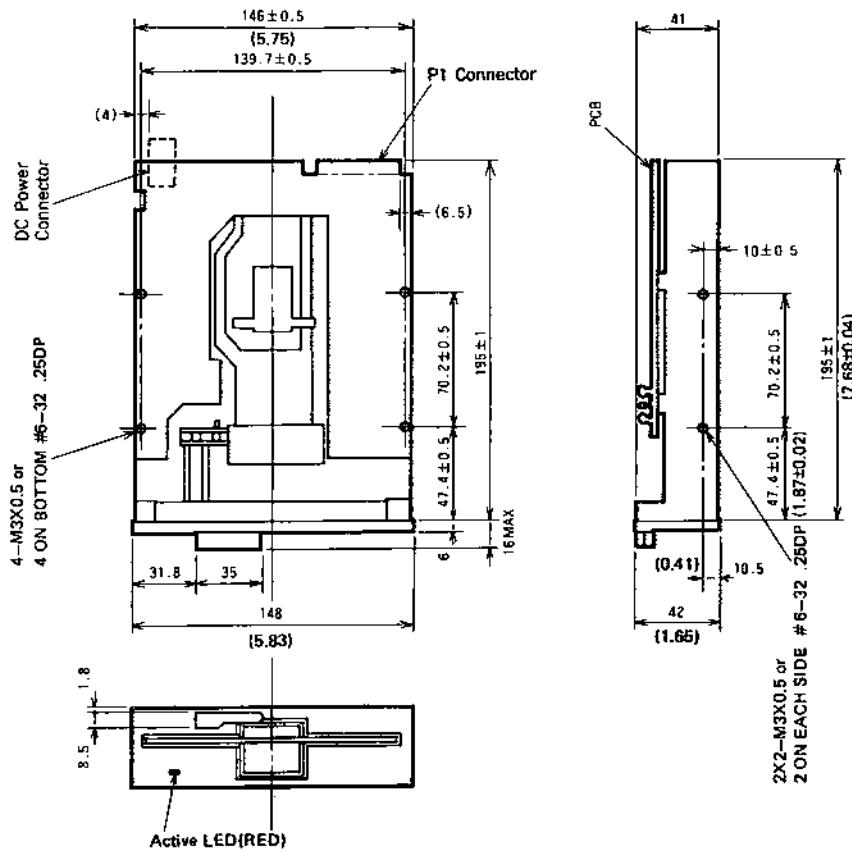
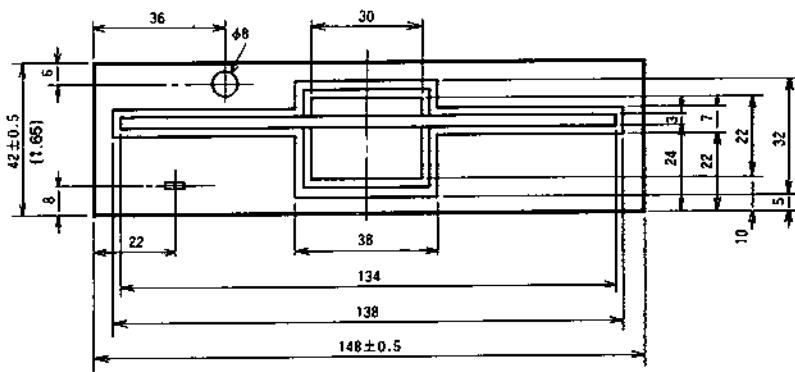


Fig. 6-3 Front Panel Dimensions

Fig. 6-2 Disk Drive Dimensions



## CHAPTER 7 ERROR DETECTION AND CORRECTION

This chapter describes the general cause analysis and corrective procedures to be followed in the event that data errors occur.

### 7.1 Write Errors

If an error occurs during a write operation, it can be detected by performing a read operation on the diskette immediately following the write operation. This is generally called a write check, which is an effective means of preventing write errors. It is recommended, therefore, that a write check be made without fail.

If a write error occurs, repeat the write operation and conduct a write check. If data cannot be correctly written even after the write operation is repeated about ten times, perform a read operation on another track to determine whether the data can be read correctly. If so, a specific track of the diskette is defective. If data cannot be correctly read on the other track, the drive is assumed to have some trouble. If the diskette is defective, replace it.

### 7.2 Read Errors

Most data errors that occur are soft errors. If a read error occurs, repeat the read operation to recover the data.

The following are possible main causes of soft errors:

- o Dust is caught between the read/write head and diskette causing a temporary fault in head contact. Such dust is generally removed by the self-cleaning wiper of the jacket, and the data is recovered by the next re-read operation. If read/write operations is continued for a long time in a very dusty environment, however, hard errors can result from a damaged diskette surface.

- o Random electrical noise ranging in time from a few microseconds to a few milliseconds can also cause read errors. Spurious noise generated by a switching regulator, particularly one that has short switching intervals, deteriorates the signal-to-noise ratio, and increases the number of re-read operations for data recovery. It is necessary, therefore, to make an adequate check on the noise levels of the DC power supplies to the drive and frame grounding.
- o Written data or diskettes may have so small a defect as cannot be detected by a data check during write operation.
- o Fingerprints or other foreign matter on a written diskette can also cause a temporary error. If foreign matter is left on a written diskette for a long time, it can adhere to the diskette, possibly causing a hard error.

It is recommended that the following read operations be performed to correct these soft errors:

- o Step 1: Repeat the read operation about ten times until the data is recovered.
- o Step 2: If the data cannot be recovered by Step 1, move the head to other track, the opposite direction of the previous track position before the designated track, and then return the head to the original position.
- o Step 3: Repeat an operation similar to Step 1.
- o Step 4: If the data cannot be recovered, take the error as a hard error.

CHAPTER 8 RESHIPMENT PRECAUTIONS

When reshipping the drive, make sure the protection sheet for transportation is in place in the drive, and open the door.



\* Additional Specifications

This item describes motor speed and data transfer rate of the M4854-1/3S Flexible Disk Drives.

Fig. 1 Implementation of motor speed selection and data transfer rate selection.

Implementation	Short plug Selection (on PCB)	SS : Short SB : Open		SS : Open SB : Short		See Note 1.
	Normal Density signal (controller output)	logical " 1 "	logical " 0 "	logical " 1 "	logical " 0 "	See Note 2.
Useable Media		High Density	Normal Density	High Density	Normal Density	
Motor Speed		360 rpm	300 rpm	360 rpm	360 rpm	
Data Transfer Rate		500 Kbits/s	250 Kbits/s	500 Kbits/s	300 Kbits/s	

Note 1. See 3.1.3 (7), page 20 in the Standard Specifications.

Note 2. See 3.1.4 (9), page 27 in the Standard Specifications.

Fig. 2. Relation to Formatted Media

Formatted Media	96 TPI High Density (1.6MB) *1	96 TPI Normal Density (1.0MB) *1	48 TPI Normal Density (0.5MB) *1
Read/Write	Read and Write possible	Read and Write possible	Read and Write possible *1
Data Transfer Rate of MFM(FM)	500(250) Kbits/s only	250(125)Kbits/s, 300(150)Kbits/s selectable	50(125)Kbits/s, 300(150)Kbits/s selectable

\*1 ( ) indicates unformatted capacity.

\*2 Only 96 TPI drive can read the revised data.

\*\*\*\*\*  
\* \*  
\* \*  
\* 1.2 Meg. Floppy Disk Drive \*  
\* \*  
\* Section 5 \*  
\* \*  
\* Parts list \*  
\* \*  
\*\*\*\*\*

November 15, 1985



Disk Drive Subassembly

Item	Quan	Description	Part No.
1	1	Floppy Disk Drive	AXX-5106
2	1	Support, Disk Drive	
3	4	Grommet	AHC-0189
4	4	Screw, Shoulder	AHD-2751
5	1	Cable, Load (Floppy Drive Only)	
6	2	Heatshrink, 1 Inch	
7	1	Resistor, 20 Ohm 25W 1%	N-0077BWC
8	2	Screw, #6-32 x 5/16 PPHD HP Thread Form W/T.S.S	AHD-2746

Ejector Assembly  
(Non-Repairable)

Item	Quan	Description	Part No.
1	1	Holder, Ejector A	
2	1	Ejector	
3	1	Shaft, Ejector	
4	1	Spring, Coil	
5	1	Switch (Micro-size)	
6	1	Screw, Pan HD., Washered	

Lever Assembly  
(Non-Repairable)

Item	Quan	Description	Part No.
1	1	Lever	
2	1	Lever Holder	

Add In Floppy Disk Drive Kit

Item	Quan	Description	Part No.
1	1	Disk Drive	AXX-5106
2	4	Grommet	AHC-0189
3	4	Screw, Thumb	8569281

Front Panel Assembly  
(Non-Repairable)

Item	Quan	Description	Part No.
1	1	Front Panel	
2	1	Indicator	

Chassis Front Assembly  
(Non-Repairable)

Item	Quan	Description	Part No.
1	1	Chassis Front	
2	2	Washer	
3	1	Ring, E	
4	1	Washer	
5	1	Washer	
6	2	Ring, E	
7	1	Holder	
8	1	Spring, W	
9	1	Holder	
10	1	Shaft A	
11	1	Link B	
12	1	Pin A	
13	1	Ring	
14	1	Shaft	
15	1	Link A	
16	1	Pin B	

Collet Assembly  
(Non-Repairable)

Item	Quan	Description	Part No.
1	1	Collet A	
2	1	Collet B	
3	1	Spring, Coil, B	
4	1	Shaft	
5	1	Bearing	
6	1	Ring, E	
7	1	Washer, Metal	

Bridge A Assembly  
(Non-Repairable)

Item	Quan	Description	Part No.
1	1	Stopper, Ejector	
2	2	Spacer A, Cartridge Guide	
3	1	Cushion Mold	
4	1	Cartridge Guide A	
5	1	Spring, Cartridge Guide	
6	2	Screw, Pan HD., Washered	

Carriage Assembly  
(Non-Repairable)

Item	Quan	Description	Part No.
1	1	Carriage	
2	1	Arm	
3	1	Sub Frame	
4	1	Stay Spring	
5	1	Head Gimbal, S0	
6	1	Head Gimbal, S1	
7	2	Shield Plate	
8	1	Spring Coil	
9	1	Head Cable Assy	
10	1	Spring, P	
11	2	Rubber	
12	1	Rubber	
13	1	Holder, Arm	
14	1	Holder, Band C	
15	2	Screw Pan HD., Washered	
16	1	Bolt, Socket (Micro-size)	
17	3	Screw Tap-Tight	
18	1	Spacer	
19	1	Cover, Head S1	
20	1	Nut	
21	1	Cover, Head S0	
22	1	Washer	

Mechanism Assembly

Item	Quan	Description	Part No.
1	1	Carriage Assy	AZ-0073
2	1	Frame	
3	1	Solenoid HLMG	AS-9098
4	1	TK00 Sensor Assy	ACS-0016
5	1	Spindle Motor Assy	AM-4025
6	1	Stepping Motor	AM-4016
7	1	Idler, Sub Assy	ART-0188
8	1	Holder, Idler C	ART-0133
9	1	Band A	ART-0134
10	1	Spring, Coil, C	ARB-6224
11	1	Holder, Band A	ART-0180
12	1	Holder, Band B	ART-0136
13	2	Guide Rod	AHC-0159
14	2	Spring Coil	ARB-6226
15	1	Terminal	
16	1	Washer Plain	AHD-8020
17	12	Screw, M3X0.5X8 Pan HD., Washered.	AHD-2888
18	1	Screw, M2.5X4 Pan HD.	AHD-2886
19	3	Screw, Flat	
20	4	Screw, M3X0.5X8 Pan HD., Washered.	AHD-2888
21	1	Screw, M3X0.5X10 Pan HD., Washered	AHD-2896
22	2	Clamp	AHC-0115
23	2	Screw, Bind	
24	2	Washer, Plain	AHD-8021
25	1	Stopper Capstan	AHC-0158
26	1	Bolt, Socket (Micro-size)	
27	1	Bridge A Assy.	ART-0181
28	1	Collet Assy	ART-0139
29	1	Spring, Leaf	ARB-5038
30	1	Ring, E	
31	3	Screw, M3X0.5X6 Pan HD., Washered	AHD-2885
32	1	Ejector Assy.	ART-0140
33	1	Front Panel Assy.	AZ-0083
34	1	Chassis Front Assy.	AZ-0075
35	1	Lever Assy.	ART-0182
36	1	PCB, NAMFM	

Tandy 3000 High Density Drive

Spindle Motor Assembly

Item	Quan	Description	Part No.
1	1	IC, M51720P Digital	MX-6360
2	1	IC, M51721L Linear	MX-6361
3	2	Pot 30K Ohm, Volume +20% 0.2W	AP-7010
4	1	Resistor, Carbon, 47K Ohm 1/6W +5%	N-0340ECC
5	1	Resistor, Carbon, 91K Ohm 1/4W +3%	N-0366DEC
6	1	Resistor, Carbon, 2.2K Ohm 1/4W +5%	N-0216EEC
7	1	Resistor, Carbon, 2.7K Ohm 1/6W +5%	N-0224ECC
8	1	Resistor, Carbon, 10K Ohm 1/6W +5%	N-0281ECC
9	1	Resistor, Carbon, 3.3K Ohm 1/6W +5%	N-0230ECC
10	1	Resistor, Carbon, 33K Ohm 1/4W +5%	N-0324EEC
11	1	Resistor, Carbon, 47K Ohm 1/6W +5%	(ABOVE)
12	1	Resistor, Carbon, 24K Ohm 1/6W +5%	N-0526ECC
13	1	Resistor, Carbon, 5.1M Ohm 1/6W +5%	N-0603ECC
14	1	Resistor, Carbon, 47K Ohm 1/6W +5%	(ABOVE)
15	5	Resistor, Carbon, 330 Ohm 1/4W +5%	N-0159EEC
16	1	Resistor, Carbon, 22K Ohm 1/6W +5%	N-0311ECC
17	1	Resistor, Metal, 1.8K Ohm 1/2W +5%	N-0210EFE
18	1	Resistor, Carbon, 470 Ohm 1/2W +5%	N-0169EFC
19	1	Resistor, Metal, 510 Ohm 1/2W +5%	N-0172BFE
20	2	Resistor, Carbon, 47 Ohm 1/4W +5%	N-0099EEC
21	1	Resistor, Metal, 0.75 Ohm 1W +5%	N-0637EGD
22	2	Capacitor, Rutiloon, 1000pF +20% 25V	(CF-1194)
23	2	Capacitor, Elec., 1uF +20% 50V	CC-F105MJNP
24	1	Capacitor, Poly, 0.056uF +5% 100V	CC-563JLGP
25	1	Capacitor, Poly, 0.047uF +5% 50V	CC-473JJGP
26	1	Capacitor, Elec., 0.15uF +20% 50V	CC-154MJGP
27	1	Capacitor, Elec., 0.47uF +20% 50V	CC-474MJNP
28	2	Capacitor, Elec., 2.2uF +20% 50V	CC-225MJAP
29	1	Capacitor, Elec., 33uF +20% 16V	CC-336MDNP
30	1	Capacitor, Elec., 0.1uF +20% 50V	CC-104MJNP
31	1	Diode, IS-1588	DX-0273
32	1	LED, GL-5AR2	AL-1005
33	1	LED, EL-1KL3	AL-1006
34	1	LED, EL-1CL3	AL-1007
35	2	Holl Element, H300A	MX-0087
36	1	Transistor, 2SA1115	2SA1115
37	1	Transistor, 2SC3402	2SC3402
38	1	Transistor, 2SA1348	2SA1348



## PCB, NAMFM

Item	Quan	Description	Part No.
1	1	PWB, NAMFM	
2	1	Terminal	
3	4	Connector, male 3 pins	AJ-1072
4	1	Connector, male 4 pins	AJ-7585
5	1	Ornament	
6	1	Connector, male 14 pins	AJ-1073
7	3	Connector, male 10 pins	AJ-1074
8	11	Connector, female 2 pins	AJ-7588
9	1	Connector, male 4 pins	AJ-1075
10	1	Connector, male 10 pins	AJ-1076
11	3	Connector, male 2 pins	AJ-7592
12	1	Connector, male 3 pins	AJ-7584
13	1	Connector, male 2 pins	AJ-1085
14	1	Connector, male 5 pins	AJ-1086
15	1	Index Sensor U Assy	ACS-0018
16	1	Write Protect Sensor	ACS-0017
17	1	Holder, Write Protect Sensor	ART-0141
18	1	Bolt, Socket (FE)	AHD-5001
19	1	Socket, IC	AJ-1057
20	2	IC, M53238P Digital (D6)	MX-6364
21	1	IC, Digital (G1)	MX-5699
22	2	IC, M54542L Linear	MX-6365
23	1	IC, MC2870P Linear	MX-6892
24	1	IC, UPA2003JC Linear	MX-6844
25	1	IC, Digital (G1) (Alternate)	
26	1	IC, Linear (G6) (Alternate)	
27	3	Capacitor, Ceramic, 0.01uF $\pm 10\%$ 50V	CC-103KJCP
28	9	Capacitor, Ceramic, 1.5uF $-20+80\%$ 25V	(CC-155ZFCP)
29	2	Capacitor, Ceramic, 0.022uF $\pm 10\%$ 50V	(CC-223KJCP)
30	2	Capacitor, Ceramic, 150pF $\pm 5\%$ 50V	CC-151JJCP
31	1	Capacitor, Ceramic, 470pF $\pm 5\%$ 50V	CC-471JJCP
32	1	Capacitor, Ceramic, 6800pF $\pm 10\%$ 50V	CC-682KJCP
33	1	Capacitor, Ceramic, 3300pF $\pm 10\%$ 50V	CC-332KJCP
34	1	Capacitor, Ceramic, 33pF $\pm 5\%$ 50V	CC-330JJCP
35	1	Capacitor, Ceramic, 1500pF $\pm 10\%$ 50V	CC-152KJCP
36	1	Capacitor, Ceramic, 680pF $\pm 10\%$ 50V	CC-681KJCP
37	1	Capacitor, Ceramic, 330pF $\pm 10\%$ 50V	WRONG # ?
38	1	Capacitor, Elec., 100uF $\pm 20\%$ 16V	CC-107MDAP
39	1	Capacitor, Ceramic, 0.22uF $\pm 10\%$ 50V	(CC-224KJCP)

## PCB, NAMFM (con't)

Item	Quan	Description	Part No.
40	1	Resistor, Carbon, 10K Ohm $\pm 5\%$ 1/6W	(N-0281ECC)
41	1	Resistor, Carbon, 3.3K Ohm $\pm 5\%$ 1/6W	(N-0230ECC)
42	4	Resistor, Carbon, 4.7K Ohm $\pm 5\%$ 1/6W	N-0247ECC
43	1	Resistor, Carbon, 1M Ohm $\pm 5\%$ 1/6W	N-0445ECC
44	2	Resistor, Metal, 470 Ohm $\pm 2\%$ 1/4W	N-0169CED
45	1	Resistor, Metal, 47K Ohm $\pm 2\%$ 1/4W	N-0340CEE
46	2	Resistor, Carbon, 47 Ohm $\pm 5\%$ 1/6W	N-0099ECC
47	2	Resistor, Carbon, 1.8K Ohm $\pm 5\%$ 1/6W	N-0210ECC
48	1	Resistor, Metal, 150 Ohm $\pm 1\%$ 1/4W	N-0142BED
49	1	Resistor, Carbon, 100K Ohm $\pm 5\%$ 1/6W	N-0371ECC
50	2	Resistor, Carbon, 27K Ohm $\pm 5\%$ 1/6W	N-0316ECC
51	1	Resistor, Carbon, 470K Ohm $\pm 5\%$ 1/6W	N-0423ECC
52	1	Resistor, Carbon, 39 Ohm $\pm 5\%$ 1/6W	N-0092ECC
53	1	Resistor, Carbon, 6.8K Ohm $\pm 5\%$ 1/6W	N-0262ECC
54	1	Resistor, Carbon, 22K Ohm $\pm 5\%$ 1/6W	(N-0311ECC)
55	2	Resistor, Carbon, 12K Ohm $\pm 5\%$ 1/6W	N-0288ECC
56	1	Resistor, Carbon, 270 Ohm $\pm 5\%$ 1/2W	N-0155EFC
57	1	Resistor, Carbon, 8.2K Ohm $\pm 5\%$ 1/6W	N-0271ECC
58	1	Resistor, Metal, 27K Ohm $\pm 2\%$ 1/4W	N-0316CED
59	3	Resistor, Carbon, 1.5K Ohm $\pm 5\%$ 1/6W	N-0206ECC
60	3	Resistor, Carbon, 2.7K Ohm $\pm 5\%$ 1/6W	(N-0244ECC)
61	1	Resistor, Metal, 10K Ohm $\pm 2\%$ 1/4W	N-0281CED
62	2	Resistor, Carbon, 82K Ohm $\pm 5\%$ 1/6W	N-0360ECC
63	1	Pot 50K Ohm Volume	AP-7389
64	2	Resistor, Carbon, 47K Ohm $\pm 5\%$ 1/6W	(N-0340ECC)
65	2	Resistor, Carbon, 560 Ohm $\pm 5\%$ 1/2W	N-0176EFC
66	1	Resistor, Metal, 1.5K Ohm $\pm 1\%$ 1/4W	N-0206BED
67	1	Resistor, Carbon, 150 Ohm $\pm 5\%$ 1/6W	M-0142ECC
68	1	Resistor, Carbon, 56 Ohm $\pm 5\%$ 1/2W	N-0107EFC
69	1	Resistor, Metal, 150 Ohm $\times 8 \pm 5\%$ 125mw	ARX-0040
70	4	Resistor, Metal, 4.7K Ohm $\times 6 \pm 5\%$ 125mw	ARX-0041
71	1	Resistor, Carbon, 1.2K Ohm $\pm 5\%$ 1/6W	N-0199ECC
72	2	Diode, 1S-953	DX-0762
73	2	Diode, LSR35-100A-T	DX-0583
74	1	Ceramic, 400 KHZ	ACA-9001
75	2	Inductor, 330uH $\pm 5\%$	ACA-1018
76	1	Inductor, 100uH $\pm 10\%$	ACA-1017
77	2	Transistor	2SA-952
78	1	Transistor	2SK-68A
79	5	Transistor, DTC-114	MX-5700
80	3	Transistor	2SC-2603

\*\*\*\*\*  
\* \*  
\* 1.2 Meg. Floppy Disk Drive \*  
\* \*  
\* Section 6 \*  
\* \*  
\* Jumper Settings \*  
\*  
\*\*\*\*\*



**1.2 Meg Disk Drive Servo/Logic Board  
Jumper Settings**

If the drive is a Mitsubishi Model MF504A-3 be sure that DC, MM, DSl, RR, SB and TD on the drive servo/logic board are jumpered.



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\*       1.2 Meg. Floppy Disk Drive       \*  
\*    \*  
\*    \*  
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\*       Schematics and Component Layout   \*  
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\*\*\*\*\*  
\* 1.2 Meg. Floppy Disk Drive  
\* Section 8  
\* Maintenance Manual  
\*\*\*\*\*



**5.25 INCH FLEXIBLE DISK DRIVE  
MAINTENANCE MANUAL  
MF504A-3**

 MITSUBISHI ELECTRIC CORPORATION

## INDEX

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## **1. Introduction**

This manual deals with the handling, maintenance, and adjustment of the MF504A-3 flexible disk unit.

## **2. Related diagrams and references**

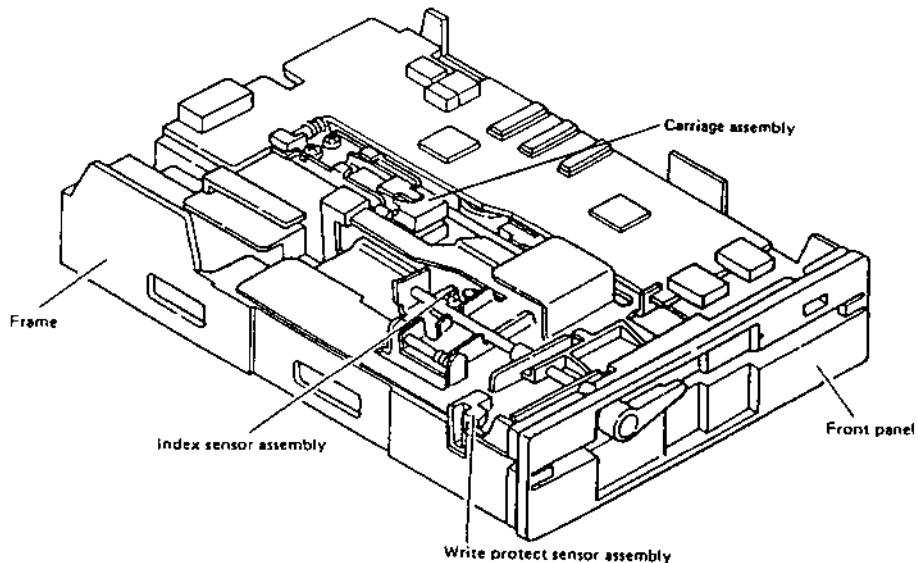
Standard specifications of MF-504A-3

Electrical diagram for maintenance of MF504A-3

Illustrated parts list

Packing instructions

## **3. Names of parts**



#### 4. Handling

##### 4.1 Operating environment

No problems are likely occur when this unit is used under normal conditions. However damage to the unit or to disk is liable to occur if the unit is used under normal conditions outside the following:

- |                               |   |   |
|-------------------------------|---|---|
| (1) Temperature and Humidity: | When in use<br>Temperature range:<br>Humidity range:  | When not in use<br>-10°C ~ 50°C<br>20% ~ 80% RH (non-condensating)<br>(Max. wet bulb 29.4%) |
| (2) Vibration and Shock       | When in use:<br>When not in use:  | less than 0.3 G (10 ~ 100 Hz)<br>Continuous vibration less than 2 G (10 ~ 100 Hz)           |
| (3) Dust                      | Special caution should be taken regarding dust as it damages the magnetic head and recording surface of the disk. |   |
| (4) Temperature drop          | Less than 20°C/Hour (when unpacked)   |   |

##### 4.2 Handling of disk cartridge (special caution should be taken regarding the following, see Diagram 1)

- (1) Do not place the unit near any device produces a magnetic field.  
(For example, radios, TVs, motors, generators etc.)
- (2) Do not bring any magnetized objects near the cartridge.  
(For example, rubber magnets, magnets for blackboards, screwdrivers etc.)
- (3) Do not bend the disk.
- (4) Place the disk cartridge into its paper case when it is transported or stored.
- (5) Do not touch the disk cartridge itself. Do not try to clean it with alcohol or similar liquids.
- (6) Do not place it in direct sunlight or in places which have high temperature or high dust levels.
- (7) Do not write anywhere but on the label. Use only a felttipped marker or similar pen.

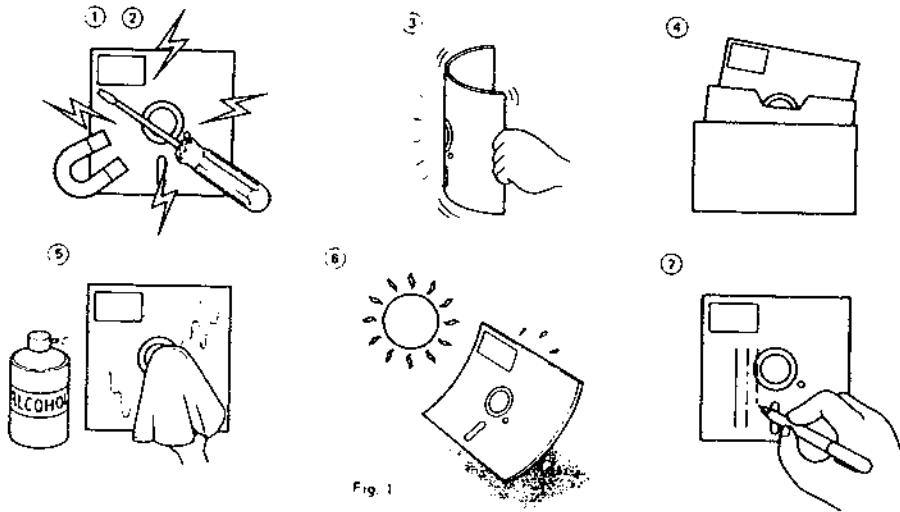


Fig. 1

## **5. Periodical maintenance**

Periodical inspection, maintenance, cleaning, and replacement of worn-out parts is recommended to maintain the correct operation of this unit and to spot trouble quickly. The time between periodical maintenance is calculated based on a 8 hour/day schedule. Thus, it may have to be adjusted if actual use is different. Based on usage of 8 hours/day under normal conditions, periodical maintenance should be once a year.

### **5.1 Precautions regarding maintenance**

#### **5.1.1 Precaution**

- (1) Be sure that dust does not get inside the unit and that the head is not damaged.
- (2) Be sure that the power is off before beginning maintenance.
- (3) The DC power must be off when the connector is inserted or removed from the PC board. This is to prevent damage to the semiconductors.
- (4) Do not touch the surface of the disk or the magnetic head.
- (5) When this unit is used for playback (when CE disks etc. are being used), be careful of operations such as write protection for the protection of recorded data.
- (6) Do not touch or attempt to adjust the steel band.
- (7) Do not force or subject the head carriage assembly to shock of any sort as it was precision adjusted. Do not use screws or nuts other than those specified and do not attempt to re-adjust the assembly.

#### **5.1.2 Disks which can be used**

- (1) CE diskettes: 502-1D standard diskette made by DYMEK
- (2) Cleaning diskette: CFD-5W made by Nihon Micro Coating

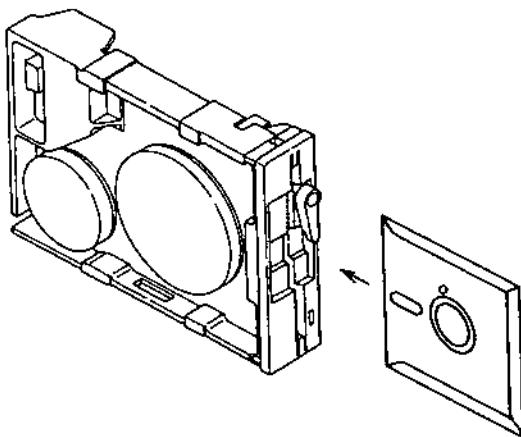
## 5.2 Head Cleaning

Clean the head as dirt on the head can lead to read errors and damage to the disk. The head is cleaned by the following procedure:

### 1) Equipment

CE tester

Cleaning diskette



### 2) Cleaning method

- 2) -1 Connect the CE tester to the unit and turn the power on.
- 2 Insert the cleaning diskette and start head loading.
- 3 Remove the cleaning diskette after about 1 minute of cleaning.

### 3) Precautions

- 3) -1 Match the head to the track of the disk to improve cleaning efficiency.
- 2 Clean the unit for about 1 minute.
- 3 The cleaning diskette is good for 1 hour per track. Replace it after the expiration of this period.
- 4 Do not clean the unit more than once at a single time or more than twice a month.  
This will prevent the head from being deformed.

### 5.3 Testing and adjustment

#### 5.3.1 Adjustment of position of TK00 sensor

##### 1) Equipment

CE tester

Blank diskette

Allen wrench (2.5 mm)

Oscilloscope

##### 2) Adjustment

2) -1 Connect the CE tester to the unit, turn the power on and insert the diskette into the unit.

-2 Turn the motor on and start drive select operations.

-3 Perform repeat seeking on tracks 00 ~ 02. (step rate 3 ms)

-4 Monitor the TPC13 waveform (TK00) with the oscilloscope.

Trigger CH1—STEP (DC,-) (TPC15)

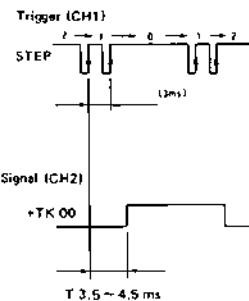
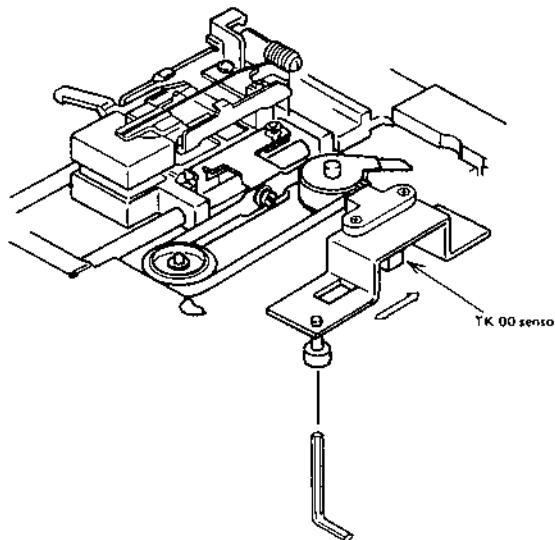
Signal CH2—TK00 (DC ) (TPC13)

-5 Turn the installation screw until the time of T is 3.5 ~ 4.5 ms. This will move the TK00 sensor in the direction of the arrows for adjustment.

-6 Confirm that there are two STEP signals.

##### 3) Checking

Check that seeking starts from track 00 and stops on track 02. Be sure the voltage of of TPD1 is 0 ~ 0.6V when the unit is stopped on track 02.



### 5.3.2 Testing of position of index sensor

#### 1) Equipment

CE tester

CE diskette

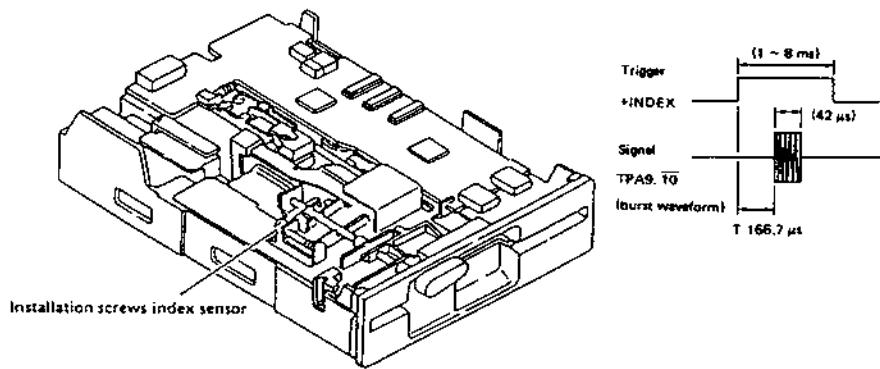
No. 2 + screw driver

Oscilloscope

#### 2) Testing

- 2) -1 Connect the CE tester to the unit, turn the power on and insert the diskette into the unit.
- 2 Turn the motor on and start drive select operations.
- 3 Set the unit to the read mode and monitor the TPA9 and TPA10 waveforms of track 02 with the oscilloscope.

Trigger	EXT → INDEX (DC,+)	(TPB14)
Signal	CH1—output waveform (AC )	(TPA9)
		ADD
	CH2—output waveform (AC,INV)	(TPA10)
Standard	Side 0	Side 1
Testing	166.7 ± 100μs	166.7 ± 150μs
Adjustment	166.7 ± 50μs	166.7 ± 100μs



### 5.3.3 Adjustment of head alignment

- 1) Equipment
  - CE tester
  - CE diskette
  - Oscilloscope
  - Allen wrench (2mm)
- 2) Adjustment
  - 1 Connect the CE tester to the unit, turn the power on and insert the diskette into the unit.
  - 2 Turn the motor on and start drive select operations.
  - 3 Set the unit to the read mode and monitor the TPA9 and TPA10 waveforms, while the unit goes from track 00 to track 32, with the oscilloscope.

Trigger	EXT—+INDEX (DC,+)	(TPB14)
Signal	CH1—output waveform (AC ) CH2—output waveform (AC, INV)	ADD (TPB9) (TPA10)

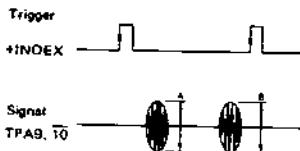
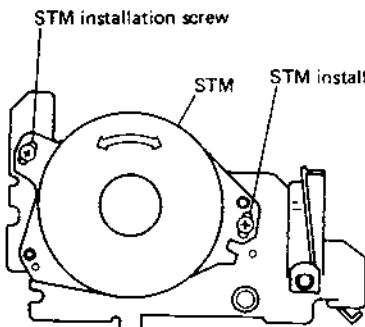
Standard	Testing	Adjustment
When A>B B/A	0.57,	0.60
When A<B A/B	0.57,	0.60

- 4 Adjust the carriage installation screws to obtain the above standards while the unit goes from track 00 to 32 or from track 9 to 32. This will move the carriage in the direction of the arrows for adjustment. (tighten the screws after adjustment)
- 5 Adjust both head 0 and head 1 until both are within the above specifications.

#### 3) Precautions

Perform adjustment until the following conditions:

Temperature  $23 \pm 2^\circ\text{C}$   
Humidity  $50 \pm 5\%\text{RH}$  } after waiting 2 hours



### 5.3.4 Testing of head azimuth

#### 1) Equipment

CE tester

CE diskette

Oscilloscope

#### 2) Testing

2) -1 Connect the CE tester to the unit and turn the power on.

-2 Insert the diskette, turn the motor on, and start drive select operations.

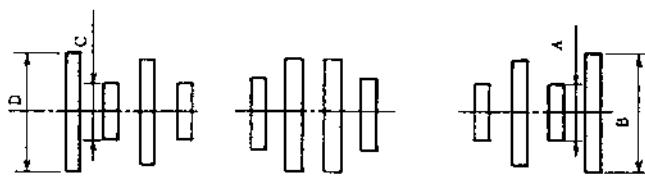
-3 Set the unit to the read mode, perform seek operations for track 68, and monitor the TPA9 and TPA10 waveforms with the oscilloscope.

Trigger EXT → INDEX (DC, +) (TPB14)

Signal CH1—output waveform (AC, ) ADD (TPA9)

CH2—output waveform (AC, INV) (TPA10)

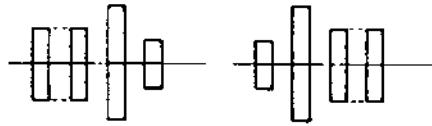
-4 The unit is operating correctly if the waveforms are within the following ranges.



$$115 > \frac{D}{C} \times 100 \quad (0^\circ \pm 0^\circ) \quad \text{Proper range}$$

$$\frac{B}{A} \times 100 < 115 \quad (0^\circ + 18^\circ)$$

Reference



\*\*\*\*\*  
\* 1.2 Meg. Floppy Disk Drive \*  
\* Section 9 \*  
\* Technical Manual \*  
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**5.25 INCH FLEXIBLE DISK DRIVE  
TECHNICAL MANUAL  
MF504A-3**

 MITSUBISHI ELECTRIC CORPORATION



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## CHAPTER 1 OUT LINE

1. This section deals with the mechanical parts and control circuits of the MF504A-3 flexible disk drive. MF504A-3 flexible disk unit with high density medium allows for more than 1MB formatted memory capacity. It is format compatible with a 8 inch flexible disk allowing the reading and writing of previously used normal density disks. However, normal density 48TPI medium can only be read. The rotational speed can be switched by an external signal for 360/300rpm for high and normal density respectively. The READ/WRITE circuitry is also automatically switched at the same time.

In addition, it is also possible to set the unit for normal density so that the rotational speed remains at 360rpm and only the READ/WRITE circuit is switched.

### 1.1 Composition of mechanism by Function

The mechanism can be divided by function as follows:

- (1) Lever mechanism and door SW mechanism
- (2) Disk rotation and clamp mechanism
- (3) Magnetic head positioning mechanism
- (4) Magnetic head/carriage mechanism
- (5) Sensors (index, write protect, track 00)

### 1.2 Composition of Electronic Circuitry by Function

The electronic circuits are installed on two printed-circuit boards and can be classified by function as follows: The spindle motor drive circuit constitutes an independent printed-circuit board which is built integrally with the motor.

- (1) Signal interface circuit and drive select circuit
- (2) Power-on reset circuit
- (3) Panel indicator drive circuit
- (4) Index pulse generator circuit and ready circuit
- (5) Step motor drive circuit
- (6) Track 00 detection circuit
- (7) Side select circuit
- (8) Write/erase circuit
- (9) Write-protect circuit
- (10) Read circuit
- (11) Spindle motor drive circuit



## CHAPTER 2 DESCRIPTION OF MECHANISM OPERATION

Figure 2-1 shows an exploded view of the mechanism.

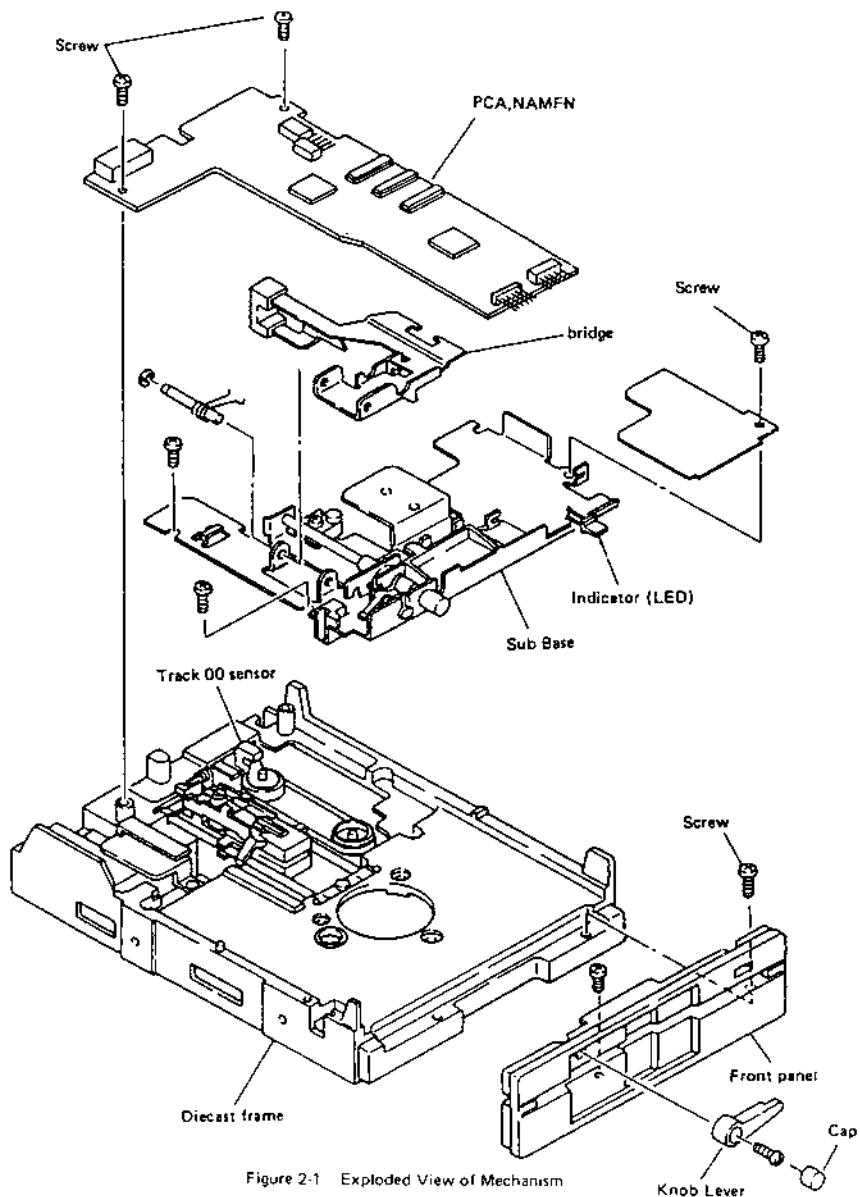


Figure 2-1 Exploded View of Mechanism

## 2.1 Disk Rotation Drive and Clamp Mechanism

The disk rotation drive motor is a flat DC servo motor. This motor has as long a life as an ordinary AC motor because it is a brushless type that uses a Hall element for coil phase-switching detection.

The motor does not use a belt, unlike conventional counterparts, but is a direct-drive type with the rotor and spindle directly connected to each other. This is another feature for prolonging motor life and assuring that the rotation mechanism is completely free of maintenance. The rotational speed of the spindle motor is 360rpm and 300rpm and this can be switched by the PCA. NAMFM signals from the main control circuit.

The frequency-generator coil detects the spindle motor speed and forms a servo circuit to control it.

The disk is clamped by the spindle cone on the motor side and by the collet on the door. The collet guides the disk to a position on the inner surface of the spindle cone. This assures compatibility between diskettes and the disk drives.

The collet is tapered to a specific angle to correct non-alignment of an inserted disk with the spindle cone.

Figure 2-2 shows the spindle motor and collet.

The printed-circuit board for the spindle motor servo circuit has an index sensor LED (light-emitting diode) for disk rotation detection, write protect sensor LED for write protect detection and indicator LED for driving signal. And a photo transistor for receiving its light is installed on another printed-circuit board (NAMFM).

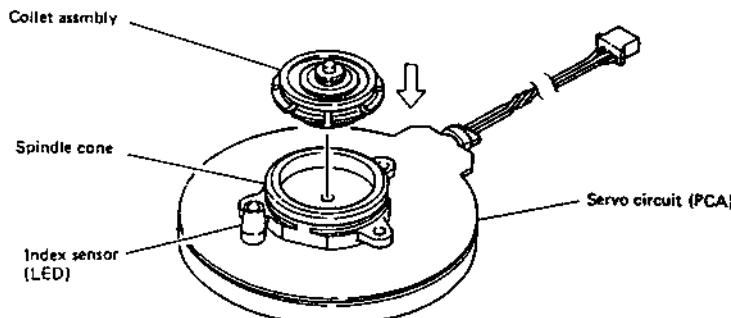


Figure 2-2 Spindle Motor and Collet

## 2.2 Magnetic Head-Positioning Drive Mechanism

The flat step motor drives the magnetic head to each track (cylinder) in succession. The capstan mounted on the step motor shaft has a thin-loop steel band, which is pulled by the spring attached to the idler pulley located opposite the steel band to maintain a specific tension. The head/carriage assembly, supported by two guide rods, is fastened to the steel band so that a turn of the step motor by one step angle moves the head by a single track distance.

Figure 2-3 shows the positioning drive mechanism.

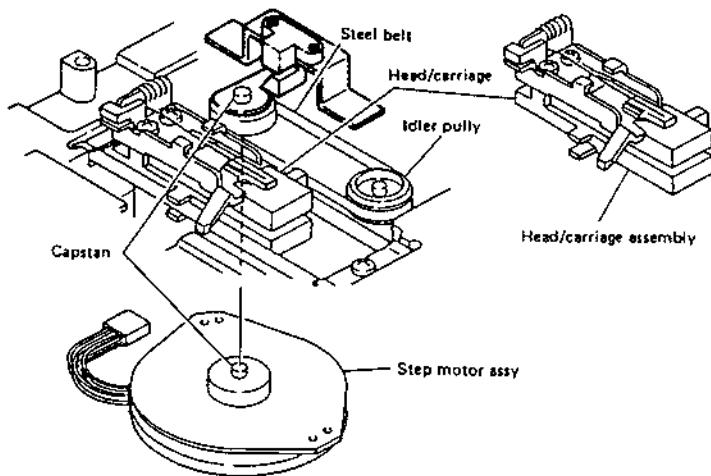


Figure 2-3 Magnetic-Head Positioning Mechanism

### 2.3 Magnetic Head/Carriage Mechanism

The magnetic head/carriage assembly consists of two magnetic head sliders that are supported by a circular gimbal spring and a plastic-molded carriage. The side 0 head is mounted in the carriage main frame, and the side 1 head is mounted on the movable arm for head loading and unloading. The movable arm is pushed by a coil spring to apply constant pressure during head loading. An external view of the carriage assembly is shown in figure 2-4, and the gimbal spring/head assembly is shown in figure 2-5.

The magnetic head is composed of three ferrite core chips and a ceramic support slider. The center core is for reading and writing, and the two cores on both sides of it are erase head cores.

Figure 2-5 shows an external view of the head slider.

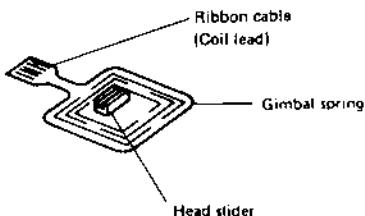


Figure 2-4 Gimbal Spring/Head Assembly

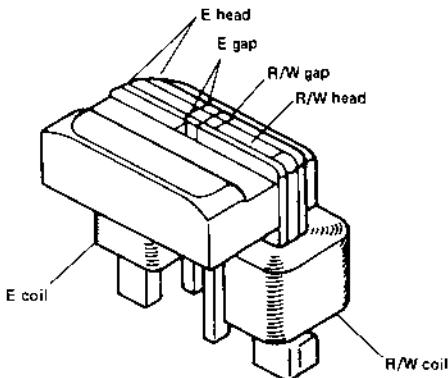


Figure 2-5 External View of Head Slider

## 2.4 Sensors (Index, Write Protect, Track 00)

### (1) Index sensor

The index sensor detects disk rotation. This sensor consists of an LED on the light-emitting side and a photo transistor on the light-receiving side. The LED is mounted on the servo circuit PCA for the spindle motor (Figure 2-2), and the photo transistor is mounted on the main control circuit PCA (NAMFM). Index sensor timing (position) can be adjusted by loosening the screws on the index sensor and removing index sensor.

Figure 2-6 shows where the photo-transistor for the index sensor is mounted.

### (2) Write-protect sensor

The write-protect sensor detects the diskette's write-protect notch and inhibits write operation.

This sensor protects information stored on read-only disks from destruction by operation errors.

Disk with the diskette's notch covered with tape or a seal that does not transmit light are protected by this sensor. Remember that vinyl or cellophane tape that has a high percentage of light transmission will not protect the disk. The write-protect sensor is mounted on sub-base ash shown in Figure 2-6. [Attached to the sub-base, this will transmit signals to PCA.]

### (3) Track 00 sensor

The track 00 sensor detects that the head is on track 00.

The track 00 sensor detects the position of the light-shielding plate that projects from the head/carriage assembly. The sensor is screwed to the STM holder and can be adjusted in position by loosening the screw.

The track 00 sensor and head/carriage assembly are shown in Figure 2-7.

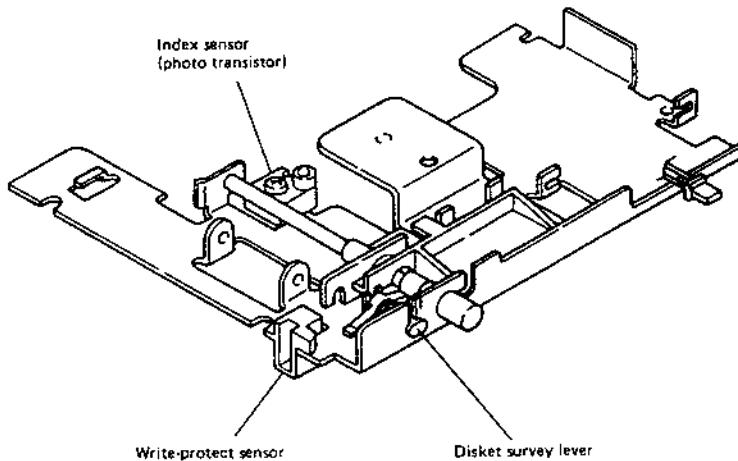


Figure 2-6 Index Sensor and Write-protect sensor

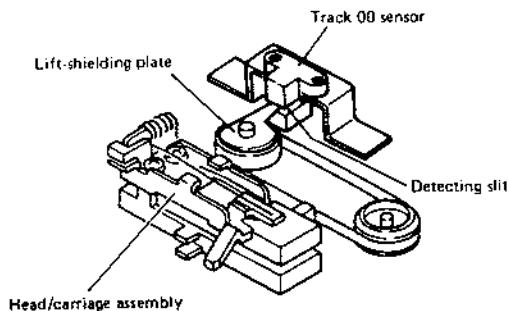


Figure 2-7 Track 00 Sensor and Head/Carriage Assembly

## CHAPTER 3 DESCRIPTION OF ELECTRONIC CIRCUIT OPERATION

Figure 3-1 shows the electronic circuits and signal connections among these circuits. The spindle motor drive circuit within the dotted lines constitutes the separate printed-circuit board that is built integrally with the motor. The parts within the chain lines belong to the mechanism described in the previous pages.

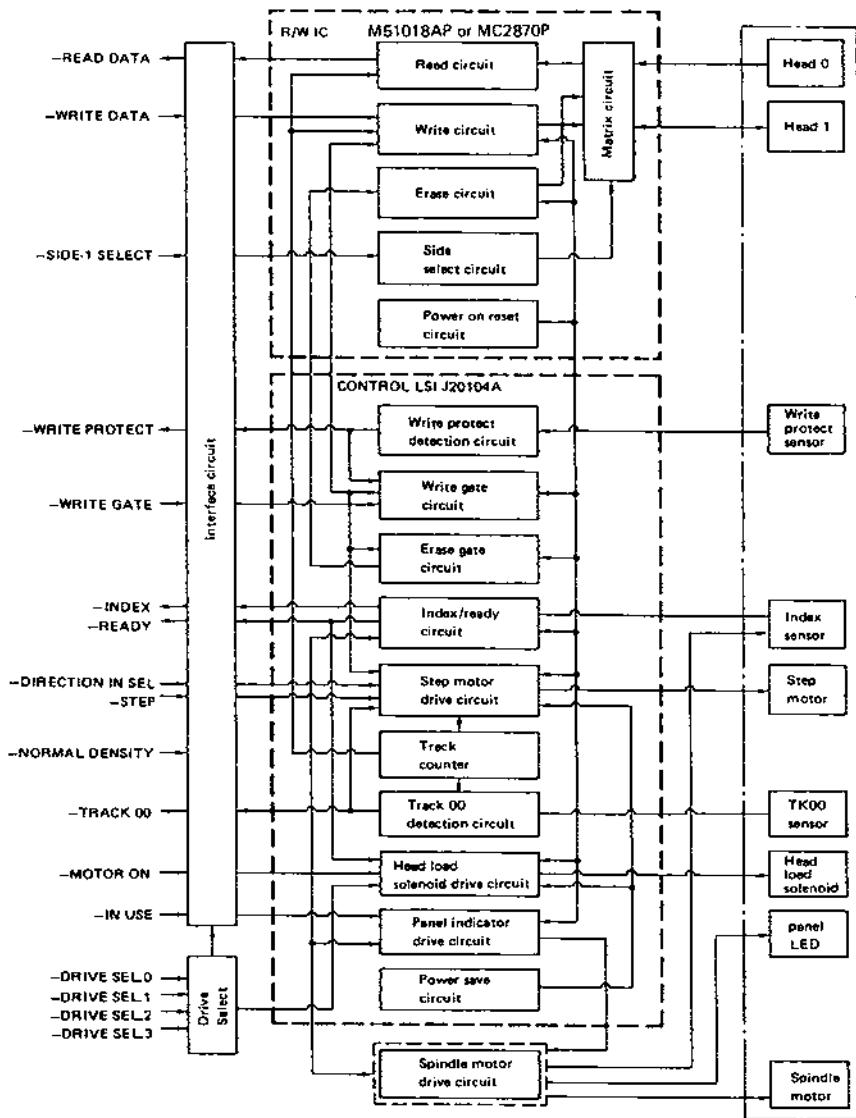


Figure 3-1 MF504A-3 Electronic Circuit

### 3-1 Interface and Drive Select Circuits

#### (1) Receive circuit

All the input terminals of the receiver that receives signals from the host controller are terminated at 150 ohms, pulling them up to +5 V. The host controller, therefore, must use driver elements with a drive capacity of 40 mA or more. Normally, an SN7438N or an equivalent open-collector drive is recommended. In connecting two or more disk drives (up to four) by a daisy-chain pattern, it is necessary to keep the cable end terminating resistor and remove the terminating resistors of the other disk drives.

#### (2) Transmit circuit

The disk drive line driver is an SN7438N or equivalent open-collector gate. It is necessary for the host controller to use a terminating resistor of 150 ohms or more.

All input signals to the line driver are gated by drive select signals. Thus, if two or more disk drives are connected in the daisy-chain pattern, the signals of only one selected disk drive are transmitted to the host controller.

#### (3) Drive select circuit

The drive select circuit selects one of the disk drives (four maximum) connected with the same cables through four interface lines (DS0 through DS3).

The four select lines correspond to the jumper plugs on the printedcircuit boards, one of which should be inserted to select the desired line. Never insert plugs into the same-numbered jacks on two or more disk drives that are connected with the same cable; interference between the output signals from such disk drives will cause errors.

The drive select signals also light the panel indicator LED.

In the case of a system requiring no drive selection, insert the jumper plug for the drive select line into the MX to maintain a selected condition.

### 3.2 Power-On Reset and Power Save Circuits

#### (1) Power-on reset circuit

The power-on reset circuit, a level-detection type reset circuit, initializes the control LSI, and that's used for preventing operation errors of the write circuit in switching power on, off.

#### (2) Power save circuit

The power save circuit controls current flowing to the step motor and head load solenoid according to their operating condition to reduce heat generation by unnecessary power consumption and thus to reduce temperature rise of the disk drive.

The step motor and head load solenoid share the same timer (mono-stable multivibrator), which has a range of 30 ms.

Timing chart of the power save circuit is shown in figure 3-2.

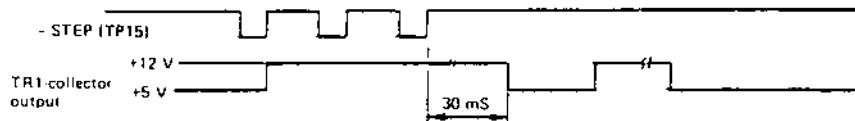


Figure 3-2 Power Save Circuit Timing Chart

### 3.3 Panel Indicator Circuit

The panel indicator is turned on by a drive select signal or by a drive select signal and in-use signal. When no in-use signal is applied to the interface, the panel indicator is turned on by a drive select signal only. If the jumper plug for the drive select circuit is inserted into the MX, the panel indicator is turned on by an in-use signal only.

Regarding jumper plug combination and indicator conditions, refer to the detailed description in the Standard Specifications MF504A-3.

### 3.4 Index Sensor and Ready Circuits

The index sensor circuit detects the index holes in the disk with a sensor, and converts its signals into logic signals.

The ready circuit checks the index pulse intervals with a timer, and becomes ready when the intervals are less than 300 ms and the next index pulse is generated.

When the door opens and the disk stops rotating and the motor-on signal turns off and the disk stops rotating the ready signal is reset.

Figure 3.3 shows a timing chart.

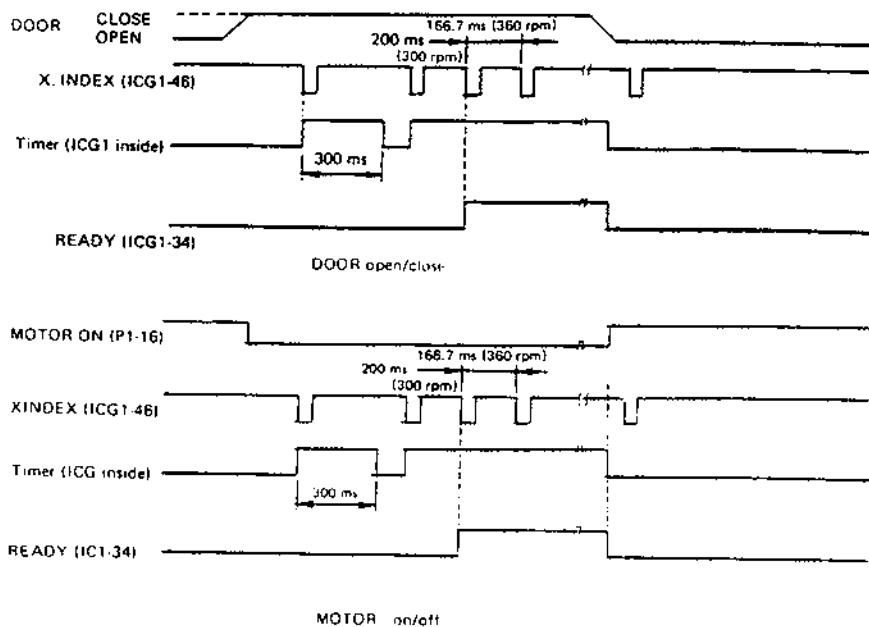


Figure 3.3 Index Sensor and Ready Circuit Timing Chart

### 3.5 Step Motor Drive Circuit

The step motor is a two-phase bipolar type and is driven to a step angle of  $1.8^\circ$  by feeding four mode currents, using two source/sink type drivers.

These four modes are generated by an up-down four-court counter that uses two flip-flops.

The step motor drive circuit switches the voltage supplied to the motor drive circuit to reduce power consumption during times other than seeking, when the motor is still.

In a seek operation, +12 V is supplied to the drive circuit, but if the next step pulse is not applied to the interface for 30 ms or more, +5 V is supplied.

Figure 3-4 shows a timing chart.

The step motor drive circuit blocks the step pulses with a write gate (except for the erase delay time) to prevent seeking during write operation. When the track 00 sensor output turns on, the circuit also blocks the step pulses to prevent further outward seek.

### 3.6 Track 00 Detection Circuit

The track 00 detection circuit detects the position of the light-shielding plate that projects from the head/carriage assembly, using a sensor. This output is ANDed with the step motor drive phase (TK00) to generate a track 00 signal. The circuit will not output a signal, therefore, unless the drive phase is at track 00 even if the sensor output is on.

For a timing chart, refer to figures 3-4.

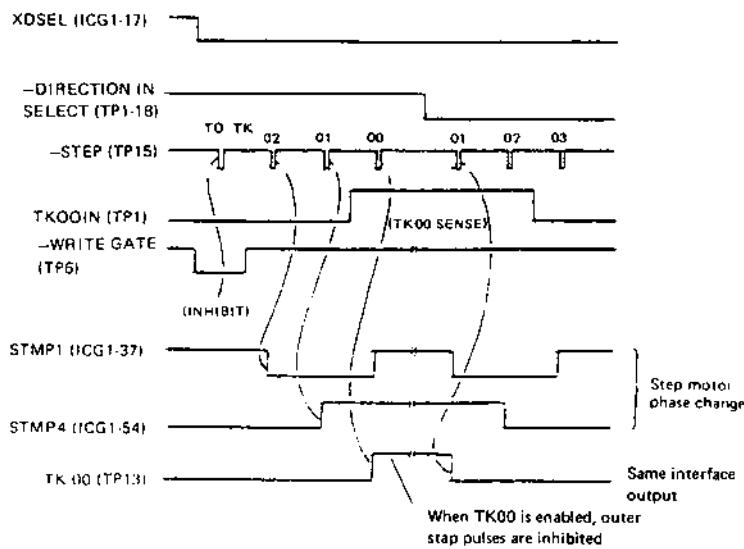


Figure 3-4 Step Motor Drive Circuit Timing Chart

### 3.7 Side Select Circuit

Side selection is made by switching the head center tap from about 0 V at off to about 11 V at on. This operation alternately feeds a write current from center tap CT-0 (CT-1) to HDA (H1A) and HOB (H1B), and an erase current from center tap CT-0 (CT-1) to ER-0 (ER-1) during write operation. In read operation a bias current is fed from CT-0 (CT-1) to HO'A (H1A) and HOB (H1B) to induce a voltage between HDA (H1B) and HOB (H1B).

The host system selects side 1 through the interface line if — SIDE ONE SELECT is low, or side 0 through the same interface line if it is high.

Figure 3-5 shows a block diagram of the side select circuit.

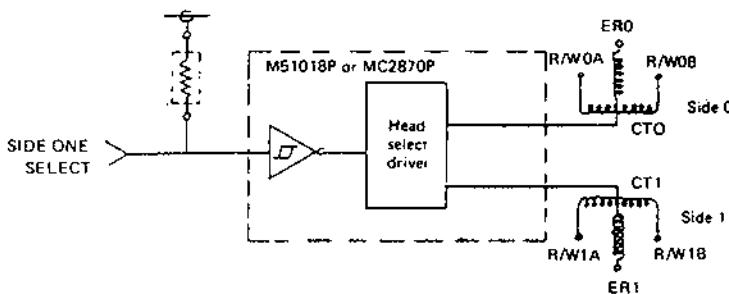


Figure 3-5 Side Select Circuit Block Diagram

### 3.8 Write/Erase Circuits

The write circuit is used for recording data on the disk. It starts writing when the write gate is opened for the selected head. If diskette write-protect status is detected, no write operation is performed.

The erase circuit erases the previous data written on both sides of the data by DC erasure. This function prevents old data from remaining on either side of newly written data due to a slight deviation of head position, and thus prevents old data crosstalk in reading the new data.

The write circuit consists of the following blocks:

- Write toggle flip-flop
- Write driver
- R/W matrix
- Write current source

When a write gate is input, the write toggle flip-flop, write driver and write current source are enabled to start a write operation. Write data is counted down to one half by the write toggle flip-flop, and a differential signal that changes synchronously with the write data is generated.

This differential signal switch the write driver.

The write driver is a switching circuit that feeds a current to the R/W head. This current is generated by the write current source and is sent to the write driver.

The R/W matrix feeds a current to the head selected by SIDE ONE SELECT as the write circuit gate is opened by a write gate.

Figure 3-6 shows the erase function and figure 3-7, a write circuit block diagram.

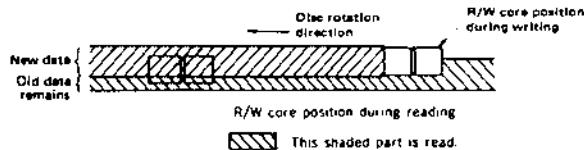
Current is alternately fed to the R/W head through two current routes, CT → R/WA and CT → R/WB as shown in the figure, according to the differential signal to invert its magnetization.

Erase operation starts with point E before write start point C and ends at point F after write end point D. The circumferential position deviation of the R/W core from the erase core is about 0.6 mm, and the erase core reaches a point that the R/W core gap has passed approx. 350 $\mu$ s at 360rpm (approx. 500 $\mu$ s at 300rpm) later (near TK.32). Therefore, the delay operation shown in figure 3-9 is required for the time from the opening of the write gate to the turning on of the erase driver and from the closing of the write gate to the turning off of the erase driver. It is for this purpose that the erase delay timer is provided to control the erase driver. Thus, for approx. 590 $\mu$ s at 360rpm (approx. 1000 $\mu$ s at 300rpm) after the closing of the write gate, the head must remain on the track and be kept selected.

The erase function erases data from the disk by always magnetizing it in one direction.

Figure 3-8 shows a conceptual diagram of write operation and figure 3-9, an erase delay operation timing chart.

(Without erase head)



(With erase head)

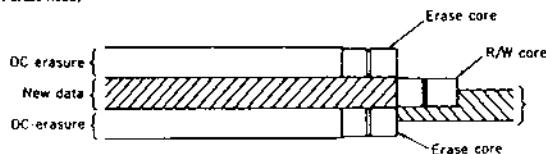


Figure 3-6 Erase Function

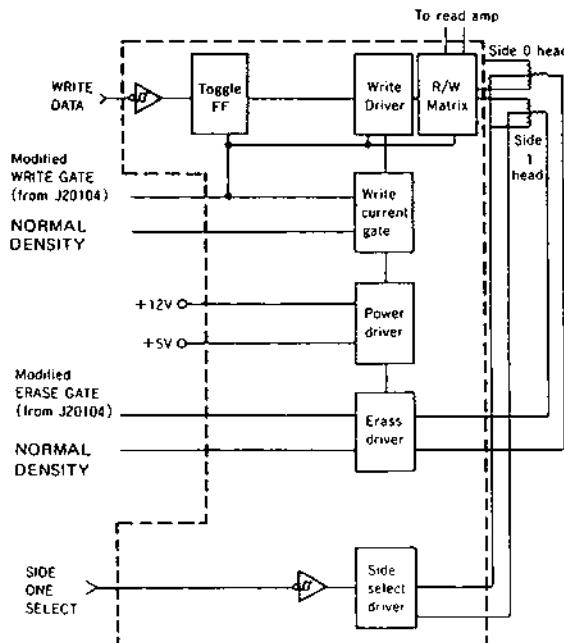


Figure 3-7 Write Circuit Block Diagram

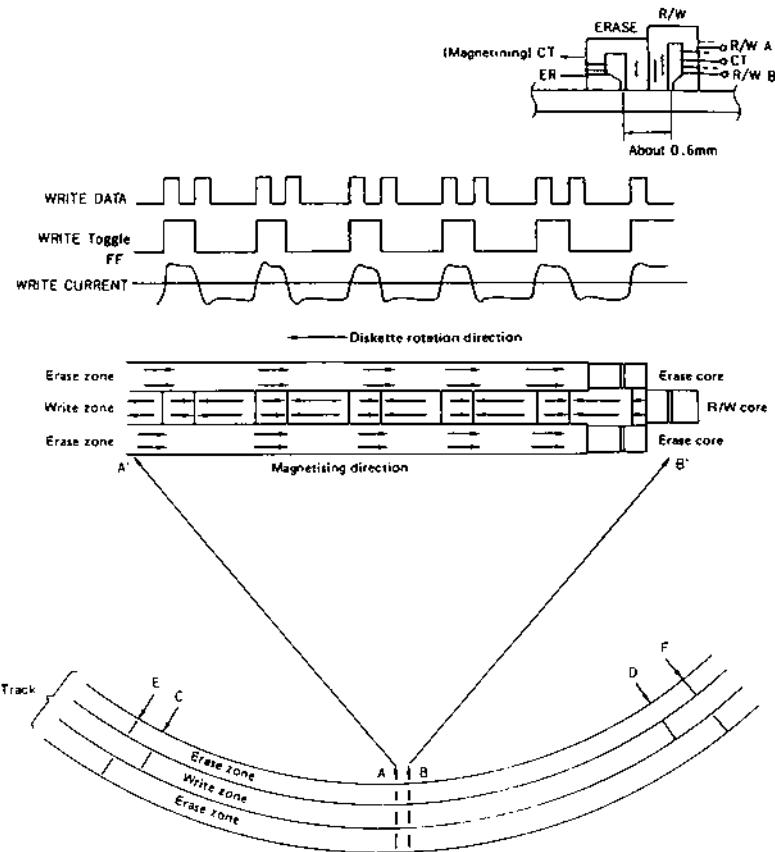


Figure 3-8 Write Operation Concept

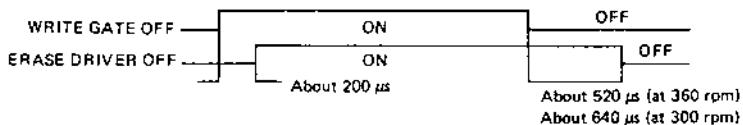


Figure 3-9 Erase Delay Operation Timing Chart

### 3.9 Write-Protect Circuit

The write-protect circuit detects the notch (cutout in the jacket) of the diskette with a sensor to inhibit write operation even if a write gate signal is received from the interface, and outputs a write-protect signal to the interface. Figure 3-16 shows a circuit diagram of the write-protect circuit.

### 3.10 Read Circuit

The diskette is read when the write gate and erase driver are closed.

The R/W core is on a track. If a head has been selected, the core reads the inversions of magnetization of the previously written data to induce a voltage between the two ends of the R/W coil (between R/WA and R/NB). This voltage is input to the read preamplifier via the R/W matrix.

The read preamplifier provides a gain about 200 times the level of a few millivolts induced in the head, and amplifies the input into a differential signal high enough for signal processing.

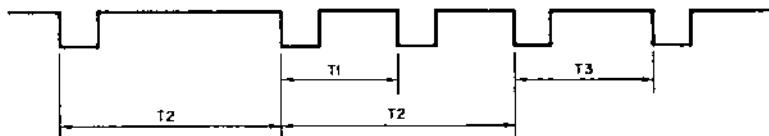
The read signal from the read preamplifier is fed through a low-pass filter that cuts out excess high frequencies. The low pass filter is constructed so that it is automatically switched for high/normal density. It is thus, matched for the optimum frequency of each of the two.

Because the position of inverting magnetization is expressed by a read signal peak, the read signal is fed to a peak-detection circuit to generate a read data pulse.

The peak-detection circuit consists of three blocks.

- Differentiator
- Comparator
- Time domain filter

The differentiator is a differentiating circuit to detect the peak point, and the detected peak point is converted to a zero-crossing point. The differentiated signal is routed to the comparator, where it is converted from an analog signal to a digital signal. The point of change of this digital signal actually becomes a data pulse. FM or MFM means frequency modulation. The frequency of magnetization inversion intervals used are in figure 3-10.



	MFM			Highest frequency (at T1)	
	FM				
	T1	T2	T3		
High density 360rpm	2.0 $\mu$ s	4.0 $\mu$ s	3.0 $\mu$ s	250 kHz	
Normal density 300rpm	4.0 $\mu$ s	8.0 $\mu$ s	6.0 $\mu$ s	125 kHz	
Normal density 360rpm	3.3 $\mu$ s	6.7 $\mu$ s	5.0 $\mu$ s	150 kHz	

Figure 3-10 DATA Timing

Adjacent magnetization inversion waveforms interfere with the magnetization inversion waveform converted from magnetism to an electronic signal, so their combined waveform is read. If magnetization inversion intervals lengthen, however, the mutual interference decreases, resulting in generating a shoulder. When a shoulder is generated, the differentiated waveform zero-crosses so that the wrong data pulse is detected. A time domain filter is provided for removing the wrong data pulse. The time domain filter is constructed so that it is automatically switched for high/normal density. It is thus, set for the optimum frequency for each of the two.

If the comparator output maintains the level prior to the single operation ① following the zero crossover point for a specific amount of time, the time domain filter generates that output as real read data ②.

The read data thus generated is sent to the host system. Figure 3-11 shows a read circuit block diagram and figure 3-12, a read timing chart.

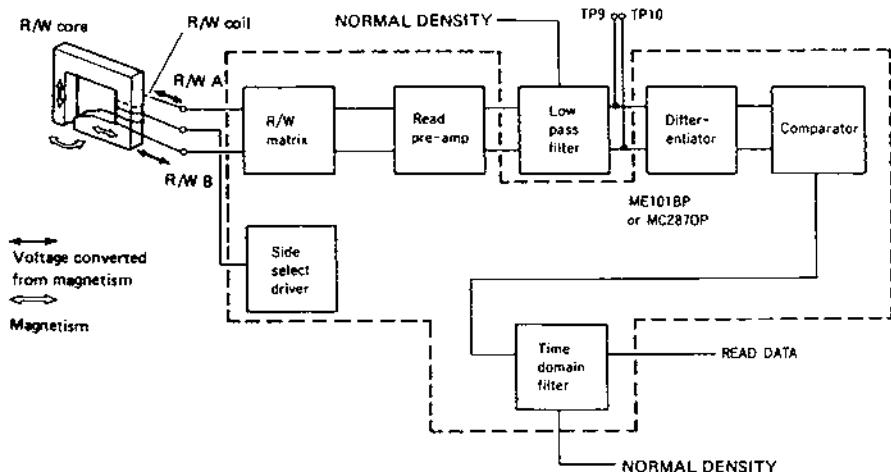


Figure 3-11 Read Circuit Block Diagram

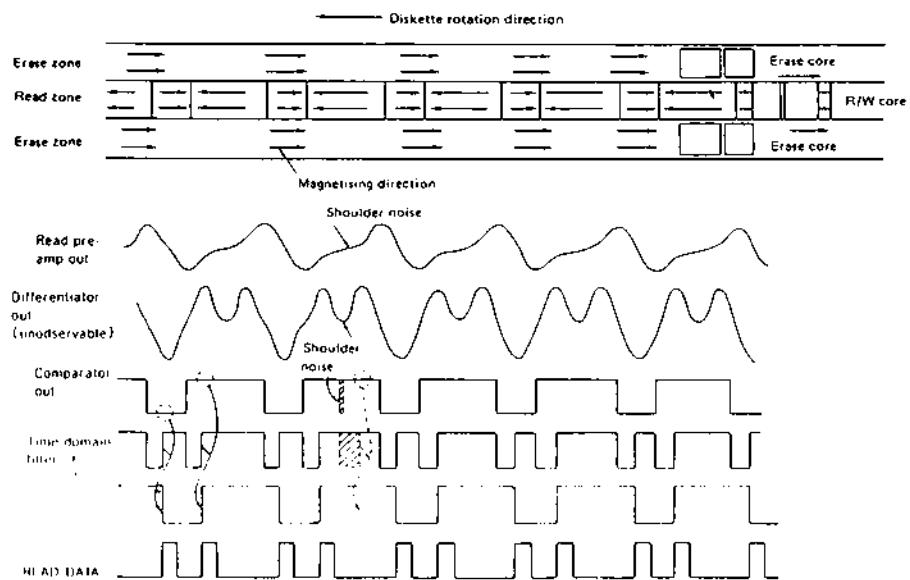


Figure 3-12 Read Timing Chart

### **3.11 Write current switch**

The write is switched on this unit for the optimum recording current for both high and normal density disks.

#### **(1) Write current switch**

Write current for high density disks is set when the interface line is logical "1".

Write current for normal density disks is set when the interface line is logical "0".

### 3.12 Spindle Motor Drive Circuit

The spindle motor is a DC, direct, brushless motor for which a feedback servo circuit is employed to maintain the correct speed at all times. This circuit is installed on a separate printed-circuit board that is built integrally with the motor.

It is connected to the main control circuit with four signal lines: +12 V DC, 0 V, motor-on signal, and IN USE LED.

This feedback servo circuit employs Hall elements for position feedback and a frequency generator, or tachometer generator, for speed feedback to constitute a secondary system to stabilize motor rotation.

Spindle rotating position is detected by the Hall elements located symmetrically from the rotating spindle, and the information is fed to the predriver to alternately switch driver 1 and driver 2.

The speed signal output by the frequency generator for speed control is rectified and integrated into a speed voltage, which is compared with the reference speed voltage to feed back the level of current to be supplied to the coil. The rotational speed of the motor is switched by changing the reference speed value.

Figure 3-13 shows a spindle motor drive circuit block diagram and figure 3-14, a conceptual diagram of the spindle motor drive circuit waveforms.

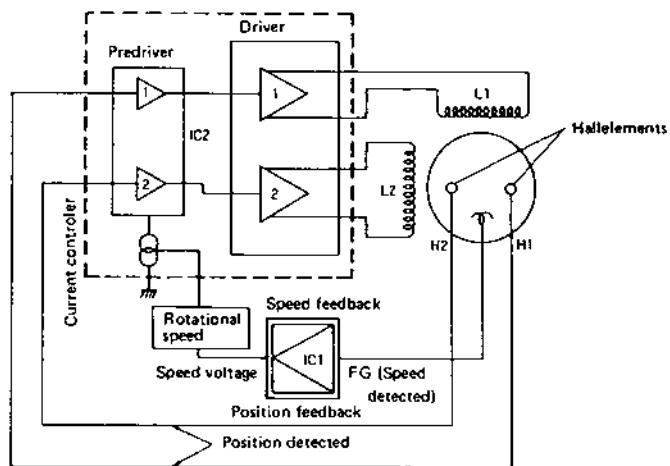


Fig. 3-13 Spindle motor drive circuit block diagram

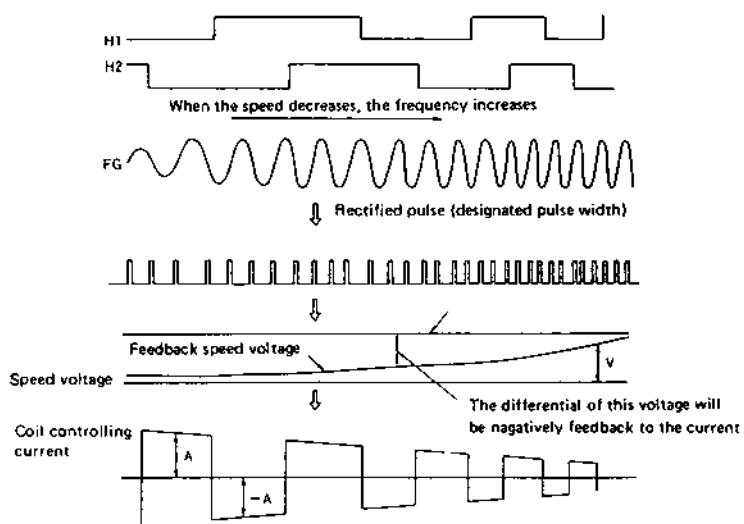


Fig. 3-14 Spindle motor drive current waveform configuration

\*\*\*\*\*  
\* \* 1.2 Meg. Floppy Disk Drive \* \*  
\* \* Section 10 \* \*  
\* \* MF504A-3 Standard Specifications \* \*  
\*\*\*\*\*



UGD-0312 B

**5.25 INCH FLEXIBLE DISK DRIVE  
STANDARD SPECIFICATIONS  
MF504A-347UA**



**MITSUBISHI ELECTRIC CORPORATION**



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## CHAPTER 1 INTRODUCTION

The Mitsubishi MF504A-3 Flexible Disk Drive is a high performance double side Disk Drive designed for use with standard 5.25 inch Diskettes. This device can perform read/write operation both with high density and normal density media.

### 1.1 General Description

1. Use of high density disk with the MF504A-3 Flexible Disk Drive allows for a formatted memory capacity exceeding 1MB, a format compatible with an 8 inch floppy disk drive. It is also a magnetic disk drive which makes possible both read and write operations with normal density media used up to now. However, 48TPI normal density media can read and write, but only 96TPI drive can read the revised data.
2. Input pin 2 is used for switching between high density and normal density media. This allows the rotational speed to be switched between 360 rpm when high density is selected, and 300 rpm when normal density is selected. The READ/WRITE circuitry is also switched at the same time.
3. When normal density has been selected, the setting can be performed so that only the READ/WRITE circuit is switched, while the rotation remains at 360 rpm.
4. A wide variety of user options makes it possible for this device to be used in various operations.
5. Half height (41 mm) dimension of conventional model and two MF504A-3 units can be fit into the industry standard size for one 5-1/4 inch flexible disk drive.
6. The soft-toch, circular gimbal-supported magnetic head provides stable contact with the medium.
7. A high-precision stepping motor and steel bands are used in a combination for the magnetic head position mechanism to achieve a fast 3 ms access time between tracks.

8. Compact Brushless D.C. Motor gives maintenance free.
9. Stable media interchangeability by keeping enough window time margin at off-track in a wide range of ambient conditions.
10. Dynamic clamping function provides high reliability of diskette centering in order to avoid possible mis-clamping.
11. Ejector for the diskette provides ease-of use in the handling the diskette.

## 1.2 Specifications

### 1.2.1 Performance specifications (Table 1-1)

			high density media		normal density media				
Encoding method			FM	MFM	FM	MFM			
Transfer rate (Kbits/s)			250	500	(150)/125	(300)/250			
Memory capacity	Unformatted	Track (K bytes)	5.208	10.416	3.125	6.25			
		Disk (K bytes)	833	1666	500	1000			
		Sector (K bytes)	0.128	0.256					
		Track (K bytes)	3.328	6.656					
		Disk (K bytes)	532.48	1064.96					
	Formatted  15 (16) sectors/ track ( ) is normal density.	Sector (K bytes)	0.256	0.512	0.128	0.256			
		Track (K bytes)	3.840	7.680	2.048	4.096			
		Disk (K bytes)	614.40	1228.80	327.68	655.36			
		Sector (K bytes)	0.512	1.024					
		Track (K bytes)	4.096	8.192					
		Disk (K bytes)	655.36	1310.72					
Recording density			BPI	4935	9870	2961			
Magnetic flux reversal density			FCL	9870	9870	5922			
Number of tracks				160	160/80				
Track density			TPI	96	96/48				
Number of cylinders				80	80/40				
Track radius	00 Track	Side 0		57.150 mm (2.2500 in)					
		Side 1		55.033 mm (2.1667 in)					
	79 Track	Side 0		36.248 mm (1.4271 in)					
		Side 1		34.131 mm (1.3438 in)					
Rotation speed				360 rpm	(360)/300 rpm				
Motor starting time				500msec or less	(500)/400msec or less				
Average latency time				83.3msec	(83.3)/100msec				
Rotation speed change time (360rpm $\rightarrow$ 300rpm)				400msec or less					
1 Track Access time				3msec					
Settling time				15msec or less					
Average Access time				94msec					

Note: ( ) of normal density media is 360 rpm selected.

1.2.2 Physical specifications (Table 1-2)

DC power requirements	
+5V	+5V + 5%, 0.5 A typical 0.7 A max
+12V	+12V ± 5%, 0.6 A typical (seeking) 1.0 A max (Spindle motor operating)
Operating environmental conditions	
Ambient temperature	5°C to 43°C (41°F to 109.4°F)
Relative humidity	20% to 80% (Maximum wet bulb temperature: 29°C (85°F))
Non-operating environmental conditions	
Ambient temperature	-20°C to 51°C (-4°F to 125°F)
Relative humidity	5% to 95%
Heat dissipation	9.7 Watts Continuous seek (typical) 5 Watts Standby (typical) 4 Watts Motor off (typical)
Physical dimensions	(Except for front panel)
Height	41 mm (1.62 in)
Width	146 mm (5.75 in)
Depth	195 mm (7.7 in)
Front panel dimensions	42 x 148.0 mm (1.65 x 5.83 in)
Weight	1.2 kg (2.9 lbs)

### 1.2.3 Reliability specifications (Table 1-3)

MTBF	10,000 POH or more
MTTR	30 minutes
Unit life	5 years or 20,000 energized hours, whichever comes first
Media life	
Insertion	$3 \times 10^4$ or more
Rotational life	$3.5 \times 10^6$ pass/track or more
Error rate	
Soft read error	$10^{-9}$ bit (Two retries)
Hard read error	$10^{-12}$ bit
Seek error	$10^{-6}$ seek

Table 1-3. Table of reliability specification.



## CHAPTER 2 OPERATION OF MAJOR COMPONENTS

### 2.1 System Operation

The MF504A-3 Flexible Disk Drive consists of a medium rotating mechanism, two read/write heads, an actuator to position the read/write heads on tracks, and electronic circuits to read and write data, and to drive these components.

The rotation mechanism clamps the medium inserted into the drive to the spindle, which is directly coupled to the DC brushless direct-drive motor, and rotates it at 360 rpm or 300 rpm. The positioning actuator moves the read/write head over the desired track of the medium. Then, read or write data.

### 2.2 Electronic Circuits

The electronic circuits to drive the individual mechanisms of the MF504A-3 are located on a single printed-circuit board, which consists of the following circuits:

- o Line driver and receiver that exchange signals with the host system
- o Drive selection circuit
- o Index detection circuit
- o Head positioning actuator drive circuit
- o Read/write circuit
- o Write protect circuit
- o Track 00 detection circuit
- o Drive ready detection circuit
- o Head selection circuit
- o In use and panel indicator LED drive circuit

The spindle motor driving circuit is within the PCB that is integrated with the motor. It consists of a rotation speed control servo circuit, motor driving circuit, speed detecting device, and hall detecting device.

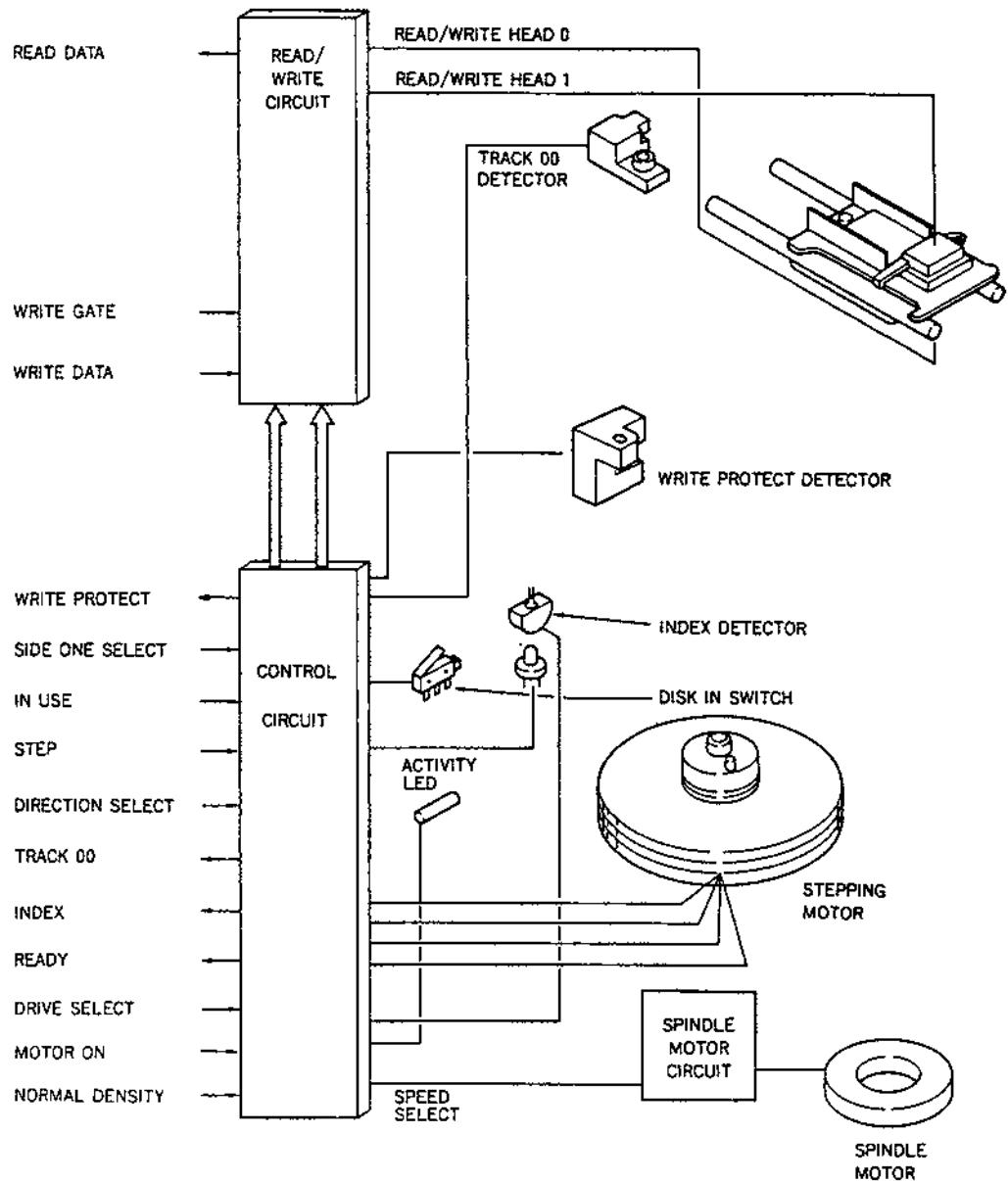


Fig. 1 Functional View

### 2.3 Rotation Mechanism

The diskette rotation mechanism used the DC brushless direct-drive motor to directly rotate the spindle at 360 rpm or 300 rpm.

### 2.4 Positioning Mechanism

The positioning mechanism positions the read/write heads as described below.

The head carriage assembly is fastened to the steel band secured around the capstan of a stepping motor; a 1.8° turn of the stepping motor moves the read/write head one track in the designated direction, thus positioning the read/write head.

This drive system is temperature compensated to minimize read/write head deviations from the disk tracks caused by ambient temperature change.

### 2.5 Read/Write Heads

The read/write heads are MnZn magnetic ferrite.

Each read/write head has three ferrite head cores, consisting read/write core and erase cores on both sides of the read/write core to erase the space between tracks (tunnel erase).

The two read/write heads, which are located face-to-face with a disk between them, are mounted on compliant, gimbal springs so that the heads track the disk with good contact to enable maximum reproduction of the signals from the disk. The high surface tracking ability of the gimbal keeps the disk free of stress, and thus improves diskette life.



## CHAPTER 3 ELECTRICAL INTERFACE

There are two kinds of electrical interfaces: Signal interface and DC power interface.

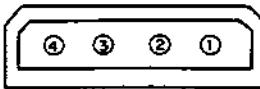
The signal interface sends and receives control signals and read/write data between the MF504A-3 and the host system via the J1/P1 connector.

The DC power interface drives the spindle drive motor of the disk drive, and supplies power to the electronic circuits and the stepping motor which drives the read/write head positioning mechanism via the J2/P2 connector.

The signals and pin arrangement of these two types of interfaces are shown in Tables 3-1 and 3-2.

Table 3-1 DC Power Connector Pin Arrangement (J2/P2)

Source voltage	Pin number	Remarks
+12 V DC	1	
+12 V DC return	2	
+5 V return	3	
+5 V DC	4	



P2 connector

Table 3-2 Signal Connector Pin Arrangement (J1/P1)

Signal	Signal Pin Number	Ground Return Pin Number
NORMAL DENSITY *1	2	1
IN USE	4	3
DRIVE SELECT 3	6	5
INDEX	8	7
DRIVE SELECT 0	10	9
DRIVE SELECT 1	12	11
DRIVE SELECT 2	14	13
MOTOR ON	16	15
DIRECTION SELECT	18	17
STEP	20	19
WRITE DATA	22	21
WRITE GATE	24	23
TRACK 00	26	25
WRITE PROTECT	28	27
READ DATA	30	29
SIDE ONE SELECT	32	31
READY *2	34	33

\*1: This line is used for switching between high and normal density.

\*2: This line can be used as HOLD READY and DISK CHANGE instead of READY with the short plug setting on the PCB.

### 3.1 Signal Interface

The signal interface is classified into control signals and data signals. These interface signal lines are all at TTL levels. The meanings and characteristics of the signal levels are as follows:

- o True = Logical "0" = VL 0 V to +0.4V  
Iin 40 mA maximum
- o False = Logical "1" = VH +2.5 V to +5.25 V  
Iin 0 mA
- o Input impedance = 150 Ohms

#### 3.1.1 Cabling method and input line termination

The drive uses a daisy chain system of cable connections. A single ribbon cable or twisted-pair cable may be fitted with multiple connectors to permit connection of up to four drives.

The connected drives are multiplex-controlled by drive select lines, and any one of the drives can be accessed.

The cabling method and input line termination are shown in Fig. 3-1. A maximum of eight input signal lines, plus the drive select lines, may be terminated at the disk drive proper operation of the drives requires termination at or near the drive connected to the end of the interface cable farthest from the host system.

The drive has detachable terminator modules on the printed-circuit board to terminate these input signal lines.

When a drive is shipped from the factory, its terminators are installed on the printed-circuit board.

Keep the terminators connected in the drive that is connected to the end of the interface cable, and disconnect the terminators in all the other drives.

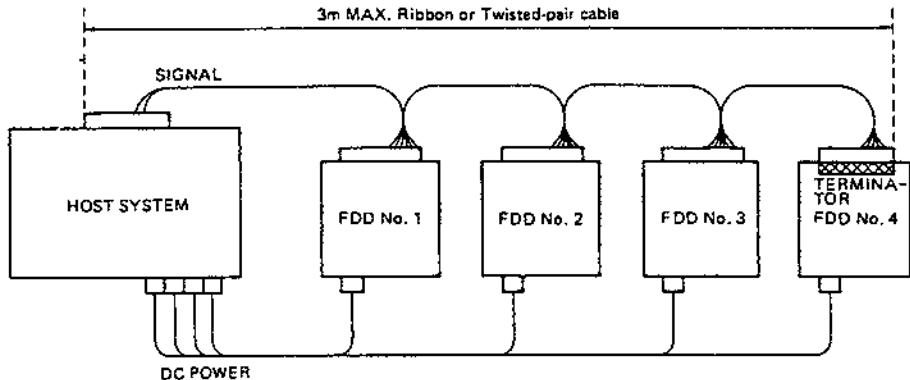


Fig. 3-1 Cabling Method (Sketch)

### 3.1.2 Line driver and line receiver

The recommended interface line driver and line receiver circuits for the host system and the drives are shown in Fig. 3-2.

It is suggested that a Schmitt trigger circuit with a hysteresis characteristic at the switching level be used for the line receiver to improve the noise resistance of the interface lines.

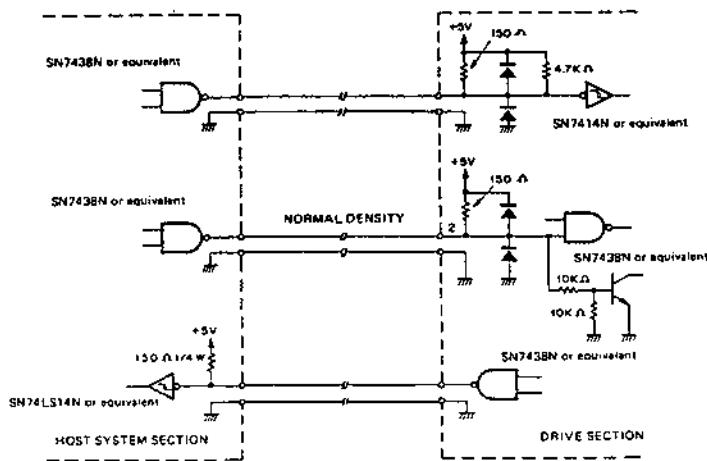


Fig. 3-2 Recommended Line Driver and Line Receiver Circuits

### 3.1.3 Short plug

The short plug sets the conditions for selecting the drive, starting the spindle motor, lighting the LED of the panel indicator and sending the ready signal.

The following is the explanation of features of the short plug.

- (1) Drive selection conditions DS0-3, MX (location A4 of PCB)

#### 1.1) DS0-3

If multiple connection is made with the system and the drive, by short-circuiting one of the DS0-3, the corresponding DRIVE SELECT line will select the drive with the logical "0" only, and input signals can be received.

For example, the drive that has had its DS0-3 short-circuited, will be selected when DRIVE SELECT 0 line is at logical "0".

#### 1.2) MX

When all of DS0-3 has been opened and MX short-circuited, the drive will always be selected regardless of the DRIVE SELECT line of the interface. However, in this case the control of the panel indicator LED can only be done with the IN USE signal. Furthermore, the power of the spindle motor cannot be controlled by DRIVE SELECT 0-3. Therefore it is necessary to revise the conditions to another.

\* DS1 is short-circuited at the factory before delivery.  
Resetting is necessary in order to use another drive number.

- 1.3) The terminator of the DRIVE SELECT line conditions selection TD (Location A3 of PCB) J10

When TD is open, the terminator of the DRIVE SELECT line can be separated.

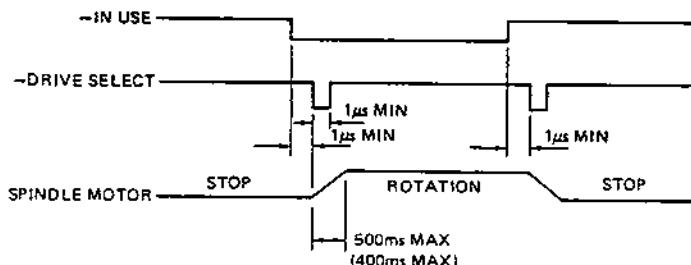
\* TD is shorted when the unit is shipped from the factory.

- (2) Spindle MOTOR ON conditions selection MM, MS (location E3 of PCB)

The conditions for Spindle MOTOR ON conditions are selected by the combination of opening and short-circuiting of MM and MS.

Short plug		Refer to	Notes
MS	MM		
open	short	2.1	Before delivery
short	open	2.2	
open	open	2.3	
short	short	2.4	

- 2.1) Power of the spindle motor is controlled by the MOTOR ON signal.
- 2.2) Power of the spindle motor is controlled by the drive select conditions that have been selected by DRIVE SELECT 0-3 signal.
- 2.3) Power of the spindle motor is controlled by the logic sum of the DRIVE SELECT 0-3 signals and MOTOR ON signal.
- 2.4) Power of the spindle motor is controlled by latching the IN USE signal with the reading edge of the DRIVE SELECT signal. At this time, the short plug IU will be short-circuited.



(Note) : The figures in brackets ( ) are for when the unit is at 300 rpm.

Fig. 5 Spindle motor on/off timing  
(IN USE latching)

- (3) Ready transmission selection conditions DC, 2S  
(location E3 of PCB) RR (location B3 of PCB)

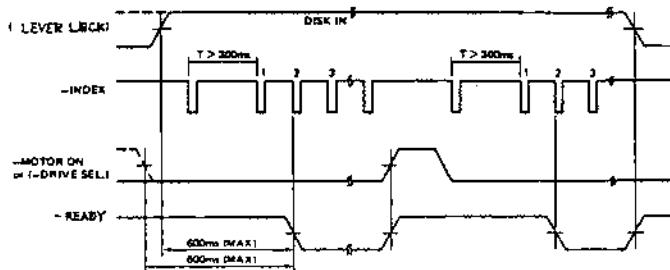
The ready transmission conditions below can be selected with the combination of opening and short-circuiting of DC and 2S.

Short plug		Refer to	Notes
DC	2S		
open	open	3.1	
open	short	3.2	
short	short	3.3	
short	open	3.4	Before delivery

### 3.1) Standard READY

With the standard READY signal, after detection for a disk rotation period of less than 300 ms, the INDEX signal is detected by two pulses and a READY signal is sent to the interface. A maximum of 600 ms is required for the output of the READY signal.

The READY signal interrupts disk rotation and renders it NOT READY for all conditions.



### 3.2) Hold ready

Indicates that the diskette is inserted and the lever is locked. This ready is set within 600 ms from when the lever is locked. When the lever is cancelled, reset starts. In order to perform read/write operations, since ready will be held even if the Spindle motor is turned off, a minimum of 500 ms should be allowed to pass after the spindle MOTOR ON signal (DRIVE SELECT signal in the case when spindle MOTOR ON is done with DRIVE SELECT 0-3) is sent.

### 3.3) Disk change

Indicates that the lever is cancelled immediately after POWER ON.

After the lever has been locked, this signal will be cancelled with the trailing edge of the first DRIVE SELECT signal and will not change with any DRIVE SELECT signal afterwards.

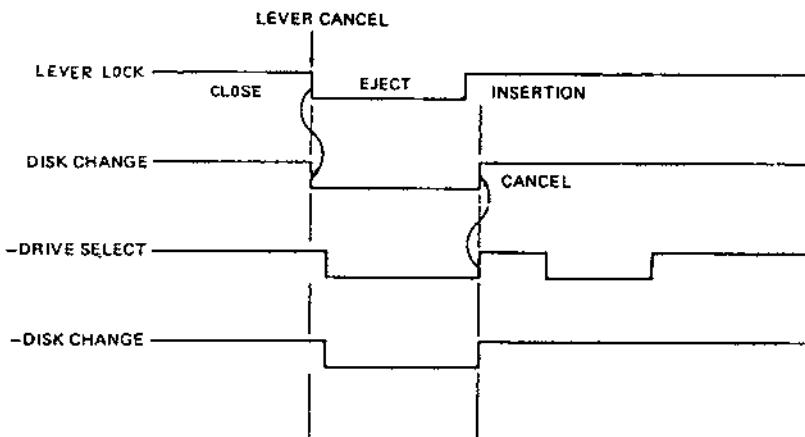


Fig. 6 Disk Change Timing

### 3.4) Diskette change

This signal become active or logic low (logical "0") when the drive door has been disturbed (opened) and reset to the inactive state when the door is closed and a step pulse has been received by the drive.

3.5) RR

In the case RR is short-circuited, the ready signal will be output after the logic product and the DRIVE SELECT signal will be taken.

In the case RR is open, this logic product will be deleted and the DRIVE SELECT signal and ready signal will be outputted regardlessly.

\* RR is shorted when the unit is shipped from the factory.

- 4) Panel indicator LED lighting conditions selection IU  
(location E3 of PCB) IR, IS, IL (location B3 of PCB)

Shown in Table 9.

- 5) Normal density condition selection SS (location C5 of PCB)  
SB (location F4 of PCB)

When SS is shorted and SB is open, the rpm of motor is set to 360 rpm by logical "1" of the NORMAL DENSITY signal, and the read/write circuitry is set for the use of high density media. The rpm of the motor is set to 300 rpm by logical "0" of the NORMAL DENSITY signal, and the read/write circuitry is set for the use of normal density media.

When SS is open and SB is shorted, the rpm is not changed by the NORMAL DENSITY signal, but the read/write circuitry is adjusted as above. Logical "0" of the NORMAL DENSITY signal allows the use of normal density media with a transfer speed of 300 kb/sec.

SS is shorted and SB is open when the unit is shipped from the factory.

Table 9 Panel Indicator LED Lighting Conditions

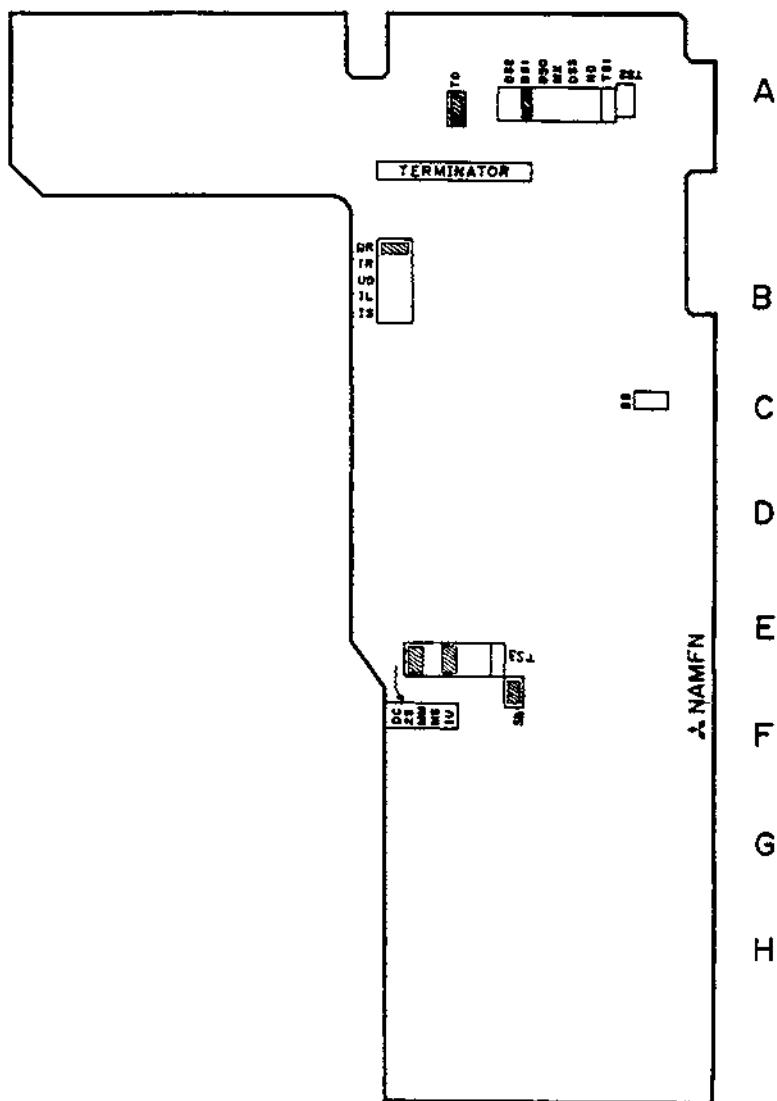
J 3	J 6	J 8	J 9	LED lighting conditions
[I U] Note 1	[I R]	[I S]	[I L]	If the IN USE signal is active, latching and lighting will be initiated with the reading edge of the DRIVE SELECT signal. Afterwards the LED will remain lighted even after the DRIVE SELECT signal inactive. By inputting the DRIVE SELECT signal once again when the IN USE signal is inactive, the latching will be cancelled and the LED will go out with this reading edge. Furthermore, these lighting conditions become effective only when the drive is READY. (Note 3) This setting will be done at the factory before delivery.
[I U]	I R	[I S]	[I L]	The READY conditions will be cancelled from the above lighting conditions.
[I U]	[I R or I R]	I S	[I L]	LED will light with the logic sum of the DRIVE SELECT signal and the lighting conditions by the latching listed above. When the IR is short-circuited, the LED will light at the READY mode and logic product and will be deleted when IR is open. (The same is with the following.)
[I U]	[I R or I R]	I R I S	I L	The LED will light with the logic sum of the DRIVE SELECT and IN USE signals.
[I U]	[I R or I R]	[I S]	I L	The LED will light with the IN USE signal.
I U	[I R or I R]	I S	- Note 2	The LED will light with the DRIVE SELECT signal.
I U	-	[I S]	-	The LED will not light.

- Note 1. The enclosed names are those shorted by jumper plugs. Those not enclosed are open.
2. - indicates that the lighting conditions will not change whether open or short-circuited.
3. When the lighting conditions are included in the ready conditions, stand-by or hold ready transmission conditions are to be used.

Object	Name	Contents	Setting when shipped from the factory	Plug number
Selection of drive select	[DS0]	Drive select 0		J11
	[DS1]	Drive select 1		
	[DS2]	Drive select 2		
	[DS3]	Drive select 3		
	[MX]	The drive select which is usually set		
	[TD]	Connection to the terminator resistance of the DRIVE SELECT signal	[O O] TD	J10
Selection of MOTOR ON conditions	[MM MS]	Motor started by the MOTOR ON signal		J14
	[MM MS]	Motor started by the DRIVE SELECT signal		
	MM MS	Motor started by the MOTOR ON signal or DRIVE SELECT signal		
	[MM MS IU]	Motor started by the IN USE signal latched by DRIVE SELECT signal		
Selection of the signal transmitted from pin 34 of the interface (Connector P1)	[DC 2S]	STANDARD READY is sent		J13
	[DC 2S]	HOLD READY is sent		
	[DC 2S]	DISK CHANGE is sent		
	[DC 2S]	(not used)		
Gate selection for the above transmission signal	[RR]	Gated by DRIVE SELECT signal		J17
	RR	Transmitted as is		
Head unload condition selection	[UD]	Head unload delay released		-
	UD	Head load mode is kept for 3 - revolutions		
Normal density condition selection	[SS SB]	360 rpm when high density is specified 300 rpm when normal density is specified	[O O] SS	J11
	[SS SB]	360 rpm for both high and normal density	[O O] SB	

Note 1 : [ ] means the plug position when shipped from factory.

1            2            3            4            5



Printed-Circuit Board Trace Location

### 3.1.4 Input signal lines

The disk drive has 12 input signal lines. Input signals can be classified into two types: One is multiplexed in a multi-drive system; and the other performs a multiplex operation.

The multiplexing signals are as follows:

- DRIVE SELECT 0
- DRIVE SELECT 1
- DRIVE SELECT 2
- DRIVE SELECT 3

#### (1) DRIVE SELECT 0 to DRIVE SELECT 3

When these drive select lines are at logical "0" level, a multiplexed I/O lines become active to enable read/write operation. These four separate input signal lines, drive select 0 to drive select 3, are provided for connecting four drives to one system and mutually multiplexing them. Jumper pins DS0, DS1, DS2, and DS3 on the printed-circuit board are used to select drive to be made active, corresponding to each of the DRIVE SELECT lines, and specify which of the drives is active.

DS0 is shorted before shipment from the factory, so this setting must be changed when establishing other select lines.

#### (2) SIDE ONE SELECT

This interface line is used to select which of the two sides of the deskette should be read/write operations. When this line is at logical "1," the side 0 head is selected; or when it is at logical "0," the side 1 head is selected. If the polarity of the side one select signal is reversed, delay read/write operation by more than 100  $\mu$ s before execution.

Upon completion of a write operation, reverse the polarity of the side one select signal after a delay of 590  $\mu$ s (\*1). The heads are tunnel type, with a physical core gap deviation between the read/write head and the erase heads so with no

delay, non-erased areas would be generated on the diskette due to a timing difference between the write data area and the erase area during write operation. This is prevented by delaying the erase current ON/OFF time of a few hundred microseconds within the disk drive. Therefore, the head select must not be reversed during this delay time. Also, the track access action must not be permitted for 590  $\mu$ s.

(\*1)

\*1: The interval is 1000  $\mu$ s when normal density at 300 rpm is specified.

(3) DIRECTION SELECT

This interface line controls the direction. (inward or outward) in which the read/write head should be moved when a step signal pulse is applied.

If the signal is at logical "1," the read/write head moves from the center of the diskette outward; if it is at logical "0," the head moves inward.

(4) STEP

This interface line is a pulse signal for moving the read/write head in the direction defined by the direction select line. The read/write head moves by one track each time a signal logical "1," and the step operation starts with the trailing edge of a negative-going pulse (reversal from logical "0" to logical "1").

The direction select line must be reversed more than 1  $\mu$ s before the trailing edge of the step pulse.

(5) WRITE GATE

When this interface line goes to logical "0," the write driver becomes active and the data given to the write data line is written on the selected side of the diskette. When it becomes logical "1," the write drive becomes inactive and the read data logic is enabled. However, the protected read data is

output  $590 \mu s$ \*1) after the write drive become inactive.  
Refer to CHAPTER 4 for the timing.

\*1: The interval is  $1000 \mu s$  when normal density at 300 rpm is specified.

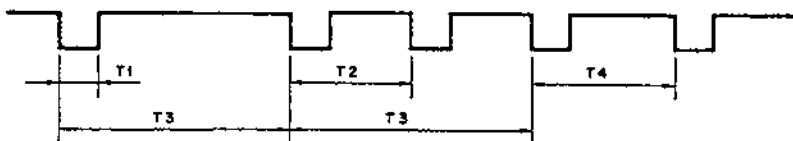
(6) WRITE DATA

Data to written on the diskette is sent to this interface line.

This line is normally at logical "1," and reverses the write current at the leading edge of a negative-going data pulse (reversal from logical "1" to logical "0") to write data bits.

This line is enabled when the write gate goes to logical "0". Fig. 3-3 shows the write data timing.

(Note: The interval is  $1000 \mu s$  when normal density at 300 rpm is specified.)



	MFM			
	FM			
	T1	T2	T3	T4
High density, 360 rpm	150 to 1100ns	$2.00\mu s \pm 10ns$	$4.00\mu s \pm 20ns$	$3.00\mu s \pm 15ns$
Normal density, 300 rpm	150 to 2100ns	$4.00\mu s \pm 20ns$	$8.00\mu s \pm 40ns$	$6.00\mu s \pm 30ns$
Normal density, 360 rpm	150 to 1800ns	$3.33\mu s \pm 17ns$	$6.67\mu s \pm 33ns$	$5.00\mu s \pm 25ns$

Fig. 3-3 Write Data Timing (FM, MFM Encoding)

(7) IN USE

An LED indicator on the front panel lights when this interface line goes to logical "0." The LED is also lit by the drive select.

(8) MOTOR ON

This interface line starts the spindle motor when it goes to logical "0." The write gate does not go to logical "0" until more than 500 ms (the interval is 400  $\mu$ s for 300 rpm) after the motor-on line goes logical "0".

The motor-on line goes logical "1" to stop the motor and keep it off while the drive is out of operation, thus prolonging motor life.

(9) NORMAL DENSITY

This interface line selects whether read/write operations are set for high density or normal density media. Logical "1" corresponds to high density, and logical "0" corresponds to normal density.

When the normal density condition selection plugs SS (shorted) and SB (open) are used to switch the rpm, read/write operations are performed after a wait of more than 400 ms after transmission of this NORMAL DENSITY signal, during which time the rpm is stabilized. When the rpm is switched, write operations always begin after the read/write head moves to track 00. This erase power delay of a few hundred microseconds, which is generated within the drive, is necessary for switching when the head is moved to track 00 or when the power is turned on. When the normal density condition selection plug SS is open and SB is closed, the rpm is always 360 rpm, and there is no waiting, and no need to move the head to track 00.

### 3.1.5 Output signal lines

The drive has five standard output signal lines.

(1) INDEX

This interface line is normally logical "1" but sends a logical "0" output pulse 3.5 ms wide each time the diskette makes one revolution.

This signal signifies the start of a track on the rotating diskette. The index signal timing is shown in Fig. 3-4.

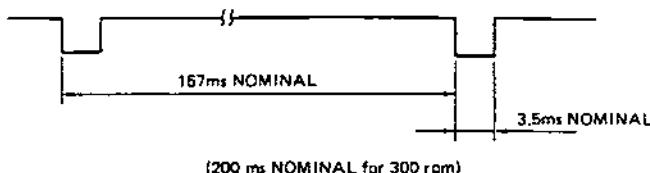


Fig. 3-4 Index Timing

(2) TRACK 00

When this interface line is at logical "0," it indicates that a read/write head of the selected drive is positioned on track 00. If the output of the selected drive is at logical "1," it indicates that the read/write head is positioned on a track other than track 00.

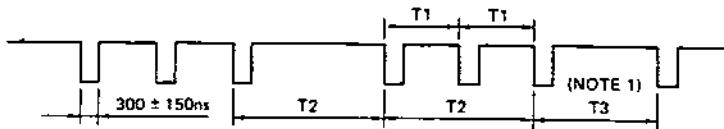
(3) READY

This interface line is logical "1" when the lever is cancelled. The line goes logical "0" (ready) if an index pulse is detected twice or more when the index hole is correctly detected, and the DC power (+5V and +12V) supplied after a diskette is inserted into the drive and the lever is locked.

(4) READ DATA

This interface line reads the data stored on the diskette with the read/write heads, and outputs raw data (combined clock and data signals) converted into pulse signals by an electronic circuit.

The read data line is normally logical "1" but it sends a logical "0" (negative-going) output pulse during a read operation. Fig. 3-5 shows allowable limits on timing variations with the usual diskette and bit shifts.



	MFM		
	FM		
	T1	T2	T3
High density, 360 rpm	$2.00\mu s \pm 400\text{ns}$	$4.00\mu s \pm 800\text{ns}$	$3.00\mu s \pm 600\text{ns}$
Normal density, 300 rpm	$4.00\mu s \pm 800\text{ns}$	$8.00\mu s \pm 1600\text{ns}$	$6.00\mu s \pm 1200\text{ns}$
Normal density, 360 rpm	$3.33\mu s \pm 667\text{ns}$	$6.67\mu s \pm 1333\text{ns}$	$5.00\mu s \pm 1000\text{ns}$

Note : Jitter caused by change in revolution speed are not considered in the above.

Fig. 3-5 Read Data Timing (FM, MFM Encoding)

#### (5) WRITE PROTECT

This interface signal notifies the host system of the insertion of a diskette with a write protect notch into the drive. The signal goes to logical "0" when a write-protected diskette is inserted into the drive. When the signal is at logical "0," write on the diskette is inhibited even if the write gate line becomes active.

#### 3.2 Power Interface

The disk drive requires two types of DC power supplies.

One is +12V DC, which drives the drive motor to rotate the disk. It is supplied to the stepping motor and the read/write circuit. The other is +5V DC, which is used for the logic circuit and the read/write circuit.

#### NOTE

The index LED is driven by the +12V DC.

### 3.2.1 DC power

DC power is supplied via connector J2/P2 on the back of the printed-circuit board. The specifications of the two DC voltages are shown in Table 3-3. The pin arrangement of connector J2/P2 is shown in Table 3-1.

Table 3-3 DC Power Specifications

DC voltage	Voltage variation	Current	Maximum ripple voltage (peak-to-peak)
+5 V DC	$\pm 0.25$ V ( $\pm 5\%$ )	0.7 A maximum 0.5 A typical	50 mV
+12 V DC	$\pm 0.6$ V ( $\pm 5\%$ )	1.0 A MAX (Spindle motor operating) 0.6 A typical at seek	100 mV



## CHAPTER 4 FUNCTIONAL OPERATION

### 4.1 Power On Sequencing

No read/write operation may be performed during the period of 100 ms or more from the start of DC power supply until the control signal stabilizes. And after the period of 600 ms from the Motor On, the drive comes to ready.

The read/write head may have been positioned on an incorrect track after switching the DC power on, so before starting a read/write operation, be sure to perform the step out operation until a track 00 signal is output to the interface line, and thus correctly position the read/write head.

### 4.2 Drive Selection

The disk drive daisy chain cabling system permits connection of multiple drives to a single cable.

These drives are selected when the drive select lines on the drive side become active. Only the drive whose drive select line is active sends and receives signals to and from the host system. The select lines on the drive must have different numbers if two or more drives are connected. If the same number is assigned, an operation error occurs due to interference among the interface output signals of the drives themselves.

### 4.3 Positioning Operation

The seek operation which moves the read/write head to the desired track selects a direction, inward or outward, depending on the polarity of the direction select signal, and moves the head by the step signal. If access to a track two or more tracks away is required, step signal are continuously sent until the head moves to the desired track.

Head movement starts with the trailing edge of the step pulse. Fig. 4-1 shows the operation timing.

#### 4.4 Side One Selection

The read/write heads located on both sides of the diskette are selected by the side one select signal. When the side one select line is high, the Side 0 head is selected. When it is low, the Side 1 head is selected.

#### 4.5 Read Operation

The required timing for read operations is shown in Figs. 4-1 and 3-5. These timing specifications are necessary for accurate read operation.

Two modes of encoding, FM and MFM, are used for the data stored on media. FM is used for single-density read, and MFM for double-density read.

A comparison of the FM and MFM encoding modes is shown in Fig. 4-3.

#### 4.6 Write Operation

The requiring timing for write operation is shown in Figs. 3-3 and 4-1.

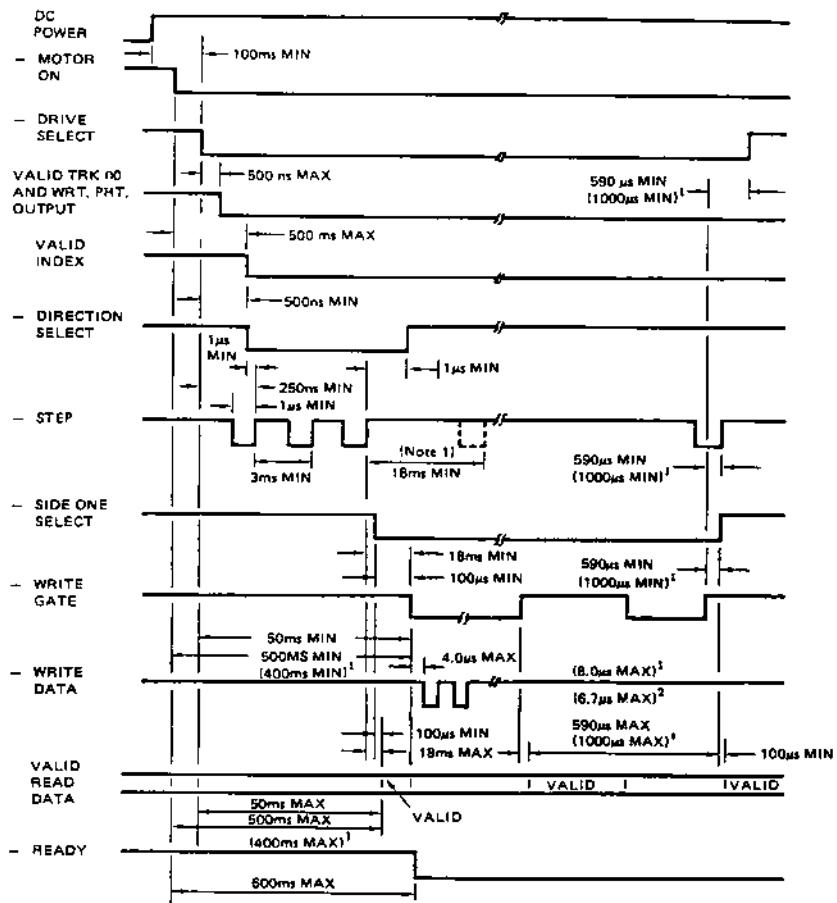
These timing specifications must be strictly observed to ensure an accurate write operation.

Write data can be encoded by either FM or MFM. The disk drive has good contact stability of the read/write heads on the medium and employs high-performance read/write heads, so no precompensation is necessary for correcting the peak shift effect when writing data in the MFM mode (double density).

In case of applying write precompensation, smaller compensation is recommended such as 150ns or smaller.

#### 4.7 READY and dynamic clamp functions

Refer to Fig. 4-2 for standard ready, hold ready, and the timing of the dynamic clamp.

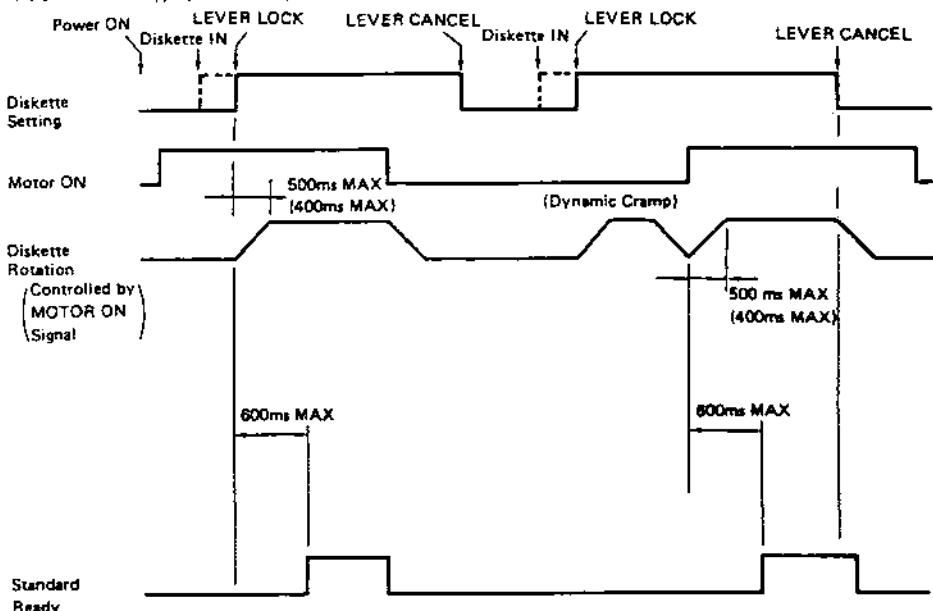


Note 1: When reversing direction, issue a next step pulse after more than 18 ms from the step pulse before inversion.

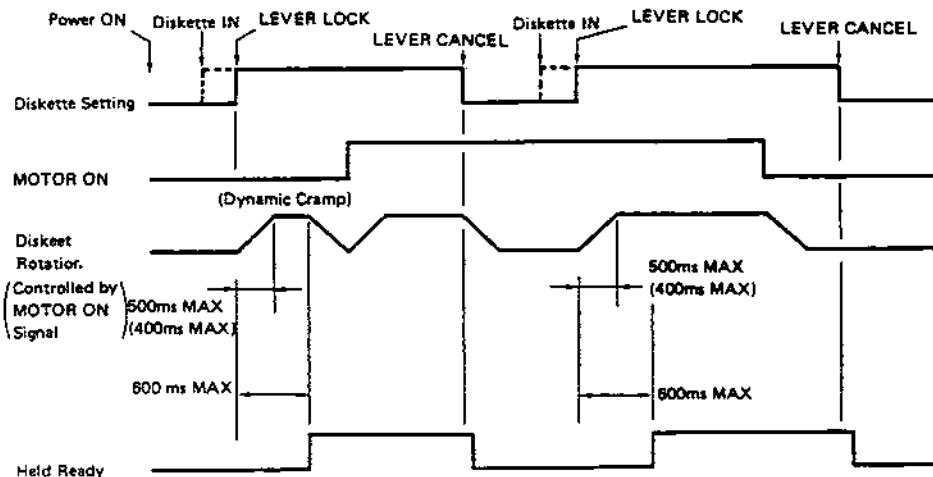
Note 2: The figures in brackets ( )<sup>1</sup> are for when the unit is specified for normal density at 300 rpm.  
The figures in brackets ( )<sup>2</sup> are for when the unit is specified for normal density at 360 rpm.

Fig. 4-1 Control and Data Timing

(1) Standard Ready, Dynamic Cramp



(2) Hold Ready, Dynamic Cramp



Note 1: The figures in brackets ( ) are for when the unit is specified for 300 rpm.

Fig. 4-2 Ready and Dynamic Cramp Timing

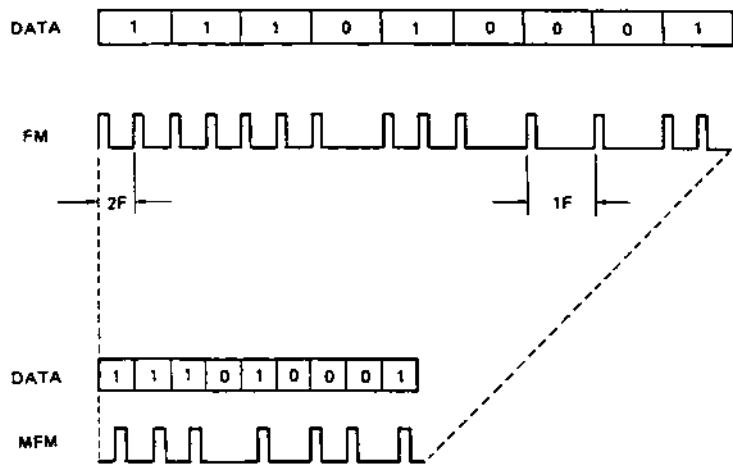


Fig. 4-3 Comparison of FM and MFM Encoding Systems

## CHAPTER 5 PHYSICAL INTERFACE

Electronic interfaces between the disk drive and the host system are accomplished with three connectors. Connector J1 is for the signal interfaces, connector J2 for the DC power supplies, and connector J7 for frame grounding. The connectors used for the disk drive and recommended mating connectors are described below.

### 5.1 Signal Connectors

J1 is a card-edge type, 34-pin (for both sides, or 17 pins for a single side) connector with even-numbered pins (2, 4, to 34) on the parts side and odd-numbered pins (1, 3, to 33) on the soldered side.

A key slot is provided between pins 4 and 6 for the polarity reversal prevention.

The dimensions of J1 are shown in Fig. 5-1.

Recommended Pl connectors that mate with J1 are shown in Tables 5-1 and 5-2.

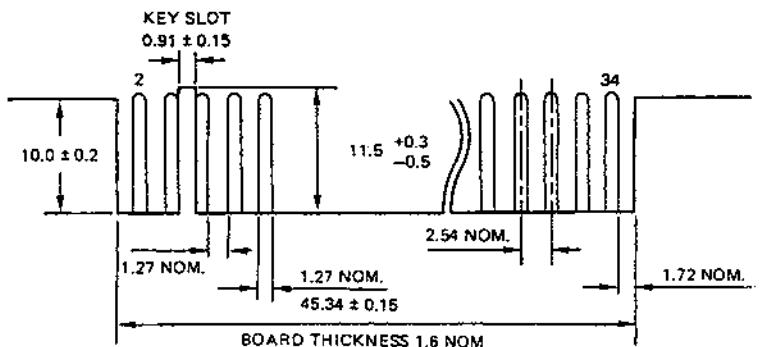


Fig. 5-1 Connector J1 Dimensions (mm) and Pin Numbers

Table 5-1 Connectors for Twisted-Pair Cable (P1)

Parts	Crimp Type	Solder Type
	AMP P/N	AMP P/N
Housing	583717-5	583717-5
Contact	1-583616-1	583854-3
Polarity key	583274-1	583274-1
Crimping tool	90268-1	-
Extraction tool	91073-1	91073-1
Twisted-pair cable (3 m max.)	AWG 26	AWG 26

Table 5-2 Connector for Flat Cable (P1)

Parts	3M P/N	
Connector	3463-0001	
Polarity key	3439-0000	
Crimping tools	Press	3440
	Locator plate	3443-11
	Platen	3442-3
Flat cable (3 m max.)	3365/34	

Items that can be used in conjunction with a connector for the flat cable.

Parts	HIROSE P/N
Connector	HIF5D-34DA-2.54R
Polarity key	CR7C-GPIN

(Items such as a fusing tool. For details refer to the manufacturers of the connector.)

## 5.2 DC Power Connector (J2/P2)

P2 is a four-pin DC power connector made by JST, located on the back of the printed-circuit board. Pin 4 on connector P2 is located closest to J1/P1; the arrangement of the pins as viewed from the side is shown in Fig. 5-2.

The connectors on the drive side and cable side are shown in Table 5-3.

Table 5-3 DC Power Connectors

Parts	J2 (Cable Side)	P2 (Drive Side)
	AMP P/N	JST P/N
Housing	1-480424-0	LC-04A
Contact (4 pins)	60619-1	-
Crimp tool	90124-2	-
Extraction tool	1-305183-2	-
Cable (3 m MAX.)	AWG 18	-



Fig. 5-2 Connector P2

## 5.3 Frame Ground Connector (J7/P7)

FASTON Terminal	Crimp Terminal
AMP P/N 60920-1	AMP P/N 60972-1

## 5.4 Interface Connector Physical Location

Fig. 5-3 shows the physical locations of the interface connectors.

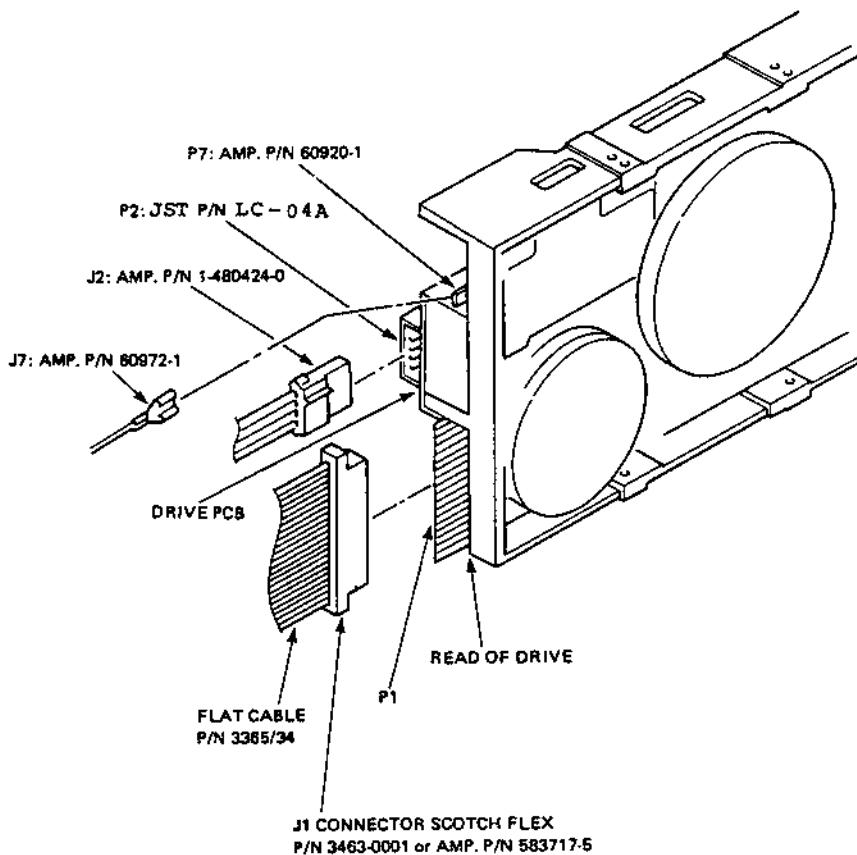


Fig. 5-3 Location of Interface Connectors

## CHAPTER 6 DRIVE PHYSICAL SPECIFICATIONS

### 6.1 Installation Direction

Install the Mini Flexible disk drive in the directions shown in Fig. 6-1.

The slant mount should be within 10 degrees.

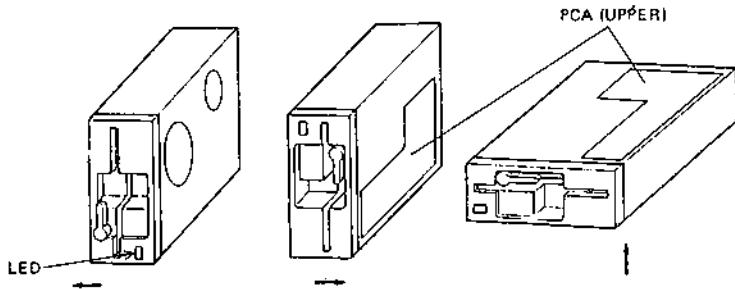


Fig. 6-1 Disk Drive Installation Directions

### 6.2 Dimensions of disk drive

See Fig. 6-2.

### 6.3 Dimensions of Front Panel

See Fig. 6-3.

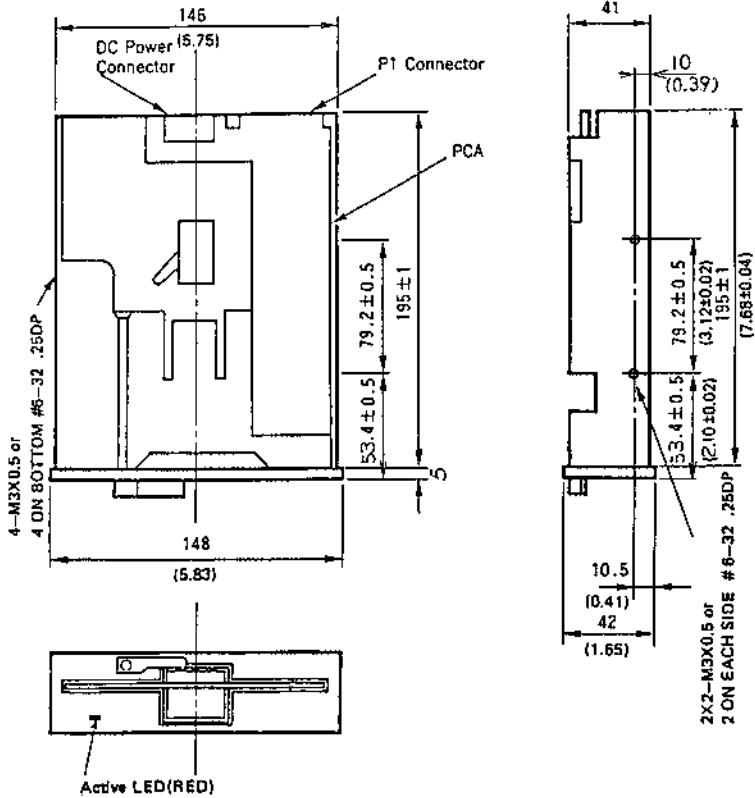


Fig. 6-3 Front Panel Dimensions

Fig. 6-2 Disk Drive Dimensions

## CHAPTER 7 ERROR DETECTION AND CORRECTION

This chapter describes the general cause analysis and corrective procedures to be followed in the event that data errors occur.

### 7.1 Write Errors

If an error occurs during a write operation, it can be detected by performing a read operation on the diskette immediately following the write operation. This is generally called a write check, which is an effective means of preventing write errors. It is recommended, therefore, that a write check be made without fail.

If a write error occurs, repeat the write operation and conduct a write check. If data cannot be correctly written even after the write operation is repeated about ten times, perform a read operation on another track to determine whether the data can be read correctly. If so, a specific track of the diskette is defective. If data cannot be correctly read on the other track, the drive is assumed to have some trouble. If the diskette is defective, replace it.

### 7.2 Read Errors

Most data errors that occur are soft errors. If a read error occurs, repeat the read operation to recover the data.

The following are possible main causes of soft errors:

- o Dust is caught between the read/write head and diskette causing a temporary fault in head contact. Such dust is generally removed by the self-cleaning wiper of the jacket, and the data is recovered by the next re-read operation. If read/write operations is continued for a long time in a very dusty environment, however, hard errors can result from a damaged diskette surface.

- o Random electrical noise ranging in time from a few microseconds to a few milliseconds can also cause read errors. Spurious noise generated by a switching regulator, particularly one that has short switching intervals, deteriorates the signal-to-noise ratio, and increases the number of re-read operations for data recovery. It is necessary, therefore, to make an adequate check on the noise levels of the DC power supplies to the drive and frame grounding.
- o Written data or diskettes may have so small a defect as cannot be detected by a data check during write operation.
- o Fingerprints or other foreign matter on a written diskette can also cause a temporary error. If foreign matter is left on a written diskette for a long time, it can adhere to the diskette, possibly causing a hard error.

It is recommended that the following read operations be performed to correct these soft errors:

- o Step 1: Repeat the read operation about ten times until the data is recovered.
- o Step 2: If the data cannot be recovered by Step 1, move the head to other track, the opposite direction of the previous track position before the designated track, and then return the head to the original position.
- o Step 3: Repeat an operation similar to Step 1.
- o Step 4: If the data cannot be recovered, take the error as a hard error.

## CHAPTER 8 RESHIPMENT PRECAUTIONS

When reshipping the drive, make sure the protection sheet for transportation is in place in the drive, and open the door.

## \* Additional Specifications

This item describes motor speed and data transfer rate of the M4854-1/3S Flexible Disk Drives.

Fig. 1 Implementation of motor speed selection and data transfer rate selection.

Implementation	Short Plug Selection (on PCB)	SS : Short SB : Open		SS : Open SB : Short		See Note 1.
	Normal Density signal (controller output)	logical " 1 "	logical " 0 "	logical " 1 "	logical " 0 "	See Note 2.
Useable Media	High Density	Normal Density	High Density	Normal Density		
Motor Speed	360 rpm	300 rpm	360 rpm	360 rpm		
Data Transfer Rate	500 Kbits/s	250 Kbits/s	500 Kbits/s	300 Kbits/s		

Note 1. See 3.1.3 (7), page 20 in the Standard Specifications.

Note 2. See 3.1.4 (9), page 27 in the Standard Specifications.

Fig. 2 Relation to Formatted Media

Formatted Media	96 TPI High Density (1.6MB) *1	96 TPI Normal Density (1.0MB) *1	48 TPI Normal Density (0.5MB) *1
Read/ Write	Read and Write Possible	Read and Write possible	Read and Write possible *2
Data Transfer Rate of MFM(FM)	500(250) Kbits/s only	250(125)Kbits/s, 300(150)Kbits/s selectable	250(125)Kbits/s, 300(150)Kbits/s selectable

\* 1 ( ) indicates unformatted capacity.

\* 2 Only 96 TPI drive can read the revised data.

\*\*\*\*\*  
\* \* 1.2 Meg. Floppy Disk Drive \* \*  
\* \* Section 11 \* \*  
\* \* Parts List \* \*  
\*\*\*\*\*



**5.25 INCH FLEXIBLE DISK DRIVE  
ILLUSTRATED PARTS LIST  
MF504A-347UA**

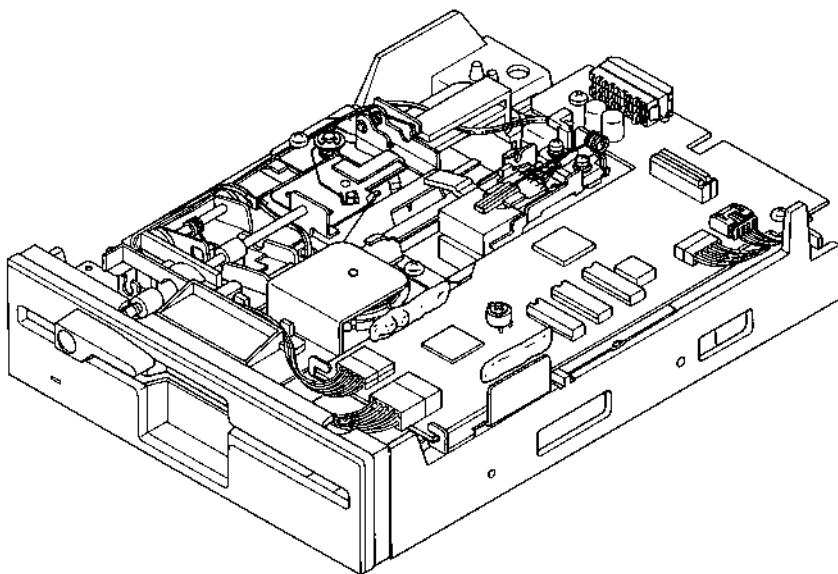


**MITSUBISHI ELECTRIC CORPORATION**



CONTNENTS

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MECHANISM ASS'Y (2).....	3	6
4. FLEXIBLE DISK DRIVE WIRING DIAGRAM .....	4	8



MF504A-34UA Flexible Disk Drive

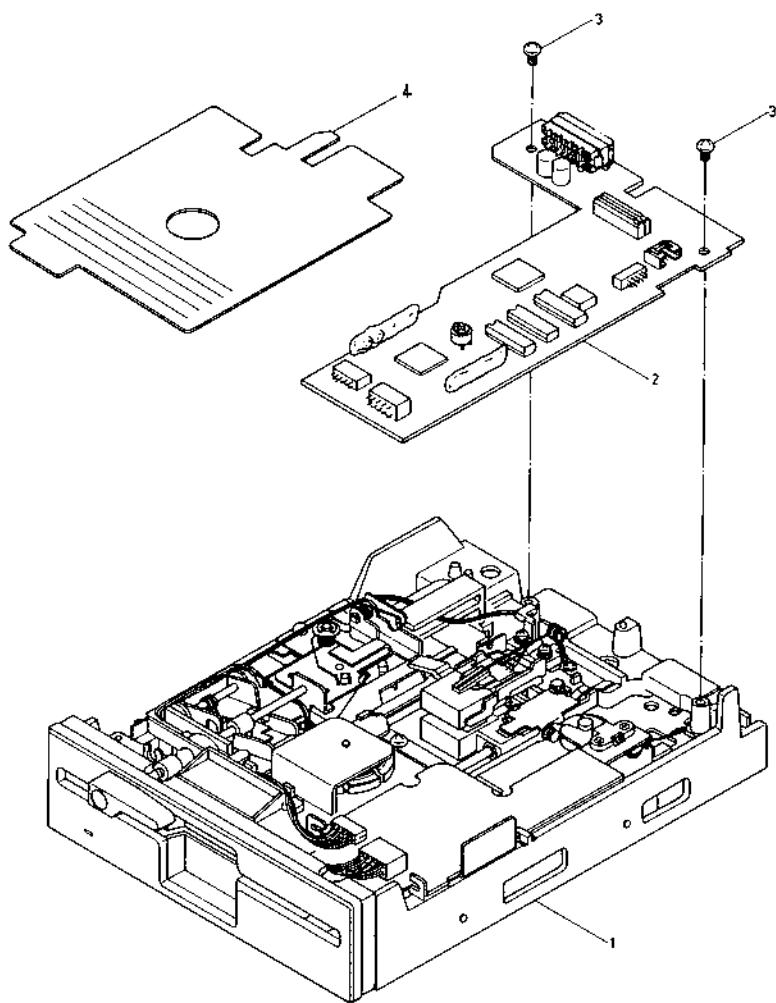


Fig. 1 Flexible Disk Drive

Fig. & Index Number	Part Number	Description	Q'ty
Fig. 1		Flexible Disk Drive	1
1	U951B016G09	Mechanism Ass'y	(1)
2	U241D506G04	PCA-NAMFN3	(1)
3	U650S063H19	Screw-B M3 x 6	(2)
4	U803C166H01	Head Protect Sheet	(1)

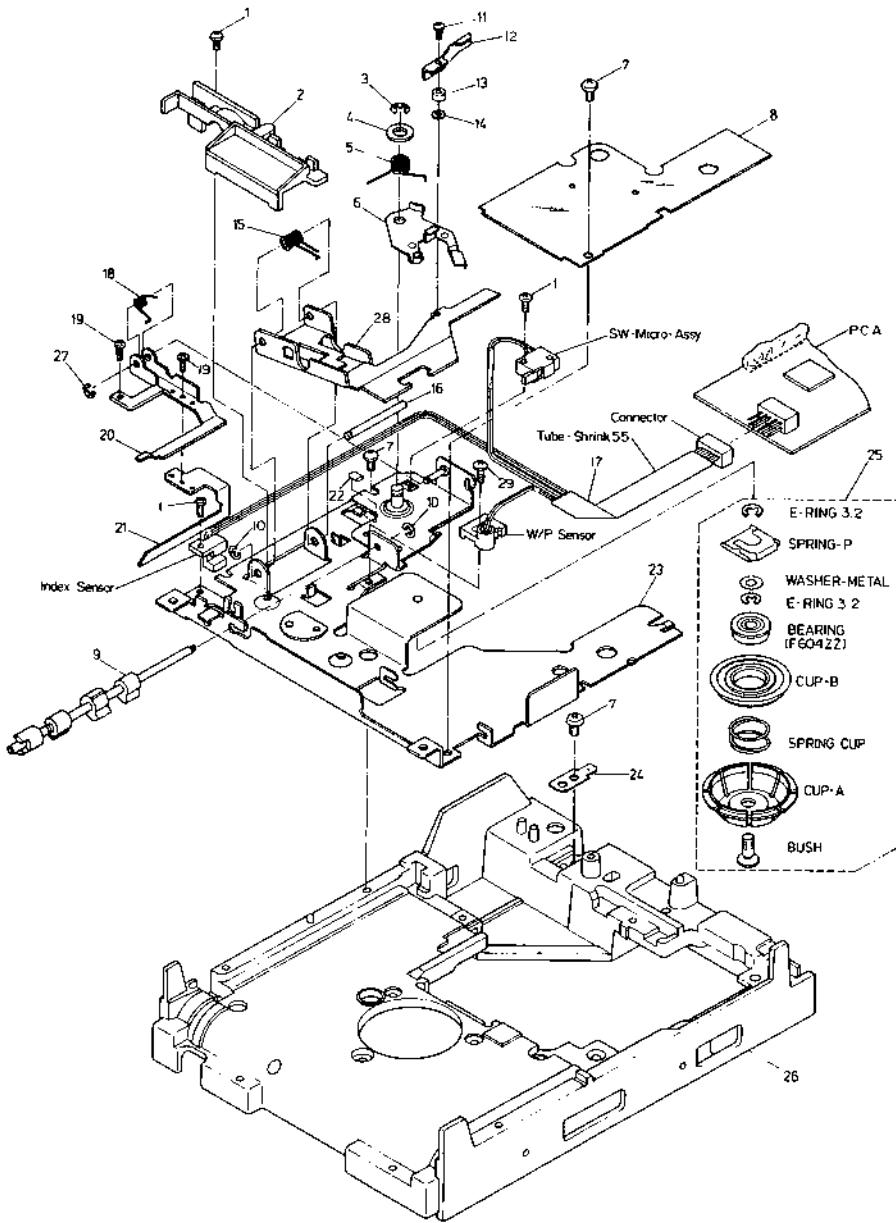


Fig. 2 Mechanism Ass'y (1)

Fig. & Index Number	Part Number	Description	Q'ty
Fig. 2		Mechanism Ass'y (1)	1
1	U650D506H01	Screw-B M2 x 6.5	(4)
2	U541C058H05	Holder	(1)
3	U685S100H05	E-Ring 3	(1)
4	U680S100H02	Washer-CU	(1)
5	U573D074H02	Spring-W	(1)
6	U525C053H02	Lever	(1)
7	U650S063H19	Screw-B M3 x 6	(4)
8	U236D005H04	Spacer-PVC	(1)
9	U536D078G01	Cam Ass'y	(1)
10	U685S100H01	E-Ring 2	(2)
11	U650S063H02	Screw-B M2 x 5	(1)
12	U572D074H02	Spring-P	(1)
13	U550D834H01	Spacer-Metal	(1)
14	U683D084H20	Washer	(1) or (2)
15	U571D094H02	Spring-W	(1)
16	U531D421H01	Shaft	(1)
17	U268C011G05	Sensor Ass'y	(1)
18	U573D075H01	Spring-W	(1)
19	U650S063H77	Screw-B M2 x 3	(2)
20	U525C042H03	Lever	(1)
21	U546D514H03	Holder-L	(1)
22	U073S733H03	Tube-Shrink 8 x 1	(1)
23	U580C088G07	Base Ass'y	(1)
24	U442D164H01	Terminal	(1)
25	U567C003G01	Cup Ass'y	(1)
26	U581A010H26	Frame	(1)
27	U685S100H14	E-Ring 1.5	(1)
28	U525C045H01	Lever	(1)
29	U650S065H86	Screw-B M2.6 x 4	(1)

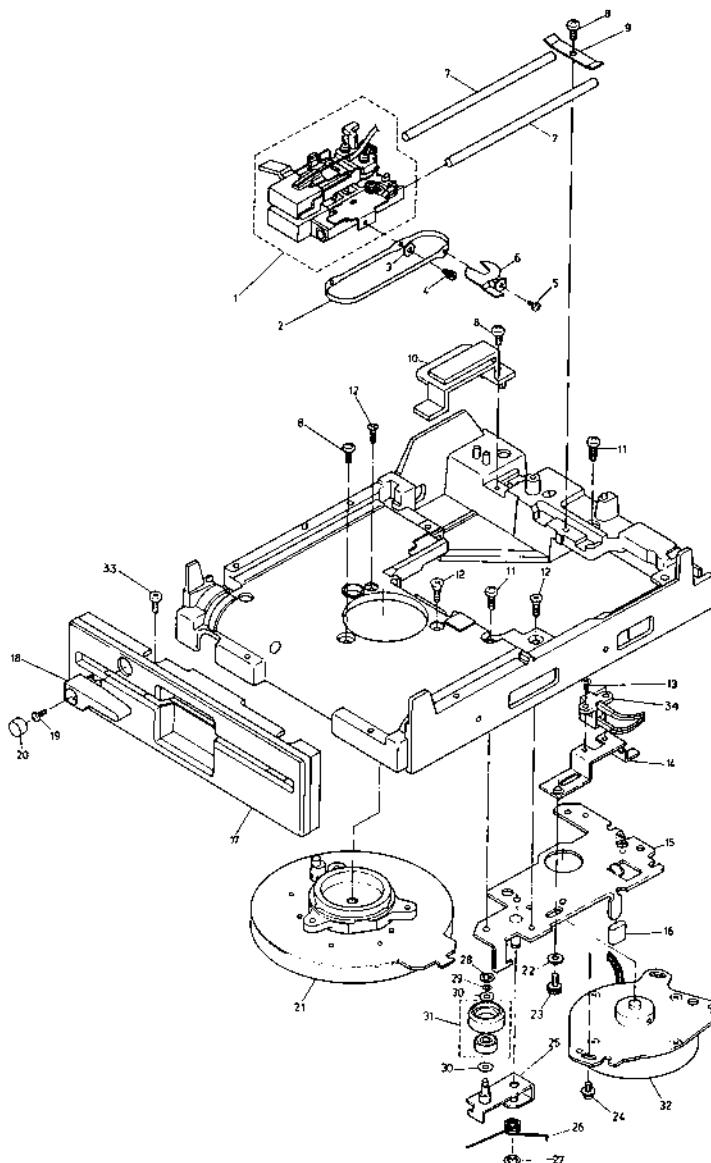


Fig. 3 Mechanism Ass'y (2)

Fig. & Index Number	Part Number	Description	Q'ty
Fig. 3		Mechanism Ass'y	1
1	U587B024G01	Carriage Ass'y	(1)
2	U521C507H03	Band	(1)
3	U680S157H02	Washer-B5	(1)
4	U667S013H01	Bolt M2.5 x 4	(1)
5	U650W021H03	Pan-FE M2.5 x 4	(1)
6	U541C071H01	Holder	(1)
7	U531D423H02	Shaft	(2)
8	U650S063H19	Screw-B M3 x 6	(4)
9	U572D055H01	Spring-P	(2)
10	U541D370H04	Holder	(1)
11	U650S063H20	Screw-B M3 x 8	(2)
12	U650S033H17	Screw-F M3 x 8	(3)
13	U650S033H02	Screw-F M2 x 6	(2)
14	U541D381H01	Holder	(1)
15	U544D197G05	Holder-F Ass'y	(1)
16	U073S733H06	Tube Shrink 13 x 2	(2)
17	U702D062G01	Panel-Front Ass'y	(1)
18	U714C014H01	Knob-Lever	(1)
19	U650S063H03	Screw-B M2 x 6	(1)
20	U567D333H14	Cap	(1)
21	U288Y026H01	Spindle Motor Ass'y	(1)
22	U680S033H03	Washer-3	(1)
23	U667S013H23	Bolt M3 x 6	(1)
24	U669S030H11	Screw-P M3 x 5	(2)
25	U525D897G03	Lever Ass'y	(1)
26	U571D093H01	Spring-W	(1)
27	U685S100H05	E-Ring-3	(1)
28	U685S140H01	CS-Ring 2	(1)
29	U680S033H01	Washer-2	(1)
30	U683S021H07	Washer-PL	(2)
31	U522D523G01	Idler Ass'y	(1)
32	U288Y030H02	Stepping-Motor	(1)
33	U650S063H20	Screw-B M3 x 8	(2)
34	U268D117G03	TK00 Sensor Ass'y	(1)

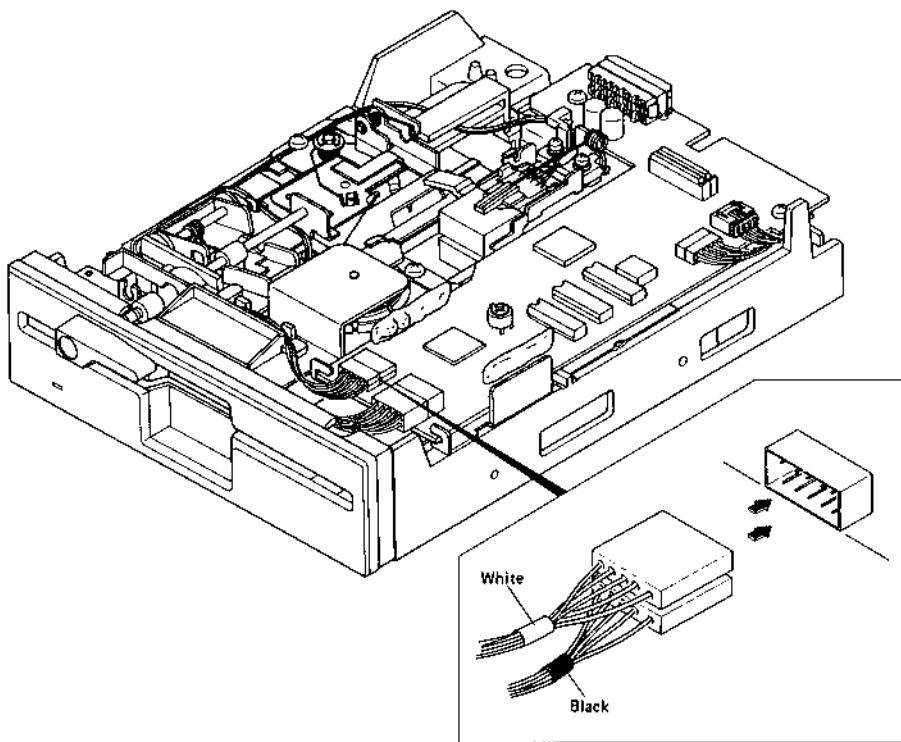


Fig. 4 Flexible Disk Drive Wiring Diagram

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\* 360 K Disk Drive  
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November 15, 1985



**Low Density 360 K. Mitsubishi M4851-347UA  
and MF501A-347UA drives**

The Tandy 3000 uses the Mitsubishi M4851-347UA and MF501A-347UA flexible disk drives with a capacity of 360 K. These standard double sided 5.25" drives can run all standard 40 track single or double sided floppy disks. These drives can be configured to run 300 rpm 40 track single sided or double sided. The drives are normally run in the Tandy 3000 in the double sided 40 track mode but can read or write to any compatible single or double sided 5.25" diskette.

The following pages contain the specifications for your reference in maintenance, troubleshooting and repair of the drives.

Contents	Section
M4851-347UA Normal Jumper Settings	1
M4851-347UA Schematics and Component Layout	2
M4851-347UA Maintenance Manual	3
M4851-347UA Standard Specifications	4
M4851-347UA Parts List	5
MF501A-347UA Normal Jumper Settings	6
MF501A-347UA Schematics and Component Layout	7
MF501A-347UA Maintenance Manual	8
MF501A-347UA Technical Manual	9
MF501A-347UA Standard Specifications	10



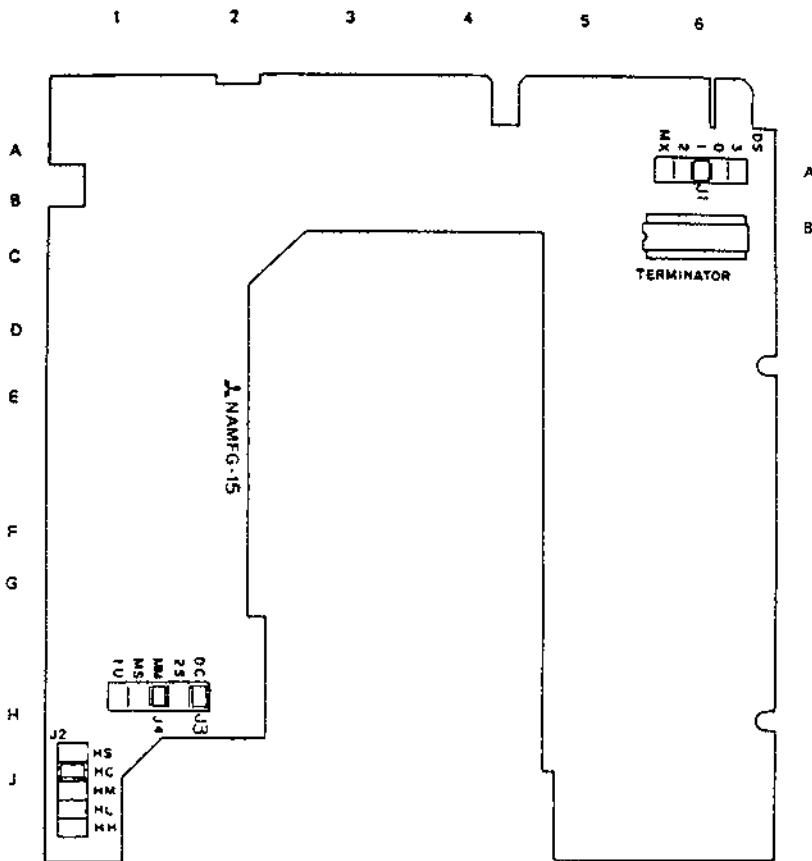
\*\*\*\*\*  
\* \*  
\* \*  
\* 360 K Disk Drive \*  
\* \*  
\* Section 1 \*  
\* \*  
\* Jumper settings \*  
\* \*  
\*\*\*\*\*

November 15, 1985



**360 K Floppy Disk Drive Servo/Logic Board  
Jumper Settings**

1. Check to be sure that HC, DC, MM, DSL, on the servo/logic board are jumpered.





\*\*\*\*\*  
\*  
\*  
\* 360 K Disk Drive  
\*  
\* Section 2  
\*  
\* Schematics & Component layout \*  
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November 15, 1985



**DISK DRIVE  
SCHEMATICS AND  
LOGIC MANUAL**

**M4851-347UA**

<u>Sheet Title</u>	<u>Page</u>	<u>Revision</u>
M4851-347UA DISK DRIVE WIRING DIAGRAM.....	26	B
M4851-347UA PCB NAMFG-15 SCHEMATIC.....	36	B
M4851-347UA PCB NAMFG-15 PARTS LOCATION DIAGRAM.....	46	A
M4851-347UA SPINDLE MOTOR ASSY SCHEMATIC.....	56	A
(NAME : E2SLR36 or TS3400N2E13)		



UGD-0263B



\*\*\*\*\*  
\*  
\*  
\* 360 K Disk Drive  
\*  
\* Section 3  
\*  
\* Maintenance manual  
\*  
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November 15, 1985



**5.25 INCH FLEXIBLE DISK DRIVE  
MAINTENANCE MANUAL  
M4851-3**

 **MITSUBISHI ELECTRIC CORPORATION**



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4. Operating Information .....	2
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4.2 Diskette Handling .....	2
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5.1 Caution .....	4
5.2 Head Cleaning .....	4
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## 1. General

This manual explains the handling, maintenance and adjustments of M4851-3 Flexible disk unit.

## 2. References (schematics and manuals)

M4851-3	
STD SPEC	SJ2-G3473
Schematic Diagram for Maintenance (PCA NAMFG)	UGD-0001
Illust Parts List	TJ2-G30315
Packing Procedure	TJ2-G30272

## 3. Names of Unit Parts

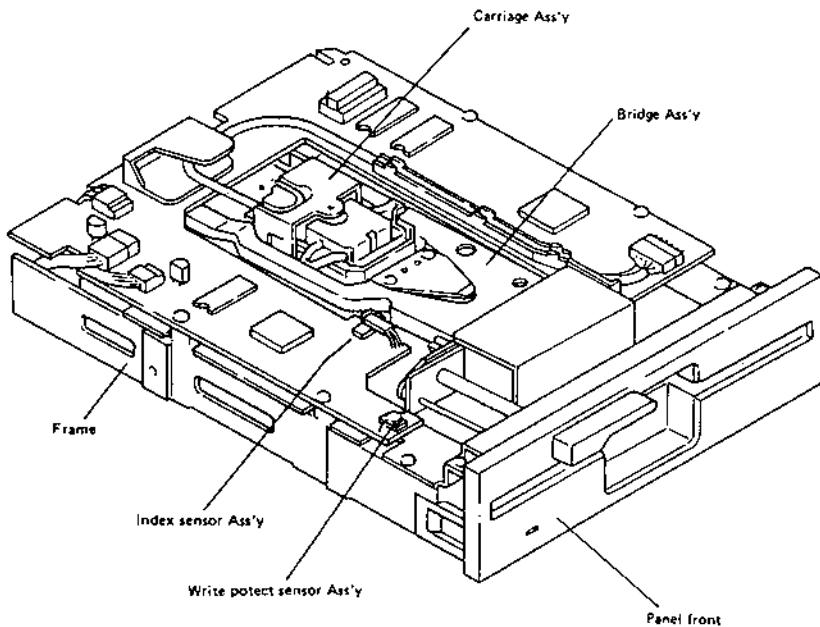


Figure 1

#### **4. Operating Information**

##### **4.1 Environment**

There is no problem in operating under normal office conditions but when operating out of following conditions, Drive may not work properly or Diskette may get damaged.

###### **(1) Temp./Humid. Range**

	During operation	During non operation
Temperature Range	5°C ~ 43°C	-20°C ~ 51°C
Humidity Range	20% ~ 80% RE (DEW LESS)	5% ~ 95% RE (DEW LESS)
(Maximum wet bulb temp. 29.4°C)		

###### **(2) Dust**

Be extra careful of dust entering unit because it may cause damage to head or diskette media.

##### **4.2 Diskette Handling**

(Be extra careful of the following)

- (1) Keep diskette media away from any appliance which may generate magnetic field.  
(ex, Radio, TV, Motor/Dynamo and other electrical appliances)
- (2) Do not bring any ferro magnetic materials near the diskette.
- (3) Do not bend media under any condition.
- (4) Return the diskette to storage envelope when transporting and storing it.
- (5) Do not touch or attempt to clean the disk media surface with alcohol.
- (6) Do not expose diskette to heat, dust, or sunlight.
- (7) Do not write anywhere except on the media label and only use a soft felt tip pen.

#### **5. Require Maintenance**

"Unit life can be affected by damaged parts as a result of dusty environment or excessive operation." So maintenance by such methods as visual inspection, cleaning/change of damaged parts and regular functional checks will keep the unit in good condition and enable the discovery of any problem at an early stage.

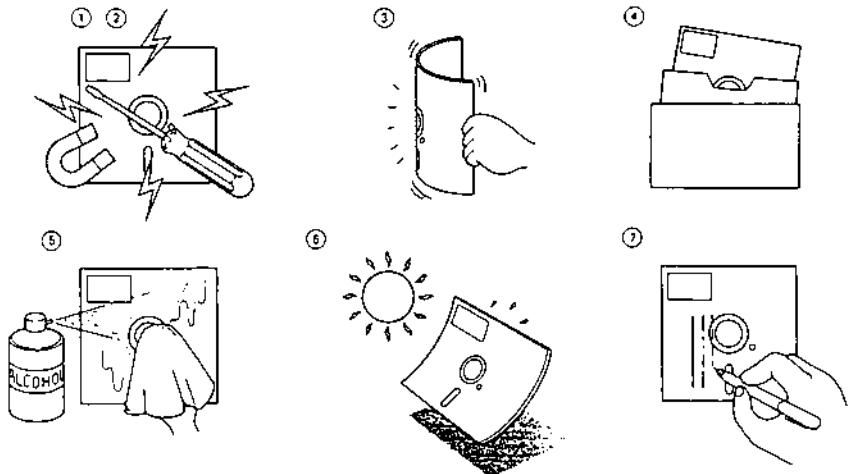


Figure 2

Time span between maintenance is calculated at an actual operation rate of 8 hours a day so in case of greater rate, differences modification is needed. When operating at a normal environment condition, perform maintenance once a year.

### 5.1 Caution

- (1) During maintenance, be careful of dust entering unit, and damaging head.
- (2) Make sure power switch is off first, when starting maintenance.
- (3) When put off/on Printed circuit Board (P.C.B.) Assy, make sure power switch is "off" to protect semiconductors and ICs.
- (4) Do not touch Disk media surface or head directly and do not bring any ferro magnetic materials near it.
- (5) When using this unit for Read data only (when using CE Disk), be careful of write mode mishandling to protect data.
- (6) Do not touch steel belt and do not adjust related mechanism.
- (7) Avoid static shock or excessive force to head carriage assembly because it has been carefully adjusted. Do not readjust any screws except where specified in this manual.

### 5.2 Head Cleaning on field applications

Head cleaning is recommended at user's sites, especially when used in severe environments, because the heads may accumulate dust in the air and magnetic coating material of the disk, causing chance of error increase and/or scratch on the disk surface.

Recommended schedules and procedures are as follows.

#### 1) Cleaning Schedules

- (1) Periodical cleaning using wet type cleaning disk.
  - 1 Once a month for normal usage in normal environments.
  - 2 Should like to be increased up to about once a week when used in severe environments such as dusty area, high humidity, high and low extreme temperatures.  
Low temperature such as 5 to 10°C (41 to 50°F) under high humidity is most severe for diskettes.
  - 3 Higher frequency for brand new drives would be recommended, for about once a week. Better matching between head and medium would be produced by a long time use, as experienced.
- (2) When frequent errors are detected.
- (3) When scratch(es) are found on the medium surface. (Wet or dry type may be use.)

### 3) Procedures of Cleaning

#### (1) Wet type

Dispense the cleaning solution onto the lint-free cleaning disk through the cutout in the disk jacket. Insert the cleaning disk and activate the drive. Load head and rotate disk for 2~3 minutes. Eject cleaning disk and wait for another 2~3 minutes to dry heads.

As the cleaning disk is high in light transmittance, cover the index hole by a semi-transparent material such as tracing paper, or color in black the index hole circular area of the disk, when the head are not loaded on the cleaning disk.

### 4) Other Comments

- (1) Please contact maintenance or service facilities if the above procedures can not recover the good performance.
- (2) The diskette medium is weak for abrasion in temperatures below the specified range (below 10°C or 50°F). The durability in such low temperatures are different largely for

## 5.3 Check and Adjustments

### 5.3.1 Diskette rotational cycle adjustments

#### 1) Equipment

CE Tester

Scratch Diskette

Universal Counter

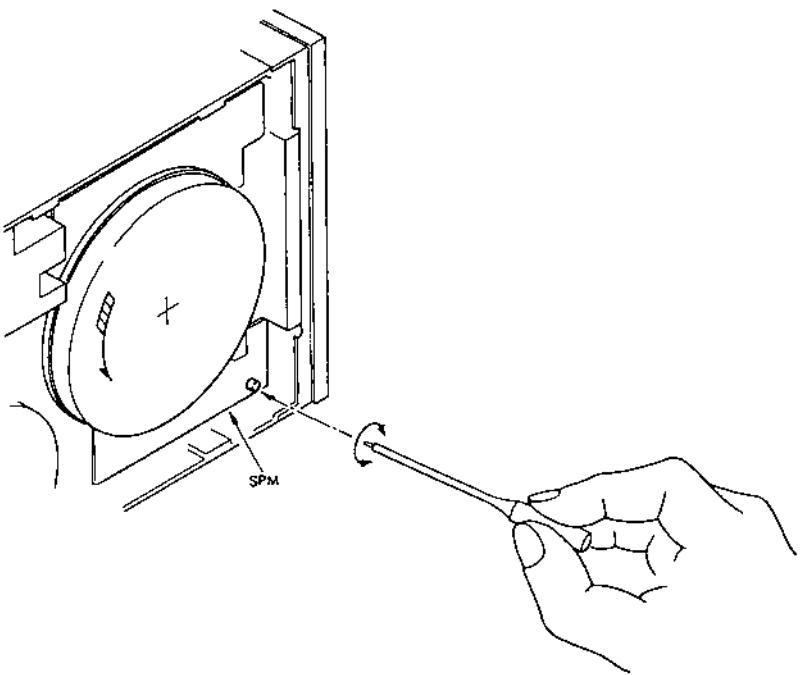
VR Adjustment Driver

#### 2) Adjustment procedure

- 1 Connect CE Tester to Drive then turn-on power switch
- 2 Load diskette then turn-on motor with drive select
- 3 Make sure HLMG ON
- 4 Seek to TK00
- 5 Connect universal counter to INDEK (TPB14) signal and measure rotational cycle rats.
- 6 Adjust counter reading until it comes within specifications using SPM VR (see figure 4)
- 7 After this adjustment, lock VR with white paint.

#### 3) Test specifications

- |            |                   |
|------------|-------------------|
| -1 Check:  | 196.8 – 203.2 ms. |
| -2 Adjust: | 198.6 – 201.4 ms. |



200.0 ms

T=198.6 ~ 201.4

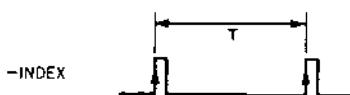


Figure 4

### 5.3.2 TK00 sensor position adjustment

#### 1) Equipments

CE Tester

scratch diskette

No. 1 plus screw driver

oscilloscope

#### 2) Adjustment procedure

-1 Connect CE Tester to drive then turn-on power switch and load diskette

-2 Turn-on motor and select drive

-3 Repeat seek between TK00 and 02 (see figure 5)

-4 Observe waveform (TK00) at TPC13 using oscilloscope.

Trigger: CH1 ..... -STEP (DC, -) TPC 15

Signal: CH2 ..... +TK00 (DC, +) TPC 13

-5 Loosen screw and adjust time T until it comes to within 6.5 – 8.0 ms by moving TK00 in the direction of the arrow. (see figure)

#### 3) Notes:

-1 Set step rate at 6 ms using CE tester

-2 Make sure there are 2 pluses on step signals.

#### 4) Check

-1 Repeat seek between TK02 and TK04

-2 Observe level of signal (TK00) at TPC 13 using oscilloscope.

Trigger: CH1 ..... -STEP (DC, -) TPC 15

Signal: CH2 ..... +TK00 (DC +) TPC 13

-3 Check level of signal is low.

-4 Seek to TK00

-5 Observe level of signal (TK00) at TPC 13 using oscilloscope.

Trigger: CH1 ..... -STEP (DC, -) TPC 15

Signal: CH2 ..... +TK00 (DC +) TPC 13

-6 Check level of signal is high

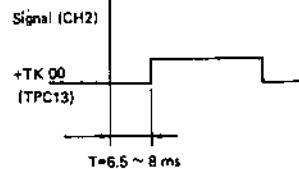
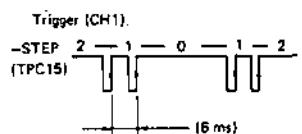
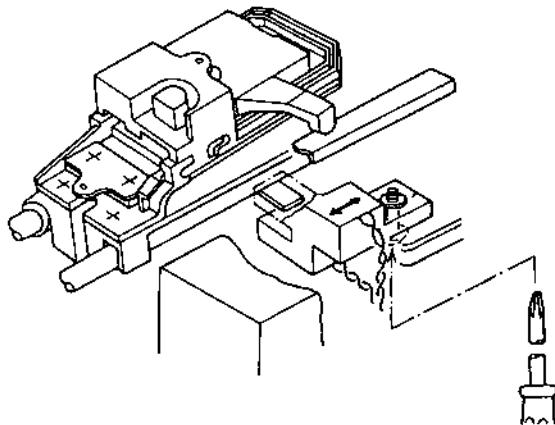


Figure 6

### 5.3.3 INDEX sensor position adjustments

- 1) Equipment
  - CE Tester
  - CE diskette (DYMEX 502-1 STANDARD DISKETTE)
  - Allen wrench(1.5 mm dia)
  - Oscilloscope

- 2) Check procedure
  - 1 Connect CE tester to drive (set power off)
  - 2 Turn-on power switch and motor-on
  - 3 Select drive and load CE diskette  
(Close clamp door slowly)
  - 4 Read timing of each waveform at TPA9.

TPA10 under read mode TK01, using oscilloscope. (see figure)

Trigger: EXT - +INDEX (DC, +) (TPB14)  
CH1 - TPA9 (AC ) }Add  
CH2 - TPA10 (AC, INV)

#### -5 Specification

	Side-0	Side-1
Check	$200 \pm 200 \mu s$	$200 \pm 300 \mu s$
Ajust	$200 \pm 100 \mu s$	$200 \pm 200 \mu s$

All at TK01

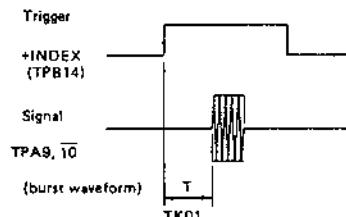
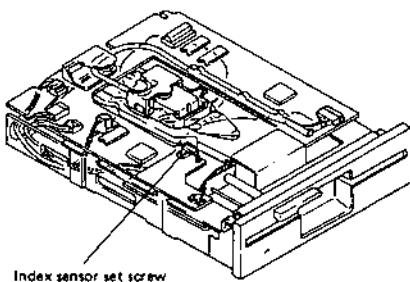


Figure 6

### 5.3.4 Head alignment adjustment

- 1) Equipment
  - CE Tester
  - CE Diskette (DYMEX 502-1 STANDARD DISKETTE)
  - Oscilloscope
  - Allen wrench(2.0 mm dia.)
  - (Fine point diagonal outer)
- 2) Adjustment procedure
  - 1 Connect CE Tester to Drive (set power off).
  - 2 Turn-on power switch and motor on.
  - 3 Select drive and load CE diskette (close clamp door slowly).
  - 4 Seek TK00 to TK16 then read amplitude of each waveform (positioning waveform) at TPA9, TPA10 under read mode (see Figure 7).
 

Trigger:	EXT - +INDEX (DC, +) (TPB14)
Signal:	CH1 - TPA9 (AC ) } Add
	CH2 - TPA10 (AC, INV) }

Specification:	CHECK	ADJUST
when      A > B	B/A > 0.67	0.75
A < B	A/B > 0.67	0.75
  - 6 In case seek direction is TK00 to TK16 or TK39 to TK16, loosen carriage installation screws, then adjust carriage Ass'y signal comes within spec. Tighten screws.
- 3) Note: Adjust under following conditions
  - Temperature: 23°C ±2°C exposed over 2 hours
  - Humidity: 50% ±5%

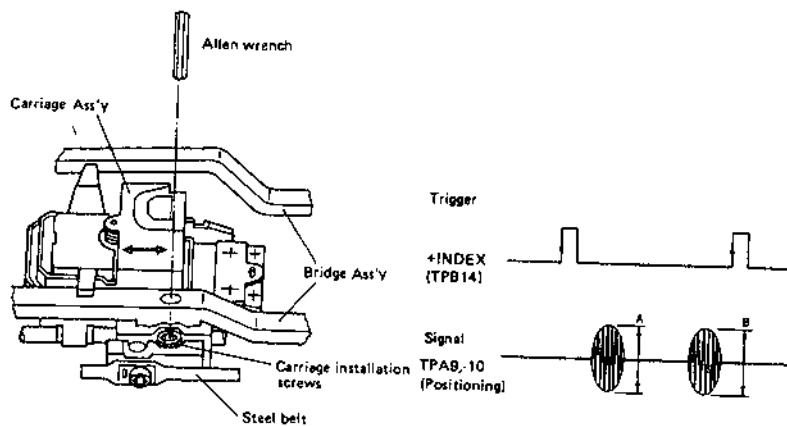


Figure 7

### 5.3.5 Head Azimuth

#### 1) Equipment

CE Tester

CE Diskette

Oscilloscope

#### 2) Check procedure

-1 Connect CE Tester to Drive then turn-on power switch.

-2 Turn on motor.

-3 Select drive and load CE diskette.

-4 Seek to TK34.

-5 Read azimuth waveform using oscilloscope.

Trigger: EXT - +INDEX (DC, +) (TPB 14)

Signal: CH1 - TPA9 (AC )  
CH2 - TAP10 (AC, INV) } Add

-6 Acceptable when adjusted waveform within following range

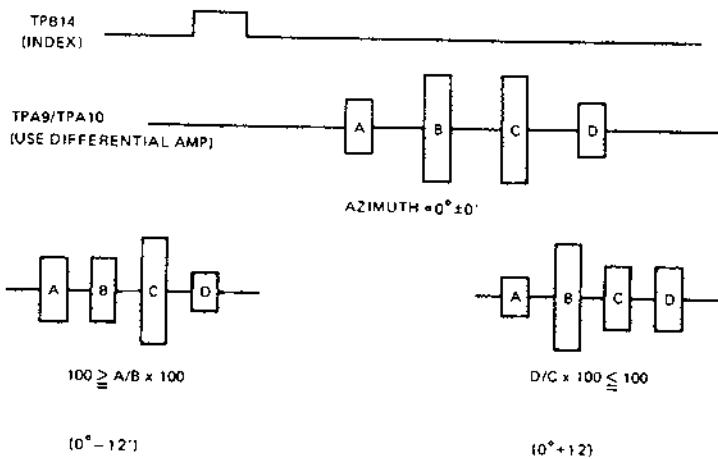


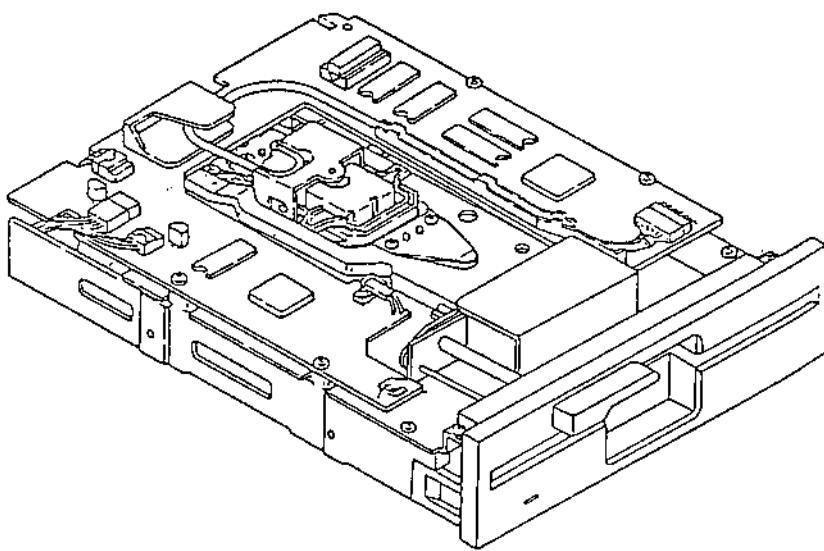
Figure B

**Note:**

The head's azimuth is not adjustable. It is suggested that the drive be sent to an authorized repair center or a new head assembly be installed. In the latter case, all previous adjustments should be made again.

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M4851-3 Flexible Disk Drive

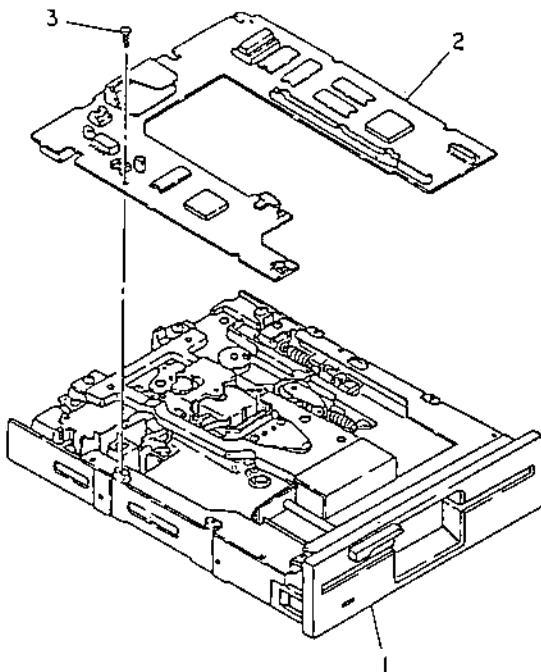


Figure 1. Flexible Disk Drive

Fig. & Index Number	Description	Q'ty
Fig. 1	Flexible Disk Drive	
-1	Mechanism Assy	1
-2	PCA, NAMPG	1
-3	Screw, Pan Hd., Washered (M3x0.5x8 FE)	4

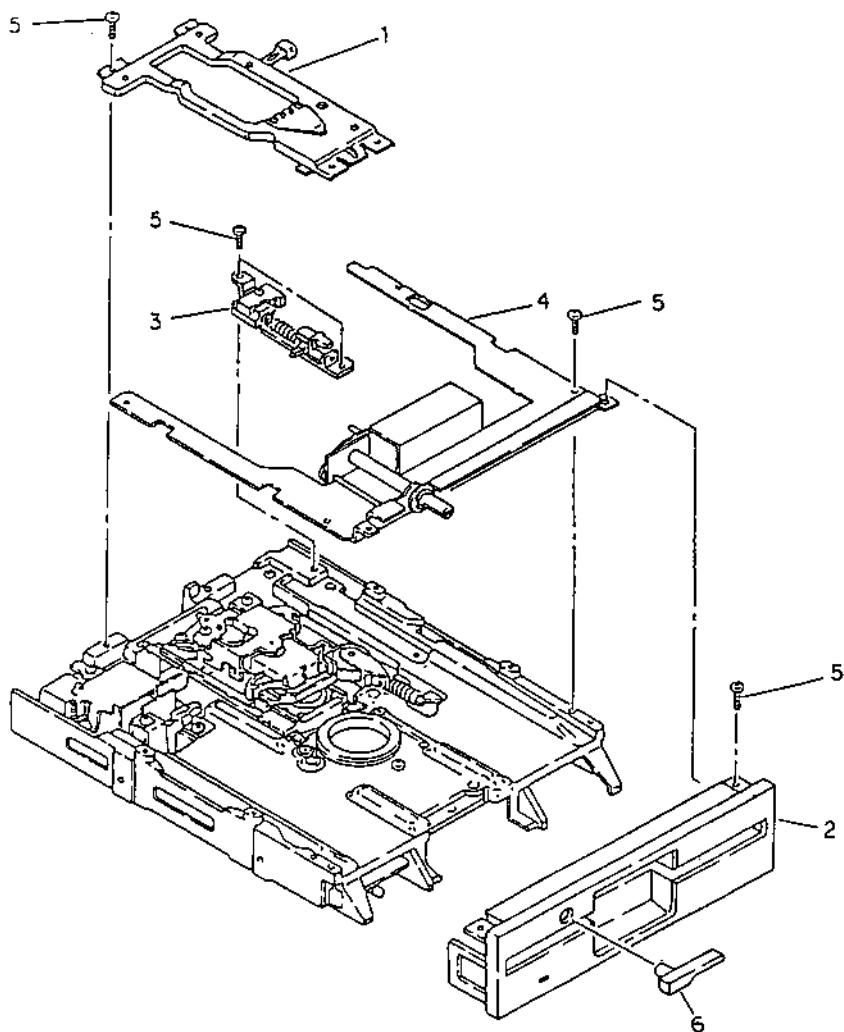


Figure 2-1. Mechanism Assy (1)

Fig. & Index Number	Description	Q'ty
Fig. 2-1	Mechanism Assy (1)	
-1	Cartridge Guide Assy	1
-2	Front Panel	1
-3	Ejector Assy	1
-4	Front Chassis Assy	1
-5	Screw, Pan Hd., Washered (M3x0.5x8 FE)	10
-6	Lever Assy	1

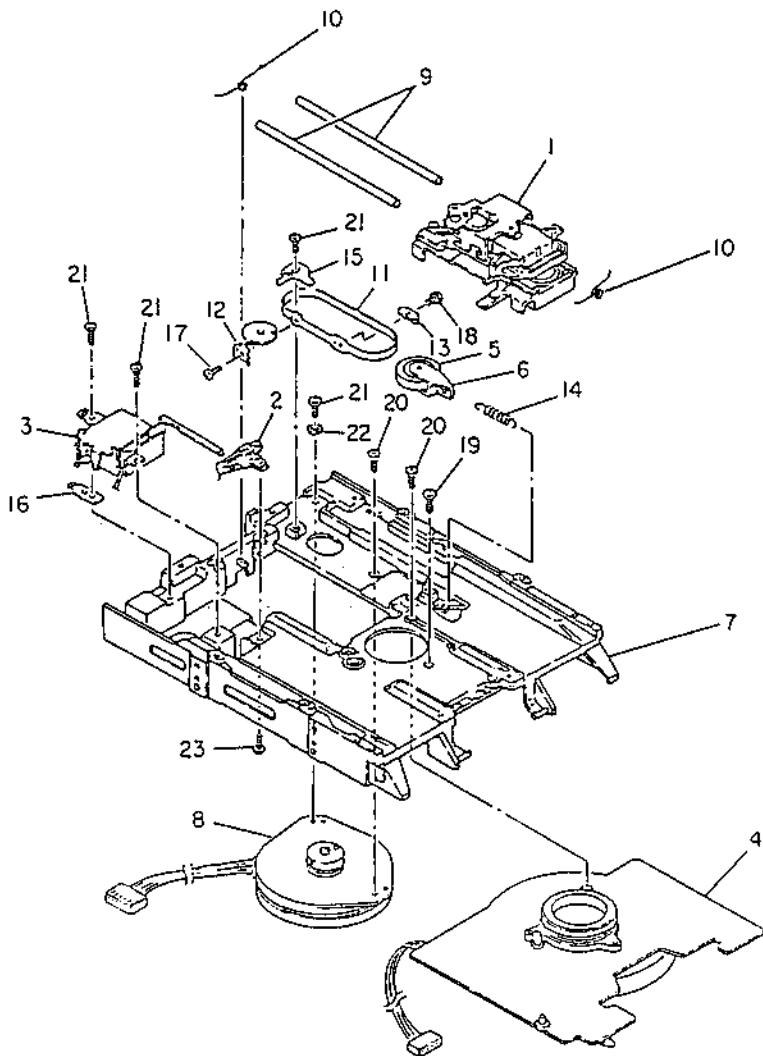


Figure 2-2. Mechanism Assy (2)

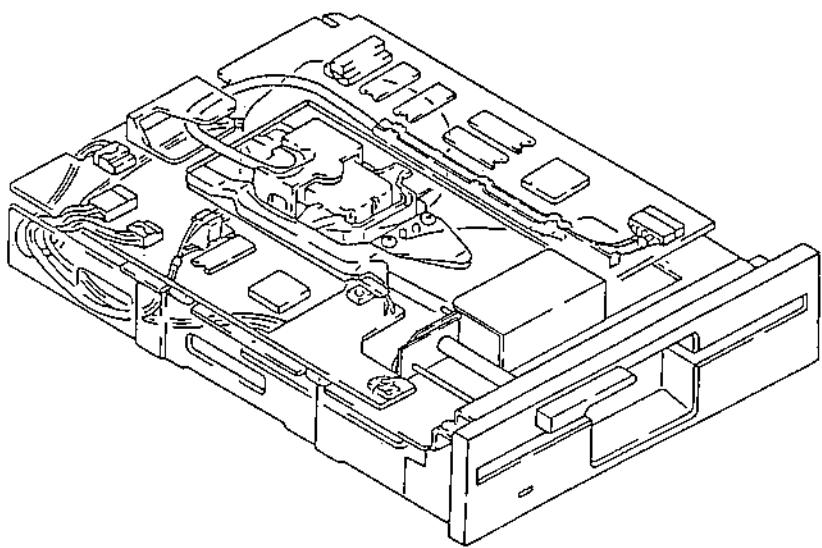


Figure 3. Flexible Disk Drive Wiring Diagram



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*****  
*  
*  
*      360 K Disk Drive  
*  
*          Section 4  
*  
*      Standard specifications  
*  
*****
```

November 15, 1985



5.25 INCH FLEXIBLE DISK DRIVE  
STANDARD SPECIFICATIONS  
M4851 -347UA



MITSUBISHI ELECTRIC CORPORATION



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## CHAPTER 1 INTRODUCTION

The Mitsubishi M4851-3 provide high capacity and high reliability in a compact configuration, with the industry standard 5-1/4 inch media.

### 1.1 General Description

1. Half height (41 mm) dimension of conventional model and two M4851-3 units can be fit into the industry standard size for one 5-1/4 inch flexible disk drive.
2. Ejector for the diskette provides ease-of use in the handling the diskette.
3. The soft-touch, circular gimbal-supported magnetic head provides stable contact with the medium.
4. Compact Brushless D.C. Motor gives maintenance free.
5. Stable media interchangeability by keeping enough window time margin at off-track in a wide range of ambient conditions.
6. Low power consumption can be achieved by a diskette detection function.
7. Dynamic clamping function provides high reilability of diskette centering in order to avoid possible mis-clamping.

## 1.2 Specifications

### 1.2.1 Performance specifications (Table 1-1)

Table 1-1 Performance Specifications

	Double Density
Memory capacity	
Unformatted	
Disk	500 kilobytes
Per surface	250 kilobytes
Per track	6.25 kilobytes
Formatted	256 bytes/selector
Disk	327.7 kilobytes
Per surface	163.8 kilobytes
Track	4096 bytes = 256 bytes x 16 sectors
Transfer rate	250 kilobits/second
Average latency time	100 ms
Access time	
Track to track	6 ms
Average	103 ms (including 6 ms step time and settling time)
Settling time	25 ms
Head loading time	50 ms
Motor starting time	250 ms (READY ON TIME 600ms MAX.)

1.2.2 Functional specifications (Table 1-2)

Table 1-2 Functional Specifications

	Double Density
Recording density	5877 BPI
Magnetic flux inversion density	5877 FCI
Encoding method	MFM
Track density	48 tracks per inch
Number of cylinders	40
Number of tracks	80
Number of heads	2
Rotation speed	300 rpm
Rotation period	200 ms
Index	1
Media	5.25 inch industry standard media

1.2.3 Physical Specifications (Table 1-3)

Table 1-3 Physical Specifications

DC power requirements	
+5 V	$+5 \text{ V} \pm 5\%$ , 0.5 A typical 0.7 A max
+12 V	$+12 \text{ V} \pm 5\%$ , 0.5 A typical (seeking) 1.0 A max
Operating environmental conditions	
Ambient temperature	5°C to 43°C (41°F to 109.4°F)
Relative humidity	20% to 80% (Maximum wet bulb temperature: 29°C (85°F))

Table I-3 (cont.)

Non-operating environmental conditions	
Ambient temperature	-20°C to 51°C (-4°F to 125°F)
Relative humidity	5% to 95%
Heat dissipation	8.5 Watts Continuous seek (typical) 5 Watts Standby (typical) 4 Watts Motor off (typical)
Physical dimensions	(Except for front panel)
Height	41 mm (1.62 in)
Width	146 mm (5.75 in)
Depth	195 mm (7.7 in)
Front panel dimensions	42 x 148.0 mm (1.65 x 5.83 in)
Weight	1.3 kg (2.9 lbs)

1.2.4 Reliability specifications (Table 1-4)

Table 1-4 Reliability Specifications

MTBF	10,000 POH or more
MTTR	30 minutes
Unit life	5 years or 20,000 energized hours, whichever comes first
Media life	
Insertion	$3 \times 10^5$ or more
Rotational life	$3.5 \times 10^6$ pass/track or more
Tap-tap	$10^5$ on the same spot of a track
Error rate	
Soft read error	$10^{-9}$ bit (Two retries)
Hard read error	$10^{-12}$ bit
Seek error	$10^{-6}$ seek

## CHAPTER 2      OPERATION OF MAJOR COMPONENTS

### 2.1    System Operation

The M4851-3 Flexible Disk Drive consists of a medium rotating mechanism, two read/write heads, an actuator to position the read/write heads on tracks, a solenoid to load the read/write heads on the medium, and electronic circuits to read and write data, and to drive these components.

The rotation mechanism clamps the medium inserted into the drive to the spindle, which is directly coupled to the DC brushless direct-drive motor, and rotates it at 300 rpm. The positioning actuator moves the read/write head over the desired track of the medium. Then, the head loading solenoid loads the read/write head on the medium to read or write data.

### 2.2    Electronic Circuits

The electronic circuits to drive the individual mechanisms of the M4851-3 are located on a single printed-circuit board, which consists of the following circuits:

- o Line driver and receiver that exchange signals with the host system
- o Drive selection circuit
- o Index detection circuit
- o Head positioning actuator drive circuit
- o Head loading solenoid drive circuit
- o Read/write circuit
- o Write protect circuit
- o Track 00 detection circuit
- o Drive ready detection circuit
- o Head selection circuit
- o In use and panel indicator LED drive circuit

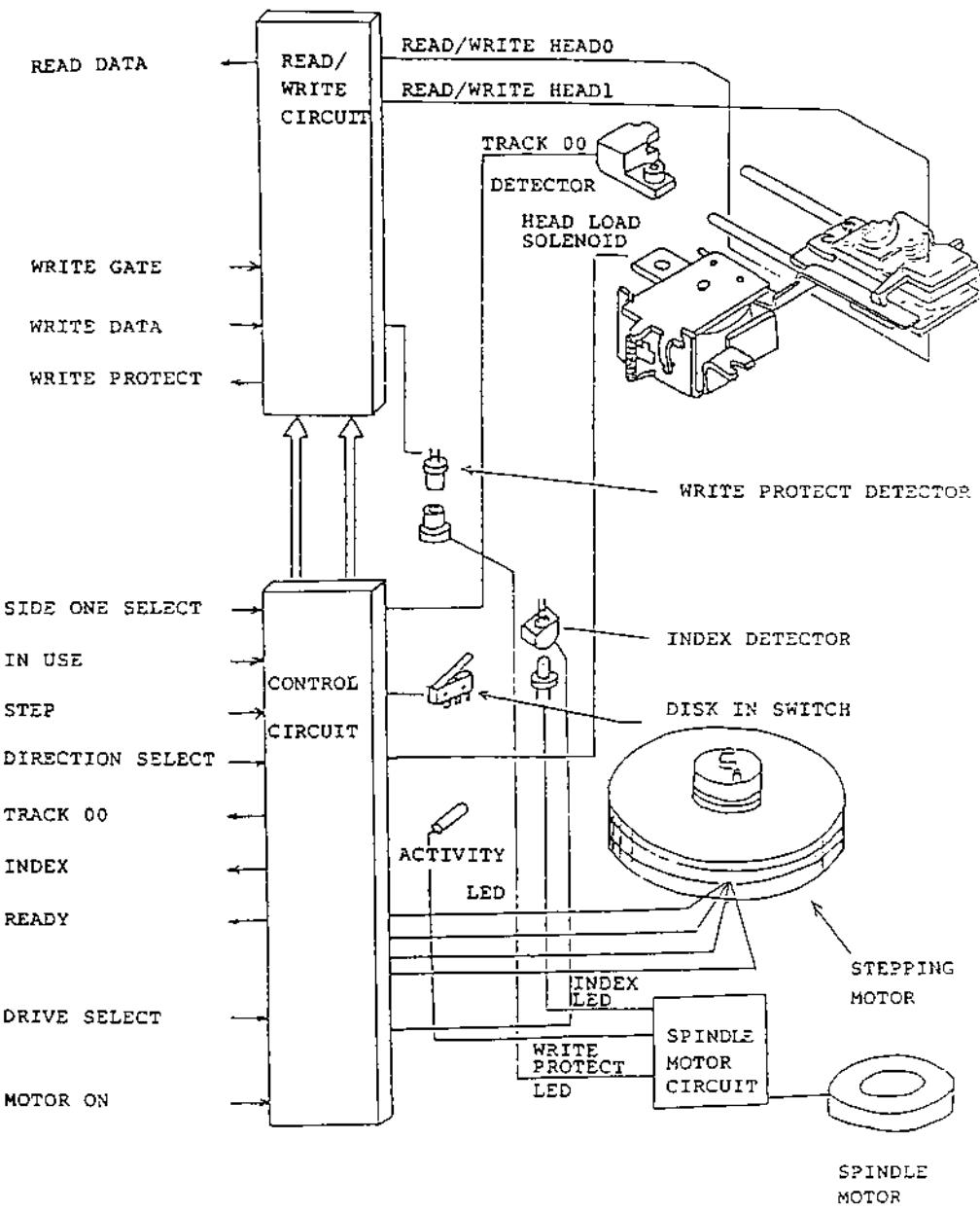


Fig. 1 Functional View

### 2.3 Rotation Mechanism

The diskette rotation mechanism uses the DC brushless direct-drive motor to directly rotate the spindle at 300 rpm.

### 2.4 Positioning Mechanism

The positioning mechanism positions the read/write heads as described below.

The head carriage assembly is fastened to the band secured around the capstan of a stepping motor; a 3.6° turn of the stepping motor moves the read/write head one track in the designated direction, thus positioning the read/write head.

This drive system is temperature compensated to minimize read/write head deviations from the disk tracks caused by ambient temperature change.

### 2.5 Read/Write Heads

The read/write heads are MnZn magnetic ferrite.

Each read/write head has three ferrite head cores, consisting read/write core and erase cores on both sides of the read/write core to erase the space between tracks (tunnel erase).

The two read/write heads, which are located face-to-face with a disk between them, are mounted on compliant, circular gimbal springs so that the heads track the disk with good contact to enable maximum reproduction of the signals from the disk. The high surface tracking ability of the circular gimbal keeps the disk free of stress, and thus improves diskette life.

## CHAPTER 3 ELECTRICAL INTERFACE

There are two kinds of electrical interfaces: Signal interface and DC power interface.

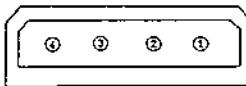
The signal interface sends and receives control signals and read/write data between the M4854-1 and the host system via the J1/P1 connector.

The DC power interface drives the spindle drive motor of the disk drive, and supplies power to the electronic circuits and the stepping motor which drives the read/write head positioning mechanism via the J2/P2 connector.

The signals and pin arrangement of these two types of interfaces are shown in Tables 3-1 and 3-2.

Table 3-1 DC Power Connector Pin Arrangement (J2/P2)

Source voltage	Pin number	Remarks
+12 V DC	1	
+12 V DC return	2	
+5 V DC return	3	
+5 V DC	4	



P2 connector

Table 3-2 Signal Connector Pin Arrangement (J1/P1)

Signal	Signal Pin Number	Ground Return Pin Number
SPARE	2	1
IN USE	4	3
DRIVE SELECT 3	6	5
INDEX	8	7
DRIVE SELECT 0	10	9
DRIVE SELECT 1	12	11
DRIVE SELECT 2	14	13
MOTOR ON	16	15
DIRECTION SELECT	18	17
STEP	20	19
WRITE DATA	22	21
WRITE GATE	24	23
TRACK 00	26	25
WRITE PROTECT	28	27
READ DATA	30	29
SIDE ONE SELECT	32	31
READY	34	33

Signal pin 2 is isolated at the FDD side from the other pins. There is no need for it to be pulled up or pulled down at the control side when it is not being used.

### 3.1 Signal Interface

The signal interface is classified into control signals and data signals. These interface signal lines are all at TTL levels. The meanings and characteristics of the signal levels are as follows:

- o True = Logical "0" = VL 0 V to +0.4 V  
Iin 40 mA maximum
- o False = Logical "1" = VH +2.5 V to +5.25 V  
Iin 0 mA
- o Input impedance = 150 Ohms

#### 3.1.1 Cabling method and input line termination

The drive uses a daisy chain system of cable connections. A single ribbon cable or twisted-pair cable may be fitted with multiple connectors to permit connection of up to four drives.

The connected drives are multiplex-controlled by drive select lines, and any one of the drives can be accessed.

The cabling method and input line termination are shown in Fig. 3-1. A maximum of seven input signal lines, plus the drive select lines, may be terminated at the disk drive. Proper operation of the drives requires termination at or near the drive connected to the end of the interface cable farthest from the host system.

The drive has detachable terminator modules on the printed-circuit board to terminate these input signal lines.

When a drive is shipped from the factory, its terminators are installed on the printed-circuit board.

Keep the terminators connected in the drive that is connected to the end of the interface cable, and disconnect the terminators in all the other drives.

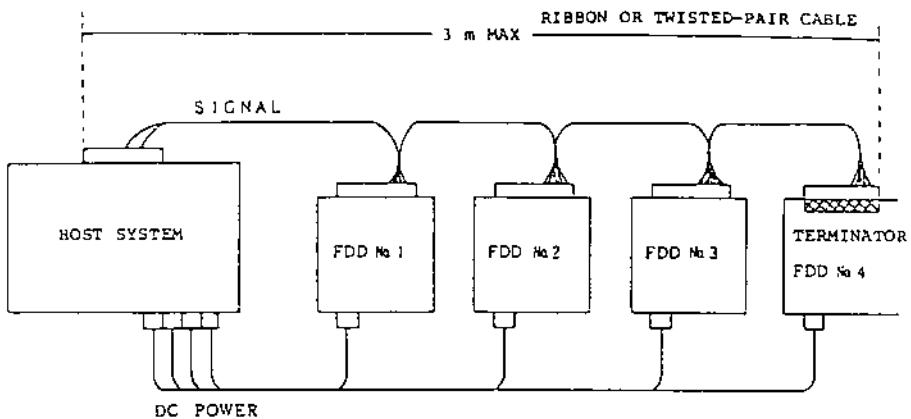


Fig. 3-1 Cabling Method (Sketch)

### 3.1.2 Line driver and line receiver

The recommended interface line driver and line receiver circuits for the host system and the drives are shown in Fig. 3-2.

It is suggested that a Schmitt trigger circuit with a hysteresis characteristic at the switching level be used for the line receiver to improve the noise resistance of the interface lines.

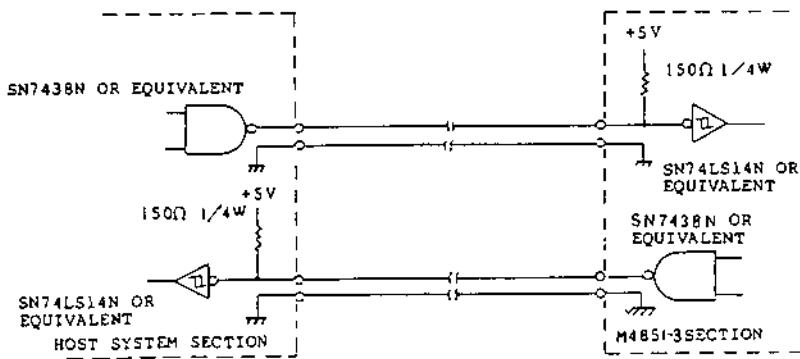


Fig. 3-2 Recommended Line Driver and Line Receiver Circuits

### 3.1.3 Short Plug

The short plug sets the conditions for selecting the drive, loading or unloading the head, starting the spindle motor, separating the in-use lines, and sending the ready signal.

The following is the explanation of features of the short plug.

- 1) Drive selection conditions DS<sub>0</sub> - 3, MX (location A<sup>6</sup> of PCB)

#### 1.1) DS<sub>0</sub> - 3

If multiple connection is made with the system and the drive, by short-circuiting one of the DS<sub>0</sub> - 3, the corresponding DRIVE SELECT line will select the drive with the logical "0" only, and input signals can be received.

For example, the drive that has had its DS<sub>0</sub> - 3 short-circuited, will be selected when DRIVE SELECT 0 line is at logical "0".

#### 1.2) MX

When all of DS<sub>0</sub> - 3 has been opened and MX is short-circuited, the drive will always be selected regardless of the DRIVE SELECT line of the interface. However, in this case the control of the panel indicator LED can only be done with the IN USE signal. Furthermore, the power of the spindle motor, and the head code cannot be controlled by DRIVE SELECT 0 -3. Therefore it is necessary to revise the conditions to another.

DS<sub>1</sub> is short-circuited at the factory before delivery. Resetting is necessary in order to use another drive number.

2) Head loading conditions selections HS, HM, HC, HL,HH  
(location J1 of PCB)

2.1) HS

In the case HS is short-circuited, the head will be loaded by DRIVE SELECT 0 - 3.

2.2) HM

In the case HM is short-circuited, the head will be loaded by the MOTOR ON signal.

2.3) HC

In the case HC is short-circuited, the head will always be loaded regardless of the interface input signal.

2.4) HL

In the case HL is short-circuited, the IN USE input signal (pin 4 of connectir J1/p1) of the head will be loaded at logical "0".

The logical product for all of the conditions for the above is taken by the HOLD READY conditions listed later on and the head code will be controlled.

HS is short-circuited at the factory before delivery.

3) Spindle MOTOR ON conditions selection MM, MS (location H1 of PCB)

The conditions for Spindle MOTOR ON conditions are selected by the combination of opening and short-circuiting of MM and MS.

Short plug		Refer to	Notes
MS	MM		
open	short	3.1	Before delivery
short	open	3.2	
open	open	3.3	
short	short	Not used	

- 3.1) Power of the spindle motor is controlled by the MOTOR ON signal.
- 3.2) Power of the spindle motor is controlled by the drive select conditions that have been selected by DRIVE SELECT 0 - 3 signal.
- 3.3) Power of the spindle motor is controlled by the logic sum of the of DRIVE SELECT 0 - 3 signals and MOTOR ON signal.

4) Ready transmission selection conditions DC, 2S

(location H1 of PCB)

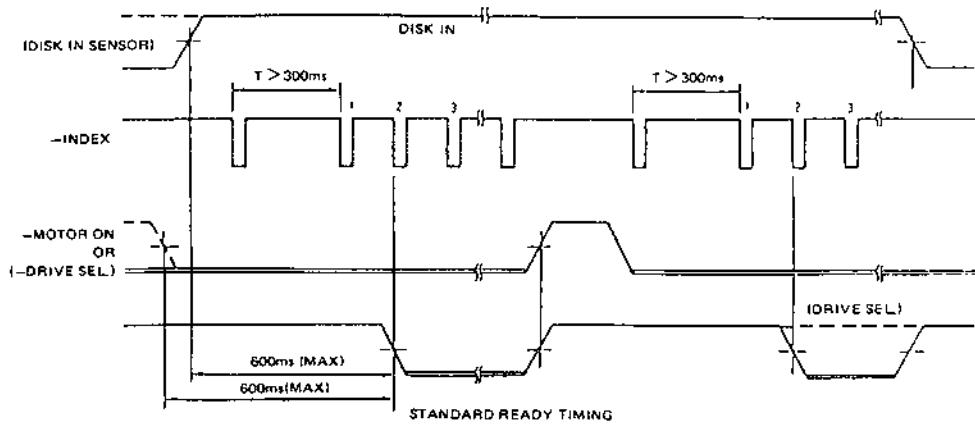
The ready transmission conditions below can be selected with the combination of opening and short-circuiting of DC and 2S.

Short plug		Refer to	Notes
DC	2S		
open	open	4.1	
open	short	4.2	
short	short	Not used	
short	open	4.3	Before delivery

4.1) Standard READY

With the standard READY signal, after detection for a disk rotation period of less than 300 ms, the INDEX signal is detected by two pulses and a READY signal is sent to the interface. A maximum of 600 ms is required for the output of the READY signal.

The READY signal interrupts disk rotation and renders it NOT READY for all conditions.



4.2) Hold ready

Indicates that diskette is inserted. This ready is set within 600 ms from when the disk is inserted. When the disk is ejected, reset starts. In order to perform read/write, since ready will be held even if the spindle motor is turned off, a minimum of 250 ms should be allowed to pass after the spindle MOTOR ON signal (DRIVE SELECT signal in the case when spindle MOTOR ON is done with DRIVE SELECT 0 - 3) is sent.

4.3) Diskette change

This signal become active or logic low (logical "0") when the drive door has been disturbed (opened) and reset to the inactive state when the door is closed and a step pulse has been received by the drive.

5) In-use Line Separation IU (PCB location H1)

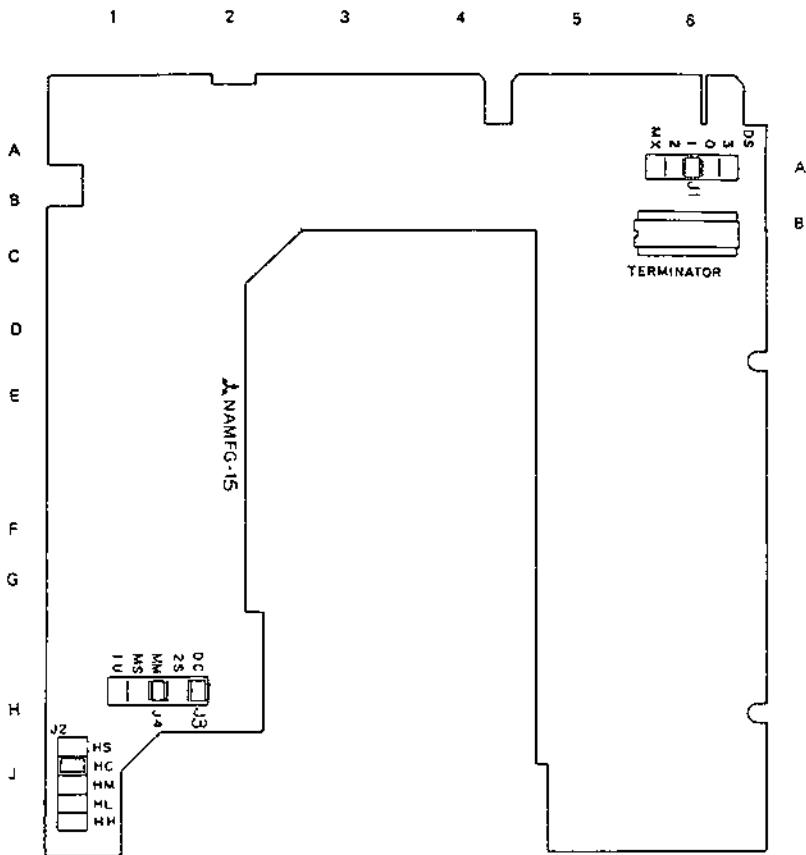
Normally, the panel indicator LED (IN USE LED) will light up according to the logical sum of DRIVE SELECT 0 - 3 and IN USE. However, when IU is set to OPEN, the control of the IN USE line will be disconnected, and only the DRIVE SELECT 0 - 3 will be effective.

Table of Shorting Plugs

Type of switching	Object	Name	Contents	Display	Name of short plug
Shorting by plugs	Selection of drive select	[DS0]	DRIVE SELECT 0		J2
		[DS1]	DRIVE SELECT 1		
		[DS2]	DRIVE SELECT 2		
		[DS3]	DRIVE SELECT 3		
		MX	The DRIVE SELECT which is usually set		
	Selection of head loading conditions	[HS]	Head loading by DRIVE SELECT		J2
		[HM]	Head loading by MOTOR ON signal		
		[HC]	Normal head loading		
		[HL]	Head loading by IN USE		
		HH	(Not used)		
	Selection of MOTOR ON conditions	[MM] [MS]	Motor started by DRIVE SELECT		J4
		[MM] MS	Motor started by MOTOR ON		
		MM MS	Motor started by MOTOR ON or DRIVE SELECT		
		[MM] [MS]	(Not used)		
	Selection of READY transmission conditions	DC 2S	Standard ready		J3
		DC 2S	Hold ready		
		DC 2S	Diskette change		
		DC 2S	(Not used)		
	Separate IN USE	IU	Separate the IN USE signal from the IN USE LED Condition. IN USE LED is activated by only DRIVE SELECT signal.		—

Note 1: The enclosed setting options are factory set at time of shipping.

Customer Installation Options



Printed-Circuit Board Trace Location

### 3.1.4 Input signal lines

The disk drive has 11 input signal lines. Input signals can be classified into two types: One is multiplexed in a multi-drive system; and the other performs a multiplex operation.

The multiplexing signals are as follows:

- o Drive select 0
  - o Drive select 1
  - o Drive select 2
  - o Drive select 3
- (1) Drive select 0 to drive select 3

When these drive select lines are at logical "0" level, a multiplexed I/O lines become active to enable read/write operation. These four separate input signal lines, drive select 0 to drive select 3, are provided for connecting four drives to one system and mutually multiplexing them. Jumper pins DS0, DS1, PS2, and DS3 on the printed-circuit board are used to select drives to be made active, corresponding to drive select lines.

DS1 is shorted before shipment from the factory, so this setting must be changed when establishing other select lines.

- (2) Side one select

This interface line is used to select which of the two sides of the diskette should be read or written. When this line is at logical "1," the Side 0 head is selected; or when it is at logical "0," the Side 1 head is selected. If the polarity of the side one select signal is reversed, delay read/write operation by more than 100  $\mu$ s before execution.

Upon completion of a write operation, reverse the polarity of the side one select signal after a delay of 1000  $\mu$ s. The heads are tunnel erase type, with a physical core gap deviation between the read/write head and the erase heads so with no delay, non-erased areas would be generated on the diskette due to a timing difference between the write data area and the erase area during write operation. This is prevented by delaying the erase current ON/OFF time of a 1000 microseconds within the disk drive. Therefore, the head select must not be reversed during this delay time. Also, the track access action must not be permitted for 1000 $\mu$ s.

(3) Direction select

This interface line controls the direction, (inward or outward) in which the read/write head should be moved when a step signal pulse is applied.

If the signal is at logical "1," the read/write head moves from the center of the diskette outward; if it is at logical "0," the head moves inward.

(4) Step

This interface line is a pulse signal for moving the read/write head in the direction defined by the direction select line. The read/write head moves by one track each time a signal pulse is applied to the step line. The step line is normally logical "1," and the step operation starts with the trailing edge of a negative-going pulse (reversal from logical "0" to logical "1").

The direction select line must be reversed more than 1  $\mu$ s before the trailing edge of the step pulse.

(5) Write gate

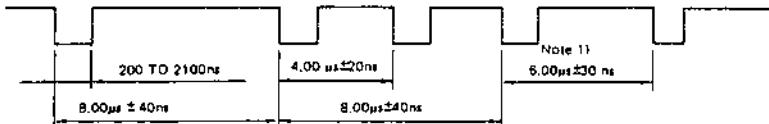
When this interface line goes to logical "0," the write driver becomes active and the data given to the write data line is written on the selected side of the diskette. When the interface line goes to logical "1," the write driver becomes inactive to enable the read data logic. The verified read data is obtained 1000  $\mu$ s (maximum) after the write driver becomes inactive. Refer to CHAPTER 4 for the timing.

(6) Write data

Data to be written on the diskette is sent to this interface line.

This line is normally at logical "1," and reverses the write current at the leading edge of a negative-going data pulse (reversal from logical "1" to logical "0") to write data bits.

This line is enabled when the write gate is at logical "0." Fig. 3-3 shows the write data timing.



Note 1) The timing for 6.00 $\mu$ s is MFM only.

Fig. 3-3 Write Data Timing (FM, MFM Encoding)

(7) In use

An LED indicator on the front panel lights when this interface line goes to logical "0." The LED is also lit by the drive select.

(8) Motor on

This interface line starts the spindle motor when it goes to logical "0." The write gate does not go to logical "0" until more than 250 ms after the motor-on line goes logical "0."

The motor-on line goes logical "1" to stop the motor and keep it off while the drive is out of operation, thus prolonging motor life.

### 3.1.5 Output signal lines

The drive has five standard output signal lines.

(1) Index

This interface line is normally logical "1" but sends a logical "0" output pulse 4 ms wide each time the diskette makes one revolution (200 ms period).

This signal signifies the start of a track on the rotating diskette. The index signal timing is shown in Fig. 3-4.



Fig. 3-4 Index Timing

(2) Track 00

When this interface line is at logical "0," it indicates that a read/write head of the selected drive is positioned on track 00. If the output of the selected drive is at logical "1," it indicates that the read/write head is positioned on a track other than track 00.

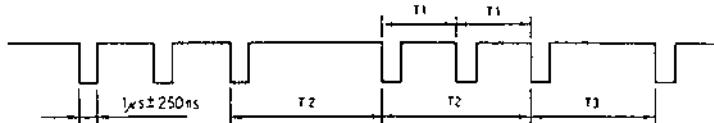
(3) Ready

This interface line is logical "1" when the door is open or no diskette is in the drive. The line goes logical "0" (ready) if an index pulse is detected twice or more when the index hole is correctly detected, and the DC power (+5 V and +12 V) supplied after a diskette is inserted into the drive and the door is closed.

(4) Read data

This interface line reads the data stored on the diskette with the read/write heads, and outputs raw data (combined clock and data signals) converted into pulse signals by an electronic circuit.

The read data line is normally logical "1" but it sends a logical "0" (negative-going) output pulse during a read operation. Fig. 3-5 shows allowable limits on timing variations with the usual diskette and bit shifts.



$T_1 = 4.00\mu s \pm 800\text{ns}$  (Jitter due to rotation variation excluded)  
 $T_2 = 8.00\mu s \pm 1.600\text{ns}$  (Jitter due to rotation variation excluded)  
 $T_3 = 6.00\mu s \pm 1.200\text{ns}$  (Jitter due to rotation variation excluded)

Fig. 3-5 Read Data Timing (FM Encoding)

(5) Write protect

This interface signal notifies the host system of the insertion of a diskette with a write protect notch into the drive. The signal goes to logical "0" when a write-protected diskette is inserted into the drive. When the signal is at logical "0," write on the diskette is inhibited even if the write gate line becomes active.

### 3.2 Power Interface

The disk drive requires two types of DC power supplies.

One is +12 V DC, which drives the drive motor to rotate the disk. It is supplied to the stepping motor and the read/write circuit. The other is +5 V DC, which is used for the logic circuit and the read/write circuit.

#### NOTE

The index LED is driven by the +12 V DC.

##### 3.2.1 DC power

DC power is supplied via connector J2/P2 on the back of the printed-circuit board. The specifications of the two DC voltages are shown in Table 3-3. The pin arrangement of connector J2/P2 is shown in Table 3-1.

Table 3-3 DC Power Specifications

DC voltage	Voltage variation (±5%)	Current	Maximum ripple voltage (peak-to-peak)
+5 V DC	±0.25 V (±5%)	0.7 A maximum 0.5 A typical	50 mV
+12 V DC	±0.6 V (±5%)	1.00 A maximum 0.5 A typical at seek	100 mV

## CHAPTER 4 FUNCTIONAL OPERATION

### 4.1 Power On Sequencing

No read/write operation may be performed during the period of 100 ms or more from the start of DC power supply until the control signal stabilizes. And after the period of 600ms from the Motor On, the drive comes to ready.

The read/write head may have been positioned on an incorrect track after switching the DC power on, so before starting a read/write operation, be sure to perform the step out operation until a track 00 signal is output to the interface line, and thus correctly position the read/write head.

Note: There is no specified power input order for + 12 V and + 5 V.

### 4.2 Drive Selection

The disk drive daisy chain cabling system permits connection of multiple drives to a single cable.

These drives are selected when the drive select lines on the drive side become active. Only the drive whose drive select line is active sends and receives signals to and from the host system. The select lines on the drive must have different numbers if two or more drives are connected. If the same number is assigned, an operation error occurs due to interference among the interface output signals of the drives themselves.

### 4.3 Positioning Operation

The seek operation which moves the read/write head to the desired track selects a direction, inward or outward, depending on the polarity of the direction select signal, and moves the head by the step signal. If access to a track two or more tracks away is required, step pulses are continuously sent until the head moves to the desired track.

Head movement starts with the trailing edge of the step pulse. Fig. 4-1 Shows the operation timing.

### 4.4 Side One Selection

The read/write heads located on both sides of the diskette are selected by the side one select signal. When the side one select line is high, the Side 0 head is selected. When it is low, the Side 1 head is selected.

#### 4.5 Read Operation

The required timing for read operations is shown in Figs. 4-1 and 3-5. These timing specifications are necessary for accurate read operation.

Two modes of encoding, FM and MFM, are used for the data stored on media. FM is used for single-density read, and MFM for double-density read.

A comparison of the FM and MFM encoding modes is shown in Fig. 4-3.

#### 4.6 Write Operation

The requiring timing for write operation is shown in Fig. 3-3.

These timing specifications must be strictly observed to ensure an accurate write operation.

Write data can be encoded by either FM or MFM. The disk drive has good contact stability of the read/write heads on the medium and employs high-performance read/write heads, so no precompensation is necessary for correcting the peak shift effect when writing data in the MFM mode (double density).

#### 4.7) READY and operation of the dynamic lamp

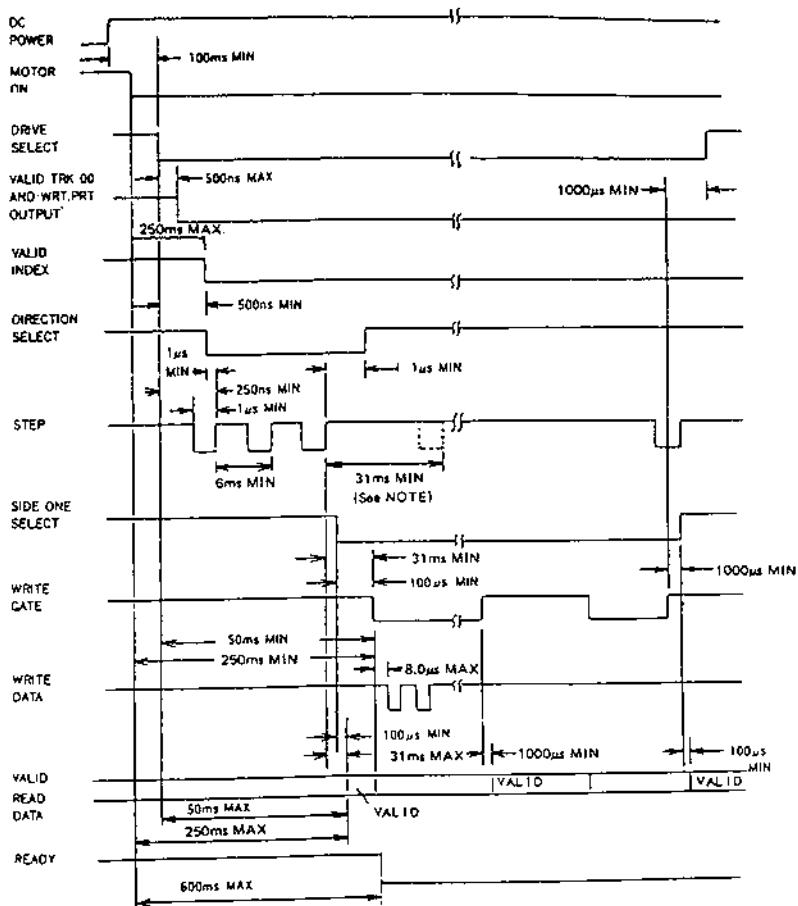
The timing of the dynamic lamp, standard READY, and standard READY is shown in Diagram 4.2.

##### Dynamic lamp function

When the disk is inserted into the unit, the two needed.

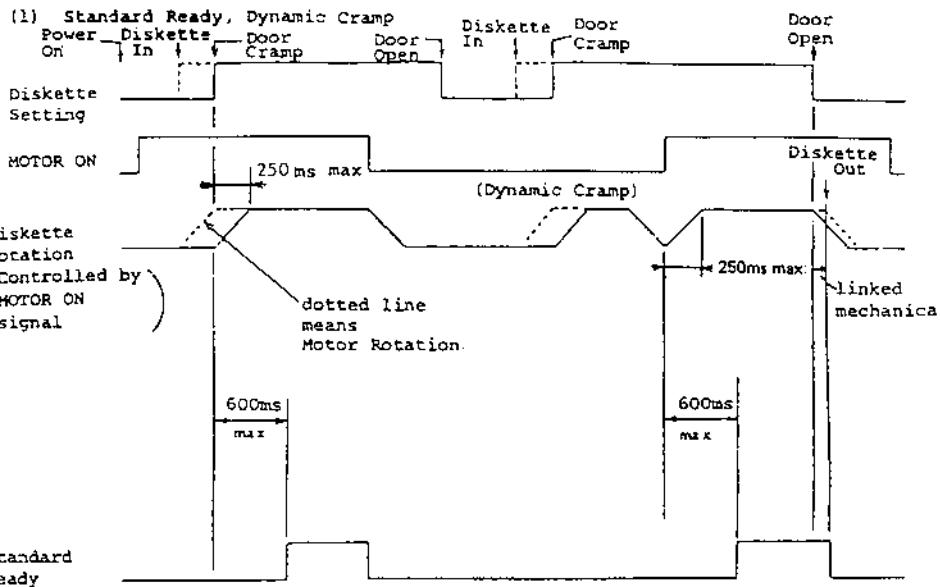
When the disk is inserted into the unit, the two steps of first inserting and then closing the door are needed.

The micro switch detects the insertion of the disk and starts forced rotation of the spindle motor. After the door is closed detection continues for the period of the index pulse, approximately 300 ms, after which forced rotation is released.



Note : When reversing direction, issue a next step pulse after more than 31ms from the step pulse before inversion.

Fig. 4-1 Control and Data Timing



(2) Hold Ready, Dynamic Clamp

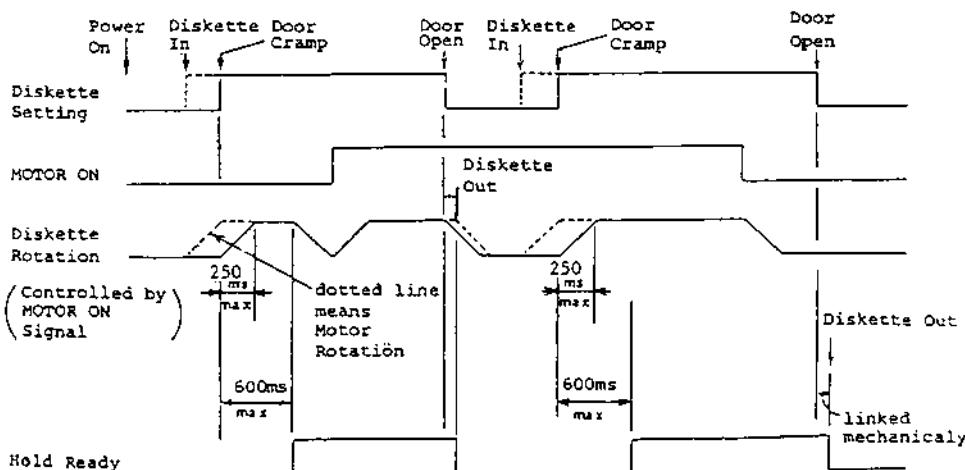


Fig. 4-2 Ready and Dynamic Clamp Timing

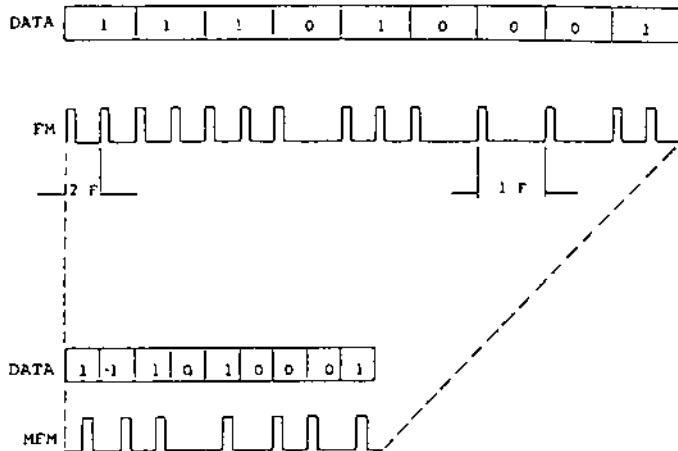


Fig. 4-3 Comparison of FM and MFM Encoding Systems

## CHAPTER 5 PHYSICAL INTERFACE

Electronic interfaces between the disk drive and the host system are accomplished with three connectors. Connector J1 is for the signal interfaces, connector J2 for the DC power supplies, and connector JS for frame grounding. The connectors used for the disk drive and recommended mating connectors are described below.

### 5.1 Signal Connectors

J1 is a card-edge type, 34-pin (for both sides, or 17 pins for a single side) connector with even-numbered pins (2, 4, to 34) on the parts side and odd-numbered pins (1, 3, to 33) on the soldered side.

A key slot is provided between pins 4 and 6 for the polarity reversal prevention.

The dimensions of J1 are shown in Fig. 5-1.

Recommended Pl connectors that mate with J1 are shown in Tables 5-1 and 5-2.

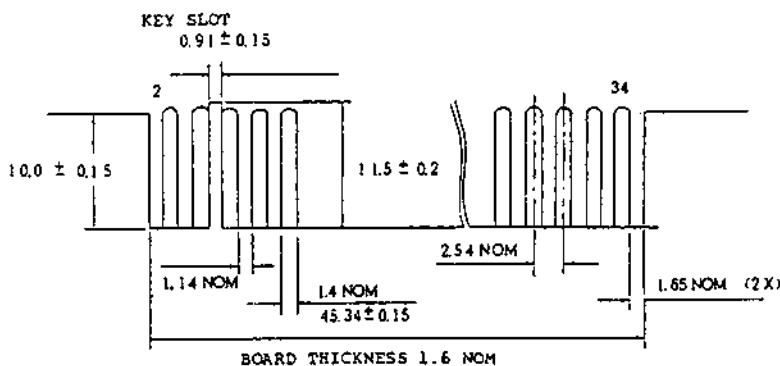


Fig. 5-1 Connector J1 Dimensions (mm) and Pin Numbers

Table 5-1 Connectors for Twisted-Pair Cable (Pl)

Parts	Crimp Type	Solder Type
	AMP P/N	AMP P/N
Housing	583717-5	583717-5
Contact	1-583616-1	583854-3
Polarity key	583274-1	583274-1
Crimping tool	90268-1	-
Extraction tool	91073-1	91073-1
Twisted-pair cable (3 m max.)	AWG 26	AWG 26

Table 5-2 Connector for Flat Cable (Pl)

Parts	3M P/N
Connector	3463-0001
Polarity key	3439-0000
Crimping tools	Press
	Locator plate
	Platen
Flat cable (3 m max.)	3365/34

Items that can be used in conjunction with a connector for the flat cable.

Parts	HIROSE P/N
Connector	HIF5D-34DA-2.54R
Polarity key	CR7C-GPIN

(Items such as a fusing tool. For details refer to the manufacturers of the connector.)

### 5.2 DC Power Connector (J2/P2)

P2 is a four-pin DC power connector made by AMP, located on the back of the printed-circuit board. Pin 4 on connector P2 is located closest to J1/P1; the arrangement of the pins as viewed from the side is shown in Fig. 5-2.

The connectors on the drive side and cable side are shown in Table 5-3.

Table 5-3 DC Power Connectors

Parts	J2 (Cable Side)	P2 (Drive Side)
	AMP P/N	AMP P/N
Housing	1-480424-0	172349-1
Contact (4 pins)	60619-1	-
Crimp tool	90124-2	-
Extraction tool	1-305183-2	-
Cable (3 m max.)	AWG 18	-

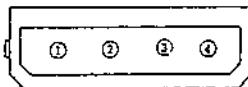


Fig. 5-2 Connector P2

### 5.3 Frame Ground Connector (J5/P5)

FASTON Terminal	Crimp Terminal
AMP P/N 60920-1	AMP P/N 60972-1

#### 5.4 Interface Connector Physical Location

Fig. 5-3 shows the physical locations of the interface connectors.

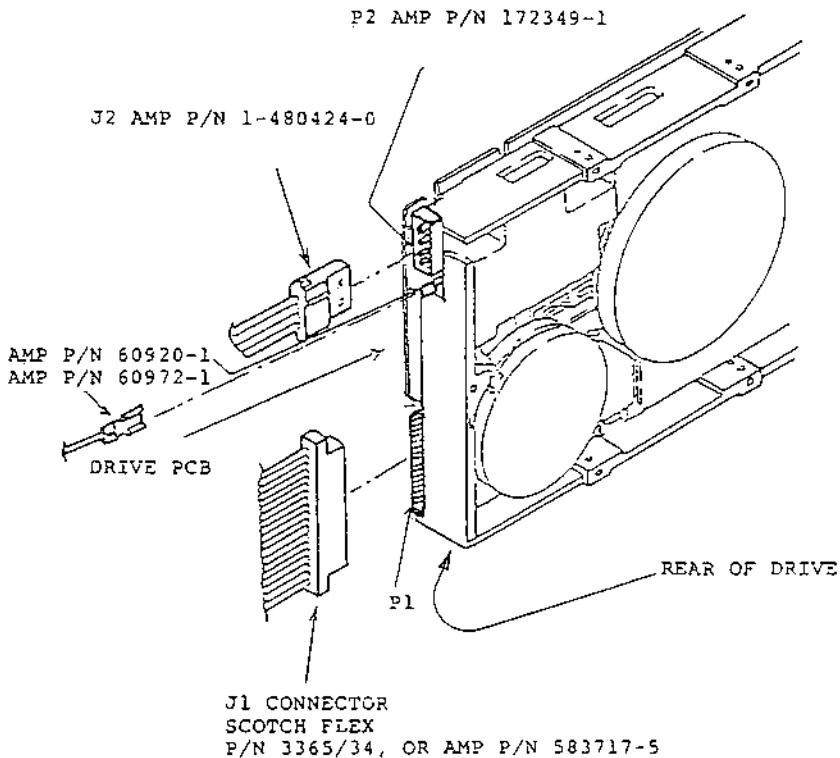


Fig. 5-3 Location of Interface Connectors

## CHAPTER 6 DRIVE PHYSICAL SPECIFICATIONS

### 6.1 Installation Direction

Install the Mini Flexible disk drive in the directions shown in Fig. 6-1.

The slant mount should be within 10 degrees.

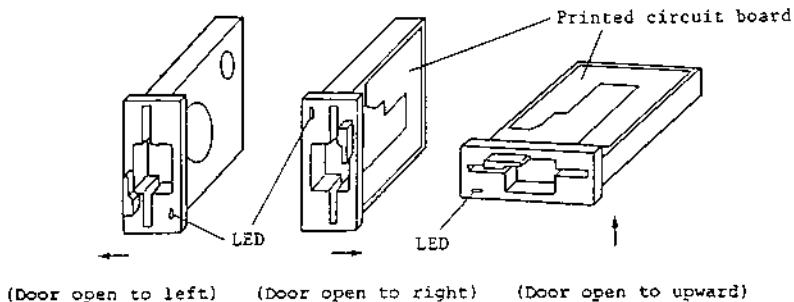


Fig. 6-1 Disk Drive Installation Directions

### 6.2 Dimensions of disk drive

See Fig. 6-2.

### 6.3 Dimensions of Front Panel

See Fig. 6-3.

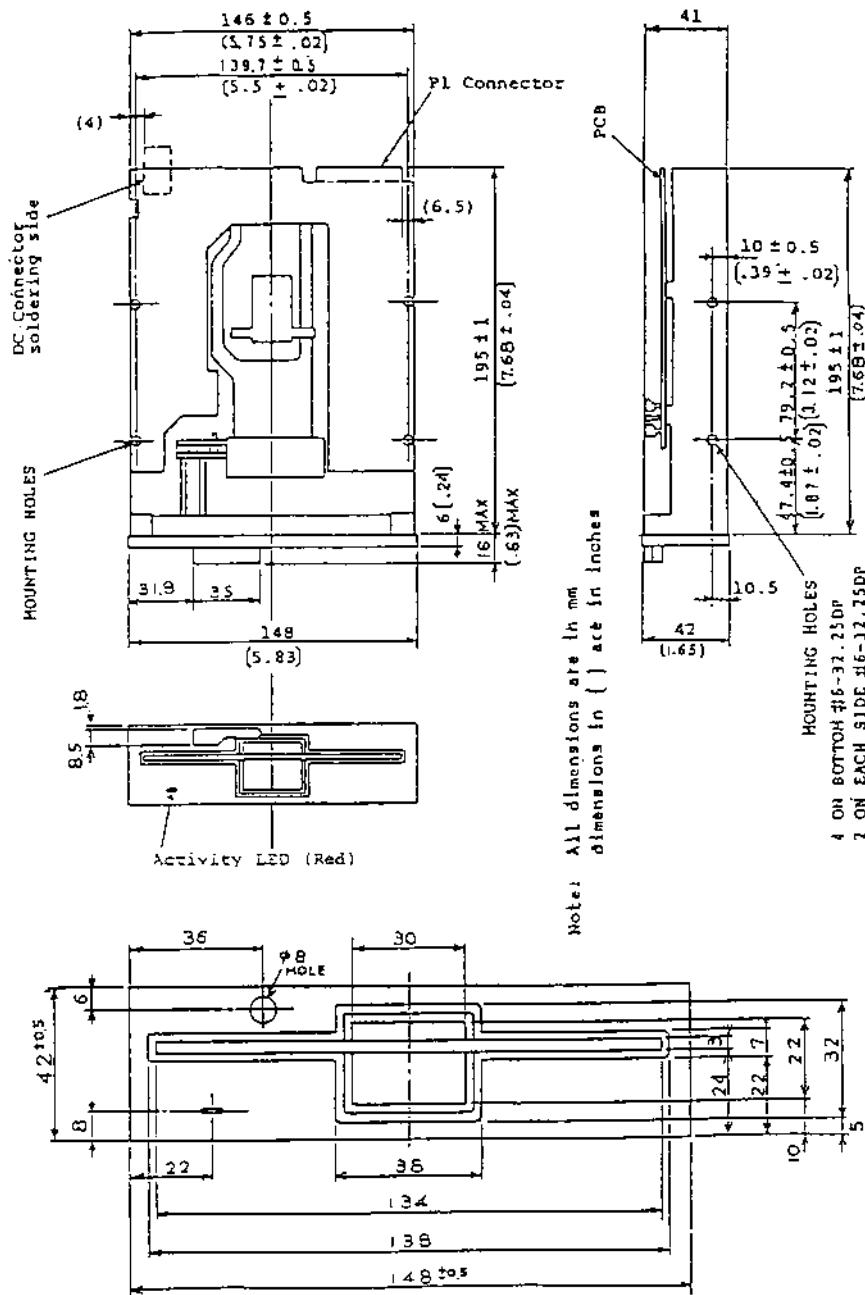


Fig. 6-3 Front Panel Dimensions

## CHAPTER 7 ERROR DETECTION AND CORRECTION

This chapter describes the general cause analysis and corrective procedures to be followed in the event that data errors occur.

### 7.1 Write Errors

If an error occurs during a write operation, it can be detected by performing a read operation on the diskette immediately following the write operation. This is generally called a write check, which is an effective means of preventing write errors. It is recommended, therefore, that a write check be made without fail.

If a write error occurs, repeat the write operation and conduct a write check. If data cannot be correctly written even after the write operation is repeated about ten times, perform a read operation on another track to determine whether the data can be read correctly. If so, a specific track of the diskette is defective. If data cannot be correctly read on the other track, the drive is assumed to have some trouble. If the diskette is defective, replace it.

### 7.2 Read Errors

Most data errors that occur are soft errors. If a read error occurs, repeat the read operation to recover the data.

The following are possible main causes of soft errors:

- o Dust is caught between the read/write head and diskette causing a temporary fault in head contact. Such dust is generally removed by the self-cleaning wiper of the jacket, and the data is recovered by the next re-read operation. If read/write operations is continued for a long time in a very dusty environment, however, hard errors can result from a damaged diskette surface.

- o Random electrical noise ranging in time from a few microseconds to a few milliseconds can also cause read errors. Spurious noise generated by a switching regulator, particularly one that has short switching intervals, deteriorates the signal-to-noise ratio, and increases the number of re-read operations for data recovery. It is necessary, therefore, to make an adequate check on the noise levels of the DC power supplies to the drive and frame grounding.
- o Written data or diskettes may have so small a defect as cannot be detected by a data check during write operation.
- o Fingerprints or other foreign matter on a written diskette can also cause a temporary error. If foreign matter is left on a written diskette for a long time, it can adhere to the diskette, possibly causing a hard error.

It is recommended that the following read operations be performed to correct these soft errors:

- o Step 1: Repeat the read operation about ten times until the data is recovered.
- o Step 2: If the data cannot be recovered by Step 1, move the head to other track, the opposite direction of the previous track position before the designated track, and then return the head to the original position.
- o Step 3: Repeat an operation similar to Step 1.
- o Step 4: If the data cannot be recovered, take the error as a hard error.

## CHAPTER 8 RESHIPMENT PRECAUTIONS

When reshipping the drive, make sure the protection sheet for transportation is in place in the drive, and open the door.



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\*  
\* 360 K Disk Drive  
\*  
\* Section 5  
\*  
\* Parts list  
\*  
\*\*\*\*\*

November 15, 1985



TANDY 3000 LOW DENSITY DRIVE

Symbol	Description	Part No.
	Drive w/ PCB	AXX-5105
	Carriage Assy.	ART-0179
	Frame	
	Solenoid HLMG	AS-9098
	TK00 Sensor Assy	ACS-0016
	Spindle Motor Assy	AM-4015
	Spindle Motor Assy (Alternate)	AM-4022
	Stepping Motor	AM-4023
	Idler, Sub Assy	ARA-0039
	Holder, Idler C	ART-0133
	Band, A	AHC-0177
	Spring, Coil, C	ARB-6224
	Holder, Band A	ART-0180
	Holder, Band B	ART-0136
	Guide Rod	AHC-0159
	Spring, Coil	ARB-6226
	Terminal	
	Washer Plain	
	Screw, Pan HD, Washered	AHD-2888
	Screw, Pan HD	AHD-2886
	Screw, Pan HD, Washered	AHD-2896
	Clamp, for Band A	AHC-0160
	Screw, Bind	
	Stopper Capstan	AHC-0158
	Bolt, Socket (Micro-size)	AHD-2886
	Bridge A Assy	ART-0181
	Collet Assy	ART-0139
	Spring, Leaf	ARB-6227
	Ring, E	
	Screw, Pan HD, Washered	AHD-2885
	Ejector Assy	ART-0140
	Front Panel Assy	AZ-0074
	Chassis Front Assy	AZ-0075
	Lever Assy	ART-0182
	PCB, NAMGF-1	

**Carriage Assy**  
**(Non-repairable)**

Symbol	Description	Part No.
	Carriage	
	Arm	
	Sub Frame	
	Stay Spring	
	Head Gimbal, S0	
	Alternate	
	Alternate	
	Head Gimbal, S1	
	Alternate	
	Alternate	
	Shield Plate	
	Spring, Coil	
	Head Cable Assy	
	Spring, CR Assy	
	Rubber	
	Rubber	
	Holder, Arm	
	Holder, Band C	
	Screw, Pan HD, Washered	
	Bolt, Socket (Micro-size)	
	Screw, Tap-Tight	
	Spacer	
	Cover, Head S0	
	Cover, Head S1	
	Washer	

**Spindle Motor Assy**

Symbol	Description	Part No.
	IC, Digital	MX-6360
	IC, Linear	MX-6361
	Capacitor, Rutilcon +20%, 25V, 1000pF	CC102MF
	Capacitor, Aluminum +20%, 50V, 1uF	CC105MJAP
	Capacitor, Polypropylen +5%, 1000V, 0.056uF	CC563JXHP
	Capacitor, Polyester +10%, 50V, 0.047uF	CC473KJGP
	Capacitor, Non-Polar +20%, 50V, 0.15uF	CC154MJBP
	Capacitor, Aluminum +20%, 50V, 0.47uF	CC474MJAP
	Capacitor, Non-Polar +20%, 50V, 2.2uF	CC225MJBP
	Capacitor, Aluminum +20%, 16V, 33uF	CC336MDAP
	Diode, Silicon	DX-0322
	LED	AL-1005

Symbol	Description	Part No.
	Resistor, Variable +20% 0.2W 30K Ohm	AP-7010
	Resistor, Carbon +1% 1/4W 47K Ohm	N0340BEC
	Resistor, Film Metal +3% 1/4W 100K Ohm	N0371DEE
	Resistor, Carbon +5% 1/4W 2.2K Ohm	N0216EEC
	Resistor, Carbon +5% 1/4W 33K Ohm	N0324EEC
	Resistor, Carbon +5% 1/4W 47K Ohm	N0340EEC
	Resistor, Carbon +5% 1/4W 24K Ohm	N0526EEC
	Resistor, Carbon +5% 1/4W 5.1K Ohm	N0252EEC
	Resistor, Carbon +5% 1/4W 56K Ohm	N0345EEC
	Resistor, Carbon +5% 1/4W 330 Ohm	N0159EEC
	Resistor, Carbon +5% 1/4W 13K Ohm	N0289EEC
	Resistor, Carbon +5% 1/2W 1.8K Ohm	N0210EFC
	Resistor, Carbon +5% 1/2W 470 Ohm	N0169EFC
	Resistor, Metal Oxide +5% 1/2W 510 Ohm	N0173EFD
	Resistor, Carbon +5% 1/4W 47 Ohm	N0099EEC
	Resistor, Metal Oxide +5% 1W 0.75 Ohm	N0637EGD

Spindle Motor Assy  
(Alternate)

Symbol	Description	Part No.
	IC, CX10040	MX-5241
	Capacitor, Elect +20%, 16V, 22uF	CC226MDAP
	Capacitor, Elect +20%, 50V, 1uF	CC105MJAP
	Capacitor, Elect +20%, 25V, 4.7uF	CC475MFAP
	Capacitor, Ceramic +20%, 50V, 1000uF	CC102MJCP
	Capacitor, Ceramic +30%, 12V, 0.033uF	CC333NCCP
	Capacitor, Ceramic +30%, 16V, 0.022uF	CC223NDCP
	Capacitor, Polypropylene +5%, 100V, 0.047uF	CC473JLHP
	Resister, Variable +20% 100V 50K Ohm	ARX-0047
	Resister, Carbon +5% 1/4W 3.3K Ohm	N0230EEC
	Resister, Carbon +5% 1/4W 680K Ohm	N0433EEC
	Resister, Carbon +5% 1/4W 4.7K Ohm	N0247EEC
	Resister, Carbon +5% 1/4W 47K Ohm	N0340EEC
	Resister, Carbon +5% 1/4W 1.2K Ohm	N0199EEC
	Resister, Carbon +5% 1/4W 39K Ohm	N0330EEC
	Resister, Carbon +5% 1/4W 330 Ohm	N0159EEC
	Resister, Carbon +5% 1/4W 100 Ohm	N0132EEC
	Resister, Carbon +5% 1/4W 1.8K Ohm	N0210EEC
	Resister, Metal +5% 2W 3.6K Ohm	N0235EMD
	Resister, Metal +5% 1W 470 Ohm	N0169EGD
	Resister, Met. Ox. +5% 1W 440 Ohm	N0819EED
	LED, Red	L-1939

**Bridge Assy**  
**(Non-repairable)**

Symbol	Description	Part No.
	Stopper, Ejector	
	Spacer A, Cartridge Guide	
	Cushion Mold	
	Cartridge Guide A	
	Spring, Cartridge Guide	
	Screw, Pan Hd., Washered	

**Collet Assy**  
**(Non-repairable)**

Symbol	Description	Part No.
	Collet A	
	Collet B	
	Spring, Coil, B	
	Shaft	
	Bearing	
	Ring, E	
	Washer, Metal	

**Ejector Assy**  
(Non-repairable)

Symbol	Description	Part No.
	Holder, Ejector A	
	Ejector	
	Shaft, Ejector	
	Spring, Coil	
	Switch (Micro-size)	
	Screw, Pan Hd., Washered	

**Front Panel Assy**  
(Non-repairable)

Symbol	Description	Part No.
	Front Panel Indicator	

**Chassis Front Assy**  
(Non-repairable)

Symbol	Description	Part No.
	Chassis Front	
	Washer	
	Ring, E	
	Washer	
	Washer	
	Ring, E	
	Holder	
	Spring, W	
	Holder	
	Shaft A	
	Link B	
	Pin A	
	Ring	
	Shaft	
	Link A	
	Pin B	

**Lever Assy**  
(Non-repairable)

Symbol	Description	Part No.
	Lever	
	Lever Holder	

## PCB, NAMFG-1

Symbol	Description	Part No.
PWB, NAMFG-1		
	Connector, male 3 pins	AJ-1072
	Connector, male 4 pins	AJ-7585
	Ornament, Conn. Clamp	AJ-7586
	Connector, male 14 pins	AJ-1073
	Connector, male 10 pins	AJ-1074
	Connector, female 2 pins	AJ-7588
	Connector, male 4 pins	AJ-1075
	Connector, male 10 pins	AJ-1076
	Connector, male 2 pins	AJ-7592
	Connector, male 3 pins	AJ-7584
	Index Sensor U Assy	ACS-0021
	Alternate	
	Write Protect Sensor	ACS-0017
	Holder, WPS	ART-0141
	Bolt, Socket (FE)	AHD-5001
	Socket, IC	AJ-1057
	IC, Digital (D6)	MX-6364
	IC, Digital (G1)	MX-5264
	IC, Linear (A4-1, A4-2)	MX-6365
	IC, Linear (G6)	MX-6892
	IC, Linear (E1)	MX-6844
	IC, Digital (G1) (Alternate)	MX-5265
	IC, Linear (G6) (Alternate)	MX-5266
	IC, Digital (E5)	MX-6890
	IC, Digital (E6)	AMX-3716
	Capacitor, Ceramic ±10% 50V 0.01uF	CC103KJCP
	Capacitor, Ceramic -20%+8% 25V 1.5uF	CC155ZFCP
	Capacitor, Ceramic ±5% 50V 0.022uF	CC223JJCP
	Capacitor, Ceramic ±5% 50V 150pF	CF-2300
	Capacitor, Ceramic ±5% 50V 220pF	CF-2072
	Capacitor, Ceramic ±5% 50V 470pF	CF-1163

Symbol	Description	Part No.
	Capacitor, Ceramic +5% 50V 1000pF	CF-2222
	Capacitor, Ceramic +10% 50V 4700pF	CC475KJCP
	Capacitor, Ceramic +10% 50V 0.1uF	CC104KJCP
	Capacitor, Ceramic +20% 16V 100uF	CC107MDCP
	Resistor, Carbon +5% 1/6W 10K Ohm	N0281ECC
	Resistor, Carbon +5% 1/6W 3.3K Ohm	N0230ECC
	Resistor, Carbon +5% 1/6W 4.7K Ohm	N0247ECC
	Resistor, Carbon +5% 1/6W 1M Ohm	N0445ECC
	Resistor, Metal +2% 1/4W 470 Ohm	N0169CED
	Resistor, Metal +2% 1/4W 47K Ohm	N0340CED
	Resistor, Carbon +5% 1/6W 47 Ohm	N0099ECC
	Resistor, Carbon +5% 1/6W 1.8K Ohm	N0210ECC
	Resistor, Metal +5% 1/6W 150K Ohm	N0384ECD
	Resistor, Carbon +5% 1/6W 100K Ohm	N0371ECC
	Resistor, Carbon +5% 1/6W 56K Ohm	N0345ECC
	Resistor, Carbon +5% 1/6W 100 Ohm	N0132ECC
	Resistor, Carbon +5% 1/6W 10K Ohm	N0281ECC
	Resistor, Metal +2% 1/4W 8.2K Ohm	N0271CED
	Resistor, Carbon +5% 1/6W 1.5K Ohm	N0206ECC
	Resistor, Metal +2% 1/4W 6.8K Ohm	N0262CED
	Resistor, Carbon +5% 1/6W 82K Ohm	N0360ECC
	Pot 50K Ohm Volume +20% 100V	P-7867
	Resistor, Carbon +5% 1/6W 47K Ohm	N0340ECC
	Resistor, Carbon +5% 1/2W 470 Ohm	N0169EFC

Symbol	Description	Part No.
	Resistor, Metal +1% 1/4W 1.5K Ohm	N0206BED
	Resistor, Carbon ±5% 1/6W 150 Ohm	N0142ECC
	Resistor, Carbon ±5% 1/2W 560 Ohm	N0107EFC
	Resistor, Metal 150 Ohm x 8 ±5% 125mw	ARX-0040
	Resistor, Metal 4.7K Ohm x 6 ±5% 125mw	ARX-0041
	Resistor, Carbon ±5% 1/6W 1.2K Ohm	N0199ECC
	Diode, 1S-953	DX-0762
	Diode, 1SR35-100A-T-81	DX-0583
	OSC, Ceramic, 400KHZ ±0.5% 50KV	ACA-9001
	Inductor 680uH ±5%	ACA-9002
	Inductor 100uH ±10%	ACA-9003
	Transistor, 2SA952	2SA-952
	Cover, HD Cabel B	
	Holder, HD Cable	



\*\*\*\*\*  
\*  
\*       360 K. Floppy Disk Drive       \*  
\*  
\*              Section 6                  \*  
\*  
\*              Jumper Settings         \*  
\*  
\*\*\*\*\*



### **360 K. Disk Drive Servo/Logic Board Jumper Settings**

If the drive is a Model MF501A-347UA be sure that MM and DS1 are jumpered and that SR, HS, HM, HL, DS3, DS2 and MX on the drive servo/logic board are not jumpered.

**Note:** On some later versions of this drive's servo/logic board the pins for jumpering MM will have been removed and a connection on the PCB will have been substituted for the jumper.



\*\*\*\*\*  
\*  
\* 360 K. Floppy Disk Drive \*  
\*  
\* Section 7 \*  
\*  
\* Schematics and Component Layout \*  
\*  
\*\*\*\*\*



**DISK DRIVE  
SCHÉMATICS AND  
LOGIC MANUAL**

**MF501A-301U**

**MF501A-301M**

**MF501A-301UE**

**MF501A-308U**

**MF501A-348U**

**Sheet Title**

**MF501A-3 DISK DRIVE WIRING DIAGRAM**

**MF501A-3 PCB NAMFK SCHEMATIC**

**MF501A-3 PCB NAMFK PARTS LOCATION DIAGRAM**

**MF501A-3 SPINDLE MOTOR ASSY SCHEMATIC**

**(NAME : F2SMR01 or TS340N4E13)**

**Page**

**Revision**

**2/4**

**A**

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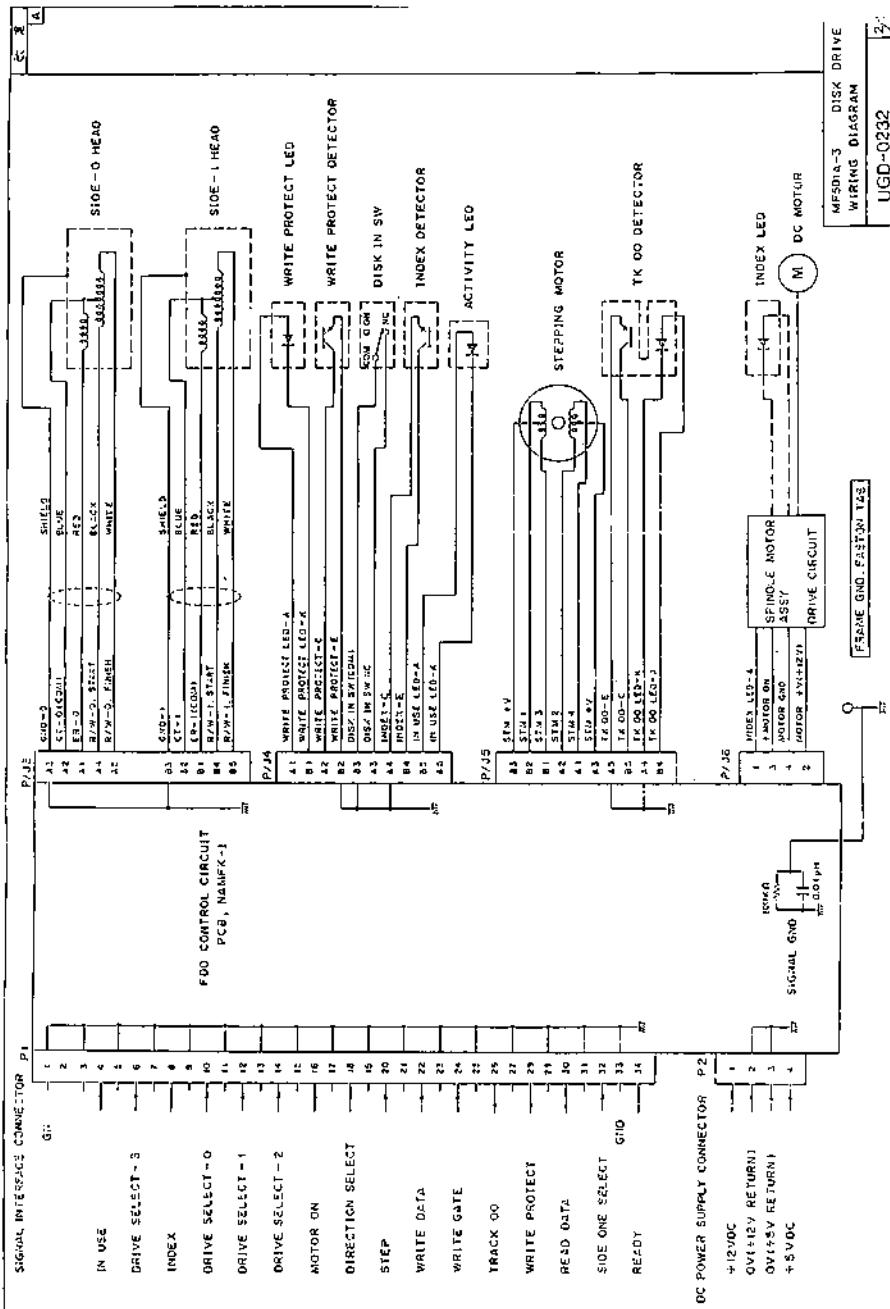
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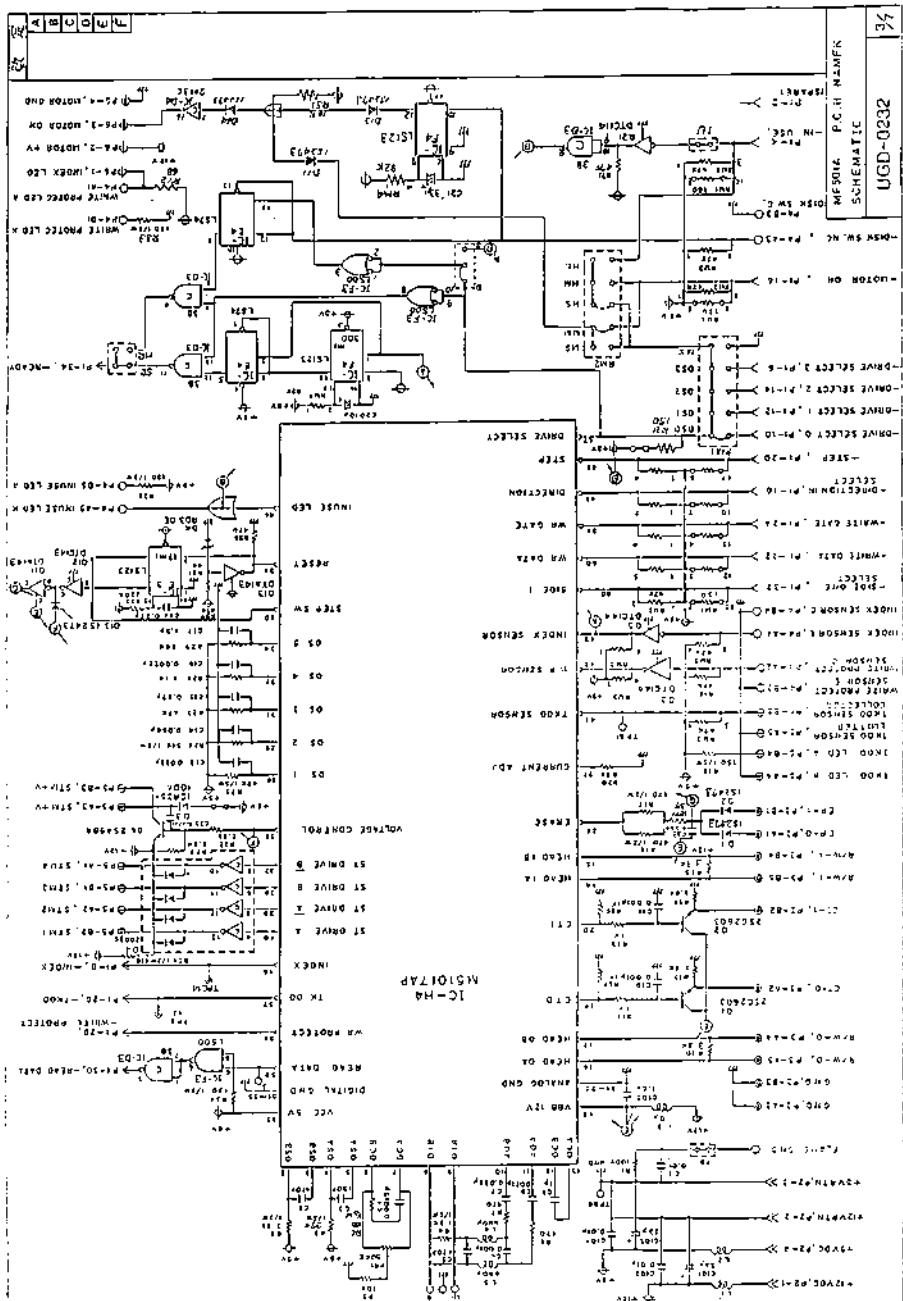
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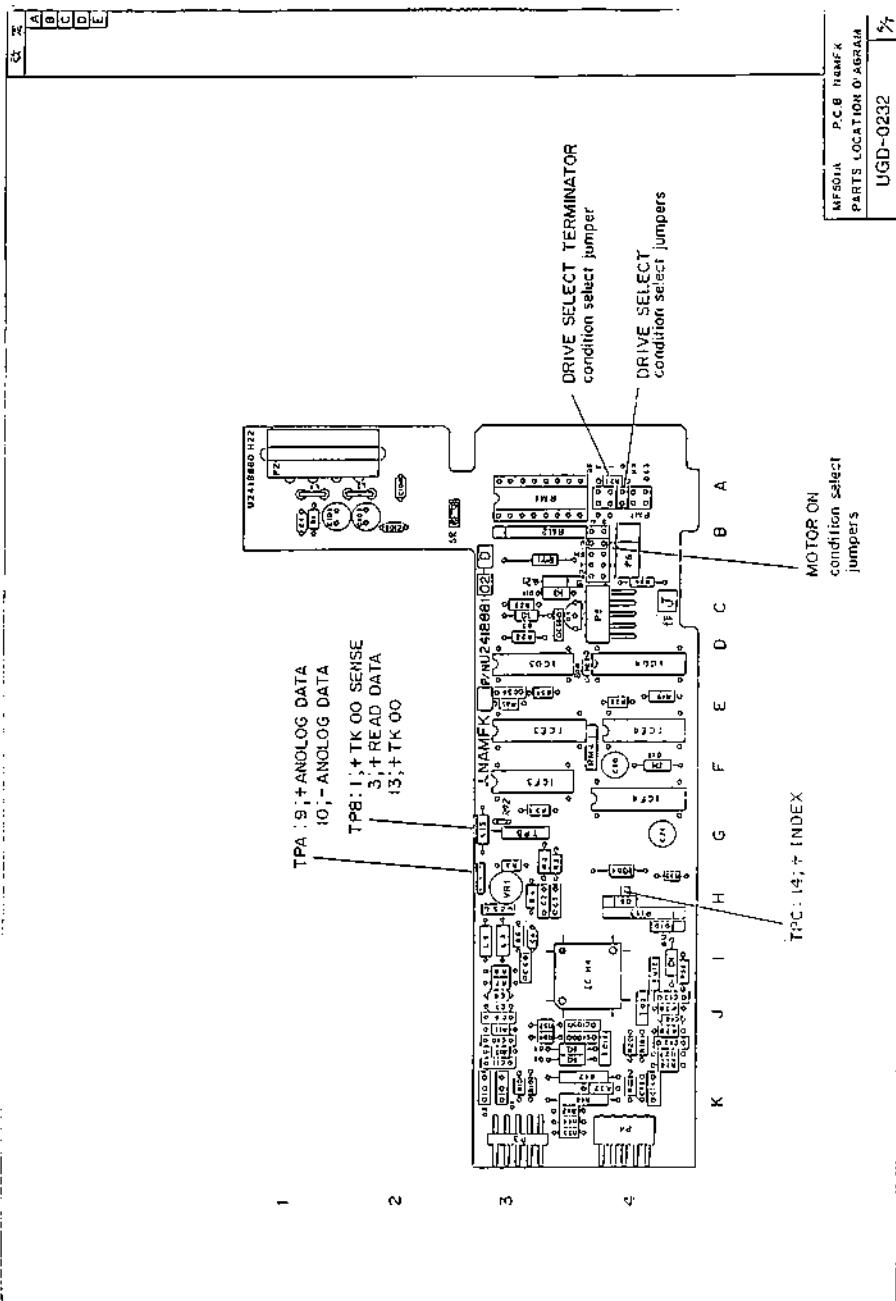
**E,A**

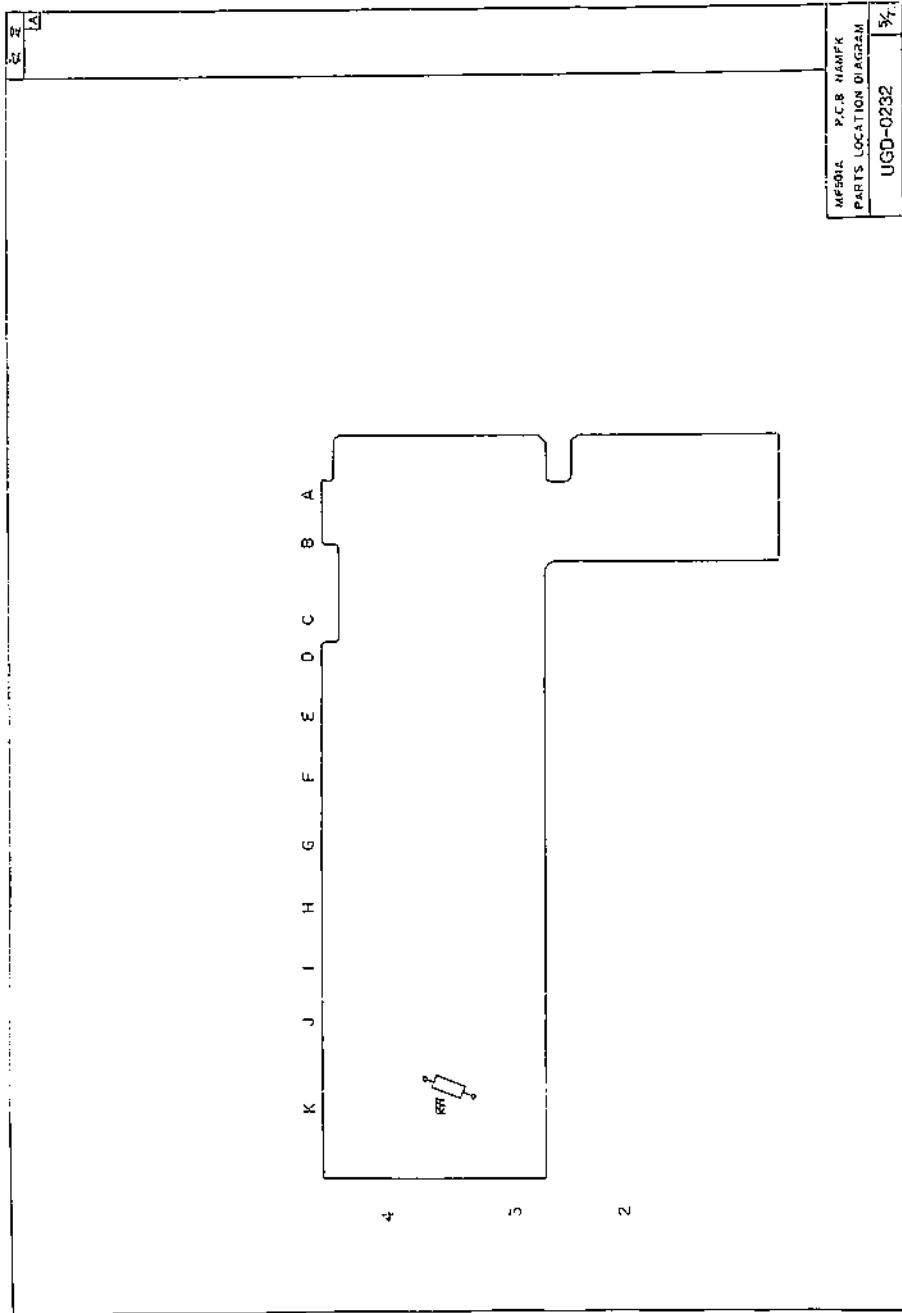
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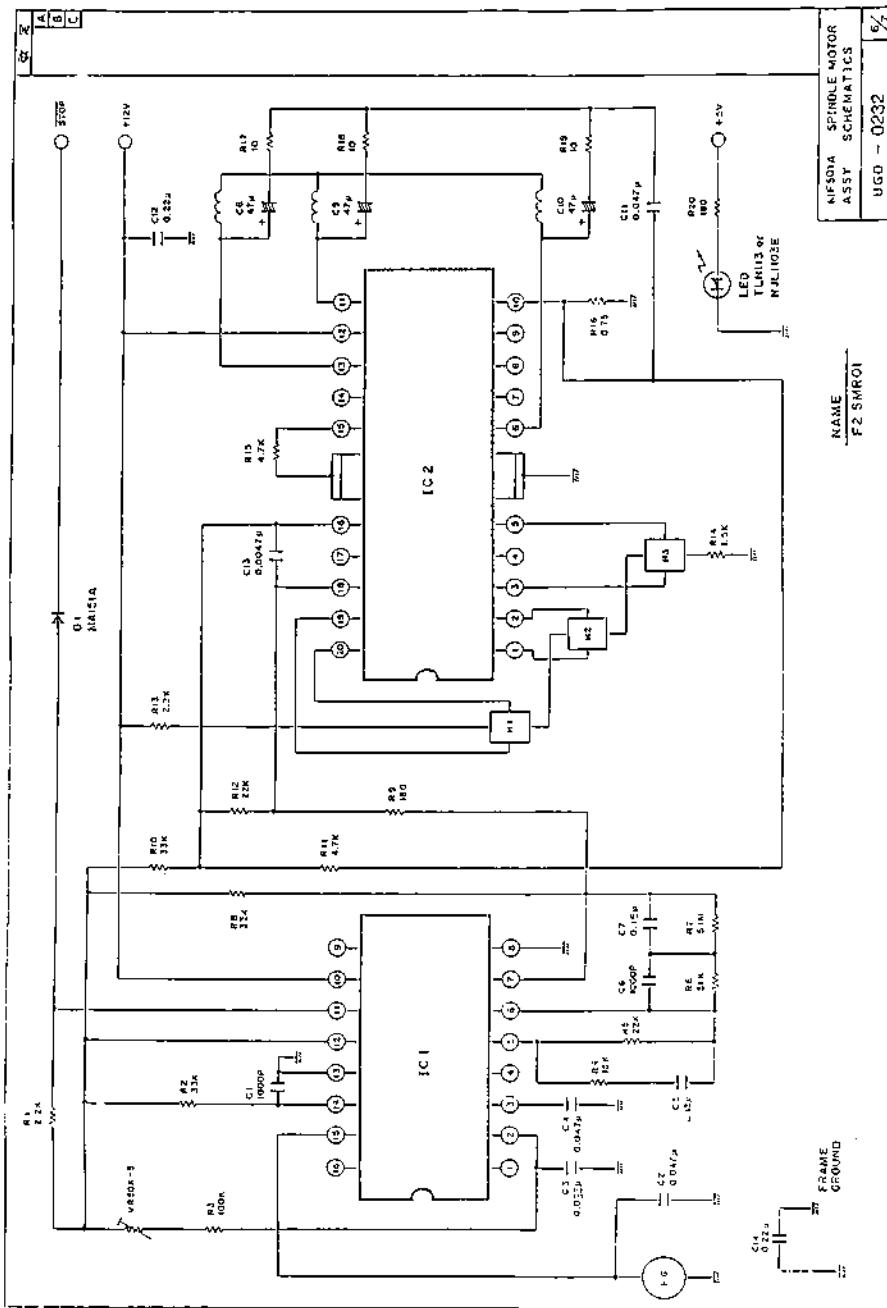
**C,A**

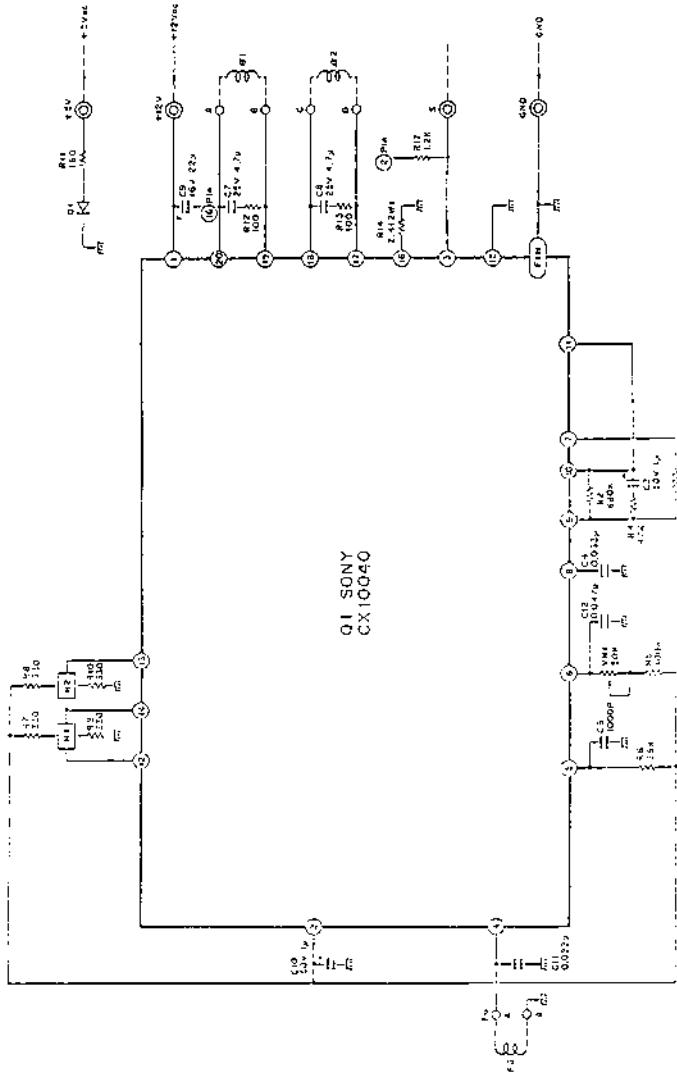












MFSQIA SPINOLE AND ASSY SCHEMATICS

u60 - 0232

NAME \_\_\_\_\_  
TEST 54E



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\*  
\* 360 K. Floppy Disk Drive  
\*  
\* Section 8  
\*  
\* Maintenance Manual  
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5.25 INCH FLEXIBLE DISK DRIVE  
**MF501A-3**

MAINTENANCE MANUAL

 MITSUBISHI ELECTRIC CORPORATION



1



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## 1. Introduction

This manual deals with the handling, maintenance, and adjustment of the MF501A-3 flexible disk unit.

## 2. Related diagrams and references

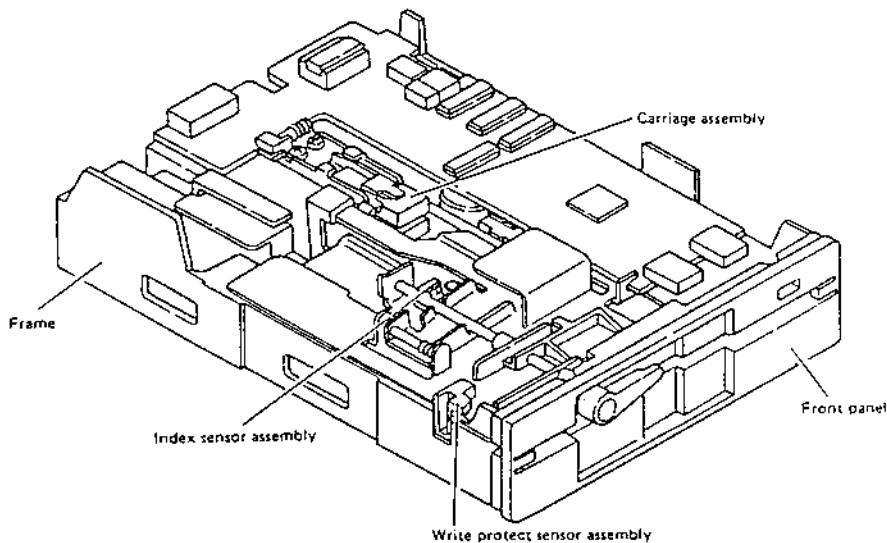
Standard specifications of MF501A-3

Electrical diagram for maintenance of MF501A-3

Illustrated parts list

Packing instructions

## 3. Names of parts



#### 4. Handling

#### 4.1 Operating environment

No problems are likely occur when this unit is used under normal conditions. However damage to the unit or to disks is liable to occur if the unit is used under conditions outside the following:

- (1) Temperature and Humidity: When in use When not in use  
 Temperature range: -10°C ~ 50°C  
 Humidity range: 20% ~ 80% RH (non-condensating)  
 (Max. wet bulb 29.4%) 20% ~ 80% RH (non-condensating)

(2) Vibration and Shock  
 When in use: less than 0.3G (10 ~ 100Hz)  
 When not in use: continuous vibration less than 2G (10 ~ 100Hz)

(3) Dust  
 Special caution should be taken regarding dust as it damages the magnetic head and recording surface of the disk.

(4) Temperature drop  
 Less than 20°C/Hour (when unpacked)

#### 4.2 Handling of disk cartridge (special caution should be taken regarding the following, see Diagram 1)

- (1) Do not place the unit near any device which produces a magnetic field.  
(For example, radios, TVs, motors, generators etc.)
  - (2) Do not bring any magnetized objects near the cartridge.  
(For example, rubber magnets, magnets for blackboards, screwdrivers etc.)
  - (3) Do not bend the disk.
  - (4) Place the disk cartridge into its paper case when it is transported or stored.
  - (5) Do not touch the disk cartridge itself. Do not try to clean it with alcohol or similar liquids.
  - (6) Do not place it in direct sunlight or in places which have high temperature or high dust levels.
  - (7) Do not write anywhere but on the label. Use only a felt-tipped marker or similar pen.

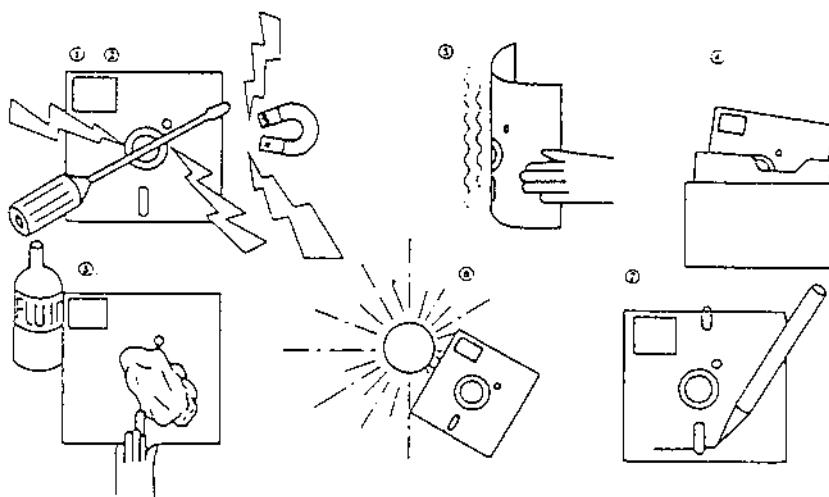


Fig. I

## 5. Periodical maintenance

Periodical inspection, maintenance, cleaning, and replacement of worn-out parts is recommended to maintain the correct operation of this unit and to spot trouble quickly.

The time between periodical maintenance is calculated based on a 8 hour/day schedule. Thus, it may have to be adjusted if actual use is different. Based on usage of 8 hours/day under normal conditions, periodical maintenance should be once a year.

### 5.1 Precautions regarding maintenance

#### 5.1.1 Precaution

- (1) Be sure that dust does not get inside the unit and that the head is not damaged.
- (2) Be sure that the power is off before beginning maintenance.
- (3) The DC power must be off when the connector is inserted or removed from the PC board. This is to prevent damage to the semiconductors.
- (4) Do not touch the surface of the disk or the magnetic head.
- (5) When this unit is used for playback (when CE disks etc are being used), be careful of operations such as write protection for the protection of recorded data.
- (6) Do not touch or attempt to adjust the steel band.
- (7) Do not force or subject the head carriage assembly to shock of any sort as it was precision adjusted. Do not use screws or nuts other than those specified and do not attempt to re-adjust the assembly.

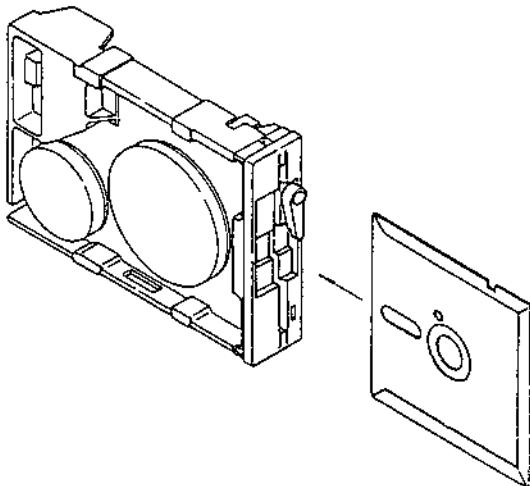
#### 5.1.2 Disks which can be used

- (1) CE diskettes: 224-2A standard diskette made by DYSAN
- (2) Cleaning diskette: CED-SM made by Nihon Micro Coating

## 5.2 Head cleaning

Clean the head as dirt on the head can lead to read errors and damage to the disk. The head is cleaned by the following procedure.

- 1) Equipment
  - CE tester
  - Cleaning diskette
- 2) Cleaning method



### 2) Cleaning method

- 2) -1 Connect the CE tester to the unit and turn the power on.
- 2 Insert the cleaning diskette and start head loading.
- 3 Remove the cleaning disk after about 1 minute of cleaning.

### 3) Precautions

- 3) -1 Match the head to the track of the disk to improve cleaning efficiency.
- 2 Clean the unit for about 1 minute.
- 3 The cleaning disk is good for 1 hour per track. Replace it after the expiration of this period.
- 4 Do not clean the unit more than once at a single time or more than twice a month. This will prevent the head from being deformed.

### 5.3 Testing and adjustment

#### 5.3.1 Adjustment of rotational speed of diskette

- 1) Tested  $T = 163.4 \sim 170.0 \text{ ms}$
- 2) Adjusted  $T = 165.0 \sim 168.3 \text{ ms}$

#### 1) Equipment

CE tester

Blank diskette

Universal counter

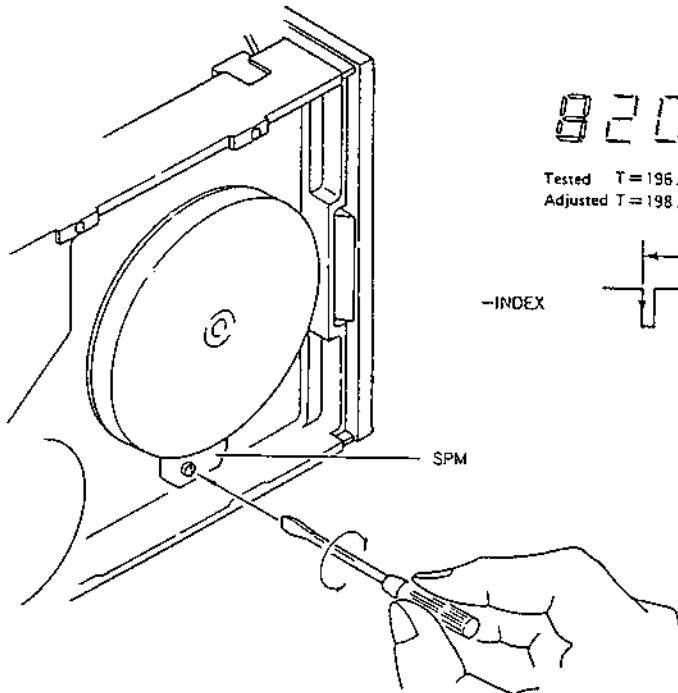
Screw driver for adjusting the volume.

#### 2) Adjustment

- 2) -1 Connect the CE tester to the unit and turn the power on.
- 2 Insert the diskette into the unit, turn the motor on, and start drive select operations.
- 3 Check HLMG ON. (Only as an option)
- 4 Go to track 00.
- 5 Connect the INDEX signal or TPC14(INDEX) to the universal counter and measure the rotational speed.
- 6 Adjust the SPM volume. Check that the counter values are within the specified ranges.

Specified values      Tested       $T = 195.8 \sim 203.2 \text{ ms}$

Adjusted       $T = 198.6 \sim 201.4 \text{ ms}$



-INDEX

8200.0 ms

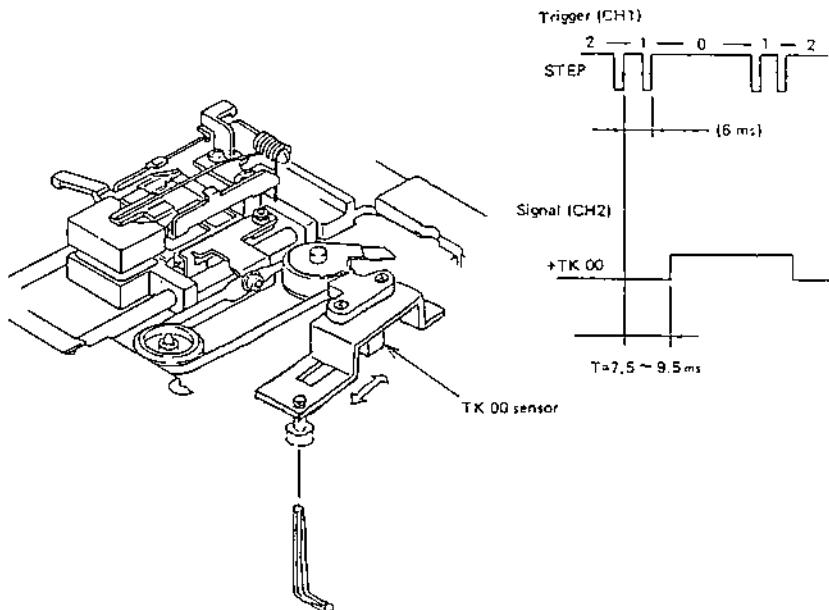
Tested  $T = 195.8 \sim 203.2 \text{ ms}$

Adjusted  $T = 198.6 \sim 201.4 \text{ ms}$

### 5.3.2 Adjustment of position of TK00 sensor

- 1) Equipment
  - CE tester
  - Blank diskette
  - Allen wrench(2.5mm)
  - Oscilloscope
- 2) Adjustment
  - 1 Connect the CE tester to the unit and turn the power on.
  - 2 Turn the motor on and start drive select operations.
  - 3 Perform repeat seeking on tracks 00 ~ 02. (step rate 6ms)
  - 4 Monitor the TPC13 waveform [TK00] with the oscilloscope.  
Trigger CH1= -STEP (DC, -)  
Signal CH2= +TK00 (DC+) (TPC13)
  - 5 Turn the installation screw until the time of T is 7.5 ~ 9.0ms. This will move the TK00 sensor in the direction of the arrows for adjustment.
  - 6 Confirm that there are two STEP signals.
- 3) Checking

Check that seeking starts from track 00 and stops on track 02. Make sure the voltage of TDP1 is 0 ~ 0.6V when the unit is stopped on track 02.



### 5.3.3 Testing of position of index sensor

#### 1) Equipment

CE tester

CE diskette

No. 1 + Screw Driver

Oscilloscope

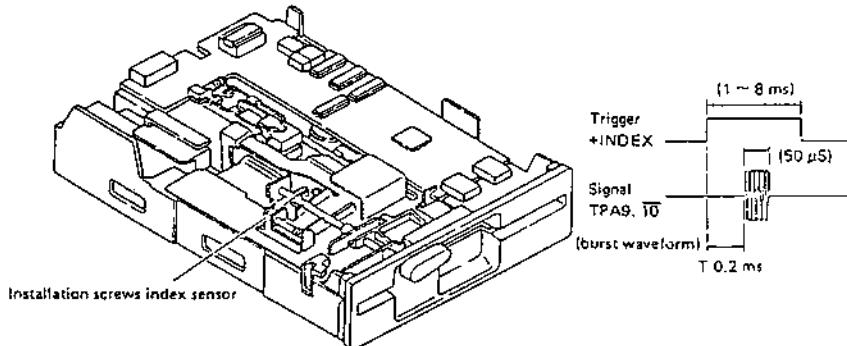
#### 2) Testing

-1 Connect the CE tester to the unit and turn the power on.

-2 Turn the motor on and start drive select operations.

-3 Set the unit to the read mode and monitor the TPA9 and TPA10 waveforms of track 02 with the oscilloscope.

Trigger	TPC14(INDEX) (DC, +)
Signal	CH1— output waveform (AC ) CH2— output waveform (AC, INV) }
Standard	Side 0 Side 2
Testing	200 ± 200μs 200 ± 300μs
Adjustment	200 ± 100μs 200 ± 200μs



### 5.3.4 Adjustment of head alignment

#### 1) Equipment

CE tester

CE diskette

Oscilloscope

No.2  $\oplus$  Screw Driver

#### 2) Adjustment

- 2) -1 Connect the CE tester to the unit and turn the power on.

-2 Turn the motor on and start drive select operations.

-3 Set the unit to the read mode and monitor the TPA9 and TPA10 waveforms, while the unit goes from track 00 to track 16, with the oscilloscope.

Trigger	TPC14(INDEX)		
Signal	CH1— output waveform (AC )	1 } ADD (TPA9)	
	CH2— output waveform (AC, INV)		{ (TPA10)

Standard      Testing      Adjustment

When A > B B/A    0.67.      0.75

When A < B A/B    0.67.      0.75

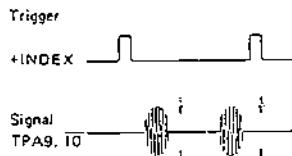
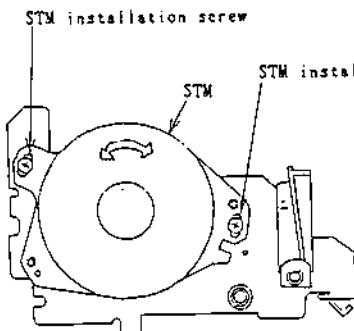
-4 Adjust the STM installation screws to obtain the above standards while the unit goes from track 00 to 16 or from track 39 to 16. This will turn the STM in the direction of the arrows for adjustment. (tighten the screws after adjustment)

-5 Adjust both head 0 and head 1 until both are within the above specifications.

#### 3) Precautions

Perform adjustment until the following conditions:

Temperature  $23 \pm 2^{\circ}\text{C}$ } after waiting 2 hours  
Humidity  $50 \pm 5\% \text{ RH}$



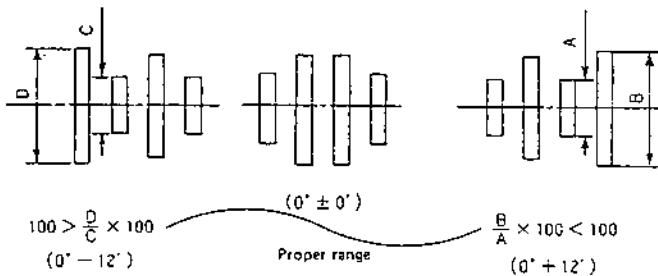
### 5.3.5 Testing of head azimuth

#### 1) Equipment

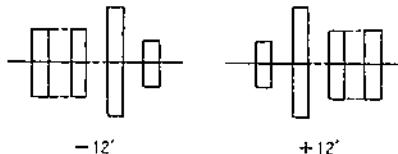
CE tester  
CE diskette  
Oscilloscope

#### 2) Testing

- 2) -1 Connect the CE tester to the unit and turn the power on.
  - 2 Insert the diskette, turn the motor on, and start drive select operations.
  - 3 Set the unit to the read mode, perform seek operations for track 34, and monitor the TPA9 and TPA10 waveforms with the oscilloscope.
- |         |  |
|---------|--|
| Trigger | TPC14(INDEX) IDC, +)   |
| Signal  | CH1— output waveform (AC, ) } ADD (TPA9)<br>CH2— output waveform (AC* INV) } (TPA10) |
- 4 The unit is operating correctly if the waveforms are within the following ranges.



Reference



\*\*\*\*\*  
\*  
\*       360 K. Floppy Disk Drive       \*  
\*  
\*                  Section 9              \*  
\*  
\*                  Technical Manual     \*  
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5.25 INCH FLEXIBLE DISK DRIVE

**MF501A-3**

TECHNICAL MANUAL



MITSUBISHI ELECTRIC



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## CHAPTER 1 GENERAL

The structures of the mechanism and control electronic circuits of the MF501A-3 Flexible Disk Drive are as follows:

The MF501A-3 is a track density 4BPI dual sided drive, with a step angle 3.6° step motor used in the head positioning mechanism, and the maximum operation step pulse rate is 6 msec.

### 1.1 Composition of mechanism by Function

The mechanism can be divided by function as follows:

- (1) Lever mechanism and door SW mechanism
- (2) Disk rotation and clamp mechanism
- (3) Magnetic head positioning mechanism
- (4) Magnetic head/carriage mechanism
- (5) Sensors (index, write protect, track 00)

### 1.2 Composition of Electronic Circuitry by Function

The electronic circuits are installed on two printed-circuit boards and can be classified by function as follows:  
The spindle motor drive circuit constitutes an independent printed-circuit board which is built integrally with the motor.

- (1) Signal interface circuit and drive select circuit
- (2) Power-on reset circuit
- (3) Panel indicator drive circuit
- (4) Index pulse generator circuit and ready circuit
- (5) Step motor drive circuit
- (6) Track 00 detection circuit
- (7) Side select circuit
- (8) Write/erase circuit
- (9) Write-protect circuit
- (10) Read circuit
- (11) Spindle motor drive circuit

## CHAPTER 2 DESCRIPTION OF MECHANISM OPERATION

Figure 2-1 shows an exploded view of the mechanism

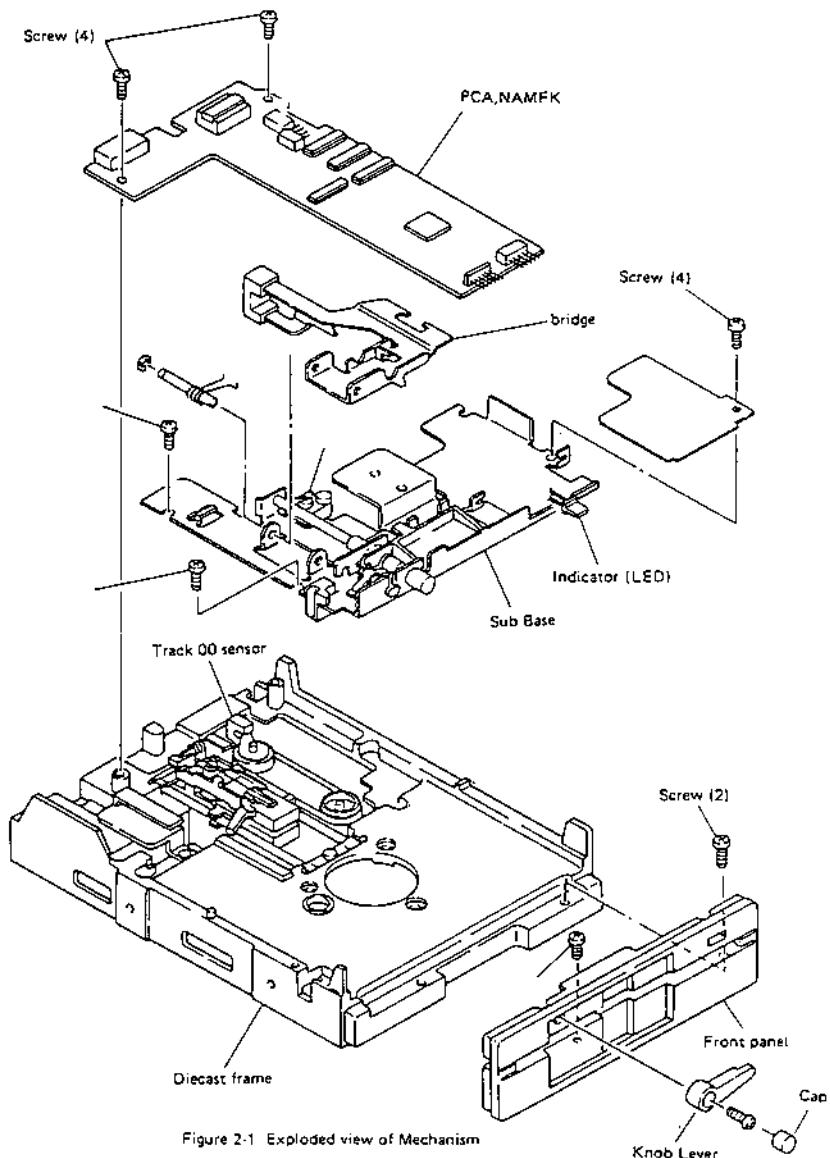


Figure 2-1 Exploded view of Mechanism

## 2-1 Disk Rotation Drive and Clamp Mechanism

The disk rotation drive motor is a flat DC servo motor. This motor has as long a life as an ordinary AC motor because it is a brushless type that uses a Hall element for coil phase-switching detection.

The motor does not use a belt, unlike conventional counterparts, but is a direct-drive type with the rotor and spindle directly connected to each other. This is another feature for prolonging motor life and assuring that the rotation mechanism is completely free of maintenance. The spindle motor runs at 300 rpm, which is controlled by the frequency-generator coil for the servo on the printed-circuit board that is built integrally with the motor. The frequency-generator coil detects the spindle motor speed and forms a servo circuit to control it.

The disk is clamped by the spindle cone on the motor side and by the collect on the sub-base. The collect guides the disk to a position on the inner surface of the spindle cone. This assures compatibility between diskettes and the disk drives.

The collect is tapered to a specific angle to correct non-alignment of an inserted disk with the spindle cone. Figure 2-2 shows the spindle motor and collect.

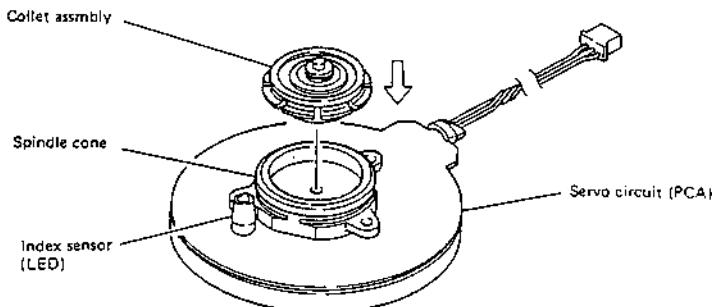


Figure 2-2 Spindle Motor and Collect

## 2-2 Magnetic Head-Positioning Drive Mechanism

The flat step motor drives the magnetic head to each track (cylinder) in succession. The capstan mounted on the step motor shaft has a thin-loop steel band, which is pulled by the spring attached to the idler pulley located opposite the steel band to maintain a specific tension. The head/carriage assembly, supported by two guide rods, is fastened to the steel band so that a turn of the step motor by  $3.6^\circ$  moves the head by a single track distance. Figure 2-3 shows the positioning drive mechanism.

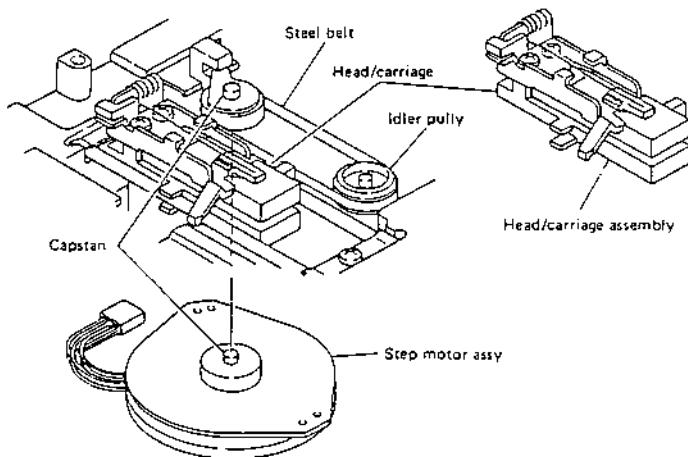


Figure 2-3 Magnetic-Head Positioning Mechanism

## 2-3 Magnetic Head/Carriage Mechanism

The magnetic head /carriage assembly consists of two magnetic head sliders that are supported by a quadrangular gimbal spring and a plastic-molded carriage. The side 0 head is mounted in the carriage main frame, and the side 1 head is mounted on the movable arm is pushed by a coil spring to apply constant pressure during head loading. An external view of the carriage assembly is shown in figure2-3, and the gimbal spring/head assembly is shown in figure 2-4.

The magnetic head is composed of three ferrite core chips and a ceramic support slider. The center core is for reading and writing, and the two cores on both sides of it are erase head cores. Figure2-5 shows an external view of the head slider.

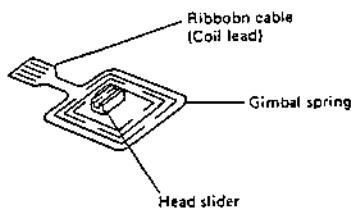


Figure 2-4 Gimbal Spring/Head Assembly

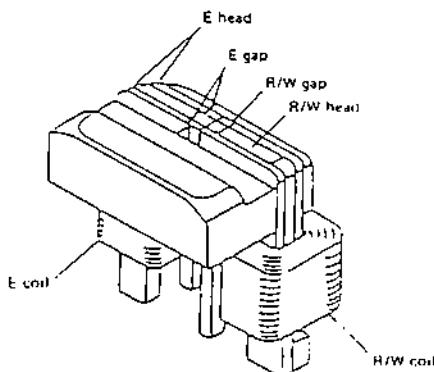


Figure 2-5 External View of Head Slider

## 2-4 Sensors (Index, Write Protect, Track 00)

### (1) Index sensor

The index sensor detects disk rotation. This sensor consists of an LED on the light-emitting side and a photo transistor on the light-receiving side. The LED is mounted on the servo circuit PCA for the spindle motor (figure 2-2), and the photo transistor is attached to the sub-base; this will transmit signals to CPA. Index sensor timing (position) can be adjusted by loosening the screws on the index sensor and repositioning index sensor.

Figure 2-6 shows where the photo-transistor for the index sensor is mounted.

### (2) Write-protect sensor

The write-protect sensor detects the diskette's write-protect notch and inhibits write operation. This sensor protects information stored on read-only disks from destruction by operation errors.

Disk with the diskette's notch covered with tape or a seal that does not transmit light are protected by this sensor. Remember that vinyl or cellophane tape that has a high percentage of light transmission will not protect the disk. The write-protect sensor is mounted on sub-base as shown in figure 2-6. [Attached to the sub-base, this will transmit signals to CPA.]

### (3) Track 00 sensor

The track 00 sensor detects that the head is on track 00.

The track 00 sensor detects the position of the light-shielding plate that projects from the head/carriage assembly. The sensor is screwed to the STM holder and can be adjusted in position by loosening the screw.

The track 00 sensor and head/carriage assembly are shown in figure 2-7.

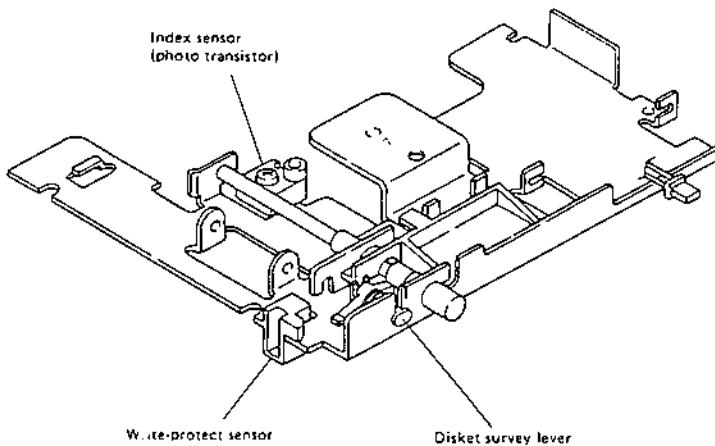


Figure 2-6 Index Sensor and Write-protect sensor

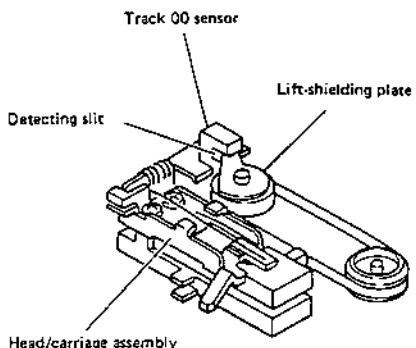


Figure 2-7 Track 00 Sensor and Head/Carriage Assembly

## CHAPTER 3 DESCRIPTION OF ELECTRONIC CIRCUIT OPERATION

Figure 3-1 shows the electronic circuits and signal connections among these circuits. The spindle motor drive circuit within the dotted lines constitutes the separate printed-circuit board that is built integrally with the motor. The parts within the chain lines belong to the mechanism described in the previous pages.

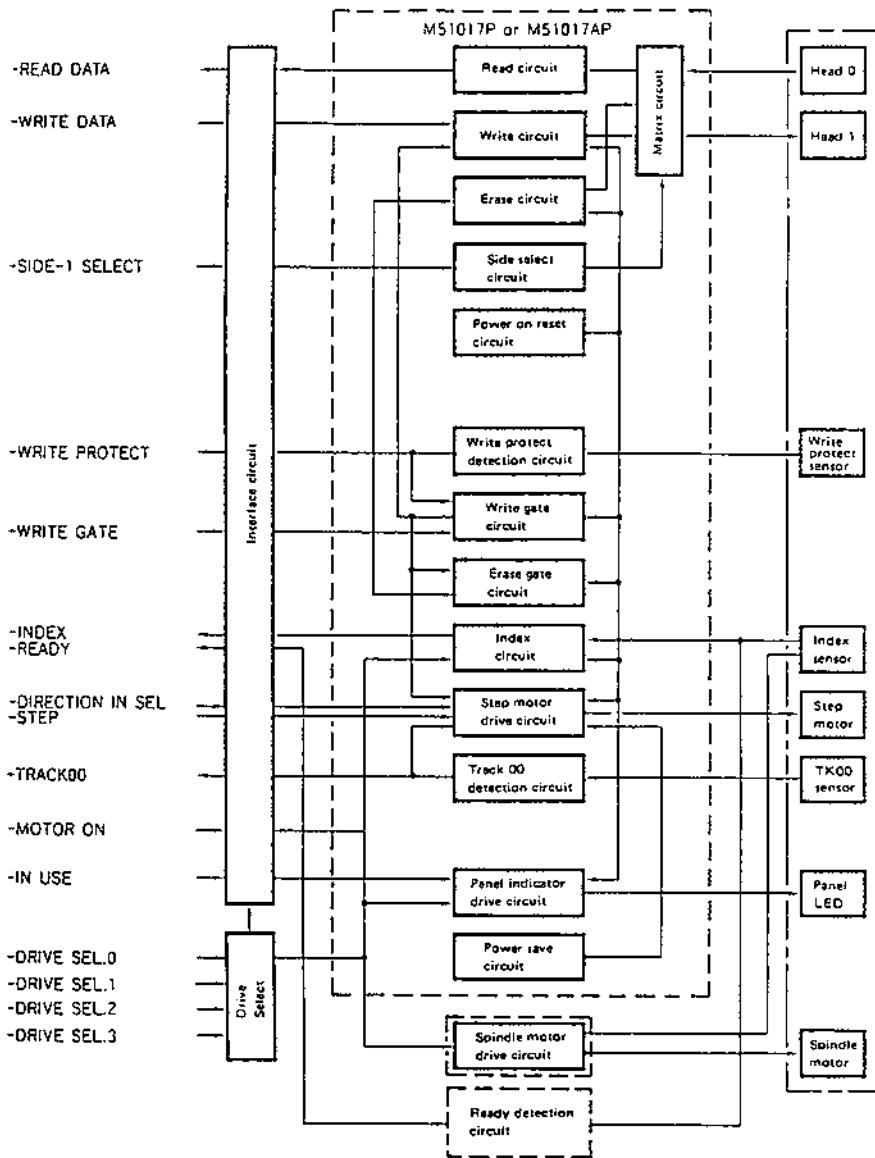


Figure 3-1 MF501A~3 Electronic circuit

### 3-1 Interface and Drive Select Circuits

#### (1) Receive circuit

All the input terminals of the receiver that receives signals from the host controller are terminated at 150 ohms, pulling them up to +5 V. The host controller, therefore, must use driver elements with a drive capacity of 40 mA or more. Normally, an SN7438N or an equivalent open-collector drive is recommended. In connecting two or more disk drives (up to four) by a daisy-chain pattern, it is necessary to keep the cable end terminating resistor and remove the terminating resistors of the other disk drives.

#### (2) Transmit circuit

The disk drive line driver is an SN7438N or equivalent open-collector gate. It is necessary for the host controller to use a terminating resistor of 150 ohms or more.

All input signals to the line driver are gated by drive select signals. Thus, if two or more disk drives are connected in the daisy-chain pattern, the signals of only one selected disk drive are transmitted to the host controller.

#### (3) Drive select circuit

The drive select circuit selects one of the disk drives (four maximum) connected with the same cables through four interface lines (DS0 through DS3).

The four select lines correspond to the jumper plugs on the printedcircuit boards, one of which should be inserted to select the desired line. Never insert plugs into the same-numbered jacks on two or more disk drives that are connected with the same cable; interference between the output signals from such disk drives will cause errors.

The drive select signals also light the panel indicator LED.

In the case of a system requiring no drive selection, insert the jumper plug for the drive select line into the MX to maintain a selected condition.

### 3.2 Power-On Reset and Power Save Circuits

#### [1] Power-on reset circuit

The power-on reset circuit, a level-detection type reset circuit, initializes the control LSI, and that's used for preventing operation errors of the write circuit in switching power on, off.

#### [2] Power save circuit

The power save circuit controls current flowing to the step motor and head load solenoid according to their operating condition to reduce heat generation by unnecessary power consumption and thus to reduce temperature rise of the disk drive.

The step motor use a 30 msec. timer.

Timing chart of the power save circuit is shown in figure 3-2.

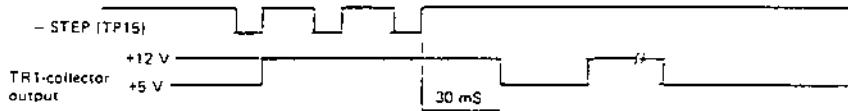


Figure 3-2 Power Save Circuit Timing Chart

### 3.3 Panel Indicator Circuit

The panel indicator is turned on by a drive select signal or by a drive select signal and in-use signal. When no in-use signal is applied to the interface, the panel indicator is turned on by a drive select signal only. If the jumper plug for the drive select circuit is inserted into the MX, the panel indicator is always lit up.

### 3.4 Index Sensor and Ready Circuits

The index sensor circuit detects the index holes in the disk with a sensor, and converts its signals into logic signals.

The ready circuit checks the index pulse intervals with a timer, and becomes ready when the intervals are less than 300 ms and the next index pulse is generated.

When the lever opens and the disk stops rotating and the motor-on signal turns off and the disk stops rotating the ready signal is reset.

Figure 3.3 shows a timing chart.

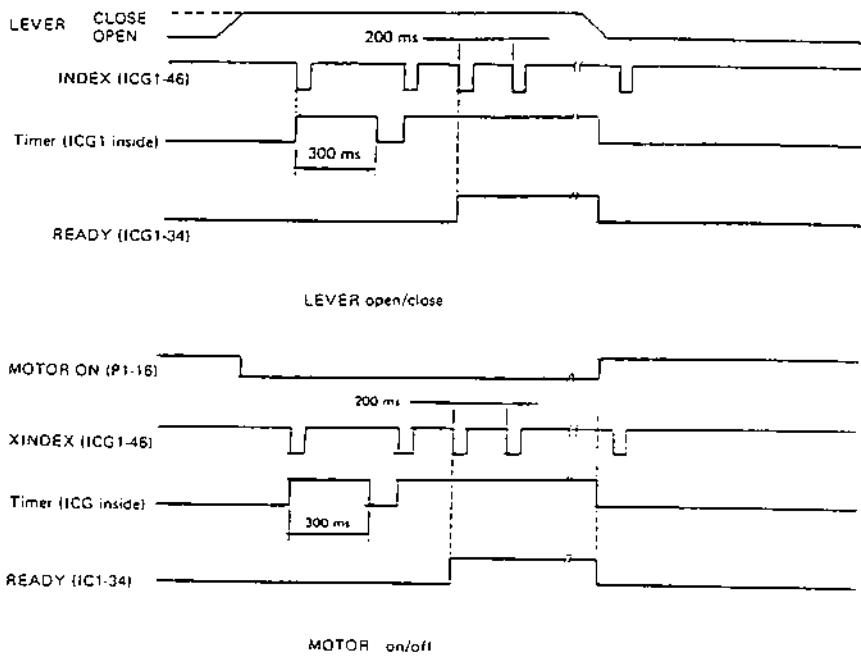


Figure 3.3 Index Sensor and Ready Circuit Timing Chart

### 3.6 Step Motor Drive Circuit

The step motor is a two-phase unipolar type and is driven to a step angle of  $3.6^\circ$  by feeding four mode currents, using four open collector type drivers.

These four modes are generated by an up-down four-court counter that uses two flip-flops.

The step motor drive circuit switches the voltage supplied to the motor drive circuit to reduce power consumption during times other than seeking, when the motor is still.

In a seek operation, +12 V is supplied to the drive circuit, but if the next step pulse is not applied to the interface for 30 ms or more, +5 V is supplied.

Figure 3-4 shows a timing chart.

The step motor drive circuit blocks the step pulses with a write gate (except for the erase delay time) to prevent seeking during write operation.

### 3.7 Track 00 Detection Circuit

The track 00 detection circuit detects the position of the light-shielding plate that projects from the step motor capstan, using a sensor. This output is ANDed with the step motor drive phase (TK00) to generate a track 00 signal. The circuit will not output a signal, therefore, unless the drive phase is at track 00 even if the sensor output is on.

For a timing chart, refer to figures 3-4.

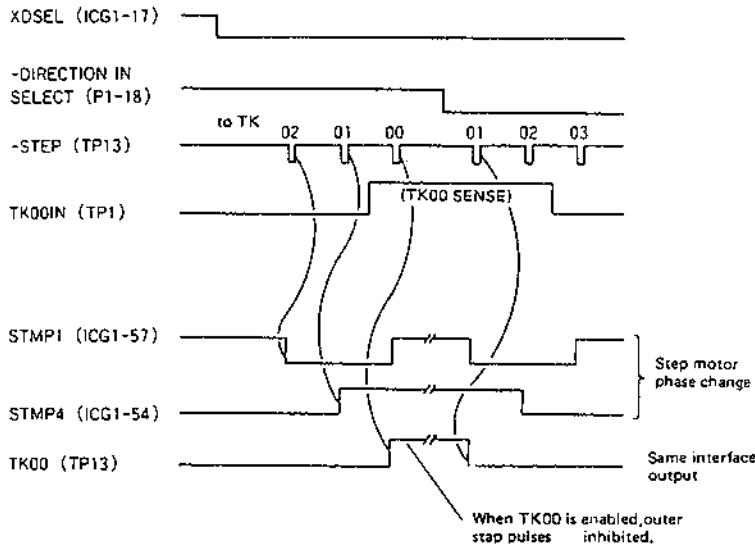


Figure 3-4 Step Motor Drive Circuit Timing Chart

### 3.8 Side Select Circuit

The host system selects side 1 through the interface line if – SIDE ONE SELECT is low, or side 0 through the same interface line if it is high.

Figure 3-5 shows a block diagram of the side select circuit.

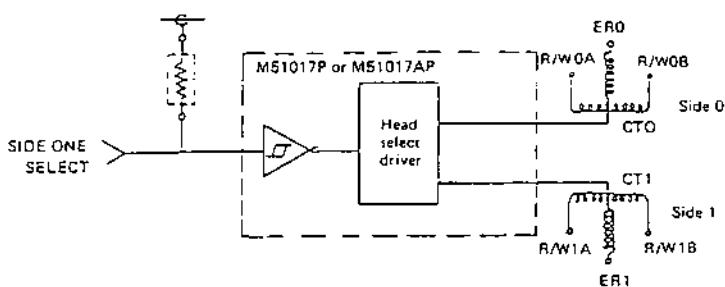


Figure 3-5 Side Select Circuit Block Diagram

### 3.9 Write/Erase Circuits

The write circuit is used for recording data on the disk. It starts writing when the write gate is opened for the selected head. If diskette write-protect status is detected, no write operation is performed.

The erase circuit erases the previous data written on both sides of the data by DC erasure. This function prevents old data from remaining on either side of newly written data due to a slight deviation of head position, and thus prevents old data crosstalk in reading the new data.

The write circuit consists of the following blocks:

- Write toggle flip-flop
- Write driver
- R/W matrix
- Write current source

When a write gate is input, the write toggle flip-flop, write driver and write current source are enabled to start a write operation. Write data is counted down to one half by the write toggle flip-flop, and a differential signal that changes synchronously with the write data is generated.

This differential signal switch the write driver.

The write driver is a switching circuit that feeds a current to the R/W head. This current is generated by the write current source and is sent to the write driver.

The R/W matrix feeds a current to the head selected by SIDE ONE SELECT as the write circuit gate is opened by a write gate.

Figure 3-6 shows the erase function and figure 3-7, a write circuit block diagram.

Current is alternately fed to the R/W head through two current routes, CT → R/WA and CT → R/WB as shown in the figure, according to the differential signal to invert its magnetization.

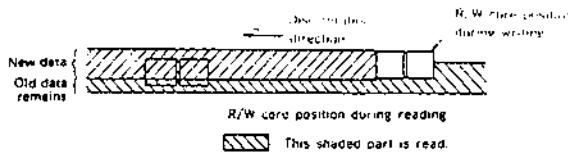
Erase operation starts with point E before write start point C and ends at point F after write end point D. The position deviation of the R/W core from the erase core is about 0.9 mm, and the erase core reaches a point that the R/W core gap has passed about 600  $\mu$ s later (near TK 32).

Therefore, the delay operation shown in figure 3-15 is required for the time from the opening of the write gate to the turning on of the erase driver and from the closing of the write gate to the turning off of the erase driver. It is for this purpose that the erase delay timer is provided to control the erase driver. Thus, for about 1000  $\mu$ s after the closing of the write gate, the head must remain on the track and be kept selected.

The erase function erases data from the disk by always magnetizing it in one direction.

Figure 3-8 shows a conceptual diagram of write operation and figure 3-9, an erase delay operation timing chart.

[Without erase head]



[With erase head]

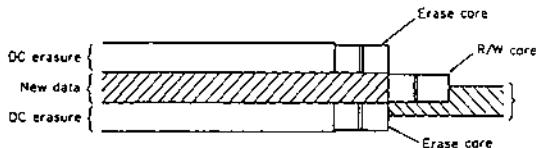


Figure 3-6 Erase Function

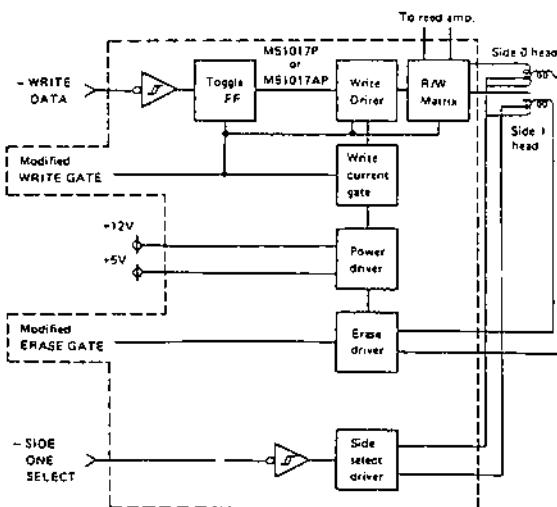


Figure 3-7 Write Circuit Block Diagram

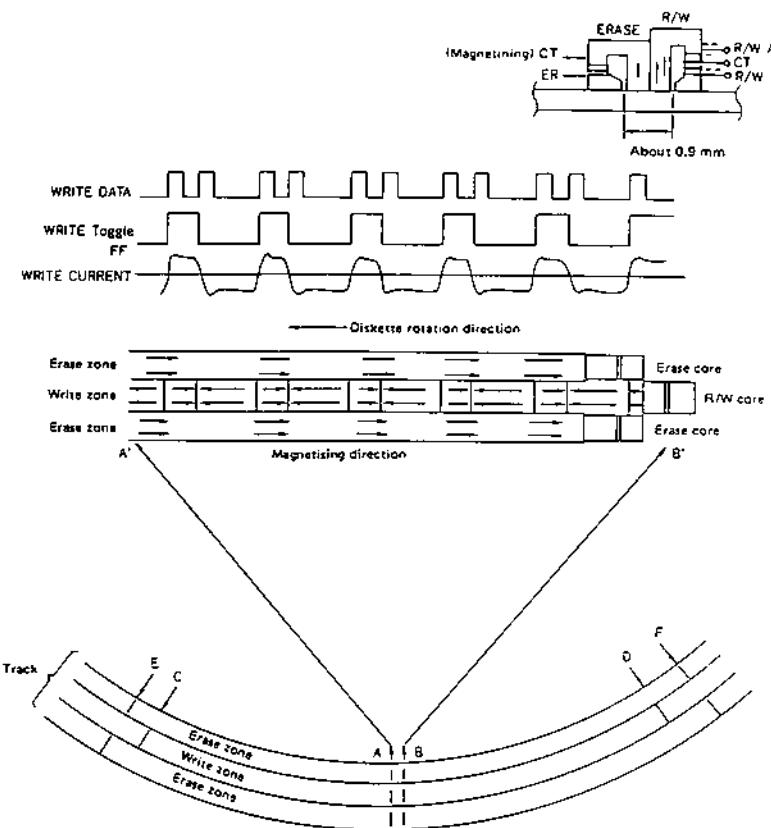


Figure 3-8 Write Operation Concept

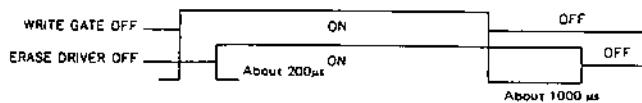


Figure 3-9 Erase Delay Operation Timing Chart

### 3.10 Write-Protect Circuit

The write-protect circuit detects the notch (cutout in the jacket) of the diskette with a sensor to inhibit write operation even if a write gate signal is received from the interface, and outputs a write-protect signal to the interface. Figure 3-16 shows a circuit diagram of the write-protect circuit.

### 3.11 Read Circuit

The diskette is read when the write gate and erase driver are closed.

The R/W core is on a track. If a head has been selected, the core reads the inversions of magnetization of the previously written data to induce a voltage between the two ends of the R/W coil (between R/WA and R/WB). This voltage is input to the read preamplifier via the R/W matrix.

The read preamplifier provides a gain about 280 times the level of a few millivolts induced in the head, and amplifies the input into a differential signal high enough for signal processing.

The read signal from the read preamplifier is fed through a low-pass filter that cuts out excess high frequencies. Because the position of inverting magnetization is expressed by a read signal peak, the read signal is fed to a peak-detection circuit to generate a read data pulse.

The peak-detection circuit consists of three blocks.

- Differentiator
- Comparator
- Time domain filter

The differentiator is a differentiating circuit to detect the peak point, and the detected peak point is converted to a zero-crossing point. The differentiated signal is routed to the comparator, where it is converted from an analog signal to a digital signal. The point of change of this digital signal actually becomes a data pulse.

FM or MFM means frequency modulation. The magnetization inversion intervals used are 8  $\mu$ s and 4  $\mu$ s for FM, and 8  $\mu$ s, 6  $\mu$ s, and 4  $\mu$ s for MFM, corresponding to a maximum frequency of 125 kHz and a minimum frequency of 62.5 kHz.

The electromagnetically converted magnetized reverse waveforms will be mutually interfered with by the neighboring magnetized reverse waveforms, and the composite waveform will be the waveform that is read out. However, when the magnetized reverse interval becomes longer, the mutual interference will decrease and shoulders will be generated. Since once shoulders are generated, the postdifferentiated waveforms will zero-cross, incorrect data pulses will be detected. To remove the incorrect data pulses, a time domain filter has been incorporated. As long as the comparator output level is maintained at the previous level, the time domain filter will output the correct (2) READ data.

The read data thus generated is sent to the host system. Figure 3-10 shows a read circuit block diagram and figure 3-11, a read timing chart.

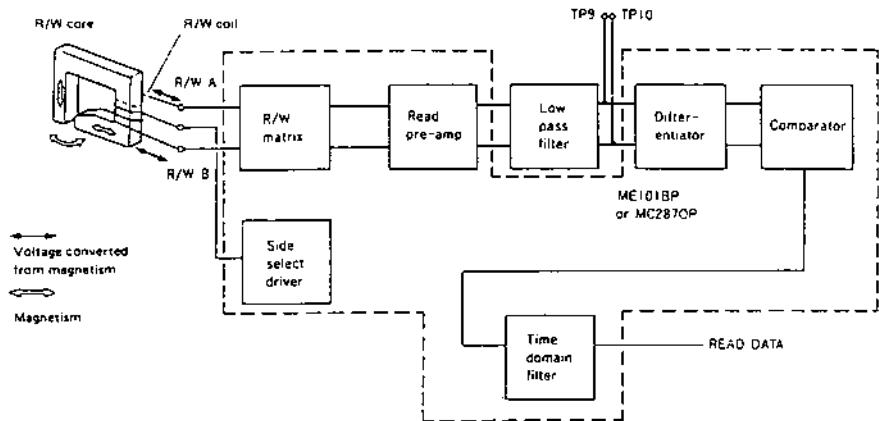


Figure 3-10 Read Circuit Block Diagram

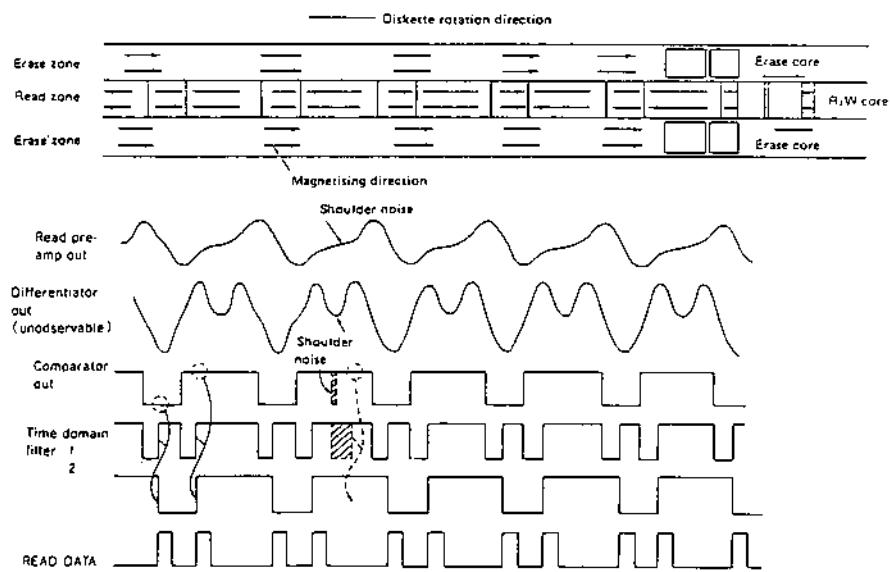


Figure 3-11 Read Timing Chart

### 3.12 Spindle Motor Drive Circuit

The spindle motor is a DC, direct, brushless motor for which a feedback servo circuit is employed to maintain the correct speed at all times. This circuit is installed on a printed-circuit board that is built integrally with the motor.

It is connected to the main control circuit with four signal lines: +12 V DC, 0V, motor-on signal, and INDEX LED.

This feedback servo circuit employs Hall elements for position feedback and a frequency generator, or tachometer generator, for speed feedback to constitute a secondary system to stabilize motor rotation.

Spindle rotating position is detected by the Hall elements located symmetrically from the rotating spindle, and the information is fed to the predriver to alternately switch driver 1 and driver 2.

The speed signal output by the frequency generator for speed control is rectified and integrated into a speed voltage, which is compared with the reference speed voltage to feed back the level of current to be supplied to the coil.

Figure 3-12 shows a spindle motor drive circuit block diagram and figure 3-13, a conceptual diagram of the spindle motor drive circuit waveforms.

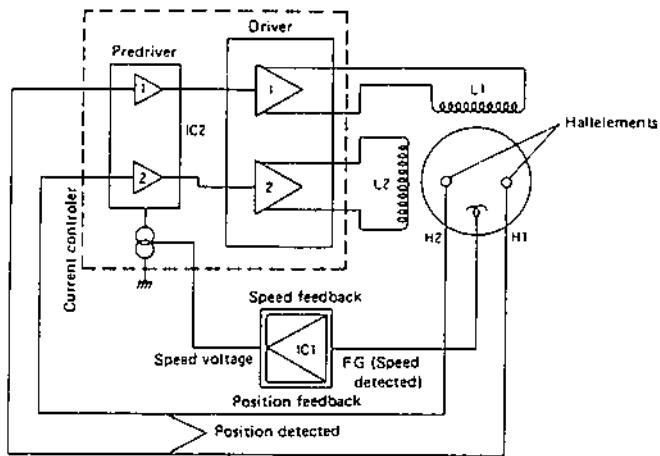


Figure 3-12 Spindle motor drive circuit Block Diagram

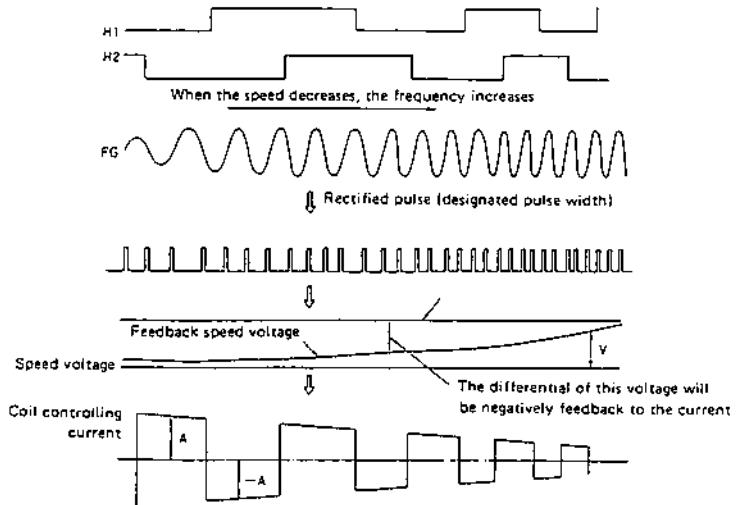


Figure 3-13 Spindle motor drive current waveform configuration

\*\*\*\*\*  
\* \* 360 K. Floppy Disk Drive \* \*  
\* \* Section 10 \* \*  
\* \* MF501A-347UA \* \*  
\* Standard Specifications \* \*  
\*\*\*\*\*



**5.25 INCH FLEXIBLE DISK DRIVE  
STANDARD SPECIFICATIONS  
MF501A-347UA**

 MITSUBISHI ELECTRIC CORPORATION



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## CHAPTER 1 INTRODUCTION

The Mitsubishi MF501A-3 provide high capacity and high reliability in a compact configuration, with the industry standard 5-1/4 inch media.

### 1.1 General Description

- 1) Half height (41 mm) dimension of conventional model and two MF501A-3 units can be fit into the industry standard size for one 5-1/4 inch flexible disk drive.
- 2) The soft-touch, gimbal-supported magnetic head provides stable contact with the medium.
- 3) Compact Brushless D.C. Motor gives maintenance free.
- 4) Stable media interchangeability by keeping enough window time margin at off-track in a wide range of ambient conditions.
- 5) Dynamic clamping function provides high reliability of diskette centering in order to avoid possible mis-clamping.

## 1.2 Specifications

### 1.2.1 Performance specifications (Table 1-1)

Table 1-1 Performance Specifications

	Double Density
<b>Memory capacity</b>	
Unformatted	
Disk	500 kilobytes
Per surface	250 kilobytes
Per track	6.25 kilobytes
Formatted	256 bytes/sector
Disk	327.7 kilobytes
Per surface	163.8 kilobytes
Track	4096 bytes = 256 bytes x 16 sectors
<b>Transfer rate</b>	250 kilobits/second
<b>Average latency time</b>	100 ms
<b>Access time</b>	
Track to track	6 ms
Average	103 ms (including 6 ms step time and settling time)
Settling time	25 ms
Motor starting time	250 ms (READY ON TIME 600ms MAX.)

1.2.2 Functional specifications (Table 1-2)

Table 1-2 Functional Specifications

	Double Density
Recording density	5877 BPI
Magnetic flux inversion density	5877 FCI
Encoding method	MFM
Track density	48 tracks per inch
Number of cylinders	40
Number of tracks	80
Number of heads	2
Rotation speed	300 rpm
Rotation period	200 ms
Index	1
Media	5.25 inch industry standard media

1.2.3 Physical Specifications (Table 1-3)

Table 1-3 Physical Specifications

DC power requirements +5 V	$+5 \text{ V} \pm 5\%$ , 0.4 A typical 0.7 A max
+12 V	$+12 \text{ V} \pm 5\%$ , 0.3 A typical (seeking) 1.0 A max
Operating environmental conditions	
Ambient temperature	5°C to 43°C (41°F to 109.4°F)
Relative humidity	20% to 80% (Maximum wet bulb temperature: 29°C (85°F))

Table 1-3 (cont..)

Non-operating environmental conditions	
Ambient temperature	-20°C to 51°C (-4°F to 125°F)
Relative humidity	5% to 95%
Heat dissipation	8.5 Watts Continuous seek (typical) 5 Watts Standby (typical) 4 Watts Motor off (typical)
Physical dimensions	(Except for front panel)
Height	41 mm (1.62 in)
Width	146 mm (5.75 in)
Depth	195 mm (7.7 in)
Front panel dimensions	42 x 148.0 mm (1.65 x 5.83 in)
Weight	1.2 kg (2.6 lbs)

1.2.4 Reliability specifications (Table 1-4)

Table 1-4 Reliability Specifications

MTBF	10,000 POH or more
MTTR	30 minutes
Unit life	5 years or 20,000 energized hours, whichever comes first
Media life	
Rotational life	$3.5 \times 10^6$ pass/track or more
Error rate	
Soft read error	$10^{-9}$ bit (Two retries)
Hard read error	$10^{-12}$ bit
Seek error	$10^{-6}$ seek



## CHAPTER 2 OPERATION OF MAJOR COMPONENTS

### 2.1 System Operation

The MF501A-3 Flexible Disk Drive consists of a medium rotating mechanism, two read/write heads, an actuator to position the read/write heads on tracks, and electronic circuits to read and write data, and to drive these components.

The rotation mechanism clamps the medium inserted into the drive to the spindle, which is directly coupled to the DC brushless direct-drive motor, and rotates it at 300 rpm. The positioning actuator moves the read/write head over the desired track of the medium to read or write data.

### 2.2 Electronic Circuits

The electronic circuits to drive the individual mechanisms of the MF501A are located on a single printed-circuit board, which consists of the following circuits:

- o Line driver and receiver that exchange signals with the host system
- o Drive selection circuit
- o Index detection circuit
- o Head positioning actuator drive circuit
- o Read/write circuit
- o Write protect circuit
- o Track 00 detection circuit
- o Drive ready detection circuit
- o Head selection circuit
- o In use and panel indicator LED drive circuit

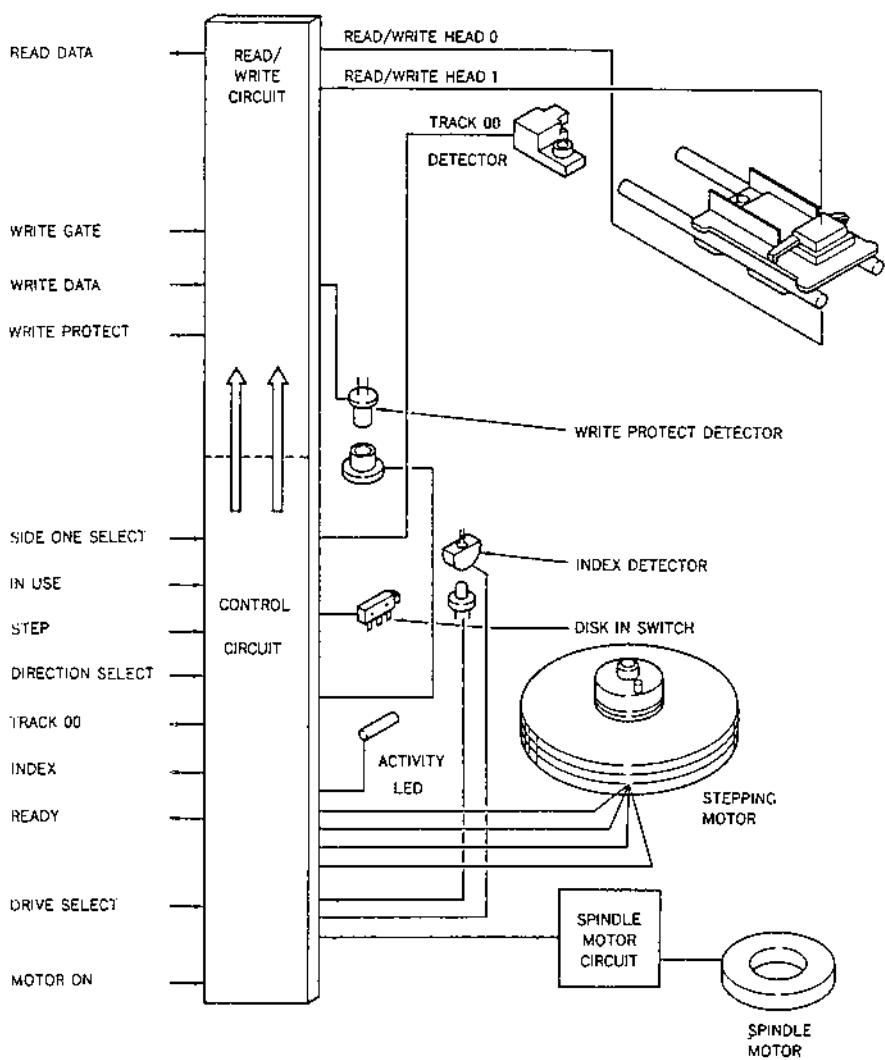


Fig. 1 Functional View

### 2.3 Rotation Mechanism

The diskette rotation mechanism uses the DC brushless direct-drive motor to directly rotate the spindle at 300 rpm.

### 2.4 Positioning Mechanism

The positioning mechanism positions the read/write heads as described below.

The head carriage assembly is fastened to the band secured around the capstan of a stepping motor; a 3.6° turn of the stepping motor moves the read/write head one track in the designated direction, thus positioning the read/write head.

This drive system is temperature compensated to minimize read/write head deviations from the disk tracks caused by ambient temperature change.

### 2.5 Read/Write Heads

The read/write heads are NiZn magnetic ferrite.

Each read/write head has three ferrite head cores, consisting read/write core and erase cores on both sides of the read/write core to erase the space between tracks (tunnel erase).

The two read/write heads, which are located face-to-face with a disk between them, are mounted on compliant, gimbal springs so that the heads track the disk with good contact to enable maximum reproduction of the signals from the disk. The high surface tracking ability of the gimbal keeps the disk free of stress, and thus improves diskette life.



## CHAPTER 3 ELECTRICAL INTERFACE

There are two kinds of electrical interfaces: Signal interface and DC power interface.

The signal interface sends and receives control signals and read/write data between the ~~M4854-1~~ and the host system via the J1/P1 connector.

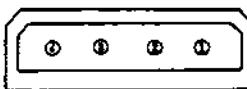
MF501A-3

The DC power interface drives the spindle drive motor of the disk drive, and supplies power to the electronic circuits and the stepping motor which drives the read/write head positioning mechanism via the J2/P2 connector.

The signals and pin arrangement of these two types of interfaces are shown in Tables 3-1 and 3-2.

Table 3-1 DC Power Connector Pin Arrangement (J2/P2)

Source voltage	Pin number	Remarks
+12 V DC	1	
+12 V DC return	2	
+5 V DC return	3	
+5 V DC	4	



P2 connector

Table 3-2 Signal Connector Pin Arrangement (J1/P1)

Signal	Signal Pin Number	Ground Return Pin Number
SPARE *	2	1
IN USE	4	3
DRIVE SELECT 3	6	5
INDEX	8	7
DRIVE SELECT 0	10	9
DRIVE SELECT 1	12	11
DRIVE SELECT 2	14	13
MOTOR ON	16	15
DIRECTION SELECT	18	17
STEP	20	19
WRITE DATA	22	21
WRITE GATE	24	23
TRACK 00	26	25
WRITE PROTECT	28	27
READ DATA	30	29
SIDE ONE SELECT	32	31
READY	34	33

- \* Signal pin 2 is not connected on the FDD side.
- \* There is no particular need to pull up or pull down signal pin 2 on the control side.

### 3.1 Signal Interface

The signal interface is classified into control signals and data signals. These interface signal lines are all at TTL levels. The meanings and characteristics of the signal levels are as follows:

- o True = Logical "0" = VL 0 V to +0.4 V  
Iin 40 mA maximum
- o False = Logical "1" = VH +2.5 V to +5.25 V  
Iin 0 mA
- o Input impedance = 150 Ohms

#### 3.1.1 Cabling method and input line termination

The drive uses a daisy chain system of cable connections. A single ribbon cable or twisted-pair cable may be fitted with multiple connectors to permit connection of up to four drives.

The connected drives are multiplex-controlled by drive select lines, and any one of the drives can be accessed.

The cabling method and input line termination are shown in Fig. 3-1. A maximum of seven input signal lines, plus the drive select lines, may be terminated at the disk drive. Proper operation of the drives requires termination at or near the drive connected to the end of the interface cable farthest from the host system.

The drive has detachable terminator modules on the printed-circuit board to terminate these input signal lines.

When a drive is shipped from the factory, its terminators are installed on the printed-circuit board.

Keep the terminators connected in the drive that is connected to the end of the interface cable, and disconnect the terminators in all the other drives.

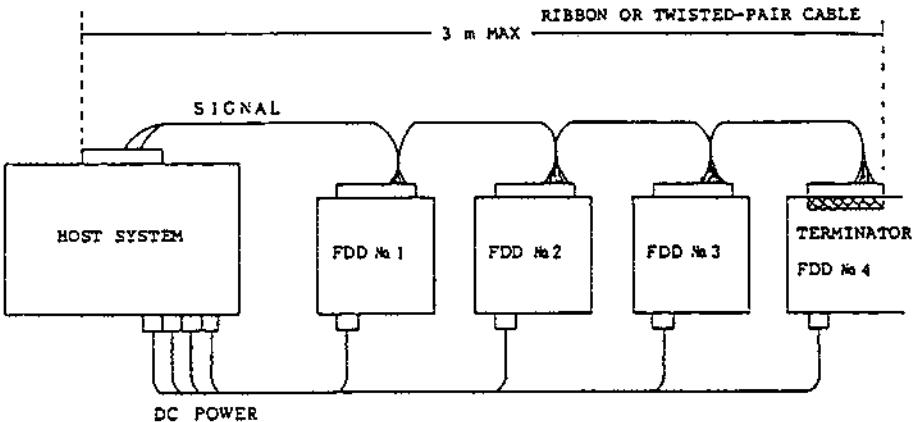


Fig. 3-1 Cabling Method (Sketch)

### 3.1.2 Line driver and line receiver

The recommended interface line driver and line receiver circuits for the host system and the drives are shown in Fig. 3-2.

It is suggested that a Schmitt trigger circuit with a hysteresis characteristic at the switching level be used for the line receiver to improve the noise resistance of the interface lines.

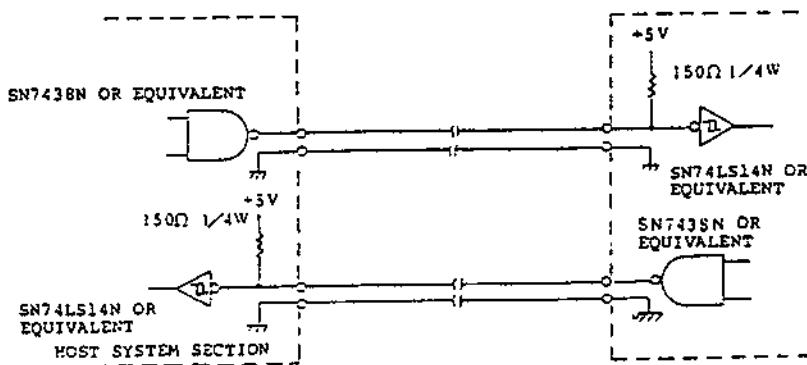


Fig. 3-2 Recommended Line Driver and Line Receiver Circuits

### 3.1.3 Short plug

The short plug sets the conditions for selecting the drive, starting the spindle motor, separating the in-use lines, and sending the ready signal.

The following is the explanation of features of the short plug.

- 1) Drive selection conditions DSO - 3, MX (location of PCB A4) PM1
- 1.1) DSO - 3

If multiple connection is made with the system and the drive, by short-circuiting one of the DSO - 3, the corresponding DRIVE SELECT line will select the drive with the logical "0" only, and input signals can be received.

For example, the drive that has had its DSO - 3 short-circuited, will be selected when DRIVE SELECT 0 line is at logical "0".

- 1.2) MX

When all of DSO - 3 has been opened and MX is short-circuited, the drive will always be selected regardless of the DRIVE SELECT line of the interface. However, in this case the control of the panel indicator LED can only be done with the IN USE signal. However, in this case, the panel indicator LEDs will be in the constant illumination mode. Additionally, since it is not possible to use DRIVE SELECT 0 - 3 to control the switching on/off of the spindle motor, the control will have to be changed to another system.

\* DS1 is short-circuited at the factory before delivery.

Resetting is necessary in order to use another drive number.

- 2) Spindle MOTOR ON conditions selection MM, MS (location of PCB B4) PM2.

The conditions for Spindle MOTOR ON conditions are selected by the combination of opening and short-circuiting of MM and MS.

Short plug		Refer to	Notes
MS	MM		
open	short	2.1	Before delivery
short	open	2.2	
open	open	Not used	
short	short	Not used	

2.1) Power of the spindle motor is controlled by the MOTOR ON signal.

2.2) Power of the spindle motor is controlled by the drive select conditions that have been selected by DRIVE SELECT # - 3 signal.

Table of Shorting Plugs

Type of switching	Object	Name	Contents	Display	Name of short plug
Shorting by plugs	Selection of drive select	[DS0]	DRIVE SELECT 0		PM1
		[DS1]	DRIVE SELECT 1		
		[DS2]	DRIVE SELECT 2		
		[DS3]	DRIVE SELECT 3		
		MX	The DRIVE SELECT which is usually set		
	Selection of MOTOR ON conditions	[MM MS]	Motor started by DRIVE SELECT		PM2
		[MM MS]	Motor started by MOTOR ON		
		[MM MS]	Motor started by MOTOR ON or DRIVE SELECT		
		[MM MS]	(Not used)		

Note 1: The enclosed setting options are factory set at time of shipping.

User setting option locations

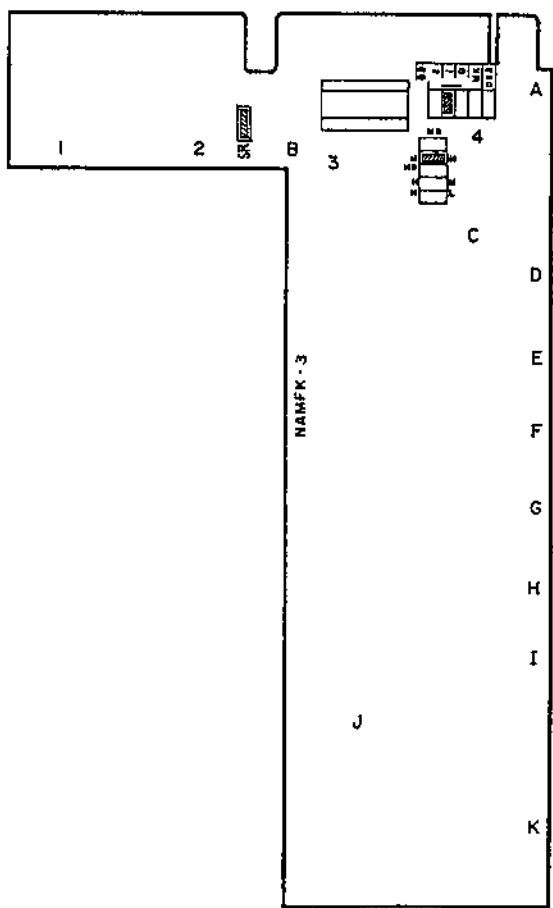


Fig. 3-3

### 3.1.4 Input signal lines

The disk drive has 11 input signal lines. Input signals can be classified into two types: One is multiplexed in a multi-drive system; and the other performs a multiplex operation.

The multiplexing signals are as follows:

- o Drive select 0
- o Drive select 1
- o Drive select 2
- o Drive select 3

#### (1) Drive select 0 to drive select 3

When these drive select lines are at logical "0" level, a multiplexed I/O lines become active to enable read/write operation. These four separate input signal lines, drive select 0 to drive select 3, are provided for connecting four drives to one system and mutually multiplexing them. Jumper pins DS0, DS1, DS2, and DS3 on the printed-circuit board are used to select drives to be made active, corresponding to drive select lines.

DS1 - DS0 is shorted before shipment from the factory, so this setting must be changed when establishing other select lines.

#### (2) Side one select

This interface line is used to select which of the two sides of the diskette should be read or written. When this line is at logical "1," the Side 0 head is selected; or when it is at logical "0," the Side 1 head is selected. If the polarity of the side one select signal is reversed, delay read/write operation by more than 100  $\mu$ s before execution.

Upon completion of a write operation, reverse the polarity of the side one select signal after a delay of 1000  $\mu$ s. The heads are tunnel erase type, with a physical core gap deviation between the read/write head and the erase heads so with no delay, non-erased areas would be generated on the diskette due to a timing difference between the write data area and the erase area during write operation. This is prevented by delaying the erase current ON/OFF time of a 1000 microseconds within the disk drive. Therefore, the head select must not be reversed during this delay time. Also, the track access action must not be permitted for 1000  $\mu$ s.

(3) Direction select

This interface line controls the direction. (inward or outward) in which the read/write head should be moved when a step signal pulse is applied.

If the signal is at logical "1," the read/write head moves from the center of the diskette outward; if it is at logical "0," the head moves inward.

(4) Step

This interface line is a pulse signal for moving the read/write head in the direction defined by the direction select line. The read/write head moves by one track each time a signal pulse is applied to the step line. The step line is normally logical "1," and the step operation starts with the trailing edge of a negative-going pulse (reversal from logical "0" to logical "1").

The direction select line must be reversed more than 1  $\mu$ s before the trailing edge of the step pulse.

(5) Write gate

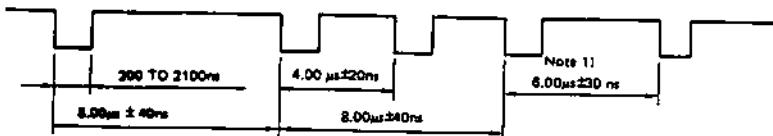
When this interface line goes to logical "0," the write driver becomes active and the data given to the write data line is written on the selected side of the diskette. When the interface line goes to logical "1," the write driver becomes inactive to enable the read data logic. The verified read data is obtained 1000  $\mu$ s (maximum) after the write driver becomes inactive. Refer to CHAPTER 4 for the timing.

(6) Write data

Data to be written on the diskette is sent to this interface line.

This line is normally at logical "1," and reverses the write current at the leading edge of a negative-going data pulse (reversal from logical "1" to logical "0") to write data bits.

This line is enabled when the write gate is at logical "0." Fig. 3-4 shows the write data timing.



Note 1) The timing for 6.00 $\mu$ s is MFM only.

Fig. 3-4 Write Data Timing (FM, MFM Encoding)

(7) In use

An LED indicator on the front panel lights when this interface line goes to logical "0." The LED is also lit by the drive select.

(8) Motor on

This interface line starts the spindle motor when it goes to logical "0." The write gate does not go to logical "0" until more than 250 ms after the motor-on line goes logical "0."

The motor-on line goes logical "1" to stop the motor and keep it off while the drive is out of operation, thus prolonging motor life.

### 3.1.5 Output signal lines

The drive has five standard output signal lines.

(1) Index

This interface line is normally logical "1" but sends a logical "0" output pulse 4 ms wide each time the diskette makes one revolution (200 ms period).

This signal signifies the start of a track on the rotating diskette. The index signal timing is shown in Fig. 3-5.

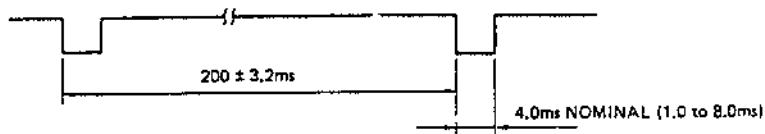


Fig. 3-5 Index Timing

(2) Track 00

When this interface line is at logical "0," it indicates that a read/write head of the selected drive is positioned on track 00. If the output of the selected drive is at logical "1," it indicates that the read/write head is positioned on a track other than track 00.

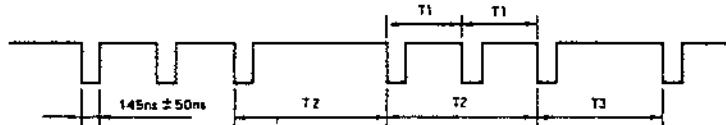
(3) Ready

This interface line is the line goes logical "0" (ready) if an index pulse is detected twice or more when the index hole is correctly detected, and the DC power (+5 V and +12 V) supplied after a diskette is inserted into the drive and the door is closed.

(4) Read data

This interface line reads the data stored on the diskette with the read/write heads, and outputs raw data (combined clock and data signals) converted into pulse signals by an electronic circuit.

The read data line is normally logical "1" but it sends a logical "0" (negative-going) output pulse during a read operation. Fig. 3-6 shows allowable limits on timing variations with the usual diskette and bit shifts.



T<sub>1</sub> = 4.00μs ± 800ns (Jitter due to rotation variation excluded)  
T<sub>2</sub> = 8.00μs ± 1.6μs (Jitter due to rotation variation excluded)  
T<sub>3</sub> = 6.00μs ± 1.2μs (Jitter due to rotation variation excluded)

Fig. 3-6 Read Data Timing (FM Encoding)

(5) Write protect

This interface signal notifies the host system of the insertion of a diskette with a write protect notch into the drive. The signal goes to logical "0" when a write-protected diskette is inserted into the drive. When the signal is at logical "0," write on the diskette is inhibited even if the write gate line becomes active.

### 3.2 Power Interface

The disk drive requires two types of DC power supplies.

One is +12 V DC, which drives the drive motor to rotate the disk. It is supplied to the stepping motor and the read/write circuit. The other is +5 V DC, which is used for the logic circuit and the read/write circuit.

#### NOTE

The index LED is driven by the +5 V DC.

##### 3.2.1 DC power

DC power is supplied via connector J2/P2 on the back of the printed-circuit board. The specifications of the two DC voltages are shown in Table 3-3. The pin arrangement of connector J2/P2 is shown in Table 3-1.

Table 3-3 DC Power Specifications

DC voltage	Voltage variation	Current	Maximum ripple voltage (peak-to-peak)
+5 V DC	±0.25 V (±5%)	0.7 A maximum 0.4 A typical	50 mV
+12 V DC	±0.6 V (±5%)	1.00 A maximum 0.3 A typical at seek	100 mV

## CHAPTER 4 FUNCTIONAL OPERATION

### 4.1 Power On Sequencing

No read/write operation may be performed during the period of 100 ms or more from the start of DC power supply until the control signal stabilizes. And after the period of 600ms from the Motor On, the drive comes to ready. The read/write head may have been positioned on an incorrect track after switching the DC power on, so before starting a read/write operation, be sure to perform the step out operation until a track 00 signal is output to the interface line, and thus correctly position the read/write head.

Note: There is no specified power input order for + 12 V and + 5 V.

### 4.2 Drive Selection

The disk drive daisy chain cabling system permits connection of multiple drives to a single cable.

These drives are selected when the drive select lines on the drive side become active. Only the drive whose drive select line is active sends and receives signals to and from the host system. The select lines on the drive must have different numbers if two or more drives are connected. If the same number is assigned, an operation error occurs due to interference among the interface output signals of the drives themselves.

### 4.3 Positioning Operation

The seek operation which moves the read/write head to the desired track selects a direction, inward or outward, depending on the polarity of the direction select signal, and moves the head by the step signal. If access to a track two or more tracks away is required, step pulses are continuously sent until the head moves to the desired track.

Head movement starts with the trailing edge of the step pulse. Fig. 4-1 Shows the operation timing.

### 4.4 Side One Selection

The read/write heads located on both sides of the diskette are selected by the side one select signal. When the side one select line is high, the Side 0 head is selected. When it is low, the Side 1 head is selected.

#### 4.5 Read Operation

The required timing for read operations is shown in Figs. 4-1 and 3-5. These timing specifications are necessary for accurate read operation.

Two modes of encoding, FM and MFM, are used for the data stored on media. FM is used for single-density read, and MFM for double-density read.

A comparison of the FM and MFM encoding modes is shown in Fig. 4-3.

#### 4.6 Write Operation

The requiring timing for write operation is shown in Fig. 3-3.

These timing specifications must be strictly observed to ensure an accurate write operation.

Write data can be encoded by either FM or MFM. The disk drive has good contact stability of the read/write heads on the medium and employs high-performance read/write heads, so no precompensation is necessary for correcting the peak shift effect when writing data in the MFM mode (double density).

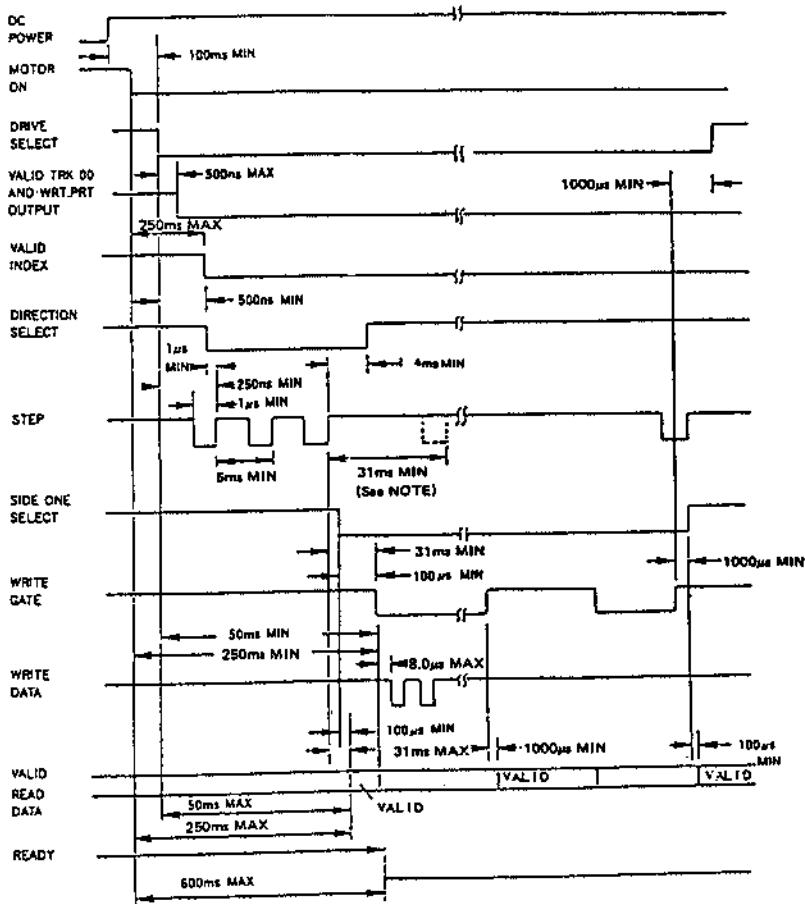
#### 4.7) READY and operation of the dynamic clamp

The timing of the dynamic clamp, standerd READY, and standard READY is shown in Diagram 4.2.

##### Dynamic clamp function

When the disk is inserted into the unit, the two needed.

When the disk is inserted into the unit, the two steps of first inserting and then closing the door are needed. The Micro switch detects the operation of the knob lever and forcibly causes the spindle motor to rotate. The forcible rotation mode will be canceled after one second.



Note : When reversing direction, issue a next step pulse after more than 31ms from the step pulse before inversion.

Fig. 4-1 Control and Data Timing

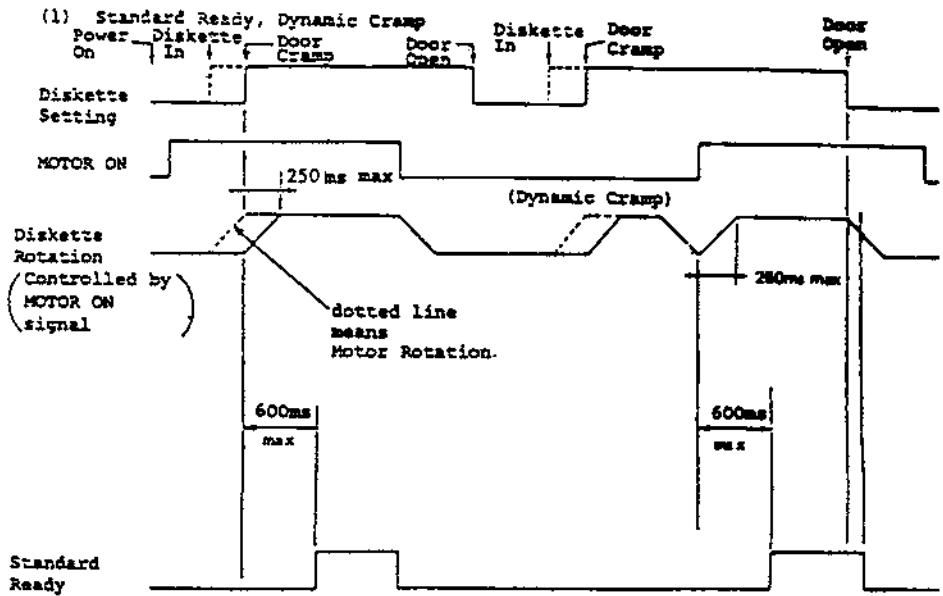


Fig. 4-2 Ready and Dynamic Cramp Timing

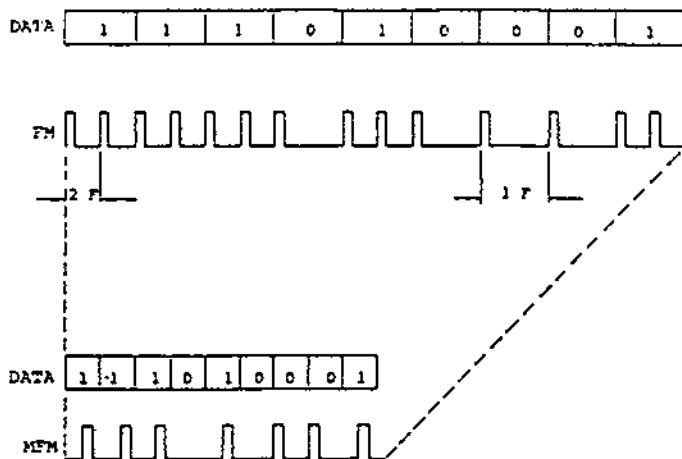


Fig. 4-3 Comparison of FM and MFM Encoding Systems

## CHAPTER 5 PHYSICAL INTERFACE

Electronic interfaces between the disk drive and the host system are accomplished with three connectors. Connector J1 is for the signal interfaces, connector J2 for the DC power supplies, and connector J3 for frame grounding. The connectors used for the disk drive and recommended mating connectors are described below.

### 5.1 Signal Connectors

J1 is a card-edge type, 34-pin (for both sides, or 17 pins for a single side) connector with even-numbered pins (2, 4, to 34) on the parts side and odd-numbered pins (1, 3, to 33) on the soldered side.

A key slot is provided between pins 4 and 6 for the polarity reversal prevention.

The dimensions of J1 are shown in Fig. 5-1.

Recommended PL connectors that mate with J1 are shown in Tables 5-1 and 5-2.

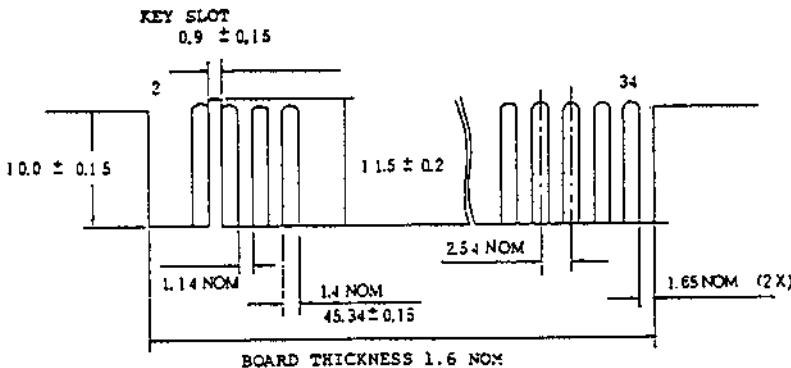


Fig. 5-1 Connector J1 Dimensions (mm) and Pin Numbers

Table 5-1 Connectors for Twisted-Pair Cable (Pl)

Parts	Crimp Type	Solder Type
	AMP P/N	AMP P/N
Housing	583717-5	583717-5
Contact	1-583616-1	583854-3
Polarity key	583274-1	583274-1
Crimping tool	90268-1	-
Extraction tool	91073-1	91073-1
Twisted-pair cable (3 m max.)	AWG 26	AWG 26

Table 5-2 Connector for Flat Cable (Pl)

Parts	3M P/N	
Connector	3463-0001	
Polarity key	3439-0000	
Crimping tools	Press	3440
	Locator plate	3443-11
	Platen	3442-3
Flat cable (3 m max.)	3365/34	

Items that can be used in conjunction with a connector for the flat cable.

Parts	HIROSE P/N
Connector	HIF5D-34DA-2.54R
Polarity key	CR7C-GPIN

(Items such as a fusing tool. For details refer to the manufacturers of the connector.)

### 5.2 DC Power Connector (J2/P2)

P 2 is a four-pin DC power connector made by JST, located on the back of the printed-circuit board. Pin 4 on connector P 2 is located closest to J1/P1; the arrangement of the pins as viewed from the side is shown in Fig. 5-2.

The connectors on the drive side and cable side are shown in Table 5-3.

Table 5-3 DC Power Connectors

Parts	J 2 (Cable Side)	P 2 (Drive Side)
	AMP P/N	JST P/N
Housing	1-480424-0	LC-04A
Contact (4 pins)	60619-1	-
Crimp tool	90124-2	-
Extraction tool	1-305183-2	-
Cable (3 m max.)	AWG 18	-

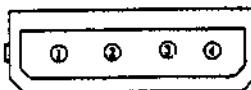


Fig. 5-2 Connector J2

### 5.3 Frame Ground Connector (J5/P5)

FASTON Terminal	Crimp Terminal
AMP P/N 60920-1	AMP P/N 60972-1

#### 5.4 Interface Connector Physical Location

Fig. 5-3 shows the physical locations of the interface connectors.

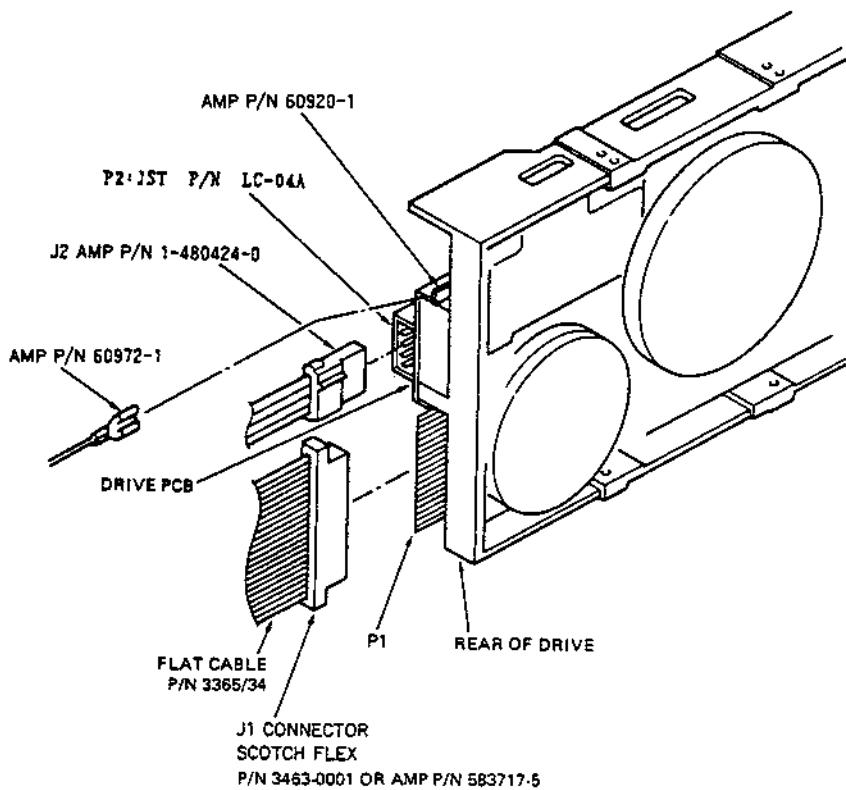


Fig. 5-3 Location of Interface Connectors

## CHAPTER 6 DRIVE PHYSICAL SPECIFICATIONS

### 6.1 Installation Direction

Install the Mini Flexible disk drive in the directions shown in Fig. 6-1.

The slant mount should be within 10 degrees.

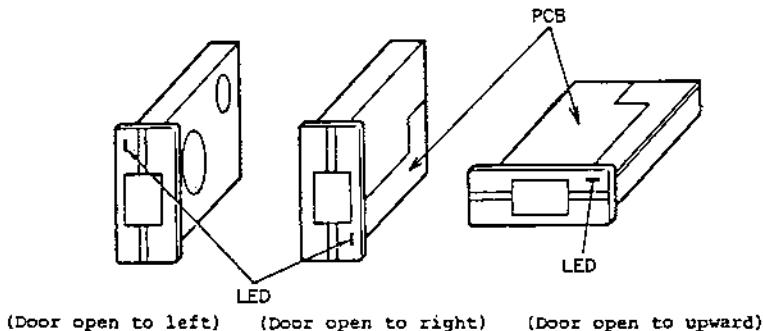


Fig. 6-1 Disk Drive Installation Directions

### 6.2 Dimensions of disk drive

See Fig. 6-2.

### 6.3 Dimensions of Front Panel

See Fig. 6-3.

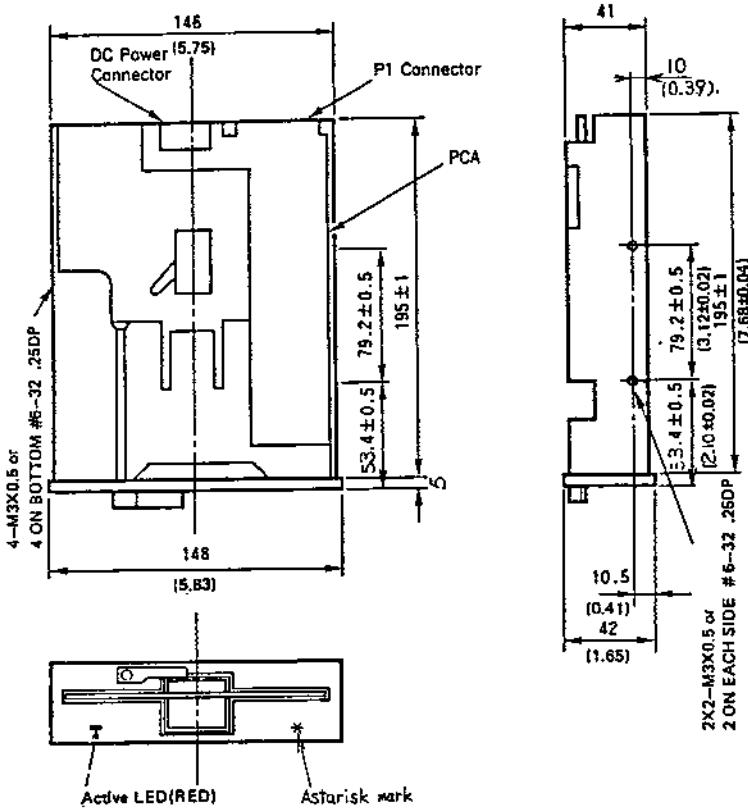


Fig. 6-2 Disk Drive Dimensions

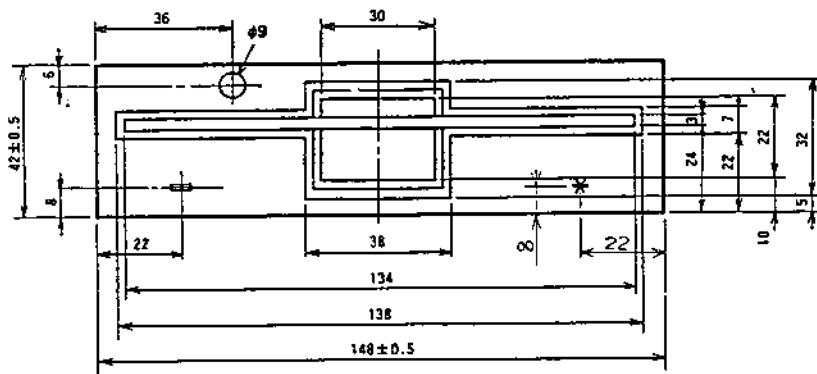


Fig. 6-3 Front Panel Dimensions

## CHAPTER 7      ERROR DETECTION AND CORRECTION

This chapter describes the general cause analysis and corrective procedures to be followed in the event that data errors occur.

### 7.1    Write Errors

If an error occurs during a write operation, it can be detected by performing a read operation on the diskette rotation immediately following the write operation. This is generally called a write check, which is an effective means of preventing write errors. It is recommended, therefore, that a write check be made without fail.

If a write error occurs, repeat the write operation and conduct a write check. If data cannot be correctly written even after the write operation is repeated about ten times, perform a read operation on another track to determine whether the data can be read correctly. If so, a specific track of the diskette is defective. If data cannot be correctly read on the other track, the drive is assumed to have some trouble. If the diskette is defective, replace it.

### 7.2    Read Errors

Most data errors that occur are soft errors. If a read error occurs, repeat the read operation to recover the data.

The following are possible main causes of soft errors:

- o Dust is caught between the read/write head and diskette causing a temporary fault in head contact. Such dust is generally removed by the self-cleaning wiper of the jacket, and the data is recovered by the next re-read operation. If read/write is continued for a long time in a very dusty environment, however, hard errors can result from a damaged diskette surface.
- o Random electrical noise ranging in time from a few microseconds to a few milliseconds can also cause read errors. Spike noise generated by a switching regulator, particularly one that has short switching intervals, deteriorates the signal-to-noise ratio, and increases the number of re-read operations for data recovery. It is necessary, therefore, to make an adequate check on the noise levels of the DC power supplies to the drive and frame grounding.
- o Written data or diskettes may have so small a defect as cannot be detected by a data check during write operation.
- o Fingerprints or other foreign matter on a written diskette can also cause a temporary error. If foreign matters is left on a

written diskette for a long time, it can adhere to the diskette, possibly causing a hard error.

It is recommended that the following read operations be performed to correct these soft errors:

- o Step 1: Repeat the read operation about ten times until the data is recovered.
- o Step 2: If the data cannot be recovered by Step 1, move the head to other track, the opposite direction of the previous track position before the designated track, and then return the head to the original position.
- o Step 3: Repeat an operation similar to Step 1.
- o Step 4: If the data cannot be recovered, take the error as a hard error.

## CHAPTER 8 RESHIPMENT PRECAUTIONS

When reshipping the drive, make sure the protection sheet for transportation is in place in the drive, and open the door.



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MODEL 3000 FDC/HDC CONTROLLER BOARD

I. Theory of Operation

Overview (Not Available)

II. Jumper Settings

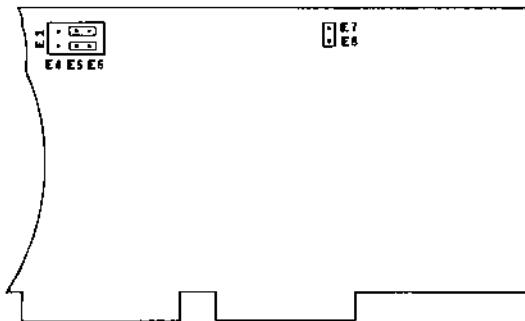
III. Schematics

IV. WD1002-WA2 Assembly and Parts List



**Hard Disk Controller Board  
Jumper Settings**

1. Check to be sure that E5 is jumpered to E1, E6 is jumpered to E1 and E7 is jumpered to E8 on the Hard Disk Controller board (see Figure 1) to be sure they are set as shown.



**Figure 1 Jumper Settings.**



WD1002-WA2 Assembly

Symbol	Description	Part No.
	Bracket I/O MTG OPT	
	Cap, Cer. 0.015MF 10%	
	Cap, Cer. 3900PF 5% 5	
	Cap, Tant 1MF 10% 35	
	IC, 74ALS245 Octal B	
	Socket, IC Dip-28 LO	
	PCB WD1002-WA2 (4 L)	
	POT TRMR 5K 10% 0.5W	
	Res, MF 1.00K 1% 1/8	
	Res, MF 1.18K 1% 1/8	
	Res, MF 6.98K 1% 1/8	
	Res, CF 51 Ohm 5% 1/	
	Res, MF 8.25K 1% 1/8	
	Screw Pan HD #4-40X	

Symbol	Description	Part No.
C1,8,11	Cap, Cer. 0.01MF +80-2	
C2,40	Cap, Cer. 150PF 5% 50	
C3	Cap, Cer. 4700PF 5% N	
C4,6	Cap, Cer. 180PF 5% NP	
C5	Cap, Cer. 1000PF 5% 5	
C7	Cap, Cer. 68PF 5% 50V	
C9	Cap, Cer. 100PF 5% NP	
C10	Cap, Cer. 120 PF 5% 50	
C12	Cap, Tant 10MF 20% 2	
C13,57	Cap, Tant 1MF 10% 35	
C14-16,19-20, 23-26,31-33, 35-39,41, 43-45,47, 50-55	Cap, Cer. 0.1MF +80-20	
C17	Cap, Cer. 470PF 5% 50	
C18	Cap, Cer. 0.1MF 10% 50	
C21-28	Cap, Var 7-60PF 0.220	
C22	Cap, Cer. 120PF 5% 50	
C24	Socket IC Dip-20 LO	
C27	Cap, Cer. 150PF 5% 50	
C29	Cap, Tant 2.2MF 20%	
C30	Cap, Cer. 0.22MF +80-2	
C34	Cap, Cer. 68PF 5% 50V	
C42	Cap, Tant 4.7MF 20%	
C46	Cap, Cer. 22PF 5% 50V	
C48-49	Cap, Cer. 47PF 5% 50V	
C56	Cap, Elect 22MF +50-	
CR2	Diode Var 1-9V MVAM	
CR3-9	Diode 1N4148 SW 0.15	
E1-6	Conn Post HDR 6 Pin	
E2-3	Conn Jumper 2 SKT	
E5-6	Conn Jumper 2 SKT	
E7-8	Conn Jumper 2 SKT	
J1,5	Conn Post HDR 34 Pin	
J3,4	Conn Post HDR 20 Pin	
J6	Conn Post HDR 4 Pin	

Symbol	Description	Part No.
L1	Inductor 4.7UH 1% A	
L2	Ferrite Bead	
L3	Inductor 4.7UH 10%	
Q1-6	Trans PNP 2N3906 40	
Q7-9	Trans NPN 2N3904 40	
R1	Res, MF 750 Ohm 1% 1	
R2	Res, MF 1.50K 1% 1/8	
R4,47,49	Res, CF 220 Ohm 5% 1	
R6	Res, CF 100K 5% 1/4W	
R7	Res, MF 3.57K 1% 1/8	
R8	Res, MF 15K 1% 1/8W	
R9	Res, CF 270 Ohm 5% 1	
R10,21-22,25	Res, CF 4.7K 5% 1/4W	
R11,41,51-55	Res, CF 2K 5% 1/4W	
R12	Res, CF 22 Ohm 5% 1/	
R13	Res, MF 475 Ohm 1% 1	
R14	Res, MF 1.21K 1% 1/8	
R15,16	Res, MF 1Meg 1% 1/8W	
R17,18	Res, CF 100 Ohm 5% 1	
R19,20	Res, CF 430 Ohm 5% 1	
R23-24,26	Res, CF 3.3K 5% 1/4W	
R27,36,38-40	Res, MF 17.8K 1% 1/8	
R28	Res, MF 4.02K 1% 1/8	
R29,58	Res, CF 120 Ohm 5% 1	
R30	Res, MF 3.48K 1% 1/8	
R31	Res, MF 1.74K 1% 1/8	
R32	Res, MF 4.75K 1% 1/8	
R33	Res, MF 5.62K 1% 1/8	
R34	Res, MF 6.19K 1% 1/8	
R35	Res, MF 12.7K 1% 1/8	
R37	Res, MF 105K 1% 1/8W	
R42	Res, MF 100 Ohm 1% 1	
R43	Res, MF 487 Ohm 1% 1	
R44,48	Res, CF 1.2K 5% 1/4W	
R45	Res, CF 27K 5% 1/4W	
R46	Res, CF 330 Ohm 5% 1	
R50	Res, CF 680 Ohm 5% 1	
R56	Res, CF 22 Ohm 5% 1/	
R57	Res, MF 2.43K 1% 1/8	

Symbol	Description	Part No.
U1	Delay Line 96NS STA	
U2	GA WD10C20-05 (F) M	
U3	IC WD1014-01 ERROR	
U4,15	IC 7406 Hex Inv/Buf	
U5,7,11	IC 7438 Quad 2-IN N	
U6	IC 9638 DUAL DIFF L	
U8	IC OP AMP LF411 JFE	
U9	IC 74LS74 Dual D ED	
U10	IC MC3486 Dual Diff	
U12	IC TPQ6700 2NPN/2PN	
U13	IC 74LS629 Dual VCO	
U14	IC WD1010A-05 WNCST	
U16-17,52	IC 74LS14 Hex Invrt	
U18	IC 74S74 Dual D EDG	
U19	IC 74LS175 Quad D F	
U20,29,37	IC 74LS373 Octl D L	
U21	IC 74LS174 Hex D ED	
U22	IC 26S02 DUAL RETRI	
U23	IC 74S113 Dual JK F	
U24	IC WD2293-07 RDRNR	
U25	IC UPD765 DISK CNTL	
U26,42	IC 74LS00 Quad 2-IN	
U27	IC 74LS04 Hex Inver	
U28	IC Mask HAL for RR	
U30	IC Mask HAL for RR	
U31	IC 74LS155 Dual 2-4	
U32	IC 74F74 Dual EDG T	
U33	IC 74LS221 Dual Ret	
U34	IC WD2293-08 RDRNR	
U36	IC MC3487 Dual Diff	
U38,47	IC RAM 2KX8 STATIC	
U39,48,54,56	IC 74LS245 Octl Bus	
U40,49	IC 74LS367 Hex Bffr	
U41	IC 74S00 Quad 2-IN	
U43	IC 74LS112 Dual JK	
U44	IC 74S196 4Bit Deca	
U45	IC WD1015-03 Mask	
U46,55	IC 74LS393 4Bit Dua	
U50	IC 74LS126 Quad Buf	
U51	IC 74LS08 Quad 2-IN	
U53	IC 74S30 8-IN Nand	
VRL	IC Volt LReg 78M05 +	
VRL	Pad Transtr Mtg T05	
Y1,3	Crystal 10Mhz 0.01%	
Y2	Oscillator 24Mhz 0.1	
Z1	Res, Ntwk 220/330 28	
Z2	Res, Ntwk 1.5K 28 1/	
Z3	Res, Ntwk 150 Ohm 28	
Z4	Res, Ntwk 220 Ohm 28	

\*\*\*\*\*  
\*                   20 Meg. Fixed Disk       \*  
\*    \*  
\*    \*  
\*\*\*\*\*

November 15, 1985



**20 Meg. Mitsubishi MR522 and Seagate ST225  
5.25" Hard Disk Drives**

The Tandy 3000 optional hard disk drive has a capacity of 20 Megabytes. Being a standard half height configuration this drive can fit in the same space as a standard half high floppy disk drive. This allows the hard disk drive to be built in to the computer as easily as a floppy drive. Up to two hard disk drives can be installed in the Tandy 3000.

Contents	Section
MR522 Normal Jumper Settings	1
MR522 Schematics and Component Layout	2
MR522 Maintenance Manual	3
MR522 Standard Specifications	4

**ST225 OEM Manual**



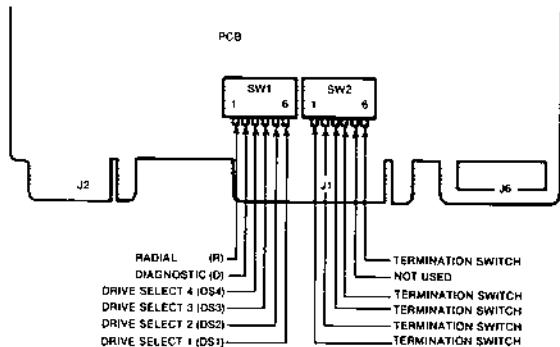
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\* \*  
\* \*  
\* 20 Meg. Fixed Disk \*  
\* \*  
\* Section 1 \*  
\* \*  
\* Jumper settings \*  
\* \*  
\*\*\*\*\*

November 15, 1985



## Setting Up the MR522 Drive

Check the settings on the dip switches near the back edge of the PCB on the bottom of the hard disk drive (see Figure 1) to be sure they are set as shown.



	SW1 (Switch Block 1)						SW2 (Switch Block 2)					
	1	2	3	4	5	6	1	2	3	4	5	6

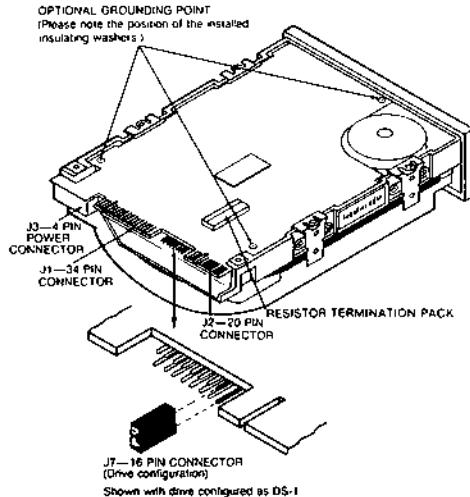
First      On Off Off Off Off On      On On On On On  
Internal HD

Second     On Off Off Off On Off     Off Off Off Off Off Off  
Internal HD

Figure 1. MR522 Hard Disk Drive  
PCB Dip Switch Settings.

## Setting Up the ST225 Drive

Check the position of the jumper on the back edge of the PCB on the bottom of the hard disk drive (see Figure 2) to be sure the jumper is set to the desired position.



First Internal HD	1	3	5	7	9	11	13	15	Terminal
	2	4	6	8	10	12	14	16	Resistor Installed
Second Internal HD	1	3	5	7	9	11	13	15	Terminal
	2	4	6	8	10	12	14	16	Resistor Removed
Radial				Life	DS4	DS3	DS2	DS1	
Recovery Mode				Write Fault					

Figure 2. ST225 Hard Disk Drive  
PCB Jumper Setting.

When installing a Seagate drive as the second hard disk drive the termination resistor should be removed from the drive prior to installation.

\*\*\*\*\*  
\*  
\*  
\* 20 Meg. Fixed Disk  
\*  
\* Section 2  
\*  
\* Schematics & Component layout \*  
\*\*\*\*\*

November 15, 1985





S06-G30080A

**MITSUBISHI  
5.25 INCH  
FIXED DISK DRIVE  
MR 521/MR 522-U24**

**LOGIC AND  
SCHEMATIC DRAWINGS**

 **mitsubishi electric corporation**



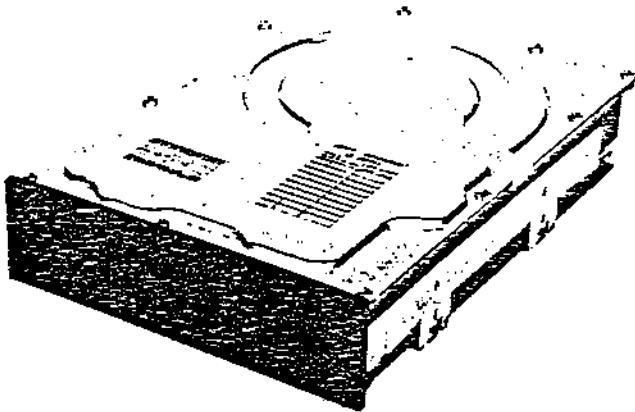
Rev.	Page	Section	Description/Reason	Note	Date & Approved
A	-	-	S06-G30080A	1st Edition	August 1, 1985

(Notice) This manual may be revised without notice. Please contact Mitsubishi Electric Corporation for the latest version when using this manual for design purposes.



MRS21/NRS22 5.25 INCH FIXED DISK DRIVE

LOGIC AND SCHEMATIC DRAWINGS  
(P/N. 6C449583)  
(12.75 MB/25.5 MB)



 MITSUBISHI ELECTRIC CORPORATION

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5. SCHEMATICS .....	1	



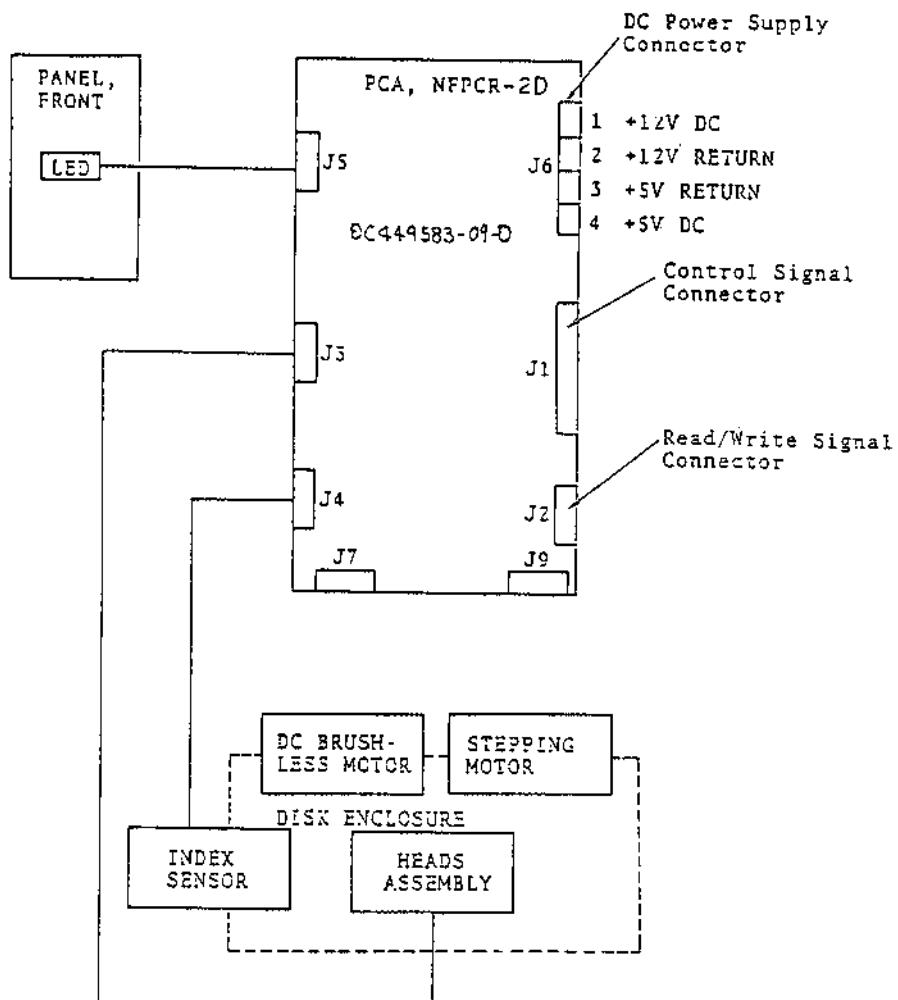


Fig. 1 WIRING DIAGRAM

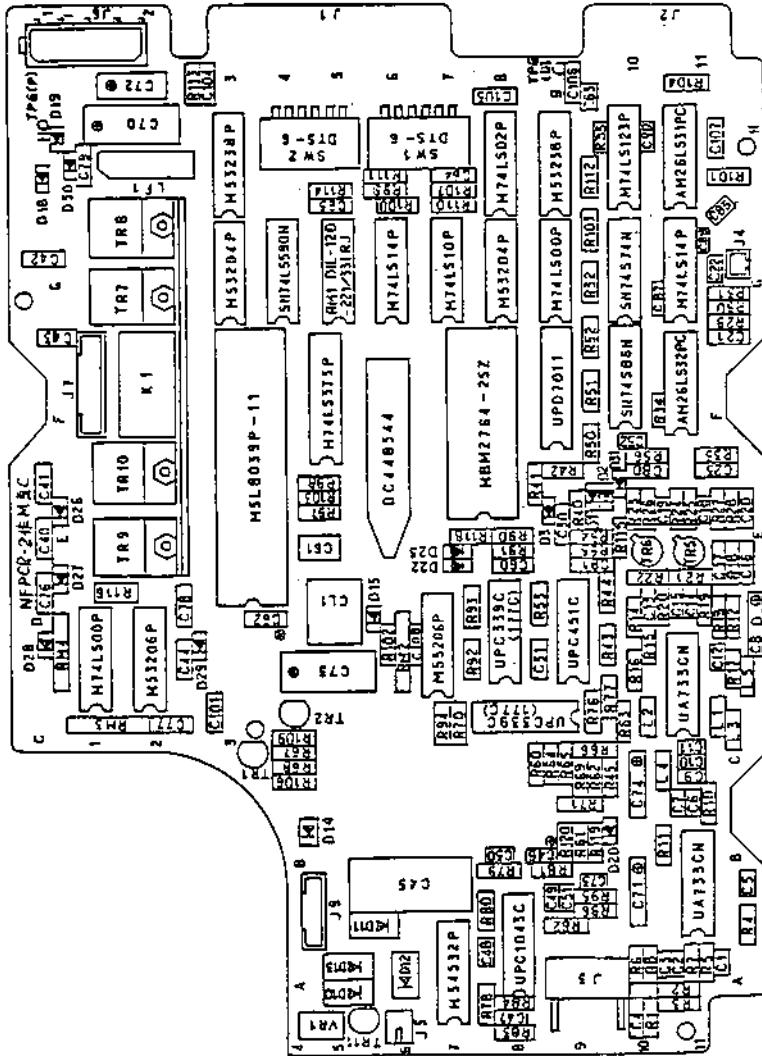


Fig. 3 PARTS LOCATION DIAGRAM

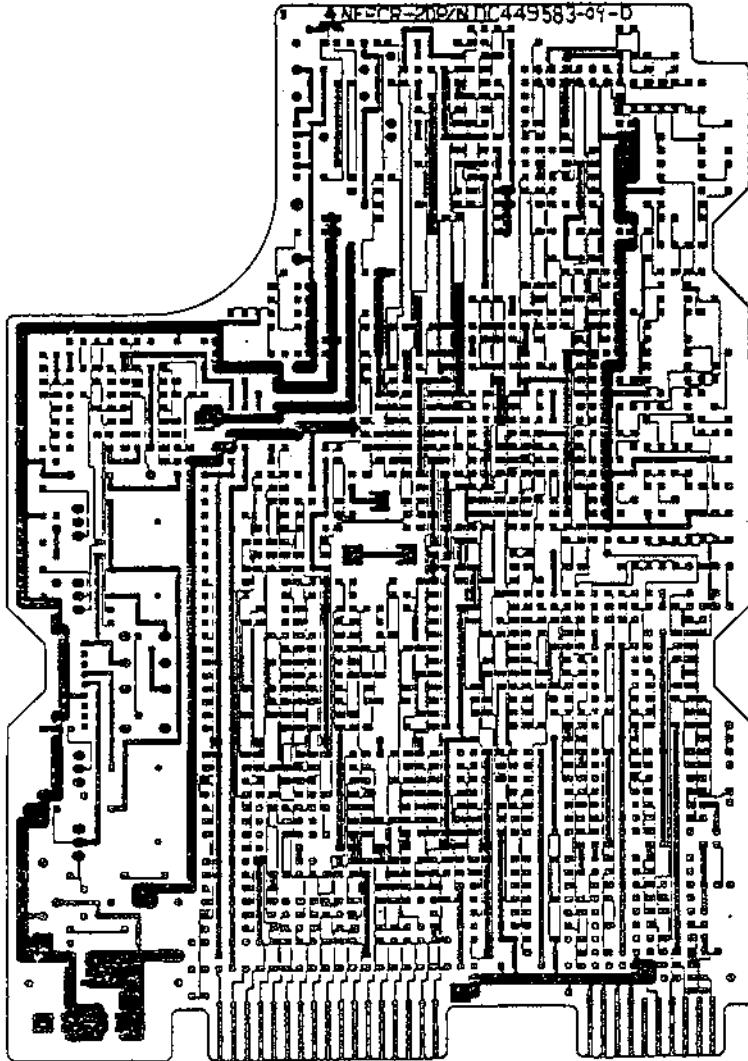


Fig. 3 LOCATION OF PART NUMBER

PARTS LIST

Symbol (Location)	Description	Part Number	Q'ty	Notes
J3	Connector, PWB	PS-I2PE-D4LTi-PN1	1	
J4	Connector, PWB	IL-S-2P-S2T2-EF	1	
J5	Connector, PWB	IL-S-2P-S2L2-EF	1	
J6	Connector, PWB	350211-1	1	
J7	Connector, PWB	IL-S-9P-S2T2-EF	1	
J8	Connector, PWB	IL-S-6P-S2T2-EF	1	
TPG(D)(H09)	Terminal	CT-1-1	1	
TPG(D)(H01)	Terminal	CT-1-1	1	
* (F06)	Printed Circuit Board Discharger, Assy	DC448544-G02	1	Foot Note 1
(E02)	Heat Sink, TR	DC449160-001	1	for TR7--TR10
	Insulation Sheet, NFPCR	DC449163-001	1	for TR7--TR10
	Silicon Sheet	DC448602-001	4	for TR7--TR10
	Insulation Bush	B17(25K Bushing)	4	for TR7--TR10
	Screw	DC445516-002	4	for TR7--TR10
	Washer	PLAIN-FE-M3	4	for TR7--TR10
	Nut	HEX-FE-M3x0.5	4	for TR7--TR10

Note 1: Electronic components on printed circuit board shall not be supplied for spare part. Values of electric parameters are reference only.

Symbol (Location)	Description	Part Number	Q'ty	Notes
(D04)	IC, MOS	M5L8039P-1I	1	P8039AHL
(F08)	IC, EPROM	MBM2764-Z25	1	DC346002EPROM
(D01)	IC, Digital	M74LS00P	1	SN74LS00N
(G09)	IC, Digital	M74LS00P	1	SN74LS00N
(H08)	IC, Digital	M74LS02P	1	SN74LS02N
(G07)	IC, Digital	M74LS10P	1	
(G06)	IC, Digital	M74LS14P	1	SN74LS14N
(G11)	IC, Digital	M74LS14P	1	
(G10)	IC, Digital	SN74S74N	1	
(H10)	IC, Digital	M74LS123P	1	SN74LS123N
(F05)	IC, Digital	M74LS373P	1	SN74LS373N
(G04)	IC, Digital	SN74LS590N	1	
(G03)	IC, Digital	M53204P	1	
(G08)	IC, Digital	M53204P	1	
(D02)	IC, Digital	M53206P	1	SN7406N
(D07)	IC, Digital	M53206P	1	SN7406N
(H03)	IC, Digital	M53238P	1	SN7438N
(H09)	IC, Digital	M53238P	1	SN7438PC
(F10)	IC, Digital	SN74S86N	1	
(H11)	IC, Linear	AM26LS31PC	1	AM26LS31DC
(F11)	IC, Linear	AM26LS32PC	1	AM26LS32DC
(A07)	IC	M54532P	1	
(F09)	IC, Linear	UPD7011C	1	
(B11)	IC, Linear	UA733CN	1	
(D11)	IC, Linear	UA733CN	1	
(C09)	IC, Linear	UPC339C	1	UPC177C
(D08)	IC, Linear	UPC339C	1	UPC177C
(D09)	IC, Linear	UPC451C	1	UPC324
(A08)	IC, Linear	UPC1043C	1	

Symbol (Location)	Description	Part Number	Q'ty	Notes
C1 (A11)	Capacitor, Ceramic	RPE122-127C104K50	1	
C2 (A11)	Capacitor, Ceramic	RPE122-127C104K50	1	
C3 (A11)	Capacitor, Ceramic	RPE122-127C104K50	1	
C4 (A10)	Capacitor, Ceramic	RPE123-127F155Z25	1	
C5 (B11)	Capacitor, Ceramic	RPE122-127C223K50	1	
C6 (C11)	Capacitor, Ceramic	RPE122-127C223K50	1	
C7 (C11)	Capacitor, Ceramic	RPE122-127C223K50	1	
C8 (D11)	Capacitor, Tantalum	CS02H1C220M	1	
C9 (C11)	Capacitor, Ceramic	RPE122-127CH101J50	1	
C10(C11)	Capacitor, Ceramic	RPE122-127CH351J50	1	
C11(C11)	Capacitor, Ceramic	RPE122-127CH680J50	1	
C12(D11)	Capacitor, Ceramic	RPE122-127CH151J50	1	
C13(D10)	Capacitor, Ceramic	RPE123-127F153Z25	1	
C14(D11)	Capacitor, Ceramic	RPE122-127CH470J50	1	
C15(D11)	Capacitor, Ceramic	RPE122-127CH470J50	1	
C16(E11)	Capacitor, Ceramic	RPE123-127F153Z25	1	
C17(E11)	Capacitor, Ceramic	RPE123-127F153Z25	1	
C18(E11)	Capacitor, Ceramic	RPE122-127C104K50	1	
C19(E11)	Capacitor, Ceramic	RPE122-127C104K50	1	
C20(E11)	Capacitor, Ceramic	RPE122-127CH330J50	1	
C21(F11)	Capacitor, Ceramic	RPE123-127F133Z25	1	
C22(G11)	Capacitor, Ceramic	RPE122-127CH471J50	1	
C23(F11)	Capacitor, Ceramic	RPE122-127CH471J50	1	
C30(E09)	Capacitor, Ceramic	RPE122-127CH681J50	1	
C31(D09)	Capacitor, Tantalum	244M1602-333M	1	
C32(F10)	Capacitor, Ceramic	RPE122-127C104K50	1	

Symbol (Location)	Description	Part Number	Q'ty	Notes
C40 (E01)	Capacitor, Ceramic	RPE123-127F155Z25	1	
C41 (E01)	Capacitor, Ceramic	RPE123-127F155Z25	1	
C42 (G01)	Capacitor, Ceramic	RPE123-127F155Z25	1	
C43 (F01)	Capacitor, Ceramic	RPE123-127F155Z25	1	
C44 (D03)	Capacitor, Ceramic	RPE123-127F155Z25	1	
C45 (B06)	Capacitor, Plastic	73IN2003-334K	1	
C46 (B09)	Capacitor, Tantalum	244M1602-335M	1	
C47 (A08)	Capacitor, Ceramic	RPE122-127C103K50	1	
C48 (A07)	Capacitor, Ceramic	RPE122-127C104K50	1	
C49 (B09)	Capacitor, Ceramic	RPE123-127F155Z25	1	
C50 (B08)	Capacitor, Ceramic	RPE122-127C223K50	1	
C51 (A09)	Capacitor, Ceramic	RPE122-127C103K50	1	
<hr/>				
C60 (E08)	Capacitor, Ceramic	RPE122-127C103K50	1	
C61 (E05)	Capacitor, Ceramic	RPE123-127F155Z25	1	
C62 (D03)	Capacitor, Tantalum	244M1602-33EM	1	
C63 (H09)	Capacitor, Ceramic	RPE122-127C682K50	1	
C64 (H07)	Capacitor, Ceramic	RPE122-127C103K50	1	
C65 (H05)	Capacitor, Ceramic	RPE122-127C104K50	1	
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C70 (H02)	Capacitor, Tantalum	CS02H1V220M	1	
C71 (E10)	Capacitor, Tantalum	CS02H1E100M	1	
C72 (H02)	Capacitor, Tantalum	CS02H1C220M	1	
C73 (B09)	Capacitor, Ceramic	RPE122-127C472K50	1	
C74 (C10)	Capacitor, Tantalum	CS02H1E100M	1	
C75 (C05)	Capacitor, Tantalum	CS02H1V220M	1	
C76 (D01)	Capacitor, Ceramic	RPE122-127C104K50	1	

Symbol (Location)	Description	Part Number	Q'ty	Notes
C77 (C02)	Capacitor, Ceramic	RPE122-127C104K50	1	
C78 (D02)	Capacitor, Ceramic	RPE122-127C104K50	1	
C79 (H01)	Capacitor, Ceramic	RPE122-127C104K50	1	
C80 (F10)	Capacitor, Ceramic	RPE123-127F155Z25	1	
C81 (E09)	Capacitor, Ceramic	RPE122-127CH471J50	1	
C85 (G11)	Capacitor, Ceramic	RPE122-127CH331J50	1	For adjustment
C87 (G11)	Capacitor, Ceramic	RPE122-127CH331J50	1	For adjustment
C88 (G11)	Capacitor, Ceramic	RPE122-127CH331J50	1	For adjustment
C90 (H10)	Capacitor, Ceramic	RPE122-127CH050D50	1	For adjustment
C101(C03)	Capacitor, Ceramic	RPE123-127F155Z25	1	
C103(G09)	Capacitor, Ceramic	RPE123-127F155Z25	1	
C104(H03)	Capacitor, Ceramic	RPE123-127F155Z25	1	
C105(H08)	Capacitor, Ceramic	RPE123-127F155Z25	1	
C106(H09)	Capacitor, Ceramic	RPE123-127F155Z25	1	
C107(H11)	Capacitor, Ceramic	RPE123-127F155Z25	1	
C108(D07)	Capacitor, Ceramic	RPE123-127F155Z25	1	
D1 (E09)	Diode	IS953	1	
D2 (E09)	Diode	IS953	1	
D3 (E09)	Diode	IS953	1	
D10 (A05)	Diode	SR1FM-2	1	
D11 (A05)	Diode	SR1FM-2	1	

Symbol (Location)	Description	Part Number	Q'ty	Notes
D12 (A06)	Diode	SR1FM-2	1	
D13 (A05)	Diode	SR1FM-2	1	
D14 (B04)	Diode, Zener	RD15FB	1	
D15 (D06)	Diode	IS953	1	
D18 (H01)	Diode, Zener	RD15FB	1	
D19 (H01)	Diode, Zener	RD6.2FB	1	
D20 (B09)	Diode, Zener	HZ4-2C	1	
D22 (E07)	Diode	IS953	1	
D23 (E07)	Diode	IS953	1	
D26 (E01)	Diode	SR1G-4	1	
D27 (D01)	Diode	IS953	1	
D28 (D01)	Diode	IS953	1	
D29 (D02)	Diode	IS953	1	
D30 (H01)	Diode	IS953	1	
D31 (E10)	Diode, Zener	HZ6-2A	1	
L1 (C11)	Inductor	TP0206-1R8K	1	
L2 (C10)	Inductor	TP0206-1R8K	1	
L3 (C11)	Inductor	TP0206-8R2K	1	
L4 (C10)	Inductor	TP0206-8R2K	1	
L5 (D11)	Inductor	TP0206-3R3K	1	

Symbol (Location)	Description	Part Number	Q'ty	Notes
R1 (A10)	Resistor, Film Metal	NL1/4J4701F	1	
R2 (A11)	Resistor, Film Metal	NL1/4J1201F	1	
R3 (A11)	Resistor, Film Metal	NL1/4J1201F	1	
R4 (B11)	Resistor, Film Metal	NL1/4J3300F	1	
R5 (A11)	Resistor, Film Metal	NL1/4J1000F	1	
R6 (A10)	Resistor, Film Metal	NL1/4J3300F	1	
R7 (A11)	Resistor, Film Metal	NL1/4J1501F	1	
R8 (A10)	Resistor, Film Metal	NL1/4J1501F	1	
R10 (C11)	Resistor, Film Metal	NL1/4J1500F	1	
R11 (B10)	Resistor, Film Metal	NL1/4J1500F	1	
R12 (D11)	Resistor, Film Metal	NL1/4J3300F	1	
R13 (D11)	Resistor, Film Metal	NL1/4J3300F	1	
R14 (D10)	Resistor, Film Metal	NL1/4J1000F	1	
R15 (D10)	Resistor, Film Metal	NL1/4J1500F	1	
R16 (D10)	Resistor, Film Metal	NL1/4J1500F	1	
R17 (D11)	Resistor, Film Metal	NL1/4J1000F	1	
R18 (E11)	Resistor, Film Metal	NL1/4J1000F	1	
R19 (D11)	Resistor, Film Metal	NL1/4J4701F	1	
R20 (D10)	Resistor, Film Metal	NL1/4J4701F	1	
R21 (E11)	Resistor, Film Metal	NL1/4J47R0F	1	
R22 (E10)	Resistor, Film Metal	NL1/4J47R0F	1	
R23 (E10)	Resistor, Film Metal	NL1/4J6800F	1	
R24 (E11)	Resistor, Film Metal	NL1/4J6800F	1	
R25 (E11)	Resistor, Film Metal	NL1/4J47R0F	1	
R26 (E10)	Resistor, Film Metal	NL1/4J47R0F	1	
R27 (E11)	Resistor, Film Metal	NL1/4J4700F	1	
R28 (E11)	Resistor, Film Metal	NL1/4J4700F	1	
R29 (G11)	Resistor, Film Metal	NL1/4J2201F	1	
R30 (G11)	Resistor, Film Metal	NL1/4J1201F	1	

Symbol (Location)	Description	Part Number	Q'ty	Notes
R31 (G11)	Resistor, Film Metal	NL1/4J47R0F	1	
R32 (G09)	Resistor, Film Metal	NL1/4J1001F	1	
R33 (F11)	Resistor, Film Metal	NL1/4J47R0F	1	
R34 (F11)	Resistor, Film Metal	RL075392G	1	
R35 (H10)	Resistor, Film Metal	NL1/4J5601F	1	
R40 (E09)	Resistor, Film Metal	NL1/4J3301F	1	
R41 (E09)	Resistor, Film Metal	NL1/4J4701F	1	
R42 (E09)	Resistor, Film Metal	NL1/4J1002F	1	
R43 (D09)	Resistor, Film Metal	NL1/4J4701F	1	
R44 (D09)	Resistor, Film Metal	NL1/4J4701F	1	
R45 (C10)	Resistor, Film Metal	NL1/4J4701F	1	
R50 (F09)	Resistor, Film Metal	NL1/4J2201F	1	
R51 (F09)	Resistor, Film Metal	NL1/4J1201F	1	
R52 (F09)	Resistor, Film Metal	NL1/4J5601F	1	
R53 (D08)	Resistor, Film Metal	NL1/4J1202F	1	
R54 (E08)	Resistor, Film Metal	NL1/4J4701F	1	
R55 (E09)	Resistor, Film Metal	NL1/4J38201F	1	
R56 (F10)	Resistor, Film Metal	NL1/4J2201F	1	
R60 (C09)	Resistor, Film Metal	NL1/4J1002F	1	
R61 (B09)	Resistor, Film Metal	NL1/4J1202F	1	
R62 (C09)	Resistor, Film Metal	NL1/4J1001F	1	
R63 (C10)	Resistor, Film Metal	NL1/4J1003F	1	
R64 (C09)	Resistor, Film Metal	NL1/4J4701F	1	

Symbol (Location)	Description	Part Number	Q'ty	Notes
R65 (C09)	Resistor, Film Metal	NL1/4J1501F	1	
R66 (C09)	Resistor, Film Metal	NL1/4J5602F	1	
R67 (C04)	Resistor, Film Metal	NL1/4J2202F	1	
R68 (C04)	Resistor, Film Metal	NL1/4J1001F	1	
R69 (C09)	Resistor, Film Metal	NL1/4J1501F	1	
R70 (C07)	Resistor, Film Metal	NL1/4J3302F	1	
R71 (B09)	Resistor, Film Metal	NL1/4J3901F	1	
R76 (C09)	Resistor, Film Metal	NL1/4J1001F	1	
R77 (C09)	Resistor, Film Metal	NL1/4J1001F	1	
R78 (A08)	Resistor, Film Metal	NL1/4J2202F	1	
R79 (B08)	Resistor, Film Metal	NL1/4J1802F	1	
R80 (A08)	Resistor, Film Metal	NL1/4J1803F	1	
R81 (B09)	Resistor, Film Metal	NL1/4J1001F	1	
R82 (A09)	Resistor, Film Metal	NL1/4J1003F	1	
R83 (A08)	Resistor, Film Metal	NL1/4J3301F	1	
R84 (A08)	Resistor, Film Metal	NL1/4J5601F	1	
R90 (E08)	Resistor, Film Metal	NL1/4J5602F	1	
R91 (E08)	Resistor, Film Metal	NL1/4J2201F	1	
R92 (D07)	Resistor, Film Metal	NL1/4J4702F	1	
R93 (D07)	Resistor, Film Metal	NL1/4J1003F	1	
R94 (C07)	Resistor, Film Metal	NL1/4J4701F	1	
R95 (B09)	Resistor, Film Metal	NL1/4J1002F	1	

Symbol (Location)	Description	Part Number	Q'ty	Notes
R97 (E05)	Resistor, Film Metal	NL1/4J27R0F	1	
R98 (E05)	Resistor, Film Metal	NL1/4J1002F	1	
R99 (H06)	Resistor, Film Metal	NL1/4J2200F	1	
R100 (H06)	Resistor, Film Metal	NL1/4J3300F	1	
R101 (H11)	Resistor, Film Metal	NL1/4J4701F	1	
R102 (D06)	Resistor, Film Metal	NL1/4J1201F	1	
R103 (E05)	Resistor, Film Metal	NL1/4J1002F	1	
R104 (H11)	Resistor, Film Metal	NL1/4J1000F	1	
R106 (C04)	Resistor, Film Metal	NL1/4J3300F	1	
R107 (H07)	Resistor, Film Metal	NL1/4J1000F	1	
R109 (C04)	Resistor, Film Metal	NL1/4J3301F	1	
R110 (H07)	Resistor, Film Metal	NL1/4J4701F	1	
R111 (H06)	Resistor, Film Metal	NL1/4J1002F	1	
R112 (H09)	Resistor, Film Metal	NL1/4J8202F	1	
R113 (H03)	Resistor, Film Metal	NL1/4J2201F	1	
R114 (H05)	Resistor, Film Metal	NL1/4J2200F	1	
R115 (E10)	Resistor, Film Metal	NL1/4J5600F	1	
R116 (D02)	Resistor, WW	MU2R2ZJ	1	
R118 (E07)	Resistor, Film Metal	NL1/4J3301F	1	
R119 (B09)	Resistor, Film Metal	NL1/4J2201F	1	
R120 (B09)	Resistor, Film Metal	NL1/4J2701F	1	

Symbol (Location)	Description	Part Number	Q'ty	Notes
VRI (A04)	Resistor, Variable Metal	POT110IT-I-103	1	
RMI (G05)	Resistor, Module	DIL-12D-221/331RJ	1	4114R-003- 221/331
RM2 (D06)	Resistor, Module	RGSD4T103J	1	
RM3 (C02)	Resistor, Module	RGSD4T222J	1	
RM4 (D01)	Resistor, Module	RGSD4T222J	1	
K1 (F02)	Relay	AG2023-9	1	DS2-M-DC24V-UL
SW1 (H07)	Switch, Dip	DYS-6	1	
SW2 (H05)	Switch, Dip	DYS-6	1	
LF1 (H02)	Line Filter	ZJK51R5-00	1	
TR1 (C04)	Transistor	2SC2718	1	
TR2 (C04)	Transistor	2SC2718	1	
TR3 (E11)	Transistor	2SC321H-B	1	
TR6 (E10)	Transistor	2SC321H-B	1	
TR7 (G01)	Transistor	2SD634	1	
TR8 (G01)	Transistor	2SD634	1	

Symbol (Location)	Description	Part Number	Q'ty	Notes
TR9 (E01)	Transistor	2SD634	1	
TR10 (E01)	Transistor	2SD634	1	
TR11 (A05)	Transistor	2SA495GTM	1	
CL1 (D05)	Crystal, Unit Quartz	HC-18/U(11000KHz)	1	



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\* 20 Meg. Fixed Disk  
\*  
\* Section 3  
\*  
\* Maintenance manual  
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November 15, 1985





# MITSUBISHI 5.25 INCH FIXED DISK DRIVE MR 521/522

## Maintenance Manual



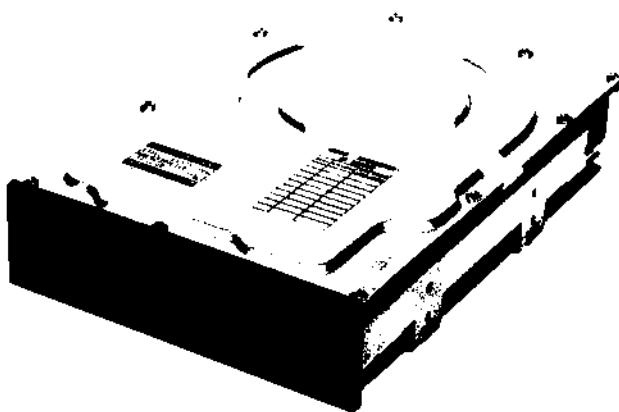
MITSUBISHI ELECTRIC CORPORATION



August 4, 1984  
S06-G30046 A

MR521/MR522 5.25 INCH FIXED DISK DRIVE

MAINTENANCE MANUAL (12.75 MB/25.5 MB)



MITSUBISHI ELECTRIC CORPORATION

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1. GENERAL

This manual describes the operation and maintenance of MR521 and MR522, 5.25 Inch Mini Fixed Disk Drives.

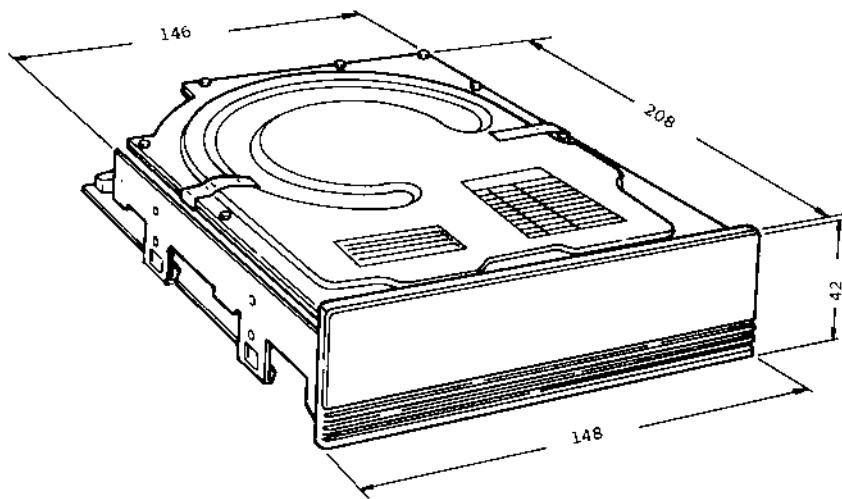


Figure 1-1 External View



## 2. UNIT DESCRIPTION

The MR521, MR522 Mini Fixed Disk Drive (referred hereafter to as "the drive") is a random access storage unit using a 5.25 inch (130 mm) diameter non-replaceable disk. Each side of the disk is equipped with a magnetic head that travels across 612 data tracks. Storage capacity is 12.75M bytes (unformatted) achieved with two heads for MR521 and 25M bytes achieved with 4 heads for MR522.

### 2.1 Features

- (1) The head positioning mechanism consists of a swing arm, actuator and stepper motor. A servo embedded, micro step driven, stepper motor arrangement is used to achieve a low cost, high precision positioning mechanism.
- (2) Basic parts such as the head, disk, and actuator are enclosed and protected in a sturdy aluminum disk enclosure. The disk enclosure is dust proof and uses a circulating clean air system to keep the environment within class 100, in order to achieve high reliability.
- (3) The external dimensions, installation dimensions, and DC power connectors of the drive are the same as industry standard mini floppy disk drives.
- (4) The interface is compatible with the industry standard SEAGATE ST506 interface.

## 2.2 Specifications

(Nominal values unless specified otherwise)

ITEM	TYPE	MR521	MR522
1. MAX. CAPACITY*	TOTAL CAPACITY (M Byte) CAPACITY PER SURFACE (M Byte) TRACK CAPACITY (Byte/TK)	12.75 6.37 10416	25.5 6.37 10416
2. DISKS	NUMBER OF DISKS DATA SURFACE NUMBER OF CYLINDERS NUMBER OF TRACKS**	1 2 612 1224	2 4 612 2448
3. MAGNETIC HEADS	NUMBER OF R/W HEADS	2	4
4. RECORDING METHOD	METHOD MAXIMUM BIT DENSITY (bPI) TRACK DENSITY (tPI) DATA TRANSFER RATE (M bits/s) (K bytes/s)		MFM 9201 690 5 625
5. ACCESS TIME	SEEK TIME TRACK TO TRACK MIN. (ms) AVERAGE*** (ms) FULL SPAN MAX. (ms) DISK ROTATIONAL SPEED (rpm) AVERAGE LATENCY TIME (ms)		18 85 199 3536 8.48
6. DIMENSION & WEIGHT	WIDTH x HEIGHT x DEPTH**** (mm) WEIGHT (kg)		146 x 41.3 x 203.2 1.6
7. POWER SOURCE		+5 VDC ±5% 0.7 A Typ. 1.5 A Max. +12 VDC ±5% 1.0 A Typ. 1.5 A Max. 3.0 A Starting	+5 VDC ±5% 0.7 A Typ. 1.5 A Max. +12 VDC ±5% 1.2 A Typ. 1.5 A Max. 3.0 A Starting
8. RELIABILITY	RECOVERABLE ERROR RATE NON-RECOVERABLE ERROR RATE SEEK ERROR RATE MTBF (hour) MTTR (hour)		10 <sup>-10</sup> 10 <sup>-12</sup> 10 <sup>-6</sup> 11000 0.5
9. OPERATING	TEMPERATURE (°C), (°F) RELATIVE HUMIDITY (% R.H.)		5 - 50, 41 - 122 8 - 80
10. INTERFACE			ST506 compatible

\* Storage capacities given in Unformat values

\*\* Including alternate tracks

\*\*\* Including average settling time

\*\*\*\* Not including front panel dimensions (See Chapter 4.4 for details)

## 2.3 Structure and Format

As shown in figure 2-1, this drive consists of a magnetic disk, magnetic head, actuator, spindle motor, printed circuit assembly (PCA) and disk enclosure.

### 2.3.1 Magnetic head and magnetic disk

#### (1) Magnetic head

The magnetic head, which is attached to the positioning actuator, flies above the disk surface to read and write information. The magnetic head rests on the disk surface when the disk is not rotating and flies on the aerodynamic lift created by the air flow when the disk rotates.

#### (2) Magnetic disk

The magnetic disk is a magnetically coated aluminum disk with an external diameter of 130 mm (5.118 inch) and an internal diameter of 40 mm (1.575 inch). It is attached to a spindle hub mechanism which is connected directly to a brushless DC motor.

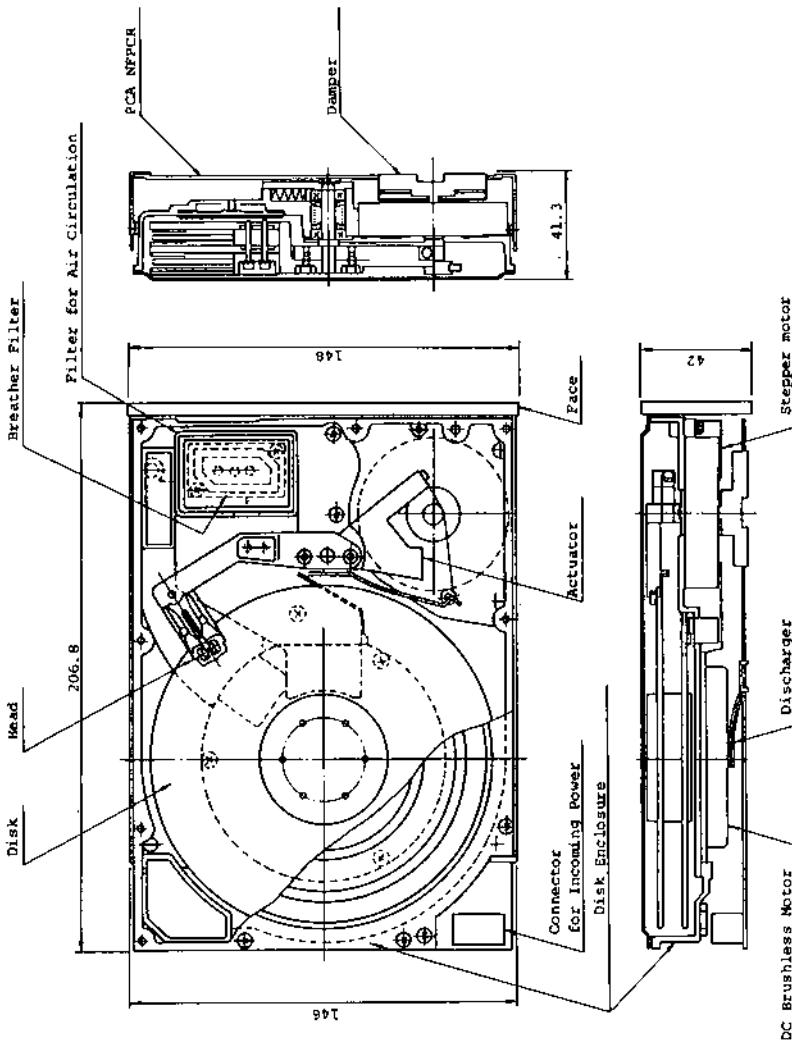
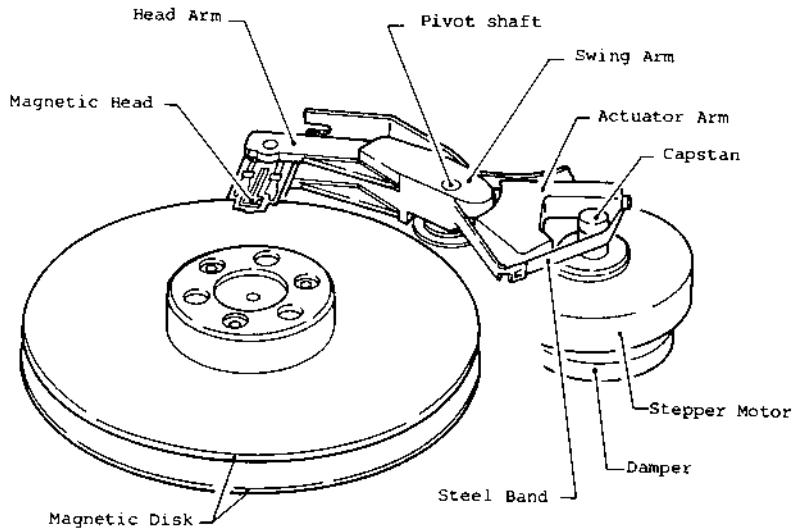


Figure 2-1 MRS21/MRS22 Structure Diagram

### 2.3.2 Actuator

As shown in figure 2-2, the actuator assembly is a rotary actuator and is used to move the magnetic head. The assembly consists of a damper, stepper motor, capstan, steel band, actuator arm, swing arm, and head arm. The damper on the stepper motor being used to reduce the head settling time.



(Note) MR521 has one disk and MR522 has two disks

Figure 2-2 Head Positioning Mechanism



### 2.3.3 Spindle motor

The spindle motor assembly, which consists of a brushless DC motor and spindle hub, rotates the magnetic disk at 3536 RPM.

### 2.3.4 Disk enclosure

The disk enclosure is a sturdy, die cast aluminum, air tight enclosure containing the magnetic head, magnetic disk and actuator. It is equipped with an air filtration system consisting of breather filter and circulation filter. The breather filter balances the pressure within the enclosure when the disk starts or stops rotating and also prevents external air from flowing in. The circulation filter is used to keep the air flow in the enclosure clean. Figure 2-3 shows the air flow inside the disk enclosure.

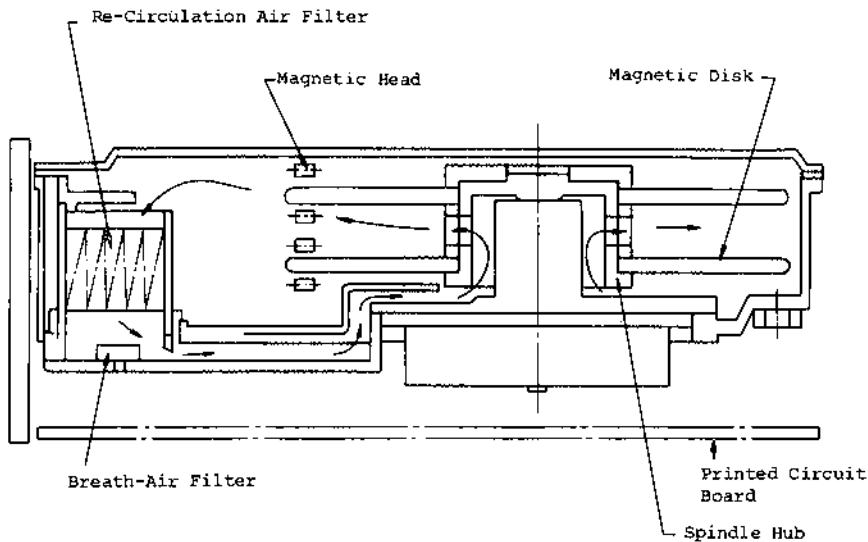


Figure 2-3 Air Filtration System

### 2.3.5 PCA (Printed Circuit Assembly)

The PCA called NFPCCR, is a single printed circuit board containing the following circuits:

- (1) Read/write
- (2) Spindle motor control
- (3) Stepper motor control
- (4) Index sensor
- (5) Write fault sense

Figure 2-4 shows a functional block diagram of the PCA.

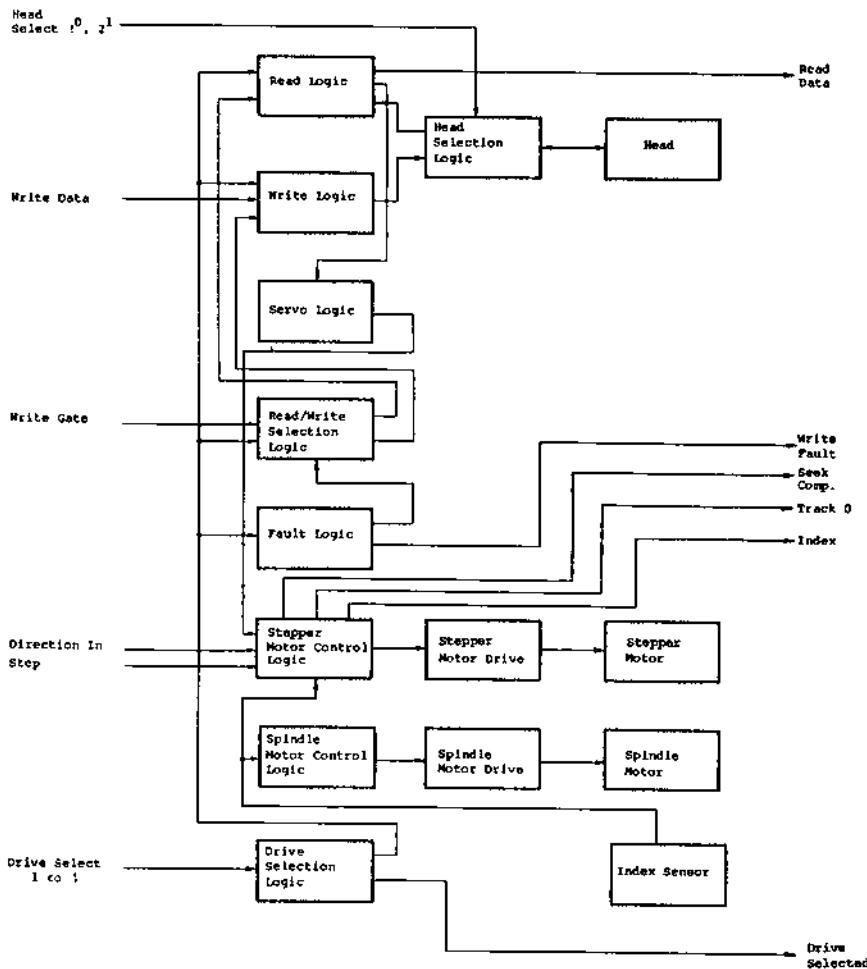


Figure 2-4 PCA Functional Block Diagram

### 3. SYSTEM OPERATIONAL METHOD

This section describes the drive mechanism and PCA circuit operation.

### 3.1 Power On Sequence

When the drive power is turned on, the spindle motor rotates. When it reaches 3536 RPM it's, the read/write head is automatically positioned at cylinder 0 (initial seek).

The power sequence is controlled by the microprocessor on the PCA. Figure 3-1 shows the microprocessor control flow.

- (1) When the drive power is turned on, the microprocessor is reset and initialized by the power-on reset circuit.
  - (2) When the power-on reset sequence is complete, the microprocessor checks for drive errors and if there are no errors, it outputs SPINDLE ON signal and starts the spindle motor.
  - (3) The rotational speed of the spindle motor is determined by comparing the microprocessor's internal timer and the index sensor output, produced at each rotation of the motor. When the rotational speed reaches 3536 ±5%, the head is positioned at cylinder 0 and the initial seek starts.

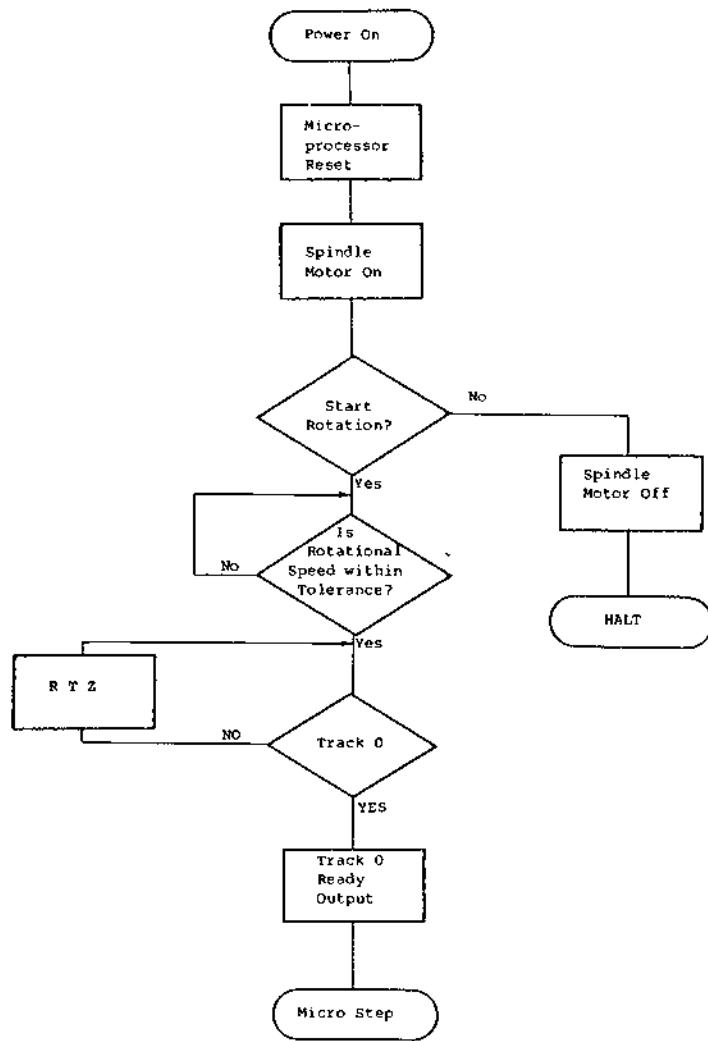


Figure 3-1 Power On Sequence Flow

- (4) The microprocessor sends stepper motor drive pulses in a to move the head reverse direction and then checks the guard band area on the external circumference of the disk. After determining the position of the guard band area, the magnetic head is positioned on cylinder 0. (Return to Zero)
- (5) After positioning the head on cylinder 0, the "Track 0" signal and "Ready signal" are output on the signal interface.
- (6) After the "Ready signal" is output, a "Seek complete" signal will be output on the signal interface after 30 seconds. Seek, read, and write operations can be performed thereafter.

### 3.2 Spindle Motor Drive

The drive uses a brushless DC motor as its spindle motor. The motor electronically switches the change in magnetic flux in its windings using an internal Hall sensor and thus has no mechanical brush contact—making it more durable.

As shown in figure 3-2, a current corresponding to the rotation period being detected by the Hall sensor is supplied to the motor windings to rotate the motor at a constant speed. The current is set by a, single chip, speed control IC.

The spindle motor of the drive has a four phase uni-polar winding (L1 to L4) and two Hall sensors. Figure 3-3 shows the relationship between the Hall sensor output and winding switching.

The spindle motor is started by the microprocessor on the PCA. The motor starts only when the microprocessor output signal SPON is active and spindle motor speed reaches 3536 ±5% RPM—after approximately 15 seconds. When the microprocessor SPON signal becomes inactive, the reverse emf in the motor winding is applied in the direction of the power source and acts as a brake to stop the rotation of the motor in approximately 15 seconds.

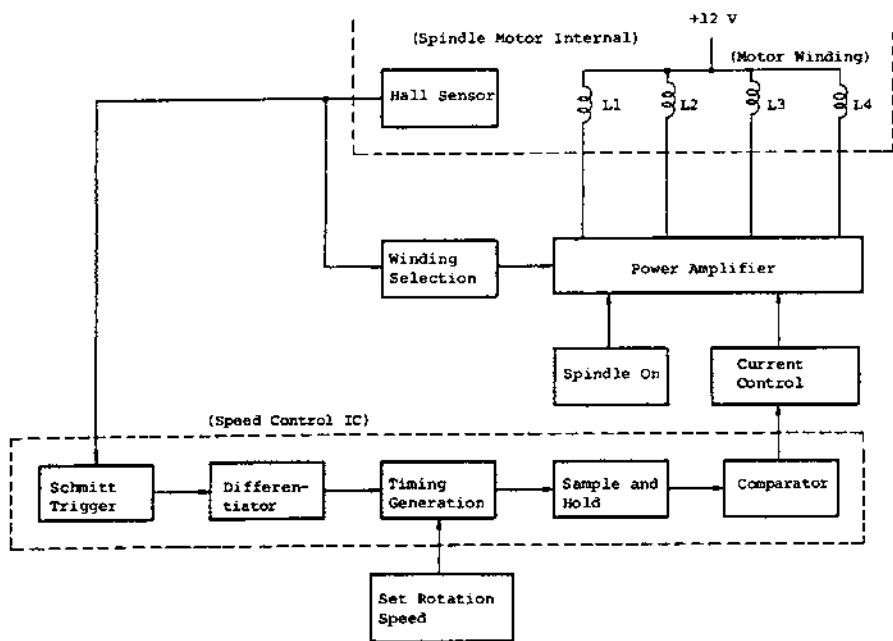


Figure 3-2 Spindle Motor Drive Block Diagram

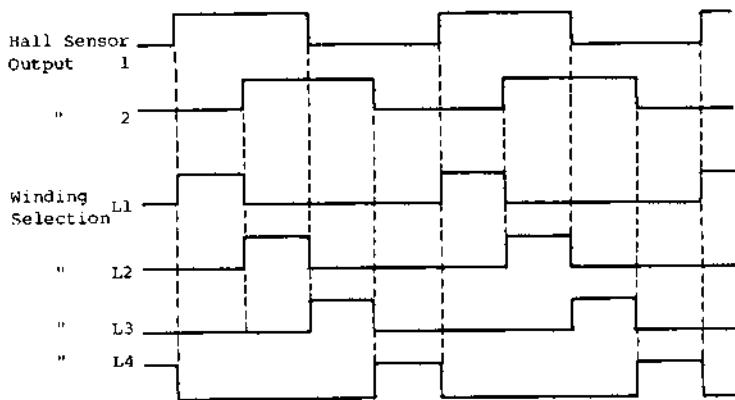


Figure 3-3 Winding Selection Timing Chart

### 3.3 Index Detection

The index sensor is attached to the disk enclosure. An index signal is sent when a magnet, which is attached to the spindle passes the sensor.

This mechanical index sensor signal notifies the controller when the magnetic head passes the servo area that is embedded on the disk surface.

The index signal that is output on the interface is generated by the microprocessor. The signal is output 395  $\mu$ s after the mechanical index has been sensed, this is to compensate for the area used by the embedded servo. n-b; The timing during seek is governed by the trailing edge of the mechanical index pulse.

This signal is used not only to check the rotation, but also to determine the start track position when formatting.

### 3.4 Drive Selection

The unit can be connected with up to four drives on the same bus.

A drive is selected, read/write and seek operations are enabled when one of the DRIVE SELECT signals 1 to 4 on the interface matches the drive address switch specification set on the drive. However, when the "R" (radial operation) option switch is OFF, a drive is selected regardless of DRIVE SELECT signals 1 to 4. The SELECT LED on the front panel illuminates only when DRIVE SELECT signals 1 to 4 matches the drive address switch.

The following signals are gated by the DRIVE SELECT signal.

Input Signal	Output Signal
(1) WRITE GATE	(1) DRIVE SELECTED
(2) WRITE DATA	(2) TRACK 0
(3) STEP	(3) READY
	(4) SEEK COMPLETE
	(5) WRITE FAULT
	(6) INDEX
	(7) READ DATA

### 3.5 Head Positioning

Head positioning is controlled by the microprocessor and consists of seek operation (figure 3-5) which moves the head to the target track and a positioning operation (figure 3-4) which positions the head on the target track.

### 3.5.1 Seek

A seek operation is executed in either normal mode or buffered mode depending on the frequency of the step pulses from the controller. The step pulses are counted by the buffer counter. The microprocessor monitors this count and performs a normal mode seek when the pulse is 3 ms or more and buffered mode seek when it is between 6  $\mu$ s and 200  $\mu$ s. A step pulse rate between 200  $\mu$ s and 3 ms must not be used, as thus may cause positioning errors in a minority of cases.

A seek operation is performed when all the following conditions are satisfied:

- o The WRITE GATE is inactive
- o A WRITE FAULT is not detected
- o The drive is READY
- o Step pulses are received from the interface
- o The DIRECTION IN signal is active when the head is at track 0
- (1) Normal mode seek

In this seek mode the head moves at a step pulse rate of 3 ms. The head seeks one track for each step pulse input. A SEEK COMPLETE signal is output 39 ms after the last step pulse is received and then the seek operation is terminated.

- (2) Buffered mode seek

In this seek mode, pulses are received at a step rate of 6  $\mu$ s to 200  $\mu$ s and are counted. A fast seek operation is then performed by the stepper motor.

In general a stepper motor has a limiting self activating frequency and will not operate properly when drive pulses with frequency greater than this limit are supplied. However, by gradually increasing the frequency of the drive pulses, a stepper motor can be driven by pulses with frequencies greater than the self activation frequency.

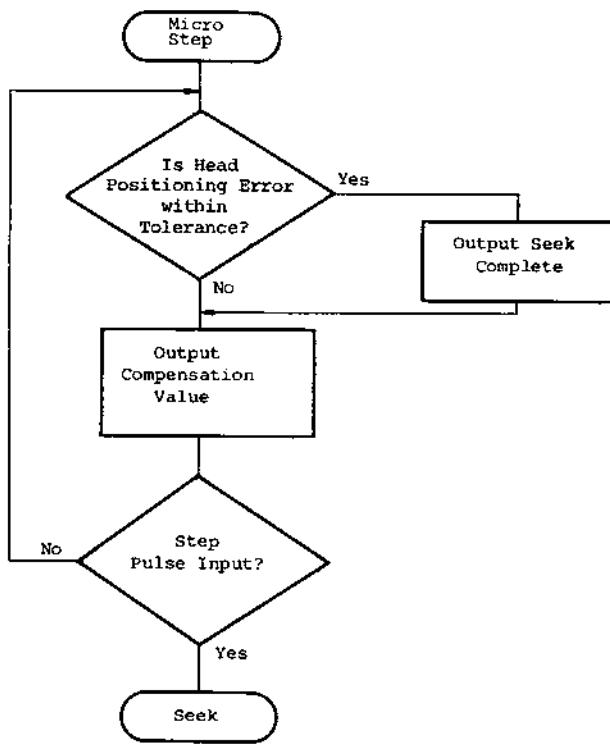


Figure 3-4 Positioning Operation Flow

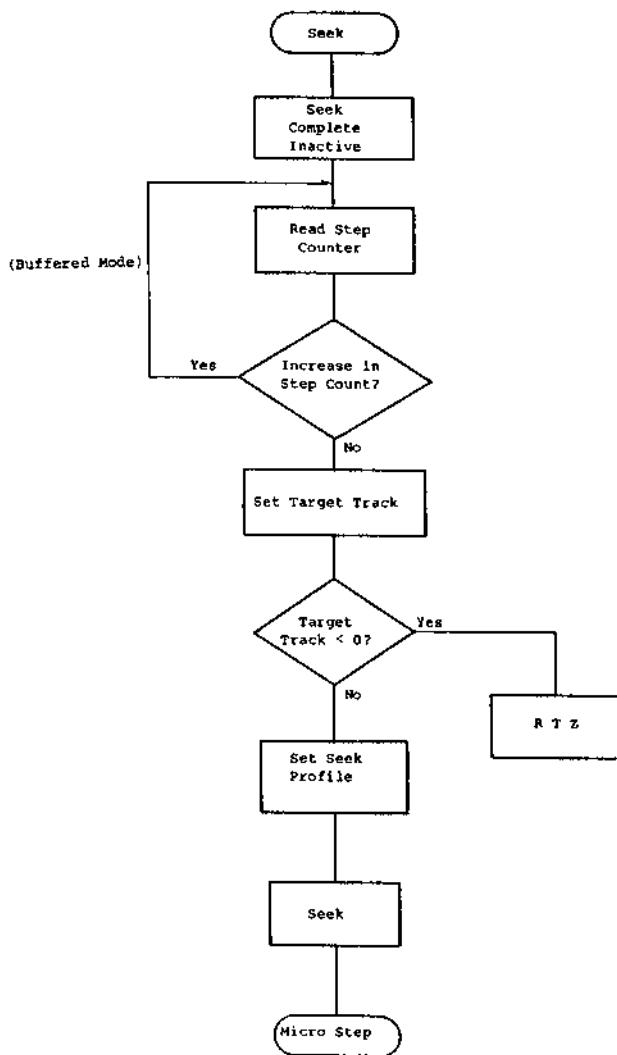


Figure 3-5 Seek Operation Flow

A stepper motor driven with pulse frequency greater than the self activation frequency can be slowed and stopped by gradually decreasing the frequency.

The drive uses an optimum stepper drive rate profile which is stored in a ROM table. This is used to control the stepper motor speed using the microprocessor.

### 3.5.2 Positioning operation

As shown in figure 3-6, positioning is performed by determining the head displacement based on the servo information. This is imbedded in the positioning information area of each data track. Compensation for head alignment errors is achieved by supplying a compensation current to the windings of the corresponding coils providing the excitation phase to the stepper motor magnets.

Figure 3-7 shows the data track and the positioning information area. Servo information is written during manufacture, in the positioning information area, based on the mechanical index signal output by the index sensor.

As shown in figure 3-7, the positioning information consist of areas of magnetization and erased areas. These are arranged in two rows in the direction of the radius so that each boundary is positioned at the center of a data track. The two rows of servo information with alternating patterns in the direction of the radius are divided into servo information A which is closer to the index area and servo information B which is down track from the index area.

Figure 3-7 shows the relationship between the signal read by the head in servo information A and B and the position of the head.

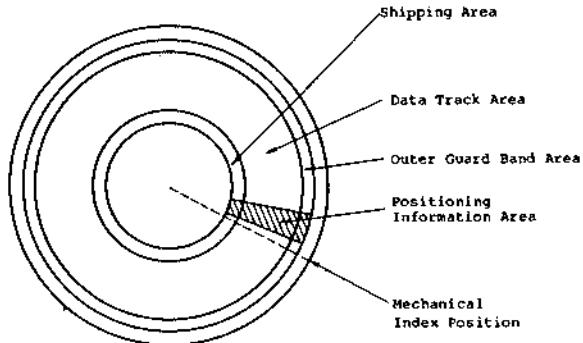


Figure 3-6 Data Surface Structure

As shown in figure 3-7, when the head is in the center of a data track, the signal amplitude of servo information A and B are the same. When the head is displaced from the center of the data track, a signal amplitude corresponding to the displacement is observed. This difference in signal amplitude is used by the microprocessor to obtain a compensation value and the stepper motor is driven so as to eliminate the positioning error.

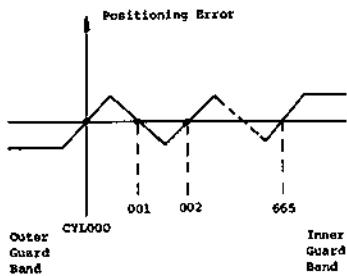
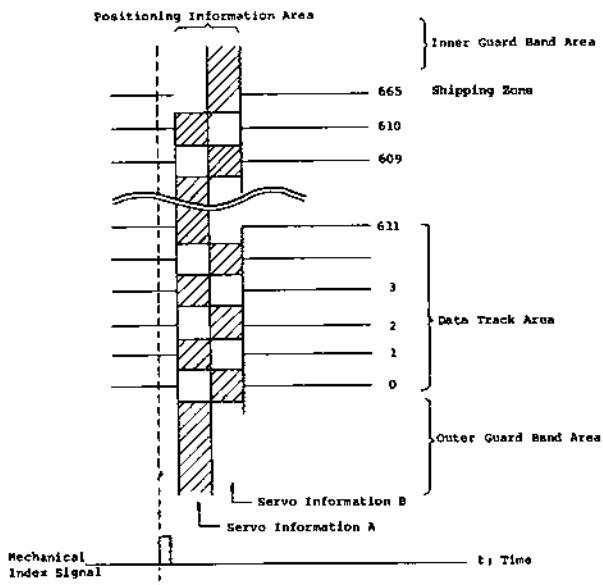


Figure 3-7 Data Track and Embedded Servo Information

### 3.5.3 Return to zero

The positioning of the head on data track 0 is referred to as a "Return to Zero" (RTZ). MR521, 522 will perform a RTZ operation under the following conditions.

- (1) During the initial seek when power is initially supplied to the drive.
- (2) When the step pulse address of the target track becomes negative.

The RTZ operation is controlled by the microprocessor, based on the servo information on the disk surface. Figure 3-8 shows the head movement and its relationship to the stepper motor excitation phases during an RTZ operation, figure 3-9 shows the control flow.

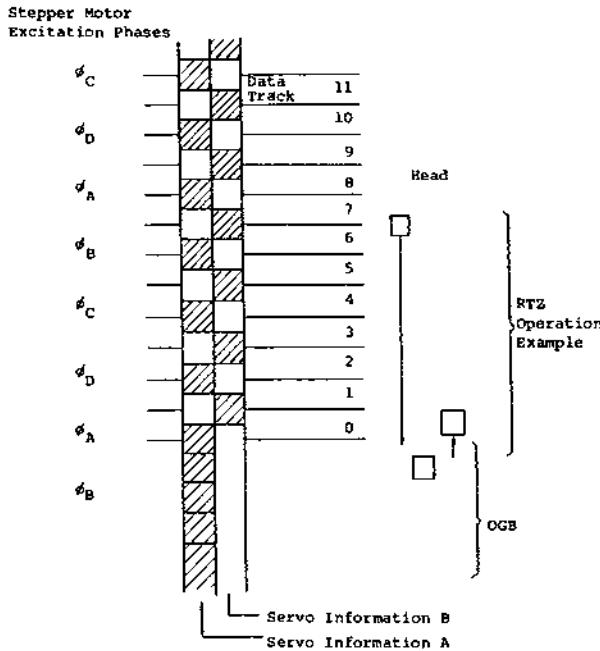


Figure 3-8 Example of Stepper Motor Excitation Phases and Head Movement During RTZ Operation

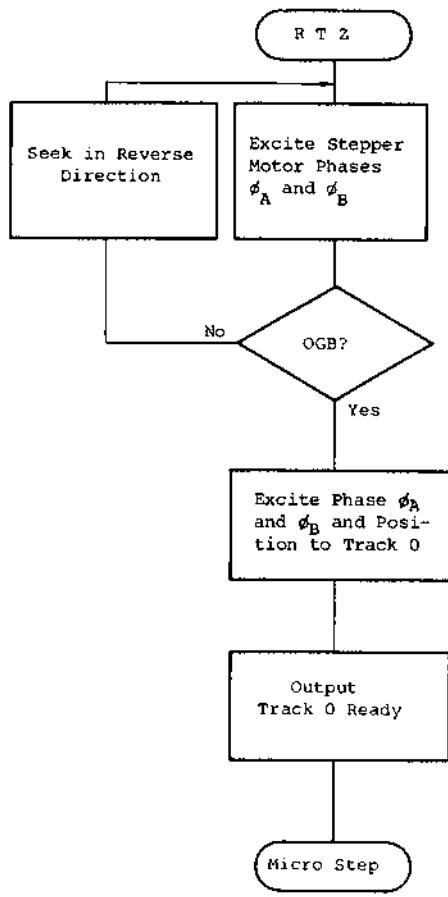


Figure 3-9 RTZ Flow

### 3.5.4 Stepper motor drive

MRS21, 522 use a 0.9°, four phase, unipolar stepper motor. During a seek operation, a 1 or 2 phase excitation is performed. Figure 3-10 shows the relationship between data track number and stepper motor excitation phase during seek operations.

The positioning of the head to the data track center is achieved by 2-phase excitation of the stepper motor under microprocessor control.

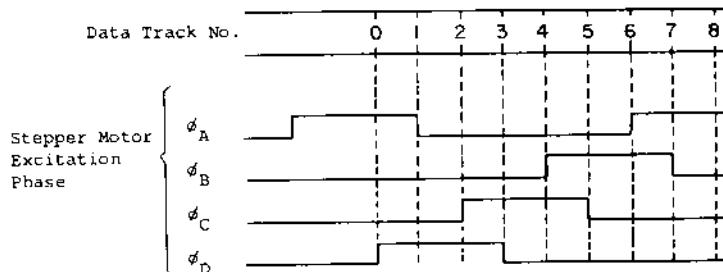


Figure 3-10 Data Track No. and Stepper Motor Excitation Phase  
(During Seek)

### 3.6 Read/Write

The read/write select, read amplification, write driver, sense write error, and pre-amplification functions are all integrated in a single chip. The actual read/write operation is performed by the read/write IC attached to the head positioning arm near the head.

The differentiating circuit, zero cross detector circuit, pseudo zero cross deletion circuit, and sense write fault circuit are all located on the PCA. Figure 3-11 shows a functional block diagram of MRS21, 522.

#### 3.6.1 Read/Write IC

The read/write IC consists of the circuits shown in Figure 3-12 which are:

- (1) Low noise read amplifier circuit (with a gain of 100)
- (2) Head selection circuit

- (3) Write driver circuit (used to change the write current polarity and is triggered by the negative edge of the MFM write data.)
- (4) Write power source circuit (with current determined by the following external resistor):
- (5) Write error detection circuit which detects the following errors:
- o Write current switching frequency abnormally low during write
  - o No write current during write
  - o The coil of the selected head is disconnected or shorted during write

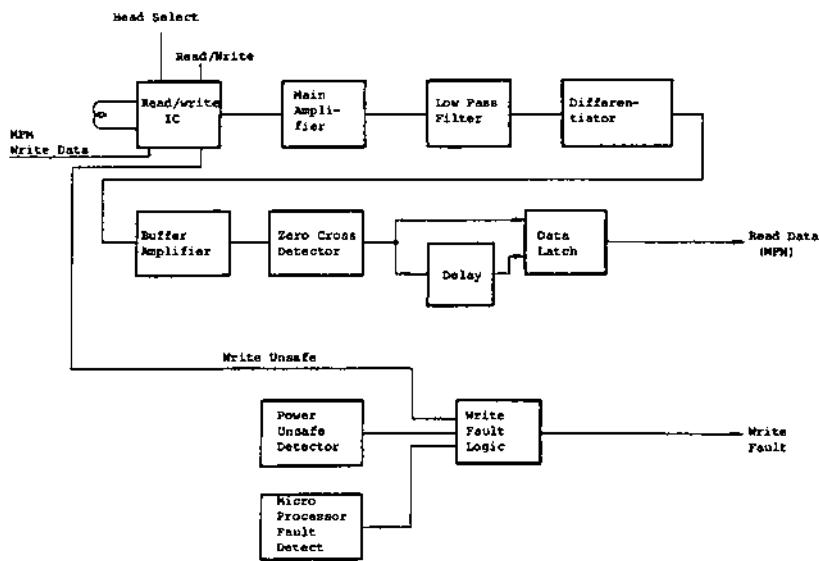


Figure 3-11 Read/Write, Write Fault Block Diagram

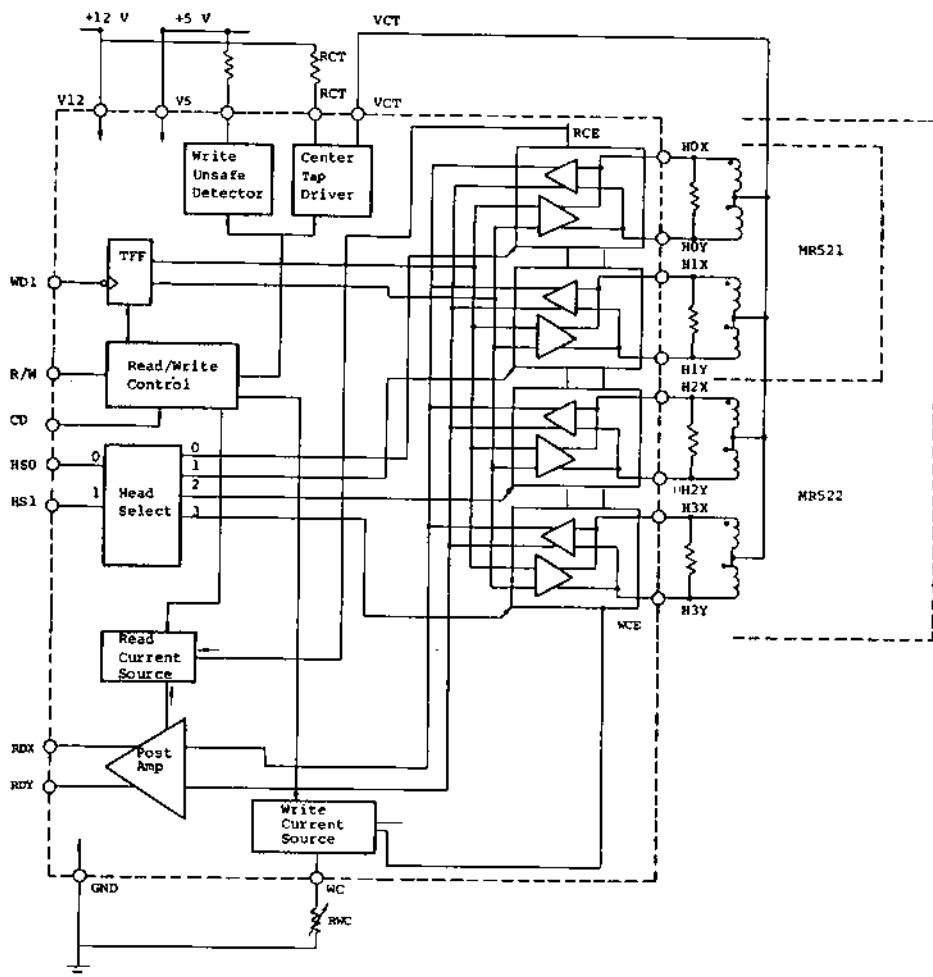


Figure 3-12 Read/Write IC Blocks



### 3.6.2 Read Operation

A read operation is performed when the following conditions are satisfied:

- (1) The DRIVE SELECT signal is active
- (2) The SEEK COMP signal is active
- (3) The HEAD SELECT signal is active
- (4) The WRITE GATE is inactive

One of the two heads MR521 or four heads MR522 heads is selected by a two bit binary signal HEAD SELECT 2 (2).

The read output from the head is amplified by the read amplifier in the read/write IC. It is then passed through a low-pass filter on the FCA to remove high-frequency noise. Up to this point, the change in flux which forms the read data is at the peak of the waveform. This peak is phase shifted by 90° with a differentiating circuit and converted to a zero cross point. It is then changed to a digital signal by a zero cross detector oct.

The signal resolution increases on the outer tracks and shoulders tend to appear in the output from the low pass filter. This shoulder acts as a virtual peak and causes noise during differentiation and zero cross detection. A shoulder noise eliminator in the form of a Time Domain Filter removes this noise so that correct read data is obtained. Because the leading and trailing edge of the signal indicate the change in flux, the signal is created by obtaining the pulse for both edges with a pulse shaper. This signal is output through the interface as an RS-422 level, differential signal.

### 3.6.3 Write Operation

A write operation is performed when the following conditions are satisfied:

- (1) The DRIVE SELECT signal is active
- (2) The DRIVE READY signal is active
- (3) The SEEK COMPLETE signal is active
- (4) The WRITE FAULT signal is inactive
- (5) The WRITE GATE is active

When "WRITE GATE" becomes active, the read/write IC power source is enabled and write current can flow to the head. In order to compensate for the difference in head flying height at the inner and outer tracks, the write current is switched by the microprocessor.

The write current is supplied to the head through the write driver of the read/write IC. The current polarity is switched using the trailing edge of the data received from the signal interface.

The selection of the write head is performed by the head select circuit in the read/write IC.

WRITE DATA signals must be write precompensated to eliminate the effect of peak shift on the innermost tracks. For a more detailed description of write precompensation, please refer to the unit specification manual (So6-G30038).

#### 3.6.4 Write fault detection

The WRITE FAULT signal becomes active under the following conditions:

- (1) When multiple heads are simultaneously selected.
- (2) When the DC voltage (+5 V, +12 V) drops by more than 15%.
- (3) When "WRITE GATE" is active and write current does not flow.
- (4) When "WRITE GATE" is inactive and write current flows.

A write operation cannot be performed when the WRITE FAULT signal is active.

### 3.7 Formatting

#### 3.7.1 Recommended format

Figure 3-13 and table 3-1 show the recommended track formats for 32 sectors/track, 17 sectors/track, and 9 sectors/track.

Each track contains 10416 bytes, which is equivalent to an 8 inch double sided double density floppy disk. The sectors are defined by a soft sectoring method with the same sector format as floppy disks, but the number of sectors per track is greater.

(1) GAP1

The length of GAP1 is determined so that the sector 0 ID field can be read when the HEAD SELECT signal is switched at the leading edge of the "INDEX" signal.

(2) ID SYNC

This field serves to synchronize and stabilize the VFO for reading the next ID field. The VFO is synchronized when the code [00]<sub>16</sub> of this SYNC field is detected for 2 consecutive bytes or more. This is the prerequisite condition for detecting the following ID ADDRESS MARK.

(3) ID ADDRESS MARK

The ID ADDRESS MARK consists of the codes [A1]<sub>16</sub> and [FE]<sub>16</sub> and indicates the beginning of the ID field. The [A1]<sub>16</sub> pattern is a unique pattern with clock bits 4 and 5 missing to distinguish it from a data zone pattern.

(4) CYLINDER, HEAD, SECTOR, CRC

This field defines the SECTOR address. The CRC code is an extra byte that is used to perform a cyclic redundancy check during a read operation.

(5) GAP2

GAP2 is provided to absorb the splice point generated when the write current is turned on, when the data field is updated and to provide a stabilizing time when relocking the VFO when performing a read operation. The VFO is synchronized when two or more consecutive [00]<sub>16</sub> bytes are detected. This is the condition for detecting the DATA ADDRESS MARK.

(6) DATA ADDRESS MARK

This consists of two bytes [A1]<sub>16</sub> and [F8]<sub>16</sub> and indicates the start of the data field. [A1]<sub>16</sub> is a unique pattern with missing clocks bus similar to the ID field.

(7) DATA CRC

Data is recorded in this field. The data length is generally 256, 521, or 1024 bytes depending on the number of sectors.

(8) WRITE GATE ENABLING

The "WRITE GATE" is turned off at the end of the data field. To compensate for the splice point due to the switching off of the write gate, the READ GATE is switched off one or more bytes before this splice point.

## (9) GAP3

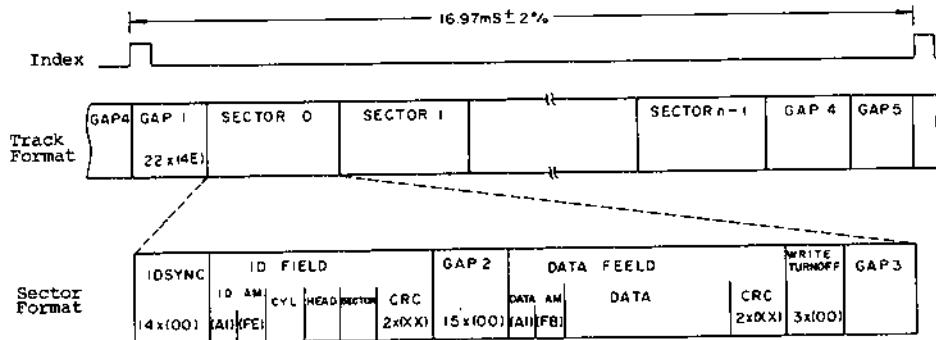
GAP3 serves to absorb the changes in sector length due to variation in the rotational period of the disk.

## (10) GAP4

GAP4 serves to absorb the changes in track length due to variations of the rotational period of the disk.

## (11) GAP5

GAP5 contains the head positioning servo information and is automatically write protected by the drive. This area is not available to the user.



## Formatting Conditions

- (1) Track capacity (excluding GAP5) ... 10,416 bytes nominal, 10,207 bytes minimum (rotation frequency -2%)
- (2) Head switching transient ..... 20  $\mu\text{s}$  maximum
- (3) "WRITE OFF" transient ..... 20  $\mu\text{s}$  maximum (write to read recover time)
- (4) INDEX detection deviation ..... 15  $\mu\text{s}$  maximum

Figure 3-13 Recommended Track Format

Table 3-1 Recommended Track Format Table

Item	Format Pattern [ ] <sub>16</sub>	Format Bytes			Remarks
		32 SECTOR/ TRACK	17 SECTOR/ TRACK	9 SECTOR/ TRACK	
GAP1	[4E] <sub>16</sub>	22 bytes	22 bytes	22 bytes	
ID SYNC *	[00] <sub>16</sub>	14	14	14	
ID ADDRESS MARK	[A1][FE] <sub>16</sub>	2	2	2	
CYLINDER & HEAD		2	2	2	
SECTOR	[00~1F] <sub>16</sub>	1	1	1	
CRC (ID)	[XX] <sub>16</sub>	2	2	2	
GAP2	[00] <sub>16</sub>	15	15	15	
DATA ADDRESS MARK*	[A1][FB]	2	2	2	
DATA	[XX] <sub>16</sub>	256	512	1024	
CRC (DATA)	[XX] <sub>16</sub>	2	2	2	
WRITE FORM OFF	[00] <sub>16</sub>	3	3	3	
GAP3	[4E] <sub>16</sub>	15	30	60	
GAP4	[4E] <sub>16</sub>	346	449	251	
GAP5	-	187	187	187	Cannot be used

\* ID and DATA ADDRESS MARK [A1]<sub>16</sub> bits 4 and 5 are assumed to be missing in order to create a unique pattern.

### 3.7.2 Read/write timing

Figure 3-14 shows the read/write timing based on the recommended format described in the previous section.

#### (1) WRITE format

A WRITE format operation outputs "WRITE DATE" and "WRITE DATA" at the leading edge of the INDEX signal of and defines the track format. The "WRITE GATE" is turned on within 200 ms a head switching operation and is turned off at the leading edge of the next INDEX.

#### (2) DATA WRITE

During a data write operation, a READ GATE signal is issued to read the ID field and when the location that is to be written to is found, the "WRITE GATE" is activated and data is written in the designated data field.

The maximum switching transient observed when the WRITE GATE is switched off is 20  $\mu$ s and falls in the ID SYNC field of the next sector. Therefore, two ID fields cannot be read consecutively.

#### (3) DATA READ

During a data read operation, the ID field is read. When the correct location is found the read gate is activated and the data field is read. The read gate switching condition is such that the splice points are not read.

During a read operation, there is no transient area problem and thus adjacent sectors can be read consecutively.

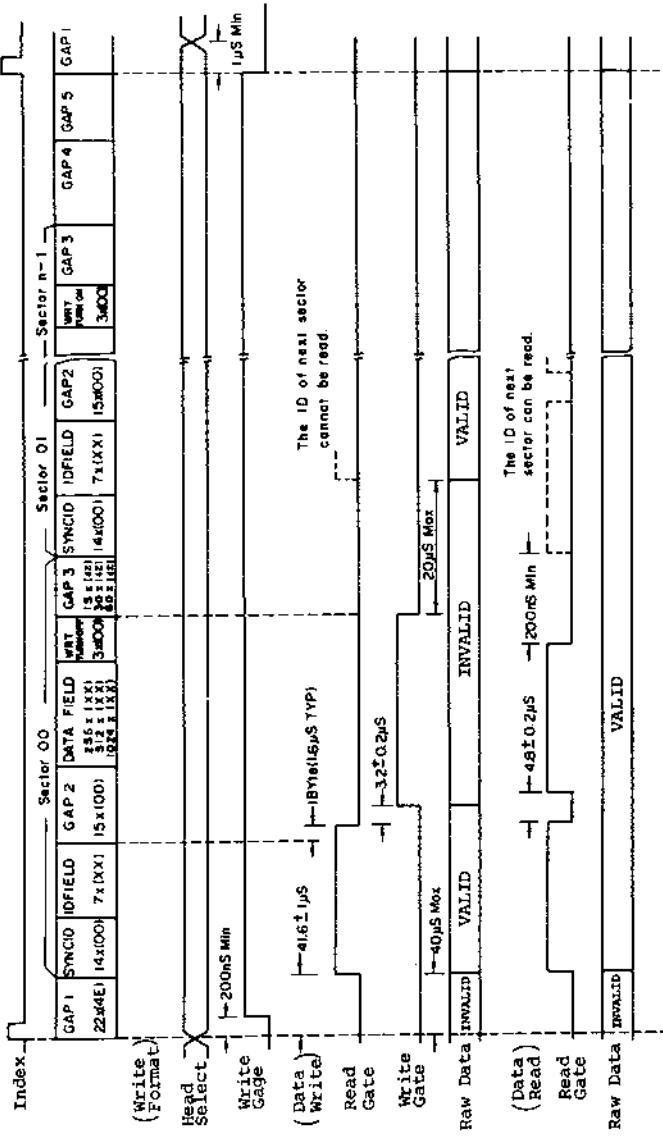


Figure 3-14 Read/Write Timing

#### 4. INSTALLATION AND HANDLING

This section describes the installation procedure and handling precautions required for MR521 and MR522

##### 4.1 Installation Environment

This drive must be operated only under the following conditions.

###### 4.1.1 Temperature and humidity

###### (1) Operating

Temperature 5° to 50°C

Temperature gradient ±8°C/Hour or less

Humidity 8 to 80% RH (at wet bulb temperature of 25°C or less) with no condensation

###### (2) Storage (in recommended package)

Temperature -40° to 70°C

Temperature gradient ±20°C/Hour or less

Humidity 5 to 95% RH (at wet bulb temperature of 26°C or less) with no condensation

#### 4.1.2 Vibration and shock

Condition		Operating	Non-operating
	Power Supply	ON	OFF
	Head Position	any zone	any zone
Vibration		0.4G	2G
Shock		2G	30G
		(Note 1)	(Note 2)
			(Note 3)

(Note 1): Freq. = 5 to 500 Hz

Mode = Automatic Sweep (3 min 1 cycle x 4)

Criteria = No Read Error and No Defect Increase.

(Note 2): Freq. = 5 to 300 Hz

Mode = Automatic Sweep  
(10 min 1 cycle x 6 cycle x 3 direction)

(Note 3): Our standard shipping package can protect damages from 90 cm drop without any actuator lock. Shock mount mechanism is built in base and frame.

#### 4.1.3 Altitude

Operating: 2,000 m maximum (6,580 ft)  
Storage: 12,000 m maximum (39,370 ft)

#### 4.1.4 Magnetic field

300 AT/m maximum (measured in close proximity to the head)

#### 4.1.5 Field Strength

0.3 V/m maximum

#### 4.1.6 Dust

0.3 mg/m<sup>3</sup> maximum ( $3 \times 10^{-4}$  oz/ft<sup>3</sup>)

### 4.2 Package Handling

- (1) Do not stack more than 10 drives.
- (2) Handle carefully and do not throw, drop, or leave the drive out of doors.
- (3) Keep away from moisture.

### 4.3 Packing and Unpacking

Do not turn the stepper motor damper during packing or unpacking.

#### 4.3.1 Unpacking

Unpack according to figure 4-1.

#### 4.3.2 Packing

Pack According to Figure 4-1. The packaging material supplied is reusable.

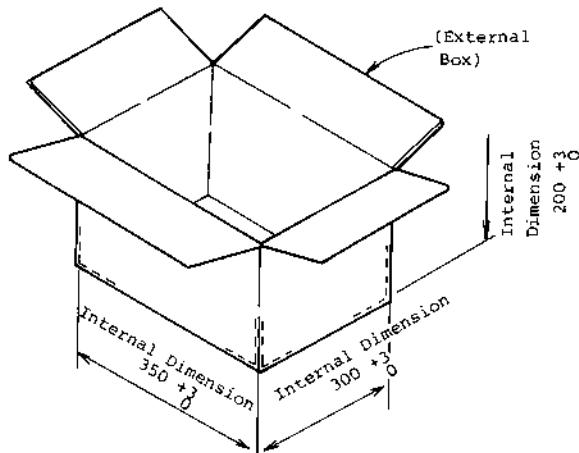
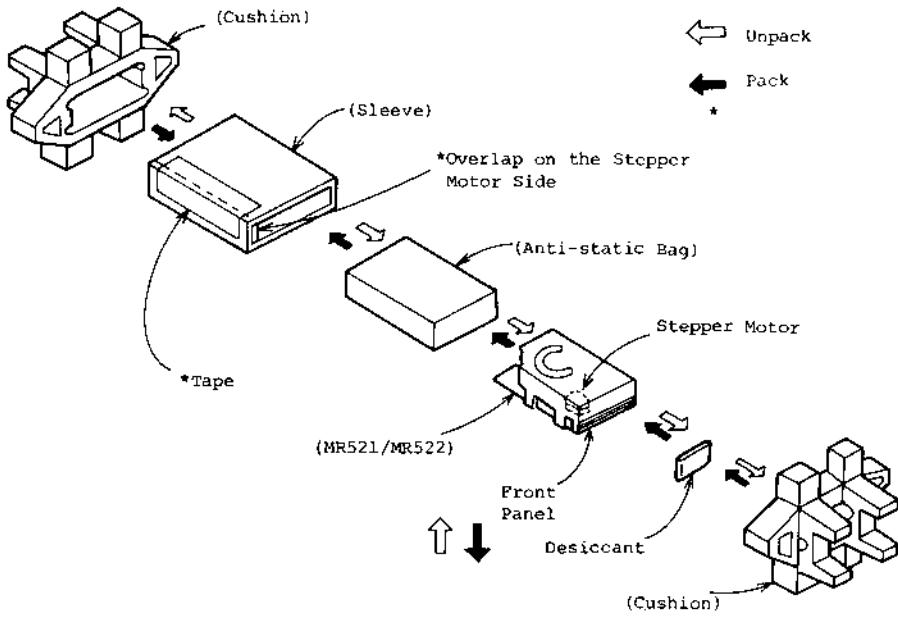


Figure 4-1 Unpacking and Packing Procedures

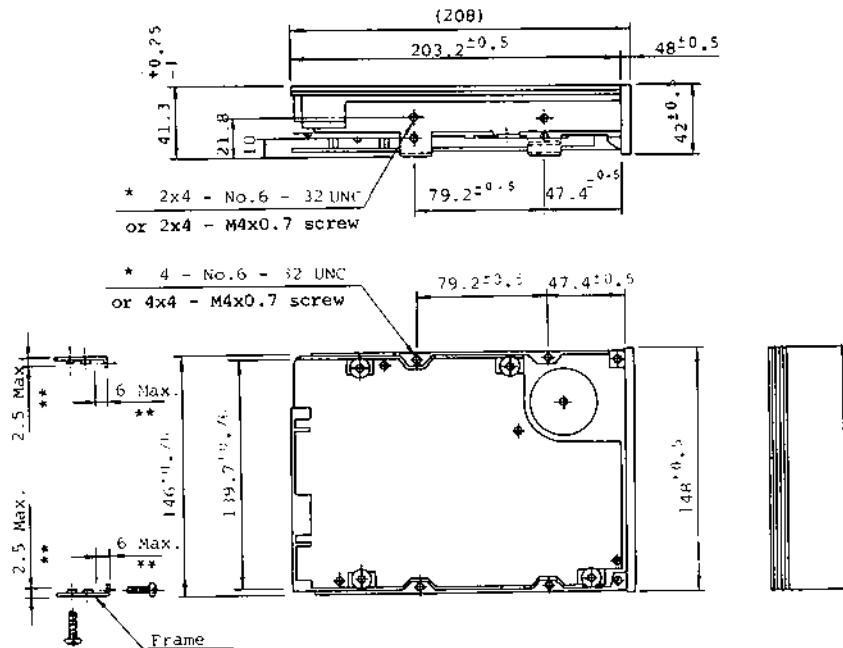
#### 4.4 Installation

Figure 4-2 shows the external dimensions and installation dimensions of the drive. Installation directions are as follows:

Vertical: on either side  
 Horizontal: circuit board side down

The following precautions should be taken when installing the drive in its host system.

- (1) The drive must be forced air cooled.
- (2) The drive must be installed so as not to put undue strain on the unit frame. (See Figure 4-3.)



\* Mounting screws are available in metric or imperial sizes.

\*\* 2.5 and 6 are screw penetrations from frame surface.

Figure 4-2 External Dimensions and Installation Dimensions

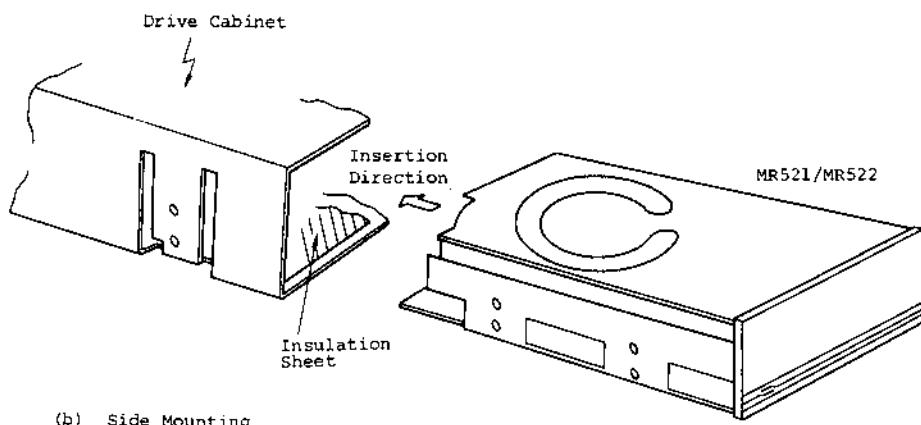
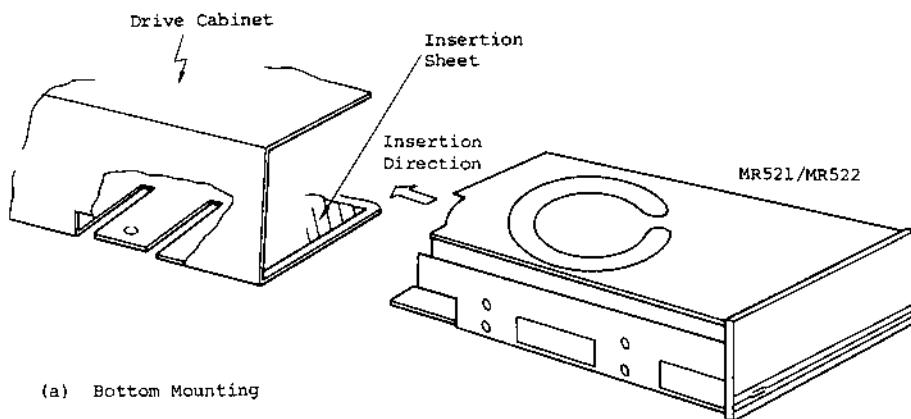


Figure 4-3 Drive Installation Examples

#### 4.5 Cable Connection

The power should be turned off when connecting or disconnecting cables. Connect the host system's DC power supply cable to connector J6 and the host system's signal cables to J1 and J2. Figures 4-4 and 4-5 show the relationship between connector pin numbers and their respective signals and Figures 4-6, 4-7, and 4-8 show the connector's physical shapes.

#### 4.6 Ground

The signal ground and BASE frame ground of this drive are connected. The fasten tab (AMP P/N61761-2 or equivalent) is shown in Figure 5-1, this is the drive ground and should be connected to the host system's DC ground.

Connector: AMP P/N62187-1

Care should be taken when grounding the drive as the noise tolerance of the drive can be adversely affected by inadequate grounding.

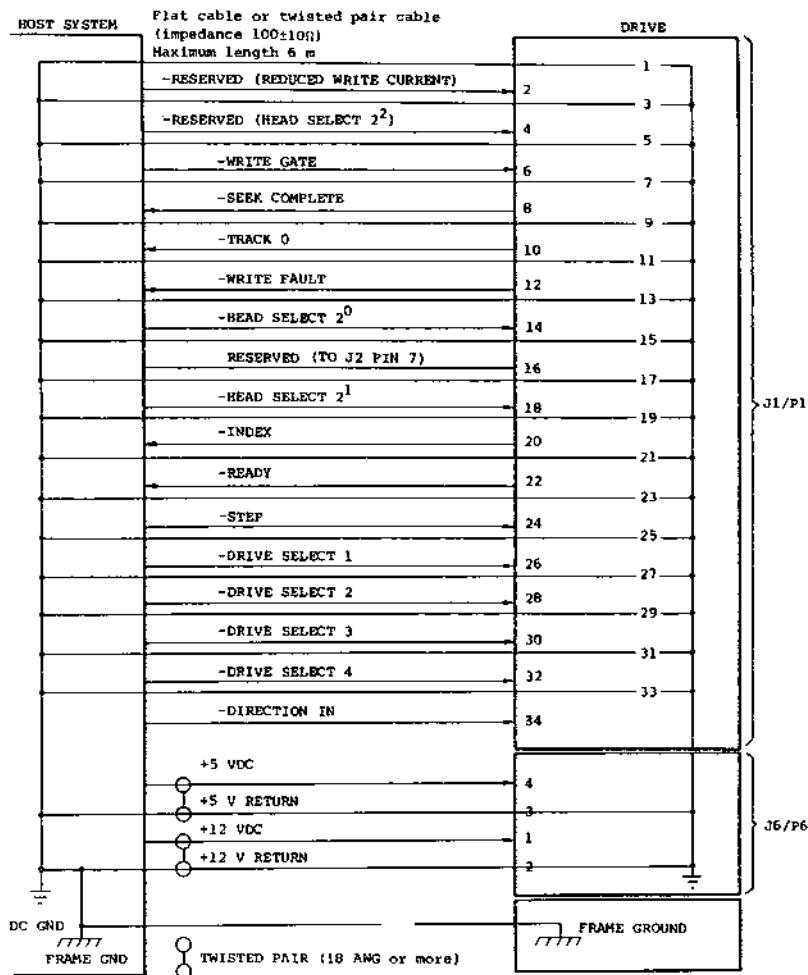


Figure 4-4 Control Signals (J1/P1 Connectors) and DC Power Supply (J6/P6 Connectors)

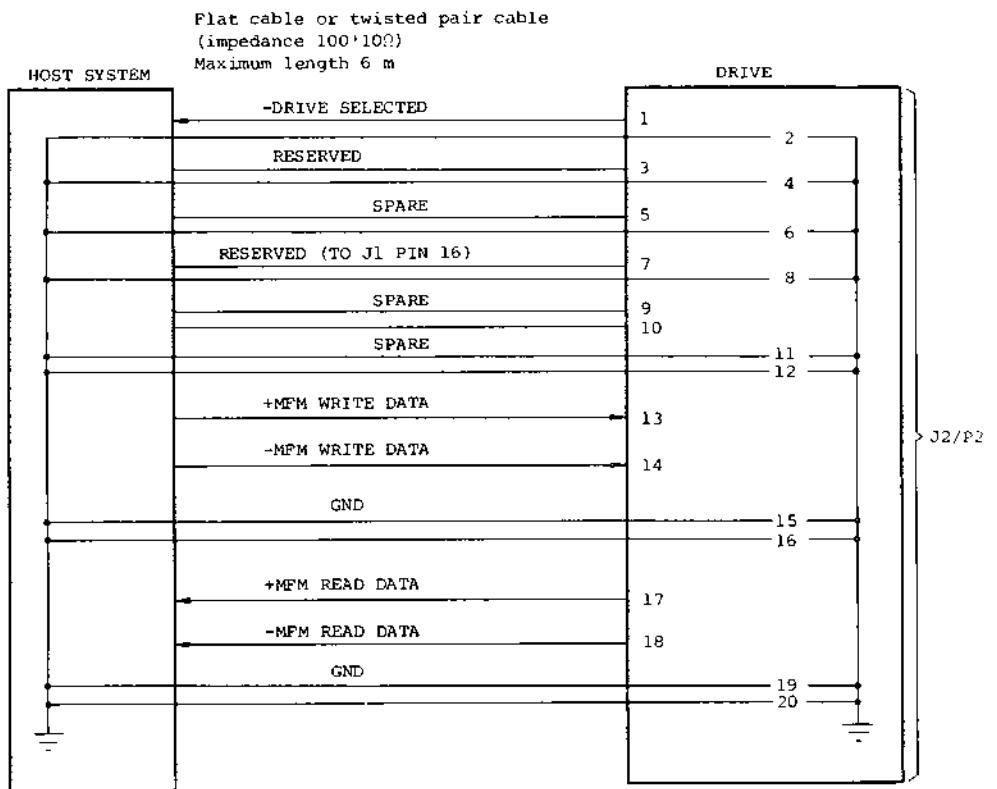


Figure 4-5 Read/Write Signals (J2/P2 Connectors)

Mating connector: 3 M ribbon connector  
P/N3463-001 or equivalent

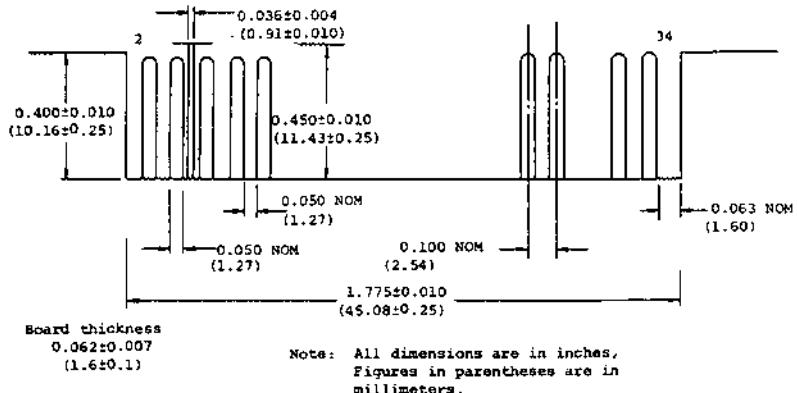


Figure 4-6 J1 Connector External

Mating connector: 3 M ribbon connector  
P/N3461-0001 or equivalent

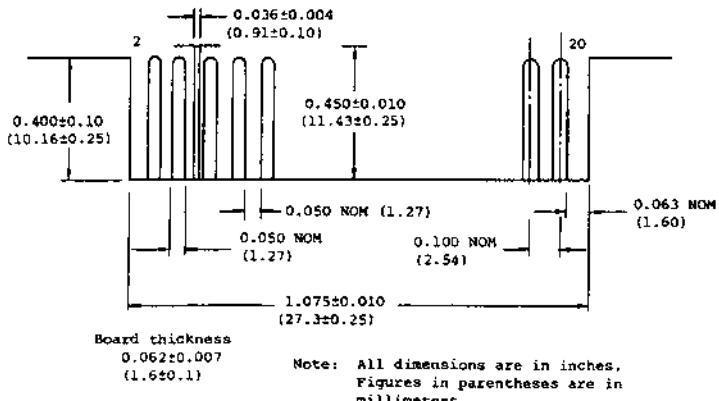


Figure 4-7 J2 Connector External

(The connector J6 is a DC Power connector. With this drive, a P/N 350211-1 AMP Mate-N-lock connector is mounted on the PCA. The pin configuration for this connector as seen from the insertion side is shown in Figure 4-8.)

Mating connector and pins: AMP P/N 1-480424 (housing)  
AMP P/N 61473-1 (pin connector)

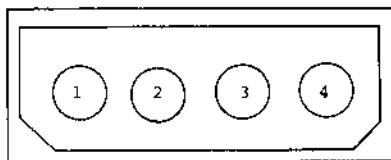


Figure 4-8 Connector J6 (External)

#### 4.7 Option Switches

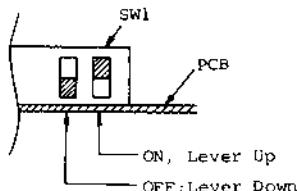
There are two switches (SW1, SW2) on the main circuit board of this drive. These switches are used to specify the drive address, interface signal termination, and radial option. Figure 4-9 shows the option switch designations.

##### 4.7.1 Drive select

When multiple units are connected, SW1 is used to set the drive address (DS1 to DS4) to match the DRIVE SELECT signals 1 to 4 and thus select a drive. Drive address settings are shown in Table 4-1.

Table 4-1 Drive Address Settings

SW1		Drive Address			
Bit	Mark	1	2	3	4
3	DS4	OFF	OFF	OFF	ON
4	DS3	OFF	OFF	ON	OFF
5	DS2	OFF	ON	OFF	OFF
6	DS1	ON	OFF	OFF	OFF



\* Marks DS1 to DS4 are printed on the printed circuit board.



#### 4.7.2 Terminator

SW2 is used for interface signal termination. Set all SW2 switches of the last drive to ON (lever up) and all SW2 switches of other drives to OFF (lever down). See Figure 4-10.

#### 4.7.3 "R" (Radial operation) option

On shipment from the factory, bit no. 1 of SW1 (marked "R") is set to ON. The drive will input then only output control signals when enabled by a DRIVE SELECT signal corresponding to that set on the drives select address setting. (daisy chain operation)

When SW1 bit no. 1 is turned off, the input/output of control signals is enabled regardless of the DRIVE SELECT signal. (Radial operation)

When the "R" option is used, the DRIVE SELECTED indicator on the front of the drive will not light when the drive is selected. To turn this indicator on, apply the DRIVE SELECT signal in the same manner as in a daisy-chain operation.

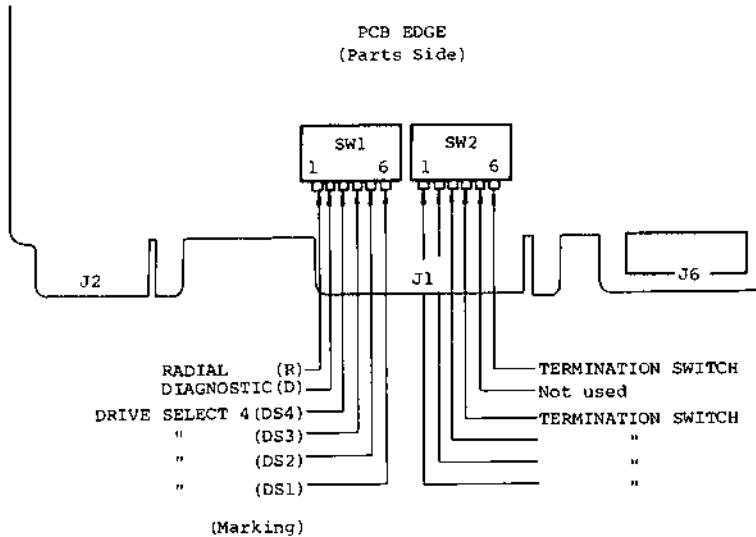


Figure 4-9 Option Switches

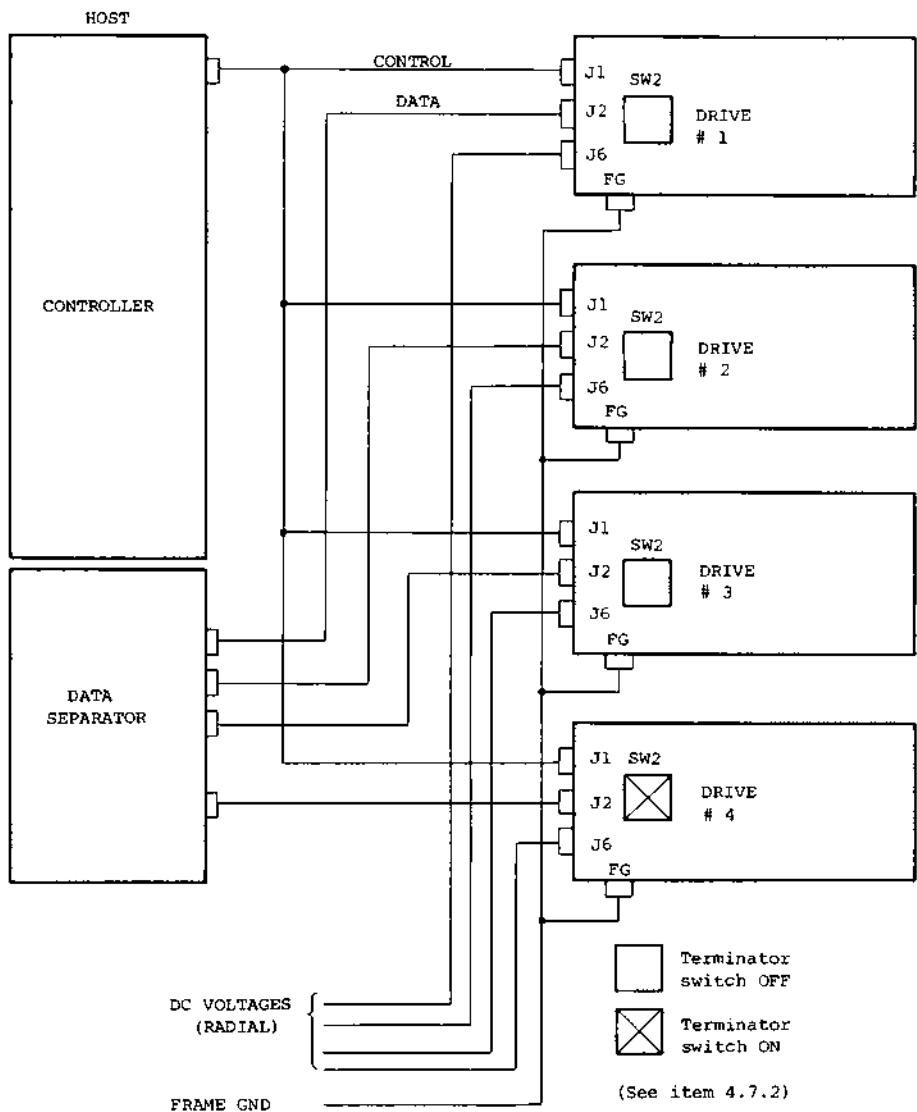


Figure 4-10 Multiple Drive Connection (4 Drives)



#### 4.7.4 "D" (Diagnostic) option

Before turning on the power set the switch marked "D" on switch assembly SW1 to on. This action will select the diagnostic option. After the power is applied and spindle spins at the specified a rotating speed, the drive will start a diagnostic seek operation.

And then the switch (SW1-D) is set off position, the head will automatically position itself in the shipping zone for shipment. The switch should be maintained in an "off" position for normal drive operation.

## 5. MAINTENANCE

This unit requires no periodic maintenance.

Field maintenance is limited to replacement of the PCA, front panel, fram L, fram R, cushions, and disk enclosure. Figure 5-1 shows these parts.

The cover on the disk enclosure containing the head and disk assembly must not be opened in the field or the unit's warranty will be invalidated.

### 5.1 Parts Replacement

#### 5.1.1 Precautions

- (1) Turn off the power when replacing parts.
- (2) Do not turn the spindle motor counter clockwise (see Figure 5-1) when replacing parts.
- (3) Do not turn the damper when replacing parts.

If precautions (2) and (3) are not observed, the disk surface may be damaged.

#### 5.1.2 Replacement procedure

##### 5.1.2.1 PCA (Printed circuit assembly) NPPCR

Tool: Allen keys

- (1) Remove the four screws holding the circuit board.
- (2) Remove connectors P3, P4, P5, P7, and P9 from the printed circuit board.  
Be careful not to damage the FPC when removing connector P3.
- (3) To re-assemble reverse the above procedure.

#### **5.1.2.2 Front panel**

Tool: plastic screw driver (no. 2)

- (1) Remove the two screws holding the front panel to frame L and frame R and then remove the front panel from the frames.
- (2) Remove connector P3 from PCA, NFPCR.
- (3) To reassemble, reverse the above procedure.

#### **5.1.2.3 Frame L/Frame R**

Tool: plastic screw driver (no. 2)

- (1) Remove PCA, NFPCR according to procedure 5.1.2.1.
- (2) Remove the front panel according to procedure 5.1.2.2.
- (3) Remove the four screws attached to the base through both frames and the cushion assembly.
- (4) Remove both frames and eight washers on the top and bottom of the cushion assembly.
- (5) Remove the four cushion assemblies from both of the frames.
- (6) To reassemble with new frames, reverse the above procedure.

#### **5.1.2.4 Cushion assembly**

Tool: plastic screw driver (no. 2)

- (1) Remove frame L and frame R according to procedure outlined above in section 5.1.2.3.
- (2) Replace cushion assembly.
- (3) Reverse procedure 5.1.2.3 and attach frame L and frame R to base.

#### **5.1.2.5 Disk enclosure**

Tool: plastic screw driver (no. 2)

- (1) Remove the PCA, NFPCR and front panel according to procedures 5.1.2.1 and 5.1.2.2.
- (2) Attach PCA, NFPCR and front panel to the new enclosure according to procedures 5.1.2.1 and 5.1.2.2.

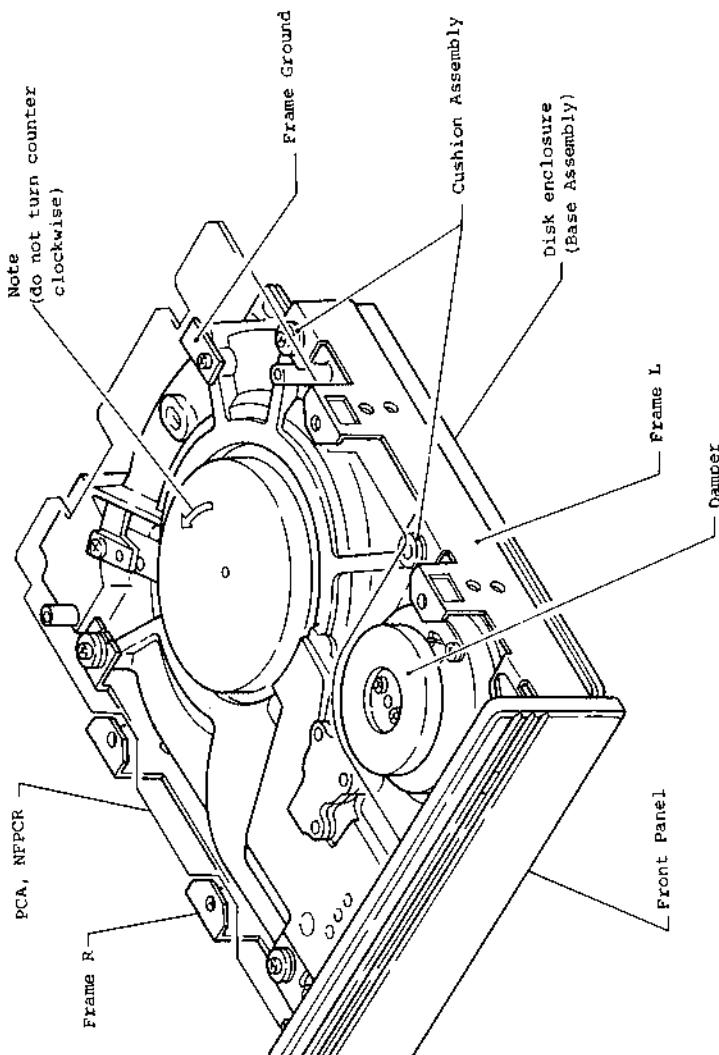


Figure 5-1 Drive Parts



Rev.	Page	Section	Description/Reason	Note	Date & Approved
A	-	-	S06-G30046A	1st Edition	August 4, 1984

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Printed in Japan 8409-500 A.S.K. 59-1000

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\* \*  
\* 20 Meg. Fixed Disk \*  
\* \*  
\* Section 4 \*  
\* \*  
\* Standard specifications \*  
\* \*  
\*\*\*\*\*

November 15, 1985





S06-G30047D

# MITSUBISHI 5.25 INCH FIXED DISK DRIVE MR 521/522

## Specifications

 MITSUBISHI ELECTRIC CORPORATION

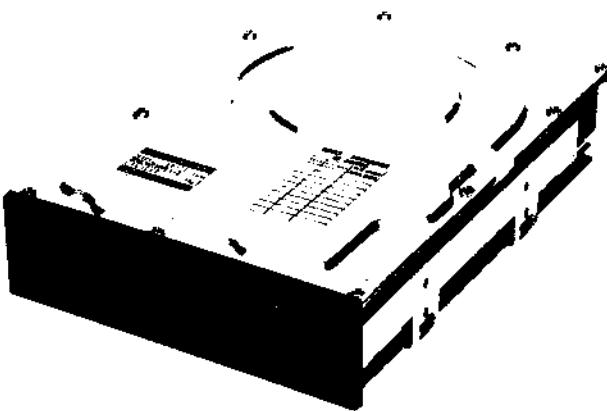


January 19, 1985

S06-G30047D

MR521/MR522 5.25 INCH FIXED DISK DRIVE

SPECIFICATIONS (12.75 MB/25.5 MB)



 MITSUBISHI ELECTRIC CORPORATION

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B	-	-	S06-G30027B	2nd Edition	Mar. 1984
-	-	-	<u>S06-G30047</u>	3rd Edition	Jun. 1984
	1-1	1.1	Editorial changed		
	1-2		Fig. 1-1 Revised		
	2-4	2.3.3	Condition and Values are changed		
	3-7	3.2.4	Note 2 in Table 3-1 is added		
	3-10	3.3.4	Write fault conditions are revised		
	3-12	3.5	- READY to - TRACK 000 timing is corrected		
	3-15	3.6.4	Diagnostic option is added		
	3-17	3.8	Shipping Zone is added		
	6-2	6.2	Write precompensation start CYL was 256		
C	1-1	1.1		4th Edition	August, 1984
	2-1	2.1	MTBF was 11000 hours		
	2-3	2.2.12	Acoustic noise is added		
	2-4	2.3.1	Storage temperature was -40° to 70°C		
	3-7		Fig. 3-6 corrected		
	3-17		Fig. 3-14 is added		
	6-3		Revised in paragraph 2		
	7-1	7.1	Revised		
	7-2		Table 7.3 is added		
		7.2	Model-M40 is added		
D				5th Edition	Jan. 1985
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## CHAPTER 1 SCOPE

These specifications are applied to the Mitsubishi 5-1/4" Mini Fixed Disk Drive (referred to below as "drive").

## 1.1 Features

This highly-reliable miniature disk drive contains a 5-1/4" fixed disk and has been designed and manufactured to the same external dimensions as a 5-1/4" half height mini flexible disk drive. The MR52X series provides large capacity and high speed, up to 25.5 M Bytes and an access time of 85 ms, in a small compact drive. The series employs many aspects of "Winchester" technology such as the disk, head, shield enc., and clean air circulation system. To achieve accurate servo system controlled by a microprocessor is utilized, the processor also being used for other task to ensure a more reliable drive.

## Key features

- |   | <u>Features</u>   |
|---|---|
| o Compact Size:                         | <ul style="list-style-type: none"><li>. Half Height 5-1/4" Winchester Disk Drive<br/>  (= Half Height Mini Floppy)</li></ul>  |
| o Proven Winchester Technology:         | <ul style="list-style-type: none"><li>. MnZn Ferrite Monolithic Heads</li></ul>   |
| o Large Capacity                        | <ul style="list-style-type: none"><li>. Up to 25.5 MB Unformatted</li></ul>   |
| o High Precision Positioning Mechanism: | <ul style="list-style-type: none"><li>. Embedded Servo System</li><li>. Micro Step Driven Stepper Motor</li><li>. Thermal Compensated Actuator</li></ul>                      |
| o High Reliability:                     | <ul style="list-style-type: none"><li>. Low Dust Level Enclosure With Air Circulation System</li><li>. Simplest Electronics on One Printed Circuit Board With LSI's</li></ul> |

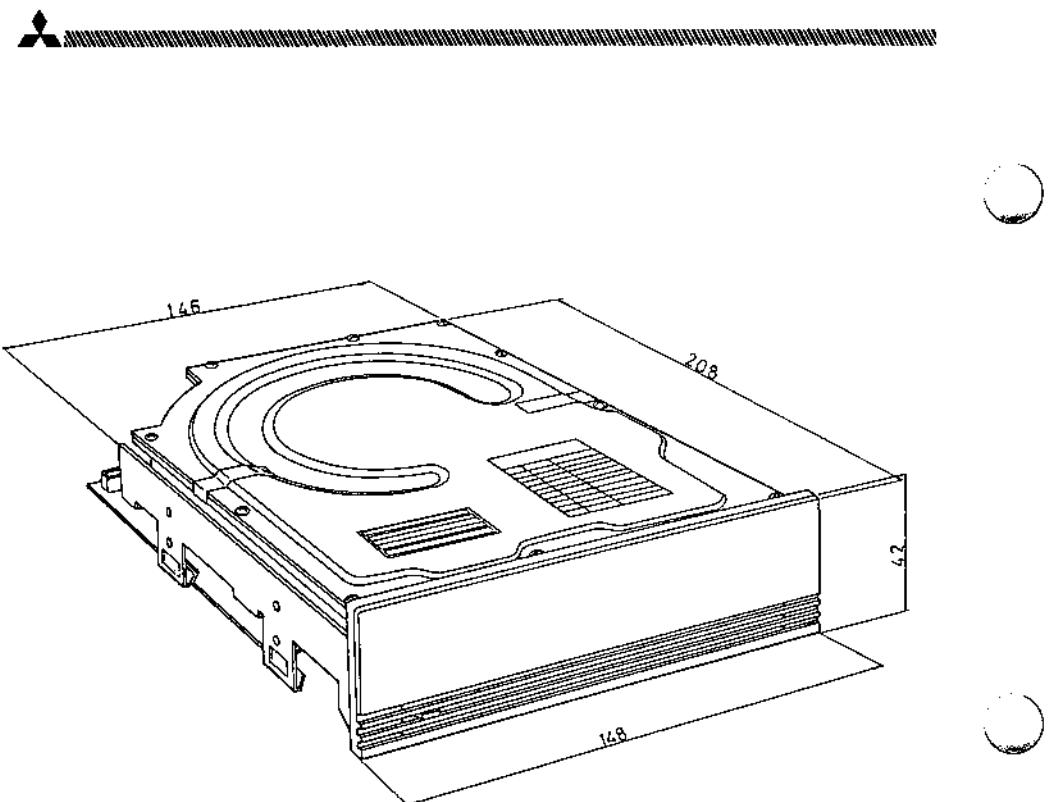


Figure 1-1 External View

CHAPTER 2 SPECIFICATIONS  
(Nominal values unless otherwise specified)

## 2.1 Summary of Specifications

ITEM	TYPE	MR521	MR522
1. MAX. CAPACITY*	TOTAL CAPACITY (M Byte) CAPACITY PER SURFACE (M Byte) TRACK CAPACITY (Byte/TK)	12.75 6.37 10416	25.5 6.37 10416
2. DISKS	NUMBER OF DISKS DATA SURFACE NUMBER OF CYLINDERS NUMBER OF TRACKS**	1 2 612 1224	2 4 612 2448
3. MAGNETIC HEADS	NUMBER OF R/W HEADS	2	4
4. RECORDING METHOD	METHOD MAXIMUM BIT DENSITY (bPI) TRACK DENSITY (tPI) DATA TRANSFER RATE (M bits/s) (K bytes/s)	HFM 9201 690 5 625	
5. ACCESS TIME	SEEK TIME TRACK TO TRACK MIN. (ms) AVERAGE*** (ms) FULL SPAN MAX. (ms) DISK ROTATIONAL SPEED (rpm) AVERAGE LATENCY TIME (ms)		18 85 199 3536 8.48
6. DIMENSION & WEIGHT	WIDTH x HEIGHT x DEPTH**** (mm) WEIGHT (kg)	146 x 41.3 x 203.2 1.6	
7. POWER SOURCE		+5 VDC ±5% 0.7 A Typ. 1.5 A Max. +12 VDC ±5% 1.0 A Typ. 3.0 A Starting	+5 VDC ±5% 0.7 A Typ. 1.5 A Max. +12 VDC ±5% 1.2 A Typ. 3.0 A Starting
8. RELIABILITY	RECOVERABLE ERROR RATE NON-RECOVERABLE ERROR RATE SEEK ERROR RATE MTBF (hour) MTTR (hour)		10 <sup>-10</sup> 10 <sup>-12</sup> 10 <sup>-6</sup> 20000 0.5
9. OPERATING	TEMPERATURE (°C), (°F) RELATIVE HUMIDITY (% R.H.)	5 - 50, 41 - 122 8 - 80	
10. INTERFACE		ST506/412 compatible	

\* Storage capacities given in Unformat values

\*\* Including alternate tracks

\*\*\* Including average settling time

\*\*\*\* Not including front panel dimensions (See Chapter 5 for details)

## 2.2 General Specifications

### 2.2.1 Processing times

#### (1) Access time

Minimum (track to track seeking): 18 ms

Maximum\* (full-track seeking): 199 ms

Average\*: 85 ms

Latency time Average: 8.48 ms

Maximum: 17.32 ms (minimum disk speed  
3465 rpm)

\* Including average settling time for embedded servo positioning

#### (2) Start/stop times

Start time (time from power-on to READY): 15 s

Stop time (time from power-off to disk stopping): 15 s

Start/stop repetition conditions: Minimum interval of 30 seconds between stopping and restarting; maximum of 1 start/stop sequence per minute

### 2.2.2 Air filtration

Superior resistance to dust.

Elimination rate of better than 99.97% for dust particles of greater than 0.3  $\mu\text{m}$  diameter. Effects of changes in altitude, atmospheric pressure, and temperature eliminated through use of special replaceable breath filter. Unnecessary to replace main filter.

### 2.2.3 Positioning method

Swing-arm system using high-performance stepping motor and band actuator in combination gives high accuracy positioning by embedded servo mechanism.

### 2.2.4 Rotation speed deviation

$\pm 2\%$  or less

2.2.5 Read error rates

The read error rates, except for errors due to media and drive defects are as follows:

(1) Recoverable errors

Errors recoverable within three retries:  $10^{-10}$  bits or less

(2) Non-recoverable errors

Errors not recoverable with 9 retries:  $10^{-12}$  bits or less

2.2.6 Service life

The unit is expected to perform satisfactorily for five years (under normal operating conditions), 20,000 hrs (continuous operation) or 8000 rotational start/stop operations whichever comes first.

2.2.7 External dimensions (nominal values, not including front panel dimensions)

Width: 146.0 mm (5.75")

Height: 41.3 mm (1.63")

Depth: 203.2 mm (8.00")

Details in Chapter 5

2.2.8 Installation method

Horizontal or vertical  
Details in Chapter 5

2.2.9 Weight

1.6 kg (3.51 lbs)

2.2.10 Heat dissipation

15 W for MR521, 18 W for MR522

2.2.11 Record media failure (tracks containing nonrecoverable errors)

Errors of more than 1 bit length: 10 tracks or less per one data head are indicated on a label affixed to the drive prior to shipment from the factory: alternate track processing is necessary for these tracks.

2.2.12 Acoustic noise

50 dbA Max. at 1 m distance.

## 2.3 Environmental Conditions

### 2.3.1 Temperature and humidity

#### (1) Operating

Temperature: 5° to 50°C  
Temperature change: Less than ±8°C/H (There must be no condensation.)  
Humidity: 8 to 80% RH (wet-bulb temperature to be less than 26°C)

#### (2) Storage

Temperature: -40° to 60°C  
Temperature change: Less than ±20°C/H (There must be no condensation.)  
Humidity: 5 to 95% RH (wet-bulb temperature to be less than 26°C)

### 2.3.2 Altitude

Operating: Below 2,000 m (6,580 ft)  
Storage: Below 12,000 m (39,370 ft)

### 2.3.3 Vibration and shock

Condition		Operating	Non-operating	
	Power supply	ON	OFF	
	Head position	Any zone	Any zone	Shipping zone
Vibration		0.4G	2G	2G
Shock		2G	3G	30G
		(Note 1)	(Note 2)	(Note 3)

(Note 1): Freq. = 5 to 500 Hz

Mode = Automatic Sweep  
(3 min/cycle x 4)

Criteria = No Read Error and No Defect Increase

(Note 2): Freq. = 5 to 300 Hz

Mode = Automatic Sweep  
(10 min/cycle x 6 cycle x 3 direction)

Criteria = No Defect Increase

(Note 3): Our standard shipping package can protect damages from 90 cm drop without any actuator lock.

Shock mount mechanism is built in base and frame.

2.3.4 Magnetic field

Less than 300 AT/m (periphery of heads)

2.3.5 Electric field

Less than 0.3 V/m

2.3.6 Dust

Less than 0.3 mg/m<sup>3</sup> (3 x 10<sup>-4</sup> oz/cubic ft)



## CHAPTER 3 INTERFACES

### 3.1 Interface Specifications

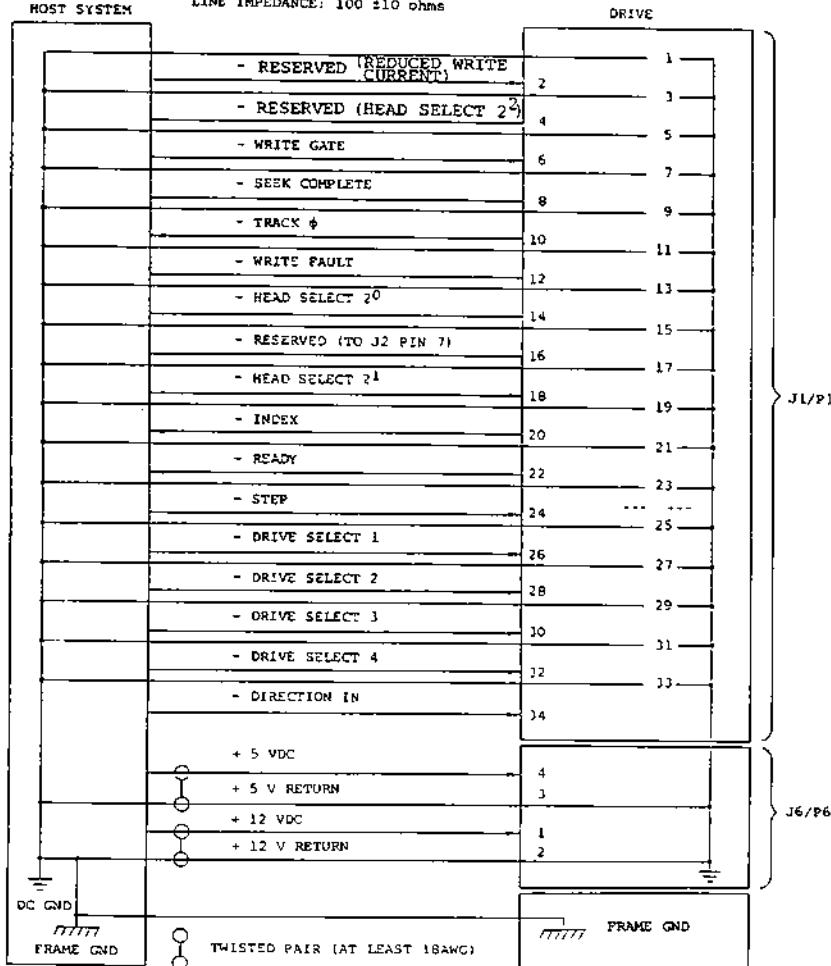
The interface provided on this drive is compatible with the ST506 fixed disk drive interface. The connectors used by this interface consist of the following four parts, each connector being a separate item.

- (1) Control signal part (J1/P1 connector)
- (2) Read/write data part (J2/P2 connector)
- (3) DC power supply part (J6/P6 connector)
- (4) Frame ground part

The interface-signal/connector-pin designations are shown in figures 3-1, 3-2.

Cable connection when two or more drives (up to four) are shown in figure 3-3. For the control signal lines (J1/P1), bus connection is used and the termination switch (SW2) is set on the final drive. Radial connection is used with the data signal lines (J2/P2).

FLAT RIBBON OR TWISTED PAIR -  
MAXIMUM LENGTH: 20 ft;  
LINE IMPEDANCE: 100 ±10 ohms



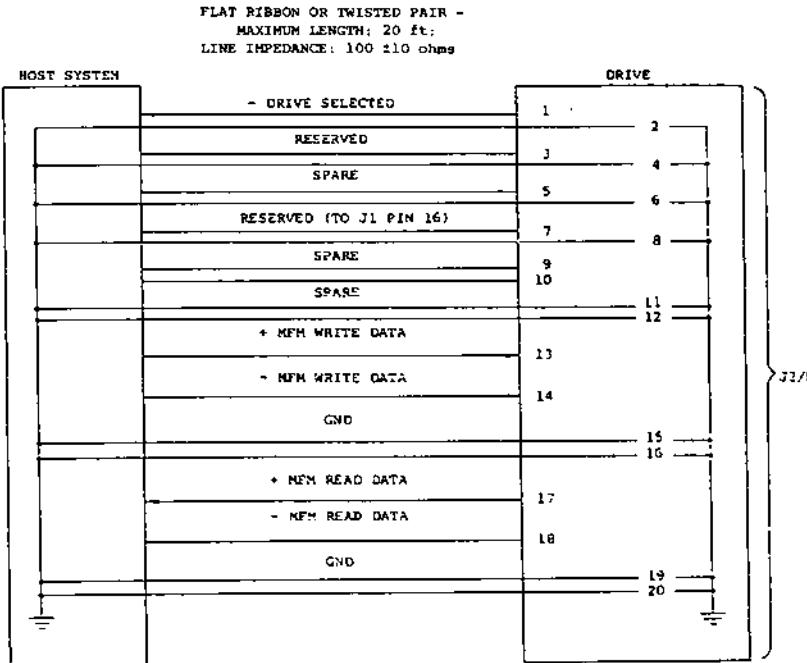


Figure 3-2 Read/Write Data Signals (J2/P2 Connector)

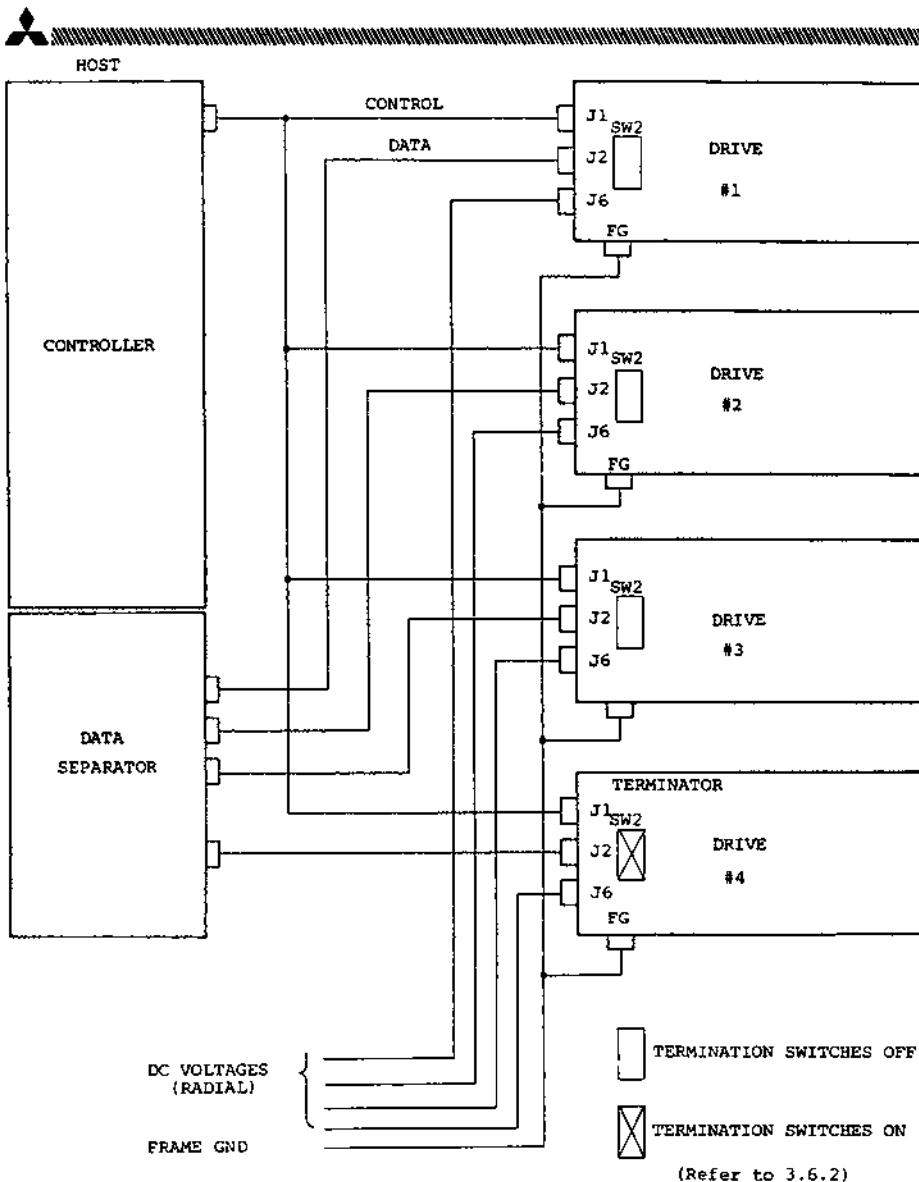


Figure 3-3 Multiple Unit Connection (Case of 4 Drives)

### 3.2 Control Input Signals

There are eleven control input signals. These being; STEP; DIRECTION IN; HEAD SELECT 2<sup>0</sup>, 2<sup>1</sup>, and 2<sup>2</sup>; WRITE GATE; REDUCED WRITE CURRENT; and DRIVE SELECT 1, 2, 3, and 4.

The recommended driver/receiver combination for the control input signal interface is shown in figure 3-4.

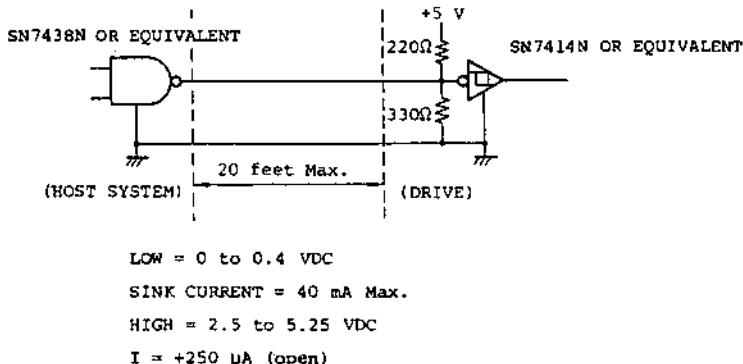


Figure 3-4 Control Input Signal Interface Circuit

#### 3.2.1 DRIVE SELECT 1 to 4

When a particular DRIVE SELECT signal is "low", control signals are sent to the drive corresponding to the selected DRIVE SELECT signal. Multiple drive selection is not possible.

Individual drive addresses are defined by using switch SW1.

#### 3.2.2 DIRECTION IN

The seek direction of the read/write head when a STEP signal is input is defined by this signal. The head seeks inward when this signal is "low" and outward when it is "high".



### 3.2.3 STEP

This signal causes the read/write head to seek in the direction specified by the DIRECTION IN signal. A seek operation is started when this signal goes from "low" to "high". The DIRECTION IN signal must be changed at least 100 ns before this signal drops to "low".

Either of two modes can be selected to perform a seek operation - normal mode or buffered mode.

#### (1) Normal mode

In this mode, the read/write heads will move at the same as the rate incoming STEP pulses. The minimum STEP interval is 3.0 ms. Refer to figure 3-5.

#### (2) Buffered mode

In this mode, short-interval STEP pulses are received by the drive's buffer counter. After the last pulse the read/write heads will move at high speed to the desired cylinder specified by the number of pulses counted. When the head is positioned on the desired cylinder, a SEEK COMPLETE signal is output.

This mode is automatically selected if the STEP pulse interval is less than 200  $\mu$ s. 120  $\mu$ s after the last pulse is input, the DRIVE SELECT signal is switched from "low" to "high" and another drive can be selected, thus overlap seeking is possible. Refer to figure 3-6.

NOTE: With pulse intervals of 200  $\mu$ s to 3.0 ms, seek operation may be unstable and accurate positioning is not guaranteed.

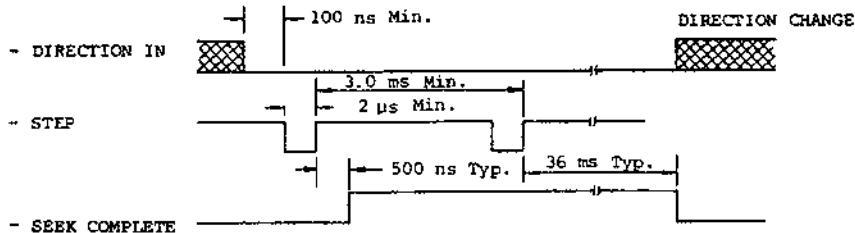


Figure 3-5 Normal Mode Timing

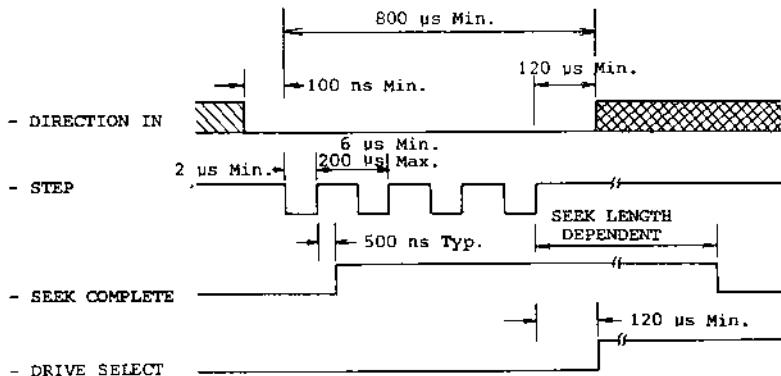


Figure 3-6 Buffer Mode Timing

3.2.4 HEAD SELECT  $2^0$ ,  $2^1$ ,  $2^2*$ 

The drive is equipped with four heads. With HEAD SELECT signals, a combination of two binary bits is used to select the head. The head-selection combinations used are shown in table 3-1. Refer to figure 3-7 for head-selection timings.

\*HEAD SELECT  $2^2$  signal is not used in this drive.

Table 3-1 Head-Selection Combination

Head Select		Selected Head Address
$2^0$	$2^1$	
0	0	0
1	0	1
0	1	2
1	1	3

NOTE 1: With HEAD SELECT  $2^0$ ,  $2^1$ ; 0 = "high" and 1 = "low"

2: HEAD SELECT  $2^1$  signal is used in MRS22.

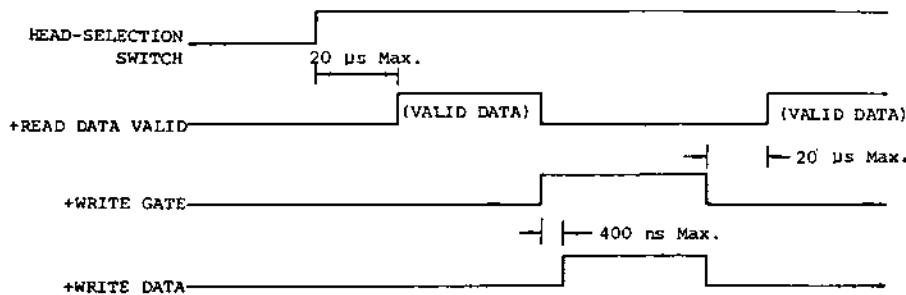


Figure 3-7 Head-Switching Timing

### 3.2.5 WRITE GATE

When this signal is "low", write data is written onto the disk.

When this signal is "high", read data read from the disk is transmitted to the interface. Seek operations and the receipt of step pulses are only possible when this signal is "high".

Refer to figure 3-7 for WRITE GATE signal timings.

This signal should not become active for more than 200 ns due to noise produced by on/off switching of the controller power supply.

### 3.2.6 REDUCED WRITE CURRENT

The REDUCED WRITE CURRENT signal is not used by this drive.

Write current switching is controlled by a circuit inside the drive.

## 3.3 Control Output Signals

The drive output five control signals, TRACK 000, INDEX, READY, WRITE FAULT, and SEEK COMPLETE. Each of these signals is output only when a given drive is selected.

The recommended driver/receiver combination for the control output signal interface is shown in figure 3-8.

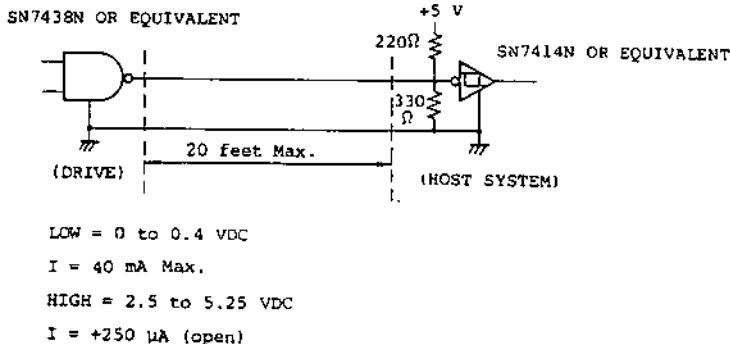


Figure 3-8 Control Output Signal Driver/Receiver

### 3.3.1 TRACK 000

When this signal is "low" the head that has been selected is positioned at Track 0 (the outermost data track) and the stepping motor is in the correct phase.

### 3.3.2 INDEX

This signal is output exactly once per disk rotation (16.97 ms period) and indicates the track starting position. The timing for this signal is shown in figure 3-9.

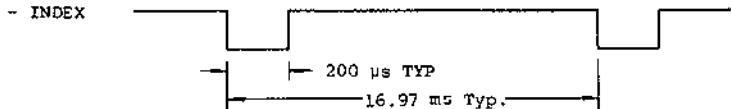


Figure 3-9 INDEX Signal Timing

### 3.3.3 READY

When this signal is "low" and the SEEK COMPLETE signal is "low", the drive is ready to perform a read/write or seek operation.

When this signal is "high", the write or seek operation is inhibited.

The READY signal goes to "low" when the disk attains a rotating speed that is steady and within 5% of the specified speed (3,359 to 3,713 rpm). 15 s (typ.) is required from power-on until the READY signal is set.

#### 3.3.4 WRITE FAULT

When this signal is "low" one of the following faults has occurred in the drive and write operation cannot therefore, be carried out.

- (1) An open head in the drive.
- (2) Write current does not flow even though a WRITE GATE signal has been input.
- (3) Write gate present but no Transition of MFM write data line.
- (4) There has been an abnormal drop in the DC power supply (+12 V, +5 V).

In the case of condition "(4)", the WRITE FAULT signal is reset automatically when the voltage returns to a nomal level.

#### 3.3.5 SEEK COMPLETE

When this signal is "low" a seek operation has been completed and the head is positioned on the desired track. When this signal is "high", read/write operations cannot be executed. The SEEK COMPLETE signal will go "high" in the following cases.

- (1) The recalibration sequence is in progress when the power is turned on and the head is not positioned at Track 000.
- (2) The SEEK COMPLETE signal goes to "high" 500 ns (Typ) after the trailing edge of a STEP pulse or series of step pulses.

### 3.4 Data-Input/Output Signals (J2/P2 connector)

There are two kinds of data signals, MFM WRITE DATA and MFM READ DATA. These are sent to the host system as differential signals via the connector J2/P2.

The recommended driver/receiver circuit for the data-input/output interface is shown in figure 3-10.

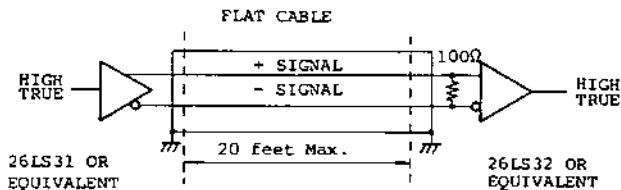


Figure 3-10 Data-Input/Output Signal  
Driver/Receiver Combination

#### 3.4.1 MFM WRITE DATA

This is a differential signal that defines the flux transition (data bits) to be written onto the disk. A flux change occurs when +MFM WRITE DATA is more positive than -MFM WRITE DATA with the WRITE GATE signal active. The MFM WRITE DATA signal should be inactive (+MFM WRITE DATA more negative than -MFM WRITE DATA) when a read operation is being executed. The signal timing is shown in figure 3-11.

#### 3.4.2 MFM READ DATA

This is a differential signal for sending read data from the disk to the host system. The point at which the potential of +MFM READ DATA is more positive than that of -MFM READ DATA with the WRITE GATE signal inactive indicates the point of flux change for the data read from the disk. The timing for this signal is also shown in figure 3-11.

#### 3.4.3 Select status

Besides the data-input/output signals, there is also a DRIVE SELECTED signal that is sent via the J2/P2 connector interface. This signal indicates that a DRIVE SELECT signal matching one of the drive-selection switch (DS1 to 4) settings has been input and that the corresponding drive has thus been selected. The driver/receiver conditions applying to this signal are the same as those for the control output signals as shown in figure 3-8.

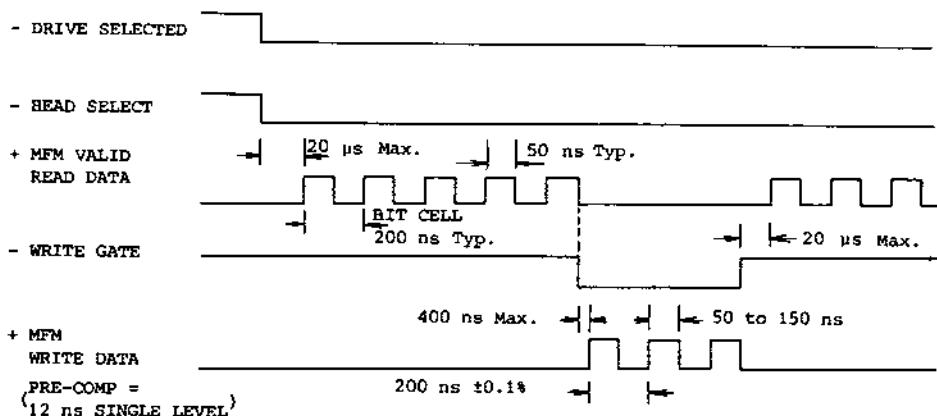


Figure 3-11 Timings for Read/Write Data

### 3.5 Power-On Sequence

A load sequence in which the head is recalibrated to Track 0 is automatically executed when the power is turned on. This load sequence is executed under the following power-on conditions.

- . The STEP signal of the J1/P1 connectors is inactive.
- . The spindle spins at the specified rotating speed.

Power-on timing sequence is as shown in figure 3-12.

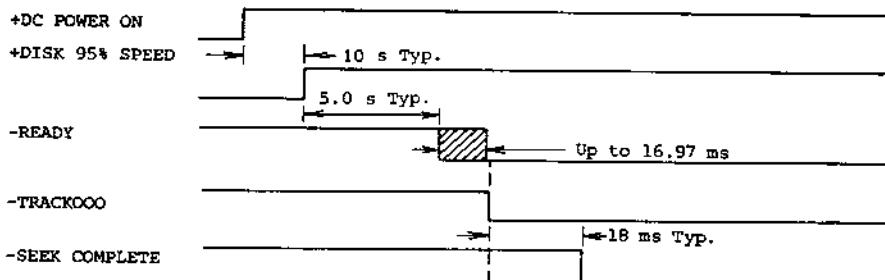


Figure 3-12 Power-On Sequence

### 3.6 Customer-Option Switches

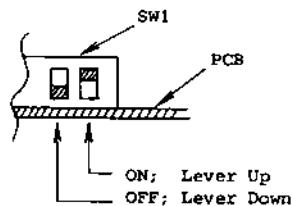
There are two switches on the main circuit board of this drive. The drive address can be specified and the customer-option functions described in 3.6.1 through 3.6.3 are selected with these switches. Refer to figure 3-13 for setup.

#### 3.6.1 Drive Select

In multiple unit connection it is necessary to configure each drive with a unique address. To select the desired drive number in a daisy-chain operation, refer to table 3-2.

Table 3-2 Drive Selection Configuration

SW1		Drive Select Number			
Bit	*Mark	1	2	3	4
3	DS4	OFF	OFF	OFF	ON
4	DS3	OFF	OFF	ON	OFF
5	DS2	OFF	ON	OFF	OFF
6	DS1	ON	OFF	OFF	OFF



\* Mark is printed on Printed Circuit Board (PCB).

#### 3.6.2 Terminators

To provide termination for the last unit, all switches of SW2 should be set in ON position --- lever up.

On all other units, all the switches of SW2 should be set in OFF position --- lever down. (See figure 3-13).

### 3.6.3 Radial option

On leaving the factory, the switch marked "R" of SW1 is set in the ON position --- lever up and the transfer of control signals to and from the drive is enabled only when the address of DRIVE SELECT 1, 2, 3, or 4 matches the drive address (daisy-chain operation).

When this switch is in the OFF position --- lever down, the transfer of control signals is enabled regardless of the DRIVE SELECT signal (radial operation).

When the "R" option is used, the "Drive Selected" indicator lamp on the front of the drive does not light. To make this lamp light, a DRIVE SELECT signal shall be applied.

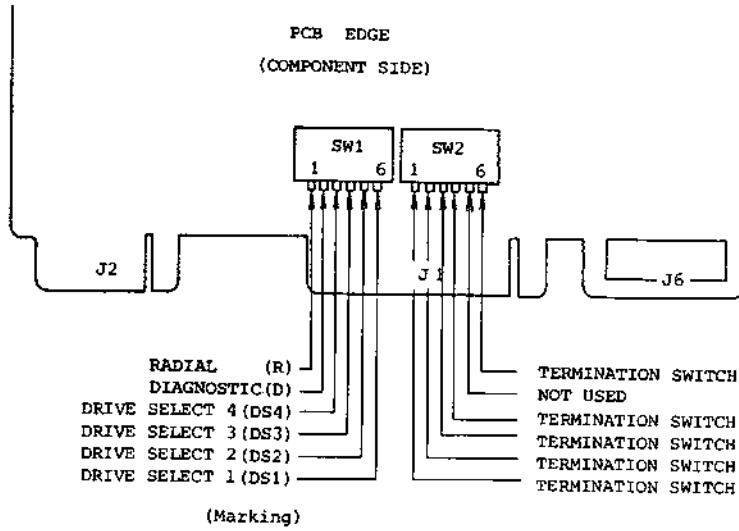


Figure 3-13 Customer-Option Switches

### 3.6.4 Diagnostic option

Before turning on the power set the switch marked "D" on switch assembly SW1 to on. This action will select the diagnostic option.

After the power is applied and spindle spins at the specified rotating speed, the drive will start a diagnostic seek operation.

And then the switch (SW1-D) is set off position, the head will automatically position itself in the shipping zone for shipment. The switch should be maintained in an "off" position for normal drive operation.

### 3.7 Power Interface

This drive requires an external DC power supply. Pin designations for the DC-power connector J1/P6 and the power requirements are shown in table 3-3.

Table 3-3 Power Connector

J6/P6 Pin No.	DC power	Power conditions	Ripple conditions
1	+12 V $\pm 0.6$ V	1.0 A Typ. (MR521) 1.2 A Typ. (MR522) 3.0 A Starting	100 mVp-p Max.
2	+12 V Return		
3	+5 V Return		
4	+5 V $\pm 0.25$ V	0.7 A Typ. 1.5 A Max.	50 mVp-p Max.

Spike noise: 4% or less

#### 3.7.1 Power-on time

The power should reach 90% of its final value within one second. When the power reaches the 90% level, an unsafe condition is cleared automatically.

#### 3.7.2 Power cut-offs

The recorded data is protected even in the event of an abnormal DC power condition, except when a write operation is being executed.

### 3.7.3 Power on/off sequence

Common power use with the host system is recommended for the +5 V power supply.

When separate power supply is used, the host system power should be turned on first, and then that of the drive(s). When turning off the power, the drive power should be turned off first, and then that of the host system.

Whenever a separate +12 V power supply is used, no particular power sequence need.

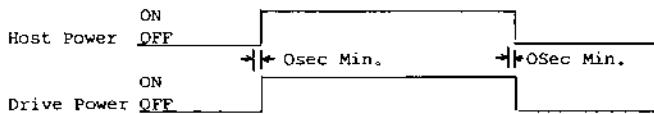


Figure 3-14 Power on/off sequence

### 3.8 Shipping Zone

In order to prevent damage to the head and disk caused by vibration and shock during shipment, an shipping zone is provided for head storage. The shipping zone is located on the inner most track at cylinder 665.

The head can be located in this zone by either of the following methods:

- (1) When the drive is in the ready state, the head can be moved by to cylinder 665 by seek operation.
- (2) After the switch (SW1-D) is set in the on position, turning on the power of the drive, the drive will start a seek operation.

N.B. Return switch SW1-D to the off position to ensure normal operation.

In diagnostic operation (cf. 3.6.4) switch off after diagnostic seek operation, then the head will be automatically moved to cylinder 665.

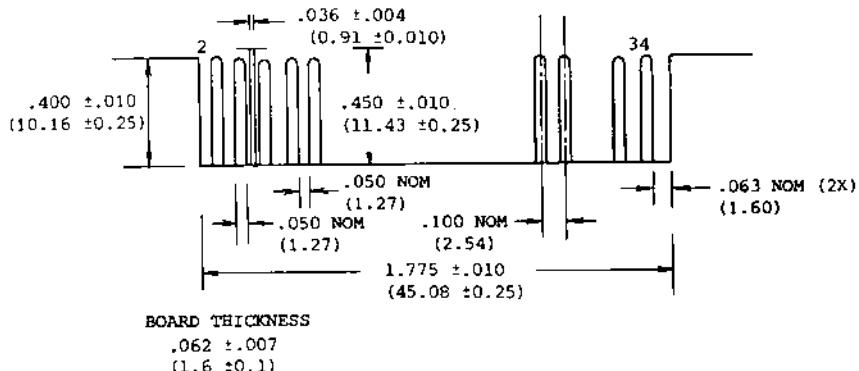


## CHAPTER 4 CONNECTORS

## 4.1 Connector J1/P1

Connector J1 is a 34-pin PCB edge connector. The dimensions of this connector are shown in figure 4-1. The pins are numbered from 1 to 34, with even numbers being on the component side of the circuit board and the odd numbers on the soldered side. There is a key slot between Pins 4 and 6.

Mating connector: 3M ribbon connector P/N 3463-0001 or equivalent



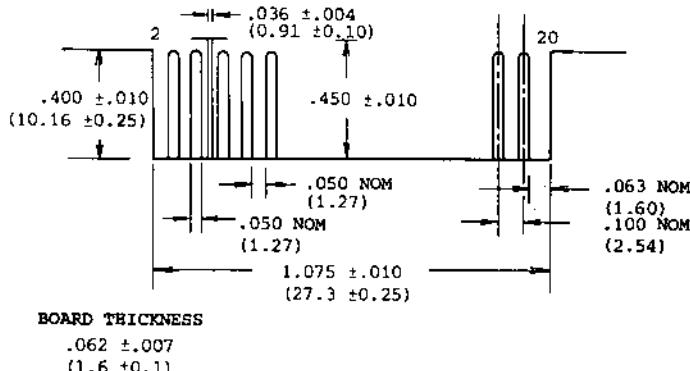
Note: All dimensions are in inches.  
(Dimensions in parentheses are in millimeters)

Figure 4-1 External Dimensions of Connector J1

## 4.2 Connector J2/P2

The connector J2 is a 20-pin PCB edge connector. The dimensions of this connector are shown in figure 4-2. The pins are numbered from 1 to 20, with the even numbers being on the component side of the circuit board. There is a key slot between Pin 4 and Pin 6.

Mating connector: 3M ribbon connector P/N 3461-001 or equivalent



Note: All dimensions are in inches.  
Figures in parentheses are in millimeters.

Figure 4-2 External Dimensions of Connector J2

#### 4.3 Connector J6/P6

The connector J6 is a DC-power connector. With this drive, a P/N 350211-1 AMP Mate-N-lock connector is mounted. The pin configuration with this connector as seen from the insertion side is shown in figure 4-3.

Mating connector and pins: AMP P/N 1-480424 (housing)  
AMP P/N 614D3-1 (pin connector)

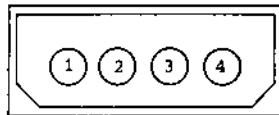


Figure 4-3 Connector J6

#### 4.4 Frame-Ground Connector

With this drive, the DC ground for the PCB and the frame-ground for the base are connected. The frame-ground connector for this drive is a P/N 61761-2 AMP Faston terminal.

Mating connector: AMP P/N 62187-1

**CHAPTER 5 INSTALLATIONS**

**5.1 Installation Dimensions and Installation Positions**

The external dimensions and installation dimensions are shown in figure 5-1. The installation directions are as follows:

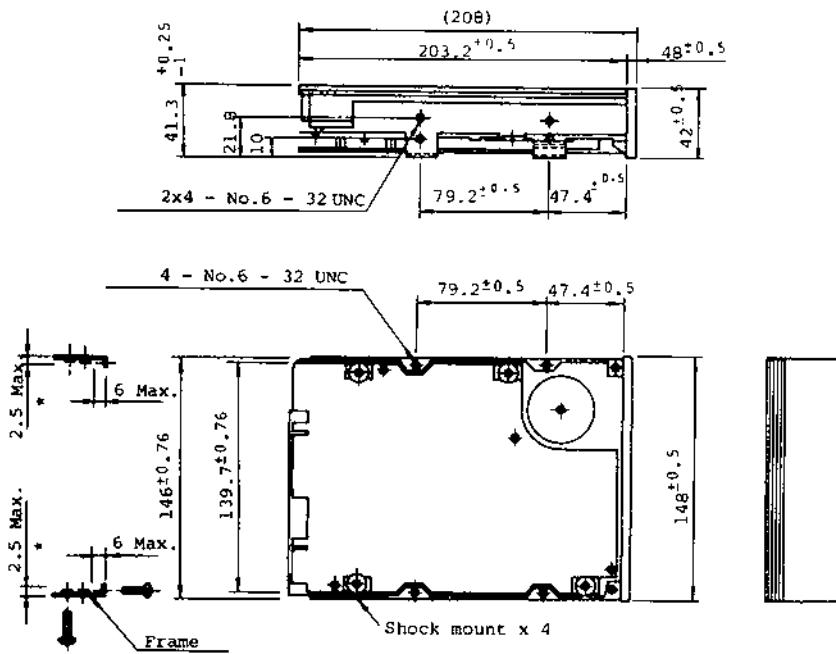
Vertical:              on either side

Horizontal:            PCB down

When installing the drive in its final location, particular attention must be paid to the following points.

- (1) Ventilation, adequate ventilation must be provided to allow any heat generated to dissipate.
- (2) Serviceability
- (3) The drive must be so installed so as to put no under strain on the units frame.

Installation Positions are shown in figure 5-2.



\* Vertical Screw Penetration 2.5 mm Max

Horizontal Screw Penetration 6.0 mm Max

Figure S-1 External Dimensions and Installation Dimensions

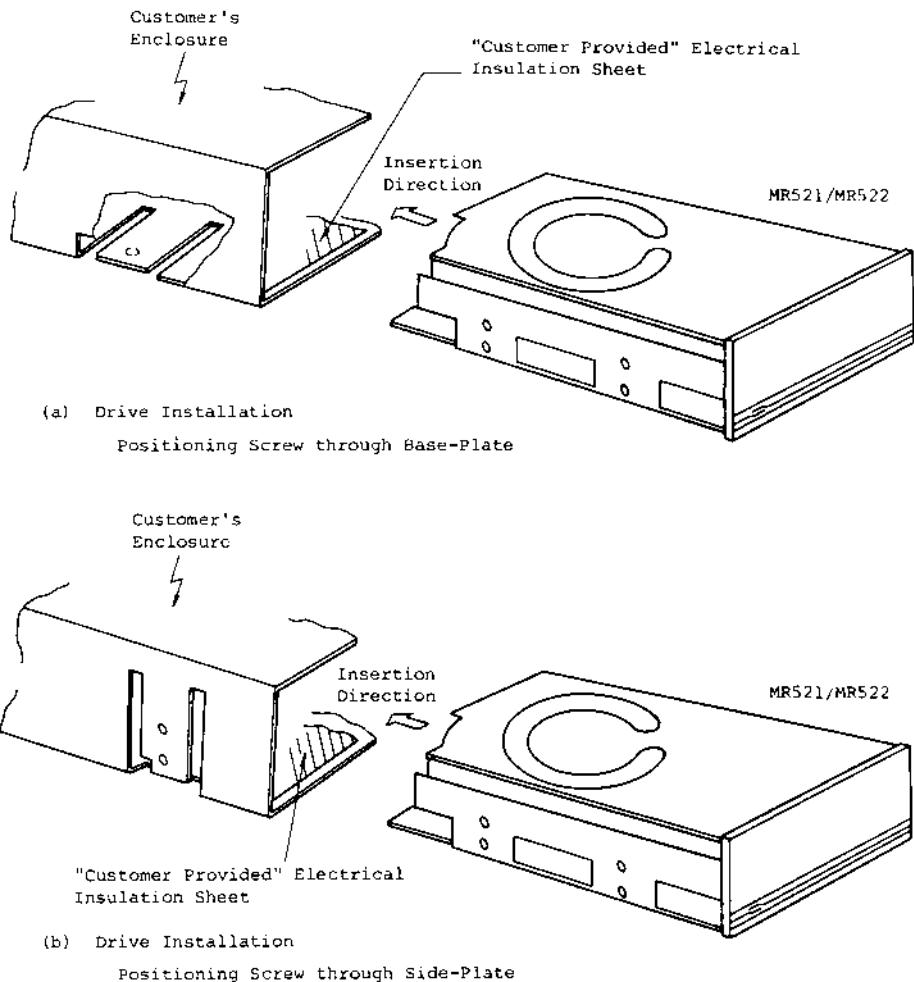
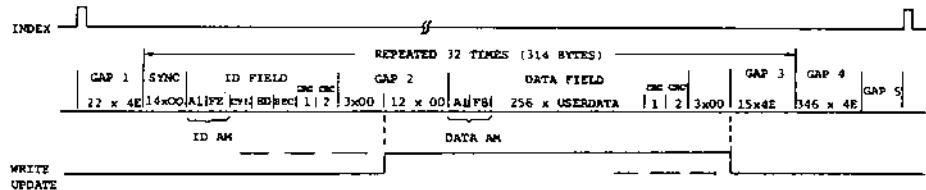


Figure 5-2      Installation Positions



## CHAPTER 6 RECOMMENDED TRACK FORMAT



- NOTE:
- 1) Usable track capacity: 10,416 bytes nom., 10,207 bytes min. (rotation deviation of 2%)
  - 2) Write to read recovery time: 35  $\mu$ s
  - 3) Head switching time: 30  $\mu$ s
  - 4) GAP 5: Embedded servo area which is write-protected in disk drive.

GAP1:	[4E] <sub>16</sub>	22 bytes	22 bytes
SYNC:	[00] <sub>16</sub>	14 bytes	
ID, AM:	[A1] EF <sub>16</sub>	2 bytes	
CYLINDER & HEAD:	[XX] <sub>16</sub>	2 bytes	
SECTOR:	[00-1F] <sub>16</sub>	1 byte	
CRC (ID)	[XX] <sub>16</sub>	2 bytes	
WRITE TURN ON:	[00] <sub>16</sub>	3 bytes	
GAP2:	[00] <sub>16</sub>	12 bytes	
DATA, AM:	[A1] F8 <sub>16</sub>	2 bytes	
DATA:	[XX] <sub>16</sub>	256 bytes	
CRC (DATA):	[XX] <sub>16</sub>	2 bytes	
WRITE TURN OFF:	[00] <sub>16</sub>	3 bytes	
GAP3:	[4E] <sub>16</sub>	15 bytes	
GAP4:	[4E] <sub>16</sub>	346 bytes	346 bytes
GAP5:		187 bytes	187 bytes

Total: 10603 bytes  
(Including embedded servo area: 187 bytes)

## 6.1 Gap Length Calculations

### (1) Gap 1

Gap 1 compensates for deviation due to read-data transience and index-detection deviation occurring at the time of head switching. Due to the existence of this gap, the head designation can be switched for each index and the tracks of the respective cylinders read without any rotation wait time. Gap 1 has a minimum length corresponding to 22 bytes (approximately 35  $\mu$ s).

### (2) Gap 2

Gap 2 is located after the ID field and separates the data field and the ID field. This gap is used to compensate for the splice point occurring when the WRITE GATE signal goes on and to synchronize read data in order to find the data-field address mark (data AM). The length of Gap 2 is determined by the synchronization time of the data-separator VFO.

### (3) Gap 3

Gap 3 is located after the data field and compensates for sector capacity tolerance occurring with the respective sectors due to deviation in the speed of disk rotation ( $\pm 2\%$ ). Gap 3 must have a minimum length corresponding to 15 bytes (with the 32 sectors/track format).

### (4) Gap 4

Gap 4 compensates for track capacity tolerance occurring with the respective tracks due to deviation in the speed of disk rotation ( $\pm 2\%$ ).

### (5) Gap 5

Gap 5 is used for embedded servo area which is write-protected in disk drives.

## 6.2 Write Precompensation

When a particular data pattern is written, bit shifting due to the superposition of the magnetization patterns of adjacent bits can occur, causing errors. Precompensation is used to prevent this. With this precompensation, when data is written, the write timing is switched beforehand to the opposite direction of the data-shift direction. The duration of the timing switch for nominal bit positions is -12 ns (early) or +12 ns (late).

Bit patterns for which precompensation should be executed are shown in Table 6-1. As shown in this table, the bit patterns are monitored in 4-bit shift registers with compensation being effected with the timing of the third bit.

In order to provide for a satisfactorily lower error rate for the drive, the host-system timing for MFM write data may not be pre-compensated at all tracks or pre-compensated at track numbers greater than 256, in accordance with the model number of the drive. (See Table 7.3)

Table 6-1 Write Precompensation Patterns

<u>Bit Patterns</u>	<u>Bit Shift Direction</u>
0000	= On Time Clock
0001	= Late Clock
0010	= On Time Data
0011	= Early Data
0100	-
0101	-
0110	= Late Data
0111	= On Time Data
1000	= Early Clock
1001	= On Time Clock
1010	= On Time Data
1011	= Early Data
1100	-
1101	-
1110	= Late Data
1111	= On Time Data

The 3rd digit is compensation bit for all Bit Pattern.

- o Direction of precompensated MFM pulses should be inverted from the "Bit Shift Direction".

### 6.3 Remarks

- (1) Write-protected area (Gap 5) used for embedded servo is located in the data track in the MR521/MR522.
- (2) CRC code is described in this track format, though ECC code is preferable to CRC code for the data integrity.

## CHAPTER 7 MODEL NUMBER

## 7.1 Definition of model number

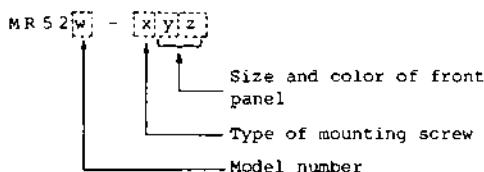


Table 7.1 w ..... Model number

w	Model number
1	Model 1 (12.75MB)
2	Model 2 (25.5MB)

Table 7.2 x ..... Type of mounting screw

x	Type of mounting screw
U	UNC-thread No.6-32UNC
M	Metric-thread M4 x 0.7

Table 7.3      y, z ..... Size and color of front panel

y	z	Dimension (mm)	Color	Note
0	0	42.0 x 148.0	Black	(1)
	8		Gray	
	9		White	
1	0	42.9 x 149.3	Black	(1)
	8		Gray	
	9		White	
4	0	42.0 x 148.0	Black	(2)
	8		Gray	
	9		White	
5	0	42.9 x 149.3	Black	(2)
	8		Gray	
	9		White	

Note (1): Write precompensation is not required.

(2): Write precompensation shall be required  
at cylinder greater than 256.

## 7.2 Standard Model Number

MR521-U00 , MR522-U00  
MR521-M40 , MR522-M40

If you need other models, please inquire us.



 **MITSUBISHI ELECTRIC CORPORATION**  
HEAD OFFICE: MITSUBISHI DENKI BLDG., MARUNOUCHI, TOKYO 100 TELEX: J24532 CABLE: MEICO TOKYO

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\* \* 20 Meg. Hard Disk Drive \*  
\* Seagate ST255 \*  
\* OEM Manual \*  
\*\*\*\*\*

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## ST225 OEM MANUAL

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October 22, 1985©

36005—001, Rev. F

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# INTRODUCTION

The Seagate ST225 disc drive provides OEMs and system integrators with over 20 megabytes of formatted capacity in a shock-resistant half-height package. The ST225 is designed for single-user desk-top systems, local storage in network or multi-user systems, or as an add-in upgrade for PCs. The low-power ST225 design is ideal for these applications in either rugged industrial or quiet office environments. The ST225 supports the industry-standard ST412 interface and has the same voltage requirements for ease of integration.

High reliability is assured through the use of LSI, a single printed circuit board, mini-monolithic heads and proven oxide media. Seagate's proprietary helical-band rotary-actuator features simplicity and ease of manufacture with excellent thermal stability. A dedicated head shipping zone assures data integrity during shipping and handling. The ST225 offers a low-cost, rugged and reliable disc drive with an MTBF of 20,000 hours.

Our manufacturing facilities have been designed and located exclusively for high volume production and testing of disc drives. Seagate's ongoing commitment to vertical integration assures availability of the latest technology at the same consistent quality and lowest possible cost. Seagate inspects every assembly at every stage of the production process. A proprietary test system continuously verifies our goals of volume production with rigorous quality control.

## ST213

Oct. 29, 1985

This manual may be used to install and configure Seagate's ST213. The ST213 is a half-height, single-disc, 10 Megabyte (formatted) Winchester. It employs the same efficient helical-band rotary-actuator as the ST225 and also supports the industry-standard ST412 interface.

Voltage requirements, interface connectors and mounting requirements are identical to the ST225. Please refer to page 40, Appendix number 3 for specifications.



# 1.0 SPECIFICATION SUMMARY

## PERFORMANCE SPECIFICATIONS

1.1

Capacity	Unformatted	Formatted
Per Drive:	25.62 MB	20.15 MB
Per Surface:	6.41 MB	5.04 MB
Per Track:	10,416 Bytes	8,192 Bytes
Per Sector:	NA	256 Bytes
Sectors per Track:	NA	32 Sectors
		17 Sectors

## ACCESS TIME DEFINITION AND TIMING

1.1.1

Access time is defined as the time from the leading edge of the last Step pulse received to SEEK COMPLETE (including carriage settling). The period between Step pulses must be between 5usec and 200usec.

Average access time is measured over a 205-track seek (one-third stroke). The calculation assumes the following:

1. Nominal temperature and power
2. The average is taken from an inward one-third stroke, plus an outward one-third stroke.

Track-to-Track:	20.0msec max.
Average:	65.0msec max. <sup>1</sup>
Maximum Seek:	150.0msec max. <sup>1</sup>

## FUNCTIONAL SPECIFICATIONS

1.2

Rotational Speed:	3,600 RPM $\pm$ 1%
Latency:	8.33msec nominal
Recording Density:	9,827 BPI (Cylinder 614)
Flux Density:	9,827 FCI (Cylinder 614)
Track Density:	588 TPI
Cylinders:	615
Tracks:	2,460
Read/Write Heads:	4
Discs:	2
Data Transfer Rate:	5.0 Megabits/second
Recording Scheme:	MFM

## PHYSICAL SPECIFICATIONS

1.3

Height:	1.63 inches max. (41.4mm)
Width:	5.75 $\frac{1}{2}$ inches (146.05 $\frac{1}{2}$ mm)
Depth:	8.00 inches max. (203.2mm)
Weight:	2.75 lbs (1.25Kg)

1. Buffered-Seek

## 1.4

## RELIABILITY SPECIFICATIONS

MTBF:	20,000 Power-on hours <sup>2</sup>
PM:	Not required
MTTR:	30 minutes
Service Life:	5 years

### 1.4.1

### READ ERROR RATES

Recoverable Read Errors: 1 per  $10^{10}$  bits read <sup>3</sup>

Nonrecoverable Read Errors: 1 per  $10^{12}$  bits read <sup>4</sup>

Seek Errors: 1 per  $10^6$  seeks

#### 1.4.1.1

#### BIT JITTER

Bit jitter reduction determines the relationship between the leading edge of READ DATA and the center of the data window.

The specified Read error rates are based on the following bit jitter specification. The data separator must provide at least -40 dB of bit jitter reduction at 2F with an offset error of less than 1.5nsec shift from the center of the data window.

### 1.4.2

### MEDIA DEFECTS

A media defect is a Read error when data, which has been correctly written, cannot be recovered within 16 retries.

A printout will be provided with each drive listing the location of any defect by head, cylinder, sector and byte. It will also specify the number of bytes from the Index pulse. <sup>5</sup>

There will be no more than eight (8) defects per surface for a maximum total of thirty-two (32) per drive. Cylinder Zero will be free of defects.

## 1.5

## ENVIRONMENTAL SPECIFICATIONS

### 1.5.1

### AMBIENT TEMPERATURE

Operating: 50°F to 113°F (10°C to 45°C)

Nonoperating: -40°F to 140°F (-40°C to 60°C)

### 1.5.2

### TEMPERATURE GRADIENT

Operating: 18°F/hr (10°C/hr) max.

Nonoperating: Below condensation

2. Typical usage at 25°C, at sea level. Calculated per *Mil. Spec. Handbook 217*.

3. Recoverable within 16 retries

4. Not recoverable within 16 retries

5. Based on a 32-sector, 256 byte/sector format

**RELATIVE HUMIDITY** 1.5.3

Operating: 8 to 80% noncondensing  
Maximum Wet Bulb: 78.8°F (26°C) noncondensing  
Nonoperating: 5 to 95% noncondensing

**ALTITUDE LIMITS** 1.5.4

Operating: - 1,000 ft to 10,000 ft  
Nonoperating: - 1,000 ft to 30,000 ft

**OPERATING SHOCK** 1.5.5

Maximum permitted shock without incurring physical damage or degradation in performance: 10 G's<sup>6,7</sup>

**OPERATING VIBRATION** 1.5.6

Maximum permitted vibration, at the following frequencies, without incurring physical damage or degradation in performance:<sup>7</sup>

Frequency	Vibration
5 - 22 Hz	.010" double amplitude
22 - 300 Hz	.25 G amplitude (peak)
300 - 22 Hz	.25 G amplitude (peak)
22 - 5 Hz	.010" double amplitude

**NONOPERATING SHOCK** 1.5.7

Maximum permitted shock without incurring physical damage or degradation in performance: 40 G's<sup>6,7,8</sup>

**NONOPERATING VIBRATION** 1.5.8

Maximum permitted vibration, at the following frequencies, without incurring physical damage or degradation in performance:<sup>7,8</sup>

Frequency	Vibration
5 - 22 Hz	.010" double amplitude
22 - 300 Hz	.50 G amplitude (peak)
300 - 22 Hz	.50 G amplitude (peak)
22 - 5 Hz	.010" double amplitude

**DC POWER REQUIREMENTS** 1.6

The ST225 is listed in accordance with UL 478 and CSA C22.2 (O-M1982), and meets all applicable sections of IEC 380 and VDE 0806/08.81, as tested by *TVU-Rheinland, North America*.

6. 11 msec half-sine wave shock pulse

7. Input levels at the drive mounting screws. Unit mounted in an approved orientation.  
See *Section 1.7*

8. Heads positioned in the shipping zone

Power may be applied or removed in any sequence without loss of data or damage to the drive.

**+ 12 Volts DC:**

Voltage Tolerance (including ripple):  $\pm 5\%$   
Maximum Current at Power-on: 2.2 Amp  
Typical Current: .9 Amp

**+ 5 Volts DC:**

Voltage Tolerance (inc. ripple):  $\pm 5\%$   
Typical Current: .8 Amp  
Power 14.8 typical\*

**1.6.1**

**INPUT NOISE RIPPLE**

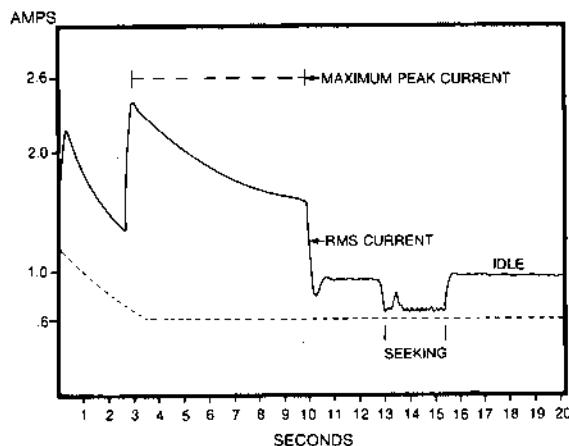
The maximum permitted ripple is 100mV (peak-to-peak) on either +12 Volts or +5 Volts measured on the host system power supply across the following equivalent resistive loads:

+ 12 Volts DC  $16\Omega$   
+ 5 Volts DC  $5\Omega$

**1.6.2**

**INPUT NOISE FREQUENCY**

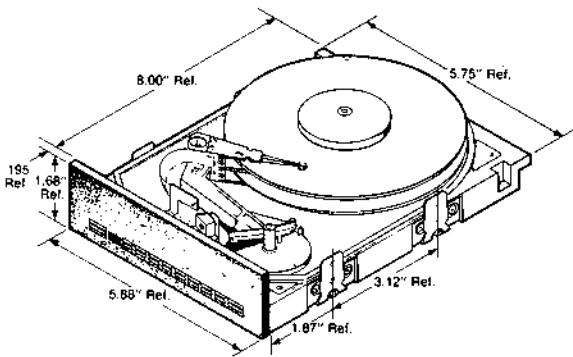
20MHz max. on both the +12 and +5 Volt lines



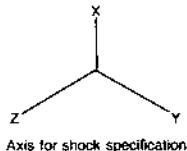
**FIGURE 1:**  
Typical RMS +12 Volt DC  
Start-Up Current Plot

9. Measured under the following standard operating conditions:  
25°C ambient temperature  
Sea level  
Nominal voltages applied  
Spindle rotating, drive not seeking

**FIGURE 2:**  
*Reference Dimensions*



Dimensions are in inches.



## MOUNTING REQUIREMENTS

1.7

The ST225 may be mounted in the following orientations:

Horizontal: Spindle motor down  
Sides: Left or right

The drive should not be tilted front to back, in any position, by more than  $\pm 5^\circ$ . Refer to Figures 2 and 3 for reference and mounting dimensions.

For optimum performance the drive should be formatted in the same orientation as it will be mounted in the host system.

### SHOCK MOUNTING RECOMMENDATION

1.7.1

It is recommended that any external shock mounts between the drive and the host frame be designed so that the composite system has a vertical resonant frequency of 25Hz or lower.

A minimum clearance of 0.050 inch should be allowed around the entire perimeter of the drive for cooling airflow and motion during mechanical shock or vibration.

## 1.7.2 HANDLING AND STATIC-DISCHARGE PRECAUTIONS

After unpacking and prior to system integration, the drive is exposed to potential handling and ESD hazard.

Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

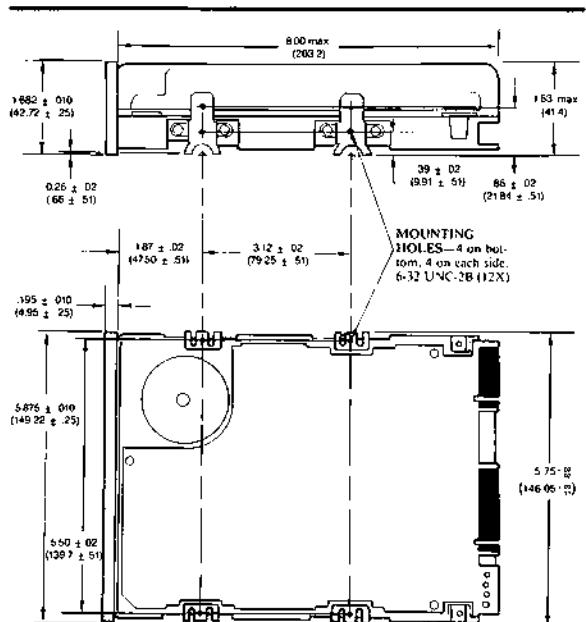
It is strongly recommended that the drive always rest on a padded surface, with the heads parked over the shipping zone, until the drive is mounted in the host system.

## 1.7.3

### SHIPPING ZONE

The ST225 employs a shipping zone, located from Cylinders 615 to 670, to preserve data integrity during shipping/transport. The Read/Write heads may be parked in the shipping zone by issuing a seek to any cylinder between 615-670. The drive may then be powered-down.

Upon power-up, the drive will recalibrate to Track  $\emptyset$ . If the heads are parked while power is still applied, any Step pulse will cause the unit to recalibrate to Track  $\emptyset$ .



Dimensions are in inches (mm).  
NOTE: Mounting screws must not extend more than .25 inch inside the drive.

FIGURE 3:  
Mounting Dimensions

## 2.0 ST225 HOST/DRIVE INTERFACE

This section details the physical specifications of the host/drive interface connectors. Connector dimensions and pin assignments follow under each section. Refer to *Figure 9* for an overall view of the drive and the interface connectors.

### CONTROL/STATUS SIGNALS PCB EDGE-CONNECTOR, J1

2.1

Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

Control and status signals between the host and the drive are transmitted through a 34-pin PCB edge-connector, J1. *Figure 4* indicates connector dimensions and *Table 1* lists the pin assignments. A host/drive interconnection is illustrated in *Figure 5*.

With the drive resting on a padded surface, oriented with the PC Board up and the edge-connectors toward you, J1 is to your left and J2 is on the right. Refer to *Figure 9* for position and other interface option connectors.

J1 pins are numbered 1 through 34 with the even pins located on the solder side of the PCB. All odd pins are ground. A key slot is provided between pins 4 and 6. Pin 2 is labeled. The recommended mating connector for J1 is AMP ribbon connector, part number 88373-3.

**FIGURE 4:**  
*J1 Connector  
Dimensions*

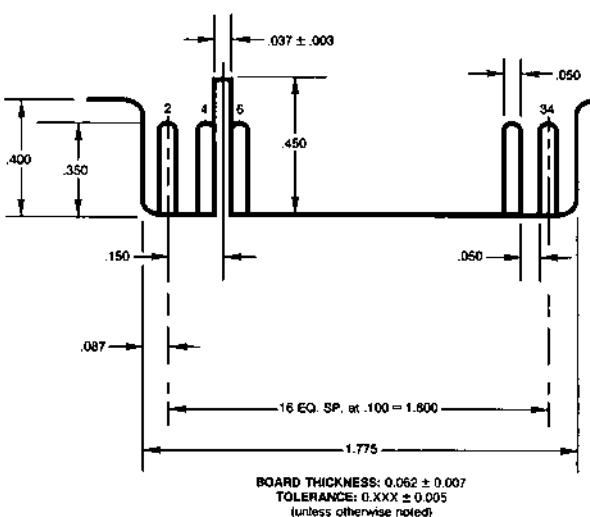
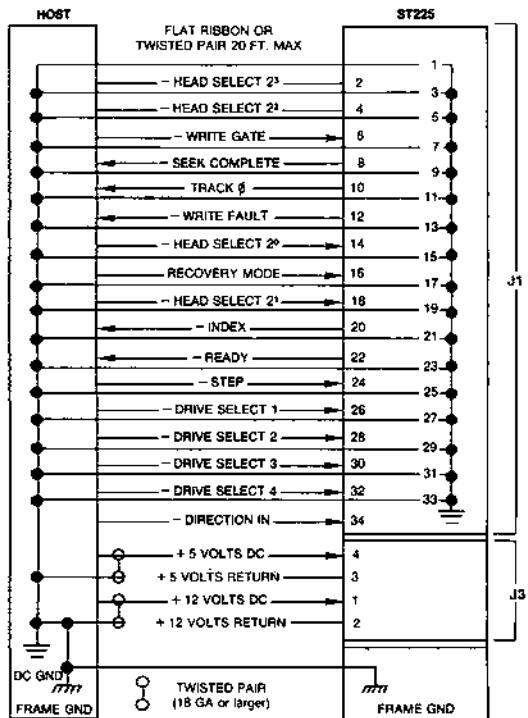


TABLE: 1  
J1 Host/Drive Pin  
Assignments

GROUND RTN PIN	SIGNAL PIN	SIGNAL NAME
1	2	-HEAD SELECT 2 <sup>3</sup>
3	4	-HEAD SELECT 2 <sup>1</sup>
5	6	-WRITE GATE
7	8†	-SEEK COMPLETE
9	10	-TRACK #
11	12†	-WRITE FAULT
13	14	-HEAD SELECT 2 <sup>0</sup>
15	16	-RECOVERY MODE
17	18	-HEAD SELECT 2 <sup>1</sup>
19	20†	-INDEX
21	22†	-READY
23	24	-STEP
25	26	-DRIVE SELECT 1
27	28	-DRIVE SELECT 2
29	30	-DRIVE SELECT 3
31	32	-DRIVE SELECT 4
33	34	-DIRECTION IN

†STATUS ENABLED WITH DRIVE SELECT

FIGURE 5:  
Control/Status Signals



## DATA SIGNALS PCB EDGE-CONNECTOR, J2

2.2

Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

Read/Write data signals are received and transmitted over a 20-pin PCB edge-connector, J2. Figure 6 below indicates connector dimensions and Table 2 lists the pin assignments. A host/drive interconnection is illustrated in Figure 7.

With the drive resting on a padded surface, oriented with the PC Board up and the edge-connectors toward you, J2 is to your right and J1 is on the left. Refer below to Figure 9.

J2 pins are numbered 1 through 20 with the even pins located on the solder side of the PCB. A key slot is provided between pins 4 and 6. Pin 2 is labeled. The recommended mating connector for J2 is AMP ribbon connector, part number 88373-6.

FIGURE 6:  
J2 Connector  
Dimensions

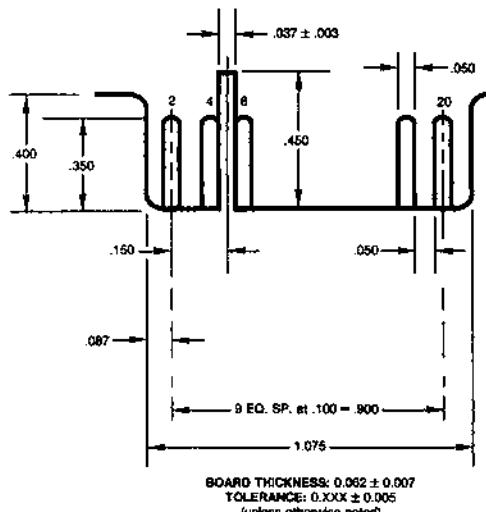
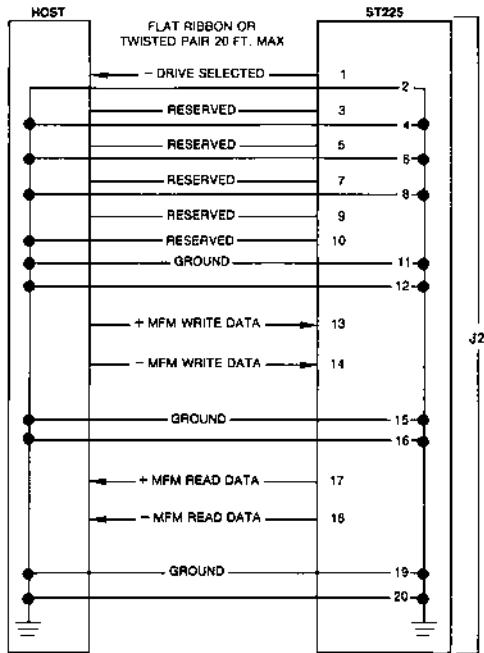


TABLE: 2  
J2 Host/Drive Pin  
Assignments

GROUND RTN PIN	SIGNAL PIN	SIGNAL NAME
2	1	-DRIVE SELECTED
4	3	RESERVED
5	5	RESERVED
8	7	RESERVED
10	9	RESERVED
12	11	GROUND
16	13	+ MFM WRITE DATA
	14	- MFM WRITE DATA
	15	GROUND
	17	+ MFM READ DATA
	18	- MFM READ DATA
20	19	GROUND

FIGURE 7:  
Data Signals



## DC POWER CONNECTOR, J3

2.3

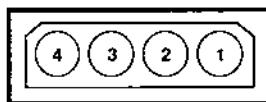
Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

DC Power is transmitted from the host to the drive via the power connector J3. J3 is a 4-pin AMP "Mate-N-Lock" connector, AMP part number 350211-1. J3 is directly to the left of J1 and mounted on the component side of the PCB. The recommended mating connector is AMP part number 1-480424-0.

Applications using cable lengths less than five feet may use #18AWG wire and AMP 61314-4 strip pins.

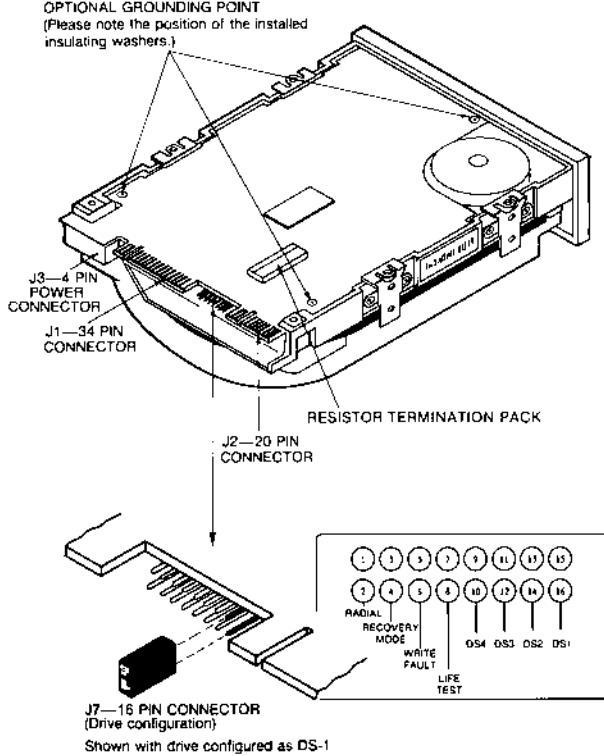
For applications requiring cable lengths greater than five feet, #14AWG wire is recommended using AMP 61117-4 strip pins.

*FIGURE 8:  
J3 Connector*



PIN	POWER
1	+ 12 VOLTS
2	+ 12 VOLTS RETURN
3	+ 5 VOLTS RETURN
4	+ 5 VOLTS

**FIGURE 9:**  
*Host/Drive Interface and  
Drive Configuration*



## 3.0 DRIVE CONFIGURATION

The ST225 may be configured to specific host system requirements. Sections 3.1 through 3.6 detail the options.

### DRIVE CONFIGURATION SHUNT, J7

3.1

J7 is a 16-pin right angle shunt located midway between J1 and J2. Use the provided shorting blocks to enable the DRIVE SELECT lines and the desired options. *Figure 9* illustrates J7 and indicates Pin 1.

### DRIVE SELECT CONFIGURATION

3.2

The DRIVE SELECT line enables the controller to select and address the drive. Control cable interface options use either a Daisy-Chain or Radial configuration.

Pins 15-16 shorted enables DRIVE SELECT 1

Pins 13-14 shorted enables DRIVE SELECT 2

Pins 11-12 shorted enables DRIVE SELECT 3

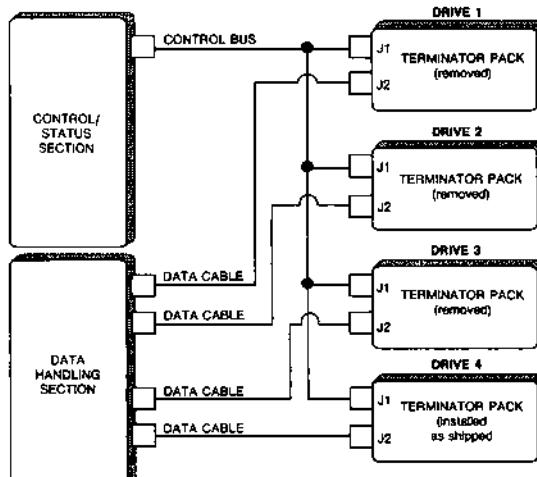
Pins 9-10 shorted enables DRIVE SELECT 4

#### DAISY-CHAIN

3.2.1

Each drive in the chain must be configured as either DRIVE 1,2,3 or 4, so that only one DRIVE SELECT line activates a device. The last drive in the chain must have a  $220/330\Omega$  resistor termination pack installed on the PCB. Refer to *Figure 9* above for resistor pack location.

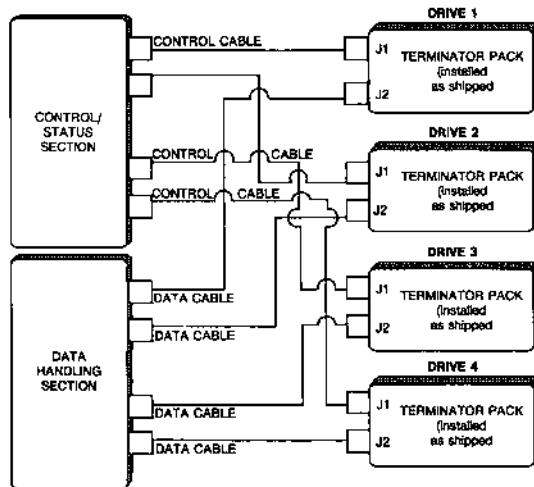
FIGURE 10:  
Daisy-Chain  
Configuration



### 3.3

### RADIAL

The Radial option is enabled by shorting pins 1 and 2 at the J7 shunt. Drives configured to this option are always selected and respond to all control signals issued on the attached control cable. The 220/330Ω resistor termination pack must remain installed on each radially-connected drive. *Figure 11* illustrates a host/drive Radial interconnection.



**FIGURE 11:**  
*Radial Configuration*

### 3.4

### WRITE FAULT

The WRITE FAULT signal may be internally latched. This latch may be cleared when DRIVE SELECT goes false (if pins 5 and 6 are shorted at J7). The standard configuration, with the shorting block removed, causes WRITE FAULT to go false when WRITE GATE goes false. Refer to Section 5.7 for a detailed discussion of WRITE FAULT.

### 3.5

### LIFE TEST

This function is used during the manufacturing process and is **not recommended for field use**. When pins 7 and 8 are shorted, the stepper motor will continuously seek between Track 0 and the maximum cylinder. When in this mode the drive will ignore control signals sent via the interface.

## RECOVERY MODE

3.6

The ST225 may be configured to the RECOVERY MODE option by shorting pins 3 and 4 at J7. This option enables the Read/Write heads to microstep. This repositioning option may be used after the controller has completed its retry options on a read error.

RECOVERY MODE is initiated by the controller asserting the RECOVERY MODE line low (true) at the interface. This changes the STEP line to a microstep function after 100nsec. A Step pulse will now cause SEEK COMPLETE to go false 100nsec after the drive receives the pulse. The drive then microsteps off-track using the optimum algorithm, allowing 8msec for the heads to settle, and then takes the SEEK COMPLETE line true.

The controller may then attempt to read data. If data is not read correctly, the controller may issue an additional Step pulse. Up to eight separate microstep algorithms may be accessed before the sequence is repeated.

When data is read correctly, the controller exits RECOVERY MODE by taking the RECOVERY MODE line false at the interface. The drive then returns the heads to the nominal position by taking SEEK COMPLETE false, waiting 8msec for the heads to settle and reasserting SEEK COMPLETE.

Note: All writing is inhibited while the RECOVERY MODE signal is true.

The control signals are of two types: those to be multiplexed in a multiple drive system and those intended to do the multiplexing.

The signals to be multiplexed are WRITE GATE, HEAD SELECT 2<sup>0</sup>, HEAD SELECT 2<sup>1</sup>, HEAD SELECT 2<sup>2</sup>, HEAD SELECT 2<sup>3</sup>, DIRECTION IN, RECOVERY MODE and STEP. These lines are terminated with a removable 220/330Ω resistor pair.

The multiplexing signals are DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3, and DRIVE SELECT 4. These lines are terminated in a single fixed 220/330Ω resistor pair.

Control signals are transmitted across the driver/receiver combination illustrated below in *Figure 12*. Control input signals are activated in accordance with the following specifications:

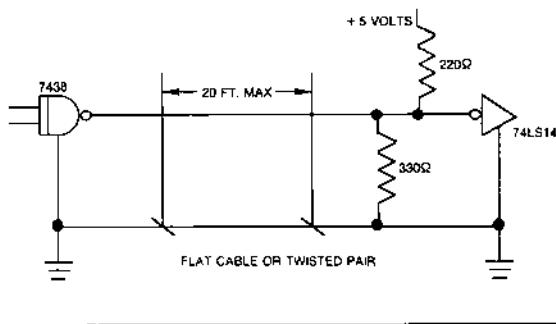
True: 0.0 Volts DC to 0.4 Volts DC at  $I = -48\text{mA}$  max.

False: 2.5 Volts DC to 5.25 Volts DC at  $I = +250\mu\text{A}$  (open collector)

Termination: A 220/330Ω resistor pack

## 4.0 CONTROL INPUT SIGNALS

**FIGURE 12:**  
*Control Signals  
Driver/Receiver  
Combination*



### 4.1

#### HEAD SELECT 2<sup>0</sup>, 2<sup>1</sup>, 2<sup>2</sup>, 2<sup>3</sup>

These signals allow the selection of each Read/Write head in a binary code sequence. The heads are numbered 0 through 3. HEAD SELECT 2<sup>0</sup> is the least significant line. When all HEAD SELECT lines are high on the interface, head 0 is selected. Refer below to *Figure 13* below for HEAD SELECT timing.

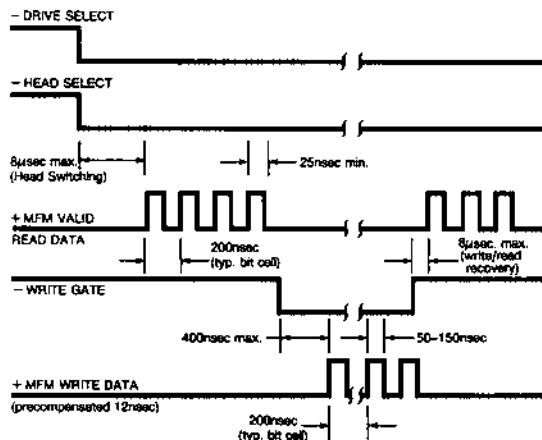
Note that both HEAD SELECT 2<sup>1</sup> and 2<sup>3</sup> are invalid signals for the ST225. These lines are present on the interface, but are terminated. The drive will not respond to these input signals.

### 4.2

#### WRITE GATE

The active state of this signal, or low level, enables data to be written to the disc and inhibits carriage motion if WRITE FAULT is active on the receipt of the first Step pulse. When inactive, or high, this signal enables data to be transferred from the drive and enables Step pulses to move the heads.

**FIGURE 13:**  
Read/Write Timing



NOTE: Heads may not be switched while WRITE GATE is active.

## STEP

4.3

The STEP signal is a 500nsec (minimum width) pulse that initiates Read/Write head motion. The number of pulses issued determines distance traveled. Pulses are edge-detected on the leading edge of the pulse.

The rate of Step pulses determines the access method. If the period between pulses is from 5usec to 200μsec, the access method will be Buffered-Seek. Slow-Step is employed if the period between pulses is greater than or equal to 3msec.

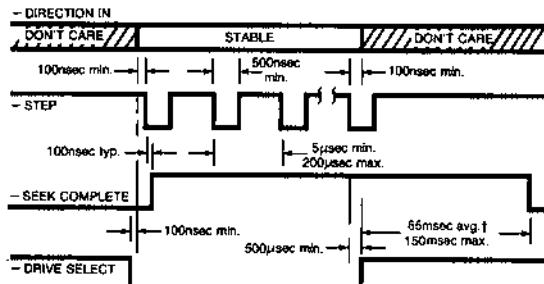
DIRECTION IN must be stable 100nsec before the leading edge of the first step pulse and remain stable for 100nsec after the last pulse in a string of Step pulses. Step pulses issued between 200μsec and 3msec may be lost.

If excessive Step pulses are issued which would cause a seek inward beyond Cylinder 670 or outward beyond Cylinder Zero, the drive will enter the Auto-Truncation mode. Refer to Section 4.3.3.

#### 4.3.1

#### BUFFERED SEEK

To minimize access time, pulses may be issued at an accelerated rate and buffered in a counter. Initiation of a seek starts immediately after the first pulse is received. Head motion occurs during pulse accumulation, and the seek is completed following receipt of all pulses.



\*Time is from start of head actuation to SEEK COMPLETE.

FIGURE 14:  
Buffered-Seek Timing

#### 4.3.2

#### SLOW-STEP (Track-to-Track)

In single-track Slow-Step mode, the Read/Write heads move at the rate of the incoming Step pulses. The minimum pulse period is 3μsec. The stepper motor is settled and SEEK COMPLETE is issued 20msec max. after the leading edge of the last pulse.

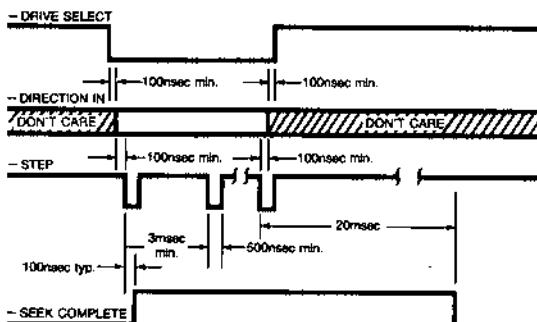


FIGURE 15:  
Slow-Step Timing

## AUTO-TRUNCATION

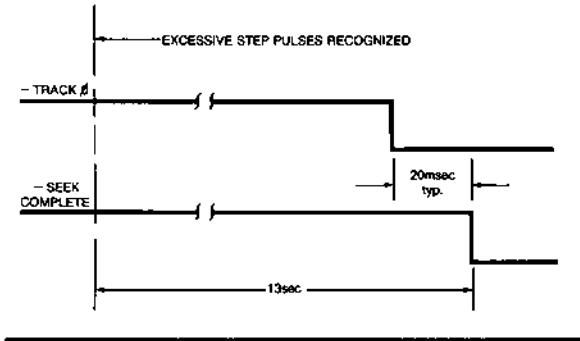
4.3.3

The drive will enter the Auto-Truncation mode if the controller issues an excessive number of Step pulses, which would place the Read/Write heads outward beyond Track 0 or inward beyond Cylinder 670.

With Auto-Truncation active, the drive will ignore additional pulses, take control of the stepper motor and recalibrate the heads to Track 0. Refer below to *Figure 16*.

**CAUTION:** If the controller is still issuing Slow-Step pulses after the ST225 issues SEEK COMPLETE from Auto-Truncation mode, the drive will either reenter Auto-Truncation mode with DIRECTION IN false, or step the remaining cylinders with DIRECTION IN true.

**FIGURE 16:**  
Auto-Truncation Timing



## DIRECTION IN

4.4

DIRECTION IN defines the direction the Read/Write heads will move when the STEP line is pulsed. With DIRECTION IN true, each pulse causes the heads to move one cylinder inward toward the spindle.

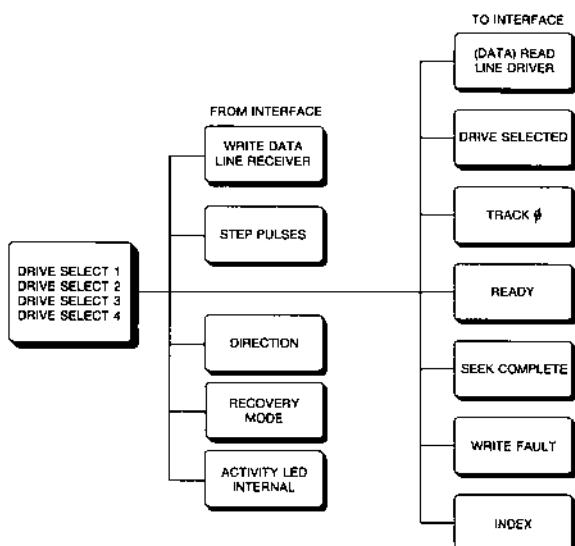
When DIRECTION IN is false, each pulse causes the heads to move one cylinder outward toward Track 0.

#### 4.5

#### DRIVE SELECT

The DRIVE SELECT line is activated by the controller to select and address the drive.

FIGURE 17:  
Drive Select

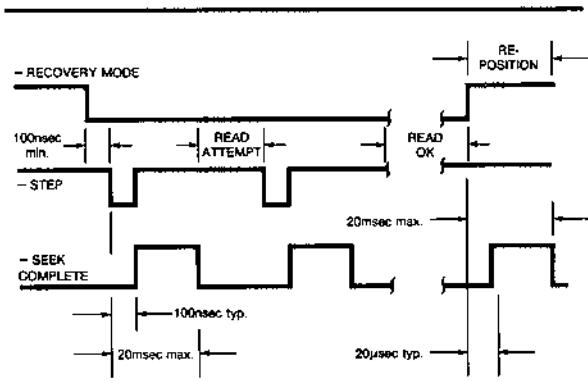


## RECOVERY MODE

4.6

The RECOVERY MODE line provides a micropositioning option that may be used after the controller has completed its retry options on a Read error. *Section 3.6* above details this option.

FIGURE 18:  
Recovery Mode Timing



The control output signals are gated to the interface when selected. The control output signals are DRIVE SELECTED, INDEX, TRACK  $\emptyset$ , READY, SEEK COMPLETE and WRITE FAULT.

## 5.1

### DRIVE SELECTED

DRIVE SELECTED is a status signal transmitted over J2, which informs the host system of the selection status of the drive. The signal is driven by a TTL open collector, as illustrated in *Figure 12*. The signal goes low (true) on the interface only when the device is configured as described in *Section 3.2*, and the appropriate DRIVE SELECT line is activated by the host system.

## 5.2

### INDEX

This signal is provided by the drive once each revolution (16.67msec nominal) to indicate the beginning of a track. Normally this signal is at a high level and makes the transition to low to indicate INDEX. Only the transition from high to low, or the leading edge, is valid.

## 5.3

### TRACK $\emptyset$

This signal is active (true) only when the Read/Write heads are positioned at Cylinder Zero.

Track  $\emptyset$  is the only cylinder that provides interface recognition. The drive is designed to recalibrate to Track  $\emptyset$  during power-on and Auto-Truncation operations.

Track  $\emptyset$  may also be accessed via conventional Buffered-Seek and Slow-Step modes. After Track  $\emptyset$  is true, no action may be taken by the controller until SEEK COMPLETE is also true.

## 5.4

### INDEX AND TRACK $\emptyset$ SENSING

The ST225 does not use either an Index or Track  $\emptyset$  sensor. The drive accesses the Index tracks on power-up for reference information. When the drive has reached proper speed, the stepper motor IC is set to phase minus A and minus B. The MPU then seeks in multiples of eight tracks until it finds Track 617 and Track minus 1. These are the reference tracks that are written on all four surfaces.

The MPU uses these tracks to set its internal track counter. The drive then steps in one track from track minus 1 and sets the Track  $\emptyset$  signal on the interface. The MPU will maintain the track count until a recalibration or Auto-Truncation triggers the set-up routine.

The Index tracks, written on Cylinder 617 and Cylinder minus 1, are written with a unique data pattern which generates the Index/Track  $\emptyset$  interface signals. The drive has a simple data discriminator which the MPU samples during initialization. By discriminating the unique data pattern on the Index/Track  $\emptyset$  reference tracks, the MPU can set a divide by two circuit. This circuit allows reliable Index from the spindle motor Hall signal.

## 5.0

# CONTROL OUTPUT SIGNALS

## READY

5.5

This signal, when true together with SEEK COMPLETE, indicates that the drive is ready to Read, Write or Step and that all control input signals are valid. When this line is high, all reading, writing and stepping are inhibited. The maximum time after power-on for READY to be true is 24 seconds.<sup>10</sup>

During the power-up sequence, READY remains false until:

1. The recalibration to Track 0 is complete
2. Spindle speed is stable within  $\pm 1\%$  of nominal
3. Drive initialization routines are complete
4. DC voltages are within tolerance

## SEEK COMPLETE

5.6

This signal goes to a low level (true) on the interface when the Read/Write heads have settled on the final track at the end of a seek. Seeking, reading or writing should not be attempted when SEEK COMPLETE is false. SEEK COMPLETE will go false in the following cases:

1. When a recalibration sequence is initiated (by drive logic) at power-on
2. 100nsec typical after the leading edge of a Step pulse
3. If either +5 Volts or +12 Volts are detected as unsafe
4. At the beginning and end of a RECOVERY MODE operation

## WRITE FAULT

5.7

This signal notifies the host system that a condition exists which, if not corrected, may cause an incorrect Write operation.

### WRITE FAULT SIGNAL GENERATION

5.7.1

With DRIVE SELECT active, and any one of the following conditions true, the WRITE FAULT signal will be issued to the interface and Write Current will be inhibited.

1. Write Gate true with no Write Current to the heads
2. Write Current to the heads with no Write Gate
3. An attempt to Write with RECOVERY MODE active
4. SEEK COMPLETE false
5. A Step pulse is received

WRITE FAULT remains true until the condition which triggered the fault is corrected and the reset is completed.

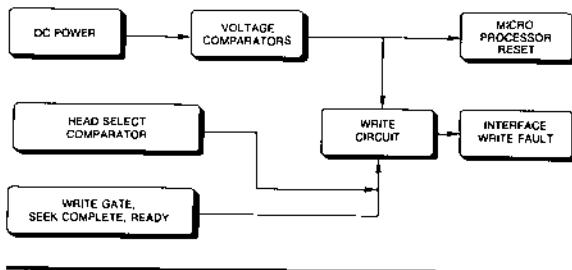
### WRITE CURRENT INTERRUPTION

5.7.1.1

Any one of the following conditions will cause Write Current to be inhibited when Write Gate is true:

1. Multiple heads selected
2. No head selected
3. READY false

<sup>10</sup> The 24 second maximum time interval is calculated from the point that the host system power supply maintains the specified  $\pm 5\%$  voltage tolerances.



**FIGURE 19:**  
*Fault Detection Flow*

### 5.8.1

#### DC-UNSAFE SIGNAL

A DC-Unsafe condition will cause a microprocessor reset. This will prohibit writing, but will not directly cause a WRITE FAULT. If Write Gate remains true, while the MPU resets from a DC-Unsafe condition, a WRITE FAULT will be triggered through the loss of READY and SEEK COMPLETE.

##### 5.8.1.1

#### VOLTAGE COMPARATOR

The Read/Write LSI (IC 5H) continually monitors the +5 and +12 VDC lines for low voltage conditions. If +5 Volts is > 15% low or +12 Volts is > 20% low, Write Current will be disabled and the MPU will be reset.

### 5.8.2

#### HEAD SELECT COMPARATORS

During normal operations a single head will be selected, and the Voltage Center Tap (VCT) will be high (IC 5H, pin-27).

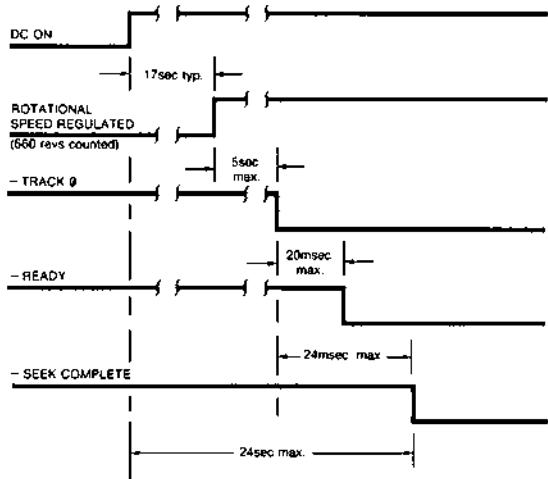
If multiple heads are selected, the voltage will increase at Voltage Head Safe (VHS, IC 5H, pin-26) forcing its output low. Less than one head selected will decrease the voltage at pin-4, forcing its output low. Write Current will then be disabled and the MPU will reset.

## 6.0 POWER-ON SEQUENCE

The application of DC power initiates a sequence that starts the spindle motor, regulates its speed, steps the Read/Write heads to Track 0 and issues READY and SEEK COMPLETE sequentially to terminate the sequence.

READY and SEEK COMPLETE are issued to the interface when the drive is available to accept commands. Upon power-up the drive is available to accept commands 24 seconds max. after the power supply voltages maintain the specified  $\pm 5\%$  voltage tolerances.

FIGURE 20:  
Power-On  
Sequence Timing



Two pairs of balanced signals are employed for data transfer: MFM WRITE DATA and MFM READ DATA. Data transfer lines between the host system and the drive are differential in nature and may not be multiplexed. Refer above to *Table 2* for data transfer pin assignments and *Figure 7* for a host/drive interconnection example.

## 7.0 DATA TRANSFER LINES

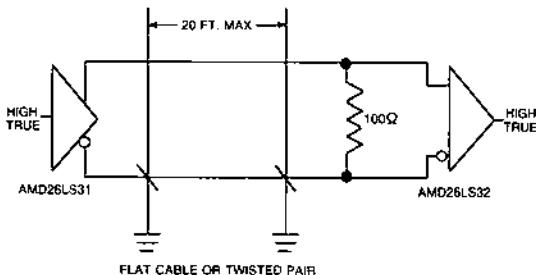


FIGURE 21:  
Data Signal  
Driver/Receiver  
Combination

### 7.1

### WRITE OPERATION

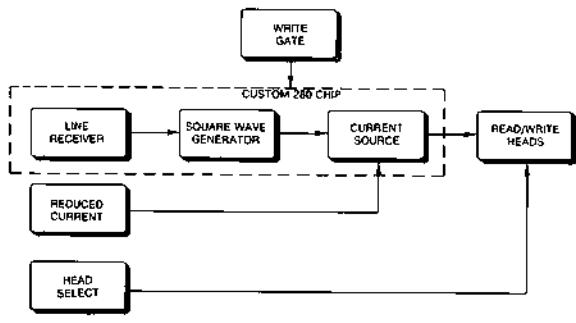


FIGURE 22:  
Write Operation

In order to Write, the following conditions must be true:

- |                         |                           |
|-------------------------|---------------------------|
| 1. DRIVE SELECT active  | 4. Write Gate active      |
| 2. READY active         | 5. WRITE FAULT inactive   |
| 3. SEEK COMPLETE active | 6. RECOVERY MODE inactive |

**MFM WRITE DATA**

7.1.1

WRITE DATA is transmitted by a differential pair which defines the transitions to be written on the disc. The + MFM WRITE DATA line going more positive than the - MFM WRITE DATA line is the active transition. This signal must be driven to an inactive state when in the Read mode.

**WRITE GATE**

7.1.2

A Write sequence is initiated when Write Gate is activated, which causes the Read/Write LSI to apply + 12 Volts to the center tap of the selected lead; concurrently data is sent to the line receiver.

**LINE RECEIVER**

7.1.3

Differential Write data, which is precompensated MFM, is received from the controller and changed to single line. It is then fed into the pulse generator, which changes pulse data to square wave data.

Pin-5, at IC 5H, will be activated if plus data is to be written. Pin-9 will be activated for minus data.

**PRECOMPENSATION**

7.1.4

Precompensation is recommended on Tracks 300 through 614. The optimum amount of precompensation is 12nsec for both early and late bits. *Table 3* below indicates the bit patterns and the direction to be compensated. An X denotes a "don't care state."

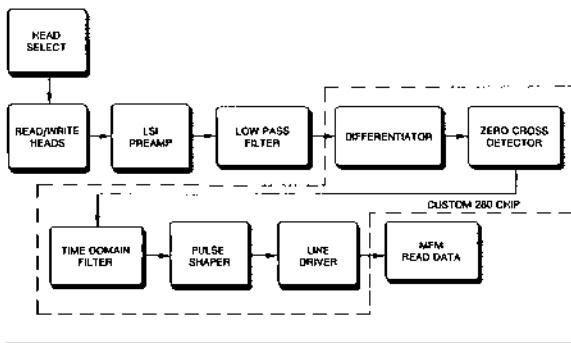
As the Read/Write heads travel inward, the track circumference of course decreases, and the data bits are necessarily written closer together. The Write Current is therefore reduced to preclude any pulse crowding.

The ST225 does not require the host to specify a cylinder(s) to begin applying reduced Write Current. This function is managed internally by the microprocessor.

**TABLE 3:**  
*Precompensation Pattern*

PREVIOUS	SENDING	NEXT	TIMING
X	0	1	WRITE DATA LATE
X	1	1	WRITE DATA EARLY
1	0	0	WRITE CLOCK LATE
0	0	0	WRITE CLOCK EARLY

ALL OTHER PATTERNS NOMINAL



**FIGURE 23:**  
Read Operation

#### 7.2.1

#### MFM READ DATA

The data recovered by reading a track is transmitted to the host system via a differential pair of MFM READ DATA lines. The transition of the + MFM READ DATA line going more positive than the - MFM READ DATA line, represents a flux reversal on the track of the selected head.

#### 7.2.2

#### HEAD SELECT

The binary decoder (IC 4H) selects the desired head based on the status of the Head Select lines. If the DC voltages are too low, possibly causing an inaccurate Read operation, the decoder (pin-12) will select a nonexistent head. By referencing 0 to + 5 Volts actual ground appears as -5 Volts, which eliminates the necessity of a negative power source normally required by the LSI preamp.

#### 7.2.3

#### LSI PREAMP

With the Head Center Tap (HCT) active, data from the selected head will flow into the preamp (9E), which amplifies the Read signal and also acts as a high-pass filter.

The HCT voltages are monitored and controlled by the custom Read/Write LSI (5H). This chip monitors the Write Gate line and sets the appropriate level on its Voltage Center Tap (VCT) for Read or Write mode.

#### 7.2.4

#### LOW-PASS FILTER

This filter network attenuates high frequency noise, which is outside the normal data signal range.

#### 7.2.5

#### PHASE SHIFTER

Amplified data enters the circuit and is shifted 90° so peak data, which was detected over a fairly broad range, is now moved to a highly sloped accurately detectable position at the zero crossing point.

**ZERO-CROSS DETECTOR**

7.2.6

This element detects bit positions as the slope of the Read Data signals crosses the zero threshold. At this point analog data are changed to digital.

**TIME DOMAIN FILTER**

7.2.7

When a high resolution head reads a low frequency data pattern, there is a tendency for the head signal to decay between bits. If the signal decays below the zero cross threshold, a spurious data bit will be generated. Such false bits are ignored by delaying the clocking bit past the potential point of highest drop.

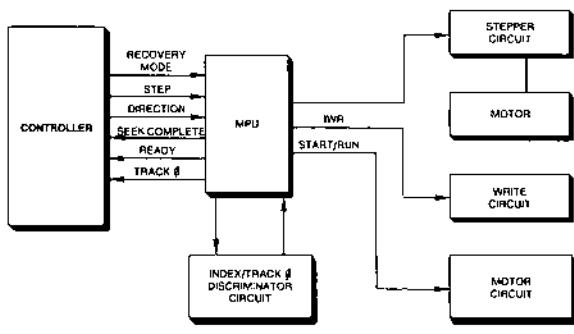
**LINE DRIVER**

7.2.8

This element changes raw digital data to a differential data, providing immunity to common mode noise during transmission.

The microprocessor monitors and controls the internal drive functions and the host interface lines. The MPU has only three active modes: Initializing, Waiting, or Seeking.

## 8.0 THEORY OF OPERATIONS



**FIGURE 24:**  
*Microprocessor  
Operation*

## 8.1.1

## MPU INITIALIZING

At power-on, the MPU initializes the stepper circuit to phase minus A and minus B, and resets all interface lines under its control.

As the drive spins-up, the MPU switches from bipolar to unipolar after approximately 40 revolutions. The processor will measure the period of the index signal to assure that the drive is up-to-speed before the re-calibration routine is initiated.

The MPU sets phase minus A and minus B on the stepper chip (IC 8D) and then executes the Seek and Discriminator routines, which recalibrates the Read/Write heads to Track 0, divides Index, and gives READY and SEEK COMPLETE. The drive is available to accept commands 24 seconds max. after power-up.

## 8.1.2

## MPU-IDLE

When in the idle mode, the MPU loops, waiting for Step pulses. The custom Read/Write LSI chip monitors the power inputs and, on transients, resets the MPU which will reinitialize the drive.

## SEEKING

8.1.3

Upon receiving a Step pulse, the MPU pauses for 250 $\mu$ sec to allow for additional pulses before executing the seek operation. Every incoming pulse resets the 250 $\mu$ sec timer. The seek will not begin until the last pulse is received.

When seeking, the MPU counts the number of tracks to be covered, and employs the optimum step algorithm to reach the target track.

While seeking, the MPU controls the direction and mode of the custom stepper IC. Pulses are sent to the stepper chip, which does the actual phase commutations. Acceleration/deceleration are determined by the varied frequency of the pulses and the use of the Motor IC Direction line. This IC provides both a current source and sink to motor windings.

With READY and SEEK COMPLETE true, the MPU returns to the Idle mode.

## SPINDLE MOTOR CONTROL

8.2

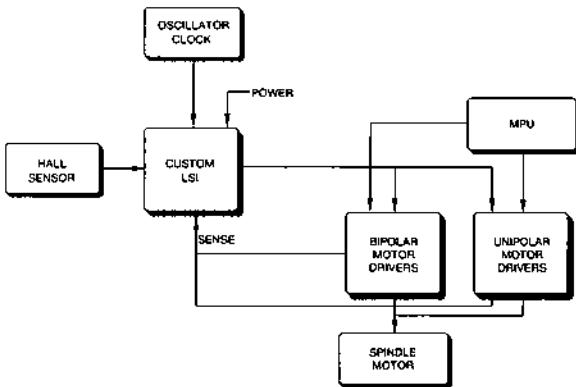


FIGURE 25:  
Spindle Motor Control

To insure sufficient starting power, the spindle motor circuit is run with a set of bipolar motor drivers. Once the spindle motor has started running, the MPU switches the motor circuit from bipolar to unipolar drivers; which significantly lowers the required running current.

The primary functions, listed below, are incorporated within the custom spindle motor IC (IC 4B).

1. Monitors the Hall signal from the spindle motor and uses the Hall transitions to commutate the motor phases. It regulates the motor speed by measuring the Hall period and comparing it to the oscillator clock period.
2. Employs a sense line to regulate the start current and execute a current limit shut-off.
3. Monitors the power supply for output driver shut-off. When the power is off, the output drivers become self-biased on, which brakes the motor using back-EMF.
4. Locked-Rotor Protection: IC 4B monitors the time from the first Hall transition. If the motor does not spin-up, the drivers will be disabled to avoid overheating the circuit. This Hall signal is generated by a transducer located in the motor hub. Two complete square waves are generated each complete revolution.

## 9.0 FIELD SERVICE

The ST225 does not require preventative maintenance. The PC Board may be exchanged in the field. Refer below to *Section 9.1* for this procedure.

### PC BOARD REMOVAL

9.1

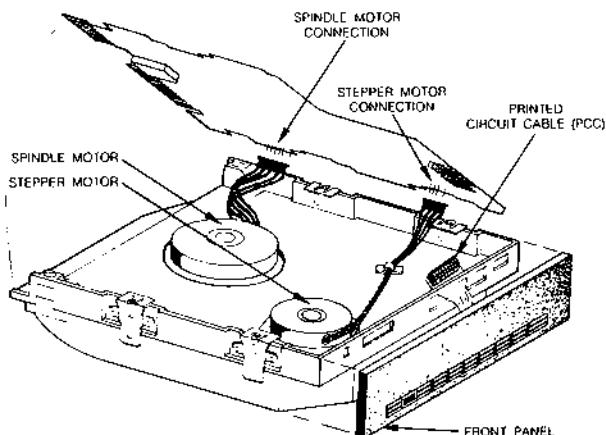
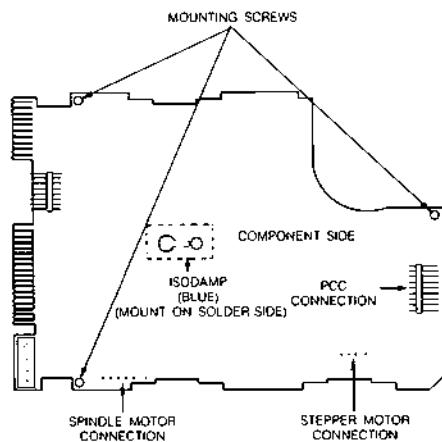


FIGURE 26:  
PC Board Removal



**It is mandatory that approved ESD precautions be observed during this procedure. This includes anti-static wrist-straps.**

Note: Earlier revisions of this PCB, Seagate part number 20301, required the PROM (7D) to be transferred to the replacement PCB. This is no longer required and the replacement board is downward compatible for all versions.

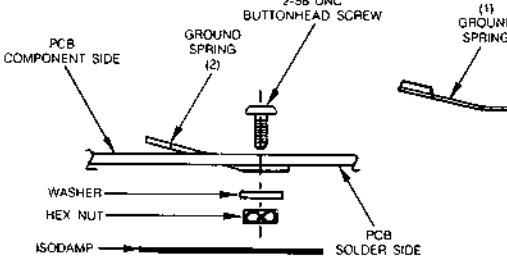
**Parts Required:** PC Board 20301-004

**Tools Required:** Torque driver, T-10 and T-5 Torx bits

1. Secure a padded anti-static work surface.
2. Remove the two front panel screws (or if installed, the printed circuit cable shield.)
3. Orient the drive with the PCB up.
4. Remove and retain the three PCB mounting screws. There may be a clear insulating washer installed at one or more of the mounting points. Be sure to replace at the same point(s) during reassembly.
5. Locate and carefully free the Printed Circuit Cable. Do not crease the cable.
6. Locate and carefully free the spindle motor and stepper motor connections.
7. Lift out the PCB.
8. Your replacement PCB will be shipped to you with a kit containing two ground springs.
  - a. If the spindle motor has a steel ball in the center of its hub, mount the spring with the graphite button (1).
  - b. If the spindle motor has a short post at the center of the hub, mount the bare copper spring (2).
9. Verify that the Ground Spring assembly is aligned and will make positive contact with the spindle hub. Note that the washer and hex nut both mount on the solder side of the PCB. Refer to *Figure 27*.
10. Tighten the Ground Spring mounting screw to 2.5 inch/lbs. Transfer the blue Isodamp pad to the replacement board.
11. Reconnect the Stepper and Spindle motor connections.
12. Reconnect the Printed Circuit cable.
13. Torque the PCB mounting screws to 9 inch/lbs. Do not forget to replace the clear insulating washer(s), if installed.

---

**FIGURE 27:**  
**Ground Spring**  
**Assembly**



## **Appendix 2: Standard Spares List**

Front Panel, half-height:	58838-001
Front Panel, full-height:	50449-001
Shunt:	10027-001
Main Control PC Board:	20301-004

# Appendix 3: ST213

## Specifications

### UNFORMATTED CAPACITY

Per Drive: 12.81 Megabytes  
Per Cylinder: 20,832 Bytes  
Per Track: 10,416 Bytes

### FORMATTED CAPACITY

Per Drive: 10.71 Megabytes  
Per Cylinder: 17,408 Bytes  
Per Track: 8,704 Bytes  
Per Sector: 512 Bytes  
Sectors per Track: 17

### PHYSICAL ORGANIZATION

Tracks: 1,230  
Cylinders: 615  
Read/Write Heads: 2  
Discs: 1

### FUNCTIONAL SPECIFICATIONS

Rotational Speed: 3,600 RPM ± 1%  
Recording Scheme: MFM  
Recording Density: 9,627 BPI  
Flux Density: 9,627 PCI  
Track Density: 568 TPI  
Interface: ST412  
Data Transfer Rate: 5.0 Megabits/sec

### ACCESS TIME (incl. settling)

Track-to-Track: 20 msec  
Average: 65 msec  
Full Stroke: 150 msec  
Latency: 8.33 msec nominal

### ERROR RATES

Recoverable Read Errors: 1 per  $10^{10}$  bits read \*  
Nonrecoverable Read Errors: 1 per  $10^{10}$  bits read \*\*  
Seek Errors: 1 per  $10^4$  seeks  
\* Recoverable within 15 retries  
\*\* Not recoverable within 15 retries

### RELIABILITY SPECIFICATIONS

MTBF: 20,000 Power-on Hours  
PM: Not Required  
MTTR: 30 Minutes  
Service Life: 5 Years

### OPERATIONAL ENVIRONMENT

Ambient Temperature: 10°C to 45°C (50°F to 113°F)  
Temperature Gradient: 10°C/hr. (18°F/hr.)  
Relative Humidity: 8 to 80% noncondensing  
Maximum Wet Bulb: 26°C (78.8°F) noncondensing

### DC POWER REQUIREMENTS

+12VDC ± 5% .9 Amps typ.  
+5VDC ± 5% 2.2 Amps max. at power-up  
Power: .8 Amps typ.  
14.6 Watts typ.

### PHYSICAL SPECIFICATIONS

Height: 1.63 inches max. (41.4mm)  
Width: 5.75  $\frac{3}{16}$  inches (146.05  $\frac{1}{16}$  mm)  
Depth: 8.00 inches max. (203.2mm)  
Weight: 2.73 lbs. (1.25 kg)

## Tandy 3000 Power Supply

### I. AAI3260 Power Supply Theory of Operation

1. Introduction
2. General Theory
3. Specific Operation
  - A. EMI Filter
  - B. Surge Protection
  - C. Capacitive Input Filter and Voltage Select
  - D. Power Conversion
  - E. Control Circuit
  - F. Turn-on/turn-off Circuits
  - G. Protection Circuit
  - H. Fan Control

### II. Jumper Settings

### III. Schematics

### IV. Subassembly and Parts List

### V. PCB Layouts

### VI. OEM Repair Manual



## AA13260 THEORY OPERATION

### I. Introduction

The Astec P/N AA13260 is a feed-forward mode off-line switching power supply accepting either 115VAC or 230VAC nominal input and delivering four regulated DC outputs at a total of 170 watts.

### II. General Theory

Referring to the block diagram of the supply (Fig.1), the AC voltage from the mains is brought in through the EMI filter, rectified, and develops approximately 300VDC across the capacitive input filters. By turning on the switch transistor (shown in the power conversion stage), this 300VDC is applied across the primary winding of the power transformer. Due to the phasing of the power transformer windings, the output rectifiers are forward biased during the primary conduction time. Energy is transferred to the output filters and then to the load.

The control circuit senses the +5VDC and +12VDC outputs. It determines the point at which the turn-off circuitry disables the switch transistor.

The protection circuitry senses over and under voltage conditions on all four outputs, over current on the +/-12VDC rails, and also generates a power good signal. Should the protection circuitry sense a fault, it shuts down the power converter until the mains is recycled.

### III. Specific Operation (Refer to Circuit Diagram)

#### A. EMI Filter

The EMI Filter consists of a common mode choke (T201), differential mode chokes (L201,L202,L203), line to line caps (C201,C202), and line and neutral to ground caps (C203,C204). The purpose of this circuit is to suppress conducted Electro Magnetic Interference which is being fed back into the AC mains by the power supply and the logic systems connected to the power supply.

#### B. Surge Protection

Because the AA13260 has a capacitive input filter, input surges can be very high due to the fact that the input capacitors act like a short circuit when power is first applied. Thermistors are designed into the input circuit to limit the turn-on surge. As current passes thru the thermistors (R202,R203,R204,R205) they heat up and consequently their resistance drops to near zero.

### C. Capacitive Input Filter and Voltage Select

C205 and C206 make up the energy storage from which the power stage draws to deliver energy to the loads. These two capacitors are wired in series which allows us to tap off from the center point. When the voltage select is in the 230VAC position this center tap is left unconnected. In this situation, the diode bridge is connected as a full wave bridge rectifier and produces a DC voltage equivalent to 1.414 times the input voltage (approximately 300VDC). When the voltage select is in the 115VAC position, the center tap is connected to the neutral line. This converts the input capacitor array into a capacitive doubler, charging C206 down approximately 150VDC during the negative half-cycle of the AC waveform and charging C205 up 150VDC during the positive half-cycle of the AC waveform. This results in B+ voltage across the full capacitor array of approximately 300 VDC. Consequently, the primary winding and switching transistor see the same B+ operating voltage at both voltage select positions.

### D. Power Conversion

As explained in Section II, The power transistor (Q11) turns on, drawing current through the primary winding to return, developing a magnetic field with a linear current ramp. Please notice the dot location on this winding. When Q11 is on, the polarity is such that the dot end of the winding is positive. The secondary windings have the same polarity. With dots marking the positive end of the windings at this instant of the cycle, the output rectifiers (D12,D13) are forward biased and conduct. Thus the energy being stored in the input caps is transferred to the output filters and the load.

A common core output choke (L2) is placed between the output rectifiers (D12,D13) and the output filters. This choke serves two purposes. One, it stores energy delivered from T1 in order to help compensate for load surges on the +12v and +5v outputs. Two, it acts as a transformer sourcing energy for the -12v and -5v outputs. The -12v and -5v outputs are derived from separate windings on L2.

The output filters are of Pi filter configuration with inductors preceded and followed by capacitors. For example, on the +5v output the filter consists of C19 followed by L4 followed by C26. The +12v and -12v outputs have similar filters. The -5v output is via a 3T regulator (IC3).

## E. Control Circuit

The control circuit consists of an Astec developed chip (IC2), a pulse transformer (T2), and associated timing and reference generating components. IC2 compares the output with a generated reference voltage. When the output starts to rise beyond a preset limit, IC2 feeds a pulse thru the primary of T2. This pulse is transferred to the turn-off circuitry in the base control of switch transistor (Q11). Consequently, Q11 is quickly turned off preventing further energy transfer to the secondary of T1 on that cycle.

## F. Turn-on/Turn-off Circuits

This section of the circuit consists of seven different parts.

1. The clock consists of Q6 and Q7 along with associated components. The clock timing is established by R12 and C4. R18 supplies an AC undervoltage lockout that prevents the clock from generating a pulse sufficient to turn on Q11 if the AC line is too low.
2. The clock is inhibited during Q11 on time by Q5. It is inhibited during Q11 recovery time by Q4.
3. When Q11 is turned on, positive feedback for base drive is supplied thru T3.
4. The normal method of turn-off for Q11 is via a pulsed signal fed back from the output thru T2 to the base of Q9. Q9 turns on and quickly robs Q11 of base-drive, thereby turning Q11 off.
5. Q11 can also be turned off via the primary volt/second limiter. When Q11 is conducting, a voltage is developed across R35. The voltage is directly proportional to the collector current of Q11. Should the current become too great, due to an overload on the secondary side of T1, the voltage across R35 will turn on Q8. This transistor then turns on Q10 and Q9, which turns off Q11.
6. If for some reason, control of Q11 can not be maintained, R23 which is a fusible resistor will open the collector current path preventing further damage to the power supply.

7. The shutdown latch can also control Q11 turn-off by inhibiting the clock pulse. The latch is initially triggered from the secondary protection circuitry thru opto coupler (IC1). Q3 provides a regenerative latch in conjunction with the transistor side of IC1. R3, C1, and Z1 provide a regulated voltage source to keep the latch on until prime power is recycled. In addition, Q2 inhibits false triggering of the latch upon power supply startup.

#### G. Protection Circuit

As stated in the General Theory section, the protection circuit fulfills numerous functions.

1. +/-12v over current protection - +12v output current is sensed via transformer (T4). The secondary of T4 provides a voltage proportional to the output current that is rectified and then fed to the base of transistor (Q104). When Q104 turns on, it turns off Q105 which turns Q12 and the LED portion of IC1 on. The -12v current is sensed as a voltage potential across resistor (R48). This voltage is then applied to the base of Q104 in the same manner as the +12v sense voltage. Capacitor (C103) is used to provide surge ride thru capability on the two outputs.
2. OVP, UVP is provided via a quad-comparator (IC102). The precision reference for IC102 is generated by programmable zener (IC101). Should any of the outputs cause IC102 to activate, Q12 and the LED portion of IC1 are turned on.
3. Power Good is also indicated by this circuit. It is tied to the +5v output thru resistor (R141). When transistor (Q106) is turned on, the power good signal is low and vice versa. The power good signal is high only when all four outputs are within their regulation band.

#### H. Fan Control

A 12VDC fan is operated from the -12VDC output. This circuit contains a fan speed control consisting of a normally open thermal switch in parallel with a ten ohm resistor. Under normal operation, the switch is open and the fan operates at a low speed. Should the power supply become too warm, the switch closes, shorting out the resistor, and the fan operates at full speed. When the power supply cools down, the switch opens again, slowing down the fan. In this manner a nearly constant temperature is maintained within the power supply.

### **Power Supply Jumper Setting**

1. Check to be sure that S201 is set to the proper voltage for the location in which the system is to be installed.



Power Supply Subassembly

Item	Quan	Description	Part No.
1	1	Power Supply, 170 Watt (Ref: Outline - PCB, 135/170 W. P.S.)	AXX-6018
2	1	Upper Enclosure-Power Supply	
3	1	Lower Enclosure-Power Supply	
4	4	Screw, #6-32 x 5/16 H.P. Thread From. W/T.S.S.	AHD-2746
5	7	Screw, #6-32 x 1/4 PPHD	AHD-2618
1		Support, Circuit Board	
7	1	Nut, Keps #6	AHD-7159
8	1	Nut, Keps #6	AHD-7159
9	1	Receptacle (AC In)	AW-1063
10	1	Receptacle (AC Out)	AJ-7538
11	1	Switch, Power	AS-1011
12	1	Bezel, Switch	AZ-1003
13	1	Bushing	
14	1	Cable, Power Switch To AC	AW-3334
15	1	Cover, Convenience	8590006
16	1	Insulator, Heat Sink	8539070
17	1	Screen, Power Supply	8729570
18	1	Fastener, Thermostats	8729563
19	1	Thermostat	AT-1005

POWER SUPPLY PARTS LIST

Tandy 3000 Power Supply

Symbol	Description	Part No.
Assy PCB-M AAL3260		
C1	Cap-MPR 0.047U +20% "X"	
C2,3,8,13,15	Cap-C 0.01U +80-20% 100V Z5U	
C4	Cap-P 0.015UF 50V +5%	
C5	Cap-C 270PF +10% 100V Z5F	
C6	Cap-P 0.01UF +5% 50V	
C7,25	Cap-C 1000P +10% 100V	
C9	Cap-MP 0.68U J 50VD	
C10	Cap-C 1000P +20% 3KV Z5P	
C11	Cap-E 47UF +20% 35V SM	
C12,16	Cap-C 4700PF +20% 50V	
C14	Cap-E 47U +20% 16V SM	
C17	Cap-P 0.047U +10% 250VDC	
C18,21,28	Cap-E 330U +20% 16V SM	
C19	Cap-E 2200UF +20% 16V SM	
C22	Cap-P 0.022U +20% 50V	
C23,27	Cap-E 3300U +20% 16V SM	
C24,32	Cap-MP 0.1U +10% 250V	
C26	Cap-E 4700U +10V SM	
C29	Cap-P 0.22U +10% 100V	
C30	Cap-E 1000U +20% 16V SM	
C31	Cap-MPR 0.01UF +20% 250V	
C33,34	Cap-C MTY 100NF +50-20%	
C35	Cap-MPR 1000PF 250VAC	
C36	Cap-MPR 4700P +20% 250V	
D9	Rect GP30A	
D20	Rect-SCK 31DQ04	
IC1	Opto-Coupler H11AV2	
IC2	IC AS4301	
Q2,5,7,8	TRS-NPN 2SD467	
Q3,4,6,10	TRS-PNP 2SB561	
Q9	TRS-NPN 2SC26550	
Q12	TRS-NPN 2SC1213PC	

Symbol	Description	Part No.
R1,2	Res-MOF 51K $\pm 5\%$ 1W	
R12	Res-MOF 27K $\pm 5\%$ 7W	
R18	Res-CF 330K $\pm 5\%$ 1/2W	
R23,35	Res-MF 0.33R $\pm 5\%$ 2W	
R24	Res-MOF 150R $\pm 5\%$ 1W	
R30	Res-WW 510R $\pm 5\%$ 5W	
R32	Res-MF 0.33R $\pm 5\%$ 1W	
R36,41	Res-CF 22R $\pm 5\%$ 1/2W	
R37,40	Res-CF 10R $\pm 5\%$ 1/2W	
R48	Res-MF 0.22R $\pm 5\%$ 1W	

Assy PCB-S Protection

C101	Cap-E 10UF $\pm 20\%$ 16V
C102	Cap-C 0.01U $\pm 20\%$ 150V z5U
C103	Cap-P 0.1U $\pm 10\%$ 100V
C104,105	Cap-MP 0.22UF $\pm 10\%$ 100V
I101	Regulator 431
I102	IC HA 17901P
Q101,103	TRS-PNP 2SB561
Q102,104, 105,106	TRS-NPN 2SD467
R101	Res-MOF 330R $\pm 5\%$ 1W

KIT AI AAI3260-S

D101-111	Diode-SI 1N4606
R102,103	Res-MF 2.7K $\pm 1\%$ 1/4W
R104-106, 108,110, 132,136	Res-CF 100K $\pm 5\%$ 1/4W
R107,114, 115,141	Res-CF 1K $\pm 5\%$ 1/4W
R109	Res-CF 56K $\pm 5\%$ 1/4W
R111	Res-CF 1.8K $\pm 5\%$ 1/4W
R112,135	Res-MF 2.2K $\pm 1\%$ 1/4W
R113	Res-MF 1.8K $\pm 1\%$ 1/4W
R116	Res-CF 470R $\pm 5\%$ 1/4W
R117	Res-MF 4.7K $\pm 1\%$ 1/4W
R118	Res-MF 6.8K $\pm 1\%$ 1/4W
R119	Res-CF 3.9K $\pm 5\%$ 1/4W

Symbol	Description	Part No.
R120,122,125	Res-MF 10K $\pm 1\%$ 1/4W	
R121	Res-MF 16K $\pm 1\%$ 1/4W	
R123	Res-MF 18K $\pm 1\%$ 1/4W	
R124	Res-MF 12K $\pm 1\%$ 1/4W	
R126,137	Res-CF 12K $\pm 5\%$ 1/4W	
R127	Res-CF 22R $\pm 5\%$ 1/4W	
R128	Res-CF 2.2M $\pm 10\%$ 1/4W	
R129,130, 142,143	Res-CF 68K $\pm 5\%$ 1/4W	
R133	Res-CF 22K $\pm 5\%$ 1/4W	
R134	Res-MF 8.2K $\pm 1\%$ 1/4W	
R138	Res-CF 150K $\pm 5\%$ 1/4W	
R139	Res-CF 2.7K $\pm 5\%$ 1/4W	
R140	Res-CF 3.3K $\pm 5\%$ 1/4W	

Symbol	Description	Part No.
P1	Assy Wire Hrn O/P P1	
P3	12 Ckts Connector Assy	
P4	Assy Wire Hrn O/P P4	
P5	Assy Wire Hrn O/P P5	
P6	Assy Wire Hrn O/P P6	

KIT AI AA13260-M

D1-6,11,14, 17,19	Diode-SI 1N4606
D8	Rect RGP10J
D16	Rect RGP10B
D22,23	Rect 1N4001GP
R3	Res-CF 390K $\pm 5\%$ 1/4W
R4,50,51	Res-CF 10K $\pm 5\%$ 1/4W
R5	Res-CF 27K $\pm 5\%$ 1/4W
R6,8,9,10, 11,13,38	Res-CF 1K $\pm 5\%$ 1/4W
R7,25,26, 28,46	Res-CF 100R $\pm 5\%$ 1/4W
R14,29	Res-CF 4.7R $\pm 5\%$ 1/4W
R15	Res-CF 2.2K $\pm 5\%$ 1/4W
R16	Res-CF 18K $\pm 5\%$ 1/4W
R17	Res-CF 15K $\pm 5\%$ 1/4W
R19,27,31, 34,44	Res-CF 10R $\pm 5\%$ 1/4W
R20	Res-CF 22R $\pm 5\%$ 1/4W
R21	Res-CF 27R $\pm 5\%$ 1/4W
R22	Res-CF 3.9K $\pm 5\%$ 1/4W
R33	Res-CF 12R $\pm 5\%$ 1/4W
R39,54	Res-CF 470R $\pm 5\%$ 1/4W
R42,64	Res-CF 3.3K $\pm 5\%$ 1/4W
R43	Res-CF 39R $\pm 5\%$ 1/4W
R47	Res-CF 82R $\pm 5\%$ 1/4W
R49	Res-MF 560K $\pm 1\%$ 1/4W
R52	Res-MF 180K $\pm 1\%$ 1/4W
R53	Res-CF 4.7K $\pm 5\%$ 1/4W
R55	Res-MF 6.8K $\pm 1\%$ 1/4W
R56,57,60,61	Res-CF 100K $\pm 5\%$ 1/4W
R58,59	Res-CF 220K $\pm 5\%$ 1/4W
R62	Res-MF 18K $\pm 1\%$ 1/4W
R63	Res-MF 2.7K $\pm 1\%$ 1/4W
R65	Res-CF 180R $\pm 5\%$ 1/4W
Z1	Diode-Z 10V 1W

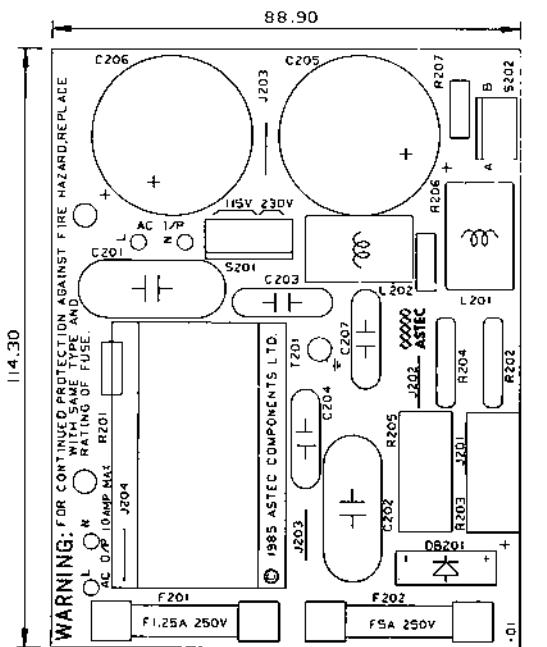
Symbol	Description	Part No.
L1	AAL3240 Trim-Choke 4T	
L2	Output Main Choke Assy	
L4	5V Filter Choke Assy	
T1	TRF Pwr AAL3260	
T2	AAL3070 Control TRF Assy	
T3	Current TRF Assy	
T4	Current Trf Assy +5V	
	TRF Subassy Pri ETD44	

Symbol	Description	Part No.
L3	Filter Choke Coil Assy	
L5	Choke Coil Assy	
	Assy-HTSK-12V Rect	
D21	Rect RG3B	

Symbol	Description	Part No.
D12,13,15,18	Assy-HTSK Rect/Sck	
Q11	Assy-HTSK Pwr Transistor	
IC3	IC Lin 3P LM337T (NEG)	

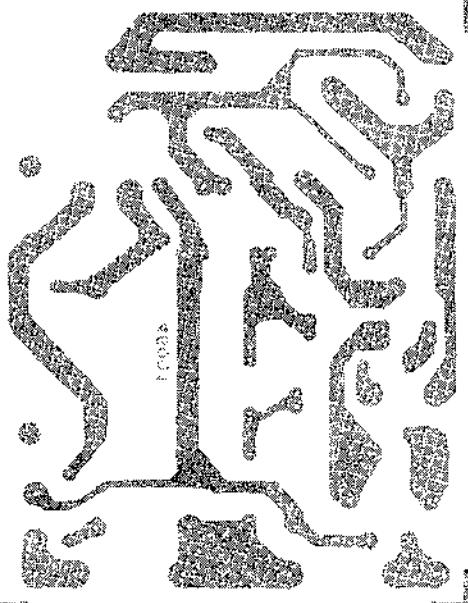
Symbol	Description	Part No.
Assy PCB-S EMI		
C201,202	Cap-MP 0.47U $\pm 20\%$ 250 VAC	
C203,204	Cap-P 4700P $\pm 20\%$ 250VAC Y	
C205,206	Cap-E 470UF M 200V HLP	
C207	Cap-MPR 1000PF 250VAC	
F201	Fuse 4A 250V 3SB	
F202	Fuse 5A 250V 3AG	
L201,202	SN Coil 72UH 3A 0.042R	
R201	Res-CF 470K $\pm 5\%$ 1/2W	
R202,204	THMTR CL50 $\pm 20\%$ 7R	
R203,205	Res-WW 8.2R $\pm 5\%$ 5W	
R206,207	Res-MOF 68K $\pm 5\%$ 1W	
T201	EMI COM Mode TRF	
KIT AI AA13260~EMI		





MODEL : AA13260    DESC. : EMI BOARD  
P/N : 042-020-60-01    DATE : 16 JUL 85  
COMPONENT SIDE

32,672

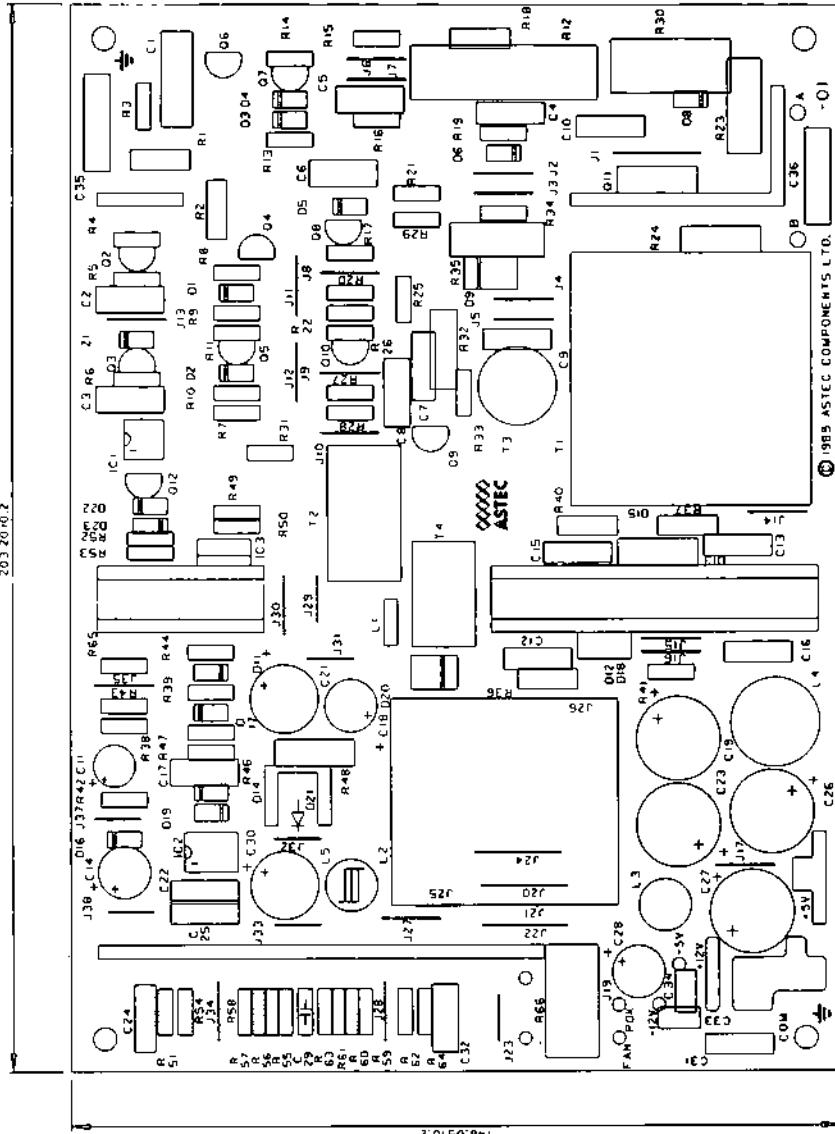


144-1000

MODEL 344-1000 ECU 5000  
P/N 344-1000-000-01  
COMPONENT SIDE  
DATE 3-20-74-SD

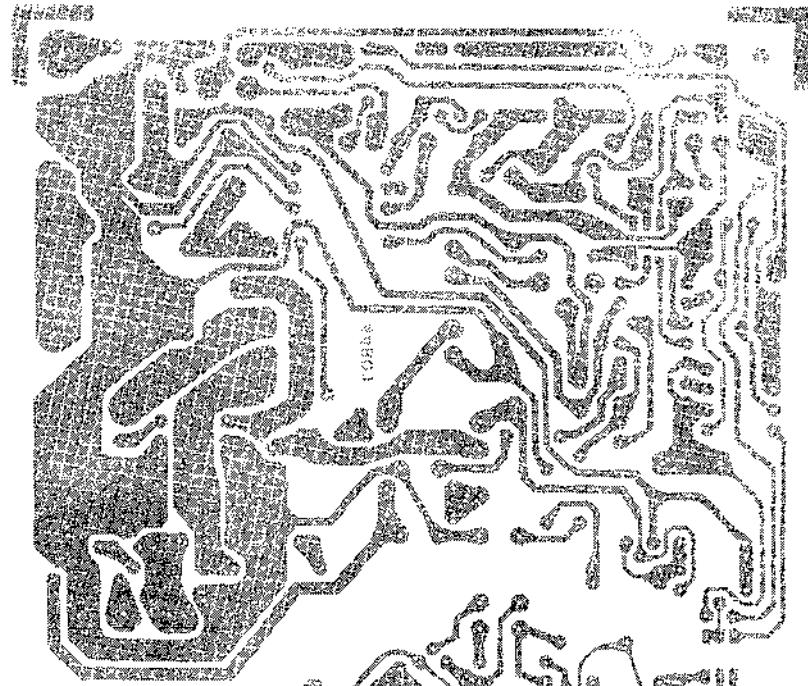


203 2040.2

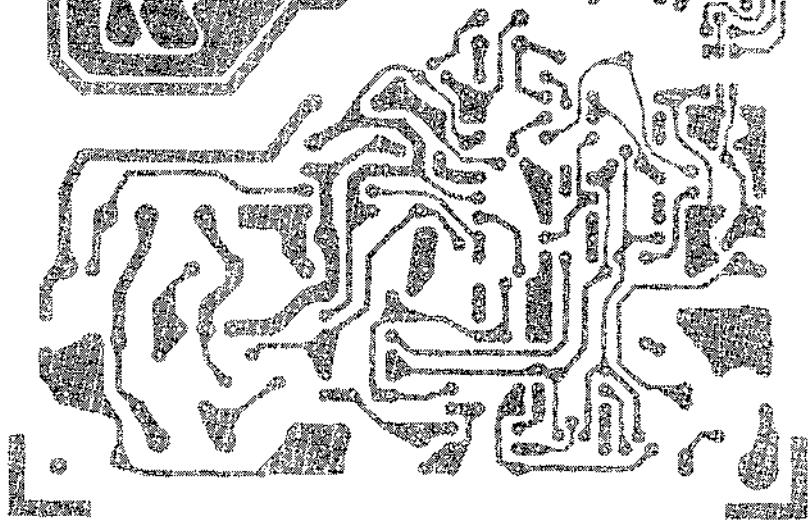


MODEL A13260.PCB.MAIN SCALE : 2:1 COMPONENT SIDE VIEW 042-02044801 18 JUL 85  
© 1985 ASTEC COMPONENTS LTD.

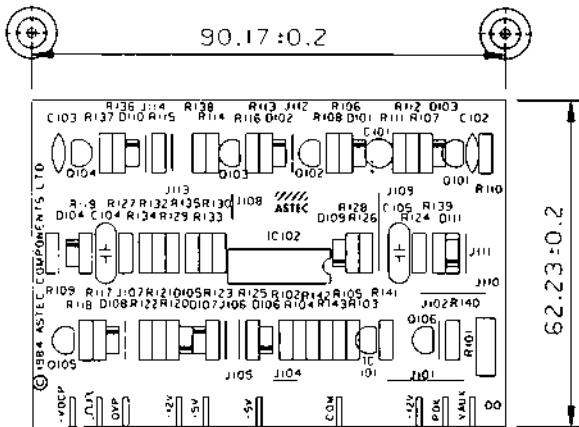
4



20824M

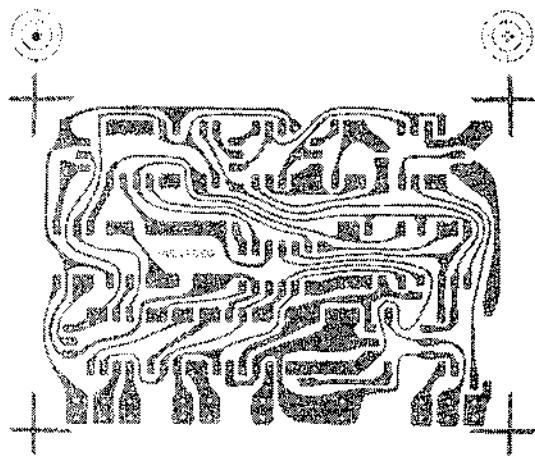


1861058B1  
P/N 547-00200  
COPPERCLAD  
PCB  
1861058A1  
P/N 547-00250  
COPPERCLAD  
PCB



AA13260  
COMPONENT SIDE

042-02046200  
DATE: 20 JUNE 85



VAA1530  
DATE : JOURNAL 89  
COPPER SIDE  
043-02048200

**REPAIR MANUAL**  
for the  
**ASTEC AA13260 POWER SUPPLY**

**SECTION 1 TEST SET UP**

**A. EQUIPMENT NEEDED**

1. Isolation Transformer (minimum 500VA rating).  
Please note that dangerously high voltages are present on this power supply. So for the safety of the individual testing please use an Isolation Transformer. The 500VA rating is needed to prevent the AC waveform from being clipped off at the peaks. This type of power supply has peak charging capacitors and draws full power at the peak of the AC waveform.
2. 0-280V VARIAC (VARIABLE TRANSFORMER)  
This is used to vary the AC input voltage.  
Recommend 10A, 1.4KVA rating, minimum.
3. VOLTMETER  
Used to measure DC voltages up to 50 VDC and AC voltages to 400 VAC. Recommend 2 DVM's.
4. OSCILLOSCOPE  
Used to measure specific waveforms.  
Also need X10 and X100 probes.
5. RESISTIVE LOADS  
See Table 1 for values.
6. OHM METER
7. WATT METER

**B. SET UP PROCEDURE**

Set up as shown in Figure 1. You will want to monitor the input voltage and power as well as the +5 volt output.



## SECTION II

For continued operation and protection against fire or shock hazard, consideration should be given to returning the unit to ASTEC for repair.

### A. VISUAL INSPECTION

Check the power supply for any broken, burned or obviously damaged components. Repair or replace any damaged components.

### B. POWER UP

First note the position of the input voltage select jumper, located on the EMI/FILTER board. Position this jumper in the 230 VAC position for testing. This manual will assume 230 VAC operation.

Load the power supply with the minimum loads as specified in Table 1.

While monitoring the output voltage with the DVM and Oscilloscope and also monitoring the input voltage with the watt-meter and DVM. Bring the AC power up slowly using the VARIAC.

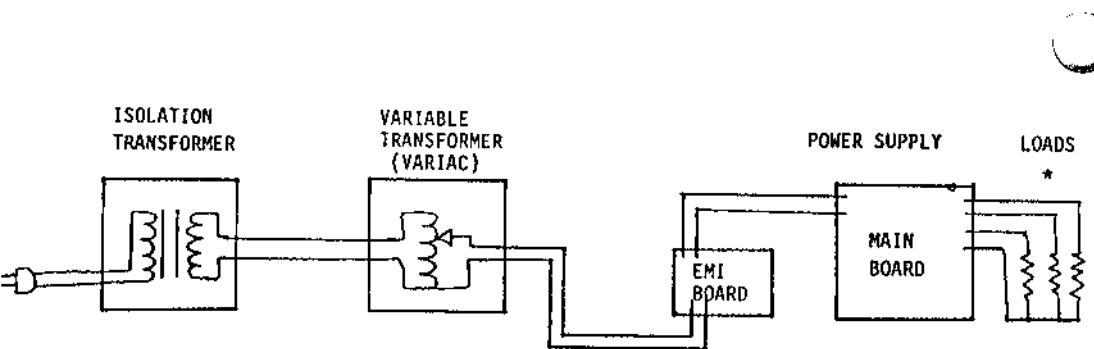
If the watt-meter shows significant power consumption with the low AC power applied, shut down the system and refer to Section III.

The power supply should start at approximately 100-120 VAC and begin to regulate when 190 VAC is applied.

If the output has reached +5 volts, do a performance test as shown in Section IV.

If there is no output present refer to Section III.

FIGURE 1 TEST SETUP



\* NOTE: All connectors must be loaded and all returns must be used to achieve proper regulation.

FIGURE 2 OUTPUT CONNECTORS

P1  
(FAN)

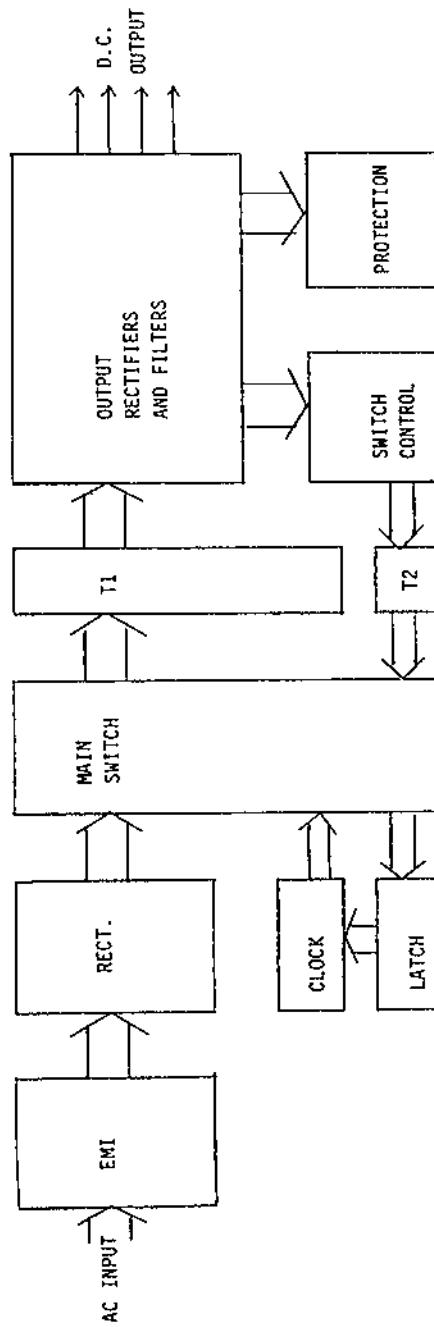
O	RTN
O	-12V

P3

1	O	+5V
2	O	+5V
3	O	+12V
4	O	+5V
5	O	+5V
6	O	RTN
7	O	RTN
8	O	RTN
9	O	RTN
10	O	-5V
11	O	-12V
12	O	PWR GOOD

P4,5,6

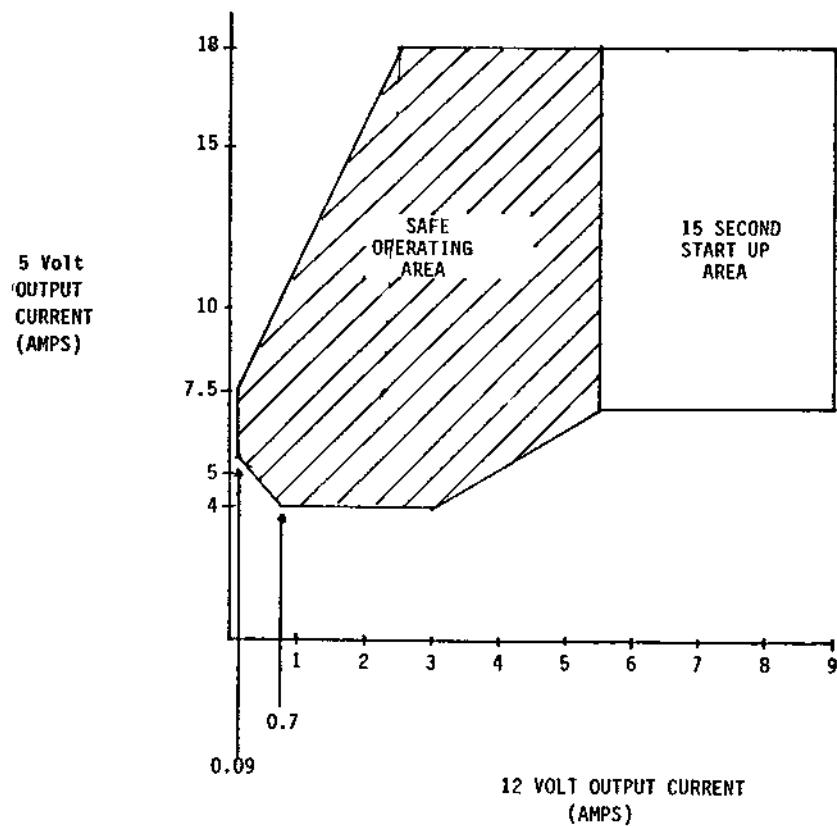
1	O	+12V
2	O	RTN
3	O	RTN
4	O	+5V

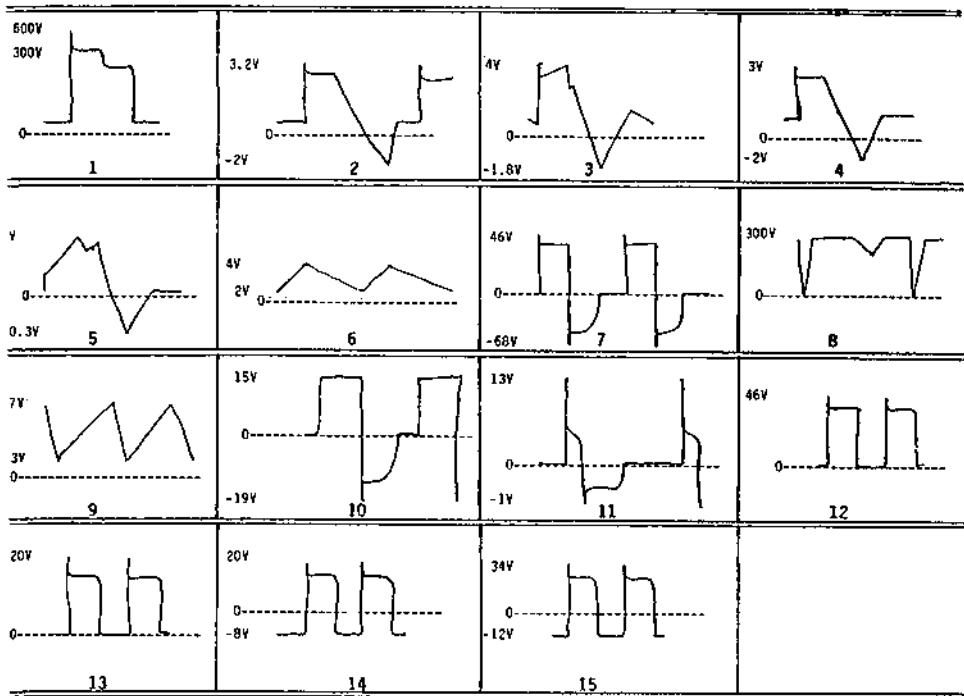


A113250

BLOCK DIAGRAM

TABLE III





#### WAVEFORMS

- |                  |                 |
|------------------|-----------------|
| 1. Q11 Collector | 9. D4 Anode     |
| 2. Q11 Base      | 10. D2 Anode    |
| 3. IC1 Base      | 11. D11 Cathode |
| 4. Q7 Base       | 12. D12 Cathode |
| 5. Q8 Base       | 13. D13 Cathode |
| 6. IC2 PIN 8     | 14. D20 Cathode |
| 7. T4 INPUT      | 15. D21 Cathode |
| 8. D8 Anode      |                 |

TABLE 1

LOAD BOARD VALUES

OUTPUT	MIN LOAD	LOAD R	MAX LOAD	LOAD R
+5.1	4 AMPS	1.25	18 AMPS	0.28
-5.1	0	0	0.3 AMPS	17
+12	0.09	133	9 AMPS	1.33
-12	0	0	0.3 AMPS	40
FAN	0	0	0.75 AMP	16

TABLE 2

VOLTAGE AND RIPPLE SPECS

OUTPUT	MIN	MAX	RIPPLE
+5.1	4.95	5.25	50 mV p/p
-5.1	-4.95	-4.95	100 mV p/p
+12	11.4	12.6	100 mV p/p
-12	-13.2	-10.8	150 mV p/p
FAN	10.8	13.2	150 mV p/p

### SECTION III NO OUTPUT

- A. Check Fuse. If fuse is blown, replace it but do not power up until a preliminary visual check has been made.
- B. Check for a proper connection between the main PWB and the EMI/Filter board.
- C. Preliminary check of major primary components.  
Check Thermistors R202 and R201  
D100E Bridge DB201  
Power Transistor Q11  
Transistors Q9,Q10  
Transformer T201, chokes L201, 202
- D. Preliminary check of secondary components using an OHM Meter from output common to each output, with loads disconnected. Check for shorted rectifiers or capacitors.
- E. Check for B+. Set up power supply and attach X100 scope probe ground to point "B" or negative side of C206.  
Slowly turn up AC power and check for B+ voltage, the positive terminal of the diode Bridge DB201. With an input of 190 VAC this point should be between 300 to 400 VDC.  
If this is not correct check the fuse, thermistors D100E block and input capacitors.
- F. Check waveforms. Using the X100 probe, begin by checking Q11 collectors' waveforms and working back through the associated turn on/off and clock transistors by comparing to the related figures.
- G. Check the latch circuit. Measure between output common and Q12 base with a DVM. If this point is zero volts the latch is disabled. If it is greater than 0.6 volts the latch is enabled. If the latch is enabled the cause must be found and removed before the power supply will operate.  
If there are no shorted components in the secondary circuitry, check Q12, Q104, Q105, T4 and the associated circuits.  
Overvoltage protection and undervoltage protection are controlled by IC102 which uses IC101 for a voltage reference. These signals may also drive Q12 into a latch condition.

A final test to determine if the latch circuit is the cause, you may remove R7 which will disable the latch. While closely monitoring the +5V output slowly increase the AC input until the power supply begins to regulate. If the +5 volts begin to go too high, shut down the power supply and proceed to the "High Output Section"

If the power supply still did not power up, check the clock circuit consisting of Q4, Q5, Q6, and Q7.

H. High Output Section.

Begin by visually checking components IC2, R64, R57, 58, 59, 60, 61, 62, 63 for loose or broken connections. If these are okay, power up unit and measure pin 2 of IC2. If this is approximately 2.5 volts, check pin 8 of IC2 and compare with Fig. 6. If this is okay, follow signal path through R44 to T2. Also check T2 for opens and shorts.

I. Perform all safety tests for hi-pot and leakage before returning power supply to normal operation.

## **SECTION IV      PERFORMANCE TEST**

**Each of these test conditions should be set up and noted to be within the limits specified in Table 2.**

TEST	INPUT	+5	-5	+12	-12	FAN
1	190	18A	0.3A	5.5A	0.3A	0.75A
2	270	18A	0.3A	5.5A	0.3A	0.75A
3	220	18A	0	2.5A	0	0.75A
4	270	4A	0	0.7A	0	0
5	190	4A	0	0.7A	0	0
6	190	18A	0.3	3.5	0.3	0.75
7	190	4A	0	5.5	0	0
8	270	4A	0	5.5	0	0

**IMPORTANT:** See table III for safe operating configurations.

**NOTE:** All measurements are made at the connectors.



Notes on the preliminary release of the Tandy 3000 diagnostics

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Enclosed are the preliminary diagnostics for the Tandy 3000. The manuals for TDC, DISKREL, and IOTEST have been shipped earlier and have been omitted. If you need them, call Gary Kueck at Technical Support, or leave a message to root on Techcomm.

The SETUP program and the hard disk format programs have been included on this diskette also. They are not visible from the menu, but are visible in the directory.

There will be a diagnostic ROM board for this computer. It will be able to run diagnostics from an onboard ROM. It will also display a series of boot codes during bootup, these are mentioned in the enclosed documentation.

The version of TDC on this diskette has the specifications for all of the Tandy 3000 disk drives and the new 1200 FD disk drives (TM65-2L). It has a bug in it and will only work with the M4854 (Hi capacity) drives when used on the Tandy 3000. The next version of TDC will correct this. This version will work properly on the other drives (Low capacity) when used on a Tandy 1200. All that is required is to copy this version of TDC to a 1200 diskette, attach the drive to be aligned to the 1200, and run TDC on the 1200.



## TANDY 3000 Power-On Self-Test Error Codes

The "DIAG OUTPUT" codes are placed at the diagnostic status port 80h to indicate tests in progress and failed tests on an installed diagnostic display board. The "BEEP CODES" are announced on the speaker if and only if a fatal failure is detected. For instance: "2-1-4" (A burst of two beeps, a single beep, a burst of four beeps) indicates a failure of bit 3 in the first 64K of RAM. Both sets of codes are only used prior to screen initialization and screen retrace verification. Once the screen has been verified, messages are written directly to the Video Memory at 80000 & B8000 hex.

## DIAG

PORT OUTPUT	BEEP CODES	DESCRIPTION OF TEST OR FAILURE
----------------	---------------	-----------------------------------

01h		80286 register test in-progress or failure
02h	1-1-3	CMOS write/read test in-progress or failure
03h	1-1-4	BIOS ROM checksum in-progress or failure
04h	1-2-1	Programmable Interval Timer test in-progress or failure
05h	1-2-2	DMA initialization in-progress or failure
06h	1-2-3	DMA page register write/read test in-progress or failure
08h	1-3-1	RAM refresh verification in progress or failure
09h		1st 64K RAM test in-progress
0Ah	1-3-3	1st 64k RAM chip or data line failure - multi-bit
0Bh	1-3-4	1st 64k RAM odd/even logic failure
0Ch	1-4-1	1st 64k RAM address line failure
0Dh	1-4-2	1st 64k parity failure
10h	2-1-1	1st 64k RAM chip or data line failure - bit 0
11h	2-1-2	1st 64k RAM chip or data line failure - bit 1
12h	2-1-3	1st 64k RAM chip or data line failure - bit 2
13h	2-1-4	1st 64k RAM chip or data line failure - bit 3
14h	2-2-1	1st 64k RAM chip or data line failure - bit 4
15h	2-2-2	1st 64k RAM chip or data line failure - bit 5
16h	2-2-3	1st 64k RAM chip or data line failure - bit 6
17h	2-2-4	1st 64k RAM chip or data line failure - bit 7
18h	2-3-1	1st 64k RAM chip or data line failure - bit 8
19h	2-3-2	1st 64k RAM chip or data line failure - bit 9
1Ah	2-3-3	1st 64k RAM chip or data line failure - bit A
1Bh	2-3-4	1st 64k RAM chip or data line failure - bit B
1Ch	2-4-1	1st 64k RAM chip or data line failure - bit C
1Dh	2-4-2	1st 64k RAM chip or data line failure - bit D
1Eh	2-4-3	1st 64k RAM chip or data line failure - bit E
1Fh	2-4-4	1st 64k RAM chip or data line failure - bit F

continued

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Error Codes

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20h	3-1-1	slave DMA register test in-progress or failure
21h	3-1-2	master DMA register test in-progress or failure
22h	3-1-3	master interrupt mask register test in-progress or fail
23h	3-1-4	slave interrupt mask register test in-progress or fail
25h		interrupt vector loading in-progress
27h	3-2-4	keyboard controller test in-progress or failure
28h		CMOS power-fail and checksum checks in-progress
29h		CMOS configuration info validation in-progress
2Bh	3-3-4	screen memory test in-progress or failure
2Ch	3-4-1	screen initialization in-progress or failure
2Dh	3-4-2	screen retraces tests in-progress or failure
2Eh		search for video ROM in-progress
30h		screen believed operable

ECOMMSpecifications

Ecomm will test both Tandy and IBM compatible RS-232 option boards for proper operation. Ecomm will test a board configured for channel 1 using the primary comm interrupt and test a board configured for channel 2 using the secondary comm interrupt. The test will run on the Tandy 1000, 1200, and 3000 computers.

Not all features may be available on every board, however Ecomm is designed to test for interrupts, break generation and detection, and both generation and detection of control signals.

For a standard test, a jumper plug should be constructed that loops RTS <=> CTR, DTR <=> DSR+CD+RI, and TX <=> RX. The RTS signal will be toggled and tested at the CTS pin. The DTR signal will be toggled and tested at DSR, CD, and the RI pins.

Interrupts are enabled for the test and the IBM scheme for gating interrupts at the 8250 is enabled so that the test will work on both Tandy and IBM boards.

Parameters

The following is required:

Computer: Tandy 1000, 1200 or 3000

RS-232 Card

Loopback connector in the following configuration:

DB-25	Signal	DB-9
2-3	TX-RX	2-3
4-5	RTS-CTS	7-8
6-8-20-22	DTR-DSR-CD-RI	1-4-6-9

continued

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ECOMM

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Operation and Messages

The test is initiated by typing 'ecomm'<CR> or selecting ecomm from the main menu. At this point the copyright and version message will appear, and a prompt for the channel to test, 1 or 2. After selecting the channel, the program will prompt for terminal mode or control check. The program will then attempt to init the UART and then check for the connection of the loopback cable. If no loopback connector is found, the program will display a message that it couldn't find it, and give the option of <M> - try testing anyway, <Q> - quit to MS-DOS, or any other key to test for the connector again.

Once the program finds the connector, it will clear the screen and put up a status display. On the left of the screen are the indications as to how the program expects the loopback to be wired. For example, RTS =>CTS. The DTR line should be connected to the DSR, CD, and RI lines. The middle column displays the static or fixed registers. That is, if the line goes to a logic 0, did the program find a logic 0 in the associated input register. The same for a logic 1. The column is configured for a 0 / 1, this means the an OK / FAIL would indicate that the program found a 0 in the input register when it should have found a 0, but it did NOT find a 1 when it was testing for a 1.

The column on the right is the Delta or change column. The 8250 sets a special flag in the registers if a status line changes. For a 1 / 0, this means that the UART detected the line changing to a 1 or changing to a 0. The RI line is special, it will only detect the change on a 1 to 0 transition hence the "na" for the 0 to 1 transition.

The break detect test is done next. This test programs the UART for 1200 baud and sends a long space disconnect. The program loops looking at the register in the UART that detects break.

The Baud Rate Generator Test points to each of the divisor registers in the UART and tests them for all 256 possible combinations. It checks that the divisor is actually working at the Baud Rates used by the program, but it only tests that the CPU can write and read the other values to the divisor.

The last test is an ASCII loopback test at 1200 baud. All previous tests were done using poll mode of the UART. For the TX-RX test, interrupts are enabled for received characters. The interrupt is used to signal the CPU to go get the characters. The program still polls the received character pending register before trying to read a character. Any failures of the transmitter should cause the system to "timeout" and display the "FAIL" message in TX. At the completion of transmitting a complete ASCII set, the program checks that an identical set is in a buffer pointed to by the interrupt service routine. Any errors and the message "FAIL" will appear in RX.

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ECOMM

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\*\*\*\*\*  
Diagnostic Memory Test  
\*\*\*\*\*

## General Description:

Before testing the memory, the program will take the following steps:

- 1) Check for either monochrome or video color board.
- 2) If a video color board is available on the system the program will reside in the surplus video RAM and the CRT mode will set properly.
- 3) If monochrome board available, then program will reside on the bottom of memory, and the CRT will set for 40x24 mode.
- 4) If a combination of both the monochrome and the color board are available then the program will reside in the video RAM. In this mode the program will use the color board for display. Make sure that the color CRT cable is connected to the color connector.

After the CRT mode is set, the program will display the main menu which consists of memory size and the different type of test. The format of main menu is as follows.

=====

Tandy xxxx Diagnostic Memory Test  
Rev. Date XX/XX/XX.  
Copyright TANDY Corp.  
All Rights Reserved

XXX K Memory  
<D> Date  
<R> Refresh  
<A> Automatic

Select:

=====

---

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**Type of Test:**

This program consists of three types of tests:

**1) Data Test:**

Write out all memory with fixed data patterns:  
(00H,55H,AAH,& FFH), and read back to compare the data read and  
the data written.

**2) Refresh:**

This test is actually a modified address, except that after  
writing all memory locations there is a delay of 30 seconds  
before reading the data back. If the refresh circuitry is not  
functional, then there will be an error.

**3) Automatic:**

The automatic test also has it's own menu which is shown  
below.

---

**Selection:**

<M> Modified Address  
<C> Checker Board  
<W>Walking Bit (word length)  
<B>Walking Bit (byte Length)

---

In this menu you have the option to choose the starting and ending segment.  
For example, when you depress 1, the logical segment will be displayed next  
to it (i.e 1000h logical). In this menu there are four types of tests, which  
are described below:

**1) Modified Address:**

Write out to all memory locations with unique data pattern generated  
from the address (segment address, Offset address, & Mask pattern).  
The difference between Short and Long tests is that the mask pattern will go  
from 0000h to OOFFh in Short and from 0000h to FFFFh in Long test. The mask  
pattern will be shown only when modified address test is selected.

**2) Checker Board**

Write out to all memory locations with fixed data patterns, (55AAH and  
AA55H), and read back to compare the data read and the data written. After  
each pass the data pattern will be changed.

## 3) Walking Bit (Word and Byte)

In this test, all memory locations will be filled with zero's and then a one will be stepped throughout the memory. The data will be complemented after each pass count (i.e one's will be filled with zero will be stepped).

When a memory read error has been found, it logs the information in the format shown below, where data written, data read back and address (Base=segment address and offset address) is displayed.

---

\*\*\*\*Memory Test\*\*\*\*\*

xxxxk Memory

Written      Read    Base

Offset

xxxx            xxxx    xxxx

xxxx

xxxx            xxxx    xxxx

xxxx

:                :        :

:

:                :        :

:

xxxx            xxxx    xxxx

xxxx

Parity At:xxxx:xxxx

Segment At:xxxx:xxxx

Mask\_pattern :xxxx

Pass-count : xxxx Error-count : xxxx

---

Note : 'xxxx' represents a hex value.

The physical address can be given from Logical address (Base : Offset).

Base Address      B BBBB    16 bits

Offset Address      0 0000    16 bits

Physical address = P PPPP    20 bits

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Throughout the memory test, the scratch pad registers are assigned as follows:

AX : General Purpose  
BX: Offset pointer from segment base register  
CX: Modified Address Mask Pattern  
DX: I/O Space pointer

BP: Current segment address  
SI: Display pointer (source)  
DI: Display pointer (destination)

DS: Test (Current) segment  
ES: Message display segment

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MEMTEST  
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**TANDY 3000 INITIALIZATION INFORMATION**

The Tandy 3000 System ROMs have self test Diagnostics which are designed to aid in determining the level of functionality of a computer in a System with a fault condition. The self test will also provide a means of a quick functional test of the system, therefore giving the operator a level of confidence in the condition of the computer. The self test will complain with a code displayed at port 80h on the diagnostic board or on the Video display when a fault is present. If the computer is functional, with regard to the self test, then it will proceed to "Boot" the operating System from the floppy disk.

The Diagnostic EPROM is very similar to the operating system self test. The following applies to the Diagnostic Self Test EPROM self test.

The 8088 CPU has a reset scheme which starts the computer by executing the instructions that it sees at address location OFFFFD hex. This means that the CPU must first be able to select the EPROM code at this address and be able to read the data contained in the EPROM. There is a large portion of the machine which must be functional in order for this to take place. If the computer cannot read the contents of the EPROM, then we must determine the location of the fault.

If the data bus buffer at reference designation U80 & U81 is replaced with a dip header which has been modified to take the CPU always see a NOP instruction then the CPU would cause the Address Bus to increment from OFFFFD to OFFFFF hex, back to 00000H and up to OFFFFF hex again. A dip header with pull up and pull down resistors to cause a 90hex to appear on the bus to the CPU, . This repeating process will cause a pattern to appear on the scope when monitoring the address lines. The pattern is easily identified due to the fact that the address signal's period's multiply by 2 as you go from A0 to A19. This means that "A0"’s frequency is twice that for "A1", etc. The observation of a break in the factor of 2 relationship across the Address Bus will identify a fault on the bus. Another consideration is that since all addresses are generated in this test loop, we realize that all memory mapped decoders should have a pulse for that time when it's address is generated.

Once the CPU can access the instructions in the ROM and the I/O ports are functional, we can proceed with the initialization.

The DIAGNOSTIC EPROM contains instructions to the CPU to initialize the computer. Initialization is the process by which the CPU sets up a starting value for every programmable function on the logic board in a sequence so that the machine "wakes up" by doing the most important things first, then those not as critical functions later.

The Tandy 3000 starts out with a jump instruction at the CPU reset location (OFFFF0 hex). This ensures that the CPU is told where to fetch the first instructions that the computer is to work on. The first instruction after the Far Jump is the CLI instruction (code FA hex).

The CPU Maskable Interrupts are shut down first because we have not posted a vector for the Interrupt Service Routine and the computer would go out of control if an interrupt occurred. The next most important thing is to shut off the Parity NMI Interrupt with output of 80h to port 70h. Next we see how much Video Memory we have in the computer, but prior to testing the Memory we must ensure that it has what is needed to make it functional.

When testing a faulty logic board, it is best to use a "known good" Monochrome Video Memory Board. This will assist in knowing if the System Bus is functional.

The Monochrome Video board has static RAM for memory and does not require 6845 operation for memory refresh. The color board has Dynamic RAM and so the 6845 must be functional to provide refresh so that we can test the memory to see if it is working. If the Video Memory is not functional at all, we output the error code to port 80h to convey this fact to the operator. Generally, if the Video Memory is faulty, then we have some major problems with the computer that will take some scope signal tracing to isolate. Often the Video Memory is partially functional. In this case the message complaining about the Video Memory problem will be partially displayed on the Video screen. The knowledge of what should be displayed and what in fact is being displayed can be very helpful in determining the fault condition. One thing is the fact that most of the screen should have spaces with the light gray attribute. Observe what is actually being displayed in place of the space and analyze the bits that are different to find the fault. This information will assist in finding the faulty condition and correcting it. When the Video Memory is functional it is used for the CPU "Stack" and "Data" Segments. Upon successful completion of the Diagnostic "Stack" test the word "Stack" will appear at the top of the screen. This designates that there is enough Video Memory available to establish a stack and data segment. Access to this Video Memory is by writing to the Monochrome Address at B0000 or Color at B8000 hex. Failure to be able to address this area would prevent any messages from being displayed on the Video Screen.

After establishing that the Video Memory is functional we must determine how much dynamic RAM memory is in the System. The dynamic RAM Memory Refresh circuit must be made functional in order to test it. The Refresh requirements are different for the System Memory, we must have channel 1 of the Counter/Timer and the 8 bit Ring Counter provide the Refresh. In order to proceed we need to test for the functionality of the Counter and the Ring Counter. This is done by writing a rotating Logic 1 pattern across the data bus of the Counter Timer to test it's I/O Operation. The Diagnostic EPROM will indicate a "T" at the top right portion of the Video as an indication of completion of the Counter portion of the initialization sequence.

Dynamic RAM memory needs to have Refresh Cycles to ensure that the information stored is not lost. The refresh is accomplished by simply reading each row at the Dynamic RAM Memory. We can Refresh the memory by setting up Counter Timer Channel 1 for 15 user "tics"; for each "tic" the 8 bit Ring Counter becomes Bus Master and reads from memory. The refresh Detector is checked so as to ensure that we are getting the Counter Timer pulses and the Ring Counter is functional as required for Refresh cycles.

Once the refresh Cycle is functional; we can expect the System Dynamic RAM Memory in the computer to be optional. This allows the testing of the System Memory to determine the total Memory Size. Once the Memory Size is obtained we display the value on the screen. The test for Memory Size involves reading the value of the first word of each segment, then writing the complement value out into memory, wait for the bus to discharge, then read the value back and compare the same.

The DMA Pass Registers are tested for I/O Operation for ports through 8F hex. We test to see if all bits are independent of the others at each port. Note that while we test the Page Register at port 80 hex, we are also displaying the test data on the port 80 hex display.

The DMA #1 and #2 are tested for I/O ports from 0 through 7 and C0 through CF hex. If the DMA's are found to support I/O to these ports then the "DMA 10" message is displayed on the Video screen. If the DMA is not found, then the "no DMA1" or no "DMA2" message is displayed.

An I/O test is done on port 61 hex which is "Port B". If this test is good, then the Diagnostic EPROM displays a "B" on the top right portion of the screen just to the right of the "T" for the Counter-Timer. After the Port B passes the I/O test it is setup for operation.

In general, the Diagnostic will output messages and error codes to prompt the operator of the conditions of the failure.

We can continue forward by setting up the Keyboard Interface Controller and the Interrupt Controller to get the keyboard operational.

The Interrupt Controllers are tested next. These Controllers have an I/O Supported mask register at port 21 & A1 hex. If writing and reading a rotating logic pattern across the data bus is functional at port 21h then the Diagnostic EPROM code displays an "I" to the right of the "B" on the top line of the Video Display. When the mask register at port A1 hex passes the I/O test an "I" is displayed under the first "I" to designate that the slave Interrupt Controller is functional.

The ROM code in the program then flushes the keyboard and displays the Menu of Diagnostic Tests for the continued analysis of the condition of the computer's functionality.

If the computer will not read a disk correctly, select the FDC Diagnostic which allows exercising of the Floppy Disk Controller circuitry. The FDC tests provided are enough to test the system in the 40 track FDC mode only (does not support the high capacity format) to isolate faults to the point of allowing floppy I/O.

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ROM Documentation

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The Initialization scheme for the Tandy 3000 diagnostic ROMs:

Diag Port output (Hex)	Operation, Test Description
	-Clear the Interrupts
1.	-Disable NMI (parity) at port 70h data bit D7
	-Output to the DOR Reg to hold FDC Chip Reset during power up
	and Select Floppy DRV #3 (deselect drives 0-2)
2.	-Check for Monochrome and/or Color Video Memory (B0000h, B8000h)
3.	-Init the Video & 6845 chips in 40 X 25 mode.
4.	-Clear the Video Ram, clear the screen on page 1 of Video memory
5.	-Check for valid Memory at the top of the Video Memory (for Stack)
8.	-Establish the Stack in the top of the Video Memory (known good
	Memory)
9.	-Check correct operation of the Counter/Timer I/O Port, ch 2 only
A.	-Setup the Counter/Timer on channel 1 to 15 usec "tics", for Refsh
D.	-Check if the Rfsh Det bit toggles data bit D4 port 6lh.
	-Find the Memory Size in the First 640K
	-Display the Memory Size on the Video Screen
10.	-Check out the DMA Page Reg I/O ports 80-8F hex
	-Check DMA I/O Operation & Initialize DMA Channel 0-7:
12.	-Check DMA #1 I/O
14.	-Check DMA #2 I/O
16.	-Init DMA #1
18.	-Init DMA #2
26.	-Test first 640k of System Memory using the CPU
30.	-Set-up NMI & Key Board Interrupt Vector
34.	-Test Port B (6lh) supports I/O on low nibble
36.	-Init Port B for parity at port 6lh (Base Memory only)
40.	-Now that Base Memory has been init, set up Base NMI parity
	-Reset 80287 Co-Processor & Configure as 80287 (Real Mode)
	-Set up the 8259 Int Controllers, mask reg I/O & mask all
42.	-Master Interrupt Controller
44.	-Slave Interrupt Controller
64-6D	-Self Test the Keyboard Controller & Initialize
80	-Check Floppy I/O during reset to check integrity
AD	-Display Main Diagnostic Menu

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VIDALGN

This program is an aid for aligning color video monitors. It uses the computer to generate dots and crosshatch patterns, color bars, and purity screens. The main menu is explained below.

## 1 Dots and Crosshatch

The <SPACE> bar will switch the screen between the two patterns. The <ESC> key returns the user to the main menu.

## 2 Color Bar Test

The <SPACE> bar shifts the pattern on the screen. The <ESC> key returns the user to the main menu.

## 3 Purity Test

The space bar changes the display color from red to blue to green. The <ESC> key returns the user to the main menu.

## Q Quit to DOS

Returns the user to the menu.

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VIDALGN

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DTA and DGA  
Deluxe Video Adapter tests

Two programs are used to test the two deluxe adapters. DTA is the deluxe text adapter (25-3046) test. DGA is the deluxe graphics adapter (25-3047) test. Both of these programs are fairly automatic. They will display test patterns on the screen & run tests on the video memory. Some of the test patterns will require hitting a key to continue, the prompt will appear on the screen. The memory tests may require pressing a key to stop them, this prompt will also appear on the screen.

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DGA-DTA  
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MONOVID-COLORVID

These two programs are for testing non-deluxe video boards. The MONOVID menu is shown below, the COLORVID menu is similar. Control C will exit the programs.

C Clear Video Screen  
Blacks out the display

F Fill Video Screen  
Whites out the display

A Alpha/Numeric display  
Fills the screen with the Alpha/numeric character set

S Special Characters display  
Fills the screen with the Special character set

M Video Memory Test  
Runs a quick memory test on the video memory

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MONOVID-COLORVID

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CMOSTEST

This test allows the user to: display & edit the CMOS RAM data, run a memory test on the CMOS RAM, set the default configuration for a floppy drive system, and set the default for a hard drive system. The main menu is described below.

## 1. Display and edit RAM

Allows the user to edit the configuration data in the CMOS RAM. Once in this option, press the keys indicated at the bottom of the screen to edit the desired data.

## 2. Test the static RAM

Runs a memory test on the static RAM, then displays the time from the clock as a clock test.

## 3. Default for a Desktop unit

Sets the CMOS RAM data for a 25-4001 default configuration (1 high capacity floppy drive, no hard disk)

## 4. Default for a unit with hard disk

Sets the CMOS RAM data for a 25-4010 default configuration (1 high capacity floppy drive, 1 20 Meg hard disk)

Once in an option pressing <q> will exit the program. There is no way back to the main menu, other than rerunning the program.

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CMOSTEST

Page 1

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KBTEST

KBTEST tests both the keyboard controller in the TANDY 3000 main unit and the processor in the keyboard unit. The program will come up with the following menu.

1. Keyboard controller self test  
Tests the keyboard controller in the main unit
2. Keyboard interface test  
Tests the interface between the main unit keyboard controller and the keyboard units processor.
3. Keyboard controller diagnostic dump (DO NOT USE)  
This function is not implemented.
4. Keyboard scan code tests (PC codes)  
Displays the code for the keys pressed on the keyboard, PC style.
5. Keyboard scan code tests (AT codes)  
Displays the code for the keys pressed on the keyboard, AT style.
6. Keyboard scan code tests (PC keyboard -- DO NOT USE)  
The user will not be able to return to the menu.
7. Exit tests  
Reboots the computer.

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NUMPROC

This program does a quick test of the 80287 numeric co-processor. It will first test for the presence of the processor and indicate if it is present or not. It will then print out a value of pi (+314159265358979324e-17) generated by the coprocessor. Then a value for the square root of 2 (+141421356237309505e-17). After these two calculations, it will test the interrupts. Once the program has been started, no user action is required.

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## DIAGNOSTIC ROM BOARD

The following is a description of the diagnostic port and ROM card.

The first feature of the card is a port mapped hex LED display. These two digits show the last byte written to port address 80H. This is because the 80286 boot ROMs output to port 80H at various times during their power-on startup. By looking at the number displayed when the machine "hangs up" it can be determined where in the boot code the program ran into trouble. This is very convenient when servicing a machine that can't get far enough into the startup routines that it could display error messages on the CRT.

A second feature is the availability of two sockets for ROMs. Each socket will support a 256K bit EPROM or ROM. Available mapping options for the ROMs are base addresses of C8000H, D0000H, D8000H, E0000H, and E8000H. These address options are selected by a jumper on the board. Software written for ROMs must follow the IBM convention for format, that is:

- Relative Byte 0 - 55H
- Relative Byte 1 - AAH
- Relative Byte 2 - The number of 512 byte blocks used in that portion of the ROM.
- Relative Byte 3 - Entry by far call to your ROM routine for power-on installation into the system. Exit back to the DOS by a FAR RETURN.

Separate modules can be written in one ROM but they must start on 2K boundaries as if they were separate ROMs.

The sum (modulo 100H) of all bytes in a defined portion must be 00H.

This board was designed for an 8 bit world. As a result it can be used in the Tandy 1000, 1200, and 3000 series machines. When used in an 80286 machine, it only uses the 8 bit bus. The diagnostic port (80H) is not a supported feature of the boot ROMs in the 1000 and 1200 machines, but there is no reason why the board could not be used as just a ROM board. The display will give meaningless information unless software is written for the board. Software developers could use the board for debugging their products in any "IBM" bus machine.



### Theory of design - Display port

After the bus buffering, U5 and U6 decode port 80H. As per IBM convention, this is only decoded modulo 400H. I/O write is part of the decode to the 138. On release of I/O write, the latch enable of the 9370 will lock the data on the data bus internally and decode it for the 7 segment LED displays. The 9370 is very similar to a 7447, except that the 9370 is a full hexadecimal decoder driver. It handles 0-9 and A-F instead of the cryptic results the 7447 gives for 0AH and above.

### Theory of design - On-Board ROM

ROM support is provided in two sockets, each supporting a 256K bit EPROM or ROM. The 138 (U10) is used to decode various address ranges from C0000H thru FFFFFH. Of these, only those with bases from C8000H thru E8000H are jumper selectable. This is to prevent a conflict with other internal options. The select signal from the 138 is not qualified with MEMR (memory read). Since memory read follows the addresses, the decode is provided to the ROM first and MEMR is used as the output gate signal. This allows a slower speed ROM to be used than is normally the case. In addition, the decode is wired "or"ed, qualified with MEMR, and finally routed to change direction of bus buffer U1. By qualifying with MEMR from the 8 bit bus any conflicts with a high memory memory device that images the lower 20 bits of the ROM address is eliminated.

The array for the memory address select is as pictured below. The sockets U3 and U4 each are designed for TMS27256 EPROMs. Column 1 is U3. Row A is address C8000 through CFFFF, Row B is address select D0000 through D7FFF, etc., as in the table. For example, to make an EPROM in socket U4 appear starting at address D8000, the jumper should be connected form C2 to C1. If a ROM or EPROM smaller than 256K is installed, there may be addressing problems. Also, ROMs smaller than 256K, even if the board is modified to address them correctly, will appear at multiple locations within the 256K range shown in the table.

	1	2	3	Address Range
A	o	o	o	A - C8000-CFFFF
B	o	o	o	B - D0000-D7FFF
C	o	o	o	C - D8000-DFFFF
D	o	o	o	D - E0000-E7FFF
E	o	o	o	E - E8000-EFFFF



### Additional Features

As an additional feature, there is a hardware 'patch' area, consisting of room for 6 dip chips of 20 pins or less. No power or ground traces are provided, any circuits have to be totally user wired. In addition, there are holes to mount a 50 pin header connector at the edge of the circuit board.



TANDY 3000 Diagnostic ROM Bd. Subassembly

Symbol	Description	Part No.
	Tandy 3000 Diagnostic Rom Bd. Subassembly	TS-985
	Diagnostic ROM Pcb. (T3000)	8709678
	Staking Pin	8529014
	Jumper Plug	8519098
	Bag, Antistatic	8590053
	Box, Individual Shipping	8769114
	Instruction Sheet (3 pages)	
C1-10	Capacitor .1 UP 50V +80/-20% Mono Ax.	8374104
RPl,2	Resistor Pack 470 Ohm 8R 16-Pin DIP	8290060
U1,2	LED - 7 Segment Common Anode	
U3,4	Socket 28-Pin DIP	8509007
U5,10	IC 74LS138	8020138
U6	IC 74LS260	8020260
U7,8	IC 9370	8040370
U9	IC 74ALS00	8025000
U11-13	IC 74ALS244	8025244
U14	IC 74ALS245	8025245



Version 2 of the Tandy 3000

Version 2 of the Tandy 3000 is very similar to Version 1. The main differences are on the Main Logic Board which has been relayed out with parts changes. These changes are reflected in the Timing Diagram, Schematic, PCB Art and Parts List which follow. All other information is the same for both versions of the Tandy 3000.



Tandy 3000 Main Logic Sub Assembly

Symbol	Description	Part No.
	Tandy 3000 Subassembly	8898952B
C1,2,5,6	Capacitor 47 PF 50V RAD	8300474
C3,63	Capacitor 0.01 UF 50V Mono Ax.	8373104
C1A,2A,4,14-17, 25-28,31,34, 36A,37-41,40A, 40B,41A,43-51, 56,58-62	Capacitor 0.1 UF 50V Mono Ax.	8374104
C7,8	Capacitor 100 PF 50V Mono Ax.	8371104
C9,24,35,36, 42,53,57,64, 101-122,124, 126, 128	Capacitor 10 UF 16V Elect. Rad.	8326101
C18,19	Capacitor 10 PF 50V Rad.	8300104
C20	Capacitor Variable 6-70 PF	8360607
C21	Capacitor 56 PF 50V Rad.	8300565
C22	Capacitor 6-70 PF	8360607
C23,52,54,55	Capacitor 0.047 UF 50V Mono Ax.	8373484
C29	Capacitor 27 PF 50V Rad.	8300273
C30	Capacitor 0.0047 UF 50V Mono Ax.	8372474
C32	Capacitor 0.001 UF 50V Ax.	8302104
C65-100	Capacitor 0.33 UF Mono Ax.	8374334
CR1-4	Diode IN4148	8150148
E1-3,7-18	Staking Pin	8529014
E4,5	Switch, 1 Pos. DIP (Observe Polarity)	8489089
FB1-3	Ferrite Bead	8419013
J1-10	Connector, 62PB	8519236
J12-17,19	Connector, 36PB	8519258
J22	Connector, 8-Pin Keybd.	8519203
J23	Connector, 12-Pin Mate-N-Lock	8519259
J24,25	Connector, 4-Pin Header	8519210
J26	Connector, 5-Pin Header	8519260
Q1	Transistor 2N3906	8100906
Q2	Transistor 2N3904	8110904

Symbol	Description	Part No.
R1,2,16,17,21, 27-31,35-37, 39,39A,40, 42-44,50,51A, 52-57	Resistor 10K Ohm 1/4 Watt 5%	8207310
R9	Resistor 4.7K Ohm 1/4 Watt 5%	8207247
R10-12,18	Resistor 300 Ohm 1/4 Watt 5%	8207130
R13,32,41	Resistor 1K Ohm 1/4 Watt 5%	8207210
R14,15	Resistor 470 Ohm 1/4 Watt 5%	8207147
R19,20,34,58,59	Resistor 33 Ohm 1/4 Watt 5%	8207033
R22	Resistor 10 Ohm 1/4 Watt 5%	8207010
R23,24	Resistor 1 Meg Ohm 1/4 Watt 5%	8207510
R25	Resistor 330 Ohm 1/4 Watt 5%	8207133
R26	Resistor 47 Ohm 1/4 Watt 5%	8207047
R33	Resistor 2 Meg Ohm 1/4 Watt 5%	8207520
R38	Resistor 51K Ohm 1/4 Watt 5%	8207351
R51	Resistor 910 Ohm 1/4 Watt 5%	8207191
R60	Resistor 150 Ohm 1/4 Watt 5%	8207115
R61	Resistor 2.2K Ohm 1/4W 5%	8207222
RP2,3	Resistor Pak 10K Ohm 10-Pin SIP	8290010
RP4,5	Resistor Pak 33 Ohm 16-Pin DIP	8290044
U2	IC 8042	8070142
U3	IC 7407	8000007
U4,25	IC 74F04	8015004
U5	IC 74F74	8015074
U6	IC 74ALS244	8025244
U7	IC 74ALS245	8025245
U8	IC 82C201	8075201
U9,12	IC 8259A	8040259
U10	IC 74LS00	8025000
U11	IC 74LS125A	8020125
U13	IC 146818	8046818
U14	IC 14069	8030069
U15,17	IC 8237A-5 (Except AMD)	8040237
U16	IC 8254-2	8040254
U18,20	IC 74ALS573	8025573
U19	IC 74ALS138	8025138
U21	IC PE21213 Delay Line 200 NS	8429010
U22	IC 82A205	8075205
U23	IC 82A203	8075203
U24	IC 74LS612	8020612

Symbol	Description	Part No.
U26,29,31	IC 74F10	8015010
U27,30	IC 74F08	8015008
U28	IC 82C202	8075202
U33	IC 80286-8	8040286
U34	IC 74F27	8015027
U35	IC 74ALS32	8025032
U36	IC 82A204	8075204
U37	IC 74F153	8015153
U38	IC 75477	8040477
U40,42	IC 27128 EPROM 200 NS	8047128
U61-78	IC 256K Dram 150 NS	8049008
U2,15,17,32	Socket 40-Pin DIP	8509002
U8	Socket 84-Pin, JADEC "C"	8509031
U9,12,39-42	Socket 28-Pin DIP	8509007
U16	Socket 24-Pin DIP	8509001
U22,23,36	Socket 68-Pin, JADEC "C"	8509020
U28	Socket 48-Pin DIP	8509032
U33	Socket 68-Pin, JADEC "A"	8509017
U43-78	Socket 16-Pin DIP	8509003
Y1	Crystal 16 MHZ	8409050
Y2	Crystal 14.318 MHZ	8409048
Y3	Crystal 32.768 KHZ	8409033
4	Cable - Multi-user Opt.Bd.	
1	Clamp - Mounting	
1	Panel - Mounting	



## iAPX 286/10 High Performance Microprocessor with Memory Management and Protection

(80286-12, 80286-10, 80286-8, 80286-6)

- High Performance Processor (Up to six times iAPX 86)
- Large Address Space:
  - 16 Megabytes Physical
  - 1 Gigabyte Virtual per Task
- Integrated Memory Management, Four-Level Memory Protection and Support for Virtual Memory and Operating Systems
- Two iAPX 86 Upward Compatible Operating Modes:
  - iAPX 86 Real Address Mode
  - Protected Virtual Address Mode
- Optional Processor Extension:
  - 80287 High Performance 80-bit Numeric Data Processor
- Range of clock rates
  - 12.5 MHz for 80286-12
  - 10 MHz for 80286-10
  - 8 MHz for 80286-8
  - 6 MHz for 80286-6
- Complete System Development Support:
  - Development Software: Assembler, PL/M, Pascal, FORTRAN, and System Utilities
  - In-Circuit-Emulator (ICE™-286)
- High Bandwidth Bus Interface (12.5 Megabyte/Sec)
- Available in EXPRESS:
  - Standard Temperature Range

The iAPX 286/10 (80286 part number) is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multi-tasking systems. The 80286 has built-in memory protection that supports operating system and task isolation as well as program and data privacy within tasks. A 12.5 MHz iAPX 286/10 provides six times or more throughput than the standard 5 MHz iAPX 86/10. The 80286 includes memory management capabilities that map  $2^{30}$  (one gigabyte) of virtual address space per task into  $2^{24}$  bytes (16 megabytes) of physical memory.

The iAPX 286 is upward compatible with iAPX 86 and 88 software. Using iAPX 86 real address mode, the 80286 is object code compatible with existing iAPX 86, 88 software. In protected virtual address mode, the 80286 is source code compatible with iAPX 86, 88 software and may require upgrading to use virtual addresses supported by the 80286's integrated memory management and protection mechanism. Both modes operate at full 80286 performance and execute a superset of the iAPX 86 and 88 instructions.

The 80286 provides special operations to support the efficient implementation and execution of operating systems. For example, one instruction can end execution of one task, save its state, switch to a new task, load its state, and start execution of the new task. The 80286 also supports virtual memory systems by providing a segment-not-present exception and restartable instructions.

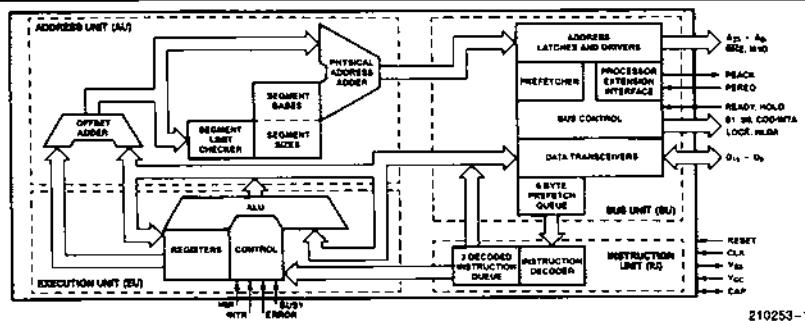


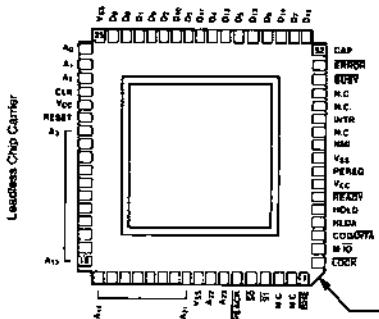
Figure 1. 80286 Internal Block Diagram

210253-1

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Order Number: 210253-008

**Component Pad Views**—As viewed from underside of component when mounted on the board.



**P.C. Board Views**—As viewed from the component side of the P.C. board.

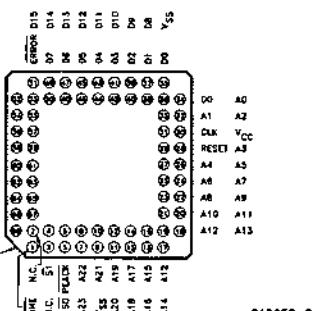
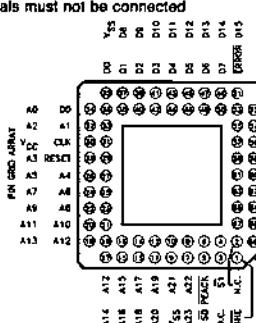
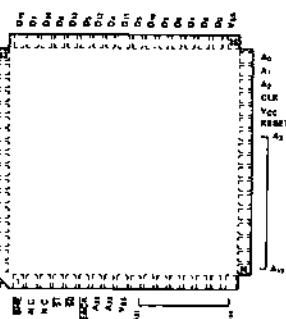


FIGURE 2. 80286 Pin Configuration

Table 1. Pin Description

The following pin function descriptions are for the 80286 microprocessor:

Symbol	Type	Name and Function															
CLK	I	<b>SYSTEM CLOCK</b> provides the fundamental timing for IAPX 286 systems. It is divided by two inside the 80286 to generate the processor clock. The internal divide-by-two circuitry can be synchronized to an external clock generator by a LOW to HIGH transition on the RESET input.															
D <sub>15</sub> -D <sub>0</sub>	I/O	<b>DATA BUS</b> inputs data during memory, I/O, and interrupt acknowledge read cycles; outputs data during memory and I/O write cycles. The data bus is active HIGH and floats to 3-state OFF during bus hold acknowledgement.															
A <sub>23</sub> -A <sub>0</sub>	O	<b>ADDRESS BUS</b> outputs physical memory and I/O port addresses. A <sub>0</sub> is LOW when data is to be transferred on pins D <sub>7</sub> -0. A <sub>23</sub> -A <sub>18</sub> are LOW during I/O transfers. The address bus is active HIGH and floats to 3-state OFF during bus hold acknowledgement.															
BHE	O	<b>BUS HIGH ENABLE</b> indicates transfer or data on the upper byte of the data bus. D <sub>15</sub> -8. Eight-bit oriented devices assigned to the upper byte of the data bus would normally use BHE to condition chip select functions. BHE is active LOW and floats to 3-state OFF during bus hold acknowledgement.															
		<b>BHE and A<sub>0</sub> Encodings</b>															
		<table border="1"> <thead> <tr> <th>BHE Value</th> <th>A<sub>0</sub> Value</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Word transfer</td> </tr> <tr> <td>0</td> <td>1</td> <td>Byte transfer on upper half of data bus (D<sub>15</sub>-D<sub>8</sub>)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Byte transfer on lower half of data bus (D<sub>7</sub>-0)</td> </tr> <tr> <td>1</td> <td>1</td> <td>Reserved</td> </tr> </tbody> </table>	BHE Value	A <sub>0</sub> Value	Function	0	0	Word transfer	0	1	Byte transfer on upper half of data bus (D <sub>15</sub> -D <sub>8</sub> )	1	0	Byte transfer on lower half of data bus (D <sub>7</sub> -0)	1	1	Reserved
BHE Value	A <sub>0</sub> Value	Function															
0	0	Word transfer															
0	1	Byte transfer on upper half of data bus (D <sub>15</sub> -D <sub>8</sub> )															
1	0	Byte transfer on lower half of data bus (D <sub>7</sub> -0)															
1	1	Reserved															

Table I. Pin Description (Cont.)

Symbol	Type	Name and Function					
S1, S0	O	<b>BUS CYCLE STATUS</b> indicates initiation of a bus cycle and, along with M/I <sup>O</sup> and COD/INTA, defines the type of bus cycle. The bus is in a T <sub>1</sub> state whenever one or both are LOW. S1 and S0 are active LOW and float to 3-state OFF during bus hold acknowledge.					
<b>80286 Bus Cycle Status Definition</b>							
COD/INTA	M/I <sup>O</sup>	S1	S0	<b>Bus Cycle Initiated</b>			
0 (LOW)	0	0	0	Interrupt acknowledge			
0	0	0	1	Will not occur			
0	0	1	0	Will not occur			
0	0	1	1	None; not a status cycle			
0	1	0	0	IF A1 = 1 then halt; else shutdown			
0	1	0	1	Memory data read			
0	1	1	0	Memory data write			
0	1	1	1	None; not a status cycle			
1 (HIGH)	0	0	0	Will not occur			
1	0	0	1	I/O read			
1	0	1	0	I/O write			
1	0	1	1	None; not a status cycle			
1	1	0	0	Will not occur			
1	1	0	1	Memory instruction read			
1	1	1	0	Will not occur			
1	1	1	1	None; not a status cycle			
M/I <sup>O</sup>	O	<b>MEMORY I/O SELECT</b> distinguishes memory access from I/O access. If HIGH during T <sub>0</sub> , a memory cycle or a halt/shutdown cycle is in progress. If LOW, an I/O cycle or an interrupt/acknowledge cycle is in progress. M/I <sup>O</sup> floats to 3-state OFF during bus hold acknowledge.					
COD/INTA	O	<b>CODE/INTERRUPT ACKNOWLEDGE</b> distinguishes instruction fetch cycles from memory data read cycles. Also distinguishes interrupt acknowledge cycles from I/O cycles. COD/INTA floats to 3-state OFF during bus hold acknowledge. Its timing is the same as M/I <sup>O</sup> .					
LOCK	O	<b>LOCK</b> indicates that other system bus masters are not to gain control of the system bus following the current bus cycle. The LOCK signal may be activated explicitly by the "LOCK" instruction prefix or automatically by 80286 hardware during memory XCHG instructions, interrupt acknowledge, or descriptor table access. LOCK is active LOW and floats to 3-state OFF during bus hold acknowledge.					
READY	I	<b>BUS READY</b> terminates a bus cycle. Bus cycles are extended without limit until terminated by READY LOW. READY is an active LOW synchronous input requiring setup and hold times relative to the system clock to be met for correct operation. READY is ignored during bus hold acknowledge.					
HOLD HLDA	I O	<b>BUS HOLD REQUEST AND HOLD ACKNOWLEDGE</b> control ownership of the 80286 local bus. The HOLD input allows another local bus master to request control of the local bus. When control is granted, the 80286 will float its bus drivers to 3-state OFF and then activate HLDA, thus entering the bus hold acknowledge condition. The local bus will remain granted to the requesting master until HOLD becomes inactive which results in the 80286 deactivating HLDA and regaining control of the local bus. This terminates the bus hold acknowledge condition. HOLD may be asynchronous to the system clock. These signals are active HIGH.					
INTR	I	<b>INTERRUPT REQUEST</b> requests the 80286 to suspend its current program execution and service a pending external request. Interrupt requests are masked whenever the interrupt enable bit in the flag word is cleared. When the 80286 responds to an interrupt request, it performs two interrupt acknowledge bus cycles to read an 8-bit interrupt vector that identifies the source of the interrupt. To assure program interruption, INTR must remain active until the first interrupt acknowledge cycle is completed. INTR is sampled at the beginning of each processor cycle and must be active HIGH at least two processor cycles before the current instruction ends in order to interrupt before the next instruction. INTR is level sensitive, active HIGH, and may be asynchronous to the system clock.					
NMI	I	<b>NON-MASKABLE INTERRUPT REQUEST</b> interrupts the 80286 with an internally supplied vector value of 2. No interrupt acknowledge cycles are performed. The interrupt enable bit in the 80286 flag word does not affect this input. The NMI input is active HIGH, may be asynchronous to the system clock, and is edge triggered after internal synchronization. For proper recognition, the input must have been previously LOW for at least four system clock cycles and remain HIGH for at least four system clock cycles.					

Table 1. Pin Description (Cont.)

Symbol	Type	Name and Function						
PREQ PEACK	I O	<b>PROCESSOR EXTENSION OPERAND REQUEST AND ACKNOWLEDGE</b> extend the memory management and protection capabilities of the 80286 to processor extensions. The PREQ input requests the 80286 to perform a data operand transfer for a processor extension. The PEACK output signals the processor extension when the requested operand is being transferred. PREQ is active HIGH and floats to 3-state OFF during bus hold acknowledge. PEACK may be asynchronous to the system clock. PEACK is active LOW.						
BUSY ERROR	I I	<b>PROCESSOR EXTENSION BUSY AND ERROR</b> indicate the operating condition of a processor extension to the 80286. An active BUSY input stops 80286 program execution on WAIT and some ESC instructions until BUSY becomes inactive (HIGH). The 80286 may be interrupted while waiting for BUSY to become inactive. An active ERROR input causes the 80286 to perform a processor extension interrupt when executing WAIT or some ESC instructions. These inputs are active LOW and may be asynchronous to the system clock.						
RESET	I	<p><b>SYSTEM RESET</b> clears the internal logic of the 80286 and is active HIGH. The 80286 may be reinitialized at any time with a LOW to HIGH transition on RESET which remains active for more than 16 system clock cycles. During RESET active, the output pins of the 80286 enter the state shown below:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="2">80286 Pin State During Reset</th> </tr> <tr> <th>Pin Value</th> <th>Pin Names</th> </tr> </thead> <tbody> <tr> <td>1 (HIGH) 0 (LOW) 3-state OFF</td> <td>S0, S1, PEACK, A23-A0, BHE, LOCK M/I/O, COD/INTA, HLDA D<sub>15</sub>-D<sub>0</sub></td> </tr> </tbody> </table> <p>Operation of the 80286 begins after a HIGH to LOW transition on RESET. The HIGH to LOW transition of RESET must be synchronous to the system clock. Approximately 50 system clock cycles are required by the 80286 for internal initializations before the first bus cycle to fetch code from the power-on execution address is performed. A LOW to HIGH transition of RESET synchronous to the system clock will end a processor cycle at the second HIGH to LOW transition of the system clock. The LOW to HIGH transition of RESET may be asynchronous to the system clock; however, in this case it cannot be predetermined which phase of the processor clock will occur during the next system clock period. Synchronous LOW to HIGH transitions of RESET are required only for systems where the processor clock must be phase synchronous to another clock.</p>	80286 Pin State During Reset		Pin Value	Pin Names	1 (HIGH) 0 (LOW) 3-state OFF	S0, S1, PEACK, A23-A0, BHE, LOCK M/I/O, COD/INTA, HLDA D <sub>15</sub> -D <sub>0</sub>
80286 Pin State During Reset								
Pin Value	Pin Names							
1 (HIGH) 0 (LOW) 3-state OFF	S0, S1, PEACK, A23-A0, BHE, LOCK M/I/O, COD/INTA, HLDA D <sub>15</sub> -D <sub>0</sub>							
V <sub>SS</sub>	I	<b>SYSTEM GROUND:</b> 0 Volts.						
V <sub>CC</sub>	I	<b>SYSTEM POWER:</b> +5 Volt Power Supply.						
CAP	I	<b>SUBSTRATE FILTER CAPACITOR:</b> a 0.047 $\mu$ F $\pm$ 20% 12V capacitor must be connected between this pin and ground. This capacitor filters the output of the internal substrate bias generator. A maximum DC leakage current of 1 $\mu$ A is allowed through the capacitor. For correct operation of the 80286, the substrate bias generator must charge this capacitor to its operating voltage. The capacitor chargeup time is 5 milliseconds (max.) after V <sub>CC</sub> and CLK reach their specified AC and DC parameters. RESET may be applied to prevent spurious activity by the CPU during this time. After this time, the 80286 processor clock can be synchronized to another clock by pulsing RESET LOW synchronous to the system clock.						

## FUNCTIONAL DESCRIPTION

### Introduction

The 80286 is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multi-tasking systems. Depending on the application, the 80286's performance is up to six times faster than the standard 5 MHz 8086's, while providing complete upward software compatibility with Intel's iAPX 86, 88, and 186 family of CPU's.

The 80286 operates in two modes: iAPX 86 real address mode and protected virtual address mode. Both modes execute a superset of the iAPX 86 and 88 instruction set.

In iAPX 86 real address mode programs use real addresses with up to one megabyte of address space. Programs use virtual addresses in protected virtual address mode, also called protected mode. In protected mode, the 80286 CPU automatically maps 1 gigabyte of virtual addresses per task into a 16 megabyte real address space. This mode also provides memory protection to isolate the operating system and ensure privacy of each tasks' programs and data. Both modes provide the same base instruction set, registers, and addressing modes.

The following Functional Description describes first, the base 80286 architecture common to both modes, second, iAPX 86 real address mode, and third, protected mode.

## iAPX 286/10 BASE ARCHITECTURE

The iAPX 86, 88, 186, and 286 CPU family all con-

tain the same basic set of registers, instructions, and addressing modes. The 80286 processor is upward compatible with the 8086, 8088, and 80186 CPU's.

### Register Set

The 80286 base architecture has fifteen registers as shown in Figure 3. These registers are grouped into the following four categories:

**General Registers:** Eight 16-bit general purpose registers used to contain arithmetic and logical operands. Four of these (AX, BX, CX, and DX) can be used either in their entirety as 16-bit words or split into pairs of separate 8-bit registers.

**Segment Registers:** Four 16-bit special purpose registers select, at any given time, the segments of memory that are immediately addressable for code, stack, and data. (For usage, refer to Memory Organization.)

**Base and Index Registers:** Four of the general purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode determines the specific registers used for operand address calculations.

**Status and Control Registers:** The 3 16-bit special purpose registers in figure 3A record or control certain aspects of the 80286 processor state including the Instruction Pointer, which contains the offset address of the next sequential instruction to be executed.

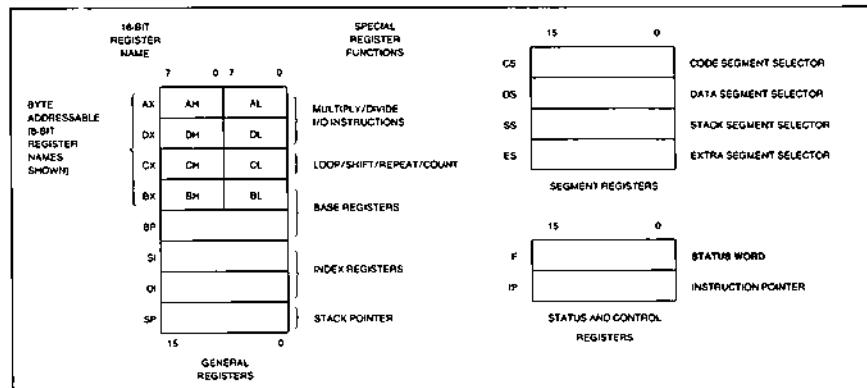


Figure 3. Register Set

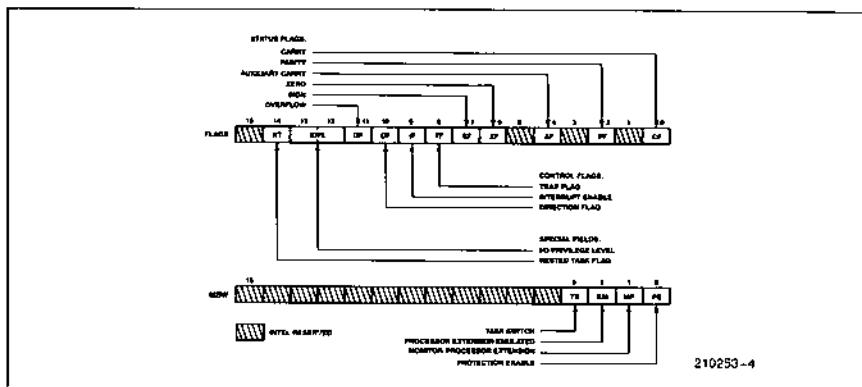


Figure 3a. Status and Control Register Bit Functions

### Flags Word Description

The Flags word (Flags) records specific characteristics of the result of logical and arithmetic instructions (bits 0, 2, 4, 6, 7, and 11) and controls the operation of the 80286 within a given operating mode (bits 8 and 9). Flags is a 16-bit register. The function of the flag bits is given in Table 2.

### Instruction Set

The instruction set is divided into seven categories: data transfer, arithmetic, shift/rotate/logical, string manipulation, control transfer, high level instructions, and processor control. These categories are summarized in Figure 4.

An 80286 instruction can reference zero, one, or two operands; where an operand resides in a register, in the instruction itself, or in memory. Zero-operand instructions (e.g. NOP and HLT) are usually one byte long. One-operand instructions (e.g. INC and DEC) are usually two bytes long but some are encoded in only one byte. One-operand instructions may reference a register or memory location. Two-operand instructions permit the following six types of instruction operations:

- Register to Register
- Memory to Register
- Immediate to Register
- Memory to Memory
- Register to Memory
- Immediate to Memory

Table 2. Flags Word Bit Functions

Bit Position	Name	Function
0	CF	Carry Flag—Set on high-order bit carry or borrow; cleared otherwise
2	PF	Parity Flag—Set if low-order 8 bits of result contain an even number of 1-bits; cleared otherwise
4	AF	Set on carry from or borrow to the low order four bits of AL; cleared otherwise
6	ZF	Zero Flag—Set if result is zero; cleared otherwise
7	SF	Sign Flag—Set equal to high-order bit of result (0 if positive, 1 if negative)
11	OF	Overflow Flag—Set if result is a too-large positive number or a too-small negative number (excluding sign-bit) to fit in destination operand; cleared otherwise
8	TF	Single Step Flag—Once set, a single step interrupt occurs after the next instruction executes. TF is cleared by the single step interrupt.
9	IF	Interrupt-enable Flag—When set, maskable interrupts will cause the CPU to transfer control to an interrupt vector specified location.
10	DF	Direction Flag—Causes string instructions to auto-decrement the appropriate index registers when set. Clearing DF causes auto increment.

Two-operand instructions (e.g. MOV and ADD) are usually three to six bytes long. Memory to memory operations are provided by a special class of string instructions requiring one to three bytes. For detailed instruction formats and encodings refer to the instruction set summary at the end of this document.

For detailed operation and usage of each instruction, see Appendix of iAPX 286 Programmer's Reference Manual (Order No. 210498)

GENERAL PURPOSE	
MOV	Move byte or word
PUSH	Push word onto stack
POP	Pop word off stack
PUSHA	Push all registers on stack
POPA	Pop all registers from stack
XCHG	Exchange byte or word
XLAT	Translate byte
INPUT/OUTPUT	
IN	Input byte or word
OUT	Output byte or word
ADDRESS OBJECT	
LEA	Load effective address
LDS	Load pointer using DS
LES	Load pointer using ES
FLAG TRANSFER	
LAHF	Load AH register from flags
SAHF	Store AH register in flags
PUSHF	Push flags onto stack
POPF	Pop flags off stack

Figure 4a. Data Transfer Instructions

MOVS	Move byte or word string
INS	Input bytes or word string
OUTS	Output bytes or word string
CMP\$	Compare byte or word string
SCAS	Scan byte or word string
LODS	Load byte or word string
STOS	Store byte or word string
REP	Repeat
REPE/REPZ	Repeat while equal/zero
REPNE/REPNZ	Repeat while not equal/not zero

Figure 4c. String Instructions

ADDITION	
ADD	Add byte or word
ADC	Add byte or word with carry
INC	Increment byte or word by 1
AAA	ASCII adjust for addition
DAA	Decimal adjust for addition
SUBTRACTION	
SUB	Subtract byte or word
SBB	Subtract byte or word with borrow
DEC	Decrement byte or word by 1
NEG	Negate byte or word
CMP	Compare byte or word
AAS	ASCII adjust for subtraction
DAS	Decimal adjust for subtraction
MULTIPLICATION	
MUL	Multiple byte or word unsigned
IMUL	Integer multiply byte or word
AAM	ASCII adjust for multiply
DIVISION	
DIV	Divide byte or word unsigned
IDIV	Integer divide byte or word
AAD	ASCII adjust for division
CBW	Convert byte to word
CWD	Convert word to doubleword

Figure 4b. Arithmetic Instructions

LOGICALS	
NOT	"Not" byte or word
AND	"And" byte or word
OR	"Inclusive or" byte or word
XOR	"Exclusive or" byte or word
TEST	"Test" byte or word
SHIFTS	
SHL/SAL	Shift logical/arithmetic left byte or word
SHR	Shift logical right byte or word
SAR	Shift arithmetic right byte or word
ROTATES	
ROL	Rotate left byte or word
ROR	Rotate right byte or word
RCL	Rotate through carry left byte or word
RCR	Rotate through carry right byte or word

Figure 4d. Shift/Rotate Logical Instructions

CONDITIONAL TRANSFERS		UNCONDITIONAL TRANSFERS	
JA/JNBE	Jump if above/not below nor equal	CALL	Call procedure
JAE/JNS	Jump if above or equal/not below	RET	Return from procedure
JB/JNAE	Jump if below/not above nor equal	JMP	Jump
JBE/JNA	Jump if below or equal/not above		
JC	Jump if carry	ITERATION CONTROLS	
JE/JZ	Jump if equal/zero	LOOP	Loop
JG/JNLE	Jump if greater/not less nor equal	LOOPE/LOOPZ	Loop if equal/zero
JGE/JNL	Jump if greater or equal/not less	LOOPNE/LOOPNZ	Loop if not equal/not zero
JL/JNGE	Jump if less/not greater nor equal	JCXZ	Jump if register CX = 0
JLE/JNG	Jump if less or equal/not greater		
JNC	Jump if not carry	INTERRUPTS	
JNE/JNZ	Jump if not equal/not zero	INT	Interrupt
JNO	Jump if not overflow	INTO	Interrupt if overflow
JNP/JPO	Jump if not parity/parity odd	IRET	Interrupt return
JNS	Jump if not sign		
JO	Jump if overflow		
JP/JPE	Jump if parity/parity even		
JS	Jump if sign		

Figure 4e. Program Transfer Instructions

FLAG OPERATIONS	
STC	Set carry flag
CLC	Clear carry flag
CMC	Complement carry flag
STD	Set direction flag
CLD	Clear direction flag
STI	Set interrupt enable flag
CLI	Clear interrupt enable flag
EXTERNAL SYNCHRONIZATION	
HLT	Halt until interrupt or reset
WAIT	Wait for BUSY not active
ESC	Escape to extension processor
LOCK	Lock bus during next instruction
NO OPERATION	
NOP	No operation
EXECUTION ENVIRONMENT CONTROL	
LMSW	Load machine status word
SMSW	Store machine status word

Figure 4f. Processor Control Instructions

ENTER	Format stack for procedure entry
LEAVE	Restore stack for procedure exit
BOUND	Deflects values outside prescribed range

Figure 4g. High Level Instructions

## Memory Organization

Memory is organized as sets of variable length segments. Each segment is a linear contiguous sequence of up to 64K (2<sup>16</sup>) 8-bit bytes. Memory is addressed using a two component address (a pointer) that consists of a 16-bit segment selector, and a 16-bit offset. The segment selector indicates the desired segment in memory. The offset component indicates the desired byte address within the segment.

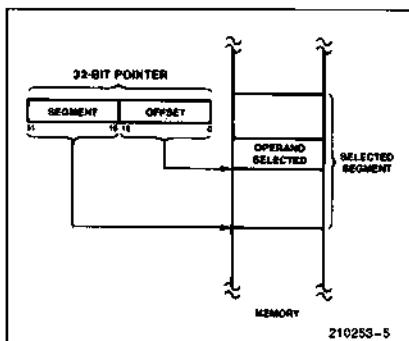


Figure 5. Two Component Address



Table 3. Segment Register Selection Rules

Memory Reference Needed	Segment Register Used	Implicit Segment Selection Rule
Instructions	Code (CS)	Automatic with instruction prefetch
Stack	Stack (SS)	All stack pushes and pops. Any memory reference which uses BP as a base register.
Local Data	Data (DS)	All data references except when relative to stack or string destination
External (Global) Data	Extra (ES)	Alternate data segment and destination of string operation

All instructions that address operands in memory must specify the segment and the offset. For speed and compact instruction encoding, segment selectors are usually stored in the high speed segment registers. An instruction need specify only the desired segment register and an offset in order to address a memory operand.

Most instructions need not explicitly specify which segment register is used. The correct segment register is automatically chosen according to the rules of Table 3. These rules follow the way programs are written (see Figure 6) as independent modules that require areas for code and data, a stack, and access to external data areas.

Special segment override instruction prefixes allow the implicit segment register selection rules to be overridden for special cases. The stack, data, and extra segments may coincide for simple programs. To access operands not residing in one of the four immediately available segments, a full 32-bit pointer or a new segment selector must be loaded.

## Addressing Modes

The 80286 provides a total of eight addressing modes for instructions to specify operands. Two addressing modes are provided for instructions that operate on register or immediate operands:

**Register Operand Mode:** The operand is located in one of the 8 or 16-bit general registers.

**Immediate Operand Mode:** The operand is included in the instruction.

Six modes are provided to specify the location of an operand in a memory segment. A memory operand address consists of two 16-bit components: segment selector and offset. The segment selector is supplied by a segment register either implicitly chosen by the addressing mode or explicitly chosen by a segment override prefix. The offset is calculated by summing any combination of the following three address elements:

the **displacement** (an 8 or 16-bit immediate value contained in the instruction)

the **base** (contents of either the BX or BP base registers)

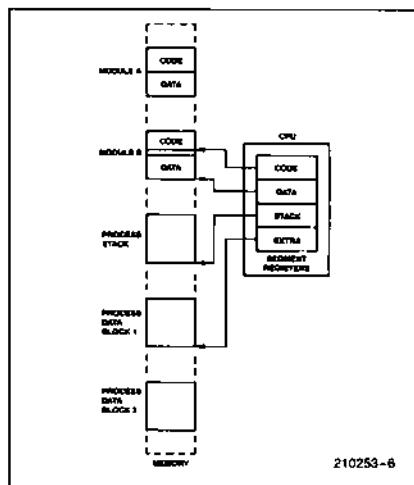


Figure 6. Segmented Memory Helps Structure Software

the **index** (contents of either the SI or DI index registers)

Any carry out from the 16-bit addition is ignored. Eight-bit displacements are sign extended to 16-bit values.

Combinations of these three address elements define the six memory addressing modes, described below.

**Direct Mode:** The operand's offset is contained in the instruction as an 8 or 16-bit displacement element.

**Register Indirect Mode:** The operand's offset is in one of the registers SI, DI, BX, or BP.

**Based Mode:** The operand's offset is the sum of an 8 or 16-bit displacement and the contents of a base register (BX or BP).

**Indexed Mode:** The operand's offset is the sum of an 8 or 16-bit displacement and the contents of an index register (SI or DI).

**Based Indexed Mode:** The operand's offset is the sum of the contents of a base register and an index register.

**Based Indexed Mode with Displacement:** The operand's offset is the sum of a base register's contents, an index register's contents, and an 8 or 16-bit displacement.

## Data Types

The 80286 directly supports the following data types:

- Integer: A signed binary numeric value contained in an 8-bit byte or a 16-bit word. All operations assume a 2's complement representation. Signed 32 and 64-bit integers are supported using the IAPX 286/20 Numeric Data Processor.
- Ordinal: An unsigned binary numeric value contained in an 8-bit byte or 16-bit word.
- Pointer: A 32-bit quantity, composed of a segment selector component and an offset component. Each component is a 16-bit word.
- String: A contiguous sequence of bytes or words. A string may contain from 1 byte to 64K bytes.
- ASCII: A byte representation of alphanumeric and control characters using the ASCII standard of character representation.
- BCD: A byte (unpacked) representation of the decimal digits 0-9.
- Packed BCD: A byte (packed) representation of two decimal digits 0-9 storing one digit in each nibble of the byte.
- Floating Point: A signed 32, 64, or 60-bit real number representation. (Floating point operands are supported using the IAPX 286/20 Numeric Processor configuration).

Figure 7 graphically represents the data types supported by the IAPX286.

either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register. 8-bit port addresses are zero extended such that A<sub>15</sub>-A<sub>8</sub> are LOW. I/O port addresses 00FB(H) through 00FF(H) are reserved.

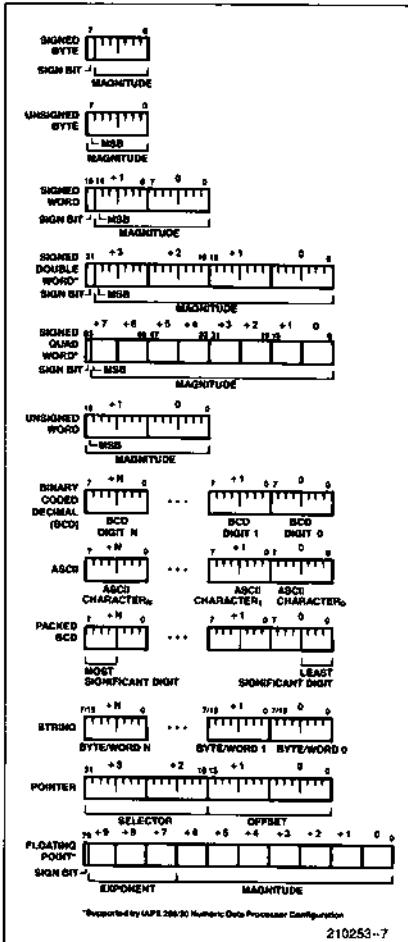


Figure 7. IAPX286 Supported Data Types

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## I/O Space

The I/O space consists of 64K 8-bit or 32K 16-bit ports. I/O instructions address the I/O space with

Table 4. Interrupt Vector Assignments

Function	Interrupt Number	Related Instructions	Does Return Address Point to Instruction Causing Exception?
Divide error exception	0	DIV, IDIV	Yes
Single step interrupt	1	All	
NMI interrupt	2	INT 2 or NMI pin	
Breakpoint interrupt	3	INT 3	
INTO detected overflow exception	4	INTO	No
BOUND range exceeded exception	5	BOUND	Yes
Invalid opcode exception	6	Any undefined opcode	Yes
Processor extension not available exception	7	ESC or WAIT	Yes
Intel reserved—do not use	8-15		
Processor extension error interrupt	16	ESC or WAIT	
Intel reserved—do not use	17-31		
User defined	32-255		

### Interrupts

An interrupt transfers execution to a new program location. The old program address (CS:P) and machine state (Flags) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware initiated, INT instructions, and instruction exceptions. Hardware initiated interrupts occur in response to an external input and are classified as non-maskable or maskable. Programs may cause an interrupt with an INT instruction. Instruction exceptions occur when an unusual condition, which prevents further instruction processing, is detected while attempting to execute an instruction. The return address from an exception will always point at the instruction causing the exception and include any leading instruction prefixes.

A table containing up to 256 pointers defines the proper interrupt service routine for each interrupt. Interrupts 0-31, some of which are used for instruction exceptions, are reserved. For each interrupt, an 8-bit vector must be supplied to the 80286 which identifies the appropriate table entry. Exceptions supply the interrupt vector internally. INT instructions contain or imply the vector and allow access to all 256 interrupts. Maskable hardware initiated interrupts supply the 8-bit vector to the CPU during an interrupt acknowledge bus sequence. Non-maskable hardware interrupts use a predefined internally supplied vector.

### MASKABLE INTERRUPT (INTR)

The 80286 provides a maskable hardware interrupt request pin, INTR. Software enables this input by

setting the interrupt flag bit (IF) in the flag word. All 224 user-defined interrupt sources can share this input, yet they can retain separate interrupt handlers. An 8-bit vector read by the CPU during the interrupt acknowledge sequence (discussed in System Interface section) identifies the source of the interrupt.

Further maskable interrupts are disabled while servicing an interrupt by resetting the IF but as part of the response to an interrupt or exception. The saved flag word will reflect the enable status of the processor prior to the interrupt. Until the flag word is restored to the flag register, the interrupt flag will be zero unless specifically set. The interrupt return instruction includes restoring the flag word, thereby restoring the original status of IF.

### NON-MASKABLE INTERRUPT REQUEST (NMI)

A non-maskable interrupt input (NMI) is also provided. NMI has higher priority than INTR. A typical use of NMI would be to activate a power failure routine. The activation of this input causes an interrupt with an internally supplied vector value of 2. No external interrupt acknowledge sequence is performed.

While executing the NMI servicing procedure, the 80286 will service neither further NMI requests, INTR requests, nor the processor extension segment overrun interrupt until an interrupt return (IRET) instruction is executed or the CPU is reset. If NMI occurs while currently servicing an NMI, its presence will be saved for servicing after executing the first IRET instruction. IF is cleared at the beginning of an NMI interrupt to inhibit INTR interrupts.

### SINGLE STEP INTERRUPT

The 80286 has an internal interrupt that allows programs to execute one instruction at a time. It is called the single step interrupt and is controlled by the single step flag bit (TF) in the flag word. Once this bit is set, an internal single step interrupt will occur after the next instruction has been executed. The interrupt clears the TF bit and uses an internally supplied vector of 1. The IRET instruction is used to set the TF bit and transfer control to the next instruction to be single stepped.

### Interrupt Priorities

When simultaneous interrupt requests occur, they are processed in a fixed order as shown in Table 5. Interrupt processing involves saving the flags, return address, and setting CS:IP to point at the first instruction of the interrupt handler. If other interrupts remain enabled they are processed before the first instruction of the current interrupt handler is executed. The last interrupt processed is therefore the first one serviced.

**Table 5. Interrupt Processing Order**

Order	Interrupt
1	Instruction exception
2	Single step
3	NMI
4	Processor extension segment overrun
5	INTR
6	INT instruction

### Initialization and Processor Reset

Processor initialization or start up is accomplished by driving the RESET input pin HIGH. RESET forces the 80286 to terminate all execution and local bus activity. No instruction or bus activity will occur as long as RESET is active. After RESET becomes inactive and an internal processing interval elapses, the 80286 begins execution in real address mode with the instruction at physical location FFFFF0(H).

RESET also sets some registers to predefined values as shown in Table 6.

**Table 6. 80286 Initial Register State after RESET**

Flag word	0002(H)
Machine Status Word	FFFO(H)
Instruction pointer	FFF0(H)
Code segment	F000(H)
Data segment	0000(H)
Extra segment	0000(H)
Stack segment	0000(H)

### Machine Status Word Description

The machine status word (MSW) records when a task switch takes place and controls the operating mode of the 80286. It is a 16-bit register of which the lower four bits are used. One bit places the CPU into protected mode, while the other three bits, as shown in Table 7, control the processor extension interface. After RESET, this register contains FFF0(H) which places the 80286 in iAPX 86 real address mode.

**Table 7. MSW Bit Functions**

Bit Position	Name	Function
0	PE	Protected mode enable places the 80286 into protected mode and cannot be cleared except by RESET.
1	MP	Monitor processor extension allows WAIT instructions to cause a processor extension not present exception (number 7).
2	EM	Emulate processor extension causes a processor extension not present exception (number 7) on ESC instructions to allow emulating a processor extension.
3	TS	Task switched indicates the next instruction using a processor extension will cause exception 7, allowing software to test whether the current processor extension context belongs to the current task.

The LMSW and SMSW instructions can load and store the MSW in real address mode. The recommended use of TS, EM, and MP is shown in Table 8.

**Table 8. Recommended MSW Encodings For Processor Extension Control**

TS	MP	EM	Recommended Use	Instructions Causing Exception 7
0	0	0	Initial encoding after RESET. iAPX 286 operation is identical to iAPX 86, 88.	None
0	0	1	No processor extension is available. Software will emulate its function.	ESC
1	0	1	No processor extension is available. Software will emulate its function. The current processor extension context may belong to another task.	ESC
0	1	0	A processor extension exists.	None
1	1	0	A processor extension exists. The current processor extension context may belong to another task. The Exception 7 on WAIT allows software to test for an error pending from a previous processor extension operation.	ESC or WAIT

## Halt

The HLT instruction stops program execution and prevents the CPU from using the local bus until restarted. Either NMI, INTR with IF = 1, or RESET will force the 80286 out of halt. If interrupted, the saved CS:IP will point to the next instruction after the HLT.

## IAPX 86 REAL ADDRESS MODE

The 80286 executes a fully upward-compatible superset of the 8086 instruction set in real address mode. In real address mode the 80286 is object code compatible with 8086 and 8088 software. The real address mode architecture (registers and addressing modes) is exactly as described in the IAPX 286/10 Base Architecture section of this Functional Description.

## Memory Size

Physical memory is a contiguous array of up to 1,048,576 bytes (one megabyte) addressed by pins A<sub>0</sub> through A<sub>19</sub> and BHE. A<sub>20</sub> through A<sub>23</sub> may be ignored.

## Memory Addressing

In real address mode physical memory is a contiguous array of up to 1,048,576 bytes (one megabyte) addressed by pins A<sub>0</sub> through A<sub>19</sub> and BHE. A<sub>20</sub> through A<sub>23</sub> may be ignored.

The selector portion of a pointer is interpreted as the upper 16 bits of a 20-bit segment address. The lower four bits of the 20-bit segment address are always zero. Segment addresses, therefore, begin on multiples of 16 bytes. See Figure 8 for a graphic representation of address information.

All segments in real address mode are 64K bytes in size and may be read, written, or executed. An exception or interrupt can occur if data operands or instructions attempt to wrap around the end of a segment (e.g. a word with its low order byte at offset FFFF(H) and its high order byte at offset 0000(H)). If, in real address mode, the information contained in a segment does not use the full 64K bytes, the unused end of the segment may be overlaid by another segment to reduce physical memory requirements.

## Reserved Memory Locations

The 80286 reserves two fixed areas of memory in real address mode (see Figure 9); system initialization area and interrupt table area. Locations from addresses FFFF0(H) through FFFFF(H) are re-

served for system initialization. Initial execution begins at location FFFF0(H). Locations 00000(H) through 003FF(H) are reserved for interrupt vectors.

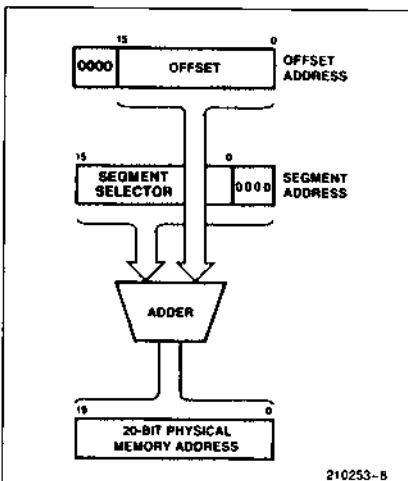


Figure 8. IAPX 86 Real Address Mode Address Calculation

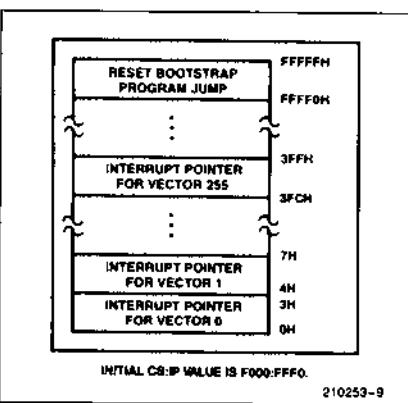


Figure 9. IAPX 86 Real Address Mode Initially Reserved Memory Locations

**Table 9. Real Address Mode Addressing Interrupts**

Function	Interrupt Number	Related Instructions	Return Address Before Instruction?
Interrupt table limit too small exception	8	iINT vector is not within table limit	Yes
Processor extension segment overrun interrupt	9	ESC with memory operand extending beyond offset FFFF(H)	No
Segment overrun exception	13	Word memory reference with offset = FFFF(H) or an attempt to execute past the end of a segment	Yes

## Interrupts

Table 9 shows the interrupt vectors reserved for exceptions and interrupts which indicate an addressing error. The exceptions leave the CPU in the state existing before attempting to execute the failing instruction (except for PUSH, POP, PUSHA, or POPA). Refer to the next section on protected mode initialization for a discussion on exception 8.

## Protected Mode Initialization

To prepare the 80286 for protected mode, the LIDT instruction is used to load the 24-bit interrupt table base and 16-bit limit for the protected mode interrupt table. This instruction can also set a base and limit for the interrupt vector table in real address mode. After reset, the interrupt table base is initialized to 000000(H) and its size set to D3FF(H). These values are compatible with iAPX 86, 88 software. LIDT should only be executed in preparation for protected mode.

## Shutdown

Shutdown occurs when a severe error is detected that prevents further instruction processing by the CPU. Shutdown and halt are externally signalled via a halt bus operation. They can be distinguished by A<sub>1</sub> HIGH for halt and A<sub>1</sub> LOW for shutdown. In real address mode, shutdown can occur under two conditions:

- Exceptions 8 or 13 happen and the IDT limit does not include the interrupt vector.
- A CALL INT or PUSH instruction attempts to wrap around the stack segment when SP is not even.

An NMI input can bring the CPU out of shutdown if the IDT limit is at least 000F(H) and SP is greater than 0005(H), otherwise shutdown can only be exited via the RESET input.

## PROTECTED VIRTUAL ADDRESS MODE

The 80286 executes a fully upward-compatible subset of the 8086 instruction set in protected virtual address mode (protected mode). Protected mode also provides memory management and protection mechanisms and associated instructions.

The 80286 enters protected virtual address mode from real address mode by setting the PE (Protection Enable) bit of the machine status word with the Load Machine Status Word (LMSW) instruction. Protected mode offers extended physical and virtual memory address space, memory protection mechanisms, and new operations to support operating systems and virtual memory.

All registers, instructions, and addressing modes described in the iAPX 286/10 Base Architecture section of this Functional Description remain the same. Programs for the iAPX 86, 88, 186, and real address mode 80286 can be run in protected mode; however, embedded constants for segment selectors are different.

## Memory Size

The protected mode 80286 provides a 1 gigabyte virtual address space per task mapped into a 16 megabyte physical address space defined by the address pin A<sub>23</sub>-A<sub>0</sub> and BHE. The virtual address space may be larger than the physical address space since any use of an address that does not map to a physical memory location will cause a restartable exception.

## Memory Addressing

As in real address mode, protected mode uses 32-bit pointers, consisting of 16-bit selector and offset components. The selector, however, specifies an index into a memory resident table rather than the upper 16-bits of a real memory address. The 24-bit

base address of the desired segment is obtained from the tables in memory. The 16-bit offset is added to the segment base address to form the physical address as shown in Figure 10. The tables are automatically referenced by the CPU whenever a segment register is loaded with a selector. All iAPX 286 instructions which load a segment register will reference the memory based tables without additional software. The memory based tables contain 8 byte values called descriptors.

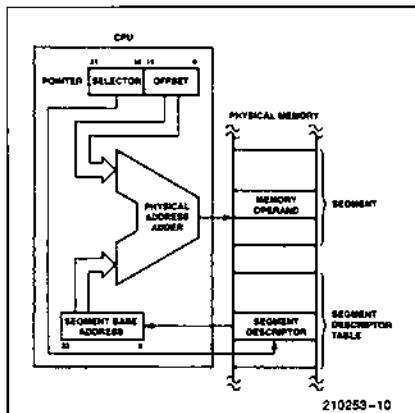


Figure 10. Protected Mode Memory Addressing

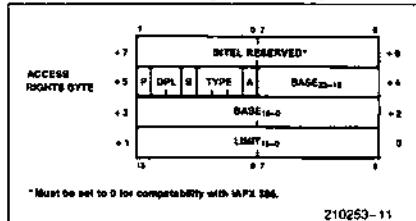
## DESCRIPTORS

Descriptors define the use of memory. Special types of descriptors also define new functions for transfer of control and task switching. The 80286 has segment descriptors for code, stack and data segments, and system control descriptors for special system data segments and control transfer operations. Descriptor accesses are performed as locked bus operations to assure descriptor integrity in multi-processor systems.

### CODE AND DATA SEGMENT DESCRIPTOR (S = 1)

Besides segment base addresses, code and data descriptors contain other segment attributes including segment size (1 to 64K bytes), access rights (read only, read/write, execute only, and execute/read), and presence in memory (for virtual memory systems) (See Figure 11). Any segment usage violating a segment attribute indicated by the segment descriptor will prevent the memory cycle and cause an exception or interrupt.

#### Code or Data Segment Descriptor



#### Access Rights Byte Definition

	Bit Position	Name	Function
Type Field Definition	7	Present (P)	P = 1 Segment is mapped into physical memory. P = 0 No mapping to physical memory exists, base and limit are not used.
	6-5	Descriptor Privilege Level (DPL)	
	4	Segment Descriptor (S)	S = 1 Code or Data (includes stacks) segment descriptor S = 0 System Segment Descriptor or Gate Descriptor
	3	Executable (E)	E = 0 Data segment descriptor type is:
	2	Expansion Direction (ED)	ED 0 Expand up segment, offsets must be < limit. ED 1 Expand down segment, offsets must be > limit.
	1	Writable (W)	W = 0 Data segment may not be written into. W = 1 Data segment may be written into.
	3	Executable (E)	E = 1 Code Segment Descriptor type is: C = 1 Code segment may only be executed when CPL ≥ DPL and CPL remains unchanged.
	2	Conforming (C)	C = 0 Code segment may be read C = 1 Code segment may be read.
	1	Readable (R)	R = 0 Code segment may not be read R = 1 Code segment may be read.
	0	Accessed (A)	A = 0 Segment has not been accessed. A = 1 Segment selector has been loaded into segment register or used by selector test instructions.

Figure 11. Code and Data Segment Descriptor Formats

Code and data (including stack data) are stored in two types of segments: code segments and data segments. Both types are identified and defined by segment descriptors ( $S = 1$ ). Code segments are identified by the executable (E) bit set to 1 in the descriptor access rights byte. The access rights byte of both code and data segment descriptor types have three fields in common: present (P) bit, Descriptor Privilege Level (DPL), and accessed (A) bit. If  $P = 0$ , any attempted use of this segment will cause a not-present exception. DPL specifies the privilege level of the segment descriptor. DPL controls when the descriptor may be used by a task (refer to privilege discussion below). The A bit shows whether the segment has been previously accessed for usage profiling, a necessity for virtual memory systems. The CPU will always set this bit when accessing the descriptor.

Data segments ( $S = 1, E = 0$ ) may be either read-only or read-write as controlled by the W bit of the access rights byte. Read-only ( $W = 0$ ) data segments may not be written into. Data segments may grow in two directions, as determined by the Expansion Direction (ED) bit: upwards ( $ED = 0$ ) for data segments, and downwards ( $ED = 1$ ) for a segment containing a stack. The limit field for a data segment descriptor is interpreted differently depending on the ED bit (see Figure 11).

A code segment ( $S = 1, E = 1$ ) may be execute-only or execute/read as determined by the Readable (R) bit. Code segments may never be written into and execute-only code segments ( $R = 0$ ) may not be read. A code segment may also have an attribute called conforming (C). A conforming code segment may be shared by programs that execute at different privilege levels. The DPL of a conforming code segment defines the range of privilege levels at which the segment may be executed (refer to privilege discussion below). The limit field identifies the last byte of a code segment.

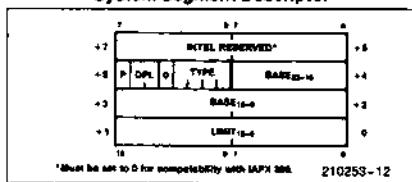
#### SYSTEM SEGMENT DESCRIPTORS ( $S = 0$ , TYPE = 1-3)

In addition to code and data segment descriptors, the protected mode 80286 defines System Segment Descriptors. These descriptors define special system data segments which contain a table of descriptors (Local Descriptor Table Descriptor) or segments which contain the execution state of a task (Task State Segment Descriptor).

Figure 12 gives the formats for the special system data segment descriptors. The descriptors contain a 24-bit base address of the segment and a 16-bit limit. The access byte defines the type of descriptor, its state and privilege level. The descriptor contents are valid and the segment is in physical memory if

$P = 1$ . If  $P = 0$ , the segment is not valid. The DPL field is only used in Task State Segment descriptors and indicates the privilege level at which the descriptor may be used (see Privilege). Since the Local Descriptor Table descriptor may only be used by a special privileged instruction, the DPL field is not used. Bit 4 of the access byte is 0 to indicate that it is a system control descriptor. The type field specifies the descriptor type as indicated in Figure 12.

#### System Segment Descriptor



#### System Segment Descriptor Fields

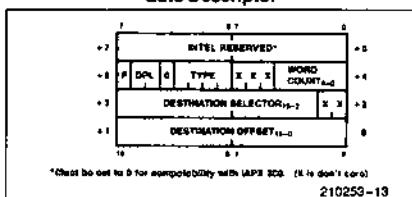
Name	Value	Description
TYPE	1	Available Task State Segment (TSS)
	2	Local Descriptor Table
	3	Busy Task State Segment (TSS)
P	0	Descriptor contents are not valid
	1	Descriptor contents are valid
DPL	0-3	Descriptor Privilege Level
BASE	24-bit number	Base Address of special system data segment in real memory
LIMIT	16-bit number	Offset of last byte in segment

Figure 12. System Segment Descriptor Format

#### GATE DESCRIPTORS ( $S = 0$ , TYPE = 4-7)

Gates are used to control access to entry points within the target code segment. The gate descriptors are call gates, task gates, interrupt gates and trap gates. Gates provide a level of indirection between the source and destination of the control transfer. This indirection allows the CPU to automatically perform protection checks and control entry point of the destination. Call gates are used to change privilege levels (see Privilege), task gates are used to perform a task switch, and interrupt and trap gates are used to specify interrupt service routines. The interrupt gate disables interrupts (resets IF) while the trap gate does not.

#### Gate Descriptor



**Gate Descriptor Fields**

Name	Value	Description
TYPE	4	-Call Gate
	5	-Task Gate
	6	-Interrupt Gate
	7	-Trap Gate
P	0	-Descriptor Contents are not valid
	1	-Descriptor Contents are valid
DPL	0-3	Descriptor Privilege Level
WORD COUNT	0-31	Number of words to copy from callers stack to called procedures stack. Only used with call gate.
DESTINATION SELECTOR	16-bit selector	Selector to the target code segment (Call, Interrupt or Trap Gate) Selector to the target task state segment (Task Gate)
DESTINATION OFFSET	16-bit offset	Entry point within the target code segment

**Figure 13. Gate Descriptor Format**

Figure 13 shows the format of the gate descriptors. The descriptor contains a destination pointer that points to the descriptor of the target segment and the entry point offset. The destination selector in an interrupt gate, trap gate, and call gate must refer to a code segment descriptor. These gate descriptors contain the entry point to prevent a program from constructing and using an illegal entry point. Task gates may only refer to a task state segment. Since task gates invoke a task switch, the destination offset is not used in the task gate.

Exception 13 is generated when the gate is used if a destination selector does not refer to the correct descriptor type. The word count field is used in the call gate descriptor to indicate the number of parameters (0-31 words) to be automatically copied from the caller's stack to the stack of the called routine when a control transfer changes privilege levels. The word count field is not used by any other gate descriptor.

The access byte format is the same for all gate descriptors. P = 1 indicates that the gate contents are valid. P = 0 indicates the contents are not valid and causes exception 11 if referenced. DPL is the de-

scriptor privilege level and specifies when this descriptor may be used by a task (refer to privilege discussion below). Bit 4 must equal 0 to indicate a system control descriptor. The type field specifies the descriptor type as indicated in Figure 13.

**SEGMENT DESCRIPTOR CACHE REGISTERS**

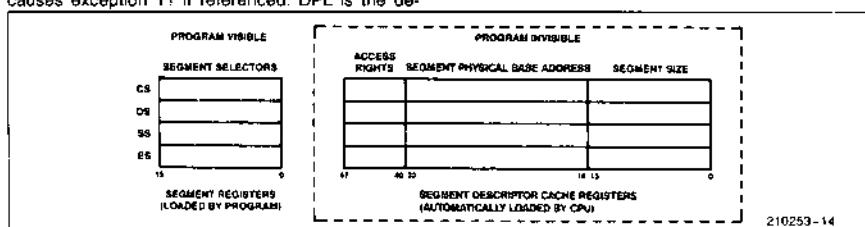
A segment descriptor cache register is assigned to each of the four segment registers (CS, SS, DS, ES). Segment descriptors are automatically loaded (cached) into a segment descriptor cache register (Figure 14) whenever the associated segment register is loaded with a selector. Only segment descriptors may be loaded into segment descriptor cache registers. Once loaded, all references to that segment of memory use the cached descriptor information instead of reaccessing the descriptor. The descriptor cache registers are not visible to programs. No instructions exist to store their contents. They only change when a segment register is loaded.

**SELECTOR FIELDS**

A protected mode selector has three fields: descriptor entry index, local or global descriptor table indicator (T1), and selector privilege (RPL) as shown in Figure 15. These fields select one of two memory based tables of descriptors, select the appropriate table entry and allow highspeed testing of the selector's privilege attribute (refer to privilege discussion below).

SELECTOR			
		INDEX	T RPL
15	14	3 2 1 0	
BIT#9	NAME	FUNCTION	
1-4	REQUESTED PRIVILEGE LEVEL (RPL)	INDICATES SELECTOR PRIVILEGE LEVEL DESIRED	
2	TABLE INDICATOR (T1)	T1 = 0 USE GLOBAL DESCRIPTOR TABLE (GDT) T1 = 1 USE LOCAL DESCRIPTOR TABLE (LDT)	
15-3	INDEX	SELECT DESCRIPTOR ENTRY IN TABLE	

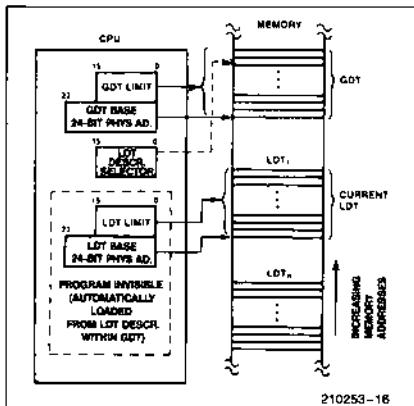
210253-15

**Figure 15. Selector Fields****Figure 14. Descriptor Cache Registers**

### LOCAL AND GLOBAL DESCRIPTOR TABLES

Two tables of descriptors, called descriptor tables, contain all descriptors accessible by a task at any given time. A descriptor table is a linear array of up to 8192 descriptors. The upper 13 bits of the selector value are an index into a descriptor table. Each table has a 24-bit base register to locate the descriptor table in physical memory and a 16-bit limit register that confine descriptor access to the defined limits of the table as shown in Figure 16. A restartable exception (13) will occur if an attempt is made to reference a descriptor outside the table limits.

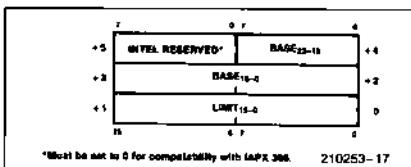
One table, called the Global Descriptor table (GDT), contains descriptors available to all tasks. The other table, called the Local Descriptor Table (LDT), contains descriptors that can be private to a task. Each task may have its own private LDT. The GDT may contain all descriptor types except interrupt and trap descriptors. The LDT may contain only segment, task gate, and call gate descriptors. A segment cannot be accessed by a task if its segment descriptor does not exist in either descriptor table at the time of access.



**Figure 16. Local and Global Descriptor Table Definition**

The LGDT and LLDT instructions load the base and limit of the global and local descriptor tables. LGDT and LLDT are privileged, i.e. they may only be executed by trusted programs operating at level 0. The LGDT instruction loads a six byte field containing the 16-bit table limit and 24-bit physical base address of the Global Descriptor Table as shown in Figure 17. The LDT instruction loads a selector which refers to a Local Descriptor Table descriptor containing the

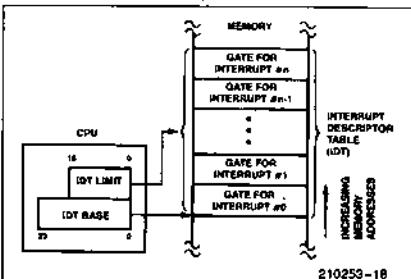
base address and limit for an LDT, as shown in Figure 12.



**Figure 17. Global Descriptor Table and Interrupt Descriptor Table Data Type**

### INTERRUPT DESCRIPTOR TABLE

The protected mode 80286 has a third descriptor table, called the Interrupt Descriptor Table (IDT) (see Figure 18), used to define up to 256 interrupts. It may contain only task gates, interrupt gates and trap gates. The IDT (Interrupt Descriptor Table) has a 24-bit physical base and 16-bit limit register in the CPU. The privileged LIDT instruction loads these registers with a six byte value of identical form to that of the LGDT instruction (see Figure 17 and Protected Mode Initialization).

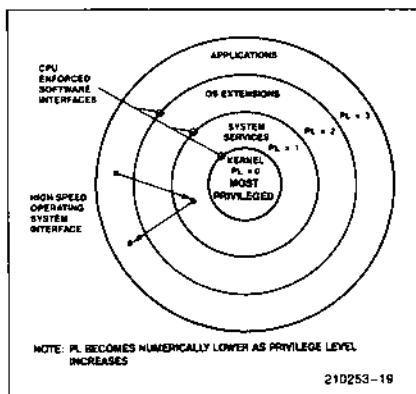


**Figure 18. Interrupt Descriptor Table Definition**

References to IDT entries are made via INT instructions, external interrupt vectors, or exceptions. The IDT must be at least 256 bytes in size to allocate space for all reserved interrupts.

### Privilege

The 80286 has a four-level hierarchical privilege system which controls the use of privileged instructions and access to descriptors (and their associated segments) within a task. Four-level privilege, as shown in Figure 19, is an extension of the user/supervisor mode commonly found in minicomputers. The privilege levels are numbered 0 through 3. Level 0 is the



most privileged level. Privilege levels provide protection within a task. (Tasks are isolated by providing private LDT's for each task.) Operating system routines, interrupt handlers, and other system software can be included and protected within the virtual address space of each task using the four levels of privilege. Each task in the system has a separate stack for each of its privilege levels.

Tasks, descriptors, and selectors have a privilege level attribute that determines whether the descriptor may be used. Task privilege effects the use of instructions and descriptors. Descriptor and selector privilege only effect access to the descriptor.

### TASK PRIVILEGE

A task always executes at one of the four privilege levels. The task privilege level at any specific instant is called the Current Privilege Level (CPL) and is defined by the lower two bits of the CS register. CPL cannot change during execution in a single code segment. A task's CPL may only be changed by control transfers through gate descriptors to a new code segment (See Control Transfer). Tasks begin executing at the CPL value specified by the code segment selector within TSS when the task is initiated via a task switch operation (See Figure 20). A task executing at Level 0 can access all data segments defined in the GDT and the task's LDT and is considered the most trusted level. A task executing at Level 3 has the most restricted access to data and is considered the least trusted level.

### DESCRIPTOR PRIVILEGE

Descriptor privilege is specified by the Descriptor Privilege Level (DPL) field of the descriptor access byte. DPL specifies the least trusted task privilege level (CPL) at which a task may access the descrip-

tor. Descriptors with DPL = 0 are the most protected. Only tasks executing at privilege level 0 (CPL = 0) may access them. Descriptors with DPL = 3 are the least protected (i.e. have the least restricted access) since tasks can access them when CPL = 0, 1, 2, or 3. This rule applies to all descriptors, except LDT descriptors.

### SELECTOR PRIVILEGE

Selector privilege is specified by the Requested Privilege Level (RPL) field in the least significant two bits of a selector. Selector RPL may establish a less trusted privilege level than the current privilege level for the use of a selector. This level is called the task's effective privilege level (EPL). RPL can only reduce the scope of a task's access to data with this selector. A task's effective privilege is the numeric maximum of RPL and CPL. A selector with RPL = 0 imposes no additional restriction on its use while a selector with RPL = 3 can only refer to segments at privilege Level 3 regardless of the task's CPL. RPL is generally used to verify that pointer parameters passed to a more trusted procedure are not allowed to use data at a more privileged level than the caller (refer to pointer testing instructions).

### Descriptor Access and Privilege Validation

Determining the ability of a task to access a segment involves the type of segment to be accessed, the instruction used, the type of descriptor used and CPL, RPL, and DPL. The two basic types of segment accesses are control transfer (selectors loaded into CS) and data (selectors loaded into DS, ES or SS).

### DATA SEGMENT ACCESS

Instructions that load selectors into DS and ES must refer to a data segment descriptor or readable code segment descriptor. The CPL of the task and the RPL of the selector must be the same as or more privileged (numerically equal to or lower than) than the descriptor DPL. In general, a task can only access data segments at the same or less privileged levels than the CPL or RPL (whichever is numerically higher) to prevent a program from accessing data it cannot be trusted to use.

An exception to the rule is a readable conforming code segment. This type of code segment can be read from any privilege level.

If the privilege checks fail (e.g. DPL is numerically less than the maximum of CPL and RPL) or an incorrect type of descriptor is referenced (e.g. gate de-

descriptor or execute only code segment) exception 13 occurs. If the segment is not present, exception 11 is generated.

Instructions that load selectors into SS must refer to data segment descriptors for writable data segments. The descriptor privilege (DPL) and RPL must equal CPL. All other descriptor types or a privilege level violation will cause exception 13. A not present fault causes exception 12.

#### CONTROL TRANSFER

Four types of control transfer can occur when a selector is loaded into CS by a control transfer operation (see Table 10). Each transfer type can only occur if the operation which loaded the selector references the correct descriptor type. Any violation of these descriptor usage rules (e.g. JMP through a call gate or RET to a Task State Segment) will cause exception 13.

The ability to reference a descriptor for control transfer is also subject to rules of privilege. A CALL or JUMP instruction may only reference a code segment descriptor with DPL equal to the task CPL or a conforming segment with DPL of equal or greater privilege than CPL. The RPL of the selector used to reference the code descriptor must have as much privilege as CPL.

RET and IRET instructions may only reference code segment descriptors with descriptor privilege equal to or less privileged than the task CPL. The selector loaded into CS is the return address from the stack. After the return, the selector RPL is the task's new CPL. If CPL changes, the old stack pointer is popped after the return address.

When a JMP or CALL references a Task State Segment descriptor, the descriptor OPL must be the same or less privileged than the task's CPL. Refer-

ence to a valid Task State Segment descriptor causes a task switch (see Task Switch Operation). Reference to a Task State Segment descriptor at a more privileged level than the task's CPL generates exception 13.

When an instruction or interrupt references a gate descriptor, the gate DPL must have the same or less privilege than the task CPL. If DPL is at a more privileged level than CPL, exception 13 occurs. If the destination selector contained in the gate references a code segment descriptor, the code segment descriptor DPL must be the same or more privileged than the task CPL. If not, Exception 13 is issued. After the control transfer, the code segment descriptors DPL is the task's new CPL. If the destination selector in the gate references a task state segment, a task switch is automatically performed (see Task Switch Operation).

The privilege rules on control transfer require:

- JMP or CALL direct to a code segment (code segment descriptor) can only be to a conforming segment with DPL of equal or greater privilege than CPL or a non-conforming segment at the same privilege level.
- interrupts within the task or calls that may change privilege levels, can only transfer control through a gate at the same or a less privileged level than CPL to a code segment at the same or more privileged level than CPL.
- return instructions that don't switch tasks can only return control to a code segment at the same or less privileged level.
- task switch can be performed by a call, jump or interrupt which references either a task gate or task state segment at the same or less privileged level.

Table 10. Descriptor Types Used for Control Transfer

Control Transfer Types	Operation Types	Descriptor Referenced	Descriptor Table
Intersegment within the same privilege level	JMP, CALL, RET, IRET*	Code Segment	GDT/LDT
Intersegment to the same or higher privilege level Interrupt within task may change CPL.	CALL	Call Gate	GDT/LDT
	Interrupt Instruction, Exception, External Interrupt	Trap or Interrupt Gate	IDT
Intersegment to a lower privilege level (changes task CPL)	RET, IRET*	Code Segment	GDT/LDT
	CALL, JMP	Task State Segment	GDT
Task Switch	CALL, JMP	Task Gate	GDT/LDT
	IRET** Interrupt Instruction, Exception, External Interrupt	Task Gate	IDT

\*NT (Nested Task bit of flag word) = 0

\*\*NT (Nested Task bit of flag word) = 1

### PRIVILEGE LEVEL CHANGES

Any control transfer that changes CPL within the task, causes a change of stacks as part of the operation. Initial values of SS:SP for privilege levels 0, 1, and 2 are kept in the task state segment (refer to Task Switch Operation). During a JMP or CALL control transfer, the new stack pointer is loaded into the SS and SP registers and the previous stack pointer is pushed onto the new stack.

When returning to the original privilege level, its stack is restored as part of the RET or IRET instruction operation. For subroutine calls that pass parameters on the stack and cross privilege levels, a fixed number of words, as specified in the gate, are copied from the previous stack to the current stack. The inter-segment RET instruction with a stack adjustment value will correctly restore the previous stack pointer upon return.

### Protection

The 80286 includes mechanisms to protect critical instructions that affect the CPU execution state (e.g. HLT) and code or data segments from improper usage. These protection mechanisms are grouped into three forms:

**Restricted usage** of segments (e.g. no write allowed to read-only data segments). The only segments available for use are defined by descriptors in the Local Descriptor Table (LDT) and Global Descriptor Table (GDT).

**Restricted access** to segments via the rules of privilege and descriptor usage.

**Privileged instructions** or operations that may only be executed at certain privilege levels as determined by the CPL and I/O Privilege Level (IOPL). The IOPL is defined by bits 14 and 13 of the flag word.

These checks are performed for all instructions and can be split into three categories: segment load checks (Table 11), operand reference checks (Table 12), and privileged instruction checks (Table 13). Any violation of the rules shown will result in an exception. A not-present exception related to the stack segment causes exception 12.

The IRET and POPF instructions do not perform some of their defined functions if CPL is not of sufficient privilege (numerically small enough). Precisely these are:

- The IF bit is not changed if CPL > IOPL.
- The IOPL field of the flag word is not changed if CPL > 0.

No exceptions or other indication are given when these conditions occur.

Table 11  
Segment Register Load Checks

Error Description	Exception Number
Descriptor table limit exceeded	13
Segment descriptor not-present	11 or 12
Privilege rules violated	13
Invalid descriptor/segment type segment register load: —Read only data segment load to SS —Special Control descriptor load to DS, ES, SS —Execute only segment load to DS, ES, SS —Data segment load to CS —Read/Execute code segment load to SS	13

Table 12. Operand Reference Checks

Error Description	Exception Number
Write into code segment	13
Read from execute-only code segment	13
Write to read-only data segment	13
Segment limit exceeded <sup>1</sup>	12 or 13

NOTE:

Carry out in offset calculations is ignored.

Table 13. Privileged Instruction Checks

Error Description	Exception Number
CPL ≠ 0 when executing the following instructions: LIDT, LLDT, LGDT, LTR, LMSW, CTS, HLT	13
CPL > IOPL when executing the following instructions: INS, IN, OUTS, OUT, STI, CLI, LOCK	13

### EXCEPTIONS

The 80286 detects several types of exceptions and interrupts, in protected mode (see Table 14). Most are restartable after the exceptional condition is removed. Interrupt handlers for most exceptions can read an error code, pushed on the stack after the return address, that identifies the selector involved (0 if none). The return address normally points to the failing instruction, including all leading prefixes. For a processor extension segment overrun exception, the return address will not point at the ESC instruction that caused the exception; however, the processor extension registers may contain the address of the failing instruction.

Table 14. Protected Mode Exceptions

Interrupt Vector	Function	Return Address At Falling Instruction?	Always Restartable?	Error Code on Stack?
8	Double exception detected	Yes	No <sup>2</sup>	Yes
9	Processor extension segment overrun	No	No <sup>2</sup>	No
10	Invalid task state segment	Yes	Yes	Yes
11	Segment not present	Yes	Yes	Yes
12	Stack segment overrun or stack segment not present	Yes	Yes <sup>1</sup>	Yes
13	General protection	Yes	No <sup>2</sup>	Yes

**NOTE:**

- When a PUSHA or POPA instruction attempts to wrap around the stack segment, the machine state after the exception will not be restartable because stack segment wrap around is not permitted. This condition is identified by the value of the saved SP being either 0000(H), 0001(H), FFFE(H), or FFFF(H).
- These exceptions indicate a violation to privilege rules or usage rules has occurred. Restart is generally not attempted under those conditions.

These exceptions indicate a violation to privilege rules or usage rules has occurred. Restart is generally not attempted under those conditions.

All these checks are performed for all instructions and can be split into three categories: segment load checks (Table 11), operand reference checks (Table 12), and privileged instruction checks (Table 13). Any violation of the rules shown will result in an exception. A not-present exception causes exception 11 or 12 and is restartable.

## Special Operations

### TASK SWITCH OPERATION

The 80286 provides a built-in task switch operation which saves the entire 80286 execution state (registers, address space, and a link to the previous task), loads a new execution state, and commences execution in the new task. Like gates, the task switch operation is invoked by executing an inter-segment JMP or CALL instruction which refers to a Task State Segment (TSS) or task gate descriptor in the GDT or LDT. An INT n instruction, exception, or external interrupt may also invoke the task switch operation by selecting a task gate descriptor in the associated IDT descriptor entry.

The TSS descriptor points at a segment (see Figure 20) containing the entire 80286 execution state while a task gate descriptor contains a TSS selector. The limit field of the descriptor must be > 002B(H).

Each task must have a TSS associated with it. The current TSS is identified by a special register in the 80286 called the Task Register (TR). This register contains a selector referring to the task state segment descriptor that defines the current TSS. A hidden base and limit register associated with TR are loaded whenever TR is loaded with a new selector.

The IRET instruction is used to return control to the task that called the current task or was interrupted. Bit 14 in the flag register is called the Nested Task (NT) bit. It controls the function of the IRET instruction. If NT = 0, the IRET instruction performs the regular current task by popping values off the stack; when NT = 1, IRET performs a task switch operation back to the previous task.

When a CALL, JMP, or INT instruction initiates a task switch, the old (except for case of JMP) and new TSS will be marked busy and the back link field of the new TSS set to the old TSS selector. The NT bit of the new task is set by CALL or INT initiated task switches. An interrupt that does not cause a task switch will clear NT. NT may also be set or cleared by POPF or IRET instructions.

The task state segment is marked busy by changing the descriptor type field from Type 1 to Type 3. Use of a selector that references a busy task state segment causes Exception 13.

### PROCESSOR EXTENSION CONTEXT SWITCHING

The context of a processor extension (such as the 80287 numerics processor) is not changed by the task switch operation. A processor extension context need only be changed when a different task attempts to use the processor extension (which still contains the context of a previous task). The 80286 detects the first use of a processor extension after a task switch by causing the processor extension not present exception (7). The interrupt handler may then decide whether a context change is necessary.

Whenever the 80286 switches tasks, it sets the Task Switched (TS) bit of the MSW. TS indicates that a processor extension context may belong to a different task than the current one. The processor extension not present exception (7) will occur when attempting to execute an ESC or WAIT instruction if TS=1 and a processor extension is present (MP=1 in MSW).

## POINTER TESTING INSTRUCTIONS

The iAPX 286 provides several instructions to speed pointer testing and consistency checks for maintaining system integrity (see Table 15). These instruc-

tions use the memory management hardware to verify that a selector value refers to an appropriate segment without risking an exception. A condition flag (ZF) indicates whether use of the selector or segment will cause an exception.

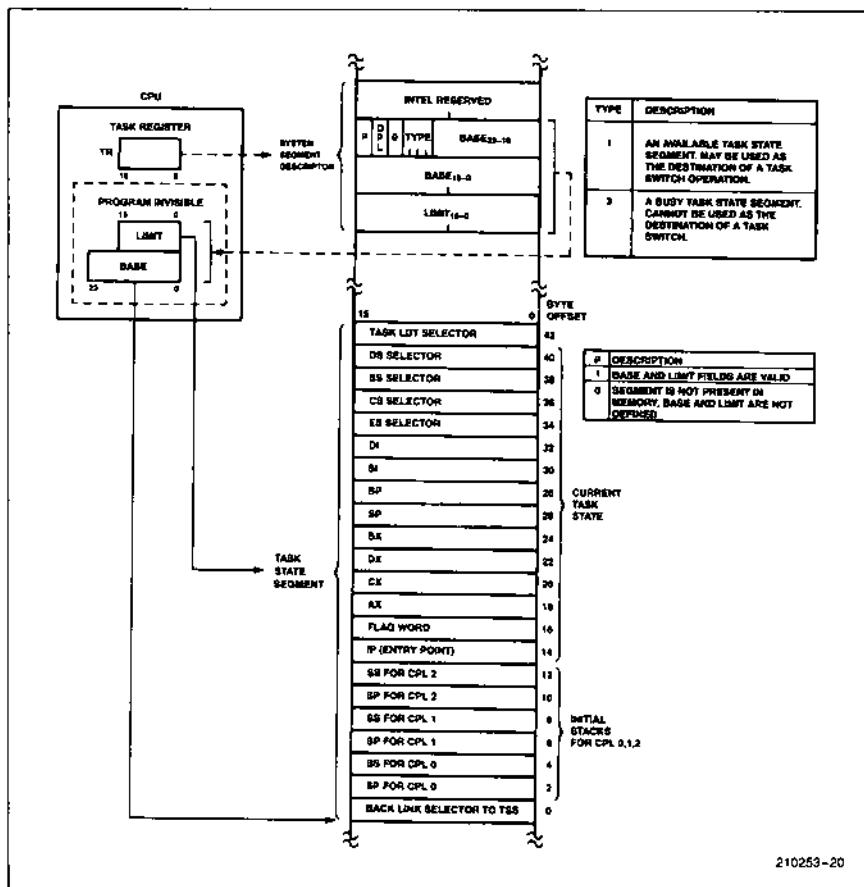


Figure 20. Task State Segment and TSS Registers

Table 15. 80286 Pointer Test Instructions

Instruction	Operands	Function
ARPL	Selector, Register	Adjust Requested Privilege Level: adjusts the RPL of the selector to the numeric maximum of current selector RPL value and the RPL value in the register. Set zero flag if selector RPL was changed by ARPL.
VERR	Selector	VERify for Read: sets the zero flag if the segment re- ferred to by the selector can be read.
VERW	Selector	VERify for Write: sets the zero flag if the segment re- ferred to by the selector can be written.
LSL	Register, Selector	Load Segment Limit: reads the segment limit into the register if privilege rules and descriptor type allow. Set zero flag if successful.
LAR	Register, Selector	Load Access Rights: reads the descriptor access rights byte into the register if privilege rules allow. Set zero flag if successful.

#### DOUBLE FAULT AND SHUTDOWN

If two separate exceptions are detected during a single instruction execution, the 80286 performs the double fault exception (B). If an execution occurs during processing of the double fault exception, the 80286 will enter shutdown. During shutdown no further instructions or exceptions are processed. Either NMI (CPU remains in protected mode) or RESET (CPU exits protected mode) can force the 80286 out of shutdown. Shutdown is externally signalled via a HALT bus operation with A<sub>1</sub> HIGH.

#### PROTECTED MODE INITIALIZATION

The 80286 initially executes in real address mode after RESET. To allow initialization code to be placed at the top of physical memory, A<sub>23-20</sub> will be HIGH when the 80286 performs memory references relative to the CS register until CS is changed. A<sub>23-20</sub> will be zero for references to the DS, ES, or SS segments. Changing CS in real address mode will force A<sub>23-20</sub> LOW whenever CS is used again. The initial CS:IP value of F000:FFFF provides 64K bytes of code space for initialization code without changing CS.

Protected mode operation requires several registers to be initialized. The GDT and IDT base registers must refer to a valid GDT and IDT. After executing the LMSW instruction to set PE, the 80286 must im-

mediately execute an intra-segment JMP instruction to clear the instruction queue of instructions decoded in real address mode.

To force the 80286 CPU registers to match the initial protected mode state assumed by software, execute a JMP instruction with a selector referring to the initial TSS used in the system. This will load the task register, local descriptor table register, segment registers and initial general register state. The TR should point at a valid TSS since any task switch operation involves saving the current task state.

#### SYSTEM INTERFACE

The 80286 system interface appears in two forms: a local bus and a system bus. The local bus consists of address, data, status, and control signals at the pins of the CPU. A system bus is any buffered version of the local bus. A system bus may also differ from the local bus in terms of coding of status and control lines and/or timing and loading of signals. The iAPX 286 family includes several devices to generate standard system buses such as the IEEE 796 standard Multibus™.

#### Bus Interface Signals and Timing

The iAPX 286 microsystem local bus interfaces the 80286 to local memory and I/O components. The interface has 24 address lines, 16 data lines, and 8 status and control signals.

The 80286 CPU, 82284 clock generator, 82288 bus controller, 82289 bus arbiter, 8286/7 transceivers, and 8282/3 latches provide a buffered and decoded system bus interface. The 82284 generates the system clock and synchronizes READY and RESET. The 82288 converts bus operation status encoded by the 80286 into command and bus control signals. The 82289 bus arbiter generates Multibus bus arbitration signals. These components can provide the timing and electrical power drive levels required for most system bus interfaces including the Multibus.

#### Physical Memory and I/O Interface

A maximum of 16 megabytes of physical memory can be addressed in protected mode. One megabyte can be addressed in real address mode. Memory is accessible as bytes or words. Words consist of any two consecutive bytes addressed with the least significant byte stored in the lowest address.

Byte transfers occur on either half of the 16-bit local data bus. Even bytes are accessed over D<sub>7-0</sub> while odd bytes are transferred over D<sub>15-8</sub>. Even-addressed words are transferred over D<sub>15-0</sub> in one bus cycle, while odd-addressed word require two bus operations. The first transfers data on D<sub>15-8</sub>, and the second transfers data on D<sub>7-0</sub>. Both byte data transfers occur automatically, transparent to software.

Two bus signals,  $A_0$  and  $BHE$ , control transfers over the lower and upper halves of the data bus. Even address byte transfers are indicated by  $A_0$  LOW and  $BHE$  HIGH. Odd address byte transfers are indicated by  $A_0$  HIGH and  $BHE$  LOW. Both  $A_0$  and  $BHE$  are LOW for even address word transfers.

The I/O address space contains 64K addresses in both modes. The I/O space is accessible as either bytes or words, as is memory. Byte wide peripheral devices may be attached to either the upper or lower byte of the data bus. Byte-wide I/O devices attached to the upper data byte ( $D_{15-8}$ ) are accessed with odd I/O addresses. Devices on the lower data byte are accessed with even I/O addresses. An interrupt controller such as Intel's 8259A must be connected to the lower data byte ( $D_{7-0}$ ) for proper return of the interrupt vector.

### Bus Operation

The 80286 uses a double frequency system clock (CLK input) to control bus timing. All signals on the local bus are measured relative to the system CLK input. The CPU divides the system clock by 2 to produce the internal processor clock, which determines bus state. Each processor clock is composed of two system clock cycles named phase 1 and phase 2. The 82284 clock generator output (PCLK) identifies the next phase of the processor clock. (See Figure 21.)

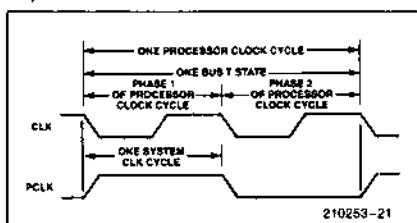


Figure 21. System and Processor Clock Relationships

Six types of bus operations are supported: memory read, memory write, I/O read, I/O write, interrupt acknowledge, and halt/shutdown. Data can be transferred at a maximum rate of one word per two processor clock cycles.

The iAPX 286 bus has three basic states: idle ( $T_I$ ), send status ( $T_S$ ), and perform command ( $T_C$ ). The 80286 CPU also has a fourth local bus state called hold ( $T_H$ ).  $T_H$  indicates that the 80286 has surrendered control of the local bus to another bus master in response to a HOLD request.

Each bus state is one processor clock long. Figure 22 shows the four 80286 local bus states and allowed transitions.

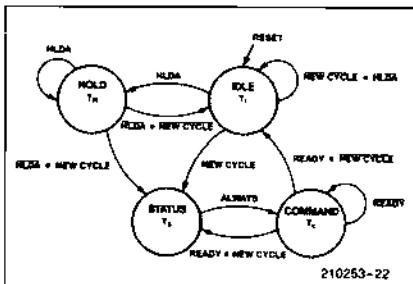


Figure 22. 80286 Bus States

### Bus States

The idle ( $T_I$ ) state indicates that no data transfers are in progress or requested. The first active state  $T_S$  is signaled by status line  $S1$  or  $S0$  going LOW and identifying phase 1 of the processor clock. During  $T_S$ , the command encoding, the address, and data (for a write operation) are available on the 80286 output pins. The 82288 bus controller decodes the status signals and generates Multibus compatible read/write command and local transceiver control signals.

After  $T_S$ , the perform command ( $T_C$ ) state is entered. Memory or I/O devices respond to the bus operation during  $T_C$ , either transferring read data to the CPU or accepting write data.  $T_C$  states may be repeated as often as necessary to assure sufficient time for the memory or I/O device to respond. A repeated  $T_C$  state is called a wait state.

During hold ( $T_H$ ), the 80286 will float all address, data, and status output pins enabling another bus master to use the local bus. The 80286 HOLD input signal is used to place the 80286 into the  $T_H$  state. The 80286 HLDA output signal indicates that the CPU has entered  $T_H$ .

### Pipelined Addressing

The 80286 uses a local bus interface with pipelined timing to allow as much time as possible for data access. Pipelined timing allows a new bus operation to be initiated every two processor cycles, while allowing each individual bus operation to last for three processor cycles.

The timing of the address outputs is pipelined such that the address of the next bus operation becomes available during the current bus operation. Or in other words, the first clock of the next bus operation is overlapped with the last clock of the current bus operation. Therefore, address decode and routing logic can operate in advance of the next bus operation.

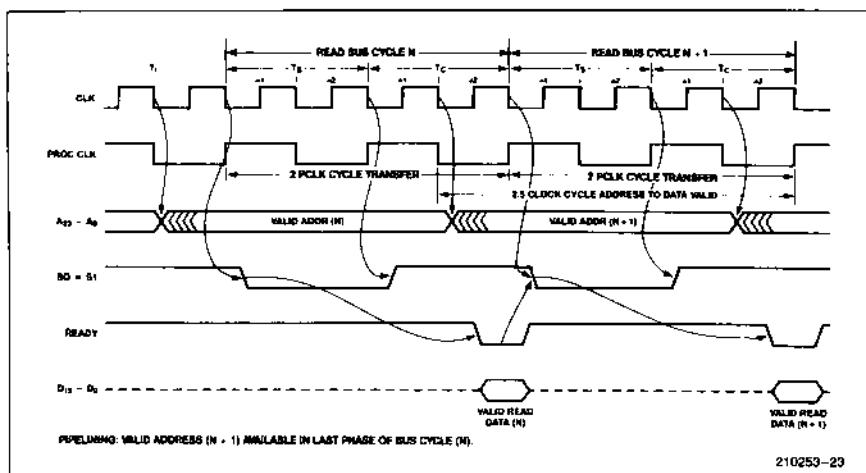


Figure 23. Basic Bus Cycle

External address latches may hold the address stable for the entire bus operation, and provide additional AC and DC buffering.

The 80286 does not maintain the address of the current bus operation during all  $T_c$  states. Instead, the address for the next bus operation may be emitted during phase 2 of any  $T_c$ . The address remains valid during phase 1 of the first  $T_c$  to guarantee hold time, relative to ALE, for the address latch inputs.

### Bus Control Signals

The 82288 bus controller provides control signals; address latch enable (ALE), Read/Write commands, data transmit/receive (DT/R), and data enable (DEN) that control the address latches, data transceivers, write enable, and output enable for memory and I/O systems.

The Address Latch Enable (ALE) output determines when the address may be latched. ALE provides at least one system CLK period of address hold time from the end of the previous bus operation until the address for the next bus operation appears at the latch outputs. This address hold time is required to support MULTIBUS® and common memory systems.

The data bus transceivers are controlled by 82288 outputs Data Enable (DEN) and Data Transmit/Receive (DT/R). DEN enables the data transceivers; while DT/R controls transceiver direction. DEN and DT/R are timed to prevent bus contention between the bus master, data bus transceivers, and system data bus transceivers.

### Command Timing Controls

Two system timing customization options, command extension and command delay, are provided on the IAPX 286 local bus.

Command extension allows additional time for external devices to respond to a command and is analogous to inserting wait states on the 8086. External logic can control the duration of any bus operation such that the operation is only as long as necessary. The READY input signal can extend any bus operation for as long as necessary.

Command delay allows an increase of address or write data setup time to system bus command active for any bus operation by delaying when the system bus command becomes active. Command delay is controlled by the 82288 CMDLY input. After  $T_S$ , the bus controller samples CMDLY at each falling edge of CLK. If CMDLY is HIGH, the 82288 will not activate the command signal. When CMDLY is LOW, the 82288 will activate the command signal. After the command becomes active, the CMDLY input is not sampled.

When a command is delayed, the available response time from command active to return read data or accept write data is less. To customize system bus timing, an address decoder can determine which bus operations require delaying the command. The CMDLY input does not affect the timing of ALE, DEN, or DT/R.

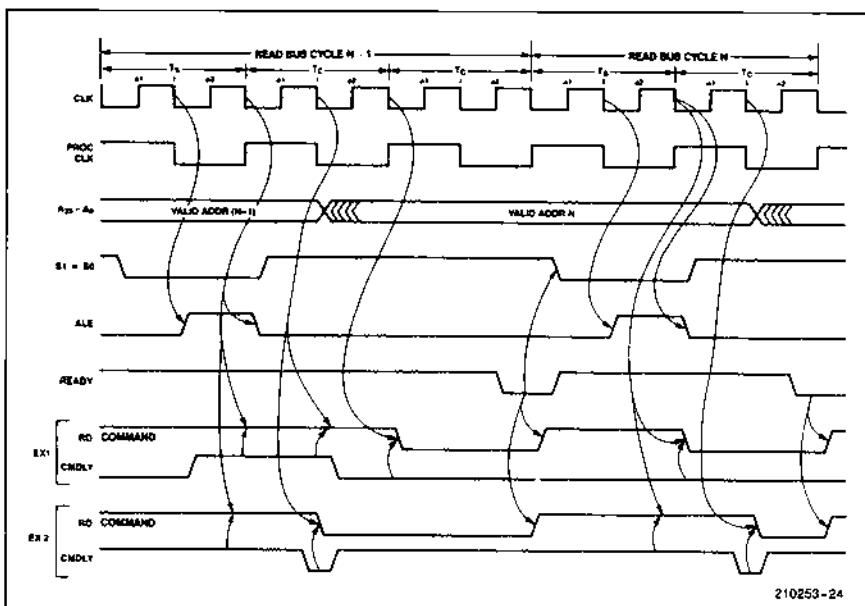


Figure 24. CMDLY Controls the Leading Edge of Command Signal

Figure 24 illustrates four uses of CMDLY. Example 1 shows delaying the read command two system CLks for cycle N-1 and no delay for cycle N, and Example 2 shows delaying the read command one system CLK for cycle N-1 and one system CLK delay for cycle N.

### Bus Cycle Termination

At maximum transfer rates, the iAPX 286 bus alternates between the status and command states. The bus status signals become inactive after  $T_S$  so that they may correctly signal the start of the next bus operation after the completion of the current cycle. No external indication of  $T_C$  exists on the iAPX 286 local bus. The bus master and bus controller enter  $T_C$  directly after  $T_S$  and continue executing  $T_C$  cycles until terminated by READY.

### READY Operation

The current bus master and 82284 bus controller terminate each bus operation simultaneously to achieve maximum bus operation bandwidth. Both are informed in advance by READY active (open-collector output from 82284) which identifies the last  $T_C$  cycle of the current bus operation. The bus master and bus controller must see the same sense of

the READY signal, thereby requiring READY be synchronous to the system clock.

### Synchronous Ready

The 82284 clock generator provides READY synchronization from both synchronous and asynchronous sources (see Figure 25). The synchronous ready input (SRDY) of the clock generator is sampled with the falling edge of CLK at the end of phase 1 of each  $T_C$ . The state of SRDY is then broadcast to the bus master and bus controller via the READY output line.

### Asynchronous Ready

Many systems have devices or subsystems that are asynchronous to the system clock. As a result, their ready outputs cannot be guaranteed to meet the 82284 SRDY setup and hold time requirements. But the 82284 asynchronous ready input (ARDY) is designed to accept such signals. The ARDY input is sampled at the beginning of each  $T_C$  cycle by 82284 synchronization logic. This provides one system CLK cycle time to resolve its value before broadcasting it to the bus master and bus controller.

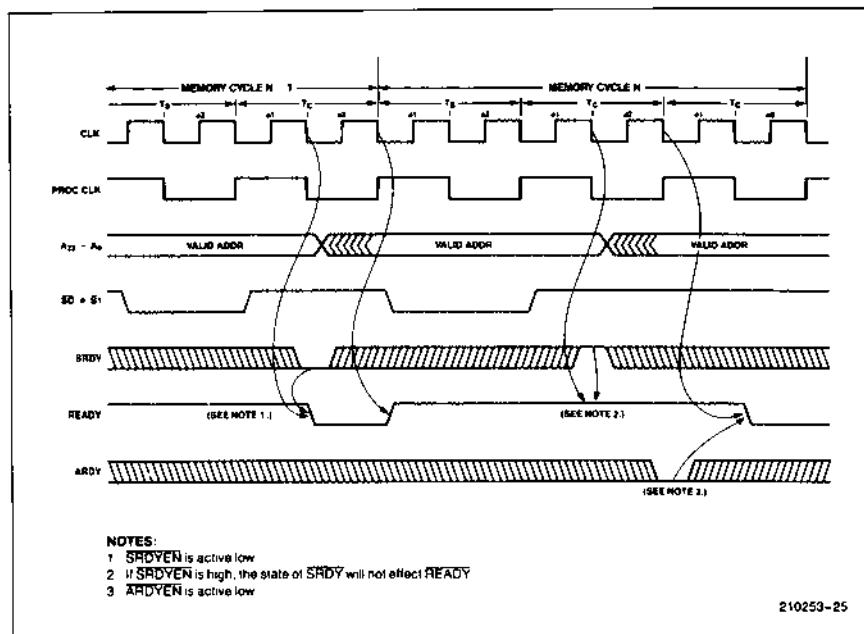


Figure 25. Synchronous and Asynchronous Ready

ARDY or ARDYEN must be HIGH at the end of T<sub>S</sub>. ARDY cannot be used to terminate bus cycle with no wait states.

Each ready input of the 82284 has an enable pin (SRDYEN and ARDYEN) to select whether the current bus operation will be terminated by the synchronous or asynchronous ready. Either of the ready inputs may terminate a bus operation. These enable inputs are active low and have the same timing as their respective ready inputs. Address decode logic usually selects whether the current bus operation should be terminated by ARDY or SRDY.

### Data Bus Control

Figures 26, 27, and 28 show how the DT/Ā, DEN, data bus, and address signals operate for different combinations of read, write, and idle bus operations. DT/R goes active (LOW) for a read operation. DT/R remains HIGH before, during, and between write operations.

The data bus is driven with write data during the second phase of T<sub>S</sub>. The delay in write data timing allows the read data drivers, from a previous read cycle, sufficient time to enter 3-state OFF before the 80286 CPU begins driving the local data bus for write operations. Write data will always remain valid for one system clock past the last T<sub>C</sub> to provide sufficient hold time for Multibus or other similar memory or I/O systems. During write-read or write-idle sequences the data bus enters 3-state OFF during the second phase of the processor cycle after the last T<sub>C</sub>. In a write-write sequence the data bus does not enter 3-state OFF between T<sub>C</sub> and T<sub>S</sub>.

### Bus Usage

The 80286 local bus may be used for several functions: instruction data transfers, data transfers by other bus masters, instruction fetching, processor extension data transfers, interrupt acknowledge, and halt/shutdown. This section describes local bus activities which have special signals or requirements.

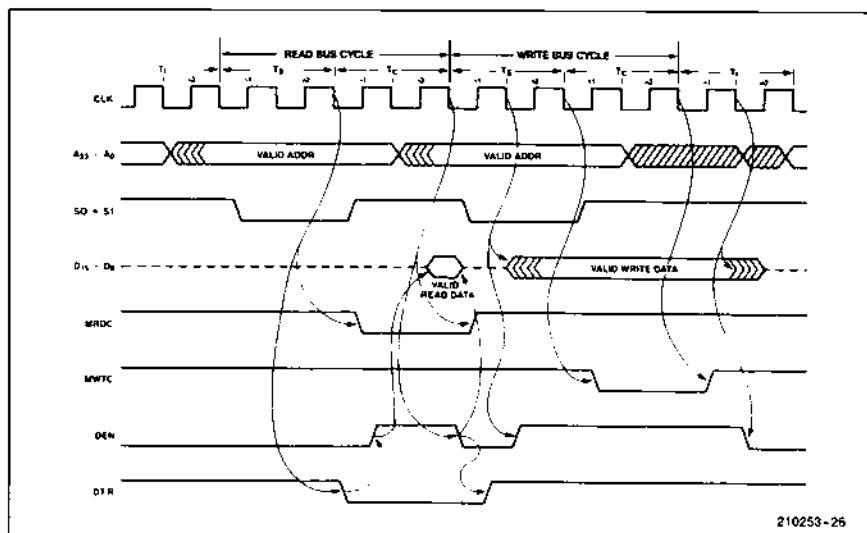


Figure 26. Back to Back Read-Write Cycles

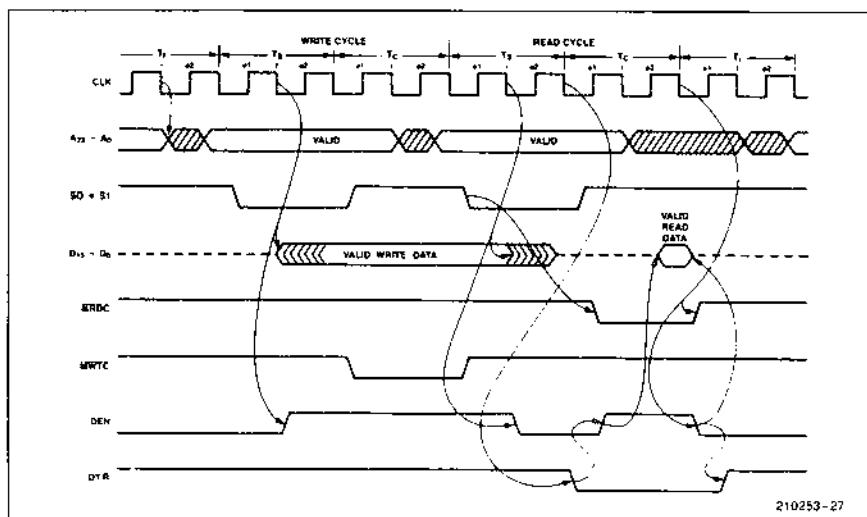


Figure 27. Back to Back Write-Read Cycles

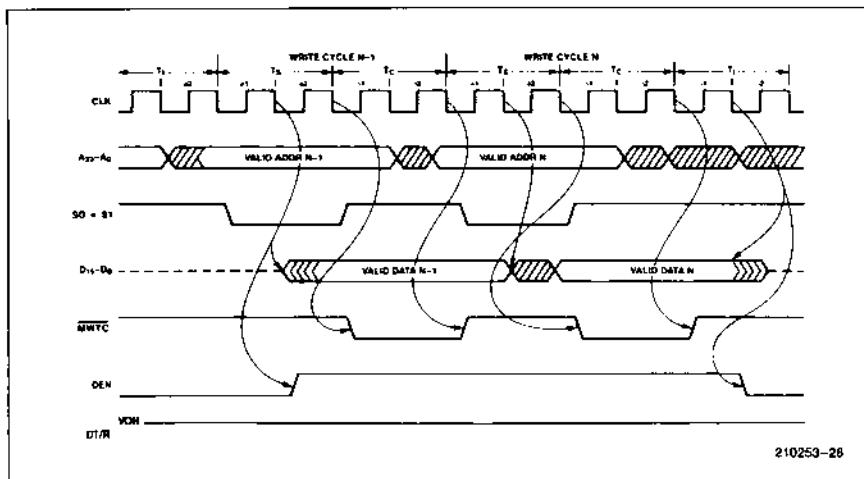


Figure 28. Back to Back Write-Write Cycles

## HOLD and HLDA

HOLD AND HLDA allow another bus master to gain control of the local bus by placing the 80286 bus into the  $T_h$  state. The sequence of events required to pass control between the 80286 and another local bus master are shown in Figure 29.

In this example, the 80286 is initially in the  $T_h$  state as signaled by HLDA being active. Upon leaving  $T_h$ , as signaled by HLDA going inactive, a write operation is started. During the write operation another local bus master requests the local bus from the 80286 as shown by the HOLD signal. After completing the write operation, the 80286 performs one  $T_1$  bus cycle, to guarantee write data hold time, then enters  $T_h$  as signified by HLDA going active.

The CMDLY signal and ARDY ready are used to start and stop the write bus command, respectively. Note that SRDY must be inactive or disabled by SRDYEN to guarantee ARDY will terminate the cycle.

## Instruction Fetching

The 80286 Bus Unit (BU) will fetch instructions ahead of the current instruction being executed. This activity is called prefetching. It occurs when the local bus would otherwise be idle and obeys the following rules:

A prefetch bus operation starts when at least two bytes of the 6-byte prefetch queue are empty.

The prefetcher normally performs word prefetches independent of the byte alignment of the code segment base in physical memory.

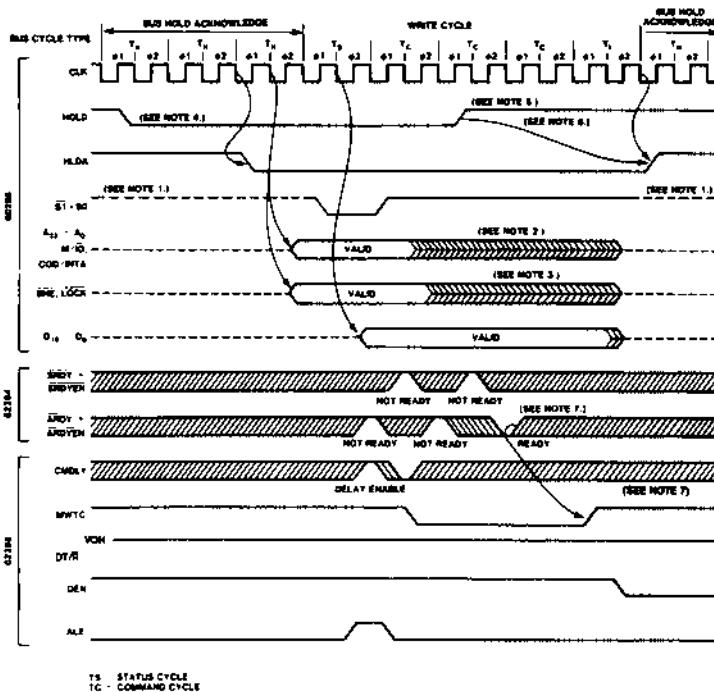
The prefetcher will perform only a byte code fetch operation for control transfers to an instruction beginning on a numerically odd physical address.

Prefetching stops whenever a control transfer or HLT instruction is decoded by the IU and placed into the instruction queue.

In real address mode, the prefetcher may fetch up to 6 bytes beyond the last control transfer or HLT instruction in a code segment.

In protected mode, the prefetcher will never cause a segment overrun exception. The prefetcher stops at the last physical memory word of the code segment. Exception 13 will occur if the program attempts to execute beyond the last full instruction in the code segment.

If the last byte of a code segment appears on an even physical memory address, the prefetcher will read the next physical byte of memory (perform a word code fetch). The value of this byte is ignored and any attempt to execute it causes exception 13.



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**NOTES:**

1. Status lines are not driven by 80286, yet remain high due to pullup resistors in 82288 and 82289 during HOLD state.
2. Address, M/I/O and COD/INTA may start floating during any TC depending on when internal 80286 bus arbiter decides to release bus to external HOLD. The float starts in  $\phi 2$  of TC.
3. BHE and LOC/R may start floating after the end of any TC depending on when internal 80286 bus arbiter decides to release bus to external HOLD. The float starts in  $\phi 1$  of TC.
4. The minimum HOLD to HLDA time is shown. Maximum is one  $T_H$  longer.
5. The earliest HOLD time is shown. It will always allow a subsequent memory cycle if pending is shown.
6. The minimum HOLD to HLDA time is shown. Maximum is a function of the instruction, type of bus cycle and other machine state (i.e., Interrupts, Waits, Lock, etc.).
7. Asynchronous ready allows termination of the cycle. Synchronous ready does not signal ready in this example. Synchronous ready state is ignored after ready is signalled via the asynchronous input.

Figure 29. Multibus Write Terminated by Asynchronous Ready with Bus Hold

## Processor Extension Transfers

The processor extension interface uses I/O port addresses 00F8(H), 00FA(H), and 00FC(H) which are part of the I/O port address range reserved by Intel. An ESC instruction with Machine Status Word bits EM = 0 and TS = 0 will perform I/O bus operations to one or more of these I/O port addresses independent of the value of IOPL and CPL.

ESC instructions with memory references enable the CPU to accept PEREQ inputs for processor extension operand transfers. The CPU will determine the operand starting address and read/write status of the instruction. For each operand transfer, two or three bus operations are performed, one word transfer with I/O port address 00FA(H) and one or two bus operations with memory. Three bus operations are required for each word operand aligned on an odd byte address.

## Interrupt Acknowledge Sequence

Figure 30 illustrates an interrupt acknowledge sequence performed by the 80286 in response to an INTR input. An interrupt acknowledge sequence consists of two INTA bus operations. The first allows a master 8259A Programmable Interrupt Controller (PIC) to determine which if any of its slaves should return the interrupt vector. An eight bit vector is read on D0-D7 of the 80286 during the second INTA bus operation to select an interrupt handler routine from the interrupt table.

The Master Cascade Enable (MCE) signal of the 82288 is used to enable the cascade address drivers, during INTA bus operations (See Figure 30), onto the local address bus for distribution to slave interrupt controllers via the system address bus. The 80286 emits the LOCK signal (active LOW) during T<sub>1</sub> of the first INTA bus operation. A local bus "hold" request will not be honored until the end of the second INTA bus operation.

Three idle processor clocks are provided by the 80286 between INTA bus operations to allow for the minimum INTA to INTA time and CAS (cascade address) out delay of the 8259A. The second INTA bus operation must always have at least one extra T<sub>c</sub> state added via logic controlling READY. A<sub>23</sub>-A<sub>0</sub> are in 3-state OFF until after the first T<sub>c</sub> state of the second INTA bus operation. This prevents bus contention between the cascade address drivers and CPU address drivers. The extra T<sub>c</sub> state allows time for the 80286 to resume driving the address lines for subsequent bus operations.

## Local Bus Usage Priorities

The 80286 local bus is shared among several internal units and external HOLD requests. In case of simultaneous requests, their relative priorities are:

(Highest) Any transfers which assert LOCK either explicitly (via the LOCK instruction prefix) or implicitly (i.e. segment descriptor access, interrupt acknowledge sequence, or an XCHG with memory).

The second of the two byte bus operations required for an odd aligned word operand.

The second or third cycle of a processor extension data transfer.

Local bus request via HOLD input.

Processor extension data operand transfer via PEREQ input.

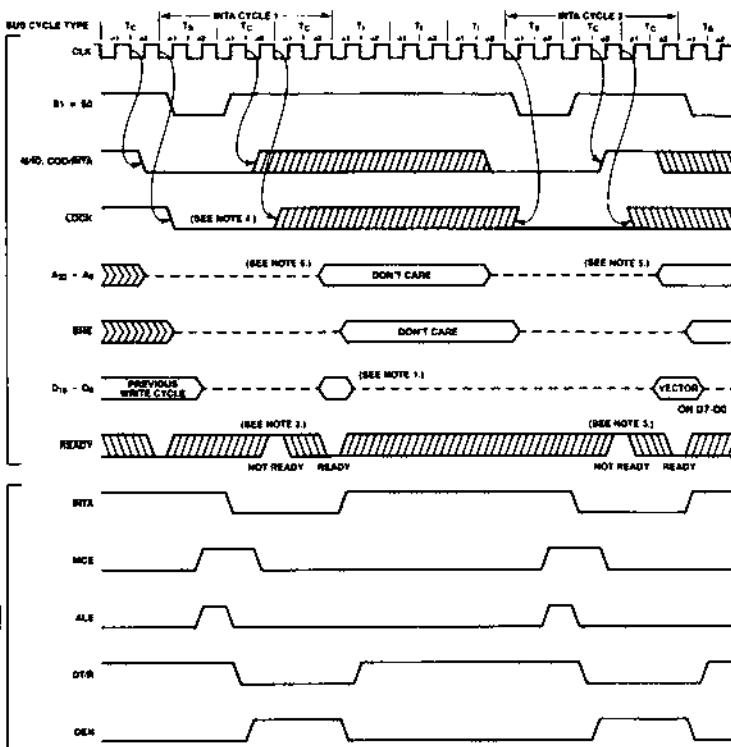
Data transfer performed by EU as part of an instruction.

(Lowest) An instruction prefetch request from BU. The EU will inhibit prefetching two processor clocks in advance of any data transfers to minimize waiting by EU for a prefetch to finish.

## Halt or Shutdown Cycles

The 80286 externally indicates halt or shutdown conditions as a bus operation. These conditions occur due to a HLT instruction or multiple protection exceptions while attempting to execute one instruction. A halt or shutdown bus operation is signalled when S1, S0 and COD/INTA are LOW and M/I0 is HIGH. A<sub>1</sub> HIGH indicates halt, and A<sub>1</sub> LOW indicates shutdown. The 82288 bus controller does not issue ALE, nor is READY required to terminate a halt or shutdown bus operation.

During halt or shutdown, the 80286 may service PEREQ or HOLD requests. A processor extension segment overrun exception during shutdown will inhibit further service of PEREQ. Either NMI or RESET will force the 80286 out of either halt or shutdown. An INTR, if interrupts are enabled, or a processor extension segment overrun exception will also force the 80286 out of halt.



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**NOTES:**

1. Data is ignored.
2. First INTA cycle should have at least one wait state inserted to meet B259A minimum INTA pulse width.
3. Second INTA cycle must have at least one wait state inserted since the CPU will not drive A<sub>23</sub>–A<sub>0</sub>, BHE, and LOCK until after the first TC state. The CPU imposed one/clock delay prevents bus contention between cascade address buffer being disabled by MCE ↓ and address outputs. Without the wait state, the 80286 address will not be valid for a memory cycle started immediately after the second INTA cycle. The 80286 also requires one wait state for minimum INTA pulse width.
4. LOCK is active for the first INTA cycle to prevent the 82289 from releasing the bus between INTA cycles in a multi-master system. LOCK is also active for the second INTA cycle.
5. A<sub>23</sub>–A<sub>0</sub> exits 3-state OFF during φ2 of the second T<sub>C</sub> in the INTA cycle.

**Figure 30. Interrupt Acknowledge Sequence**

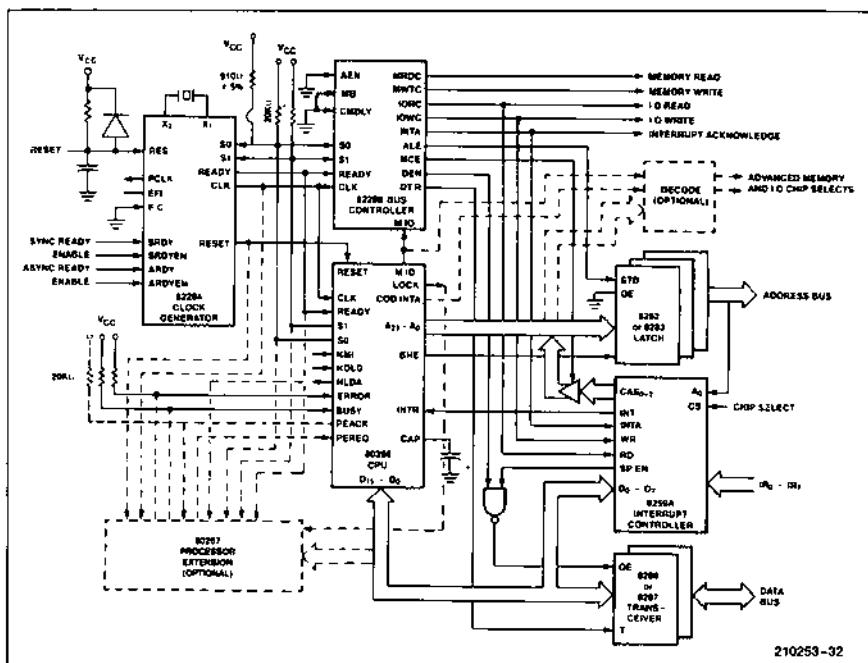


Figure 31. Basic IAPX 286 System Configuration

## SYSTEM CONFIGURATIONS

The versatile bus structure of the iAPX 286 microsystem, with a full complement of support chips, allows flexible configuration of a wide range of systems. The basic configuration, shown in Figure 31, is similar to an iAPX 86 maximum mode system. It includes the CPU plus an 8259A interrupt controller, 82284 clock generator, and the 82288 Bus Controller. The iAPX 86 latches (8282 and 8283) and transceivers (8286 and 8287) may be used in an iAPX 286 microsystem.

As indicated by the dashed lines in Figure 31, the ability to add processor extensions is an integral feature of iAPX 286 microsystems. The processor extension interface allows external hardware to perform special functions and transfer data concurrent with CPU execution of other instructions. Full system integrity is maintained because the 80286 supervises all data transfers and instruction execution for the processor extension.

The iAPX 286/20 numeric data processor which includes the 80287 numeric processor extension

(NPX) uses this interface. The iAPX 286/20 has all the instructions and data types of an iAPX 86/20 or iAPX 88/20. The 80287 NPX can perform numeric calculations and data transfers concurrently with CPU program execution. Numerics code and data have the same integrity as all other information protected by the iAPX 286 protection mechanism.

The 80286 can overlap chip select decoding and address propagation during the data transfer for the previous bus operation. This information is latched into the 8282/3's by ALE during the middle of a  $T_S$  cycle. The latched chip select and address information remains stable during the bus operation while the next cycle's address is being decoded and propagated into the system. Decode logic can be implemented with a high speed bipolar PROM.

The optional decode logic shown in Figure 31 takes advantage of the overlap between address and data of the 80286 bus cycle to generate advanced memory and IO-select signals. This minimizes system

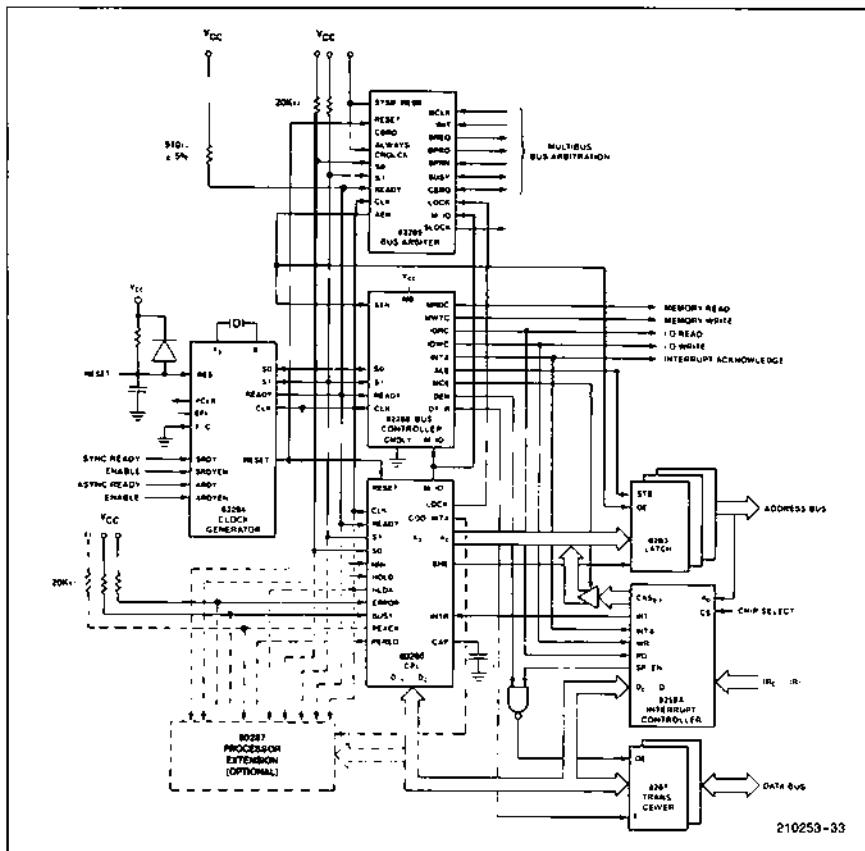


Figure 32. MULTIBUS® System Bus Interface

performance degradation caused by address propagation and decode delays. In addition to selecting memory and I/O, the advanced selects may be used with configurations supporting local and system buses to enable the appropriate bus interface for each bus cycle. The COD/INTA and M/I/O signals are applied to the decode logic to distinguish between interrupt, I/O, code and data bus cycles.

By adding the 82289 bus arbiter chip the 80286 provides a MULTIBUS system bus interface as shown in Figure 32. The ALE output of the 82288 for the

MULTIBUS bus is connected to its CMDLY input to delay the start of commands one system CLK as required to meet MULTIBUS address and write data setup times. This arrangement will add at least one extra  $T_c$  state to each bus operation which uses the MULTIBUS.

A second 82288 bus controller and additional latches and transceivers could be added to the local bus of Figure 32. This configuration allows the 80286 to support an on-board bus for local memory and peripherals, and the MULTIBUS for system bus interfacing.

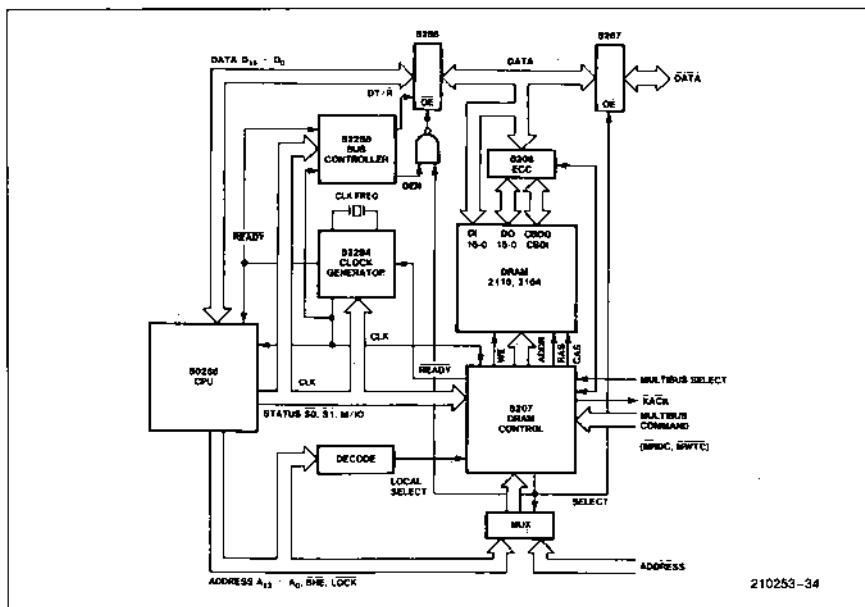


Figure 33. IAPX 286 System Configuration with Dual-Ported Memory

Figure 33 shows the addition of dual ported dynamic memory between the MULTIBUS system bus and the IAPX 286 local bus. The dual port interface is provided by the 8207 Dual Port DRAM Controller. The 8207 runs synchronously with the CPU to maximize throughput for local memory references. It also arbitrates between requests from the local and system buses and performs functions such as refresh,

initialization of RAM, and read/modify/write cycles. The 8207 combined with the 8206 Error Checking and Correction memory controller provide for single bit error correction. The dual-ported memory can be combined with a standard MULTIBUS system bus interface to maximize performance and protection in multiprocessor system configurations.

Table 16. 80286 Systems Recommended Pull Up Resistor Values

80286 Pin and Name	Pullup Value	Purpose
4—S1		
5—S0	20 KΩ ± 10%	Pull S0, S1, and PEACK inactive during 80286 hold periods
6—PEACK		
53—ERROR	20 KΩ ± 10%	Pull ERROR and BUSY inactive when 80287 not present (or temporarily removed from socket)
54—BUSY		
63—READY	810Ω ± 5%	Pull READY inactive within required minimum time ( $C_L = 150\text{ pF}$ , $I_R \leq 7\text{ mA}$ )

**PACKAGE**

The 80286 is packaged in a 68-pin, leadless JEDEC type A hermetic leadless chip carrier (LCC) and 68-pin pin grid array (PGA). Figure 34 illustrates the packages, and Figure 2 shows the pinout.

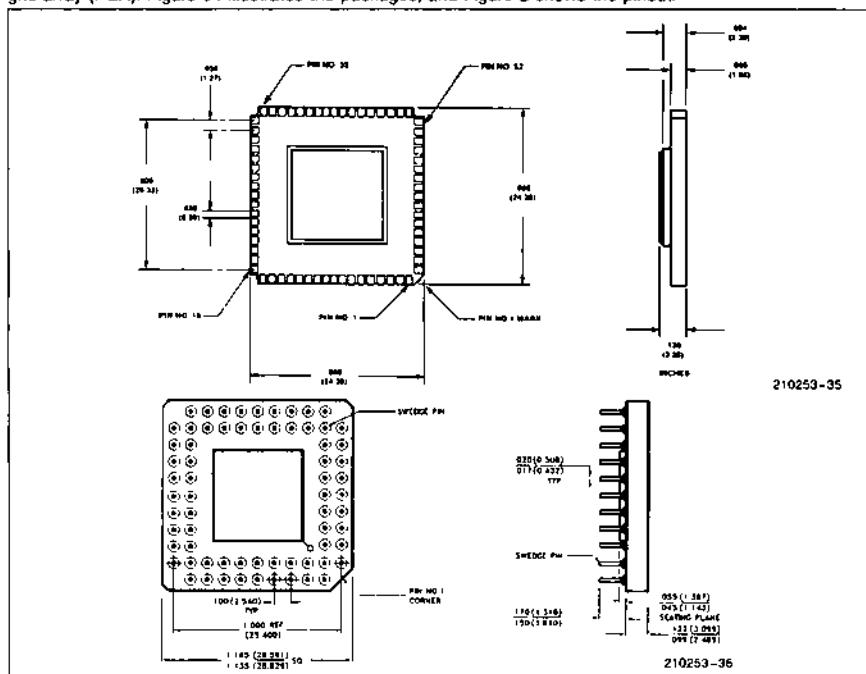


Figure 34. JEDEC Type A Package (Top) and Pin Grid Array Package

**ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature Under Bias ..... 0°C to + 70°C

Storage Temperature ..... - 65°C to + 150°C

Voltage on Any Pin with

Respect to Ground ..... - 1.0V to + 7V

Power Dissipation ..... 3.3 Watt

\*Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*NOTICE: Specifications contained within the following tables are subject to change.*

**D.C. CHARACTERISTICS ( $V_{CC} = 5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+ 55^\circ C$ , or  $T_{CASE} = 0^\circ C$  to  $+ 85^\circ C$ )**

Symbol	Parameter	6 MHz		8 MHz		10 MHz		12.5 MHz		Unit	Test Condition
		-6 Min	-6 Max	-8 Min	-8 Max	-10 Min	-10 Max	-12 Min	-12 Max		
$V_{IL}$	Input LOW Voltage	-.5	.8	-.5	.8	-.5	.8	-.5	.8	V	
$V_{IH}$	Input HIGH Voltage	2.0	$V_{CC} + .5$	2.0	$V_{CC} + .5$	2.0	$V_{CC} + .5$	2.0	$V_{CC} + .5$	V	
$V_{ILC}$	CLK Input LOW Voltage	-.5	.6	-.5	.6	-.5	.6	-.5	.6	V	
$V_{IHC}$	CLK Input HIGH Voltage	3.8	$V_{CC} + .5$	3.8	$V_{CC} + .5$	3.8	$V_{CC} + .5$	3.8	$V_{CC} + .5$	V	

**D.C. CHARACTERISTICS** ( $V_{CC} = 5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+55^\circ C$ , or  $T_{CASE} = 0^\circ C$  to  $+85^\circ C$ )

Symbol	Parameter	6 MHz		8 MHz		10 MHz		12.5 MHz		Unit	Test Condition
		-6 Min	-6 Max	-8 Min	-8 Max	-10 Min	-10 Max	-12 Min	-12 Max		
$V_{OL}$	Output LOW Voltage		0.45		0.45		0.45		0.45	V	$I_{OL} = 2.0 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.4		2.4		2.4		2.4		V	$I_{OH} = -400 \mu\text{A}$
$I_{IN}$	Input Leakage Current	$\pm 10$		$\pm 10$		$\pm 10$		$\pm 10$		$\mu\text{A}$	$0V \leq V_{IN} \leq V_{CC}$
$I_{IL}$	Input Sustaining Current on BUSY and ERROR Pins	30	500	30	500	30	500	30	500	$\mu\text{A}$	$V_{IN} = 0V$
$I_{IO}$	Output Leakage Current	$\pm 10$		$\pm 10$		$\pm 10$		$\pm 10$		$\mu\text{A}$	$0.45V \leq V_{OUT} \leq V_{CC}$
$I_{IO}$	Output Leakage Current	$\pm 1$		$\pm 1$		$\pm 1$		$\pm 1$		$\text{mA}$	$0V \leq V_{OUT} \leq 0.45V$
$I_{CC}$	Supply Current (turn on, $0^\circ C$ )	600		600		600		600		$\text{mA}$	Note 1
$C_{CLK}$	CLK Input Capacitance	20		20		20		20		$\text{pF}$	$F_C = 1 \text{ MHz}$
$C_{IN}$	Other Input Capacitance	10		10		10		10		$\text{pF}$	$F_C = 1 \text{ MHz}$
$C_O$	Input/Output Capacitance	20		20		20		20		$\text{pF}$	$F_C = 1 \text{ MHz}$

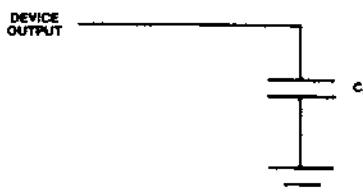
**A.C. CHARACTERISTICS** ( $V_{CC} = 5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+55^\circ C$ , or  $T_{CASE} = 0^\circ C$  to  $+85^\circ C$ )

AC timings are referenced to 0.8V and 2.0V points of signals as illustrated in datasheet waveforms, unless otherwise noted.

Symbol	Parameter	6 MHz		8 MHz		10 MHz		12.5 MHz		Unit	Test Condition
		-6 Min	-6 Max	-8 Min	-8 Max	-10 Min	-10 Max	-12 Min	-12 Max		
1	System Clock (CLK) Period	83	250	62	250	50	250	40	250	ns	
2	System Clock (CLK) LOW Time	20	225	15	225	11	232	9	234	ns	at 1.0V
3	System Clock (CLK) HIGH Time	25	230	25	235	18	239	16	241	ns	at 3.6V
17	System Clock (CLK) Rise Time		10		10		8		6	ns	1.0V to 3.6V
18	System Clock (CLK) Fall Time		10		10		8		6	ns	3.6V to 1.0V
4	Asynch. Inputs Setup Time	30		20		20		15		ns	Note 1
5	Asynch. Inputs Hold Time	30		20		20		15		ns	Note 1
6	RESET Setup Time	33		28		23		18		ns	
7	RESET Hold Time	5		5		5		5		ns	
8	Read Data Setup Time	20		10		8		8		ns	
9	Read Data Hold Time	8		8		8		8		ns	
10	READY Setup Time	50		38		26		20		ns	
11	READY Hold Time	35		25		25		20		ns	
12	Status/PEACK Valid Delay	1	55	1	40	—	—	—	—	ns	Note 2 Note 3
12a	Status/PEACK Active Delay	—	—	—	—	1	28	1	22	ns	Note 2 Note 3
12b	Status/PEACK Inactive Delay	—	—	—	—	1	30	1	24	ns	Note 2 Note 3
13	Address Valid Delay	1	80	1	60	1	47	1	37	ns	Note 2 Note 3
14	Write Data Valid Delay	0	65	0	50	0	40	0	30	ns	Note 2 Note 3
15	Address/Status/Data Float Delay	0	80	0	50	0	47	0	37	ns	Note 2 Note 4
16	HLD A Valid Delay	0	80	0	50	0	47	0	37	ns	Note 2 Note 3
19	Address Valid To Status Valid Setup Time	—		38		27		27		ns	Note 3 Note 5 Note 6

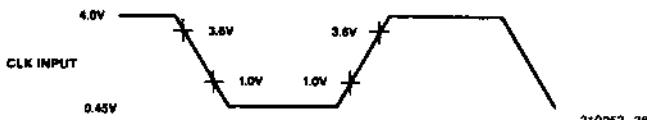
**NOTES**

1. Asynchronous inputs are INTR, NMI, HOLD, PEREQ, ERROR, and BUSY. This specification is given only for testing purposes to assure recognition at a specific CLK edge.
2. Delay from 0.8V on the CLK, to 0.8V or 2.0V or float on the output as appropriate for valid or floating condition.
3. Output load:  $C_L = 100 \text{ pF}$ .
4. Float condition occurs when output current is less than  $I_{OL}$  in magnitude.
5. Delay measured from address either reaching 0.8V or 2.0V (valid) to status going active reaching 2.0V or status going inactive reaching 0.8V.
6. For load capacitance of 10 pF on STATUS/PEACK lines, subtract typically 7 ns for 8 MHz spec, and maximum 7 ns for 10 MHz and 12 MHz spec.

**A.C. CHARACTERISTICS** (Continued)

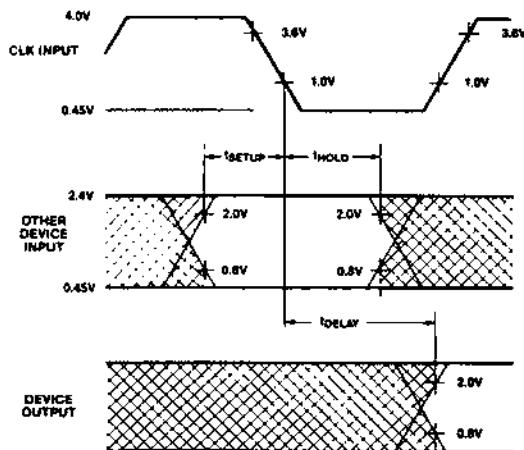
210253-37

**NOTE 7:**  
AC Test Loading on Outputs



210253-38

**NOTE 8:**  
AC Drive and Measurement Points—CLK Input



210253-39

**NOTE 9:**  
AC Setup, Hold and Delay Time Measurement—General

**A.C. CHARACTERISTICS** (Continued)**82284 Timing Requirements**

Symbol	Parameter	82284-6		82284-8		82284-10		82284-12		Units	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
11	SIRDY/SRDYEN Setup Time	25		17		15		15		ns	
12	SIRDY/SRDYEN Hold Time	0		0		0		0		ns	
13	ARDY/ARDYEN Setup Time	5		0		0		0		ns	See Note 1
14	ARDY/ARDYEN Hold Time	30		30		30		25		ns	See Note 1
19	PCLK Delay	0	45	0	45	0	35	0	32	ns	$C_L = 75 \text{ pF}$ $I_{OL} = 5 \text{ mA}$ $I_{OH} = -1 \text{ mA}$

**NOTE 1:**

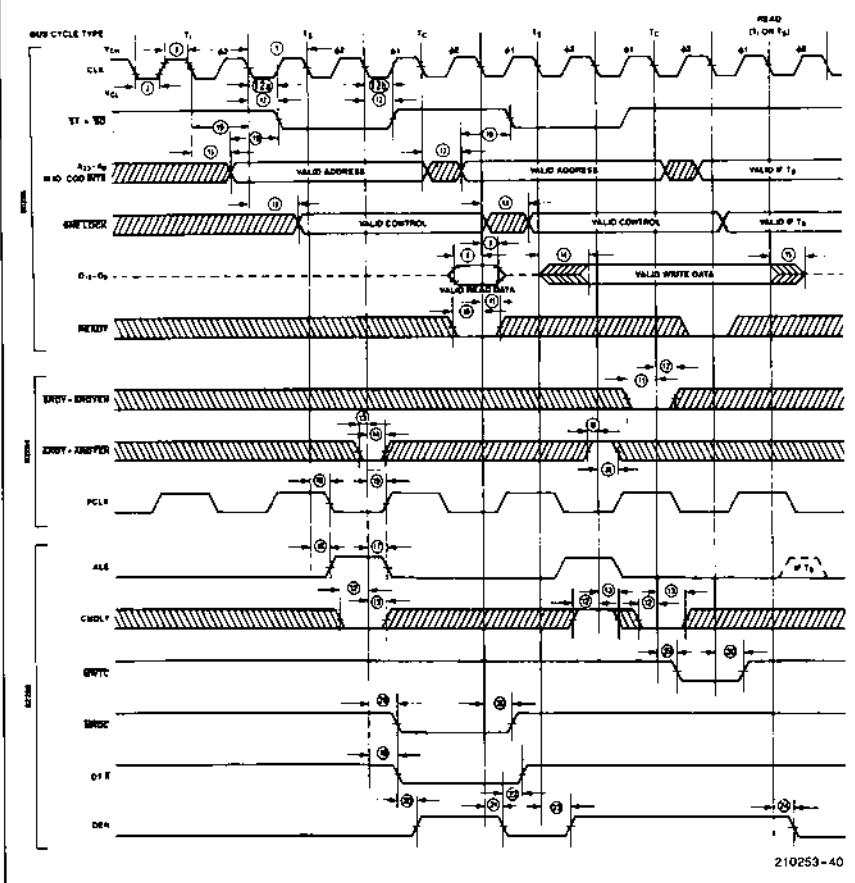
These times are given for testing purposes to assure a predetermined action.

**82288 Timing Requirements**

Symbol	Parameter	82288-6		82288-8		82288-10		Units	Test Conditions
		Min	Max	Min	Max	Min	Max		
12	CMDLY Setup Time	25		20		15		ns	
13	CMDLY Hold Time	1		1		1		ns	
30	Command Delay from CLK	3	30	3	25	3	20	ns	$C_L = 300 \text{ pF max}$ $I_{OL} = 32 \text{ mA max}$ $I_{OH} = 5 \text{ mA max}$
29	Command Active	3	40	3	25	3	21		
16	ALE Active Delay	3	25	3	20	3	16	ns	
17	ALE Inactive Delay		35		25		19	ns	
19	DT/R Read Active Delay		40	0	25	0	23	ns	
22	DT/R Read Inactive Delay	5	45	5	35	5	20	ns	
20	DEN Read Active Delay	5	50	5	35	5	21	ns	
21	DEN Read Inactive Delay	3	40	3	35	3	21	ns	
23	DEN Write Active Delay		35		30		23	ns	
24	DEN Write Inactive Delay	3	35	3	30	3	19	ns	

## WAVEFORMS

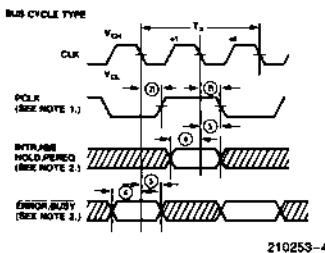
## MAJOR CYCLE TIMING



210253-40

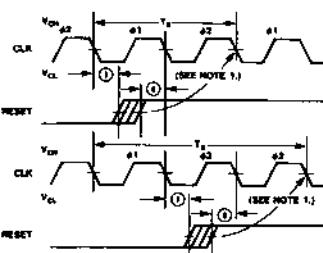
## WAVEFORMS (Continued)

## 80286 ASYNCHRONOUS INPUT SIGNAL TIMING



210253-41

## 80286 RESET INPUT TIMING AND SUBSEQUENT PROCESSOR CYCLE PHASE



210253-42

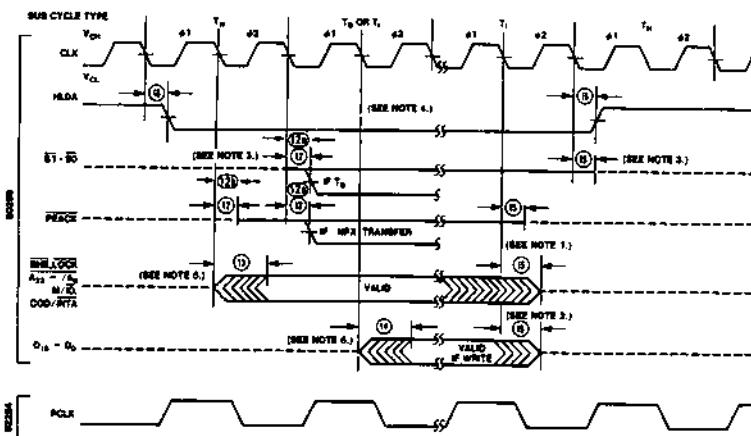
## NOTES:

1. PCLK indicates which processor cycle phase will occur on the next CLK. PCLK may not indicate the correct phase until the first bus cycle is performed.
2. These inputs are asynchronous. The setup and hold times shown assure recognition for testing purposes.

## NOTE:

When RESET meets the setup time shown, the next CLK will start or repeat  $\phi_2$  of a processor cycle.

## EXITING AND ENTERING HOLD



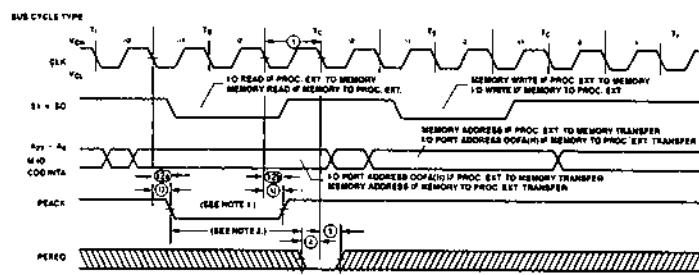
210253-43

## NOTES:

1. These signals may not be driven by the 80286 during the time shown. The worst case in terms of latest float time is shown.
2. The data bus will be driven as shown if the last cycle before  $T_1$  in the diagram was a write  $T_C$ .
3. The 80286 floats its status pins during  $T_H$ . External 20 K $\Omega$  resistors keep these signals high (see Table 16).
4. For HOLD request set up to HLDA, refer to Figure 29.
5. BHE and LOCK are driven at this time but will not become valid until  $T_S$ .
6. The data bus will remain in 3-state OFF if a read cycle is performed.

## **WAVEFORMS** (Continued)

#### **80286 PERIODIC TIMING FOR ONE TRANSFER ONLY**



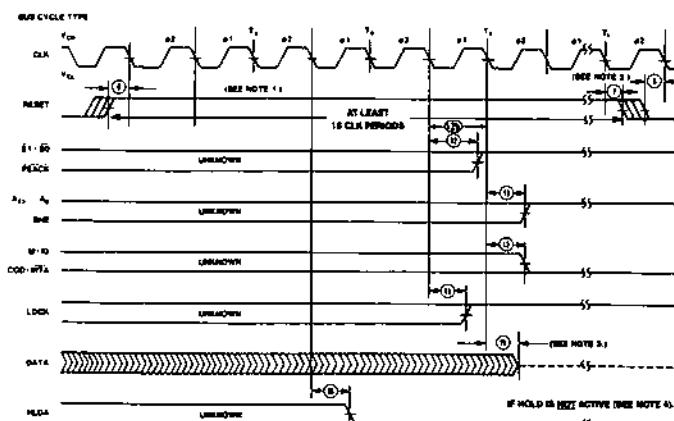
210363 14

## NOTES.

- NOTE:**

  - PEACK always goes active during the first bus operation of a processor extension data operand transfer sequence. The first bus operation will be either a memory read at operand address or I/O read at port address OOF(A-H).
  - To prevent a second processor extension data operand transfer, the worst case maximum time (Shown above) is:  $3 \times T_{C-D} - T_{max} - T_{min}$ . The actual, configuration dependent, maximum time is:  $3 \times T_{C-D} - T_{max} - T_{min} + A \times 2 \times T_C$ . A is the number of extra  $T_C$  states added to either the first or second bus operation of the processor extension data operand transfer sequence.

#### **INITIAL 80286 PIN STATE DURING RESET**



CHAPRED 45

#### NOTES.

- Notes:**

  1. Setup time for **RESET** ↓ may be violated with the consideration that  $\phi_1$  of the processor clock may begin one system CLK period later.
  2. Setup and hold times for **RESET** ↓ must be met for proper operation, but **RESET** ↓ may occur during  $\phi_1$  or  $\phi_2$ .
  3. The data bus is only guaranteed to be in 3-state OFF at the time shown.
  4. **HOLD** is acknowledged during **RESET**, causing **HLD** to go active and the appropriate pins to float. If **HOLD** remains active while **RESET** goes inactive, the 80286 remains in **HOLD** state and will not perform any bus accesses until **HOLD** is de-asserted.

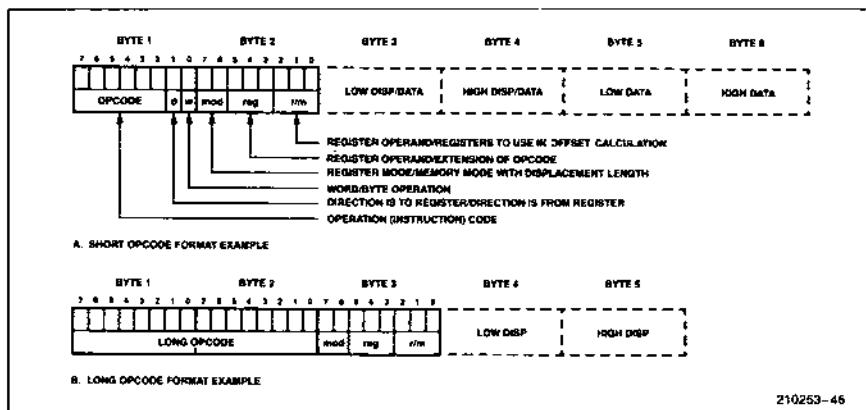


Figure 35. 80286 Instruction Format Examples

## 80286 INSTRUCTION SET SUMMARY

### Instruction Timing Notes

The instruction clock counts listed below establish the maximum execution rate of the 80286. With no delays in bus cycles, the actual clock count of an 80286 program will average 5% more than the calculated clock count, due to instruction sequences which execute faster than they can be fetched from memory.

To calculate elapsed times for instruction sequences, multiply the sum of all instruction clock counts, as listed in the table below, by the processor clock period. An 8 MHz processor clock has a clock period of 125 nanoseconds and requires an 80286 system clock (CLK input) of 16 MHz.

### Instruction Clock Count Assumptions

1. The instruction has been prefetched, decoded, and is ready for execution. Control transfer instruction clock counts include all time required to fetch, decode, and prepare the next instruction for execution.
2. Bus cycles do not require wait states.
3. There are no processor extension data transfer or local bus HOLD requests.
4. No exceptions occur during instruction execution.

### Instruction Set Summary Notes

Addressing displacements selected by the MOD field are not shown. If necessary they appear after the instruction fields shown.

Above/below refers to unsigned value

Greater refers to positive signed value

Less refers to less positive (more negative) signed values

if d = 1 then to register; if d = 0 then from register  
if w = 1 then word instruction; if w = 0 then byte instruction

if s = 0 then 16-bit immediate data form the operand

if s = 1 then an immediate data byte is sign-extended to form the 16-bit operand

x don't care

z used for string primitives for comparison with ZF FLAG

If two clock counts are given, the smaller refers to a register operand and the larger refers to a memory operand

\* = add one clock if offset calculation requires summing 3 elements

n = number of times repeated

m = number of bytes of code in next instruction

Level (L)—Lexical nesting level of the procedure

The following comments describe possible exceptions, side effects, and allowed usage for instructions in both operating modes of the 80286.

#### REAL ADDRESS MODE ONLY

1. This is a protected mode instruction. Attempted execution in real address mode will result in an undefined opcode exception (6).
2. A segment overrun exception (13) will occur if a word operand reference at offset FFFF(H) is attempted.
3. This instruction may be executed in real address mode to initialize the CPU for protected mode.
4. The IOPL and NT fields will remain 0.
5. Processor extension segment overrun interrupt (9) will occur if the operand exceeds the segment limit.

#### EITHER MODE

6. An exception may occur, depending on the value of the operand.
7. LOCK is automatically asserted regardless of the presence or absence of the LOCK instruction prefix.
8. LOCK does not remain active between all operand transfers.

#### PROTECTED VIRTUAL ADDRESS MODE ONLY

9. A general protection exception (13) will occur if the memory operand cannot be used due to either a segment limit or access rights violation. If a stack segment limit is violated, a stack segment overrun exception (12) occurs.
10. For segment load operations, the CPL, RPL, and DPL must agree with privilege rules to avoid an exception. The segment must be present to avoid a not-present exception (11). If the SS register is the destination, and a segment not-present violation occurs, a stack exception (12) occurs.
11. All segment descriptor accesses in the GDT or LDT made by this instruction will automatically assert LOCK to maintain descriptor integrity in multiprocessor systems.
12. JMP, CALL, INT, RET, IRET instructions referring to another code segment will cause a general protection exception (13) if any privilege rule is violated.
13. A general protection exception (13) occurs if CPL ≠ 0.
14. A general protection exception (13) occurs if CPL > IOPL.
15. The IF field of the flag word is not updated if CPL > IOPL. The IOPL field is updated only if CPL = 0.
16. Any violation of privilege rules as applied to the selector operand do not cause a protection exception; rather, the instruction does not return a result and the zero flag is cleared.
17. If the starting address of the memory operand violates a segment limit, or an invalid access is attempted, a general protection exception (13) will occur before the ESC instruction is executed. A stack segment overrun exception (12) will occur if the stack limit is violated by the operand's starting address. If a segment limit is violated during an attempted data transfer, then a processor extension segment overrun exception (9) occurs.
18. The destination of an INT, JMP, CALL, RET or IRET instruction must be in the defined limit of a code segment or a general protection exception (13) will occur.

## 80286 INSTRUCTION SET SUMMARY

FUNCTION	FORMAT	CLOCK COUNT		COMMENTS					
		Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode				
<b>DATA TRANSFER</b>									
<b>MOV - Move:</b>									
Register to Register/Memory	<table border="1"><tr><td>1000100w</td><td>mod reg r/m</td></tr></table>	1000100w	mod reg r/m	2,3*	2,3*	2	9		
1000100w	mod reg r/m								
Register/memory to register	<table border="1"><tr><td>1000101w</td><td>mod reg r/m</td></tr></table>	1000101w	mod reg r/m	2,5*	2,5*	2	9		
1000101w	mod reg r/m								
Immediate to register/memory	<table border="1"><tr><td>1100011w</td><td>mod 000 r/m</td><td>data</td><td>data if w = 1</td></tr></table>	1100011w	mod 000 r/m	data	data if w = 1	2,2*	2,3*	2	9
1100011w	mod 000 r/m	data	data if w = 1						
Immediate to register	<table border="1"><tr><td>1011w reg</td><td>data</td><td>data if w = 1</td></tr></table>	1011w reg	data	data if w = 1	2	2			
1011w reg	data	data if w = 1							
Memory to accumulator	<table border="1"><tr><td>1010000w</td><td>addr-low</td><td>addr-high</td></tr></table>	1010000w	addr-low	addr-high	5	5	2	9	
1010000w	addr-low	addr-high							
Accumulator to memory	<table border="1"><tr><td>1010001w</td><td>addr-low</td><td>addr-high</td></tr></table>	1010001w	addr-low	addr-high	3	3	2	9	
1010001w	addr-low	addr-high							
Register/memory to segment register	<table border="1"><tr><td>10001110</td><td>mod 0 reg r/m</td></tr></table>	10001110	mod 0 reg r/m	2,5*	17,19*	2	9,10,11		
10001110	mod 0 reg r/m								
Segment register to register/memory	<table border="1"><tr><td>10001100</td><td>mod 0 reg r/m</td></tr></table>	10001100	mod 0 reg r/m	2,3*	2,3*	2	9		
10001100	mod 0 reg r/m								
<b>PUSH - Push:</b>									
Memory	<table border="1"><tr><td>11111111</td><td>mod 110 r/m</td></tr></table>	11111111	mod 110 r/m	5*	5*	2	9		
11111111	mod 110 r/m								
Register	<table border="1"><tr><td>01010 reg</td></tr></table>	01010 reg	3	3	2	9			
01010 reg									
Segment register	<table border="1"><tr><td>000 reg 110</td></tr></table>	000 reg 110	3	3	2	9			
000 reg 110									
Immediate	<table border="1"><tr><td>011010s0</td><td>data</td><td>data if s=0</td></tr></table>	011010s0	data	data if s=0	3	3	2	9	
011010s0	data	data if s=0							
<b>PUSHA - Push All:</b>	<table border="1"><tr><td>01100000</td></tr></table>	01100000	17	17	3	9			
01100000									
<b>POP - Pop:</b>									
Memory	<table border="1"><tr><td>10001111</td><td>mod 000 r/m</td></tr></table>	10001111	mod 000 r/m	5*	5*	2	9		
10001111	mod 000 r/m								
Register	<table border="1"><tr><td>01011 reg</td></tr></table>	01011 reg	5	5	2	9			
01011 reg									
Segment register	<table border="1"><tr><td>000 reg 111</td><td>(reg ≠ 01)</td></tr></table>	000 reg 111	(reg ≠ 01)	5	20	2	9,10,11		
000 reg 111	(reg ≠ 01)								
<b>POPA - Pop All:</b>	<table border="1"><tr><td>01100001</td></tr></table>	01100001	19	19	2	9			
01100001									
<b>XCHG - Exchange:</b>									
Register/memory with register	<table border="1"><tr><td>1000011w</td><td>mod reg r/m</td></tr></table>	1000011w	mod reg r/m	3,5*	3,5*	2,7	7,9		
1000011w	mod reg r/m								
Register with accumulator	<table border="1"><tr><td>10010 reg</td></tr></table>	10010 reg	3	3					
10010 reg									
<b>IN - Input from:</b>									
Fixed port	<table border="1"><tr><td>1110010w</td><td>port</td></tr></table>	1110010w	port	5	5		14		
1110010w	port								
Variable port	<table border="1"><tr><td>1110110w</td></tr></table>	1110110w	5	6		14			
1110110w									
<b>OUT - Output to:</b>									
Fixed port	<table border="1"><tr><td>1110011w</td><td>port</td></tr></table>	1110011w	port	3	3		14		
1110011w	port								
Variable port	<table border="1"><tr><td>1110111w</td></tr></table>	1110111w	3	3		14			
1110111w									
<b>XLAT - Translate byte to AL</b>	<table border="1"><tr><td>11010111</td></tr></table>	11010111	5	5		9			
11010111									
<b>LEA - Load EA to register</b>	<table border="1"><tr><td>10001101</td><td>mod reg r/m</td></tr></table>	10001101	mod reg r/m	3*	3*				
10001101	mod reg r/m								
<b>LOS - Load pointer to DS</b>	<table border="1"><tr><td>11000101</td><td>mod reg r/m</td><td>(mod ≠ 11)</td></tr></table>	11000101	mod reg r/m	(mod ≠ 11)	7*	21*	2	8,10,11	
11000101	mod reg r/m	(mod ≠ 11)							
<b>LES - Load pointer to ES</b>	<table border="1"><tr><td>11000100</td><td>mod reg r/m</td><td>(mod ≠ 1)</td></tr></table>	11000100	mod reg r/m	(mod ≠ 1)	7*	21*	2	8,10,11	
11000100	mod reg r/m	(mod ≠ 1)							

Shaded areas indicate instructions not available in iAPX 86, 88 microsystems.

## 80286 INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT	CLOCK COUNT		COMMENTS					
		Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode				
<b>DATA TRANSFER (Continued)</b>									
LAHF Load AH with flags	<table border="1"><tr><td>10011111</td></tr></table>	10011111	2	2					
10011111									
SAHF - Store AH into flags	<table border="1"><tr><td>10011110</td></tr></table>	10011110	2	2					
10011110									
PUSHF - Push flags	<table border="1"><tr><td>10011100</td></tr></table>	10011100	3	3	2	9			
10011100									
POPF = Pop flags	<table border="1"><tr><td>10011101</td></tr></table>	10011101	5	5	2,4	9,15			
10011101									
<b>ARITHMETIC</b>									
ADD - Add:									
Reg/memory with register to either	<table border="1"><tr><td>000000 dw</td><td>mod reg r/m</td></tr></table>	000000 dw	mod reg r/m	2,7*	2,7*	2	9		
000000 dw	mod reg r/m								
Immediate to register/memory	<table border="1"><tr><td>100000 sw</td><td>mod D 00 r/m</td><td>data</td><td>data if w = 01</td></tr></table>	100000 sw	mod D 00 r/m	data	data if w = 01	3,7*	3,7*	2	9
100000 sw	mod D 00 r/m	data	data if w = 01						
Immediate to accumulator	<table border="1"><tr><td>0000010w</td><td>data</td><td>data if w = 1</td></tr></table>	0000010w	data	data if w = 1	3	3			
0000010w	data	data if w = 1							
ADC - Add with carry:									
Reg/memory with register to either	<table border="1"><tr><td>000100 dw</td><td>mod reg r/m</td></tr></table>	000100 dw	mod reg r/m	2,7*	2,7*	2	9		
000100 dw	mod reg r/m								
Immediate to register/memory	<table border="1"><tr><td>100000 sw</td><td>mod D 10 r/m</td><td>data</td><td>data if w = 01</td></tr></table>	100000 sw	mod D 10 r/m	data	data if w = 01	3,7*	3,7*	2	9
100000 sw	mod D 10 r/m	data	data if w = 01						
Immediate to accumulator	<table border="1"><tr><td>0001010w</td><td>data</td><td>data if w = 1</td></tr></table>	0001010w	data	data if w = 1	3	3			
0001010w	data	data if w = 1							
INC = Increment:									
Register/memory	<table border="1"><tr><td>1111111w</td><td>mod D 00 r/m</td></tr></table>	1111111w	mod D 00 r/m	2,7*	2,7*	2	9		
1111111w	mod D 00 r/m								
Register	<table border="1"><tr><td>010000 reg</td></tr></table>	010000 reg	2	2					
010000 reg									
SUB = Subtract:									
Reg/memory and register to either	<table border="1"><tr><td>001010 dw</td><td>mod reg r/m</td></tr></table>	001010 dw	mod reg r/m	2,7*	2,7*	2	9		
001010 dw	mod reg r/m								
Immediate from register/memory	<table border="1"><tr><td>100000 sw</td><td>mod D 01 r/m</td><td>data</td><td>data if w = 01</td></tr></table>	100000 sw	mod D 01 r/m	data	data if w = 01	3,7*	3,7*	2	9
100000 sw	mod D 01 r/m	data	data if w = 01						
Immediate from accumulator	<table border="1"><tr><td>0010110w</td><td>data</td><td>data if w = 1</td></tr></table>	0010110w	data	data if w = 1	3	3			
0010110w	data	data if w = 1							
SSB = Subtract with borrow:									
Reg/memory and register to either	<table border="1"><tr><td>000110 dw</td><td>mod reg r/m</td></tr></table>	000110 dw	mod reg r/m	2,7*	2,7*	2	9		
000110 dw	mod reg r/m								
Immediate from register/memory	<table border="1"><tr><td>100000 sw</td><td>mod D 11 r/m</td><td>data</td><td>data if w = 01</td></tr></table>	100000 sw	mod D 11 r/m	data	data if w = 01	3,7*	3,7*	2	9
100000 sw	mod D 11 r/m	data	data if w = 01						
Immediate from accumulator	<table border="1"><tr><td>0001110w</td><td>data</td><td>data if w = 1</td></tr></table>	0001110w	data	data if w = 1	3	3			
0001110w	data	data if w = 1							
DEC = Decrement									
Register/memory	<table border="1"><tr><td>1111111w</td><td>mod D 01 r/m</td></tr></table>	1111111w	mod D 01 r/m	2,7*	2,7*	2	9		
1111111w	mod D 01 r/m								
Register	<table border="1"><tr><td>01001 reg</td></tr></table>	01001 reg	2	2					
01001 reg									
CMP = Compare									
Register/memory with register	<table border="1"><tr><td>0011101w</td><td>mod reg r/m</td></tr></table>	0011101w	mod reg r/m	2,8*	2,8*	2	9		
0011101w	mod reg r/m								
Register with register/memory	<table border="1"><tr><td>0011100w</td><td>mod reg r/m</td></tr></table>	0011100w	mod reg r/m	2,7*	2,7*	2	9		
0011100w	mod reg r/m								
Immediate with register/memory	<table border="1"><tr><td>100000 sw</td><td>mod S 11 r/m</td><td>data</td><td>data if w = 01</td></tr></table>	100000 sw	mod S 11 r/m	data	data if w = 01	3,8*	3,8*	2	9
100000 sw	mod S 11 r/m	data	data if w = 01						
Immediate with accumulator	<table border="1"><tr><td>0011110w</td><td>data</td><td>data if w = 1</td></tr></table>	0011110w	data	data if w = 1	3	3			
0011110w	data	data if w = 1							
NEG = Change sign	<table border="1"><tr><td>1111011w</td><td>mod D 11 r/m</td></tr></table>	1111011w	mod D 11 r/m	2	7*	2	7		
1111011w	mod D 11 r/m								
AAA = ASCII adjust for add	<table border="1"><tr><td>00110111</td></tr></table>	00110111	3	3					
00110111									
DAA = Decimal adjust for add	<table border="1"><tr><td>00100111</td></tr></table>	00100111	3	3					
00100111									

## 80286 INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT	CLOCK COUNT		COMMENTS							
		Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode						
<b>ARITHMETIC (Continued)</b>											
AAS = ASCII adjust for subtract	<table border="1"><tr><td>00111111</td></tr></table>	00111111	3	3							
00111111											
DAS = Decimal adjust for subtract	<table border="1"><tr><td>00101111</td></tr></table>	00101111	3	3							
00101111											
MUL = Multiply (unsigned):	<table border="1"><tr><td>1111011w</td><td>mod 100 r/m</td></tr></table>	1111011w	mod 100 r/m								
1111011w	mod 100 r/m										
Register-Byte		13	13								
Register-Word		21	21								
Memory-Byte		18*	16*	2	9						
Memory-Word		24*	24*	2	9						
IMUL = Integer multiply (signed):	<table border="1"><tr><td>1111011w</td><td>mod 101 r/m</td></tr></table>	1111011w	mod 101 r/m								
1111011w	mod 101 r/m										
Register-Byte		13	13								
Register-Word		21	21								
Memory-Byte		18*	16*	2	9						
Memory-Word		24*	24*	2	9						
BSW = Integer immediate multiply	<table border="1"><tr><td>01110101</td><td>immediate</td><td>r/m</td><td>count</td><td>mod</td><td>disp</td></tr></table>	01110101	immediate	r/m	count	mod	disp				
01110101	immediate	r/m	count	mod	disp						
[Legend]											
DIV = Divide (unsigned)	<table border="1"><tr><td>1111011w</td><td>mod 110 r/m</td></tr></table>	1111011w	mod 110 r/m								
1111011w	mod 110 r/m										
Register-Byte		14	14	8	6						
Register-Word		22	22	6	6						
Memory-Byte		17*	17*	2,6	6,9						
Memory-Word		25*	25*	2,6	6,9						
IDIV = Integer divide (signed)	<table border="1"><tr><td>1111011w</td><td>mod 111 r/m</td></tr></table>	1111011w	mod 111 r/m								
1111011w	mod 111 r/m										
Register-Byte		17	17	6	6						
Register-Word		25	25	6	6						
Memory-Byte		20*	20*	2,6	6,9						
Memory-Word		28*	28*	2,6	6,9						
AAM = ASCII adjust for multiply	<table border="1"><tr><td>11010100</td><td>00001010</td></tr></table>	11010100	00001010								
11010100	00001010										
AAD = ASCII adjust for divide	<table border="1"><tr><td>11010101</td><td>00001010</td></tr></table>	11010101	00001010								
11010101	00001010										
CBW = Convert byte to word	<table border="1"><tr><td>10011000</td></tr></table>	10011000									
10011000											
CWD = Convert word to double word	<table border="1"><tr><td>10011001</td></tr></table>	10011001									
10011001											
Logic											
Shift/Rotate Instructions											
Register/Memory by 1	<table border="1"><tr><td>1101000w</td><td>mod TTT r/m</td></tr></table>	1101000w	mod TTT r/m		2,7*	2,7*	2				
1101000w	mod TTT r/m										
Register/Memory by CL	<table border="1"><tr><td>1101001w</td><td>mod TTT r/m</td></tr></table>	1101001w	mod TTT r/m		5+n,8+n*	5+n,8+n*	2				
1101001w	mod TTT r/m										
Register/Memory by Count	<table border="1"><tr><td>1100000w</td><td>mod TTT r/m</td><td>count</td></tr></table>	1100000w	mod TTT r/m	count		5+n,8+n*	5+n,8+n*	2			
1100000w	mod TTT r/m	count									
TTT           Instruction											
000           RDL											
001           ROR											
010           RCL											
011           RCR											
100           SHL/SAL											
101           SHR											
111           SAR											

Shaded areas indicate instructions not available in iAPX 86, 88 microsystems.

## 80286 INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT	CLOCK COUNT		COMMENTS							
		Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode						
<b>ARITHMETIC (Continued)</b>											
<b>AND = And:</b>											
Reg/memory and register to either	<table border="1"><tr><td>001000 d w</td><td>mod reg</td><td>r/m</td><td></td><td></td><td></td></tr></table>	001000 d w	mod reg	r/m				2.7*	2.7*	2	9
001000 d w	mod reg	r/m									
Immediate to register/memory	<table border="1"><tr><td>1000000 w</td><td>mod 100</td><td>r/m</td><td>data</td><td>data if w = 1</td><td></td></tr></table>	1000000 w	mod 100	r/m	data	data if w = 1		3.7*	3.7*	2	9
1000000 w	mod 100	r/m	data	data if w = 1							
Immediate to accumulator	<table border="1"><tr><td>0010010 w</td><td></td><td></td><td>data</td><td>data if w = 1</td><td></td></tr></table>	0010010 w			data	data if w = 1		3	3		
0010010 w			data	data if w = 1							
<b>TEST ~ And function to flags, no result:</b>											
Register/memory and register	<table border="1"><tr><td>1000010 w</td><td>mod reg</td><td>r/m</td><td></td><td></td><td></td></tr></table>	1000010 w	mod reg	r/m				2.6*	2.6*	2	9
1000010 w	mod reg	r/m									
Immediate data and register/memory	<table border="1"><tr><td>1111011 w</td><td>mod 001</td><td>r/m</td><td>data</td><td>data if w = 1</td><td></td></tr></table>	1111011 w	mod 001	r/m	data	data if w = 1		3.6*	3.6*	2	9
1111011 w	mod 001	r/m	data	data if w = 1							
Immediate data and accumulator	<table border="1"><tr><td>1010100 w</td><td></td><td></td><td>data</td><td>data if w = 1</td><td></td></tr></table>	1010100 w			data	data if w = 1		3	3		
1010100 w			data	data if w = 1							
<b>OR = Or:</b>											
Reg/memory and register to either	<table border="1"><tr><td>000010 d w</td><td>mod reg</td><td>r/m</td><td></td><td></td><td></td></tr></table>	000010 d w	mod reg	r/m				2.7*	2.7*	2	9
000010 d w	mod reg	r/m									
Immediate to register/memory	<table border="1"><tr><td>1000000 w</td><td>mod 001</td><td>r/m</td><td>data</td><td>data if w = 1</td><td></td></tr></table>	1000000 w	mod 001	r/m	data	data if w = 1		3.7*	3.7*	2	9
1000000 w	mod 001	r/m	data	data if w = 1							
Immediate to accumulator	<table border="1"><tr><td>0000110 w</td><td></td><td></td><td>data</td><td>data if w = 1</td><td></td></tr></table>	0000110 w			data	data if w = 1		3	3		
0000110 w			data	data if w = 1							
<b>XOR = Exclusive or:</b>											
Reg/memory and register to either	<table border="1"><tr><td>001100 d w</td><td>mod reg</td><td>r/m</td><td></td><td></td><td></td></tr></table>	001100 d w	mod reg	r/m				2.7*	2.7*	2	9
001100 d w	mod reg	r/m									
Immediate to register/memory	<table border="1"><tr><td>1000000 w</td><td>mod 110</td><td>r/m</td><td>data</td><td>data if w = 1</td><td></td></tr></table>	1000000 w	mod 110	r/m	data	data if w = 1		3.7*	3.7*	2	9
1000000 w	mod 110	r/m	data	data if w = 1							
Immediate to accumulator	<table border="1"><tr><td>0011010 w</td><td></td><td></td><td>data</td><td>data if w = 1</td><td></td></tr></table>	0011010 w			data	data if w = 1		3	3		
0011010 w			data	data if w = 1							
NOT ~ Invert register/memory	<table border="1"><tr><td>1111011 w</td><td>mod 010</td><td>r/m</td><td></td><td></td><td></td></tr></table>	1111011 w	mod 010	r/m				2.7*	2.7*	2	9
1111011 w	mod 010	r/m									
<b>STRING MANIPULATION:</b>											
MOVSB = Move byte/word	<table border="1"><tr><td>1010010 w</td><td></td><td></td><td></td><td></td><td></td></tr></table>	1010010 w						5	5	2	9
1010010 w											
CMPSB = Compare byte/word	<table border="1"><tr><td>1010011 w</td><td></td><td></td><td></td><td></td><td></td></tr></table>	1010011 w						6	6	2	9
1010011 w											
BCAS = Scan byte/word	<table border="1"><tr><td>1010111 w</td><td></td><td></td><td></td><td></td><td></td></tr></table>	1010111 w						7	7	2	9
1010111 w											
LODS = Load byte/wd to AL/AX	<table border="1"><tr><td>1010110 w</td><td></td><td></td><td></td><td></td><td></td></tr></table>	1010110 w						5	5	2	9
1010110 w											
STOS = Sto byte/wd from AL/A	<table border="1"><tr><td>1010101 w</td><td></td><td></td><td></td><td></td><td></td></tr></table>	1010101 w						3	3	2	9
1010101 w											
INP = Input byte/wd from DX port	<table border="1"><tr><td>0110110 w</td><td></td><td></td><td></td><td></td><td></td></tr></table>	0110110 w						5	6	2	0,14
0110110 w											
OUTP = Output byte/wd to DX port	<table border="1"><tr><td>0110111 w</td><td></td><td></td><td></td><td></td><td></td></tr></table>	0110111 w						5	6	2	0,14
0110111 w											
Repeated by count in CX											
MOVSD = Move string	<table border="1"><tr><td>11110011</td><td>1010010 w</td><td></td><td></td><td></td><td></td></tr></table>	11110011	1010010 w					5+4n	5+4n	2	9
11110011	1010010 w										
CMPSD = Compare string	<table border="1"><tr><td>11110012</td><td>1010011 w</td><td></td><td></td><td></td><td></td></tr></table>	11110012	1010011 w					5+9n	5+9n	2,6	8,9
11110012	1010011 w										
BCASD = Scan string	<table border="1"><tr><td>11110012</td><td>1010111 w</td><td></td><td></td><td></td><td></td></tr></table>	11110012	1010111 w					5+8n	5+8n	2,8	8,9
11110012	1010111 w										
LODSD = Load string	<table border="1"><tr><td>11110011</td><td>1010110 w</td><td></td><td></td><td></td><td></td></tr></table>	11110011	1010110 w					5+4n	5+4n	2,8	8,9
11110011	1010110 w										
STOSD = Store string	<table border="1"><tr><td>11110011</td><td>1010101 w</td><td></td><td></td><td></td><td></td></tr></table>	11110011	1010101 w					4+3n	4+3n	2,8	8,9
11110011	1010101 w										
INPD = Input string	<table border="1"><tr><td>11100011</td><td>0110110 w</td><td></td><td></td><td></td><td></td></tr></table>	11100011	0110110 w					5+4n	5+4n	2	0,14
11100011	0110110 w										
OUTPD = Output string to DX port	<table border="1"><tr><td>11100011</td><td>0110111 w</td><td></td><td></td><td></td><td></td></tr></table>	11100011	0110111 w					5+4n	5+4n	2	0,14
11100011	0110111 w										

Shaded areas indicate instructions not available in IAPX 86/88 microsystems.

## 80286 INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT	CLOCK COUNT		COMMENTS				
		Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode			
<b>CONTROL TRANSFER</b>								
<b>CALL - Call:</b>								
Direct within segment	<table border="1"><tr><td>11101000</td><td>disp-low</td><td>disp-high</td></tr></table>	11101000	disp-low	disp-high	7+m	7+m	2	18
11101000	disp-low	disp-high						
Register/memory indirect within segment	<table border="1"><tr><td>11111111</td><td>mod 010</td><td>r/m</td></tr></table>	11111111	mod 010	r/m	7+m, 11+m*	7+m, 11+m*	2,6	8,9,15
11111111	mod 010	r/m						
Direct intersegment	<table border="1"><tr><td>10011010</td><td>segment offset</td><td></td></tr></table>	10011010	segment offset		13+m	26+m	2	11,12,18
10011010	segment offset							
Protected Mode Only (Direct Intersegment):	<table border="1"><tr><td>segment selector</td><td></td><td></td></tr></table>	segment selector						
segment selector								
Via call gate to same privilege level			41+m		8,11,12,18			
Via call gate to different privilege level, no parameters			82+m		8,11,12,18			
Via call gate to different privilege level, x parameters			86+4x+m		8,11,12,18			
Via TSS			177+m		8,11,12,18			
Via task gate			182+m		8,11,12,18			
Indirect intersegment	<table border="1"><tr><td>11111111</td><td>mod 011</td><td>r/m</td></tr></table>	11111111	mod 011	r/m	(mod=11)	16+m	29+m*	2,8,9,11,12,18
11111111	mod 011	r/m						
Protected Mode Only (Indirect Intersegment):								
Via call gate to same privilege level			44+m*		8,8,11,12,18			
Via call gate to different privilege level, no parameters			83+m*		8,9,11,12,18			
Via call gate to different privilege level, x parameters			90+4x+m*		8,9,11,12,18			
Via TSS			180+m*		8,9,11,12,18			
Via task gate			185+m*		8,9,11,12,18			
JMP = Unconditional jump:								
Short/long	<table border="1"><tr><td>11101011</td><td>disp-low</td><td></td></tr></table>	11101011	disp-low			7+m	7+m	18
11101011	disp-low							
Direct within segment	<table border="1"><tr><td>11101001</td><td>disp-low</td><td>disp-high</td></tr></table>	11101001	disp-low	disp-high		7+m	7+m	18
11101001	disp-low	disp-high						
Register/memory indirect within segment	<table border="1"><tr><td>11111111</td><td>mod 100</td><td>r/m</td></tr></table>	11111111	mod 100	r/m		7+m, 11+m*	7+m, 11+m*	2
11111111	mod 100	r/m						
Direct intersegment	<table border="1"><tr><td>11101010</td><td>segment offset</td><td></td></tr></table>	11101010	segment offset			11+m	23+m	11,12,18
11101010	segment offset							
Protected Mode Only (Direct Intersegment):	<table border="1"><tr><td>segment selector</td><td></td><td></td></tr></table>	segment selector						
segment selector								
Via call gate to same privilege level			38+m		8,11,12,18			
Via TSS			175+m		8,11,12,18			
Via task gate			180+m		8,11,12,18			
Indirect intersegment	<table border="1"><tr><td>11111111</td><td>mod 101</td><td>r/m</td></tr></table>	11111111	mod 101	r/m	(mod=11)	15+m*	26+m*	2,8,9,11,12,18
11111111	mod 101	r/m						
Protected Mode Only (Indirect Intersegment):								
Via call gate to same privilege level			41+m*		8,9,11,12,18			
Via TSS			178+m*		8,9,11,12,18			
Via task gate			183+m*		8,9,11,12,18			
RET = Return from CALL:								
Within segment	<table border="1"><tr><td>11000011</td><td></td><td></td></tr></table>	11000011				11+m	11+m	2,8,9,18
11000011								
Within seg adding immediate to SP	<table border="1"><tr><td>11000010</td><td>data-low</td><td>data-high</td></tr></table>	11000010	data-low	data-high		11+m	11+m	2,8,9,18
11000010	data-low	data-high						
Intersegment	<table border="1"><tr><td>11001011</td><td></td><td></td></tr></table>	11001011				15+m	25+m	2,8,9,11,12,18
11001011								
Intersegment adding immediate to SP	<table border="1"><tr><td>11001010</td><td>data-low</td><td>data-high</td></tr></table>	11001010	data-low	data-high		15+m		2,8,9,11,12,18
11001010	data-low	data-high						
Protected Mode Only (RET):								
To different privilege level				55+m	9,11,12,18			

## 80286 INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT	CLOCK COUNT		COMMENTS	
		Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode
<b>CONTROL TRANSFER (Continued)</b>					
JE/JZ = Jump on equal/zero	01110100 disp	7+m or 3	7+m or 3	18	
JL/JNQE = Jump on less/not greater or equal	01111100 disp	7+m or 3	7+m or 3	18	
JLE/JNG = Jump on less or equal/not greater	01111110 disp	7+m or 3	7+m or 3	18	
JB/JNAE = Jump on below/not above or equal	01110010 disp	7+m or 3	7+m or 3	18	
JBE/JNA = Jump on below or equal/not above	01110110 disp	7+m or 3	7+m or 3	18	
JP/JPE = Jump on parity/parity even	011111010 disp	7+m or 3	7+m or 3	18	
JO = Jump on overflow	01110000 disp	7+m or 3	7+m or 3	18	
JS = Jump on sign	01111000 disp	7+m or 3	7+m or 3	18	
JNE/JNZ = Jump on not equal/not zero	01110101 disp	7+m or 3	7+m or 3	18	
JNL/JGE = Jump on not less/greater or equal	01111101 disp	7+m or 3	7+m or 3	18	
JNL/E/JG = Jump on not less or equal/greater	01111111 disp	7+m or 3	7+m or 3	18	
JKB/JAE = Jump on not below/above or equal	01110011 disp	7+m or 3	7+m or 3	18	
JNBE/JA = Jump on not below or equal/above	01110111 disp	7+m or 3	7+m or 3	18	
JNP/JPO = Jump on not par/par odd	01111011 disp	7+m or 3	7+m or 3	18	
JND = Jump on not overflow	01110001 disp	7+m or 3	7+m or 3	18	
JNS = Jump on not sign	01111001 disp	7+m or 3	7+m or 3	18	
LOOP = Loop CX times	11000010 disp	8+m or 4	8+m or 4	18	
LOOPZ/LOOPNE = Loop while zero/equal	11000001 disp	8+m or 4	8+m or 4	18	
LOOPNZ/LOOPNE = Loop while not zero/equal	11000000 disp	8+m or 4	8+m or 4	18	
JCXZ = Jump on CX zero	11000011 disp	8+m or 4	8+m or 4	18	
ENTER = Enter Procedure	11001000 datum1 datum2 L			26	69
L=0		11	11		
L=1		10	10		
L>1		10+4(L-1)	10+4(L-1)		
LEAVE = Leave Procedure	11001001	6	6		
INT = Interrupt:					
Type specified	11001101 type	23+m		2,7,8	
Type 3	11001100	23+m		2,7,8	
INTO = Interrupt on overflow	11001110	24+m or 3 (3 if no interrupt)		2,8,8	

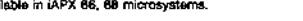
Shaded areas indicate instructions not available in IAPX 86, 88 microsystems.

## 80286 INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT	CLOCK COUNT		COMMENTS	
		Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode
<b>CONTROL TRANSFER (Continued)</b>					
Protected Mode Only:					
Via interrupt or trap gate to same privilege level		40+ m		7,8,11,12,15	
Via interrupt or trap gate to different privilege level		78+ m		7,8,11,12,15	
Via Task Gate		167+ m		7,8,11,12,15	
IRET = Interrupt return	<b>11 001111</b>	17+ m	31+ m	2,4	8,9,11,12,15,16
Protected Mode Only:					
To different privilege level		55+ m		8,9,11,12,15,16	
To different task (NT = 1)		169+ m		8,9,11,12,15	
JBUND = Detect value out of range	<b>D1100010 mod reg r/m</b>	13*	13* (Use INT clock count if exception 9)	2,6	8,9,11,12,16
<b>PROCESSOR CONTROL</b>					
CLC = Clear carry	<b>11111000</b>	2	2		
CNC = Complement carry	<b>11110101</b>	2	2		
STC = Set carry	<b>11111001</b>	2	2		
CLD = Clear direction	<b>11111100</b>	2	2		
STD = Set direction	<b>11111101</b>	2	2		
CLI = Clear interrupt	<b>11111010</b>	3	3		14
STI = Set interrupt	<b>11111011</b>	2	2		14
MLT = Halt	<b>11110100</b>	2	2		13
WAIT = Wait	<b>10011011</b>	3	3		
LOCK = Bus lock prefix	<b>11110000</b>	0	0		14
OTS = Clear task switched flag	<b>00001111 00000010</b>	2	2	3	13
ESC = Processor Extension Escape	<b>11011111 mod LLL r/m</b>	9-20*	9-20*	5,8	8,17
(LLL LLL are opcode to processor extension)					
SEG = Segment Override Prefix	<b>001 reg 110</b>	0	0		
<b>PROTECTION CONTROL</b>					
LGDT = Load global descriptor table register	<b>00001111 00000001 mod 010 r/m</b>	11*	11*	2,8	8,13
SGDT = Store global descriptor table register	<b>00001111 00000001 mod 000 r/m</b>	11*	11*	2,8	8
LIDT = Load interrupt descriptor table register	<b>00001111 00000001 mod 011 r/m</b>	12*	12*	2,8	8,13
SIDT = Store interrupt descriptor table register	<b>00001111 00000001 mod 001 r/m</b>	12*	12*	2,8	8
LLDT = Load local descriptor table register from register/memory	<b>00001111 00000000 mod 010 r/m</b>	17,19*	1	8,11,12	
SLDT = Store local descriptor table register to register/memory	<b>00001111 00000000 mod 000 r/m</b>	2,6*	1	8	

Shaded areas indicate instructions not available in iAPX 86, 88 microsystems.

## 60266 INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT	CLOCK COUNT		COMMENTS	
		Real Address Mode	Protected Virtual Address Mode	Real Address Mode	Protected Virtual Address Mode
<b>PROTECTION CONTROL (Continued)</b>					
LTR = Local task register from register/memory				17.10*	1 8,11,13
STR = Store task register to register/memory				2.0*	1 9
LMSW = Load machine status word from register/memory				8.0*	8,9
SMSW = Store machine status word				2.0*	8
LAR = Load access rights from register/memory				14.10*	1 8,11,16
LSE = Load segment limit from register/memory				14.10*	1 8,11,16
ADPL = Adjust requested privilege level from register/memory				10.11*	2 8,9
VIRR = Verify read access: register/memory				14.10*	1 8,11,16
VISR = Verify write access				14.10*	1 8,11,16

Shaded areas indicate instructions not available in IAPX 86, 88 microsystems.

## Footnotes

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

- if mod = 11 then r/m is treated as a REG field
- if mod = 00 then DISP = 0\*, disp-low and disp-high are absent
- if mod = 01 then DISP = disp-low sign-extended to 16 bits, disp-high is absent
- if mod = 10 then DISP = disp-high: disp-low
- if r/m = 000 then EA = (BX) + (SI) + DISP
- if r/m = 001 then EA = (BX) + (DI) + DISP
- if r/m = 010 then EA = (BP) + (SI) + DISP
- if r/m = 011 then EA = (BP) + (DI) + DISP
- if r/m = 100 then EA = (SI) + DISP
- if r/m = 101 then EA = (DI) + DISP
- if r/m = 110 then EA = (BP) + DISP\*
- if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

\*except if mod = 00 and r/m = 110 then EQ ← disp-high: disp-low.

REG is assigned according to the following table:

16-Bit (w = 1)		8-Bit (w = 0)	
000	AX	000	AL
001	CX	001	CL
010	DX	010	DL
011	BX	011	BL
100	SP	100	AH
101	BP	101	CH
101	SI	110	OH
111	DI	111	BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

## SEGMENT OVERRIDE PREFIX

0	0	1	reg	1	1	0
---	---	---	-----	---	---	---

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

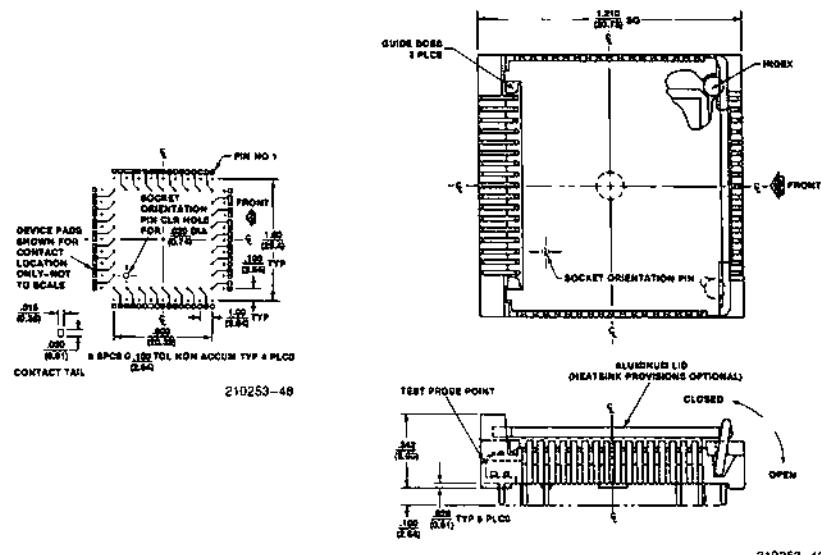
**PC BOARD PATTERN**

Figure 36. Textool 68 Lead Chip Carrier Socket



IAPX 286/10

ADVANCE INFORMATION

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## 80287 80-Bit HMOS NUMERIC PROCESSOR EXTENSION 80287-3

- High Performance 80-Bit Internal Architecture
- Implements Proposed IEEE Floating Point Standard 754
- Expands iAPX 286/10 Datatypes to Include 32-, 64-, 80-Bit Floating Point, 32-, 64-Bit Integers and 18-Digit BCD Operands
- Object Code Compatible with 8087
- Built-in Exception Handling
- Operates in Both Real and Protected Mode iAPX 286 Systems
- Protected Mode Operation Completely Conforms to the iAPX 286 Memory Management and Protection Mechanisms
- Directly Extends iAPX 286/10 Instruction Set to Trigonometric, Logarithmic, Exponential and Arithmetic Instructions for All Datatypes
- 8x80-Bit, Individually Addressable, Numeric Register Stack
- Available in EXPRESS—Standard Temperature Range

The Intel® 80287 is a high performance numerics processor extension that extends the iAPX 286/10 architecture with floating point, extended integer and BCD data types. The iAPX 286/20 computing system (80286 with 80287) fully conforms to the proposed IEEE Floating Point Standard. Using a numerics oriented architecture, the 80287 adds over fifty mnemonics to the iAPX 286/20 instruction set, making the iAPX 286/20 a complete solution for high performance numeric processing. The 80287 is implemented in N-channel, depletion load, silicon gate technology (HMOS) and packaged in a 40-pin ceramic package. The iAPX 286/20 is object code compatible with the iAPX 86/20 and iAPX 88/20.

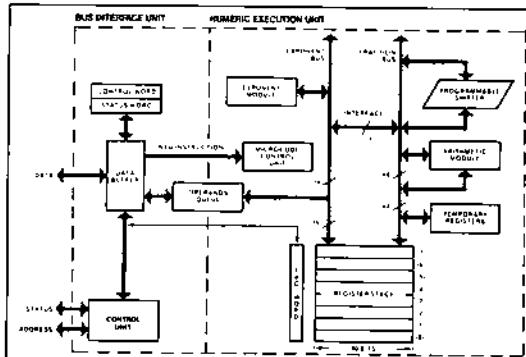
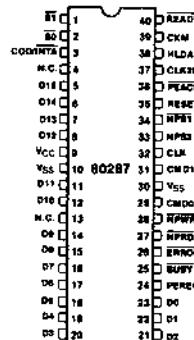


Figure 1. 80287 Block Diagram



NOTE:  
N.C. PINS MUST NOT BE CONNECTED.

Figure 2. 80287 Pin Configuration

Table 1. 80287 Pin Description

Symbols	Type	Name and Function
CLK	I	Clock input: this clock provides the basic timing for internal 80287 operations. Special MOS level inputs are required. The 82284 or 8284A CLK outputs are compatible to this input.
CKM	I	Clock Mode signal: indicates whether CLK input is to be divided by 3 or used directly. A HIGH input will cause CLK to be used directly. This input may be connected to V <sub>CC</sub> or V <sub>SS</sub> as appropriate. This input must be either HIGH or LOW 20 CLK cycles before RESET goes LOW.
RESET	I	System Reset: causes the 80287 to immediately terminate its present activity and enter a dormant state. RESET is required to be HIGH for more than 4 80287 CLK cycles. For proper initialization the HIGH-LOW transition must occur no sooner than 50 µs after V <sub>CC</sub> and CLK meet their D.C. and A.C. specifications.
D15-D0	I/O	Data: 16-bit bidirectional data bus. Inputs to these pins may be applied asynchronous to the 80287 clock.
BUSY	O	Busy status: asserted by the 80287 to indicate that it is currently executing a command.
ERROR	O	Error status: reflects the ES bit of the status word. This signal indicates that an unmasked error condition exists.
PEREQ	O	Processor Extension Data Channel operand transfer request: a HIGH on this output indicates that the 80287 is ready to transfer data. PEREQ will be disabled upon assertion of PEACK or upon actual data transfer, whichever occurs first, if no more transfers are required.
PEACK	I	Processor Extension Data Channel operand transfer ACKnowledge: acknowledges that the request signal (PEREQ) has been recognized. Will cause the request (PEREQ) to be withdrawn in case there are no more transfers required. PEACK may be asynchronous to the 80287 clock.
NPRO	I	Numeric Processor Read: Enables transfer of data from the 80287. This input may be asynchronous to the 80287 clock.
NPWR	I	Numeric Processor Write: Enables transfer of data to the 80287. This input may be asynchronous to the 80287 clock.
NPS1, NPS2	I	Numeric Processor Selects: indicate the CPU is performing an ESCAPE instruction. Concurrent assertion of these signals (i.e., NPS1 is LOW and NPS2 is HIGH) enables the 80287 to perform floating point instructions. No data transfers involving the 80287 will occur unless the device is selected via these lines. These inputs may be asynchronous to the 80287 clock.
CMD1, CMD0	I	Command lines: These, along with select inputs, allow the CPU to direct the operation of the 80287. These inputs may be asynchronous to the 80287 clock.

Table 1. 80287 Pin Description (cont.)

Symbols	Type	Name and Function
CLK286	I	CPU Clock: This input provides a sampling edge for the 80287 inputs S1, S0, COD/INTA, READY, and HLDA. It must be connected to the 80286 CLK input.
<u>S1, S0</u> COD/INTA	I	Status: These inputs must be connected to the corresponding 80286 pins.
HLDA	I	Hold Acknowledge: This input informs the 80287 when the 80286 controls the local bus. It must be connected to the 80286 HLDA output.
READY	I	Ready: The end of a bus cycle is signaled by this input. It must be connected to the 80286 READY input.
VSS	I	System ground, both pins must be connected to ground.
VCC	I	+5V supply

## FUNCTIONAL DESCRIPTION

The 80287 Numeric Processor Extension (NPX) provides arithmetic instructions for a variety of numeric data types in iAPX 286/20 systems. It also executes numerous built-in transcendental functions (e.g., tangent and log functions). The 80287 executes instructions in parallel with a 80286. It

effectively extends the register and instruction set of an iAPX 286/10 system for existing iAPX 286 data types and adds several new data types as well. Figure 3 presents the program visible register model of the iAPX 286/20. Essentially, the 80287 can be treated as an additional resource or an extension to the iAPX 286/10 that can be used as a single unified system, the iAPX 286/20.

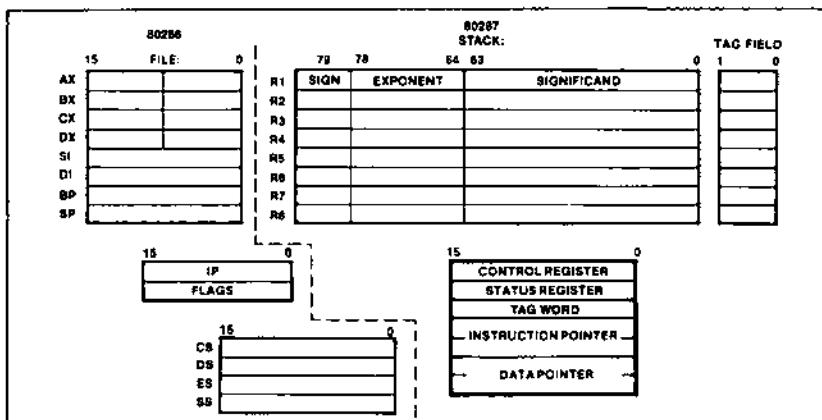


Figure 3. IAPX 286/20 Architecture

The 80287 has two operating modes similar to the two modes of the 80286. When reset, 80287 is in the real address mode. It can be placed in the protected virtual address mode by executing the SETPM ESC instruction. The 80287 cannot be switched back to the real address mode except by reset. In the real address mode, the iAPX 286/20 is completely software compatible with iAPX 86/20, 88/20.

Once in protected mode, all references to memory for numerics data or status information, obey the iAPX 286 memory management and protection rules giving a fully protected extension of the 80286 CPU. In the protected mode, iAPX 286/20 numerics software is also completely compatible with iAPX 86/20 and iAPX 88/20.

### SYSTEM CONFIGURATION

As a processor extension to an 80286, the 80287 can be connected to the CPU as shown in Figure 4. The data channel control signals (PEREQ, PEACK), the BUSY signal and the NPPD, NPWR signals, allow the NPX to receive instructions and data from the CPU. When in the protected mode, all information received by the NPX is validated by the 80286 memory management and protection unit. Once started, the 80287 can process in parallel with and independent of the host CPU. When the NPX detects an error or exception, it will indicate this to the CPU by asserting the ERROR signal.

The NPX uses the processor extension request and acknowledge pins of the 80286 CPU to implement data transfers with memory under the protection model of the CPU. The full virtual and physical address space of the 80286 is available. Data for the 80287 in memory is addressed and represented in the same manner as for an 8087.

The 80287 can operate either directly from the CPU clock or with a dedicated clock. For operation with the CPU clock ( $CKM=0$ ), the 80287 works at one-third the frequency of the system clock (i.e., for an 8 MHz 80286, the 16 MHz system clock is divided down to 5.3 MHz). The 80287 provides a capability to internally divide the CPU clock by three to produce the required internal clock (33% duty cycle). To use a higher performance 80287 (8 MHz), an 8284A clock driver and appropriate crystal may be used to directly drive the 80287 with a 1/3 duty cycle clock on the CLK input ( $CKM=1$ ).

### HARDWARE INTERFACE

Communication of instructions and data operands between the 80286 and 80287 is handled by the CMD0, CMD1, NPST, NPS2, NPPD, and NPWR signals. I/O port addresses 00F8H, 00FAH, and 00FCH are used by the 80286 for this communication. When any of these addresses are used, the NPST input must be LOW and NPS2 input HIGH. The IORC and IOWC outputs of the 82288 identify I/O space transfers (see Figure 4). CMD0 should be connected to latched 80286 A1 and CMD1 should be connected to latched 80286 A2. The ST, S0, COD/INTA/READY, HLDA, and CLK pins of the 80286 are connected to the same named pins on the 80287.

I/O ports 00F8H to 00FFH are reserved for the 80286/80287 interface. To guarantee correct operation of the 80287, programs must not perform any I/O operations to these ports.

The PEREQ, PEACK, BUSY, and ERROR signals of the 80287 are connected to the same-named 80286 input. The data pins of the 80287 should be directly connected to the 80286 data bus. Note that all bus drivers connected to the 80286 local bus must be inhibited when the 80286 reads from the 80287. The use of COD/INTA and M/I/O in the decoder prevents INTA bus cycles from disabling the data transceivers.

### PROGRAMMING INTERFACE

Table 2 lists the seven data types the 80287 supports and presents the format for each type. These values are stored in memory with the least significant digits at the lowest memory address. Programs retrieve these values by generating the lowest address. All values should start at even addresses for maximum system performance.

Internally the 80287 holds all numbers in the temporary real format. Load instructions automatically convert operands represented in memory as 16-, 32-, or 64-bit integers, 32- or 64-bit floating point number or 18-digit packed BCD numbers into temporary real format. Store instructions perform the reverse type conversion.

80287 computations use the processor's register stack. These eight 80-bit registers provide the equivalent capacity of 40 16-bit registers. The 80287 register set can be accessed as a stack, with

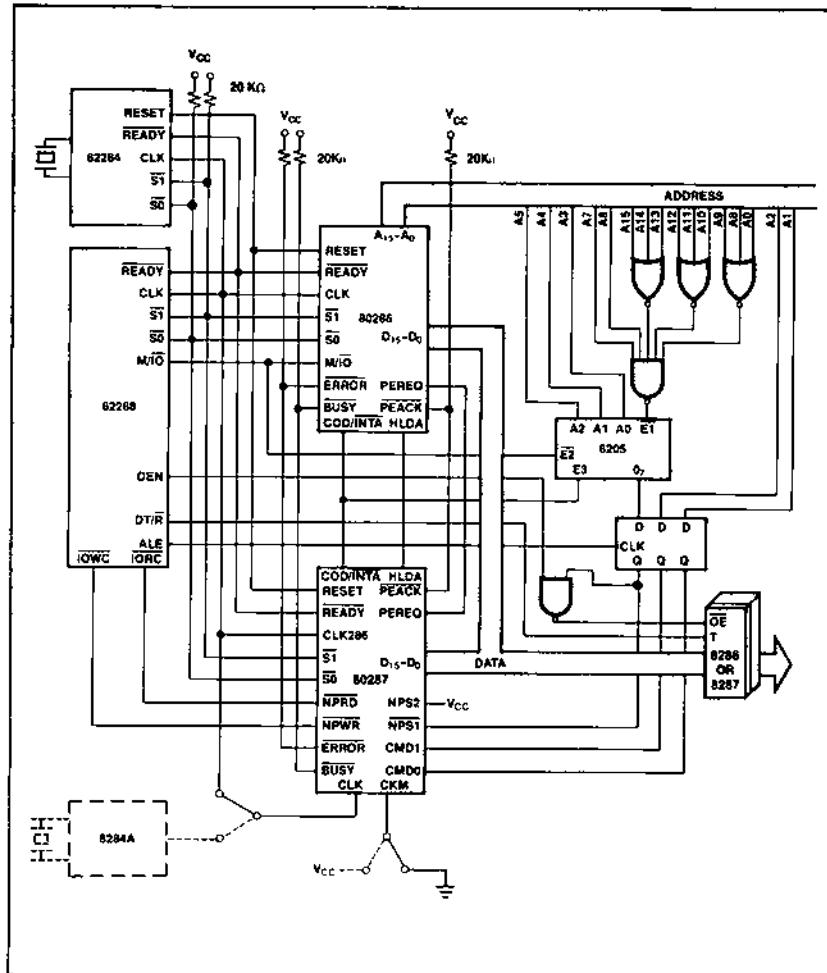


Figure 4. IAPX 286/20 System Configuration

Table 2. 80287 Datatype Representation in Memory

Data Formats	Range	Precision	Most Significant Byte														HIGHEST ADDRESSED BYTE																
			7	0	7	0	7	0	7	0	7	0	7	0	7	0	7	0	7	0	7	0	7	0	7	0	7	0					
Word Integer	$10^4$	16 Bits	S	MAGNITUDE	[TWO'S COMPLEMENT]																												
Short Integer	$10^9$	32 Bits	S	MAGNITUDE	[TWO'S COMPLEMENT]																												
Long Integer	$10^{19}$	64 Bits	S	MAGNITUDE	[TWO'S COMPLEMENT]																												
Packed BCD	$10^{18}$	18 Digits	S	X	$d_{17}, d_{16}, d_{15}, d_{14}, d_{13}, d_{12}, d_{11}, d_{10}, d_9, d_8, d_7, d_6, d_5, d_4, d_3, d_2, d_1, d_0$	MAGNITUDE																											
Short Real	$10^{\pm 38}$	24 Bits	S	BIASED EXPONENT	SIGNIFICAND																												
Long Real	$10^{\pm 308}$	53 Bits	S	BIASED EXPONENT	SIGNIFICAND																												
Temporary Real	$10^{\pm 4932}$	64 Bits	S	BIASED EXPONENT	I	SIGNIFICAND																											

**NOTES:**

- (1) S = Sign bit (0 = positive, 1 = negative)
- (2)  $d_n$  = Decimal digit (two per byte)
- (3) X = Bits have no significance; 8087 ignores them when loading, zeros when storing.
- (4)  $\downarrow$  = Position of implicit binary point
- (5) I = Integer bit of significand; stored in temporary real, implicit in short and long real

**(6) Exponent Bias (normalized values):**

- Short Real: 127 (7FH)  
Long Real: 1023 (3FFH)  
Temporary Real: 16383 (FFFH)

**(7) Packed BCD:  $(-1)^S(D_{17} \dots D_0)$** **(8) Real:  $(-1)^S(2^{E-BIAS})(F_0 F_1 \dots)$** 

instructions operating on the top one or two stack elements, or as a fixed register set, with instructions operating on explicitly designated registers.

Table 6 lists the 80287's instructions by class. No special programming tools are necessary to use the 80287 since all new instructions and data types are directly supported by the iAPX 286 assembler

and appropriate high level languages. All iAPX 86/88 development tools which support the 8087 can also be used to develop software for the iAPX 286/20 in real address mode.

Table 3 gives the execution times of some typical numeric instructions.

**Table 3. Execution Time for Selected 80287 Instructions**

Floating Point Instruction	Approximate Execution Time (μs)
	80287 (5 MHz Operation)
Add/Subtract	14/18
Multiply (single precision)	19
Multiply (extended precision)	27
Divide	39
Compare	9
Load (double precision)	10
Store (double precision)	21
Square Root	36
Tangent	90
Exponentiation	100

**SOFTWARE INTERFACE**

The iAPX 286/20 is programmed as a single processor. All communication between the 80286 and the 80287 is transparent to software. The CPU automatically controls the 80287 whenever a numeric instruction is executed. All memory addressing modes, physical memory, and virtual memory of the CPU are available for use by the NPX.

Since the NPX operates in parallel with the CPU, any errors detected by the NPX may be reported after the CPU has executed the ESCAPE instruction which caused it. To allow identification of the failing numeric instruction, the NPX contains two pointer registers which identify the address of the failing numeric instruction and the numeric memory operand if appropriate for the instruction encountering this error.

**INTERRUPT DESCRIPTION**

Several interrupts of the iAPX 286 are used to report exceptional conditions while executing numeric programs in either real or protected mode. The interrupts and their functions are shown in Table 4.

**PROCESSOR ARCHITECTURE**

As shown in Figure 1, the NPX is internally divided into two processing elements, the bus interface unit (BIU) and the numeric execution unit (NEU). The NEU executes all numeric instructions, while the BIU receives and decodes instructions, requests operand transfers to and from memory and executes processor control instructions. The two units are able to operate independently of one another allowing the BIU to maintain asynchronous communication with the CPU while the NEU is busy processing a numeric instruction.

**BUS INTERFACE UNIT**

The BIU decodes the ESC instruction executed by the CPU. If the ESC code defines a math instruction, the BIU transmits the formatted instruction to the NEU. If the ESC code defines an administrative instruction, the BIU executes it independently of the NEU. The parallel operation of the NPX with the CPU is normally transparent to the user. The BIU generates the BUSY and ERROR signals for 8086/80287 processor synchronization and error notification, respectively.

The 80287 executes a single numeric instruction at a time. When executing most ESC instructions, the

Table 4. 80286 Interrupt Vectors Reserved for NPX

Interrupt Number	Interrupt Function
7	An ESC instruction was encountered when EM or TS of the 80286 MSW was set. EM=1 indicates that software emulation of the instruction is required. When TS is set, either an ESC or WAIT instruction will cause interrupt 7. This indicates that the current NPX context may not belong to the current task.
9	The second or subsequent words of a numeric operand in memory exceeded a segment's limit. This interrupt occurs after executing an ESC instruction. The saved return address will not point at the numeric instruction causing this interrupt. After processing the addressing error, the iAPX 286 program can be restarted at the return address with IRET. The address of the failing numeric instruction and numeric operand are saved in the 80287. An interrupt handler for this interrupt must execute FNINIT before any other ESC or WAIT instruction.
13	The starting address of a numeric operand is not in the segment's limit. The return address will point at the ESC instruction, including prefixes, causing this error. The 80287 has not executed this instruction. The instruction and data address in 80287 refer to a previous, correctly executed, instruction.
16	The previous numeric instruction caused an unmasked numeric error. The address of the faulty numeric instruction or numeric data operand is stored in the 80287. Only ESC or WAIT instructions can cause this interrupt. The 80286 return address will point at a WAIT or ESC instruction, including prefixes, which may be restarted after clearing the error condition in the NPX.

80286 tests the BUSY pin and waits until the 80287 indicates that it is not busy before initiating the command. Once initiated, the 80286 continues program execution while the 80287 executes the ESC instruction. In iAPX 86/20 systems, this synchronization is achieved by placing a WAIT instruction before an ESC instruction. For most ESC instructions, the iAPX 286/20 does not require a WAIT instruction before the ESC opcode. However, the iAPX 286/20 will operate correctly with these WAIT instructions. In all cases, a WAIT or ESC instruction should be inserted after any 80287 store to memory (except FSTSW and FSTCW) or load from memory (except FLDENV or FRSTOR) before the 80286 reads or changes the value to be sure the numeric value has already been written or read by the NPX.

Data transfers between memory and the 80287, when needed, are controlled by the PEREQ, PEACK, NPROD, NPWR, NPS1, NPS2 signals. The 80286 does the actual data transfer with memory through its processor extension data channel. Numeric data transfers with memory performed by the 80286 use the same timing as any other bus

cycle. Control signals for the 80287 are generated by the 8086 as shown in Figure 4, and meet the timing requirements shown in the AC requirements section.

#### NUMERIC EXECUTION UNIT

The NEU executes all instructions that involve the register stack; these include arithmetic, logical, transcendental, constant and data transfer instructions. The data path in the NEU is 84 bits wide (68 significant bits, 15 exponent bits and a sign bit) which allows internal operand transfers to be performed at very high speeds.

When the NEU begins executing an instruction, it activates the BiU BUSY signal. This signal is used in conjunction with the CPU WAIT instruction or automatically with most of the ESC instructions to synchronize both processors.

#### REGISTER SET

The 80287 register set is shown in Figure 5. Each of the eight data registers in the 8087's register stack

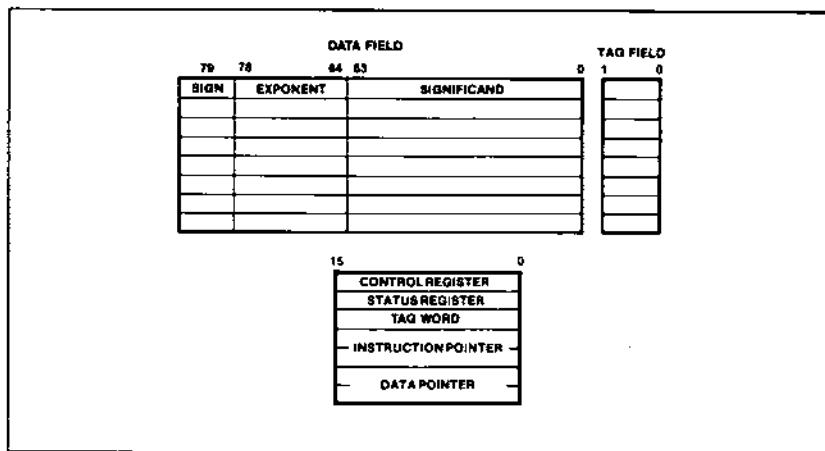


Figure 5. 80287 Register Set

is 80 bits wide and is divided into "fields" corresponding to the NPX's temporary real data type.

At a given point in time the TOP field in the status word identifies the current top-of-stack register. A "push" operation decrements TOP by 1 and loads a value into the new top register. A "pop" operation stores the value from the current top register and then increments TOP by 1. Like 80286 stacks in memory, the 80287 register stack grows "down" toward lower-addressed registers.

Instructions may address the data registers either implicitly or explicitly. Many instructions operate on the register at the TOP of the stack. These instructions implicitly address the register pointed by the TOP. Other instructions allow the programmer to explicitly specify the register which is to be used. This explicit register addressing is also "top-relative."

#### STATUS WORD

The 16-bit status word (in the status register) shown in Figure 5 reflects the overall state of the 80287. It may be read and inspected by CPU code. The busy bit (bit 15) indicates whether the NEU is executing an instruction ( $B = 1$ ) or is idle ( $B = 0$ ).

The instructions FSTSW, FSTSW AX, FSTENV, and FSAVE which store the status word are executed exclusively by the BIU and do not set the busy bit themselves or require the Busy bit be cleared in order to be executed.

The four numeric condition code bits ( $C_0-C_3$ ) are similar to the flags in a CPU: instructions that perform arithmetic operations update these bits to reflect the outcome of NPX operations. The effect of these instructions on the condition code bits is summarized in Tables 5a and 5b.

Bits 14-12 of the status word point to the 80287 register that is the current top-of-stack (TOP) as described above. Figure 6 shows the six error flags in bits 5-0 of the status word. Bits 5-0 are set to indicate that the NEU has detected an exception while executing an instruction. The section on exception handling explains how they are set and used.

Bit 7 is the error summary status bit. This bit is set if any unmasked exception bit is set and cleared otherwise. If this bit is set, the ERROR signal is asserted.

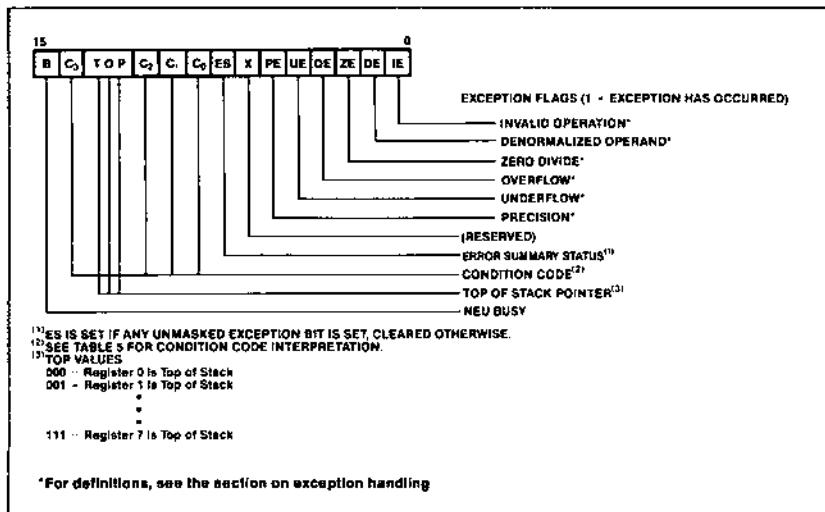


Figure 6. 80287 Status Word

#### TAG WORD

The tag word marks the content of each register as shown in Figure 7. The principal function of the tag word is to optimize the NPX's performance. The eight two-bit tags in the tag word can be used, however, to interpret the contents of 80287 registers.

#### INSTRUCTION AND DATA POINTERS

The instruction and data pointers (See Figures 8a and 8b) are provided for user-written error handlers. Whenever the 80287 executes a new instruction, the BIU saves the instruction address, the operand address (if present) and the instruction opcode. 80287 instructions can store this data into memory.

The instruction and data pointers appear in one of two formats depending on the operating mode of the 80287. In real mode, these values are the 20-bit physical address and 11-bit opcode formatted like the 8087. In protected mode, these values are the 32-bit virtual addresses used by the program

which executed an ESC instruction. The same FLDENV/FSTENV/FSAVE/FRSTOR instructions as those of the 8087 are used to transfer these values between the 80287 registers and memory.

The saved instruction address in the 80287 will point at any prefixes which preceded the instruction. This is different than in the 8087 which only pointed at the ESCAPE instruction opcode.

#### CONTROL WORD

The NPX provides several processing options which are selected by loading a word from memory into the control word. Figure 9 shows the format and encoding of fields in the control word.

The low order byte of this control word configures the 80287 error and exception masking. Bits 5-0 of the control word contain individual masks for each of the six exceptions that the 80287 recognizes. The high order byte of the control word configures the 80287 operating mode including precision,

Table 5a. Condition Code Interpretation

Instruction Type	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>	Interpretation
Compare, Test	0	0	X	0	ST > Source or 0 (FTST)
	0	0	X	1	ST < Source or 0 (FTST)
	1	0	X	0	ST = Source or 0 (FTST)
	1	1	X	1	ST is not comparable
Remainder	Q <sub>1</sub>	0	Q <sub>0</sub>	Q <sub>2</sub>	Complete reduction with three low bits of quotient (See Table 5b)
	U	1	U	U	Incomplete Reduction
Examine	0	0	0	0	Valid, positive unnormalized
	0	0	0	1	Invalid, positive, exponent = 0
	0	0	1	0	Valid, negative, unnormalized
	0	0	1	1	Invalid, negative, exponent = 0
	0	1	0	0	Valid, positive, normalized
	0	1	0	1	Infinity, positive
	0	1	1	0	Valid, negative, normalized
	0	1	1	1	Infinity, negative
	1	0	0	0	Zero, positive
	1	0	0	1	Empty
	1	0	1	0	Zero, negative
	1	0	1	1	Empty
	1	1	0	0	Invalid, positive, exponent = 0
	1	1	0	1	Empty
	1	1	1	0	Invalid, negative, exponent = 0
	1	1	1	1	Empty

**NOTES:**

1. ST = Top of stack
2. X = value is not affected by instruction
3. U = value is undefined following instruction
4. Q<sub>n</sub> = Quotient bit n

Table 5b. Condition Code Interpretation after FPREM Instruction As a Function of Dividend Value

Dividend Range	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
Dividend < 2 * Modulus	C <sub>3</sub>	C <sub>1</sub>	Q <sub>0</sub>
Dividend < 4 * Modulus	C <sub>3</sub>	Q <sub>1</sub>	Q <sub>0</sub>
Dividend ≥ 4 * Modulus	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>

**NOTE:**

1. Previous value of indicated bit, not affected by FPREM instruction execution.

rounding, and infinity control. The precision control bits (bits 9-8) can be used to set the 80287 internal operating precision at less than the default of temporary real (80-bit) precision. This can be useful in providing compatibility with the early generation arithmetic processors of smaller precision than the 80287. The rounding control bits (bits 11-10) provide for directed rounding and true chop as well as the unbiased round to nearest even mode specified in the IEEE standard. Control over closure of the number space at infinity is also provided (either affine closure:  $\pm \infty$ , or projective closure:  $\infty$ , is treated as unsigned, may be specified).

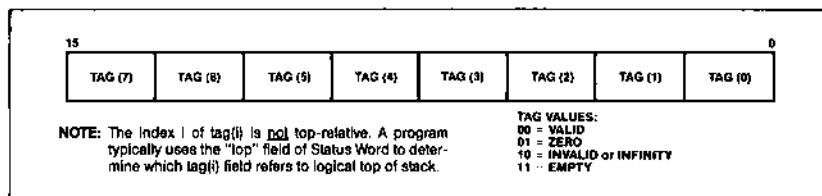


Figure 7. 80287 Tag Word

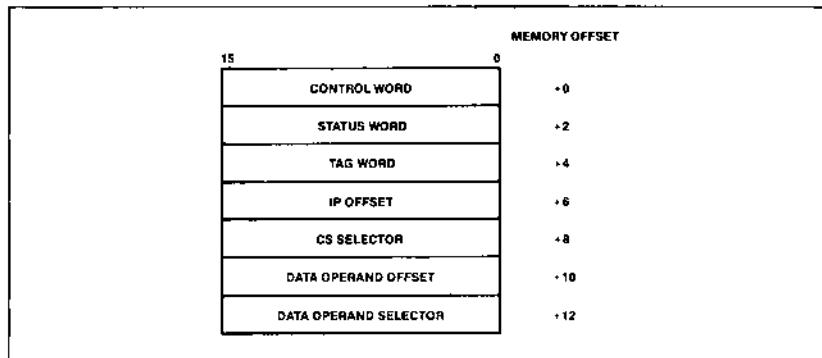


Figure 8a. Protected Mode 80287 Instruction and Data Pointer Image in Memory

### EXCEPTION HANDLING

The 80287 detects six different exception conditions that can occur during instruction execution. Any or all exceptions will cause the assertion of external ERROR signal and ES bit of the Status Word if the appropriate exception masks are not set.

The exceptions that the 80287 detects and the 'default' procedures that will be carried out if the exception is masked, are as follows:

**Invalid Operation:** Stack overflow, stack underflow, indeterminate form (0/0,  $\infty$ ,  $-\infty$ , etc) or the use of a Non-Number (NAN) as an operand. An exponential value of all ones and non-zero significand is reserved to identify NaNs. If this exception is masked, the 80287 default response is to generate a specific NAN called

INDEFINITE, or to propagate already existing NaNs as the calculation result.

**Overflow:** The result is too large in magnitude to fit the specified format. The 80287 will generate an encoding for infinity if this exception is masked.

**Zero Divisor:** The divisor is zero while the dividend is a non-infinite, non-zero number. Again, the 80287 will generate an encoding for infinity if this exception is masked.

**Underflow:** The result is non-zero but too small in magnitude to fit in the specified format. If this exception is masked the 80287 will denormalize (shift right) the fraction until the exponent is in range. The process is called gradual underflow.

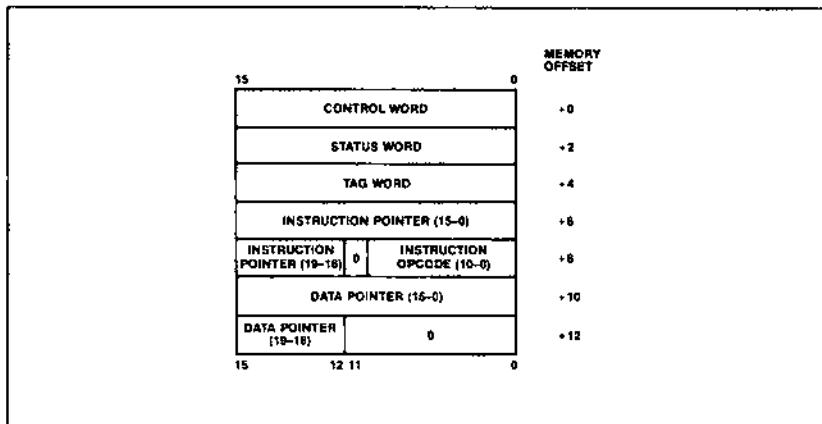


Figure 8b. Real Mode 80287 Instruction and Data Pointer Image in Memory

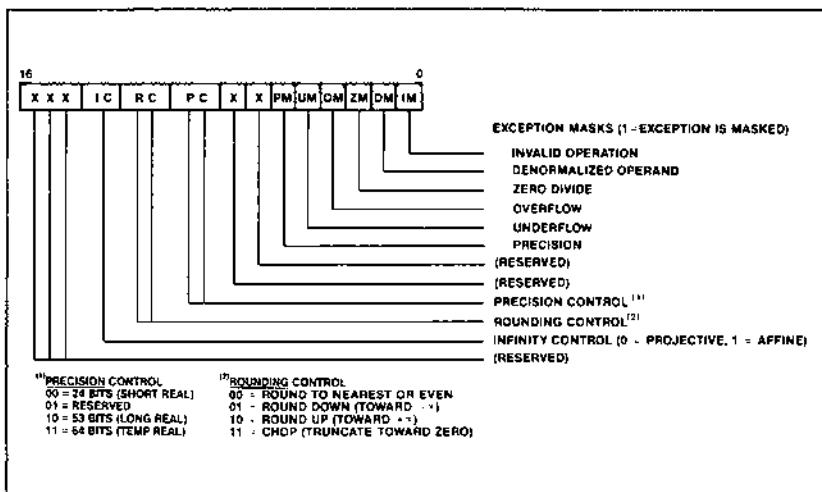


Figure 9. 80287 Control Word

**Denormalized Operand:** At least one of the operands is denormalized; it has the smallest exponent but a non-zero significand. Normal processing continues if this exception is masked off.

**Inexact Result:** The true result is not exactly representable in the specified format; the result is rounded according to the rounding mode, and this flag is set. If this exception is masked, processing will simply continue.

If the error is not masked, the corresponding error bit and the error status bit (ES) in the control word will be set, and the ERROR output signal will be asserted. If the CPU attempts to execute another ESC or WAIT instruction, exception 7 will occur.

The error condition must be resolved via an interrupt service routine. The 80287 saves the address of the floating point instruction causing the error as well as the address of the lowest memory location of any memory operand required by that instruction.

#### IAPX 86/20 COMPATIBILITY:

IAPX 286/20 supports portability of IAPX 86/20 programs when it is in the real address mode. However, because of differences in the numeric error handing techniques, error handling routines may need to be changed. The differences between an IAPX 286/20 and IAPX 86/20 are:

1. The NPX error signal does not pass through an interrupt controller (8087 INT signal does).

Therefore, any interrupt controller oriented instructions for the IAPX 86/20 may have to be deleted.

2. Interrupt vector 16 must point at the numeric error handler routine.
3. The saved floating point instruction address in the 80287 includes any leading prefixes before the ESCAPE opcode. The corresponding saved address of the 8087 does not include leading prefixes.
4. In protected mode, the format of the saved instruction and operand pointers is different than for the 8087. The instruction opcode is not saved—it must be read from memory if needed.
5. Interrupt 7 will occur when executing ESC instructions with either TS or EM of MSW=1. If TS of MSW=1 then WAIT will also cause interrupt 7. An interrupt handler should be added to handle this situation.
6. Interrupt 9 will occur if the second or subsequent words of a floating point operand fall outside a segment's size. Interrupt 13 will occur if the starting address of a numeric operand falls outside a segment's size. An interrupt handler should be added to report these programming errors.

In the protected mode, IAPX 86/20 application code can be directly ported via recompilation if the 286 memory protection rules are not violated.

**ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature Under Bias ... 0°C to 70°C  
 Storage Temperature ..... -65°C to +150°C  
 Voltage on Any Pin with  
 Respect to Ground ..... -1.0 to +7V  
 Power Dissipation ..... 3.0 Watt

\*NOTICE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D.C. CHARACTERISTICS  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5\text{V}, +/-5\%$** 

5 MHz

Symbol	Parameter	-3 Min	-3 max	Unit	Test Conditions
$V_{IL}$	Input LOW Voltage	-5	.8	V	
$V_{IH}$	Input HIGH Voltage	2.0	$V_{CC} + .5$	V	
$V_{ILC}$	Clock Input LOW Voltage CKM = 1: CKM = 0:	.5 .5	.8 .6	V V	
$V_{IHC}$	Clock Input HIGH Voltage CKM = 1: CKM = 0:	2.0 3.8	$V_{CC} + 1$ $V_{CC} + 1$	V V	
$V_{OL}$	Output LOW Voltage		.45	V	$I_{OL} = 3.0 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.4		V	$I_{OH} = -400 \mu\text{A}$
$I_{IU}$	Input Leakage Current	.	$\pm 10$	$\mu\text{A}$	$0\text{V} \leq V_{IN} \leq V_{CC}$
$I_{LO}$	Output Leakage Current	.	$\pm 10$	$\mu\text{A}$	$.45\text{V} \leq V_{OUT} \leq V_{CC}$
$I_{CC}$	Power Supply Current	.	475	mA	
$C_{IN}$	Input Capacitance	.	10	pF	$F_C = 1 \text{ MHz}$
$C_O$	Input/Output Capacitance (D0-D15)	.	20	pF	$F_C = 1 \text{ MHz}$
$C_{CLK}$	CLK Capacitance	.	12	pF	$F_C = 1 \text{ MHz}$

**A.C. CHARACTERISTICS** ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} + 5\text{V}, +/- 5\%$ )

**TIMING REQUIREMENTS**

A.C. timings are referenced to 0.8V and 2.0V points on signals unless otherwise noted.

5 MHz

Symbol	Parameter	-3 Min	-3 max	Unit	Test Conditions
$T_{CLCL}$	CLK Period CKM = 1; CKM = 0;	200 62.5	500 250	ns ns	
$T_{CLCH}$	CLK LOW Time CKM = 1; CKM = 0;	118 15	230	ns ns	At 0.8V At 0.6V
$T_{CHCL}$	CLK HIGH Time CKM = 1; CKM = 0;	69 20	235	ns ns	At 2.0V At 3.8V
$T_{CH1CH2}$	CLK Rise Time	.	10	ns	1.0V to 3.5V if CKM = 1.
$T_{CL2CL1}$	CLK Fall Time	.	10	ns	3.5V to 1.0V if CKM = 1.
$T_{DWHH}$	Data Setup to <b>NPWR</b> Inactive	75	.	ns	
$T_{WHDX}$	Data Hold from <b>NPWR</b> Inactive	30	.	ns	
$T_{WLWH}, T_{RLRH}$	<b>NPWR</b> , <b>NPRD</b> Active Time	95	.	ns	At 0.8V
$T_{AVRL}, T_{AWL}$	Command Valid to <b>NPWR</b> or <b>NPRD</b> Active	0	.	ns	
$T_{MHRL}$	Minimum Delay from PEREQ Active to <b>NPRD</b> Active	130	.	ns	
$T_{KLKH}$	<b>PEACK</b> Active Time	85	.	ns	At 0.8V
$T_{KHKL}$	<b>PEACK</b> Inactive Time	250	.	ns	At 2.0V
$T_{KHCH}$	<b>PEACK</b> Inactive to <b>NPWR</b> , <b>NPRD</b> Inactive	50	.	ns	
$T_{CHKL}$	<b>NPWR</b> , <b>NPRD</b> Inactive to <b>PEACK</b> Active	-30	.	ns	
$T_{WHAX}, T_{AHAX}$	Command Hold from <b>NPWR</b> , <b>NPRD</b> Inactive	30	.	ns	
$T_{KLCL}$	<b>PEACK</b> Active Setup to <b>NPWR</b> , <b>NPRD</b> Active	50	.	ns	
$T_{2CLCL}$	CLK286 Period	62.5	.	ns	
$T_{2CLCH}$	CLK286 LOW Time	15	.	ns	At 0.8V
$T_{2CHCL}$	CLK286 HIGH Time	20	.	ns	At 2.0V
$T_{2SWCL}$	<b>SO</b> , <b>ST</b> Setup Time to CLK286	22.5	.	ns	
$T_{2CLSH}$	<b>SO</b> , <b>ST</b> Hold Time from CLK286	0	.	ns	

**A.C. CHARACTERISTICS, continued**  
**TIMING REQUIREMENTS**
**5 MHz**

Symbol	Parameter	-3 Min	-3 max	Unit	Test Conditions
$T_{CIVCL}$	COD/INTA Setup Time to CLK286	0	.	ns	
$T_{CLCIH}$	COD/INTA Hold Time from CLK286	0	.	ns	
$T_{RVCL}$	READY Setup Time to CLK286	38.5	.	ns	
$T_{CLRH}$	READY Hold Time from CLK286	25	.	ns	
$T_{HVCL}$	HLDA Setup Time to CLK286	0	.	ns	
$T_{CLHH}$	HLDA Hold Time from CLK286	0	.	ns	
$T_{IVCL}$	NPWR, NPROD to CLK Setup Time	70	.	ns	NOTE 1
$T_{CLIH}$	NPWR, NPROD from CLK Hold Time	45	.	ns	NOTE 1
$T_{RSCL}$	RESET to CLK Setup Time	20	.	ns	NOTE 1
$T_{CLRS}$	RESET from CLK Hold Time	20	.	ns	NOTE 1

**A.C. CHARACTERISTICS,**  
**TIMING RESPONSES**
**5 MHz**

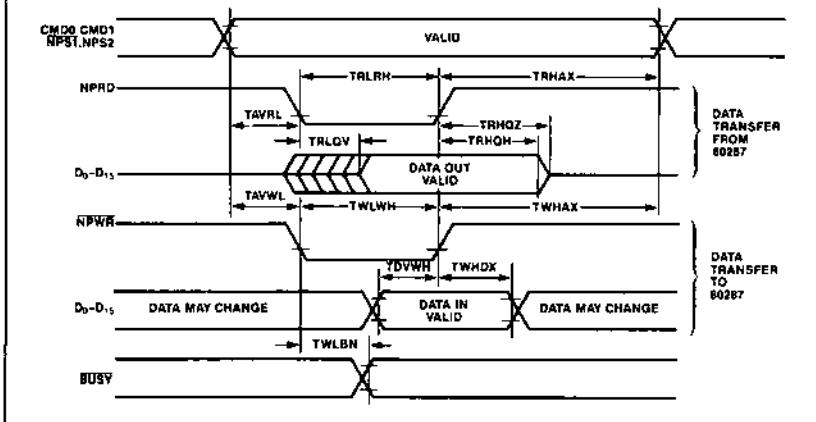
Symbol	Parameter	-3 Min	-3 max	Unit	Test Conditions
$T_{RHQZ}$	NPROD Inactive to Data Float	.	37.5	ns	NOTE 2
$T_{RLQV}$	NPROD Active to Data Valid	.	60	ns	NOTE 3
$T_{ILSH}$	ERROR Active to BUSY Inactive	100	.	ns	NOTE 4
$T_{WLBV}$	NPWR Active to BUSY Active	.	100	ns	NOTE 5
$T_{KLML}$	PEACK Active to PEREQ Inactive	.	127	ns	NOTE 6
$T_{CMDI}$	Command Inactive Time Write-to-Write Read-to-Read Write-to-Read Read-to-Write	95 250 105 95	.	ns	At 2.0V
$T_{RHQH}$	Data Hold from NPROD Inactive	5	.	ns	NOTE 7

**NOTES:**

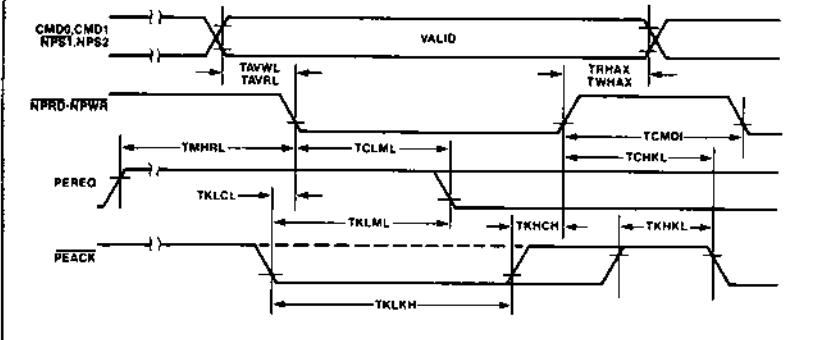
1. This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at a specific CLK edge.
2. Float condition occurs when output current is less than  $I_{LO}$  on D0-D15.
3. D0-D15 loading: CL = 100pF
4. BUSY loading: CL = 100pF
5. BUSY loading: CL = 100pF
6. On last data transfer of numeric instruction.
7. D0-D15 loading: CL = 100pF

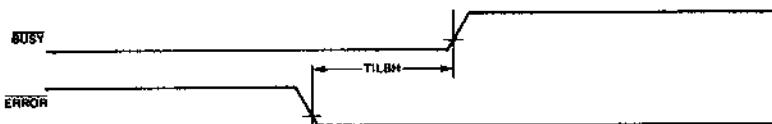
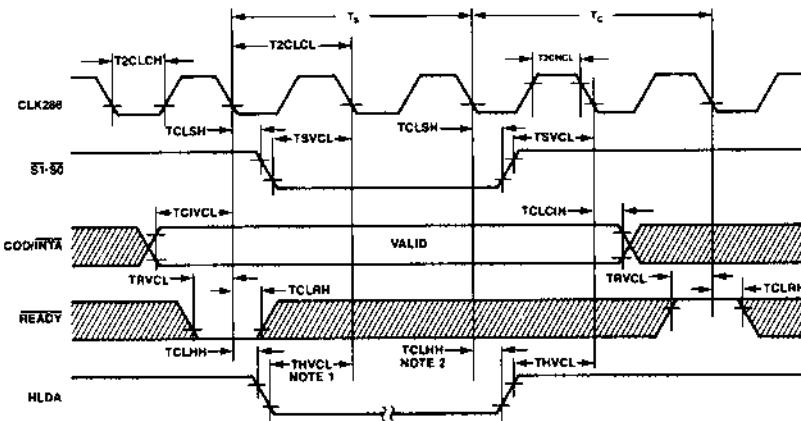
## WAVEFORMS (cont.)

## DATA TRANSFER TIMING (INITIATED BY 80287)



## DATA CHANNEL TIMING (INITIATED BY 80287)



**WAVEFORMS (cont.)****ERROR OUTPUT TIMING****80286 STATUS TIMING****NOTES:**

1. This input transition occurs before  $T_s$ .
2. This input transition occurs after  $T_c$ .

**WAVEFORMS**

(Reset, NPWD, NPROD are inputs asynchronous to CLK. Timing requirements on this page are given for testing purposes only, to assure recognition of a specific CLK edge.)

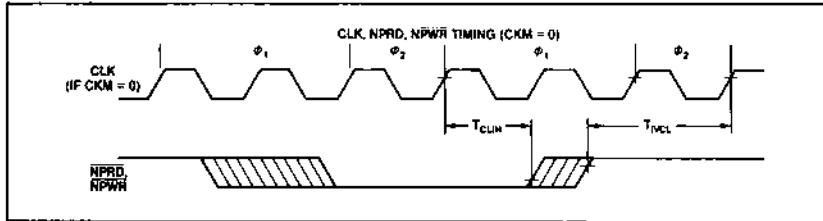
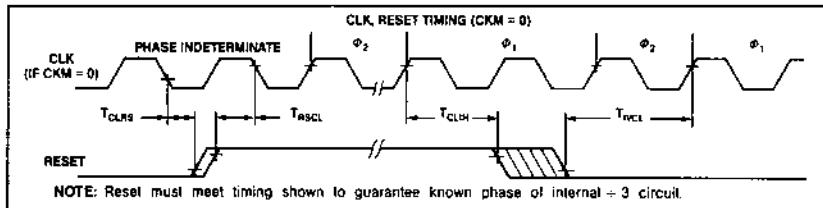
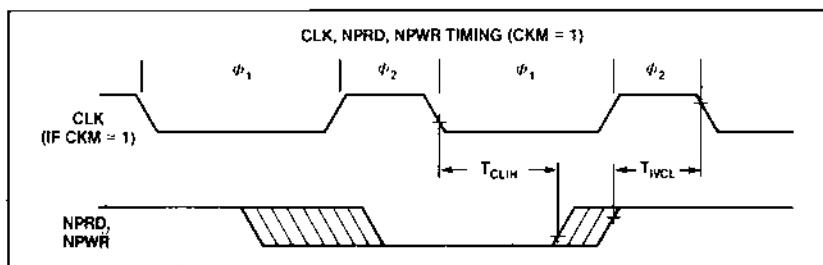
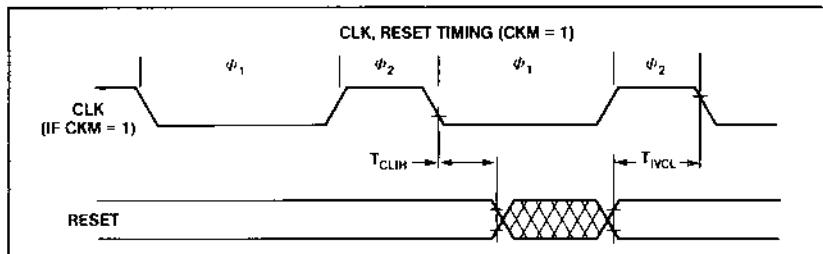


Table 6. 80287 Extensions to the 80286 Instruction Set

Data Transfer	MF	-	Optional 8,16 Bit Displacement	Clock Count Range			
				32 Bit Real	32 Bit Integer	64 Bit Real	16 Bit Integer
<b>FLD = LOAD</b>	MF	-		00	01	10	11
Integer/Real Memory to ST(0)	ESCAPE	MF 1	MOD 0 0 0 R/M	DISP	36-56	52-60	40-60
Long Integer Memory to ST(0)	ESCAPE	1 1 1	MOD 1 0 1 R/M	DISP	60-68		
Temporary Real Memory to ST(0)	ESCAPE	0 1 1	MOD 1 0 1 R/M	DISP	53-65		
BCD Memory to ST(0)	ESCAPE	1 1 1	MOD 1 0 0 R/M	DISP	290-310		
ST(i) to ST(0)	ESCAPE	0 0 1	1 1 0 0 0 ST(i)		17-22		
<b>FST = STORE</b>							
ST(0) to Integer/Real Memory	ESCAPE	MF 1	MOD 0 1 0 R/M	DISP	84-90	82-92	96-104
ST(0) to ST(i)	ESCAPE	1 0 1	1 1 0 1 0 ST(i)		15-22		
<b>FSTP = STORE AND POP</b>							
ST(0) to Integer/Real Memory	ESCAPE	MF 1	MOD 0 1 1 R/M	DISP	66-92	64-94	98-106
ST(0) to Long Integer Memory	ESCAPE	1 1 1	MOD 1 1 1 R/M	DISP	94-105		
ST(0) to Temporary Real Memory	ESCAPE	0 1 1	MOD 1 1 1 R/M	DISP	52-58		
ST(0) to BCD Memory	ESCAPE	1 1 1	MOD 1 1 0 R/M	DISP	920-540		
ST(0) to ST(i)	ESCAPE	1 0 1	1 1 0 1 1 ST(i)		17-24		
<b>FXCH = Exchange ST(i) and ST(0)</b>	ESCAPE	0 0 1	1 1 0 0 1 ST(i)		10-15		
<b>Comparison</b>							
<b>FCOM = Compare</b>							
Integer/Real Memory to ST(0)	ESCAPE	MF 0	MOD 0 1 0 R/M	DISP	60-70	78-91	65-75
ST(i) to ST(0)	ESCAPE	0 0 0	1 1 0 1 0 ST(i)		40-50		
<b>FCOMP = Compare and Pop</b>							
Integer/Real Memory to ST(0)	ESCAPE	MF 0	MOD 0 1 1 R/M	DISP	63-73	80-93	67-77
ST(i) to ST(0)	ESCAPE	0 0 0	1 1 0 1 1 ST(i)		45-52		
<b>FCOMPP = Compare ST(i) to ST(0) and Pop Twice</b>	ESCAPE	1 1 0	1 1 0 1 1 0 0 1		45-55		
<b>FTST = Test ST(0)</b>	ESCAPE	0 0 1	1 1 1 0 0 1 0 0		38-48		
<b>FXAM = Examine ST(0)</b>	ESCAPE	0 0 1	1 1 1 0 0 1 0 1		12-23		

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Table 6. 80287 Extensions to the 80286 Instruction Set (cont.)

Constants		MF	=	Optional 6,16 Bit Displacement	Clock Count Range			
					32 Bit Real	32 Bit Integer	64 Bit Real	16 Bit Integer
FLDZ = LOAD + 0.0 into ST(0)	ESCAPE 0 0 1	1 1 1 0 1 1 1 0			00	01	10	11
FLD1 = LOAD + 1.0 into ST(0)	ESCAPE 0 0 1	1 1 1 0 1 0 0 0			15-21			
FLDP1 = LOAD π into ST(0)	ESCAPE 0 0 1	1 1 1 0 1 0 1 1			16-22			
FLDLZT = LOAD log <sub>2</sub> 10 into ST(0)	ESCAPE 0 0 1	1 1 1 0 1 0 0 1			16-22			
FLDL2E = LOAD log <sub>2</sub> e into ST(0)	ESCAPE 0 0 1	1 1 1 0 1 0 1 0			15-21			
FLDLG2 = LOAD log <sub>10</sub> 2 into ST(0)	ESCAPE 0 0 1	1 1 1 0 1 1 0 0			18-24			
FLDLH2 = LOAD log <sub>e</sub> 2 into ST(0)	ESCAPE 0 0 1	1 1 1 0 1 1 0 1			17-23			
<b>Arithmetic</b>								
FADD = Addition								
Integer/Real Memory with ST(0)	ESCAPE MF 0	MOD 0 0 0 R/M	DISP		90-120	108-143	95-125	102-137
ST(i) and ST(0)	ESCAPE d P 0	1 1 0 0 0 ST(i)			70-100	(Note 1)		
FSUB = Subtraction								
Integer/Real Memory with ST(0)	ESCAPE MF 0	MOD 1 0 R/M	DISP		90-120	108-143	95-125	102-137
ST(i) and ST(0)	ESCAPE d P 0	1 1 1 0 R/M			70-100	(Note 1)		
FMUL = Multiplication								
Integer/Real Memory with ST(0)	ESCAPE MF 0	MOD 0 0 1 R/M	DISP		110-125	130-144	112-168	124-138
ST(i) and ST(0)	ESCAPE d P 0	1 1 0 0 1 R/M			90-145	(Note 1)		
FDIV = Division								
Integer/Real Memory with ST(0)	ESCAPE MF 0	MOD 1 1 R/M	DISP		215-225	230-243	220-230	224-238
ST(i) and ST(0)	ESCAPE d P 0	1 1 1 1 R/M			193-203	(Note 1)		
FSQRT = Square Root of ST(0)								
	ESCAPE 0 0 1	1 1 1 1 1 0 1 0			180-186			
FSCALE = Scale ST(0) by ST(1)								
	ESCAPE 0 0 1	1 1 1 1 1 1 0 1			32-38			
FPREM = Partial Remainder of ST(0) + ST(1)								
	ESCAPE 0 0 1	1 1 1 1 1 0 0 0			15-190			
FRNDINT = Round ST(0) to Integer								
	ESCAPE 0 0 1	1 1 1 1 1 1 0 0			18-50			

## NOTE:

1. If P=1 then add 5 clocks.

Table 8. 80287 Extensions to the 80286 Instruction Set (cont.)

		Optional 8,15 Bits Displacement	Clock Count Range
<b>FXTRACT = Extract Components of ST(0)</b>	ESCAPE 0 0 1   1 1 1 1 0 1 0 0		27-65
<b>FABS = Absolute Value of ST(0)</b>	ESCAPE 0 0 1   1 1 1 0 0 0 0 1		10-17
<b>FCHS = Change Sign of ST(0)</b>	ESCAPE 0 0 1   1 1 1 0 0 0 0 0		10-17
<b>Transcendental</b>			
<b>FPTAN = Partial Tangent of ST(0)</b>	ESCAPE 0 0 1   1 1 1 1 0 0 1 0		30-540
<b>FPATAN = Partial Arc tangent of ST(0) - ST(1)</b>	ESCAPE 0 0 1   1 1 1 0 0 0 1 1		250-800
<b>F2XM1 = <math>2^{ST(0)} \cdot 1</math></b>	ESCAPE 0 0 1   1 1 1 1 0 0 0 0		310-830
<b>FYL2X = ST(1) * Log2  ST(0) </b>	ESCAPE 0 0 1   1 1 1 1 0 0 0 1		900-1100
<b>FYL2XP1 = ST(1) * Log2  ST(0) + 1 </b>	ESCAPE 0 0 1   1 1 1 1 1 0 0 1		700-1000
<b>Processor Control</b>			
<b>FINIT = Initialize NPX</b>	ESCAPE 0 1 1   1 1 1 0 0 0 1 1		2-8
<b>FSETPM = Enter Protected Mode</b>	ESCAPE 0 1 1   1 1 1 0 0 1 0 0		2-8
<b>FSTSWAX = Store Control Word</b>	ESCAPE 1 1 1   1 1 1 0 0 0 0 0		10-16
<b>FLDCW = Load Control Word</b>	ESCAPE 0 0 1   MOD 1 0 1 R/M	DISP	7-14
<b>FSTCW = Store Control Word</b>	ESCAPE 0 0 1   MOD 1 1 1 R/M	DISP	12-18
<b>FSTSW = Store Status Word</b>	ESCAPE 1 0 1   MOD 1 1 1 R/M	DISP	12-18
<b>FCLEX = Clear Exceptions</b>	ESCAPE 0 1 1   1 1 1 0 0 0 1 0		2-6
<b>FSTENV = Store Environment</b>	ESCAPE 0 0 1   MOD 1 1 0 R/M	DISP	40-50
<b>FLDENV = Load Environment</b>	ESCAPE 0 0 1   MOD 1 0 0 R/M	DISP	35-45
<b>FSAVE = Save State</b>	ESCAPE 1 0 1   MOD 1 1 0 R/M	DISP	205-215
<b>FRSTOR = Restore State</b>	ESCAPE 1 0 1   MOD 1 0 0 R/M	DISP	205-215
<b>FINCSTP = Increment Stack Pointer</b>	ESCAPE 0 0 1   1 1 1 1 0 1 1 1		8-12
<b>FDECSTP = Decrement Stack Pointer</b>	ESCAPE 0 0 1   1 1 1 1 0 1 1 0		8-12

Table 8. 80287 Extensions to the 80286 Instruction Set (cont.)

		Clock Count Range
FFREE = Free ST(i)	ESCAPE 1 0 1   1 1 0 0 0 ST(i)	9-16
FNOP = No Operation	ESCAPE 0 0 1   1 1 0 1 0 0 0 0	10-16

**NOTES:**

- If mod=00 then DISP=0\*, disp-low and disp-high are absent.  
If mod=01 then DISP=disp-low sign-extended to 16-bits, disp-high is absent.  
If mod=10 then DISP=disp-high; disp-low.  
If mod=11 then r/m is treated as an ST(i) field.
- If r/m=000 then EA=(BX)+(SI)+DISP  
if r/m=001 then EA=(BX)+(DI)+DISP  
if r/m=010 then EA=(BP)+(SI)+DISP  
if r/m=011 then EA=(BP)+(DI)+DISP  
if r/m=100 then EA=(SI)+DISP  
if r/m=101 then EA=(DI)+DISP  
if r/m=110 then EA=(BP)+DISP  
if r/m=111 then EA=(BX)+DISP  
  
\*except if mod=000 and r/m=110 then EA=disp-high; disp-low.
- MF = Memory Format  
00—32-bit Real  
01—32-bit Integer  
10—64-bit Real  
11—16-bit Integer
- ST(0) = Current stack top  
ST(i) = <sup>i</sup>th register below stack top
- d = Destination  
0—Destination is ST(0)  
1—Destination is ST(i)
- P = Pop  
0—No pop  
1—Pop ST(0)
- R = Reverse: When d=1 reverse the sense of R  
0—Destination (op) Source  
1—Source (op) Destination
- For FSQRT:  $-0 \leq ST(0) \leq +\infty$   
For FSCALE:  $-2^{15} \leq ST(1) \leq +2^{15}$  and ST(1) integer  
For F2XM1:  $0 \leq ST(0) \leq 2^{-1}$   
For FYL2X:  $0 < ST(0) \leq \infty$   
 $-\infty < ST(1) < +\infty$   
For FYL2XP1:  $0 \leq ST(0) < (2 - \sqrt{2})/2$   
 $-\infty < ST(1) < \infty$   
For FPTAN:  $0 \leq ST(0) \leq \pi/4$   
For FPATAN:  $0 \leq ST(0) < ST(1) < +\infty$
- ESCAPE bit pattern is 11011.



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Microprocessors

## 82284 CLOCK GENERATOR AND READY INTERFACE FOR iAPX 286 PROCESSORS

- Generates System Clock for iAPX 286 Processors
- 18-pin Package
- Uses Crystal or TTL Signal for Frequency Source
- Single +5V Power Supply
- Provides Local READY and Multibus\* READY Synchronization
- Generates System Reset Output from Schmitt Trigger Input

The 82284 is a clock generator/driver which provides clock signals for iAPX 286 processors and support components. It also contains logic to supply READY to the CPU from either asynchronous or synchronous sources and synchronous RESET from an asynchronous input with hysteresis.

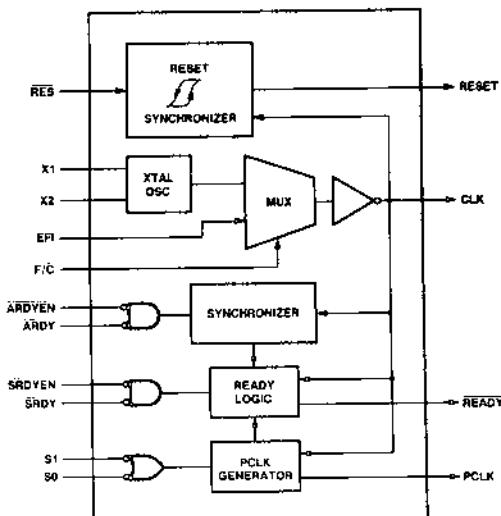


Figure 1. 82284 Block Diagram

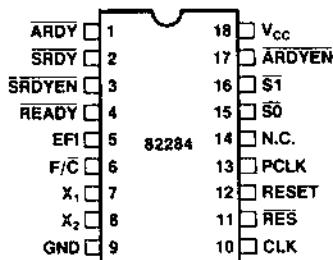


Figure 2.  
82284 Pin Configuration

\* Multibus is a patented bus of Intel

Table 1. Pin Description

The following pin function descriptions are for the 82284 clock generator.

Symbol	Type	Name and Function
CLK	O	<b>System Clock</b> is the signal used by the processor and support devices which must be synchronous with the processor. The frequency of the CLK output has twice the desired internal processor clock frequency. CLK can drive both TTL and MOS level inputs.
F/C	I	<b>Frequency/Crystal Select</b> is a strapping option to select the source for the CLK output. When F/C is strapped LOW, the internal crystal oscillator drives CLK. When F/C is strapped HIGH, the EFI input drives the CLK output.
X1, X2	I	<b>Crystal In</b> are the pins to which a parallel resonant fundamental mode crystal is attached for the internal oscillator. When F/C is LOW, the internal oscillator will drive the CLK output at the crystal frequency. The crystal frequency must be twice the desired internal processor clock frequency.
EFI	I	<b>External Frequency</b> in drives CLK when the F/C input is strapped HIGH. The EFI input frequency must be twice the desired internal processor clock frequency.
PCLK	O	<b>Peripheral Clock</b> is an output which provides a 50% duty cycle clock with 1/2 the frequency of CLK. PCLK will be in phase with the internal processor clock following the first bus cycle after the processor has been reset.
ARDYEN	I	<b>Asynchronous Ready Enable</b> is an active LOW input which qualifies the ARDY input. ARDYEN selects ARDY as the source of ready for the current bus cycle. Inputs to ARDYEN may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
ARDY	I	<b>Asynchronous Ready</b> is an active LOW input used to terminate the current bus cycle. The ARDY input is qualified by ARDYEN. Inputs to ARDY may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
SRDYEN	I	<b>Synchronous Ready Enable</b> is an active LOW input which qualifies SRDY. SRDYEN selects SRDY as the source for READY to the CPU for the current bus cycle. Setup and hold times must be satisfied for proper operation.
SRDY	I	<b>Synchronous Ready</b> is an active LOW input used to terminate the current bus cycle. The SRDY input is qualified by the SRDYEN input. Setup and hold times must be satisfied for proper operation.
READY	O	<b>Ready</b> is an active LOW output which signals the current bus cycle is to be completed. The SRDY, SRDYEN, ARDY, ARDYEN, S0, S1 and RES inputs control READY as explained later in the READY generator section. READY is an open collector output requiring an external 300 ohm pullup resistor.
S0, S1	I	<b>Status</b> inputs prepare the 82284 for a subsequent bus cycle. S0 and S1 synchronize PCLK to the internal processor clock and control READY. These inputs have pullup resistors to keep them HIGH if nothing is driving them. Setup and hold times must be satisfied for proper operation.
RESET	O	<b>Reset</b> is an active HIGH output which is derived from the RES input. RESET is used to force the system into an initial state. When RESET is active, READY will be active (LOW).
RES	I	<b>Reset In</b> is an active LOW input which generates the system reset signal RESET. Signals to RES may be applied asynchronously to CLK. A Schmitt trigger input is provided on RES, so that an RC circuit can be used to provide a time delay. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
V <sub>CC</sub>		<b>System Power:</b> +5V power supply
GND		<b>System Ground:</b> 0 volts

## FUNCTIONAL DESCRIPTION

### Introduction

The 82284 generates the clock, ready, and reset signals required for iAPX 286 processors and support components. The 82284 is packaged in an 18-pin DIP and contains a crystal controlled oscillator, MOS clock generator, peripheral clock generator, Multibus

ready synchronization logic and system reset generation logic.

### Clock Generator

The CLK output provides the basic timing control for an iAPX 286 system. CLK has output characteristics sufficient to drive MOS devices. CLK is generated by either an internal crystal oscillator or an external source as selected by the F/C strapping option. When

$F/C$  is LOW, the crystal oscillator drives the CLK output. When  $F/C$  is HIGH, the EFI input drives the CLK output.

The 82284 provides a second clock output (PCLK) for peripheral devices. PCLK is CLK divided by two. PCLK has a duty cycle of 50% and TTL output drive characteristics. PCLK is normally synchronized to the internal processor clock.

After reset, the PCLK signal may be out of phase with the internal processor clock. The ST and SD signals of the first bus cycle are used to synchronize PCLK to the internal processor clock. The phase of the PCLK output changes by extending its HIGH time beyond one system clock (see waveforms). PCLK is forced HIGH whenever either SD or ST were active (LOW) for the two previous CLK cycles. PCLK continues to oscillate when both SD and ST are HIGH.

Since the phase of the internal processor clock will not change except during reset, the phase of PCLK will not change except during the first bus cycle after reset.

### Oscillator

The oscillator circuit of the 82284 is a linear Pierce oscillator which requires an external parallel resonant, fundamental mode, crystal. The output of the oscillator is internally buffered. The crystal frequency chosen should be twice the required internal processor clock frequency. The crystal should have a typical load capacitance of 32 pF.

X1 and X2 are the oscillator crystal connections. For stable operation of the oscillator, two loading capacitors are recommended, as shown in Figure 3. The sum of the board capacitance and loading capacitance should equal the values shown. It is advisable to limit stray board capacitances (not including the effect of the loading capacitors or crystal capacitance) to less than 10 pF between the X1 and X2 pins.

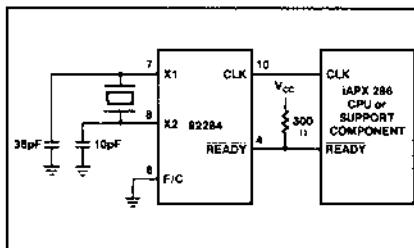


Figure 3. Recommended Crystal and Ready Connections

### Reset Operation

The reset logic provides the RESET output to force the system into a known, initial state. When the RES input is active (LOW), the RESET output becomes active (HIGH). RES is synchronized internally at the falling edge of CLK before generating the RESET output (see waveforms). Synchronization of the RES input introduces a one or two CLK delay before affecting the RESET output.

At power up, a system does not have a stable  $V_{CC}$  and CLK. To prevent spurious activity, RES should be asserted until  $V_{CC}$  and CLK stabilize at their operating values. iAPX 286 processors and support components also require their RESET inputs be HIGH a minimum number of CLK cycles. An RC network, as shown in Figure 4, will keep RES LOW long enough to satisfy both needs.

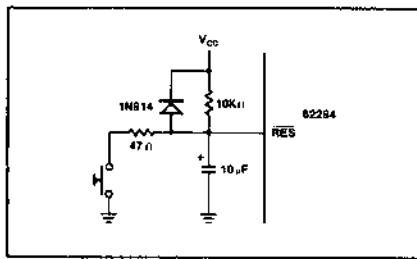


Figure 4. Typical RC RESET Timing Circuit

A Schmitt trigger input with hysteresis on RES assures a single transition of RESET with an RC circuit on RES. The hysteresis separates the input voltage level at which the circuit output switches between HIGH to LOW from the input voltage level at which the circuit output switches between LOW to HIGH. The RES HIGH to LOW input transition voltage is lower than the RES LOW to HIGH input transition voltage. As long as the slope of the RES input voltage remains in the same direction (increasing or decreasing) around the RES input transition voltage, the RESET output will make a single transition.

### Ready Operation

The 82284 accepts two ready sources for the system ready signal which terminates the current bus cycle. Either a synchronous (SRDY) or asynchronous ready (ARDY) source may be used. Each ready input has an enable (SRDYEN and ARDYEN) for selecting the type of ready source required to terminate the current bus cycle. An address decoder would normally select one of the enable inputs.

READY is enabled (LOW), if either SRDY + SRDYEN = 0 or ARDY + ARDYEN = 0 when sampled by the 82284 READY generation logic. READY will remain active for at least two CLK cycles.

The READY output has an open-collector driver allowing other ready circuits to be wire or'ed with it. The READY signal of an iAPX 286 system requires an external 300 ohm pull-up resistor. To force the READY signal inactive (HIGH) at the start of a bus cycle, the READY output floats when either S1 or S0 are sampled LOW at the falling edge of CLK. Two system clock periods are allowed for the pull-up resistor to pull the READY signal to  $V_{IH}$ . When RESET is active, READY is forced active one CLK later (see waveforms).

Figure 5 illustrates the operation of SRDY and

SRDYEN. These inputs are sampled on the falling edge of CLK when S1 and S0 are inactive and PCLK is HIGH. READY is forced active when both SRDY and SRDYEN are sampled as LOW.

Figure 6 shows the operation of ARDY and ARDYEN. These inputs are sampled by an internal synchronizer at each falling edge of CLK. The output of the synchronizer is then sampled when PCLK is HIGH. If the synchronizer resolved both the ARDY and ARDYEN inputs to have been LOW, READY becomes LOW. When both ARDY and ARDYEN have been resolved as active, the SRDY and SRDYEN inputs are ignored.

READY remains active until either S1 or S0 are sampled LOW, or the ready inputs are sampled as inactive.

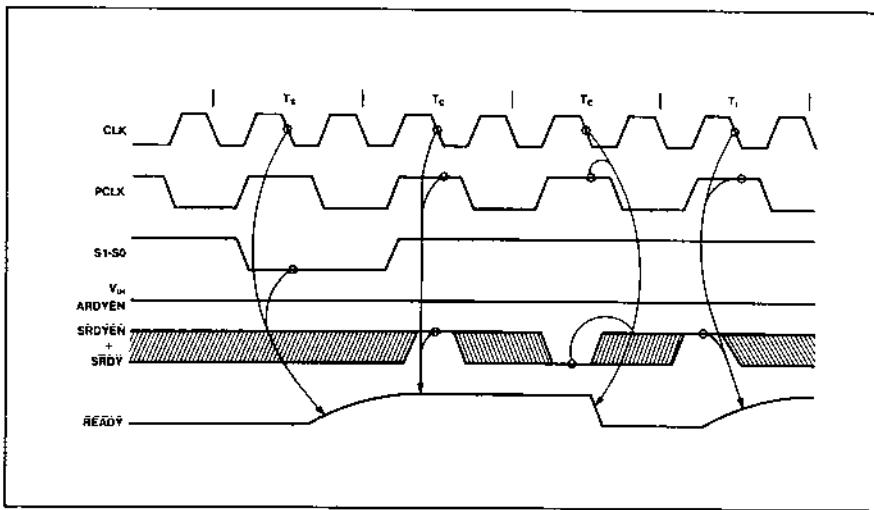


Figure 5. Synchronous Ready Operation

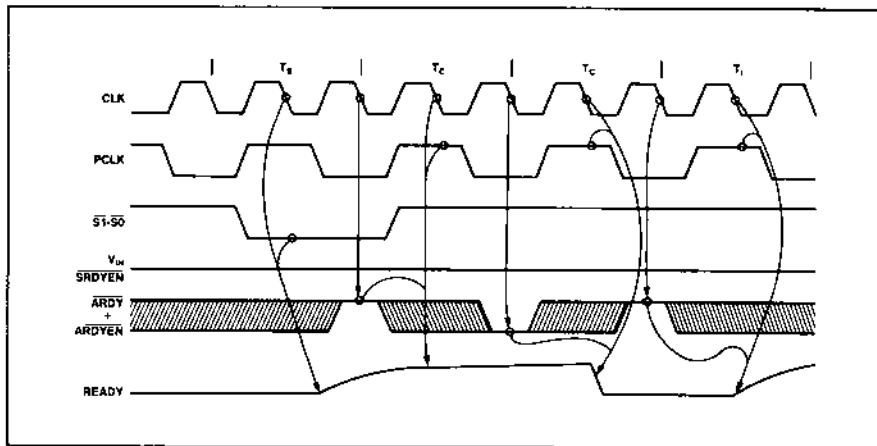


Figure 8. Asynchronous Ready Operation

**ABSOLUTE MAXIMUM RATINGS\***

Temperature Under Bias . . . . .	0°C to 70°C
Storage Temperature . . . . .	-65°C to +150°C
All Output and Supply Voltages . . . . .	-0.5V to +7V
All Input Voltages . . . . .	-1.0V to +5.5V
Power Dissipation . . . . .	1 Watt

\*Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D.C. CHARACTERISTICS (T<sub>A</sub> = 0°C to 70°C, V<sub>CC</sub> = 5V ± 10%)**

Symbol	Parameter	Min.	Max.	Units	Test Conditions
I <sub>F</sub>	Forward Input Current		-0.5	mA	V <sub>F</sub> = 0.45V
I <sub>R</sub>	Reverse Input Current		50	uA	V <sub>R</sub> = 5.25V
V <sub>C</sub>	Input Forward Clamp Voltage		-1.0	V	I <sub>C</sub> = -5 mA
I <sub>CC</sub>	Power Supply Current		145	mA	
V <sub>IL</sub>	Input LOW Voltage		0.8	V	
V <sub>IH</sub>	Input HIGH Voltage	2.0		V	
V <sub>OL</sub> , V <sub>CL</sub>	Output LOW Voltage		0.45	V	I <sub>OL</sub> = 5 mA
V <sub>CH</sub>	CLK Output HIGH Voltage	4.0		V	I <sub>OH</sub> = -1 mA
V <sub>OH</sub>	Output HIGH Voltage	2.4		V	I <sub>OH</sub> = -1 mA
V <sub>IH<sub>B</sub></sub>	RES Input HIGH Voltage	2.6		V	
V <sub>IR<sub>B</sub></sub> - V <sub>IR<sub>R</sub></sub>	RES Input Hysteresis	0.25		V	
C <sub>I</sub>	Input Capacitance		10	pF	

A.C. CHARACTERISTICS ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$ )

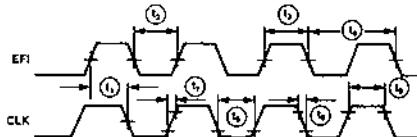
Symbol	Parameter	Min.	Max.	Units	Test Conditions
$t_1$	EFI to CLK Delay		40	ns	$t_{OL} = 5\text{ mA}$ $C_L = 150\text{ pF}$ $t_{OL} = 5\text{ mA}$
$t_2$	EFI Low Time	32		ns	
$t_3$	EFI High Time	28		ns	
$t_4$	CLK Period	55	500	ns	
$t_5$	CLK Low Time	15		ns	
$t_6$	CLK High Time	20		ns	
$t_7$	CLK Rise Time		10	ns	
$t_8$	CLK Fall Time		10	ns	
$t_9$	Status Setup Time	22.5		ns	
$t_{10}$	Status Hold Time	0		ns	
$t_{11}$	$\overline{\text{SRDY}} + \overline{\text{SRDYEN}}$ Setup Time	15		ns	$t_{OL} = 20\text{ mA}$ $C_L = 150\text{ pF}$ $t_{OL} = 20\text{ mA}$
$t_{12}$	$\overline{\text{SRDY}} + \overline{\text{SRDYEN}}$ Hold Time	0		ns	
$t_{13}$	$\overline{\text{ARDY}} + \overline{\text{ARDYEN}}$ Setup Time	0		ns	
$t_{14}$	$\overline{\text{ARDY}} + \overline{\text{ARDYEN}}$ Hold Time	16		ns	
$t_{15}$	RES Setup Time	16		ns	
$t_{16}$	RES Hold Time	0		ns	
$t_{17}$	READY Inactive Delay	5		ns	
$t_{18}$	READY Active Delay	0	24	ns	
$t_{19}$	PCLK Delay	0	40	ns	
$t_{20}$	RESET Delay	0	40	ns	
$t_{21}$	PCLK Low Time	$t_4 - 12.5$		ns	$t_{OL} = 5\text{ mA}$ $C_L = 75\text{ pF}$
$t_{22}$	PCLK High Time	$t_4 - 12.5$		ns	

Note 1.  $C_L = 150\text{ pF}$ ,  $I_{OL} = 5\text{ mA}$ . With either the internal oscillator with the recommended crystal and load or the EFI input.

Note 2.  $C_L = 150\text{ pF}$   
 $I_{OL} = 5\text{ mA}$

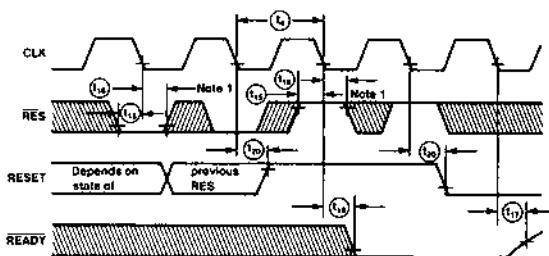
Note 3.  $I_{OL} = 5\text{ mA}$   
 $C_L = 75\text{ pF}$

## Waveforms



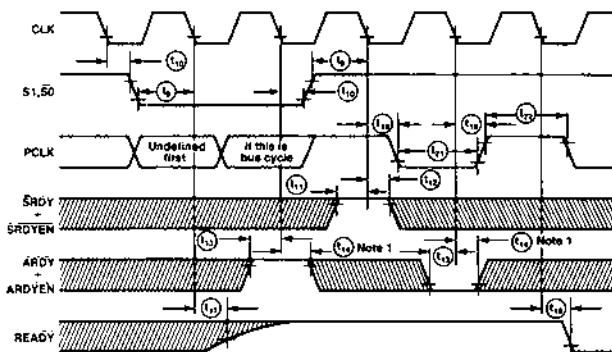
**NOTE:** The E1 input LOW and HIGH times as shown are required to guarantee the CLK LOW and HIGH times shown.

#### **RESET and READY Timing as a Function of RES with S1 and S0 HIGH**



**NOTE 1:** This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

#### **READY** and PCLK Timing with **RES HIGH**



**NOTE 1:** This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.



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## 82288 BUS CONTROLLER FOR iAPX 286 PROCESSORS

- Provides Commands and Control for Local and System Bus
- Offers Wide Flexibility in System Configurations
- Flexible Command Timing
- Optional Multibus\* Compatible Timing
- Control Drivers with 16 mA  $I_{OL}$  and 3-State Command Drivers with 32 mA  $I_{OL}$
- Single +5V Supply

The Intel 82288 Bus Controller is a 20-pin HMOS component for use in iAPX 286 microsystems. The bus controller provides command and control outputs with flexible timing options. Separate command outputs are used for memory and I/O devices. The data bus is controlled with separate data enable and direction control signals.

Two modes of operation are possible via a strapping option: Multibus compatible bus cycles, and high speed bus cycles.

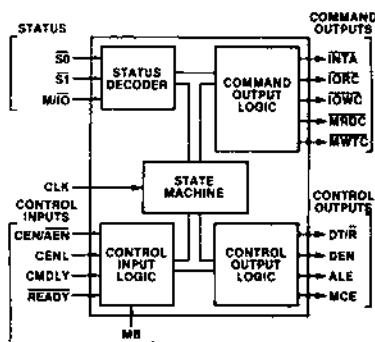


Figure 1. 82288 Block Diagram

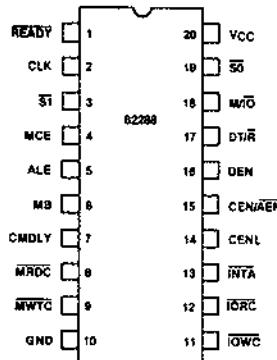


Figure 2. 82288 Pin Diagram

\*Multibus is a patented bus of Intel.

Table 1. Pin Description

The following pin function descriptions are for the 82288 bus controller.

Symbol	Type	Name and Function																																								
CLK	I	System Clock provides the basic timing control for the 82288 in an iAPX 286 microsystem. Its frequency is twice the internal processor clock frequency. The falling edge of this input signal establishes when inputs are sampled and command and control outputs change.																																								
S0, S1	I	Bus Cycle Status starts a bus cycle and, along with M/I/O, defines the type of bus cycle. These inputs are active LOW. A bus cycle is started when either S1 or S0 is sampled LOW at the falling edge of CLK. These inputs have pullups sufficient to hold them HIGH when nothing drives them. Setup and hold times must be met for proper operation.																																								
		<table border="1"> <thead> <tr> <th colspan="4">iAPX 286 Bus Cycle Status Definition</th> </tr> <tr> <th>M/I/O</th> <th>S1</th> <th>S0</th> <th>Type of Bus Cycle</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Interrupt acknowledge</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>I/O Read</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>I/O Write</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>None; idle</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Halt or shutdown</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Memory read</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Memory write</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>None; idle</td> </tr> </tbody> </table>	iAPX 286 Bus Cycle Status Definition				M/I/O	S1	S0	Type of Bus Cycle	0	0	0	Interrupt acknowledge	0	0	1	I/O Read	0	1	0	I/O Write	0	1	1	None; idle	1	0	0	Halt or shutdown	1	0	1	Memory read	1	1	0	Memory write	1	1	1	None; idle
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M/I/O	I	Memory or I/O Select determines whether the current bus cycle is in the memory space or I/O space. When LOW, the current bus cycle is in the I/O space. Setup and hold times must be met for proper operation.																																								
MB	I	Multibus Mode Select determines timing of the command and control outputs. When HIGH, the bus controller operates in Multibus mode. When LOW, the bus controller optimizes the command and control output timing for short bus cycles. The function of the CEN/AEN input pin is selected by this signal. This input is intended to be a strapping option and not dynamically changed. This input may be connected to VCC or GND.																																								
CENL	I	Command Enable Latched is a bus controller select signal which enables the bus controller to respond to the current bus cycle being initiated. CENL is an active HIGH input latched internally at the start of each bus cycle. CENL is used to select the appropriate bus controller for each bus cycle in a system where the CPU has more than one bus it can use. This input may be connected to VCC to select this 82288 for all transfers. No control inputs affect CENL. Setup and hold times must be met for proper operation.																																								
CMDLY	I	Command Delay allows delaying the start of a command. CMDLY is an active HIGH input. If sampled HIGH, the command output is not activated and CMDLY is again sampled at the next CLK cycle. When sampled LOW the selected command is enabled. If READY is detected LOW before the command output is activated, the 82288 will terminate the bus cycle, even if no command was issued. Setup and hold times must be satisfied for proper operation. This input may be connected to GND if no delays are required before starting a command.																																								
READY	I	READY indicates the end of the current bus cycle. READY is an active LOW input. Multibus mode requires at least one wait state to allow the command outputs to become active. READY must be LOW during reset, to force the 82288 into the idle state. Setup and hold times must be met for proper operation.																																								

Table 1. Pin Description (Cont.)

Symbol	Type	Name and Function
CEN/AEN	I	<p><b>Command Enable/Address Enable</b> controls the command and DEN outputs of the bus controller. CEN/AEN inputs may be asynchronous to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs. This input may be connected to VCC or GND.</p> <p>When MB is HIGH this pin has the AEN function. AEN is an active LOW input which indicates that the CPU has been granted use of a shared bus and the bus controller command outputs may exit 3-state OFF and become inactive (HIGH). AEN HIGH indicates that the CPU does not have control of the shared bus and forces the command outputs into 3-state OFF and DEN inactive (LOW). AEN would normally be controlled by an 82289 bus arbiter which activates AEN when that arbiter owns the bus to which the bus controller is attached.</p> <p>When MB is LOW this pin has the CEN function. CEN is an unlatched active HIGH input which allows the bus controller activate its command and DEN outputs. With MB LOW, CEN LOW forces the command and DEN outputs inactive but does not latches them.</p>
ALE	O	<b>Address Latch Enable</b> controls the address latches used to hold an address stable during a bus cycle. This control output is active HIGH. ALE will not be issued for the halt bus cycle and is not affected by any of the control inputs.
MCE	O	<b>Master Cascade Enable</b> signals that a cascade address from a master 8259A interrupt controller may be placed onto the CPU address bus for latching by the address latches under ALE control. The CPU's address bus may then be used to broadcast the cascade address to slave interrupt controllers so only one of them will respond to the interrupt acknowledge cycle. This control output is active HIGH. MCE is only active during interrupt acknowledge cycles and is not affected by any control input. Using MCE to enable cascade address drivers requires latches which save the cascade address on the falling edge of ALE.
DEN	O	<b>Data Enable</b> controls when data transceivers connected to the local data bus should be enabled. DEN is an active HIGH control output. DEN is delayed for write cycles in the Multibus mode.
DT/R	O	<b>Data Transmit/Receive</b> establishes the direction of data flow to or from the local data bus. When HIGH, this control output indicates that a write bus cycle is being performed. A LOW indicates a read bus cycle. DEN is always inactive when DT/R changes states. This output is HIGH when no bus cycle is active. DT/R is not affected by any of the control inputs.
IOWC	O	<b>I/O Write Command</b> instructs an I/O device to read the data on the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. READY controls when it becomes inactive.
IORC	O	<b>I/O Read Command</b> instructs an I/O device to place data onto the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. READY controls when it becomes inactive.
MWTC	O	<b>Memory Write Command</b> instructs a memory device to read the data on the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. READY controls when it becomes inactive.
MRDC	O	<b>Memory Read Command</b> instructs the memory device to place data onto the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. READY controls when it becomes inactive.
INTA	O	<b>Interrupt Acknowledge</b> tells an interrupting device that its interrupt request is being acknowledged. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. READY controls when it becomes inactive.
VCC		<b>System Power:</b> +5V power supply
GND		<b>System Ground:</b> 0 volts

## FUNCTIONAL DESCRIPTION

### Introduction

The 82288 bus controller is used in iAPX 286 systems to provide address latch control, data transceiver control, and standard level-type command outputs. The command outputs are timed and have sufficient drive capabilities for large TTL buses and meet all IEEE-796 requirements for Multibus. A special Multibus mode is provided to satisfy all address/data setup and hold time requirements. Command timing may be tailored to special needs via a CMDLY input to determine the start of a command and READY to determine the end of a command.

Connection to multiple buses are supported with a latched enable input (CENL). An address decoder can determine which, if any, bus controller should be enabled for the bus cycle. This input is latched to allow an address decoder to take full advantage of the pipelined timing on the iAPX 286 local bus.

Buses shared by several bus controllers are supported. An AEN input prevents the bus controller from driving the shared bus command and data

signals except when enabled by an external bus arbiter such as the 82289.

Separate DEN and DT/R outputs control the data transceivers for all buses. Bus contention is eliminated by disabling DEN before changing DT/R. The DEN timing allows sufficient time for tristate bus drivers to enter 3-state OFF before enabling other drivers onto the same bus.

The term CPU refers to any iAPX 286 processor or iAPX 286 support component which may become an iAPX 286 local bus master and thereby drive the 82288 status inputs.

### Processor Cycle Definition

Any CPU which drives the local bus uses an internal clock which is one half the frequency of the system clock (CLK) (see Figure 3). Knowledge of the phase of the local bus master internal clock is required for proper operation of the iAPX 286 local bus. The local bus master informs the bus controller of its internal clock phase when it asserts the status signals. Status signals are always asserted in Phase 1 of the local bus master's internal clock.

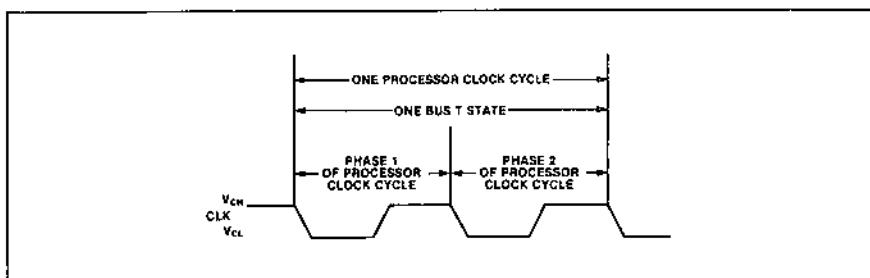


Figure 3. CLK Relationship to the Processor Clock and Bus T-States

### Bus State Definition

The 82288 bus controller has three bus states (see Figure 4): Idle ( $T_s$ ) Status ( $T_c$ ) and Command ( $T_d$ ). Each bus state is two CLK cycles long. Bus state phases correspond to the internal CPU processor clock phases.

The  $T_s$  bus state occurs when no bus cycle is currently active on the iAPX 286 local bus. This state may be repeated indefinitely. When control of the local bus is being passed between masters, the bus remains in the  $T_s$  state.

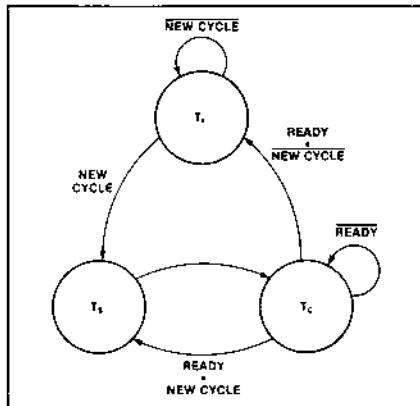


Figure 4. 82288 Bus States

### Bus Cycle Definition

The  $S_1$  and  $S_0$  inputs signal the start of a bus cycle. When either input becomes LOW, a bus cycle is started. The  $T_s$  bus state is defined to be the two CLK cycles during which either  $S_1$  or  $S_0$  are active (see Figure 5). These inputs are sampled by the 82288 at every falling edge of CLK. When either  $S_1$  or  $S_0$  are sampled LOW, the next CLK cycle is considered the second phase of the internal CPU clock cycle.

The local bus enters the  $T_c$  bus state after the  $T_s$  state. The shortest bus cycle may have one  $T_s$  state and one  $T_c$  state. Longer bus cycles are formed by repeating  $T_c$  states. A repeated  $T_c$  bus state is called a wait state.

The  $\overline{\text{READY}}$  input determines whether the current  $T_c$  bus state is to be repeated. The  $\overline{\text{READY}}$  input has the same timing and effect for all bus cycles.  $\overline{\text{READY}}$  is sampled at the end of each  $T_c$  bus state to see if it is active. If sampled HIGH, the  $T_c$  bus state is repeated. This is called inserting a wait state. The control and command outputs do not change during wait states.

When  $\overline{\text{READY}}$  is sampled LOW, the current bus cycle is terminated. Note that the bus controller may enter the  $T_s$  bus state directly from  $T_c$  if the status lines are sampled active at the next falling edge of CLK.

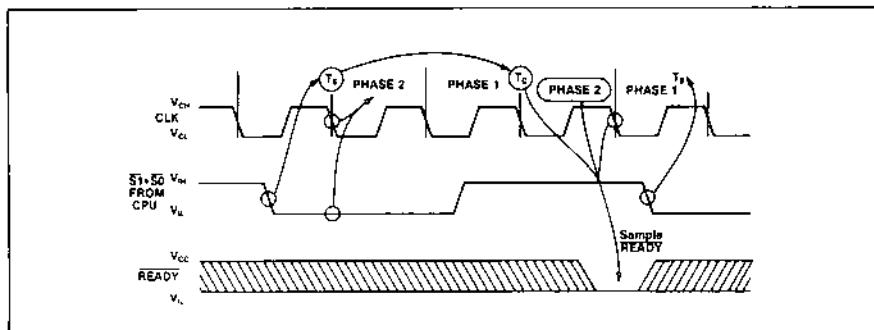


Figure 5. Bus Cycle Definition

Table 2. Command and Control Outputs for Each Type of Bus Cycle

Type of Bus Cycle	M/I/O	$\bar{S}1$	$S0$	Command Activated	DT/R State	ALE, DEN Issued?	MCE Issued?
Interrupt Acknowledge	0	0	0	INTA	LOW	YES	YES
I/O Read	0	0	1	IORC	LOW	YES	NO
I/O Write	0	1	0	IOWC	HIGH	YES	NO
None; idle	0	1	1	None	HIGH	NO	NO
Halt/Shutdown	1	0	0	None	HIGH	NO	NO
Memory Read	1	0	1	MRDC	LOW	YES	NO
Memory Write	1	1	0	MWTC	HIGH	YES	NO
None; idle	1	1	1	None	HIGH	NO	NO

### Operating Modes

Two types of buses are supported by the 82288: Multibus and non-Multibus. When the MB input is strapped HIGH, Multibus timing is used. In Multibus mode, the 82288 delays command and data activation to meet IEEE-796 requirements on address to command active and write data to command active setup timing. Multibus mode requires at least one wait state in the bus cycle since the command outputs are delayed. The non-Multibus mode does not delay any outputs and does not require wait states. The MB input affects the timing of the command and DEN outputs.

### Command and Control Outputs

The type of bus cycle performed by the local bus master is encoded in the M/I/O, S1, and S0 inputs. Different command and control outputs are activated depending on the type of bus cycle. Table 2 indicates the cycle decode done by the 82288 and the effect on command, DT/R, ALE, DEN, and MCE outputs.

Bus cycles come in three forms: read, write, and halt. Read bus cycles include memory read, I/O read, and interrupt acknowledge. The timing of the associated read command outputs (MRDC, IORC, and INTA), control outputs (ALE, DEN, DT/R) and control inputs (CEN/AEN, CENL, CMDLY, MB, and READY) are identical for all read bus cycles. Read cycles differ only in which command output is activated. The MCE control output is only asserted during interrupt acknowledge cycles.

Write bus cycles activate different control and command outputs with different timing than read bus cycles. Memory write and I/O write are write bus cycles whose timing for command outputs (MWTC and IOWC), control outputs (ALE, DEN, DT/R) and control inputs (CEN/AEN, CENL, CMDLY, MB, and READY) are identical. They differ only in which command output is activated.

Halt bus cycles are different because no command or control output is activated. All control inputs are ignored until the next bus cycle is started via S1 and S0.

Figures 6-10 show the basic command and control output timing for read and write bus cycles. Halt bus cycles are not shown since they activate no outputs. The basic idle-read-idle and idle-write-idle bus cycles are shown. The signal label CMD represents the appropriate command output for the bus cycle. For Figures 6-10, the CMDLY input is connected to GND and CENL to V<sub>CC</sub>. The effects of CENL and CMDLY are described later in the section on control inputs.

Figures 6 and 7 show non-Multibus cycles. MB is connected to GND while CEN is connected to V<sub>CC</sub>. Figure 6 shows a read cycle with no wait states while Figure 7 shows a write cycle with one wait state. The READY input is shown to illustrate how wait states are added.

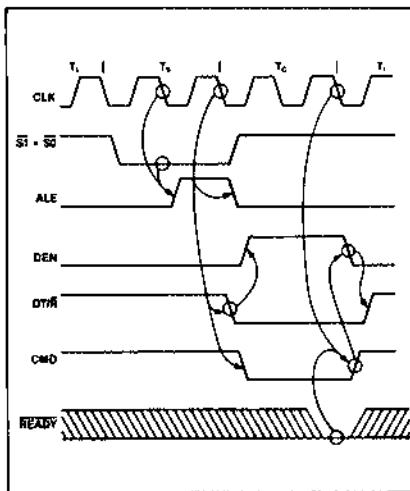


Figure 6. Idle-Read-Idle Bus Cycles with MB = 0

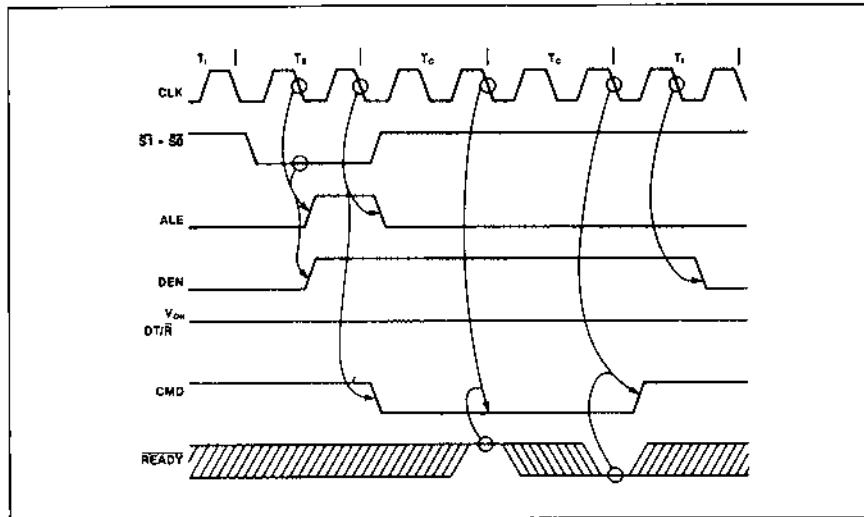


Figure 7. Idle-Write-Idle Bus Cycles with MB = 0

Bus cycles can occur back to back with no  $T_1$  bus states between  $T_C$  and  $T_S$ . Back to back cycles do not affect the timing of the command and control outputs. Command and control outputs always reach the states shown for the same clock edge (within  $T_S$ ,  $T_C$ , or following bus state) of a bus cycle.

A special case in control timing occurs for back to back write cycles with  $MB = 0$ . In this case,  $DT/R$  and  $DEN$  remain HIGH between the bus cycles (see Figure 8). The command and ALE output timing does not change.

Figures 9 and 10 show a Multibus cycle with  $MB = 1$ .  $AEN$  and  $CMDLY$  are connected to GND. The effects of  $CMDLY$  and  $\overline{AEN}$  are described later in the section on control inputs. Figure 9 shows a read cycle with one wait state and Figure 10 shows a write cycle with two wait states. The second wait state of the write cycle is shown only for example purposes and is not required. The  $READY$  input is shown to illustrate how wait states are added.

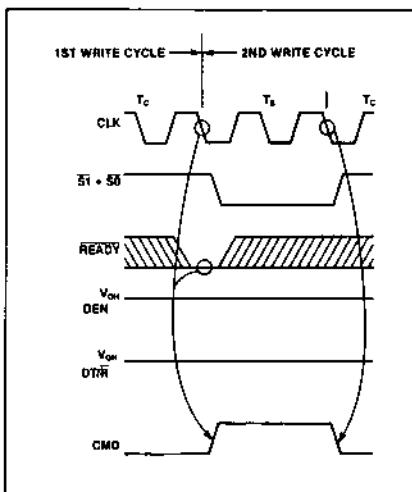


Figure 8. Write-Write Bus Cycles with  $MB = 0$

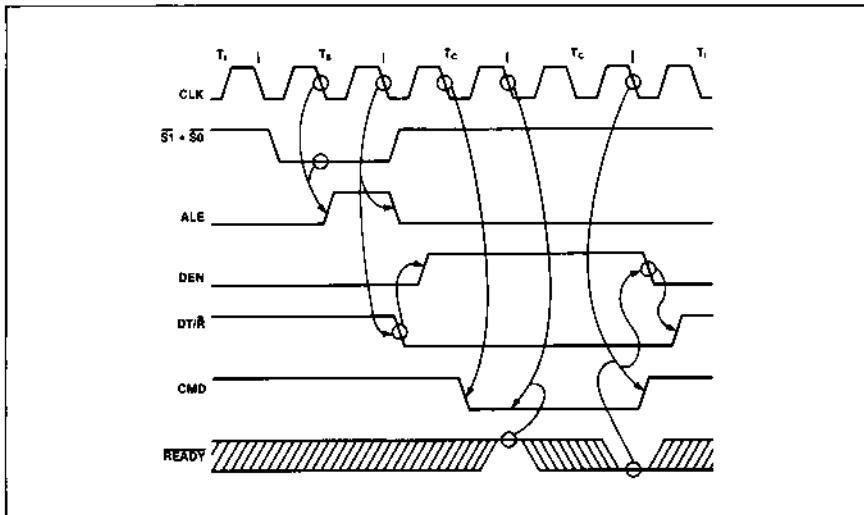


Figure 9. Idle-Read-Idle Bus Cycles with  $MB = 1$

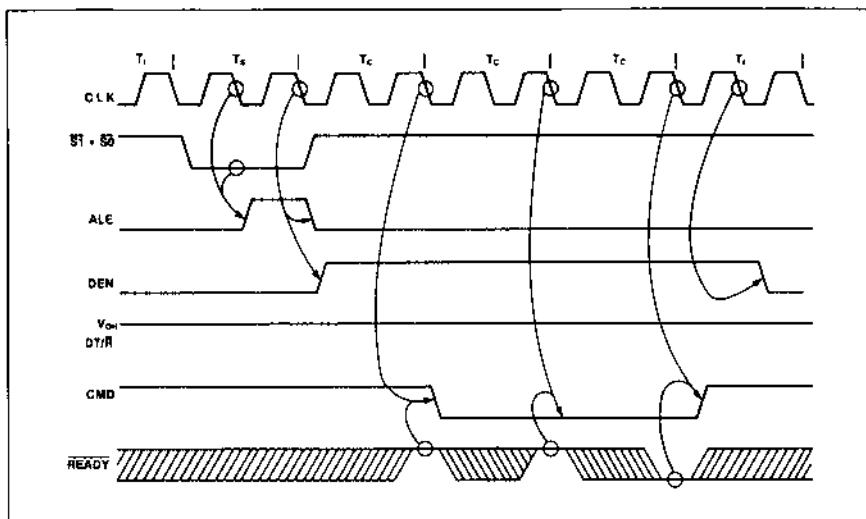


Figure 10. Idle-Write-Idle Bus Cycles with MB = 1

The MB control input affects the timing of the command and DEN outputs. These outputs are automatically delayed in Multibus mode to satisfy three requirements:

- 1) 50 ns minimum setup time for valid address before any command output becomes active.
- 2) 50 ns minimum setup time for valid write data before any write command output becomes active.
- 3) 65 ns maximum time from when any read command becomes inactive until the slave's read data drivers reach 3-state OFF.

Three signal transitions are delayed by MB = 1 as compared to MB = 0:

- 1) The HIGH to LOW transition of the read command outputs (IORC, MRDC, and INTA) are delayed one CLK cycle.
- 2) The HIGH to LOW transition of the write command outputs (IOWC and MWTC) are delayed two CLK cycles.
- 3) The LOW to HIGH transition of DEN for write cycles is delayed one CLK cycle.

Back to back bus cycles with MB = 1 do not change the timing of any of the command or control outputs. DEN always becomes inactive between bus cycles with MB = 1.

Except for a halt or shutdown bus cycle, ALE will be issued during the second half of T<sub>2</sub> for any bus cycle. ALE becomes inactive at the end of the T<sub>2</sub> to allow latching the address to keep it stable during the entire bus cycle. The address outputs may change during Phase 2 of any T<sub>c</sub> bus state. ALE is not affected by any control input.

Figure 11 shows how MCE is timed during interrupt acknowledge (INTA) bus cycles. MCE is one CLK cycle longer than ALE to hold the cascade address from a master 8259A valid after the falling edge of ALE. With the exception of the MCE control output, an INTA bus cycle is identical in timing to a read bus cycle. MCE is not affected by any control input.

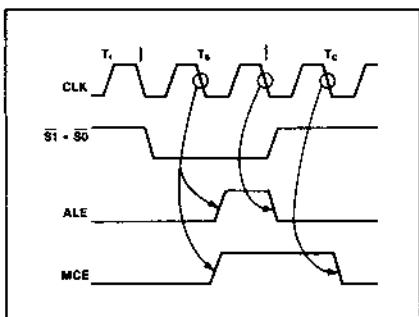


Figure 11. MCE Operation for an INTA Bus Cycle

### Control Inputs

The control inputs can alter the basic timing of command outputs, allow interfacing to multiple buses, and share a bus between different masters. For many IAPX 286 systems, each CPU will have more than one bus which may be used to perform a bus cycle. Normally, a CPU will only have one bus controller active for each bus cycle. Some buses may be shared by more than one CPU (i.e. Multibus) requiring only one of them use the bus at a time.

Systems with multiple and shared buses use two control input signals of the 82288 bus controller, CENL and AEN (see Figure 12). CENL enables the bus controller to control the current bus cycle. The AEN input prevents a bus controller from driving its command outputs. AEN HIGH means that another bus controller may be driving the shared bus.

In Figure 12, two buses are shown: a local bus and a Multibus. Only one bus is used for each CPU bus cycle. The CENL inputs of the bus controllers select which bus controller is to perform the bus cycle. An address decoder determines which bus to use for each bus cycle. The 82288 connected to the shared Multibus must be selected by CENL and be given access to the Multibus by AEN before it will begin a Multibus operation.

CENL must be sampled HIGH at the end of the  $T_s$  bus state (see waveforms) to enable the bus controller to activate its command and control outputs. If sampled LOW the commands and DEN will not go active and DT/R will remain HIGH. The bus controller will ignore the CMDLY, CEN, and READY inputs until another bus cycle is started via S1 and S0. Since an address decoder is commonly used to identify which bus is required for each bus cycle, CENL is latched to avoid the need for latching its input.

The CENL input can affect the DEN control output. When MB = 0, DEN normally becomes active during Phase 2 of  $T_s$  in write bus cycles. This transition occurs before CENL is sampled. If CENL is sampled LOW, the DEN output will be forced LOW during  $T_c$  as shown in the timing waveforms.

When MB = 1, CEN/AEN becomes AEN. AEN controls when the bus controller command outputs enter and exit 3-state OFF. AEN is intended to be driven by a bus arbiter, like the 82289, which assures only one bus controller is driving the shared bus at any time. When AEN makes a LOW to HIGH transition, the command outputs immediately enter 3-state OFF and DEN is forced inactive. An inactive DEN should force the local data transceivers connected to the shared data bus into 3-state OFF (see Figure 12). The LOW to HIGH transition of AEN should only occur during  $T_s$  or  $T_c$  bus states.

The HIGH to LOW transition of AEN signals that the bus controller may now drive the shared bus command signals. Since a bus cycle may be active or be in the process of starting, AEN can become active during any  $T$ -state. AEN LOW immediately allows DEN to go to the appropriate state. Three CLK edges later, the command outputs will go active (see timing waveforms). The Multibus requires this delay for the address and data to be valid on the bus before the commands become active.

When MB = 0, CEN/AEN becomes CEN. CEN is an asynchronous input which immediately affects the command and DEN outputs. When CEN makes a HIGH to LOW transition, the commands

and DEN are immediately forced inactive. When CEN makes a LOW to HIGH transition, the commands and DEN outputs immediately go to the appropriate state (see timing waveforms). READY must still become active to terminate a bus cycle if CEN remains LOW for a selected bus controller (CENL was latched HIGH).

Some memory or I/O systems may require more address or write data setup time to command active than provided by the basic command output timing. To provide flexible command timing, CMDLY input can delay the activation of command outputs. The CMDLY input must be sampled LOW to activate the command outputs. CMDLY does not affect the control outputs ALE, MCE, DEN, and DT/R.

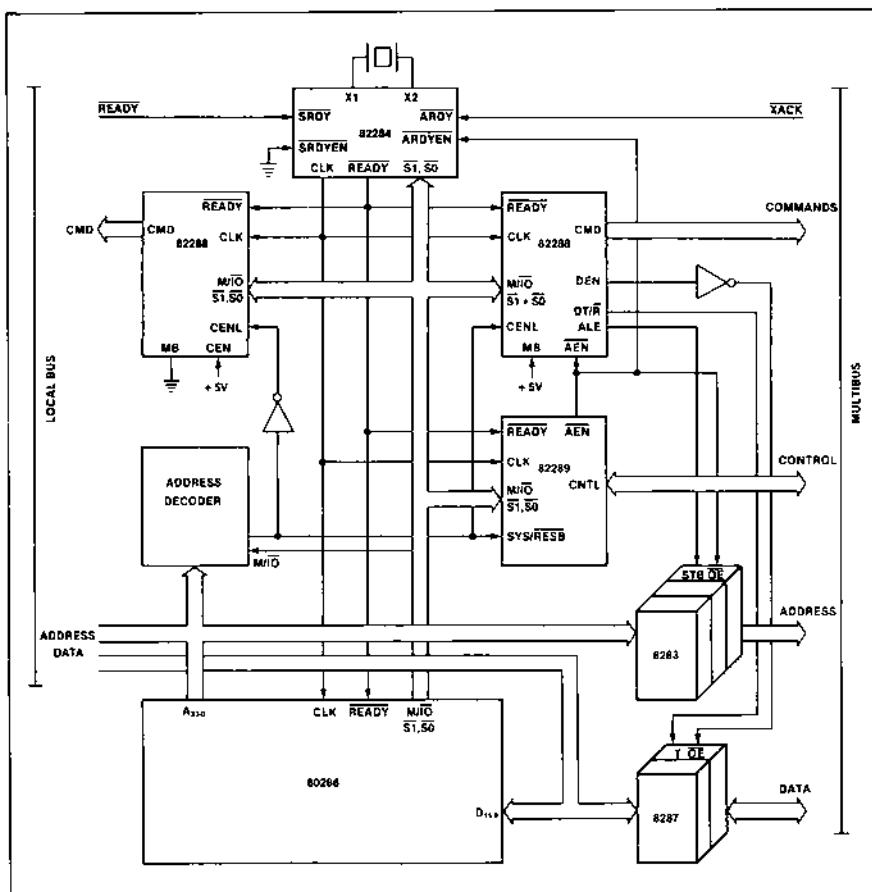


Figure 12. System Use of AEN and CENL

CMDLY is first sampled on the falling edge of the CLK ending  $T_5$ . If sampled HIGH, the command output is not activated, and CMDLY is again sampled on the next falling edge of CLK. Once sampled LOW, the proper command output becomes active immediately if MB = 0. If MB = 1, the proper command goes active no earlier than shown in Figures 9 and 10.

READY can terminate a bus cycle before CMDLY allows a command to be issued. In this case no commands are issued and the bus controller will deactivate DEN and DT/R in the same manner as if a command had been issued.

### Waveforms Discussion

The waveforms show the timing relationships of inputs and outputs and do not show all possible transitions of all signals in all modes. Instead, all signal timing relationships are shown via the general cases. Special cases are shown when needed. The waveforms provide some functional descriptions of the 82288; however, most functional descriptions are provided in Figures 5 through 11.

To find the timing specification for a signal transition in a particular mode, first look for a special case in the waveforms. If no special case applies, then use a timing specification for the same or related function in another mode.

### ABSOLUTE MAXIMUM RATINGS\*

Ambient Temperature Under Bias ..... 0°C to 70°C  
 Storage Temperature ..... -65°C to +150°C  
 Voltage on Any Pin with  
 Respect to GND ..... -0.5V to +7V  
 Power Dissipation ..... 1 Watt

*\*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

### D.C. CHARACTERISTICS ( $V_{CC} = 5V \pm 10\%$ , $T_A = 0^\circ C$ to $70^\circ C$ )

Symbol	Parameter	Min	Max	Units	Test Conditions
$I_{CC}$	Power Supply Current		100	mA	
$I_F$	Forward Input Current CLK Input Other Inputs		-.1 -.5	mA mA	$V_F = 0.45V$ $V_F = 0.45V$
$I_R$	Reverse Input Current		.50	uA	$V_R = V_{CC}$
$V_{OL}$	Output LOW Voltage Command Outputs Control Outputs		.45 .45	V V	$I_{OL} = 32\text{ mA}$ $I_{OL} = 16\text{ mA}$
$V_{OH}$	Output HIGH Voltage Command Outputs Control Outputs	2.4 2.4		V V	$I_{OH} = -5\text{ mA}$ $I_{OH} = -1\text{ mA}$
$V_{IL}$	Input LOW Voltage	-.5	.8	V	
$V_{CL}$	CLK Input LOW Voltage	-.5	.6	V	
$V_{IH}$	Input HIGH Voltage	2.0	$V_{CC} + 0.5$	V	
$V_{CH}$	CLK Input HIGH Voltage	3.9	$V_{CC} + 0.5$	V	
$I_{OFF}$	Output Off Current		100	uA	
$C_{CLK}$	CLK Input Capacitance		10	pF	
$C_I$	Input Capacitance		10	pF	

**A.C. CHARACTERISTICS** ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$ )

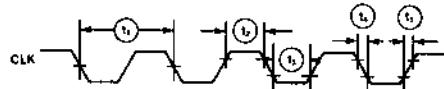
Symbol	Parameter	Min	Max	Units	Test Conditions
t <sub>1</sub>	CLK Period	62.5	250	ns	at 1.5V
t <sub>2</sub>	CLK HIGH Time	20	235	ns	at 3.9V
t <sub>3</sub>	CLK LOW Time	15	230	ns	at 0.6V
t <sub>4</sub>	CLK Fall Time		10	ns	3.5V to 1.0V
t <sub>5</sub>	CLK Rise Time		10	ns	1.0V to 3.5V
t <sub>6</sub>	M/I/O and Status Setup Time	22.5		ns	
t <sub>7</sub>	M/I/O and Status Hold Time	0		ns	
t <sub>8</sub>	CENL Setup Time	20		ns	
t <sub>9</sub>	CENL Hold Time	0		ns	
t <sub>10</sub>	READY Setup Time	38.5		ns	
t <sub>11</sub>	READY Hold Time	25		ns	
t <sub>12</sub>	CMDLY Setup Time	20		ns	
t <sub>13</sub>	CMDLY Hold Time	0		ns	
t <sub>14</sub>	AEN Setup Time	25		ns	
t <sub>15</sub>	AEN Hold Time	0		ns	
t <sub>16</sub>	ALE, MCE Active Delay	3	15	ns	
t <sub>17</sub>	ALE, MCE Inactive Delay		20	ns	
t <sub>18</sub>	DEN (WRITE) Inactive From CENL		35	ns	
t <sub>19</sub>	DT/R LOW From CLK		20	ns	
t <sub>20</sub>	DEN (READ) Active From DT/R	10	50	ns	
t <sub>21</sub>	DEN (READ) Inactive Delay	3	15	ns	
t <sub>22</sub>	DT/R HIGH From DEN Inactive	10	40	ns	
t <sub>23</sub>	DEN (WRITE) Active Delay		30	ns	
t <sub>24</sub>	DEN (WRITE) Inactive Delay	3	30	ns	
t <sub>25</sub>	DEN Inactive From CEN		25	ns	
t <sub>26</sub>	DEN Active From CEN		25	ns	
t <sub>27</sub>	DT/R HIGH From CLK And CEN		50	ns	Note 2
t <sub>28</sub>	DEN Active From AEN		30	ns	
t <sub>29</sub>	Command Active Delay	3	20	ns	
t <sub>30</sub>	Command Inactive Delay	3	15	ns	
t <sub>31</sub>	Command Inactive From CEN		25	ns	
t <sub>32</sub>	Command Active From CEN		25	ns	
t <sub>33</sub>	Command Inactive Enable From AEN		40	ns	
t <sub>34</sub>	Command Float Time		40	ns	

Note 1: AEN is a asynchronous input. AEN setup and hold time is specified to guarantee the response shown in the waveforms.

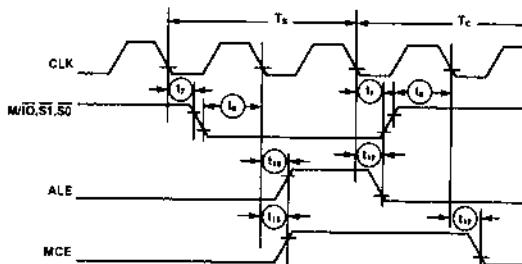
Note 2: T<sub>27</sub> only applies to bus cycles where MB = 0, the 82288 was selected, and DEN = 0 when the cycle terminated (because CEN = 0).

## WAVEFORMS

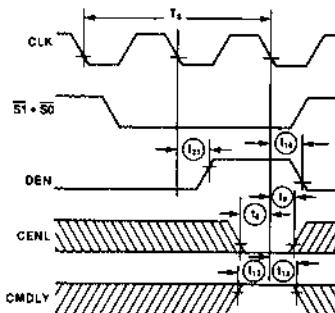
## CLK CHARACTERISTICS



## STATUS, ALE, MCE, CHARACTERISTICS

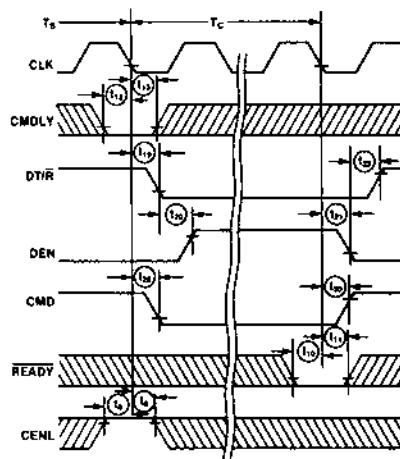


## CENL, CMDLY, DEN CHARACTERISTICS WITH MB = 0 AND CEN = 1 DURING WRITE CYCLE

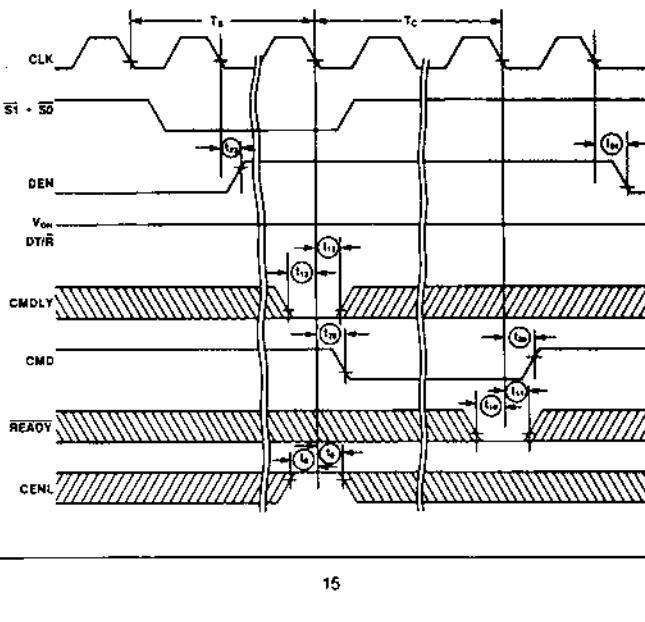


## WAVEFORMS (Continued)

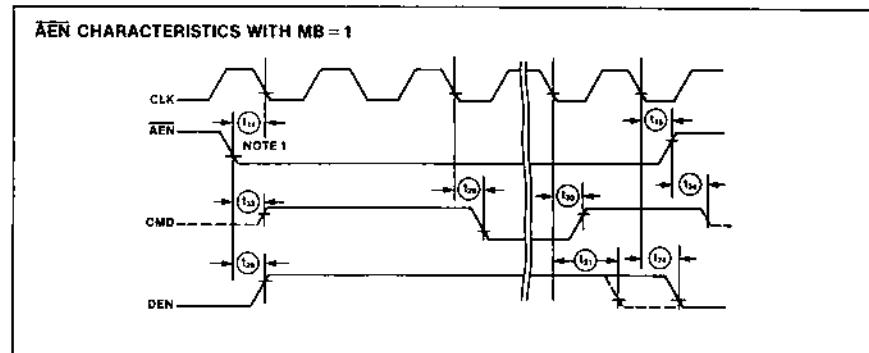
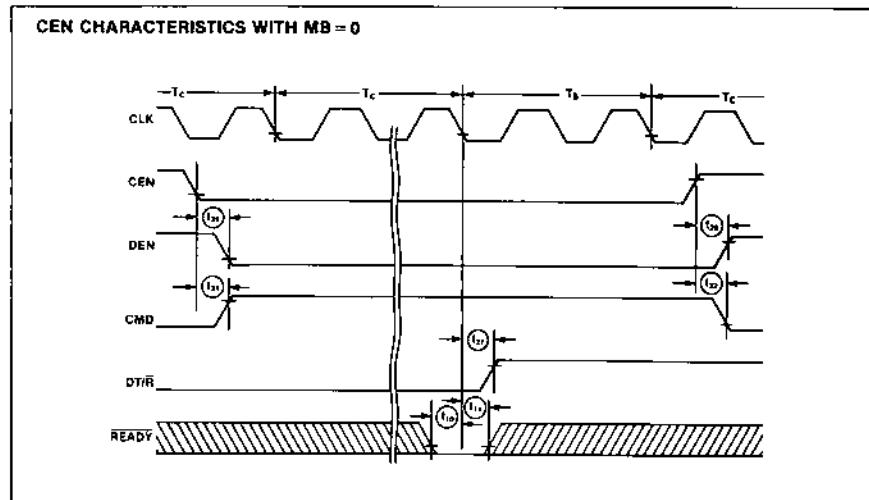
## READ CYCLE CHARACTERISTICS WITH MB = 0 AND CEN = 1



WRITE CYCLE CHARACTERISTICS WITH MB = 0 AND CEN = 1



## WAVEFORMS (Continued)



NOTE 1: AEN is an asynchronous input. AEN setup and hold time is specified to guarantee the response shown in the waveforms.



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MOTOROLA

# SEMICONDUCTORS

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## Advance Information

### REAL-TIME CLOCK PLUS RAM (RTC)

The MC146818A Real-Time Clock plus RAM is a peripheral device which includes the unique MOTEI concept for use with various microprocessors, microcomputers, and larger computers. This part combines three unique features: a complete time-of-day clock with alarm and one hundred year calendar, a programmable periodic interrupt and square-wave generator, and 50 bytes of low-power static RAM. The MC146818A uses high-speed CMOS technology to interface with 1 MHz processor buses, while consuming very little power.

The Real-Time Clock plus RAM has two distinct uses. First, it is designed as a battery powered CMOS part (in an otherwise NMOS/TTL system) including all the common battery backed-up functions such as RAM, time, and calendar. Secondly, the MC146818A may be used with a CMOS microprocessor to relieve the software of the timekeeping workload and to extend the available RAM of an MPU such as the MC146805E2.

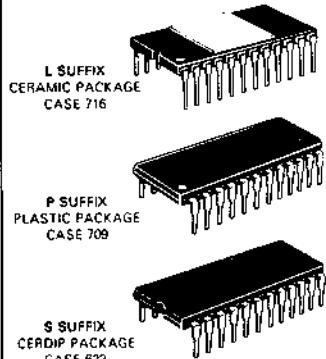
- Low-Power, High-Speed CMOS
- Internal Time Base and Oscillator
- Counts Seconds, Minutes, and Hours of the Day
- Counts Days of the Week, Date, Month, and Year
- 3 V to 6 V Operation
- Time Base Input Options: 4.194304 MHz, 1.048576 MHz, or 32.768 kHz
- Time Base Oscillator for Parallel Resonant Crystals
- 40 to 200  $\mu$ W Typical Operating Power at Low Frequency Time Base
- 4.0 to 20 mW Typical Operating Power at High Frequency Time Base
- Binary or BCD Representation of Time, Calendar, and Alarm
- 12- or 24-Hour Clock with AM and PM in 12-Hour Mode
- Daylight Savings Time Option
- Automatic End of Month Recognition
- Automatic Leap Year Compensation
- Microprocessor Bus Compatible
- Selectable Between Motorola and Competitor Bus Timing
- Multiplexed Bus for Pin Efficiency
- Interfaced with Software as 64 RAM Locations
- 14 Bytes of Clock and Control Registers
- 50 Bytes of General Purpose RAM
- Status Bit indicates Data Integrity
- Bus Compatible Interrupt Signals (IRQ)
- Three Interrupts are Separately Software Maskable and Testable  
Time-of-Day Alarm, Once-per-Second to Once-per-Day  
Periodic Rates from 30.5  $\mu$ s to 500 ms  
End-of-Clock Update Cycle
- Programmable Square-Wave Output Signal
- Clock Output May Be Used as Microprocessor Clock Input  
At Time Base Frequency +1 or +4
- 24-Pin Dual-In-Line Package
- Quad Pack Also Available

## MC146818A

### CMOS

(HIGH-PERFORMANCE  
SILOON-GATE COMPLEMENTARY MOS)

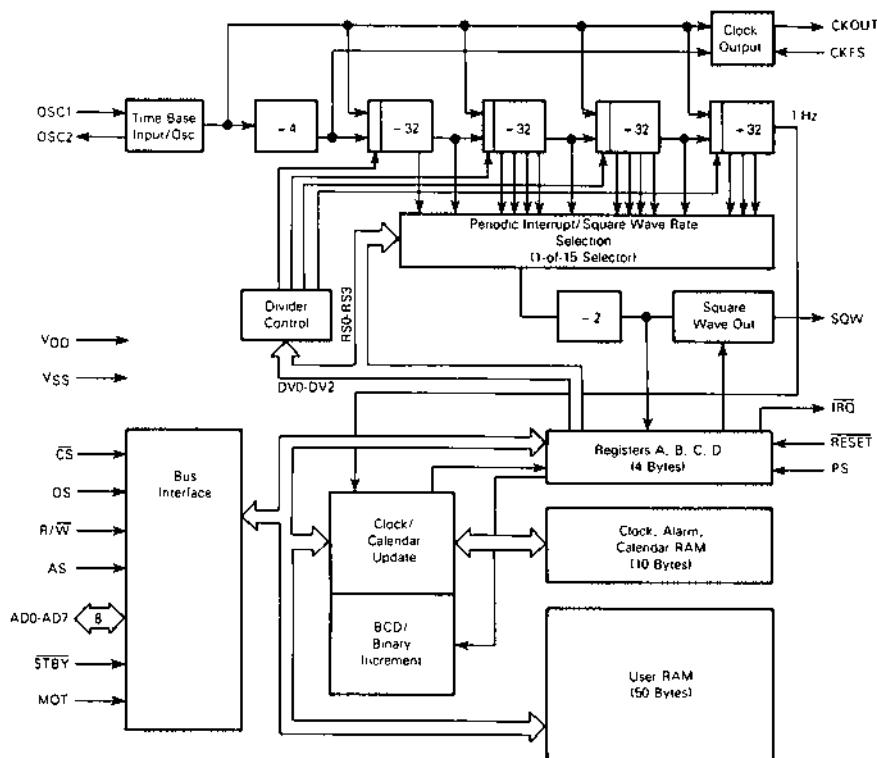
### REAL-TIME CLOCK PLUS RAM



### PIN ASSIGNMENT

MOT	1	●	24	VDD
OSC1	2		23	SQW
OSC2	3		22	PS
AD0	4		21	CLOCKOUT
AD1	5		20	CFCS
AD2	6		19	IRQ
AD3	7		18	RESET
AD4	8		17	DS
AD5	9		16	STBY
AD6	10		15	R/W
AD7	11		14	AS
VSS	12		13	CS

FIGURE 1 - BLOCK DIAGRAM

MAXIMUM RATINGS (Voltages referenced to V<sub>SS</sub>)

Rating	Symbol	Value	Unit
Supply Voltage	V <sub>DD</sub>	-0.3 to +8.0	V
All Input Voltages Except OSC1	V <sub>in</sub>	V <sub>SS</sub> - 0.5 to V <sub>DD</sub> + 0.5	V
Current Draw per Pin Excluding V <sub>DD</sub> and V <sub>SS</sub>	I	10	mA
Operating Temperature Range MC146818A MC146818AC	T <sub>A</sub>	T <sub>L</sub> to T <sub>H</sub> 0 to 70 -40 to 85	°C
Storage Temperature Range	T <sub>SIG</sub>	-65 to +150	°C

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance			
Plastic	θ <sub>JA</sub>	120	°C/W
Cerip		65	
Ceramic		50	

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V<sub>in</sub> and V<sub>out</sub> be constrained to the range V<sub>SS</sub> ≤ V<sub>in</sub> or V<sub>out</sub> ≤ V<sub>DD</sub>. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>).



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DC ELECTRICAL CHARACTERISTICS ( $V_{DD} = 3$  Vdc,  $V_{SS} = 0$  Vdc,  $T_A = T_L$  to  $T_H$  unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Frequency of Operation	$f_{osc}$	32.768	32.768	kHz
Output Voltage $I_{Load} < 10 \mu A$	$V_{OL}$	—	0.1	V
	$V_{OH}$	$V_{DD} - 0.1$	—	
$I_{DD} =$ Bus Idle $CKOUT = f_{osc}$ , $C_L = 15 \text{ pF}$ , SQW Disabled, $STBY = 0.2$ V, $C_L (OSC2) = 10 \text{ pF}$ $f_{osc} = 32.768$ kHz	$I_{DD3}$	—	50	$\mu A$
$I_{DD} =$ Quiescent $f_{osc} = DC$ , $OSC1 = DC$ , All Other Inputs = $V_{DD} - 0.2$ V, No Clock	$I_{DD4}$	—	50	$\mu A$
Output High Voltage $I_{Load} = -0.25$ mA, All Outputs)	$V_{OH}$	2.7	—	V
Output Low Voltage $I_{Load} = 0.25$ mA, All Outputs)	$V_{OL}$	—	0.3	V
Input High Voltage STBY, ADD-AD7, DS, AS, R/W, CS, RESET, CKFS, PS, OSC1, MOT	$V_{IH}$	2.1 2.5 $V_{DD}$	$V_{DD}$ $V_{DD}$	V
Input Low Voltage STBY, ADD-AD7, DS, AS, R/W, CS, CKFS, PS, RESET, OSC1, MOT	$V_{IL}$	$V_{SS}$ $V_{SS}$	0.5 $V_{SS}$	V
Input Current AS, DS, R/W MOT, OSC1, OE, STBY, RESET, CKFS, PS	$I_{in}$	—	$\pm 10$ $\pm 1$	$\mu A$
Three-State Leakage I <sub>IQ</sub> , ADD-AD7	$I_{TSL}$	—	$\pm 10$	$\mu A$

DC ELECTRICAL CHARACTERISTICS ( $V_{DD} = 5$  Vdc  $\pm 10\%$ ,  $V_{SS} = 0$  Vdc,  $T_A = T_L$  to  $T_H$  unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Frequency of Operation	$f_{osc}$	32.768	4194.304	kHz
Output Voltage $I_{Load} < 10 \mu A$	$V_{OL}$	—	0.1	V
	$V_{OH}$	$V_{DD} - 0.1$	—	
$I_{DD} =$ Bus Idle (External Clock) $CKOUT = f_{osc}$ , $C_L = 15 \text{ pF}$ ; SQW Disabled, $STBY = 0.2$ V, $C_L (OSC2) = 10 \text{ pF}$ $f_{osc} = 4.194304$ MHz $f_{osc} = 1.048516$ MHz $f_{osc} = 32.768$ kHz	$I_{DD1}$ $I_{DD2}$ $I_{DD3}$	— — —	3 800 50	$\mu A$ $\mu A$ $\mu A$
$I_{DD} =$ Quiescent $f_{osc} = DC$ , $OSC1 = DC$ , All Other Inputs = $V_{DD} - 0.2$ V, No Clock	$I_{DD4}$	—	50	$\mu A$
Output High Voltage $I_{Load} = -1.6$ mA, ADD-AD7, CKOUT)	$V_{OH}$	4.1	—	V
$I_{Load} = -1.0$ mA, SQW)				
Output Low Voltage $I_{Load} = 1.6$ mA, ADD-AD7, CKOUT)	$V_{OL}$	—	0.4	V
$I_{Load} = 1.0$ mA, I <sub>IQ</sub> and SQW)				
Input High Voltage STBY, CKFS, ADD-AD7, DS, AS, R/W, CS, PS, RESET, OSC1, MOT	$V_{IH}$	$V_{DD} - 2.0$ $V_{DD} - 0.8$ $V_{DD} - 1.0$ $V_{DD}$	$V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$	V
Input Low Voltage CKFS, PS, RESET, STBY, ADD-AD7, DS, AS, R/W, CS, OSC1, MOT	$V_{IL}$	$V_{SS}$ $V_{SS}$	0.8 $V_{SS}$	V
Input Current AS, DS, R/W MOT, OSC1, OE, STBY, RESET, CKFS, PS	$I_{in}$	—	$\pm 10$ $\pm 1$	$\mu A$
Three-State Leakage I <sub>IQ</sub> , ADD-AD7	$I_{TSL}$	—	$\pm 10$	$\mu A$



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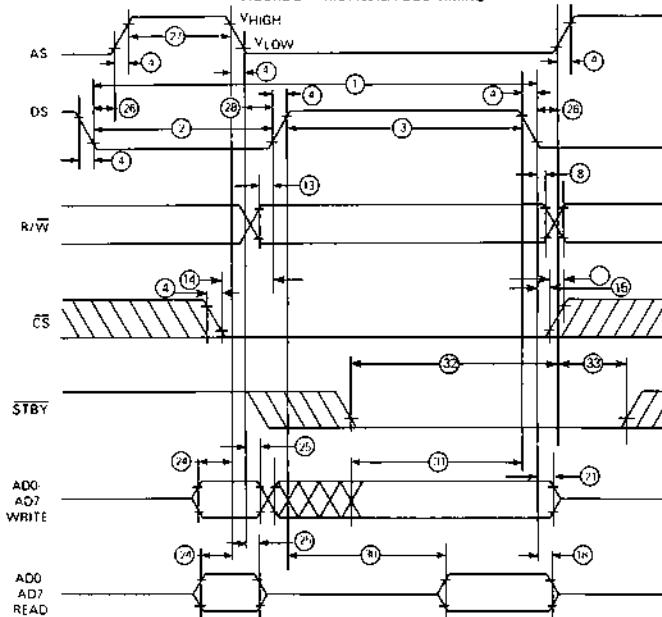
BUS TIMING

Ident. Number	Characteristics	Symbol	V <sub>DD</sub> = 3.0 V 50 pF Load		V <sub>DD</sub> = 5.0 V ± 10% 1 TTL and 130 pF Load		Unit
			Min	Max	Min	Max	
1	Cycle Time	t <sub>cyc</sub>	5000	—	953	dc	ns
2	Pulse Width, DS/E Low or RD/WR High	t <sub>PWEL</sub>	1000	—	300	—	ns
3	Pulse Width, DS/E High or RD/WR Low	t <sub>PWEH</sub>	1500	—	325	—	ns
4	Input Rise and Fall Time	t <sub>r, f</sub>	—	100	—	30	ns
8	R/W Hold Time	t <sub>RWH</sub>	10	—	10	—	ns
13	R/W Setup Time Before DS/E	t <sub>RWS</sub>	200	—	80	—	ns
14	Chip Select Setup Time Before DS, WR, or RD	t <sub>CS</sub>	200	—	25	—	ns
15	Chip Select Hold Time	t <sub>CH</sub>	10	—	0	—	ns
18	Read Data Hold Time	t <sub>IDHR</sub>	10	1000	10	100	ns
21	Write Data Hold Time	t <sub>IDHW</sub>	100	—	0	—	ns
24	Muxed Address Valid Time to AS/ALE Fall	t <sub>ASL</sub>	200	—	50	—	ns
25	Muxed Address Hold Time	t <sub>AHL</sub>	100	—	20	—	ns
26	Delay Time DS/E to AS/ALE Rise	t <sub>ASD</sub>	500	—	50	—	ns
27	Pulse Width, AS/ALE High	t <sub>PWAH</sub>	600	—	135	—	ns
28	Delay Time, AS/ALE to DS/E Rise	t <sub>ASED</sub>	500	—	60	—	ns
30	Peripheral Output Data Delay Time from DS/E or RD	t <sub>DDR</sub>	1300	—	20	240	ns
31	Peripheral Data Setup Time	t <sub>DSW</sub>	1500	—	200	—	ns
32	STBY Setup Time before AS/ALE Rise	t <sub>SBSS</sub>	TBD	—	TBD	—	ns
33	STBY Hold Time after AS/ALE Fall	t <sub>SBH</sub>	TBD	—	TBD	—	ns

NOTE: Designations E, ALE, RD, and WR refer to signals from alternative microprocessor signals.

\* Refer to **IMPORTANT NOTICES** appearing on page 20 of this data sheet.

**FIGURE 2 - MC146816A BUS TIMING**



Note:  $V_{HIGH} = V_{DD} - 2.0\text{ V}$ ,  $V_{LOW} = 0.8\text{ V}$ , for  $V_{DD} = 5.0\text{ V} \pm 10\%$  for outputs only.  
 $V_{HIGH} = 2.0\text{ V}$ ,  $V_{LOW} = 0.5\text{ V}$ , for  $V_{DD} = 3.0\text{ V}$  for outputs only.



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FIGURE 3 - BUS READ TIMING COMPETITOR MULTIPLEXED BUS

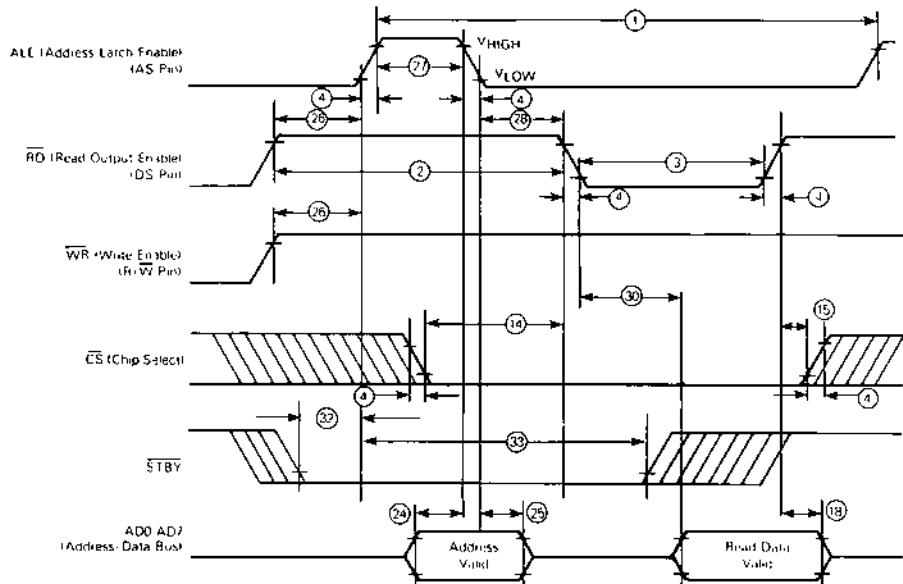
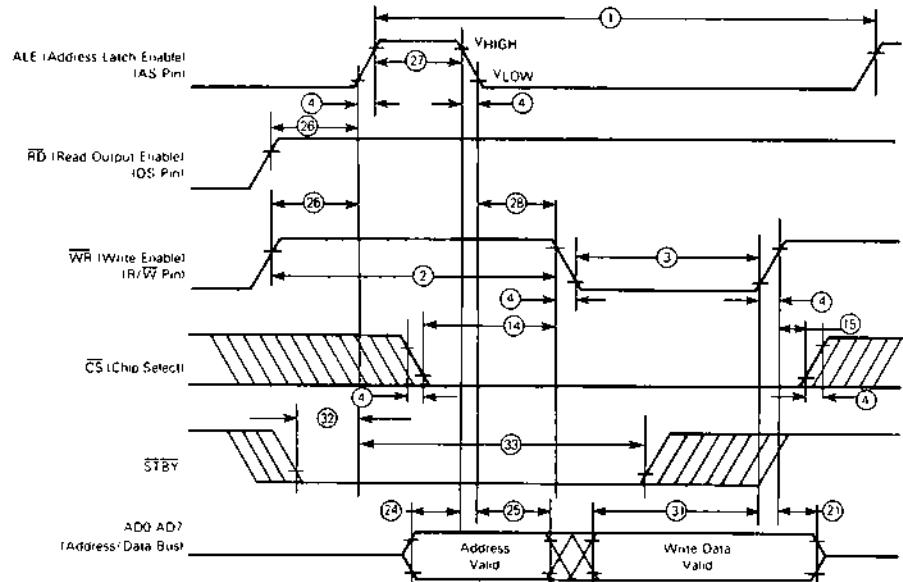


FIGURE 4 -- BUS WRITE TIMING COMPETITOR MULTIPLEXED BUS



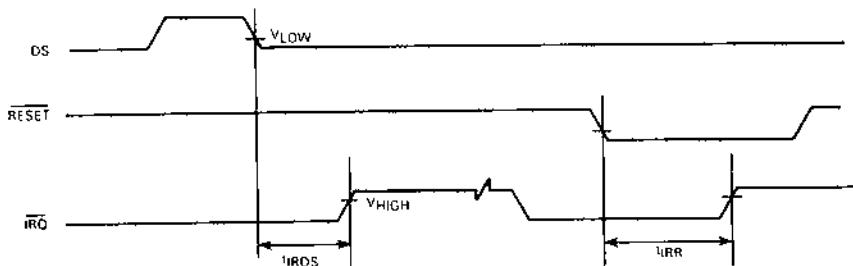
Note: VHIGH =  $V_{DD} - 2.0\text{ V}$ , VLLOW = 0.8 V, for  $V_{DD} = 5.0\text{ V} \pm 10\%$  for outputs only  
 $VHIGH = 2.0\text{ V}$ , VLLOW = 0.5 V, for  $V_{DD} = 3.0\text{ V}$  for outputs only.



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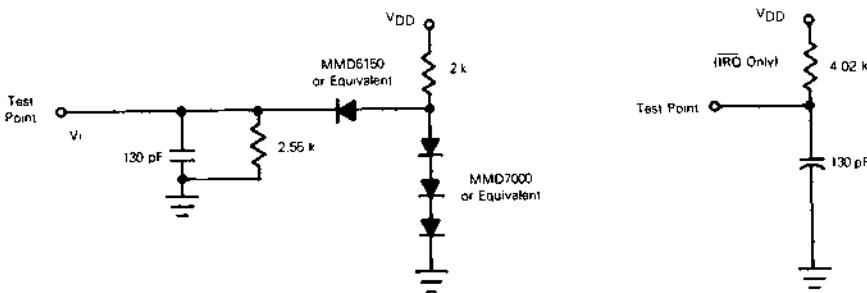
TABLE 1 — SWITCHING CHARACTERISTICS ( $V_{SS} = 0$  Vdc,  $T_A = T_L$  to  $T_H$ )

Description	Symbol	$V_{DD} = 3.0$ Vdc			$V_{DD} = 5.0$ Vdc $\pm 10\%$		
		Min	Max	Unit	Min	Max	Unit
Oscillator Startup	$t_{RC}$	—	TBD	ms	—	100	ms
Reset Pulse Width	$t_{RWL}$	TBD	—	$\mu s$	5	—	$\mu s$
Reset Delay Time	$t_{RLH}$	TBD	—	$\mu s$	5	—	$\mu s$
Power Sense Pulse Width	$t_{PWL}$	TBD	—	$\mu s$	5	—	$\mu s$
Power Sense Delay Time	$t_{PLH}$	TBD	—	$\mu s$	5	—	$\mu s$
$\overline{IRO}$ Release from DS	$t_{IRDs}$	—	TBD	$\mu s$	—	2	$\mu s$
$\overline{IRO}$ Release from RESET	$t_{IRR}$	—	TBD	$\mu s$	—	2	$\mu s$
VRT Bit Delay	$t_{VRTD}$	—	TBD	$\mu s$	—	2	$\mu s$

FIGURE 5 —  $\overline{IRO}$  RELEASE DELAY

NOTE  $V_{HIGH} = V_{DD} - 2.0$  V,  $V_{LOW} = 0.8$  V, for  $V_{DD} = 5.0$  V  $\pm 10\%$

FIGURE 6 — TTL EQUIVALENT TEST LOAD



All Outputs Except OSC2 (See Figure 10)



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FIGURE 7 - POWER-UP

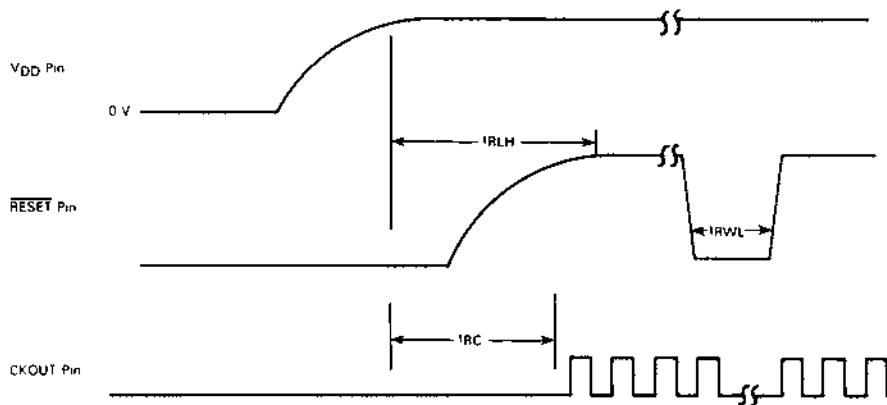
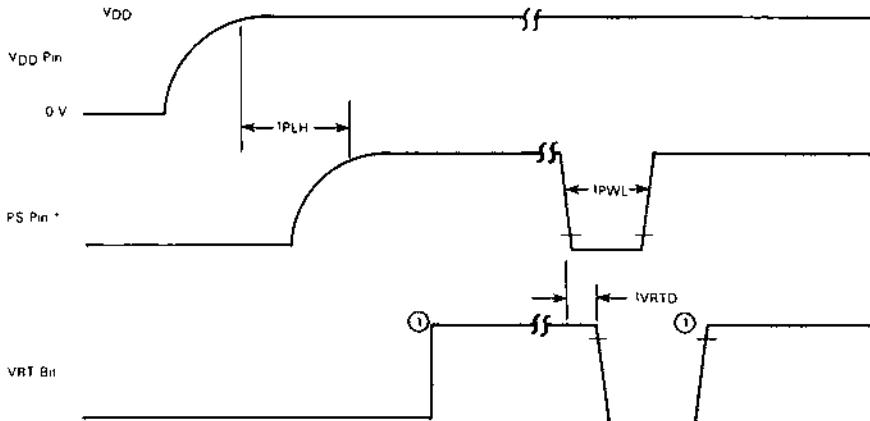


FIGURE 8 - CONDITIONS THAT CLEAR VRT BIT



① The VRT bit is set to a "1" by reading Register d. The VRT bit can only be cleared by pulling the PS pin low (see REGISTER D (#0D)).



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## SIGNAL DESCRIPTIONS

The block diagram in Figure 1, shows the pin connection with the major internal functions of the MC146818A. Real-Time Clock plus RAM. The following paragraphs describe the function of each pin.

### V<sub>DD</sub>, V<sub>SS</sub>

DC power is provided to the part on these two pins, V<sub>DD</sub> being the more positive voltage. The minimum and maximum voltages are listed in the Electrical Characteristics tables.

### MOT — MOTEI

The MOT pin offers flexibility when choosing bus type. When tied to V<sub>DD</sub>, Motorola timing is used. When tied to V<sub>SS</sub>, competitor timing is used. The MOT pin must be hard-wired to the V<sub>DD</sub> or V<sub>SS</sub> supply and cannot be switched during operation of the MC146818A.

### OSC1, OSC2 — TIME BASE, INPUTS

The time base for the time functions may be an external signal or the crystal oscillator. External square waves at 4.194304 MHz, 1.048576 MHz, or 32.768 kHz may be connected to OSC1 as shown in Figure 9. The internal time-base frequency to be used is chosen in Register A.

The on-chip oscillator is designed for a parallel resonant AT cut crystal at 4.194304 MHz, 1.048576 MHz or 32.768 kHz frequencies. The crystal connections are shown in Figure 10 and the crystal characteristics in Figure 11.

### CKOUT — CLOCK OUT, OUTPUT

The CKOUT pin is an output at the time-base frequency divided by 1 or 4. A major use for CKOUT is as the input clock to the microprocessor; thereby saving the cost of a second crystal. The frequency of CKOUT depends upon the time-base frequency and the state of the CKFS pin as shown in Table 2.

### CKFS — CLOCK OUT FREQUENCY SELECT, INPUT

When the CKFS pin is tied to V<sub>DD</sub>, it causes CKOUT to be the same frequency as the time base at the OSC1 pin. When CKFS is tied to V<sub>SS</sub>, CKOUT is the OSC1 time-base frequency divided by four. Table 2 summarizes the effect of CKFS.

TABLE 2 — CLOCK OUTPUT FREQUENCIES

Time Base (OSC1) Frequency	Clock Frequency Select Pin (CKFS)	Clock Frequency Output Pin (CKOUT)
4.194304 MHz	High	4.194304 MHz
4.194304 MHz	Low	1.048576 MHz
1.048576 MHz	High	1.048576 MHz
1.048576 MHz	Low	262.144 kHz
32.768 kHz	High	32.768 kHz
32.768 kHz	Low	8.192 kHz

### SQW — SQUARE WAVE, OUTPUT

The SQW pin can output a signal from one of the 15 taps provided by the 22 internal-divider stages. The frequency of the SQW may be altered by programming Register A, as shown in Table 5. The SQW signal may be turned on and off using the SQWE bit in Register B.

### A00-AD7 — MULTIPLEXED BI DIRECTIONAL ADDRESS/DATA BUS

Multiplexed bus processors save pins by presenting the address during the first portion of the bus cycle and using the same pins during the second portion for data. Address-then-data multiplexing does not slow the access time of the MC146818A since the bus reversal from address to data is occurring during the internal RAM access time.

The address must be valid just prior to the fall of AS/ALE at which time the MC146818A latches the address from A00 to AD5. Valid write data must be presented and held stable during the latter portion of the DS or WR pulses. In a read cycle, the MC146818A outputs eight bits of data during the latter portion of the DS or RD pulses, then ceases driving the bus (returns the output drivers to the high-impedance state) when DS falls in the Motorola case of MOTEI or RD rises in the other case.

### AS — MULTIPLEXED ADDRESS STROBE, INPUT

A positive going multiplexed address strobe pulse serves to demultiplex the bus. The falling edge of AS or ALE causes the address to be latched within the MC146818A.

### DS — DATA STROBE OR READ, INPUT

The DS pin has two interpretations via the MOTEI circuit. When emanating from a Motorola type processor, DS is a positive pulse during the latter portion of the bus cycle, and is variously called DS (data strobe), E (enable), and φ2 (φ2 clock). During read cycles, DS signifies the time that the RTC is to drive the bidirectional bus. In write cycles, the trailing edge of DS causes the Real-Time Clock plus RAM to latch the written data.

The second MOTEI interpretation of DS is that of RD, MEMR, or I70W emanating from the competitor type processor. In this case, DS identifies the time period when the real-time clock plus RAM drives the bus with read data. This interpretation of DS is also the same as an output-enable signal on a typical memory.

### R/W — READ/WRITE, INPUT

The MOTEI circuit treats the R/W pin in one of two ways. When a Motorola type processor is connected, R/W is a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/W while DS is high, whereas a write cycle is a low on R/W during DS.

The second interpretation of R/W is as a negative write pulse, WR, MEMW, and I70W from competitor type processors. The MOTEI circuit in this mode gives R/W pin the same meaning as the write (W) pulse on many generic RAMs.

### CS — CHIP SELECT, INPUT

The chip-select (CS) signal must be asserted (low) for a bus cycle in which the MC146818A is to be accessed. CS is not latched and must be stable during DS and AS (Motorola case of MOTEI) and during RD and WR. Bus cycles which take place without asserting CS cause no actions to take place within the MC146818A. When CS is not used, it should be grounded. (See Figure 20).



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FIGURE 9 — EXTERNAL TIME-BASE CONNECTION

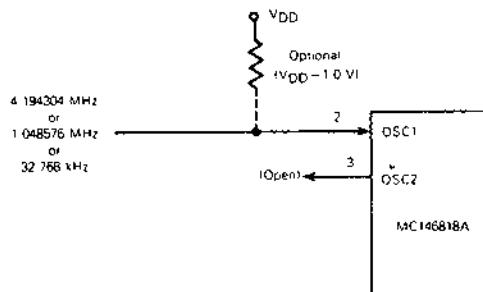
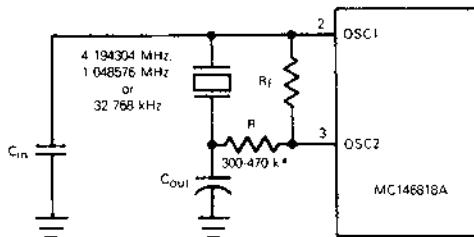


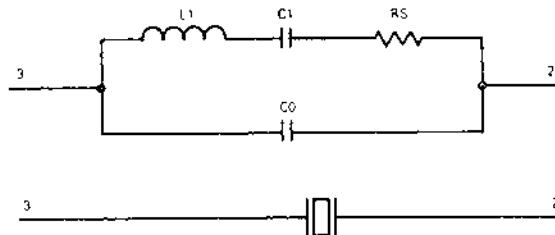
FIGURE 10 — CRYSTAL OSCILLATOR CONNECTION



\* 32.768 kHz Only - Consult Crystal Manufacturer's Specification

FIGURE 11 — CRYSTAL PARAMETERS

Crystal Equivalent Circuit



I <sub>osc</sub>	4.194304 MHz	1.048576 MHz	32.768 kHz
R <sub>S</sub> (Maximum)	75 Ω	200 Ω	10 k
C <sub>O</sub> (Maximum)	1 pF	5 pF	7 pF
C <sub>1</sub>	12 pF	2.008 pF	1.003 pF
Q	50	35	35
C <sub>in</sub> · C <sub>out</sub>	15-40 pF	15-40 pF	10.72 pF
R	400-470 k	400-470 k	400-470 k
R <sub>f</sub>	10 M	10 M	22 M



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**IRQ - INTERRUPT REQUEST, OUTPUT**

The IRQ pin is an active low output of the MC146818A that may be used as an interrupt input to a processor. The IRQ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the IRQ pin, the processor program normally reads Register C. The RESET pin also clears pending interrupts.

When no interrupt conditions are present, the IRQ level is in the high-impedance state. Multiple interrupting devices may thus be connected to an IRQ bus with one pullup at the processor.

**RESET - RESET, INPUT**

The RESET pin does not affect the clock, calendar, or RAM functions. On powerup, the RESET pin must be held low for the specified time,  $t_{RLH}$ , in order to allow the power supply to stabilize. Figure 12 shows a typical representation of the RESET pin circuit.

When RESET is low the following occurs:

- Periodic Interrupt Enable (PIE) bit is cleared to zero,
- Alarm Interrupt Enable (AIE) bit is cleared to zero,
- Alarm Interrupt Enable (AIE) bit is cleared to zero,
- Update ended Interrupt Flag (IUF) bit is cleared to zero,
- Interrupt Request status Flag (IRQF) bit is cleared to zero,
- Periodic Interrupt Flag (PIF) bit is cleared to zero,
- The part is not accessible.
- Alarm Interrupt Flag (AF) bit is cleared to zero,
- IRQ pin is in high-impedance state, and
- Square Wave output Enable (SQWE) bit is cleared to zero.

**STBY - STAND-BY**

The STBY pin, when active, prevents access to the MC146818A making it ideal for battery back-up applications. Stand-by operation incorporates a transparent latch. After data strobe (DS) goes low (RD or WR rises), STBY is recognized as a valid signal.

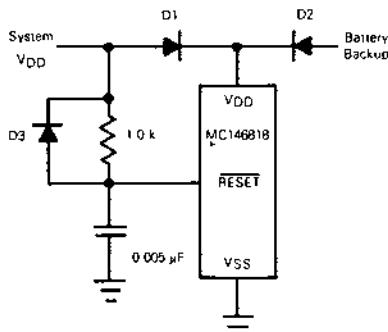
The STBY signal is totally asynchronous. Its transparent latch is opened by the falling edge of DS (rising edge of RD or WR) and clocked by the rising edge of AS (AIE). Therefore, for STBY to be recognized, DS and AS should occur in pairs. When STBY goes low before the falling edge of DS (rising edge of WR or RD), the current cycle is completed at that edge and the next cycle will not be executed.

**PS - POWER SENSE, INPUT**

The power-sense pin is used in the control of the valid RAM and time (VRT) bit in Register D. When the PS pin is low the VRT bit is cleared to zero.

When using the VRT feature during powerup, the PS pin must be externally held low for the specified  $t_{PLH}$  time. As power is applied, the VRT bit remains low indicating that the contents of the RAM, time registers, and calendar are not guaranteed. PS must go high after powerup to allow the VRT bit to be set by a read of register D.

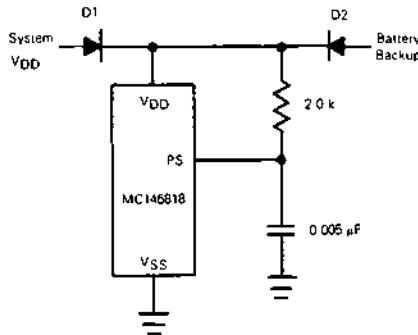
**FIGURE 12 - TYPICAL POWERUP DELAY CIRCUIT FOR RESET**



D1 = MBD701 (Schottky) or Equivalent  
D2 = D3 = IN4148 or Equivalent

Note: If the RTC is isolated from the MPU or MCU power by a diode drop, care must be taken to meet  $V_{in}$  requirements.

**FIGURE 13 - TYPICAL POWERUP DELAY CIRCUIT FOR POWER SENSE**



D1 = MBD701 (Schottky) or Equivalent  
D2 = IN4148 or Equivalent



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### POWER-DOWN CONSIDERATIONS

In most systems, the MC146818A must continue to keep time when system power is removed. In such systems, a conversion from system power to an alternate power supply, usually a battery, must be made. During the transition from system to battery power, the designer of a battery backed-up RTC system must protect data integrity, minimize power consumption, and ensure hardware reliability.

The stand-by (STBY) pin controls all bus inputs (R/W, DS, AS, ADD-AD7). STBY, when negated, disallows any unintended modification of the RTC data by the bus. STBY also reduces power consumption by reducing the number of transitions seen internally.

Power consumption may be further reduced by removing resistive and capacitive loads from the clock out (CKOUT1) pin and the squarewave (SQW) pin.

During and after the power source conversion, the V<sub>H</sub> maximum specification must never be exceeded. Failure to meet the V<sub>H</sub> maximum specification can cause a virtual SCR to appear which may result in excessive current drain and destruction of the part.

### ADDRESS MAP

Figure 14 shows the address map of the MC146818A. The memory consists of 50 general purpose RAM bytes, 10 RAM bytes which normally contain the time, calendar, and alarm data, and four control and status bytes. All 64 bytes are directly readable and writable by the processor program except for the following: 1) Registers C and D are read only, 2) bit 7 of Register A is read only, and 3) the high-order bit of the seconds byte is read only. The contents of four control and status registers (A, B, C, and D) are described in REGISTERS.

### TIME, CALENDAR, AND ALARM LOCATIONS

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the 10 time, calendar, and alarm bytes may be either binary or binary-coded decimal (BCD).

Before initializing the internal registers, the SET bit in Register B should be set to a "1" to prevent time/calendar updates from occurring. The program initializes the 10 locations in the selected format (binary or BCD), then indicates the format in the data mode (DM) bit of Register B. All 10 time, calendar, and alarm bytes must use the same data mode, either binary or BCD. The SET bit may now be cleared to allow updates. Once initialized the real-time clock makes all updates in the selected data mode. The data mode cannot be changed without reinitializing the 10 data bytes.

Table 3 shows the binary and BCD formats of the 10 time, calendar, and alarm locations. The 24:12 bit in Register B establishes whether the hour locations represent 1-to-12 or 0-to-23. The 24:12 bit cannot be changed without reinitializing the hour locations. When the 12 hour format is selected the high-order bit of the hours byte represents PM when it is a "1".

The time, calendar, and alarm bytes are not always accessible by the processor program. Once per second the 10 bytes are switched to the update logic to be advanced by one second and to check for an alarm condition. If any of the 10 bytes are read at this time, the data outputs are undefined. The update lockout time is 248  $\mu$ s at the 4.194304 MHz and 1.048567 MHz time bases and 1948  $\mu$ s for the 32.768 kHz time base. The Update Cycle section shows how to accommodate the update cycle in the processor program.

The three alarm bytes may be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is any hexadecimal byte from CO to FF. That is, the two most-significant bits of each byte, when set to "1", create a "don't care" situation. An alarm interrupt each hour is created with a "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

FIGURE 14 — ADDRESS MAP

Address	Description	Binary ... BCD Contents
0	Seconds	00
1	Seconds Alarm	01
2	Minutes	02
3	Minutes Alarm	03
4	Hours	04
5	Hours Alarm	05
6	Day of Week	06
7	Date of Month	07
8	Month	08
9	Year	09
10	Register A	(IA)
11	Register B	0B
12	Register C	0C
13	Register D	0D



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TABLE 3 - TIME, CALENDAR, AND ALARM DATA MODES

Address Location	Function	Decimal Range	Range		Example*	
			Binary Data Mode	BCD Data Mode	Binary Data Mode	BCD Data Mode
0	Seconds	0-59	\$00-\$3B	000-59	15	21
1	Seconds Alarm	0-59	\$00-\$3B	000-59	15	21
2	Minutes	0-59	\$00-\$3B	000-59	3A	58
3	Minutes Alarm	0-59	\$00-\$3B	000-59	3A	58
4	Hours (12 Hour Mode)	1-12	\$01-\$DC (AMI and \$81-\$BC IPMI)	\$01-\$12 (AMI and \$81-\$92 IPMI)	05	05
	Hours (24 Hour Mode)	0-23	\$00-\$17	\$00-93	05	06
5	Hours Alarm (12 Hour Mode)	1-12	\$01-\$0C (AMI and \$81-\$8C IPMI)	\$01-\$12 (AMI and \$81-\$92 IPMI)	05	05
	Hours Alarm (24 Hour Mode)	0-23	\$00-\$17	\$00-23	05	05
6	Day of the Week Sunday = 1	1-7	\$01-\$07	\$01-507	05	05
7	Date of the Month	1-31	\$01-\$1F	\$01-531	9F	15
8	Month	1-12	\$01-\$0C	\$01-\$12	02	02
9	Year	0-99	\$00-\$63	\$00-999	4F	79

\*Example. 5.58 21 Thursday 15 February 1979 (time is AM)

#### STATIC CMOS RAM

The 50 general purpose RAM bytes are not dedicated within the MC146818A. They can be used by the processor program, and are fully available during the update cycle.

When time and calendar information must use battery back-up, very frequently there is other non-volatile data that must be retained when main power is removed. The 50 user RAM bytes serve the need for low-power CMOS battery-backed storage, and extend the RAM available to the program.

When further CMOS RAM is needed, additional MC146818As may be included in the system. The time/calendar functions may be disabled by holding the DV0-DV2 dividers, in Register A, in the reset state by setting the SET bit in Register B or by removing the oscillator. Holding the dividers in reset prevents interrupts or SOW output from operating while setting the SET bit allows these functions to occur. With the dividers clear, the available user RAM is extended to 59 bytes. The high-order bit of the seconds byte, bit 7 of Register A, and all bits of Registers C and D cannot effectively be used as general purpose RAM.

#### INTERRUPTS

The RTC plus RAM includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from once-per-second to one-a-day. The periodic interrupt may be selected for rates from half-a-second to 30.517 µs. The update-ended interrupt may be used to indicate to the program that an update cycle is completed. Each of these independent interrupt conditions are described in greater detail in other sections.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in Register B enable the three interrupts. Writing a "1" to a interrupt-enable bit permits that interrupt to be initiated when the event occurs. A "0" in the interrupt-enable bit prohibits the IRQ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enabled, the IRQ pin is immediately activated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, a flag bit is set to a "1" in Register C. Each of the three interrupt sources have separate flag bits in Register C, which are set independent of the state of the corresponding enable bits in Register B. The flag bit may be used with or without enabling the corresponding enable bits.

In the software scanned case, the program does not enable the interrupt. The "interrupt" flag bit becomes a status bit, which the software interrogates, when it wishes. When the software detects that the flag is set, it is an indication to software that the "interrupt" event occurred since the bit was last read.

However, there is one precaution. The flag bits in Register C are cleared (record of the interrupt event is erased) when Register C is read. Double latching is included with Register C so the bits which are set are stable throughout the read cycle. All bits which are high when read by the program are cleared, and new interrupts (on any bits) are held after the read cycle. One, two or three flag bits may be found to be set when Register C is used. The program should inspect all utilized flag bits every time Register C is read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt-flag bit is set and the corresponding interrupt-enable bit is also set, the IRQ pin is asserted low. IRQ is asserted as long as at least one of the three interrupt sources has its flag and enables bits both set. The IRQ bit in Register C is a "1" whenever the IRQ pin is being driven low.

The processor program can determine that the RTC initiated the interrupt by reading Register C. A "1" in bit 7



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(IRQF bit) indicates that one or more interrupts have been initiated by the part. The act of reading Register C clears all the then-active flag bits, plus the IRQF bit. When the program finds IRQF set, it should look at each of the individual flag bits in the same byte which have the corresponding interrupt-mask bits set and service each interrupt which is set. Again, more than one interrupt-flag bit may be set.

#### DIVIDER STAGES

The MC146818A has 22 binary-divider stages following the time base as shown in Figure 1. The output of the dividers is a 1 Hz signal to the update-cycle logic. The dividers are controlled by three divider bus (DV2, DV1, and DV0) in Register A.

#### DIVIDER CONTROL

The divider-control bits have three uses, as shown in Table 4. Three usable operating time bases may be selected (4.194304 MHz, 1.048576 MHz, or 32.768 kHz). The divider chain may be held at reset, which allows precision setting of the time. When the divider is changed from reset to an

operating time base, the first update cycle is one-half second later. The divider-control bits are also used to facilitate testing the MC146818A.

#### SQUARE-WAVE OUTPUT SELECTION

Fifteen of the 22 divider taps are made available to a 1-of-15 selector as shown in Figure 1. The first purpose of selecting a divider tap is to generate a square-wave output signal at the SQW pin. The RS0-RS3 bits in Register A establish the square-wave frequency as listed in Table 5. The SQW frequency selection shares the 1-of-15 selector with periodic interrupts.

Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square-wave output selection bits, or the SOWE output-enable bit may generate an asymmetrical waveform at the time of execution. The square-wave output pin has a number of potential uses. For example, it can serve as a frequency standard for external use, a frequency synthesizer, or could be used to generate one or more audio tones under program control.

TABLE 4 - DIVIDER CONFIGURATIONS

Time-Base Frequency	Divider Bits Register A			Operation Mode	Divider Reset	Bypass First N-Divider Bits
	DV2	DV1	DV0			
4.194304 MHz	0	0	0	Yes		N = 0
1.048576 MHz	0	0	1	Yes		N = 2
32.768 kHz	0	1	0	Yes		N = 7
Any	1	1	0	No	Yes	—
Any	1	1	1	No	Yes	

Note: Other combinations of divider bits are used for test purposes only.

TABLE 5 - PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY

Select Bits Register A				4.194304 or 1.048576 MHz Time Base		32.768 kHz Time Base			
				RS3	RS2	RS1	RS0	Periodic Interrupt Rate 1/P	SQW Output Frequency
0	0	0	0	None	None	None	None	None	None
0	0	0	1	30.517 μs	32.768 kHz	3.90625 ms	256 Hz	3.90625 ms	256 Hz
0	0	1	0	61.035 μs	16.384 kHz	7.8125 ms	128 Hz	7.8125 ms	128 Hz
0	0	0	1	122.070 μs	8.192 kHz	122.070 μs	8.192 kHz	122.070 μs	8.192 kHz
0	1	0	0	244.141 μs	4.096 kHz	244.141 μs	4.096 kHz	244.141 μs	4.096 kHz
0	1	0	1	488.281 μs	2.048 kHz	488.281 μs	2.048 kHz	488.281 μs	2.048 kHz
0	1	1	0	976.562 μs	1.024 kHz	976.562 μs	1.024 kHz	976.562 μs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz	1.953125 ms	512 Hz	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz	3.90625 ms	256 Hz	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz	7.8125 ms	128 Hz	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz	15.625 ms	64 Hz	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz	31.25 ms	32 Hz	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz	62.5 ms	16 Hz	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz	125 ms	8 Hz	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz	250 ms	4 Hz	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz	500 ms	2 Hz	500 ms	2 Hz



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**PERIODIC INTERRUPT SELECTION**

The periodic interrupt allows the  $\overline{IRQ}$  pin to be triggered from once every 500 ms to once every 30.517  $\mu$ s. The periodic interrupt is separate from the alarm interrupt which may be output from once per second to once per day.

Table 5 shows that the periodic interrupt rate is selected with the same Register A bits which select the square-wave frequency. Changing one also changes the other. But each function may be separately enabled so that a program could switch between the two features or use both. The SQW pin is enabled by the SQWE bit in Register B. Similarly the periodic interrupt is enabled by the PIE bit in Register B.

Periodic interrupt is usable by practically all real-time systems. It can be used to scan for all forms of inputs from contact closures to serial receive bits or bytes. It can be used in multiplexing displays or with software counters to measure inputs, create output intervals, or await the next needed software function.

**UPDATE CYCLE**

The MC146818A executes an update cycle once per second, assuming one of the proper time bases is in place, the DVO-DV2 divider is not clear, and the SET bit in Register B is clear. The SET bit in the "1" state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the seconds byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code (11XXXXXX) is present in all three positions.

With a 4.194304 MHz or 1.048576 MHz time base the update cycle takes 248  $\mu$ s while a 32.768 kHz time base update cycle takes 1984  $\mu$ s. During the update cycle, the time, calendar, and alarm bytes are not accessible by the processor program. The MC146818A protects the program from reading transitional data. This protection is provided by switching the time, calendar, and alarm portion of the RAM off the microprocessor bus during the entire update cycle. If the processor reads these RAM locations before the update is

complete, the output will be undefined. The update in progress (UIP) status bit is set during the interval.

A program which randomly accesses the time and date information finds data unavailable statistically once every 4032 attempts. Three methods of accommodating nonavailability during update are usable by the program. In discussing the three methods, it is assumed that at random points user programs are able to call a subroutine to obtain the time of day.

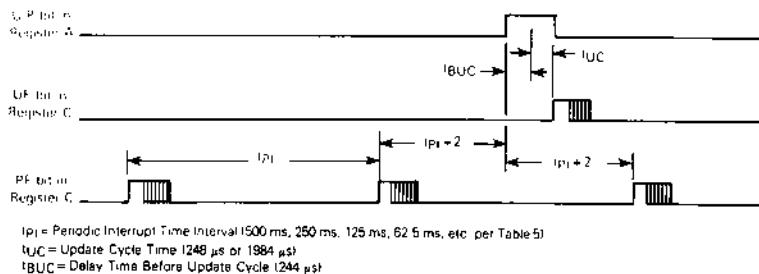
The first method of avoiding the update cycle uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information. During this time a display could be updated or the information could be transferred to continuously available RAM. Before leaving the interrupt service routine, the IRQF bit in Register C should be cleared.

The second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress or not. The UIP bit will pulse once per second. Statistically, the UIP bit will indicate that time and date information is unavailable once every 2032 attempts. After the UIP bit goes high, the update cycle begins 244  $\mu$ s later. Therefore, if a low is read on the UIP bit, the user has at least 244  $\mu$ s before the time/calendar data will be changed. If a "1" is read in the UIP bit, the time/calendar data may not be valid. The user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244  $\mu$ s.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 15). Periodic interrupts that occur at a rate of greater than  $t_{BUC} + t_{UC}$  allow valid time and date information to be read at each occurrence of the periodic interrupt. The reads should be completed within  $(t_{PI} + 2) + t_{BUC}$  to ensure that data is not read during the update cycle.

To properly setup the internal counters for daylight savings time operation, the user must set the time at least two seconds before the rollover will occur. Likewise, the time must be set at least two seconds before the end of the 29th or 30th day of the month.

FIGURE 15 - UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP



## REGISTERS

The MC146818A has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

### REGISTER A (\$0A)

MSB

b7	b6	b5	b4	b3	b2	b1	LSB	Read/Write Register except UIP
UIP	DV2	DV1	DVO	RS3	RS2	RS1	RS0	

UIP – The update in progress (UIP) bit is a status flag that may be monitored by the program. When UIP is a "1", the update cycle is in progress or will soon begin. When UIP is a "0", the update cycle is not in progress and will not be for at least 244  $\mu$ s (for all time bases). This is detailed in Table 6. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is zero – it is not in transition. The UIP bit is a read-only bit, and is not affected by Reset. Writing the SET bit in Register B to a "1" inhibits any update cycle and then clears the UIP status bit.

TABLE 6 – UPDATE CYCLE TIMES

UIP Bit	Time Base (TOSC1)	Update Cycle Time (tUCL)	Minimum Time Before Update Cycle (tBUCL)
1	4.194304 MHz	248 $\mu$ s	–
1	1.048576 MHz	248 $\mu$ s	–
1	32.768 kHz	1984 $\mu$ s	–
0	4.194304 MHz	–	244 $\mu$ s
0	1.048576 MHz	–	244 $\mu$ s
0	32.768 kHz	–	244 $\mu$ s

DV2, DV1, DVO – Three bits are used to permit the program to select various conditions of the 22-stage divider chain. The divider selection bits identify which of the three time-base frequencies is in use. Table 4 shows that time bases of 4.194304 MHz, 1.048576 MHz, and 32.768 kHz may be used. The divider selection bits are also used to reset the divider chain. When the time/calendar is first initialized, the program may start the divider at the precise time stored in the RAM. When the divider reset is removed, the first update cycle begins one-half second later. These three read/write bits are not affected by RESET.

RS3, RS2, RS1, RS0 – The four rate selection bits select one of 15 rates on the 22-stage divider, or disable the divider output. The rate selected may be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The program may do one of the following: 1) enable the interrupt with the PIE bit, 2) enable the SQW output pin with the SOWE bit, 3) enable both at the same time at the same rate, or 4) enable neither. Table 5 lists the periodic interrupt rates and the square-wave frequencies that may be chosen with the RS bits. These four bits are read/write bits which are not affected by RESET.

### REGISTER B (\$0B)

MSB

b7	b6	b5	b4	b3	b2	b1	LSB	Read/Write Register
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE	

SET – When the SET bit is a "0", the update cycle functions normally by advancing the counts once-per-second. When the SET bit is written to a "1", any update cycle in

progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. SET is a read/write bit which is not modified by RESET or internal functions of the MC146818A.

PIE – The periodic interrupt enable (PIE) bit is a read/write bit which allows the periodic-interrupt flag (PF) bit in Register C to cause the IRQ pin to be driven low. A program writes a "1" to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in Register A. A zero in PIE blocks IRQ from being initiated by a periodic interrupt, but the periodic flag (PIF) bit is still set at the periodic rate. PIE is not modified by any internal MC146818A functions, but is cleared to "0" by a RESET.

AIE – The alarm interrupt enable (AIE) bit is a read/write bit which when set to a "1" permits the alarm flag (AF) bit in Register C to assert IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code by binary 11XXXX). When the AIE bit is a "0", the AF bit does not initiate an IRQ signal. The RESET pin clears AIE to "0". The internal functions do not affect the AIE bit.

UIE – The update-ended interrupt enable (UIE) bit is a read/write bit which enables the update-end flag (UF) bit in Register C to assert IRQ. The RESET pin going low or the SET bit going high clears the UIE bit.

SQWE – When the square-wave enable (SQWE) bit is set to a "1" by the program, a square-wave signal at the frequency specified in the rate selection bits (RS3 to RS0) appears on the SQW pin. When the SQWE bit is set to a zero the SQW pin is held low. The state of SQWE is cleared by the RESET pin. SQWE is a read/write bit.

DM – The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or RESET. A "1" in DM signifies binary data, while a "0" in DM specifies binary-coded-decimal (BCD) data.

24/12 – The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode (a "1") or the 12-hour mode (a "0"). This is a read/write bit, which is affected only by software.

DSE – The daylight savings enable (DSE) bit is a read/write bit which allows the program to enable two special updates (when DSE is a "1"). On the last Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a "0". DSE is not changed by any internal operations or reset.

### REGISTER C (\$0C)

MSB

b7	b6	b5	b4	b3	b	b1	b0	LSB	Read-Only Register
IRQF	PF	AF	UF	0	0	0	0		

IRQF – The interrupt request flag (IRQF) is set to a "1" when one or more of the following are true:

$$PF = PIE = "1"$$

$$AF = AIE = "1"$$

$$UF = UIE = "1"$$

i.e.,  $IRQF = PF \cdot PIE + AF \cdot AIE + UF \cdot UIE$



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Any time the IROF bit is a "1", the IRQ pin is driven low. All flag bits are cleared after Register C is read by the program or when the RESET pin is low.

**PF** — The periodic interrupt flag (PF) is a read-only bit which is set to a "1" when a particular edge is detected on the selected tap of the divider chain. The R53 to R50 bits establish the periodic rate. PF is set to a "1" independent of the state of the PIE bit. PF being a "1" initiates an IRQ signal and sets the IRQF bit when PIE is also a "1". The PF bit is cleared by a RESET or a software read of Register C.

**AF** — A "1" in the AF (alarm interrupt flag) bit indicates that the current time has matched the alarm time. A "1" in the AF causes the IRQ pin to go low, and a "1" to appear in the IRQF bit, when the AIE bit also is a "1." A RESET or a read of Register C clears AF.

**UF** — The update-ended interrupt flag (UF) bit is set after each update cycle, when the UIE bit is a "1", the "1" in UF causes the IRQF bit to be a "1", asserting IRQ. UF is cleared by a Register C read or a RESET.

**b3 TO b0** — The unused bits of Status Register 1 are read as "0's". They can not be written.

#### REGISTER D (90D)

MSB	b7	b6	b5	b4	b3	b2	b1	LSB	Read Only
VRT	0	0	0	0	0	0	0	0	Register

**VRT** — The valid RAM and time (VRT) bit indicates the condition of the contents of the RAM, provided the power sense (PS) pin is satisfactorily connected. A "0" appears in the VRT bit when the power sense pin is low. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is a read only bit which is not modified by the RESET pin. The VRT bit can only be set by reading Register D.

**b6 TO b0** — The remaining bits of Register D are unused. They cannot be written, but are always read as "0's."

#### TYPICAL INTERFACING

The MC14681BA is best suited for use with microprocessors which generate an address-then-data multiplexed bus. Figures 16 and 17 show typical interfaces to bus-compatible processors. These interfaces assume that the address decoding can be done quickly. However, if standard metalgate CMOS gates are used, the CS setup time may be violated. Figure 16 illustrates an alternative method of chip selection which will accommodate such slower decoding.

The MC14681BA can be interfaced to single-chip microcomputers (MCU) by using eleven port lines as shown in Figure 19. Non-multiplexed bus microprocessors can be interfaced with additional support.

There is one method of using the multiplexed bus MC14681BA with non-multiplexed bus processors. The interface uses available bus control signals to multiplex the address and data bus together.

An example using either the Motorola MC6800, MC6808, MC6809 microprocessor is shown in Figure 20. When the MC14681BA is I/O mapped as shown in Figures 19 and 20, the AS and DS inputs should be left in a low state when the part is not being accessed. Refer to the STBY pin description for the conditions which must be met before STBY can be recognized.

Figure 21 illustrates the subroutines which may be used for data transfers in a non-multiplexed system. The subroutines should be entered with the registers containing the following data:

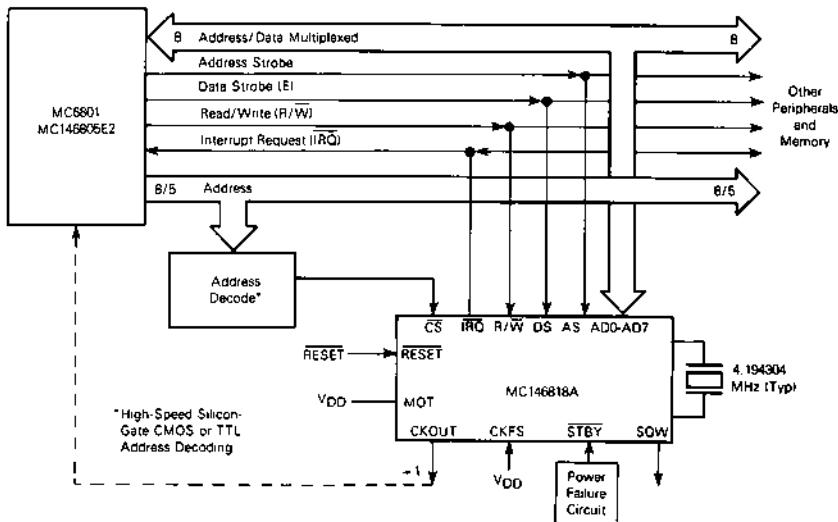
Accumulator A: The address of the RTC to be accessed.

Accumulator B: Write: The data to be written.

Read: The data read from the RTC.

The RTC is mapped to two consecutive memory locations — RTC and RTC+1 as shown in Figure 20.

FIGURE 16 — MC14681BA INTERFACED WITH  
MOTOROLA COMPATIBLE MULTIPLEXED BUS MICROPROCESSORS



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**FIGURE 17 - MC146818A INTERFACED WITH COMPETITOR COMPATIBLE MULTIPLEXED BUS MICROPROCESSORS**

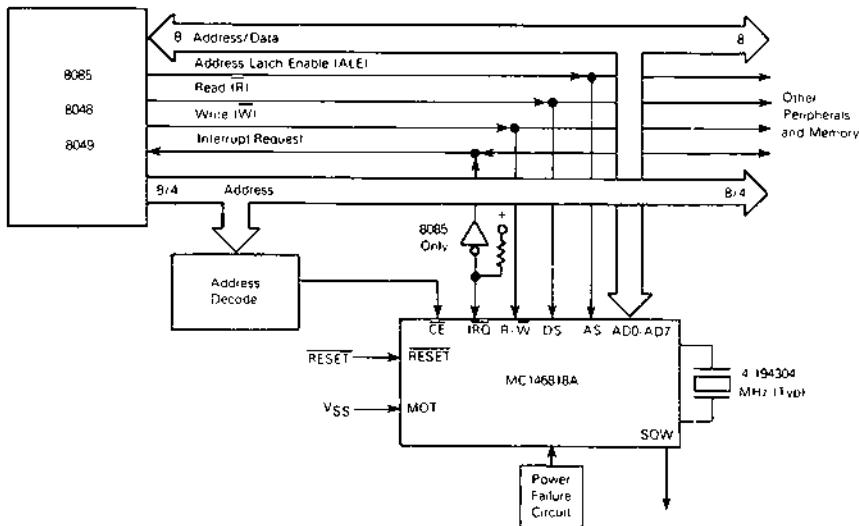
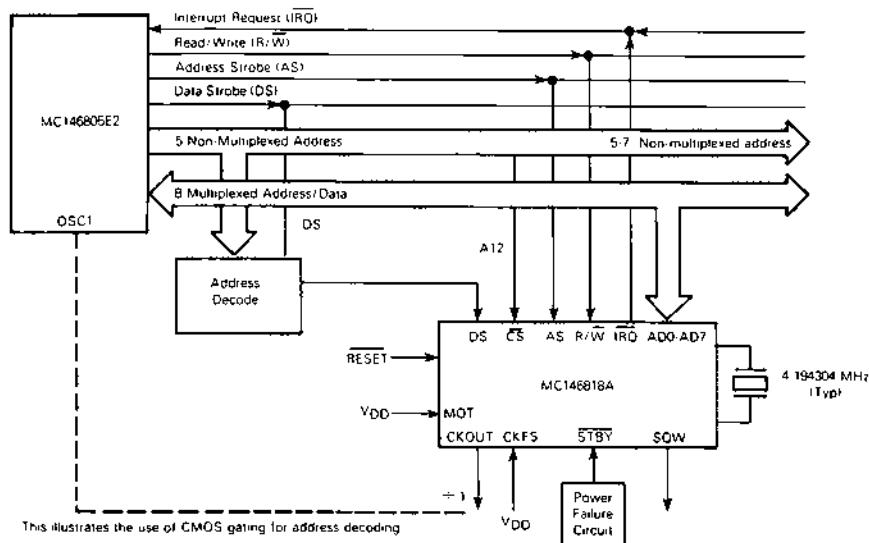
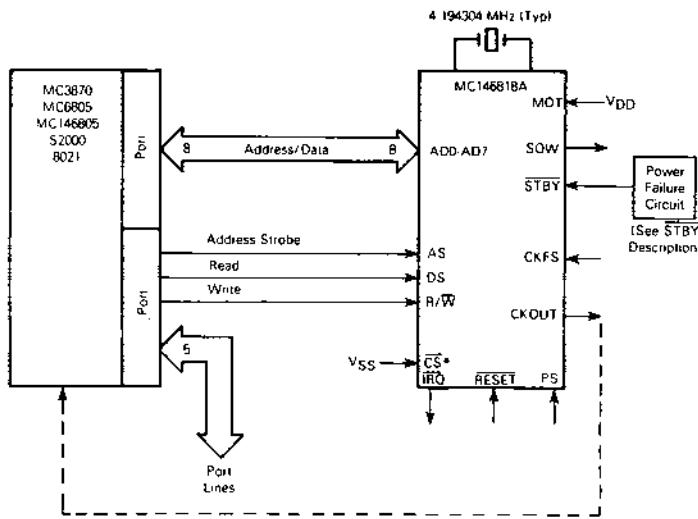


FIGURE 18 — MC146818A INTERFACE WITH MC146805E2  
CMOS MULTIPLEXED MICROPROCESSOR WITH SLOW ADDRESSING DECODING



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FIGURE 19 — MC146818A INTERFACED WITH THE PORTS OF A  
TYPICAL SINGLE CHIP MICROCOMPUTER



\* NOTE: CS can be controlled by a port pin if available.

FIGURE 20 — MC146818A INTERFACED WITH MOTOROLA PROCESSORS

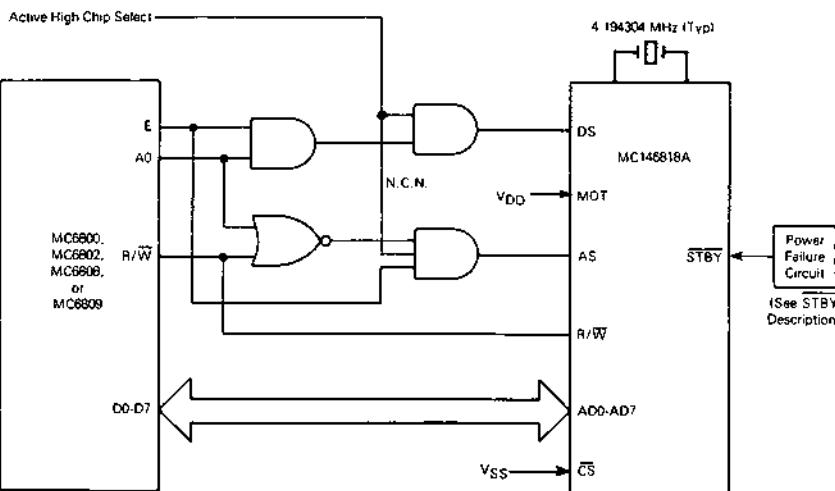


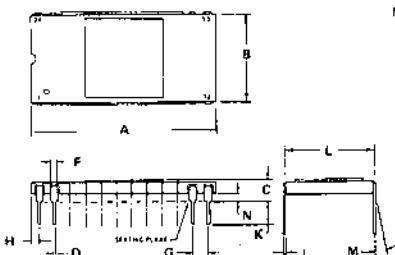
FIGURE 27 - SUBROUTINE FOR READING AND WRITING  
THE MC146818A WITH A NON-MULTIPLEXED BUS

READ	STA	RTC	Generate AS and Latch Data from ACCA
	LDAB	RTC + 1	Generate DS and Get Data
	RTS		
WRITE	STA	RTC	Generate AS and Latch Data from ACCA
	STAB	RTC + 1	Generate DS and Store Data
	RTS		



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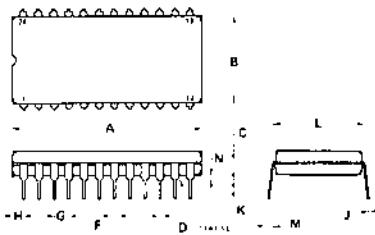
### PACKAGE DIMENSIONS



- NOTE:**
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010 INCH) AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
  2. DIM 'L' TO CENTER OF LEADS WHEN FORMED PARALLEL.

MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX
A	27.64	30.99	1.088	1.220
B	14.73	15.34	0.580	0.614
C	2.67	4.32	0.105	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.39	0.008	0.012
K	2.54	4.57	0.100	0.180
L	14.99	15.49	0.590	0.610
M	-	10°	-	10°
N	1.02	1.52	0.040	0.060

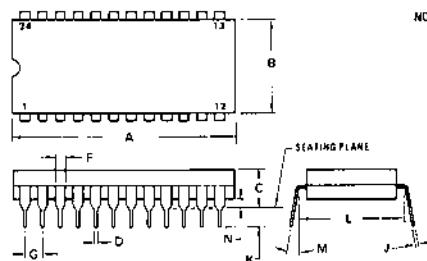
**L SUFFIX**  
CERAMIC PACKAGE  
CASE 716-06



- NOTES**
1. POSITIONAL TOLERANCE OF LEADS (I) SHALL BE WITHIN 0.25 mm (0.010 INCH) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
  2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.57	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

**P SUFFIX**  
PLASTIC PACKAGE  
CASE 709-02



- NOTES:**
1. DIM 'L' TO CENTER OF LEADS WHEN FORMED PARALLEL.
  2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)

MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.616
C	4.05	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.57	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.29	4.06	0.090	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

**S SUFFIX**  
CERDIP PACKAGE  
CASE 623-04

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**MOTOROLA Semiconductor Products Inc.**

3501 ED BLUESTEIN BLVD AUSTIN TEXAS 78721 • A SUBSIDIARY OF MOTOROLA INC

## ENGINEERING SPECIFICATION

Floppy Read/Write Support Device

WD16C92

P/N: 62-003037-00

REV.	ECO	DESCRIPTION	APPR.	DATE
TOLERANCES (EXCEPT (AS NOTED)	SIGNATURE	DATE	<b>WESTERN DIGITAL</b> CORPORATION	
PLACES $\text{XX} \pm .010$ $\text{XXX} \pm .005$	CHECK <i>J. Moore</i>	8/26/85	TITLE ENGINEERING SPECIFICATION WD16C92	
ANGLES $\pm 0^\circ 30'$	HOLES $+.004$ $-.001$	ENGINEER <i>J. Moore</i>	DWG SIZE 	DRAWING NUMBER 96-000190 REV X0
DO NOT SCALE DWG			SCALE	SHT 1 OF 19

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Reorder No A26733

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FIGURES



**RADIO SHACK, A Division of Tandy Corporation**

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