EMIF06-10006F1

6 LINES EMI FILTER AND ESD PROTECTION

IPAD™

MAIN PRODUCT CHARACTERISTICS

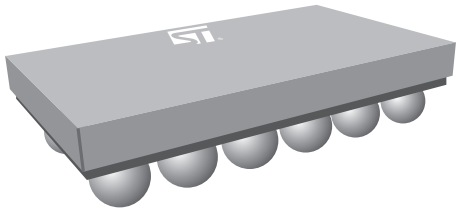
Where EMI filtering in ESD sensitive equipment is required:

- Mobile phones
- Computers and printers
- Communication systems
- MCU Boards

DESCRIPTION

The EMIF06-10006F1 is a highly integrated devices designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF06 flip-chip packaging means the package size is equal to the die size.

This filter includes an ESD protection circuitry which prevents the device from destruction when subjected to ESD surges up 15kV. This device includes 6 EMIF filters.



Flip-Chip package

BENEFITS

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Very low PCB space consuming: 2.92mm x 1.29mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression (IEC61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration and wafer level packaging.

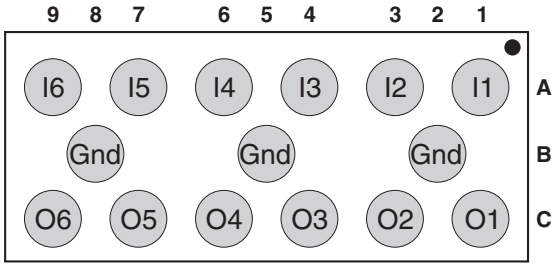
COMPLIES WITH THE FOLLOWING STANDARDS :

IEC 61000-4-2 level 4:

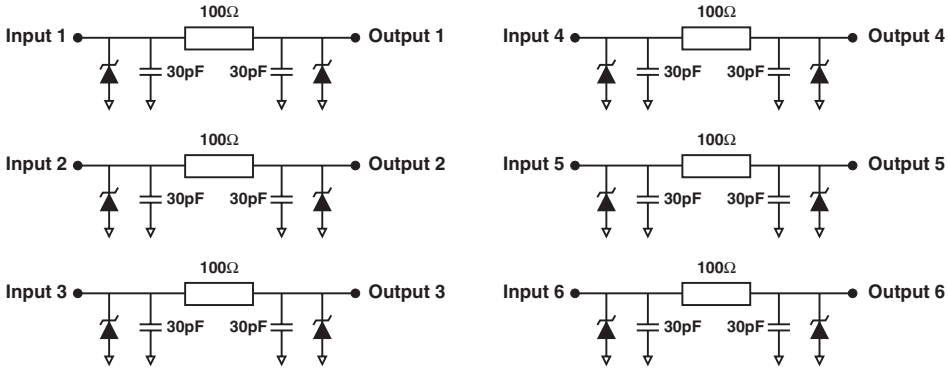
15kV (air discharge)
8 kV (contact discharge)

MIL STD 883E - Method 3015-6 Class 3: 30kV

PIN CONFIGURATION (ball side)



BASIC CELL CONFIGURATION



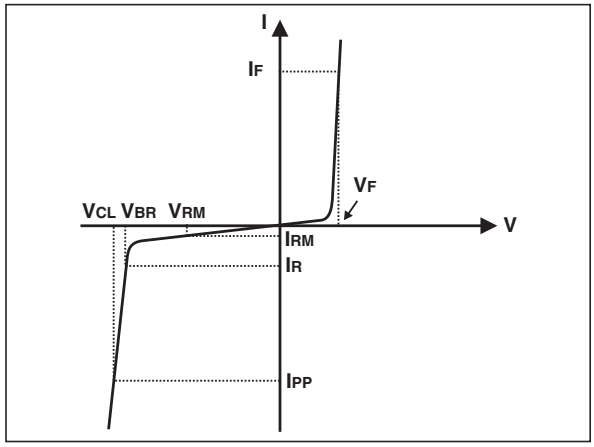
TM : IPAD is a trademark of STMicroelectronics.

ABSOLUTE RATINGS (limiting values)

Symbol	Parameter and test conditions	Value	Unit
P_R	DC power per resistance	0.1	W
P_T	Total DC power per package	0.6	W
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	-40 to + 85	°C
T_{stg}	Storage temperature range	125	°C

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input and Output
C_{line}	Capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	5.5	7	9	V
I_{RM}	V_{RM} = 3.3 V per line			500	nA
$R_{I/O}$	I = 10 mA	80	100	120	Ω
C_{line}	V_R = 2.5 V, F = 1 MHz, 30 mV (on filter cells)	50	60	70	pF

Fig. 1: S21 (dB) attenuation measurements and Aplac simulation.

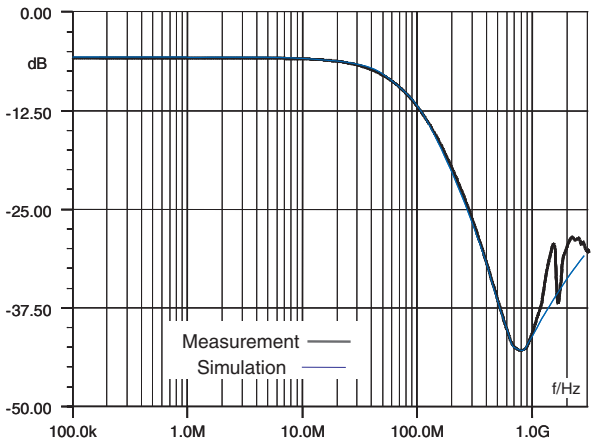


Fig. 2: Analog crosstalk measurements.

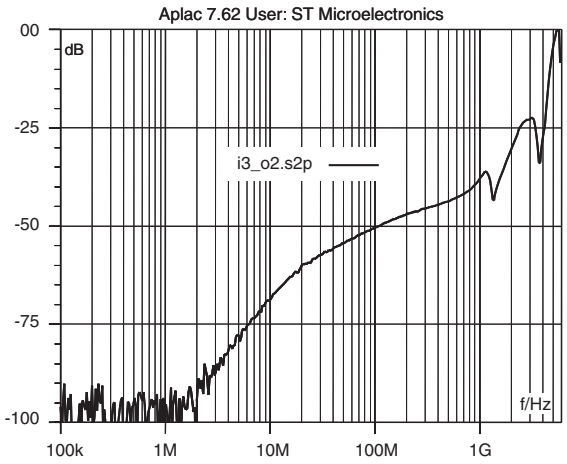


Fig. 3: Digital crosstalk measurements.

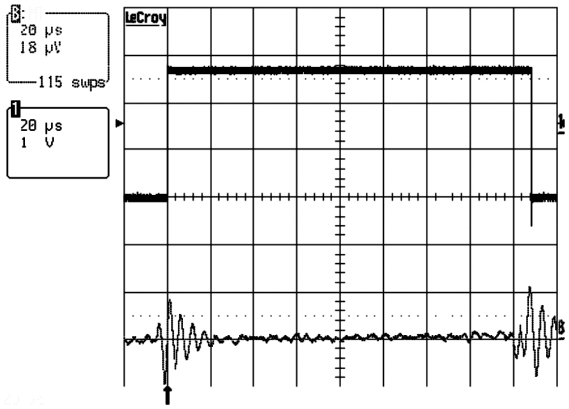


Fig. 4: ESD response to IEC61000-4-2 (+15kV air discharge) on one input V(in) and one output V(out).

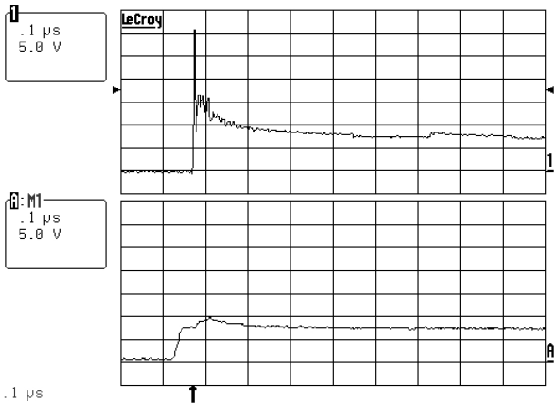


Fig. 5: ESD response to IEC61000-4-2 (-15kV air discharge) on one input V(in) and one output V(out).

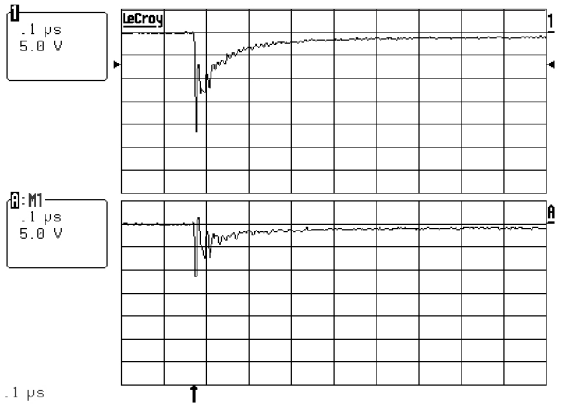
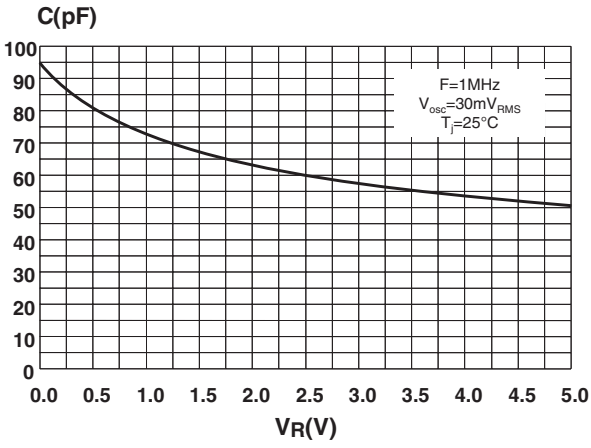
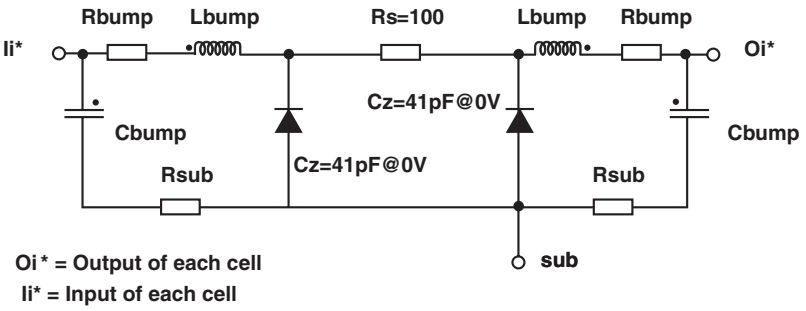


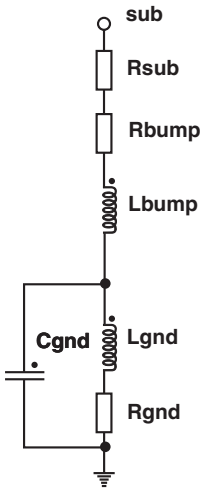
Fig. 6: Line capacitance versus applied voltage for filter.



Aplac model



EMIF06-10006F1 model

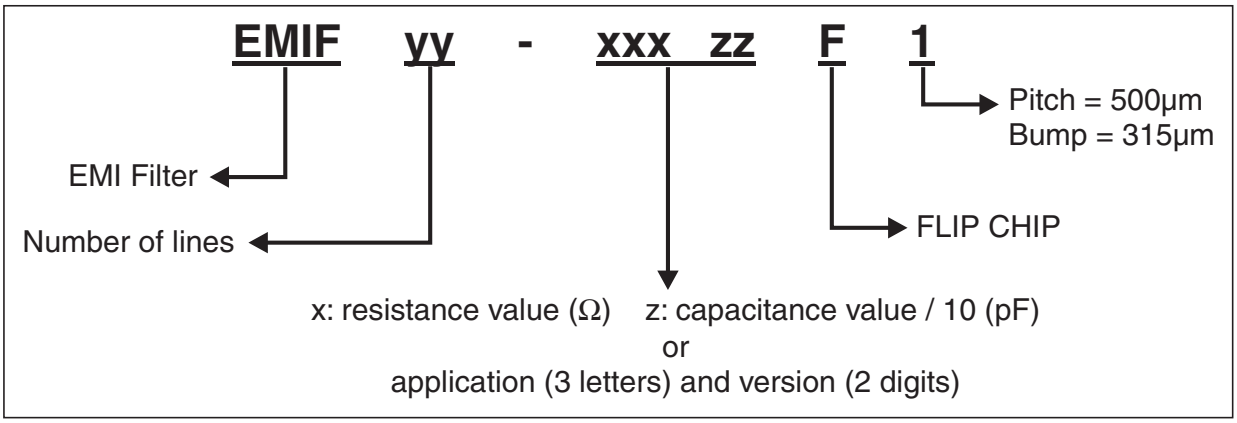


Ground return for each GND bump

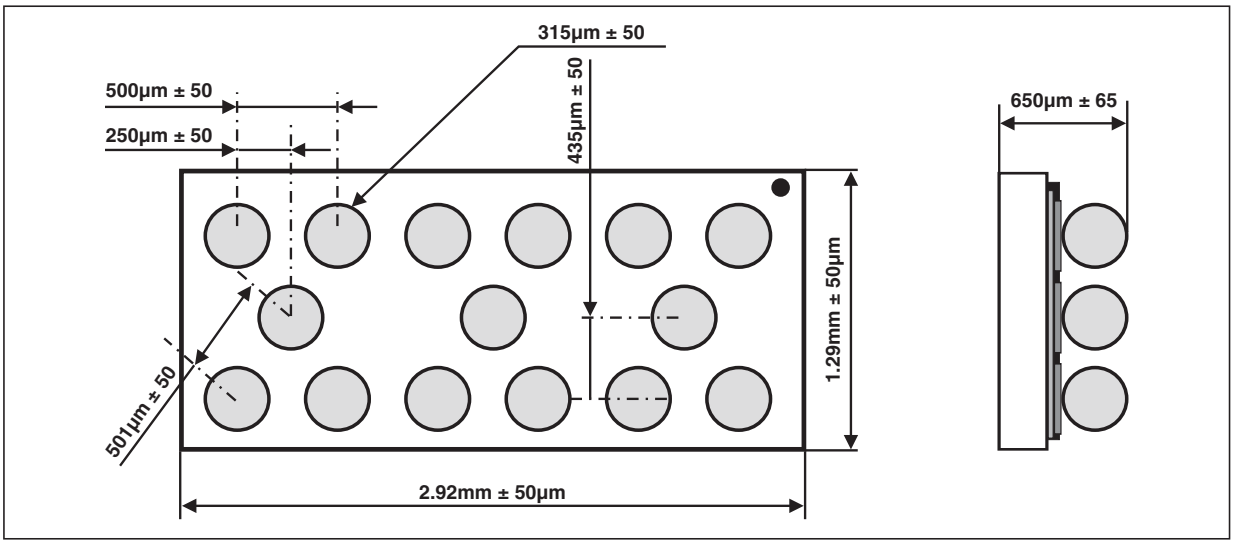
Aplac parameters

aplacvar Rs	100 Ω
aplacvar Cz	41 pF
aplacvar Lbump	50 pH
aplacvar Rbump	20 m
aplacvar Cbump	1.2 pF
aplacvar Rsub	100 m
aplacvar Rgnd	100 m
aplacvar Lgnd	100 pH
aplacvar Cgnd	0.15 pF

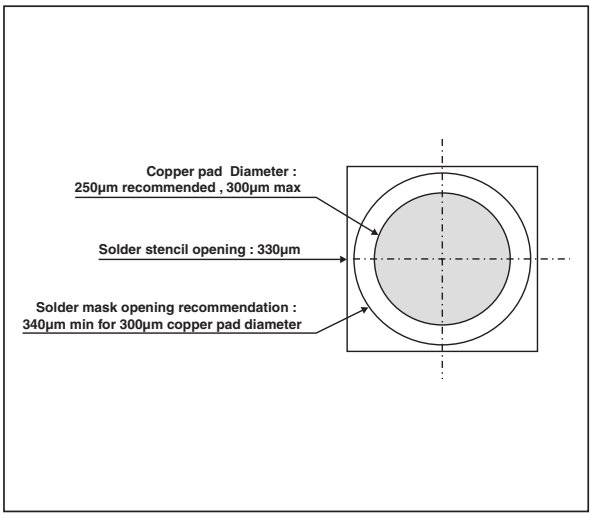
ORDER CODE



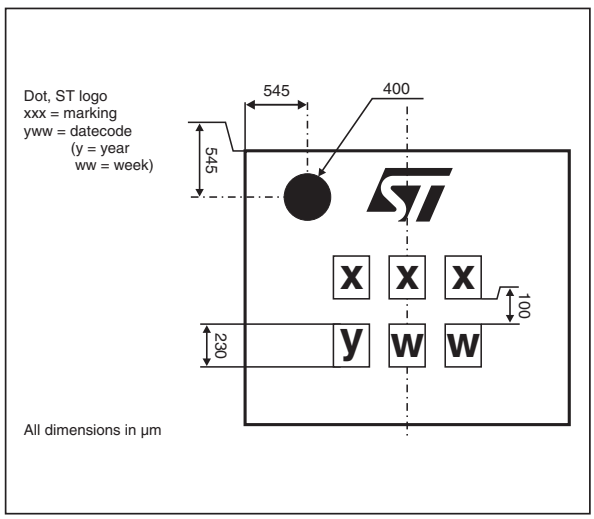
PACKAGE MECHANICAL DATA



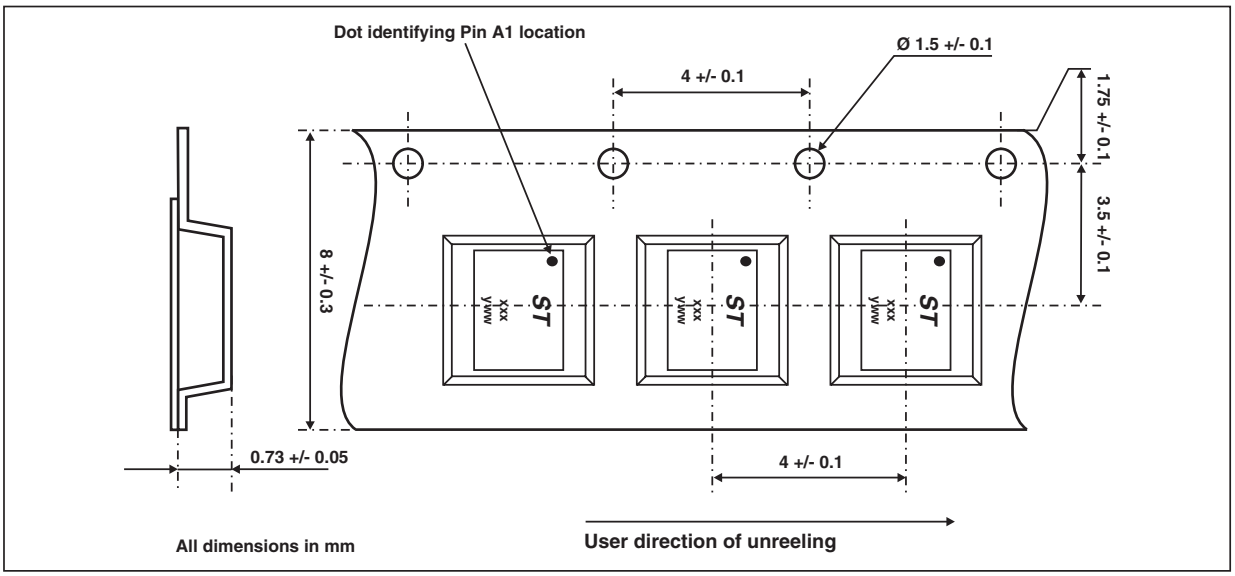
FOOT PRINT RECOMMENDATIONS



MARKING



FLIP-CHIP TAPE AND REEL SPECIFICATION



OTHER INFORMATION

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF06-10006F1	FTT	Flip-Chip	5.4 mg	5000	Tape & reel

Note: More packing informations are available in the application note AN1235: "Flip-Chip: Package description and recommandations for use"