2006 Signal Integrity Design Suite

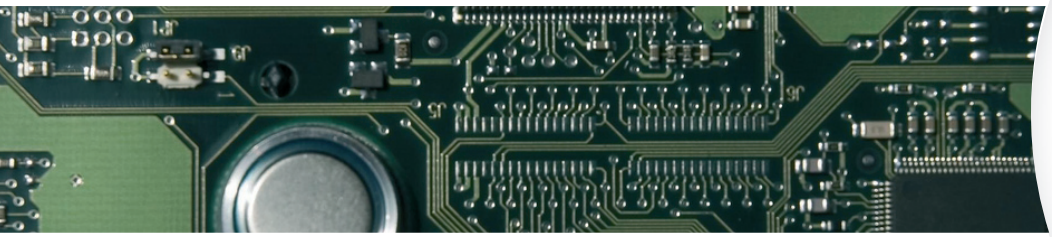
The industry's first high-speed, cross domain signal integrity design solution

Benefits

- Identify, analyze, and fix signal integrity issues early in the design cycle
- Reduce or eliminate design iterations, speeding time-to-market
- Designs perform to specifications the first time

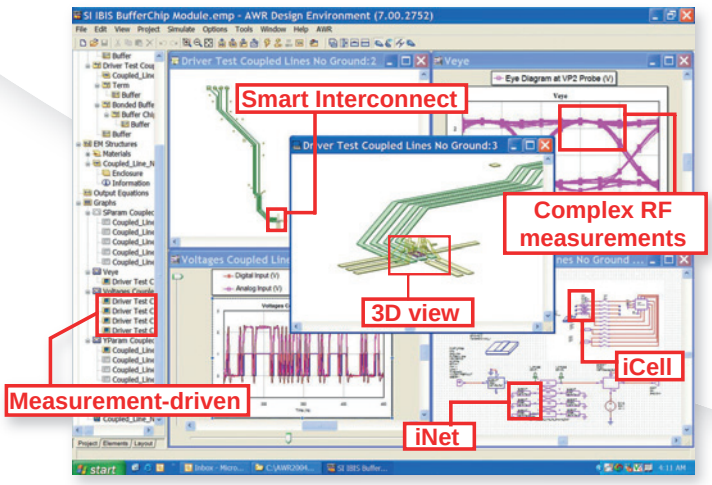
Key Features

- Powerful, concurrent, and unified signal integrity analysis environment for high-frequency/high-speed designs
- Supports multiple technologies including IC, package, module, and PCB
- Supports signals from hardware, IBIS models or MatLab™ co-simulation
- Supports multiple electromagnetic (EM) simulation and analysis tools



including AWR EMSight™ technology

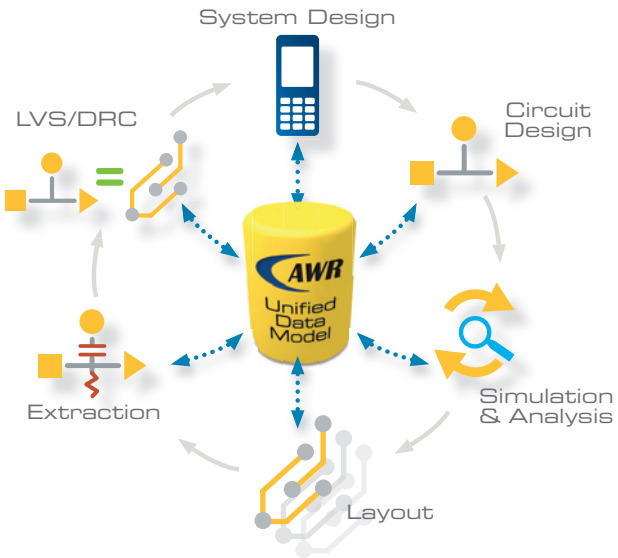
- Ability to import/support multiple models such as circuit netlist (SPICE or Spectre format), IBIS, S-parameter block, etc.
- Utilizes Intelligent Net™ (iNet) technology to extract and model complex cross-domain interconnects "on-the-fly"
- Includes high-speed high-capacity AWR harmonic balance simulator for comprehensive and accurate frequency-domain simulation
- Integrated with Synopsys' HSPICE for fast and accurate time-domain simulation or higher quality multi-domain signal integrity analysis



AWR Signal Integrity solution

Overview

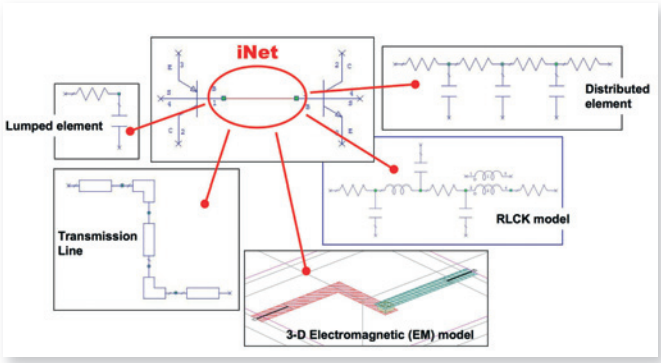
The AWR SI 2006 design suite is a new and highly integrated co-chip/package/module EDA solution developed specifically to address the complex cross-domain signal integrity issues inherent in the design of next-generation, high-performance/high-frequency products. The new solution is architected from the ground up, incorporating a unified data model (UDM) to ensure complete design closure between integrated circuit (IC), package, module, and printed circuit board (PCB) design phases. The unique AWR Design Environment™ encompasses all of these domains, and the data model is high-frequency aware, permitting accurate extraction and modeling of all design elements, including active and passive devices as well as interconnects at high frequency. The new solution is built on an open, standards-based software platform, enabling easy integration of the most capable, best-in-class tools to capture, synthesize, simulate, optimize, layout, extract, and verify designs in all domains.



The Signal Integrity 2006 design suite provides better Integration of best-in-class tools through the modern AWR open design platform

Interconnect-driven design with iNet technology

Gigahertz broadband SI issues are difficult to tackle because they cross so many boundaries. Because of the complex interactions of many effects, AWR SI 2006 design suite approaches the problem in two completely new ways. First, SI design suite enables interconnects to be designed in a top down process and, second, it provides procedures in this process for exploring the depth and breadth of SI issues. The first task is accomplished by incorporating AWR's industry-leading RF/microwave technology at the core of the software. Using the AWR Design Environment unified data model, interconnects can be defined at the circuit level and then manipulated through multiple representations as the problem solution evolves: layout, electromagnetic (EM), extraction, system, etc. This is combined with integration to the PCB tools that couple with this top-down flow and allow SI physical information to be brought back into the interconnect design subflow.



Interconnect-driven design with Intelligent Net (iNet) technology

The second task is accomplished using the AWR Design Environment. Through the unified data model, all manifestations of the interconnect—circuit, layout, EM, extracted, system, etc.—are simultaneously represented and available. SI engineers can switch "views" of the interconnect, without the need for translations, loss of information, and desynchronization of the database. Furthermore, the AWR Design Environment open architecture enables the SI designer to use multiple, complementary tools for the same task to bring the best approach to bear on the problem.

Industrial strength EMSight

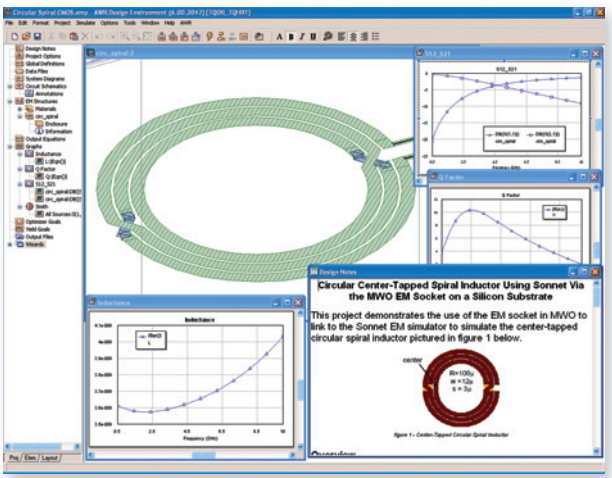
The typical RF/microwave approach to signal integrity design problems is to put the whole PCB or module into a three-dimen-sional (3D) EM solver and wait for a week to get an answer. This approach has gained in popularity because 3D EM solvers can be shown to provide compelling accuracy for some of the toughest SI problems. The problem with this approach is that all the engineer gets is "go/no-go" answers. If the EM solver does not crash and a solution is returned, the jumble of coupling data is difficult or impossible to pick apart in order to discern the primary and secondary physical mechanisms at the root of the SI problem for that design. 3D EM, and all EM methods, have value in specific subsets of the SI problem and are valuable tools in unraveling SI issues. However, it is rare, when putting an entire 12-layer low temperature cofired ceramic (LTCC) into an EM solver, that it will yield the root cause of SI problems. Where other SI/EM solutions crash, the EMSight technology in SI 2006 design suite succeeds. The matrix solvers have increased capacity, which eliminates the memory limitations of previous versions (typical limit of 8000 unknowns in 1GB of RAM). Now problems can be solved with 50,000+ unknowns in 512MB of RAM using dense out of core direct matrix solvers – there are no practical limits.

Support for multiple EM simulation and analysis tools

AWR SI 2006 design suite offers the broadest range of EM solvers, all with their own strengths when it comes to tough SI problems, which can be used to partition the problem and get accurate answers.

Signal integrity solutions available today are generally based on technology developed for SI issues at a few hundred MHz. These solutions "hit the wall" when distributed

coupling and broadband considerations come into play in applications approaching and above 1 GHz. For these highest-performance designs, interconnects are best-modeled in the frequency-domain with EM or EM-based models. SI design suite supports multiple technologies for traditional bottom up SI as well as top down interconnect design in all design domains. The software package includes all the features of AWR's RF/microwave design software: concurrent design, logical/physical design, EM table-based models, and EM Socket™ open integration. For the first time, engineers can design interconnects as well as analyze them. The software builds on AWR's proven, industry-leading interconnect modeling and simulation technology by adding time-domain simulation and a closed-loop flow with major PCB tools.



AWR supports integration with third-party EM simulators

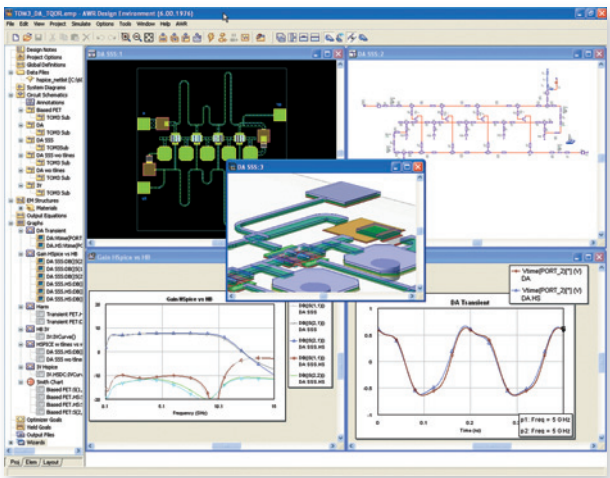
Through AWR's EM Socket open standard interface, SI 2006 design suite users can access a broad variety of EM simulators from leading vendors, without leaving the SI design environment. The underlying technology can interface with virtually any EM simulator and seamlessly integrates third-party design tools into the SI design flow. Users can combine multiple EM algorithms, such as finite element analysis, finite difference time domain (FDTD), and a variety of method-of-moments approaches to solve planar and full 3D problems. The solution facilitates greater flexibility in the design methodology, while providing a common user interface.

Signals: internally or test-generated, IBIS, or MatLab co-simulation

As clock rates and signal speeds increase, designers have found that a simple current source is insufficient to model the complexities of fast, leading-edge signals, variable fan-outs, dense interconnects, and complex loads and receivers. SI 2006 supports several ways of generating signals for SI design and analysis. The simplest way is to use the internal frequency- and time-domain sources. By adding on AWR's TestWave™ software, signals can be acquired and used directly from test equipment or from the designer's own device hardware. IBIS is also supported and, if models are available in MatLab, AWR's Visual System Simulator™ (VSS) system simulation tool co-simulates with MatLab to bring the signals right into the AWR Design Environment, where trade-offs can be made in real time.

Flows into industry-popular third-party tools

The ability to design interconnects as part of a top-down, SI flow is unique. SI design suite offers a truly useable design flow by creating a closed-loop flow to popular, enterprise PCB tools. Schematics and layouts can be exported to Mentor Graphics BoardStation using libraries and footprints automatically generated from BoardStation, LMS, or DMS, and can continue in the enterprise PCB flow for bill-of-materials (BOM) generation, routing, and design-for-manufacturing (DFM). High-speed, multi-level traces of interest can be brought back into SI design suite and analyzed as-is or with user-selectable adjacent metal.



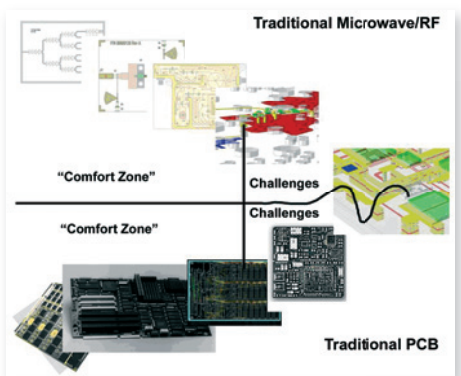
HSPICE for fast and accurate simulations

Integrated with Synopsys' HSPICE for fast and accurate simulations

AWR's time-domain engine is included in the AWR SI 2006 design suite, and is integrated with Synopsys' gold standard HSPICE software, providing the fastest, most accurate, highest capacity simulations, as well as hundreds of foundry-proven built-in device models for most commercial IC foundries. Synthesized schematics and related analyses can then be stored and viewed directly in the AWR design platform.

Typical SI design challenges

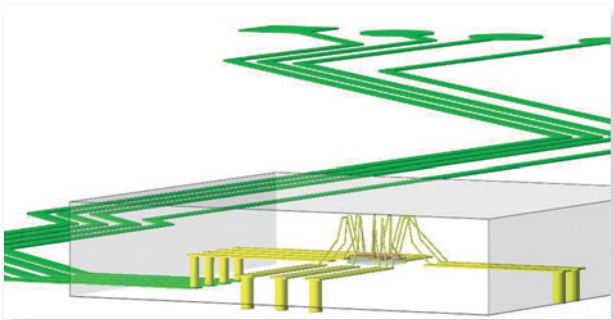
Many of the challenges new to the IC and PCB world have been a reality for decades in RF/microwave design. AWR has integrated into the AWR SI design suite many of the tried-and-true techniques and proven solutions used in microwave design, making them easily accessible to IC and PCB designers. The following problems examine some typical SI design problems and offer a solution made possible through the unique AWR SI software.



Many typical challenges for RF/microwave design are new to IC and PCB design

Problem: Dispersive interconnects

At frequencies up to a few hundred MHz, current on an IC, package, or PCB metal interconnect in general behaves itself and its distribution across the conductor's cross-section remains constant, making it very easy to model short, coupled lines with resistors (Rs) and capacitors (Cs). By making the lines a little longer, it is also possible to extend this modeling approach with the introduction of some inductance (L). Standard SI technologies took advantage of this with fast extraction and reduction techniques using RC and RLC networks. When the frequency is increased a little bit further, something odd begins to happen: the wire loss is no longer constant. The current, rather than being evenly distributed throughout the wire, begins to crowd toward the surface at a frequency-dependent rate. Coupled with dielectric losses that also vary with frequency, this results in interconnect properties that are dispersive and lumped element techniques break down. The simplifications to the physics of signal propagation, Maxwell's equations, that make RLC practical at lower frequencies, break down at these frequencies. RF/microwave designers encountered this problem many years ago, and created dispersive transmission line models such as microstrip, stripline, and coplanar waveguide, that incorporate the frequency-dependent characteristics of the lines in a single model that run from DC to 100s of GHz. AWR SI software uses these models, which are proven over tens of thousands of designs, and, in addition, uses the same model regardless of the simulator.



Design issues are compounded when the previously packaged IC is integrated onto a PCB

Problem: Multi-domain analysis

For the design of ICs, an IC suite with IC timing analysis is needed. For the design of PCBs and modules, a PCB tool with SI tools is required. In the GHz range, the packaging of the die not only degrades the performance, but couples to the operation of the die, making it almost impossible to design the IC separately from the package. All of these issues are compounded when the previously packaged IC is integrated onto a PCB.

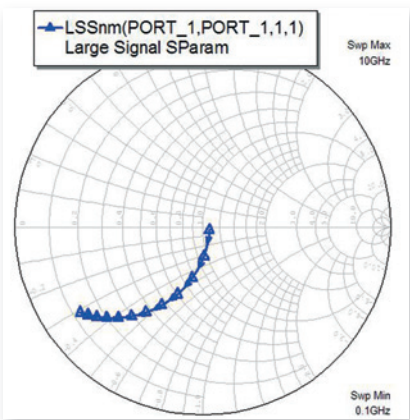
Traditional IC tools are difficult to adapt to PCB design because they do not support packaged components very well and PCB tools have a limited notion of continuously scalable layout cells. The result has been flows that span half a dozen or more disparate tools, which requires that data be translated, designs be manually repaired, and the database be synchronized by hand, all with no guarantee of closure across the domains.

The AWR SI design suite leverages the fact that microwave designers have been doing "chip and board" design for decades. The single, integrated AWR design platform does not differentiate among IC, package, and chip, consequently all three design issues are addressed on an equal basis within the same project without the need for translation.

Problem: Signal sources and IP access: IBIS, Encrypted HSPICE, and MatLab

Component vendors and other intellectual property (IP) providers walk a precarious line. They need to provide their customers with compact, efficient, and accurate models for the pin I/Os on their parts, but, at the same time, they don't want to give away the "family jewels. " One approach proposed by some is to simply use the ideal voltage and current waveforms coming out of drivers. The problem with this is that it does not capture the subtle, dynamic impedance changes of the driver, nor the nonlinear loading of the driver by the interconnect and receiver. Simply designing something like an LVDS driver with a DC or low frequency impedance of 50 ohms misses the dramatic impedance changes for broadband designs.

IBIS and SPICE models are a good solution, but they can expose too much information about vendors' technology. Encrypted HSPICE, has been a popular solution, and MatLab has been gaining support, but these are proprietary solutions.



Broadband LVDS driver output impedance varies from 50 ohms as the bandwidth of the design increases

AWR SI design suite supports all of these technologies. The integration of Mathworks MatLab and Synopsys' HSPICE directly into the AWR design environment ensures that SI design and analysis has direct access to all the most popular signal sources—protected and open—from component vendors.

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