

EMIF04-MMC02F1

 $IPAD^{TM}$

4 LINES EMI FILTER INCLUDING ESD PROTECTION

MAIN APPLICATION

■ MULTIMEDIACARD™

DESCRIPTION

The EMIF04-MMC02F1 is a highly integrated array designed to suppress EMI / RFI noise for MULTIMEDIACARD™ port filtering.

The EMIF04-MMC02F1 flip-chip packaging means the package size is equal to the die size. That's why EMIF04-MMC02F1 is a very small device.

Additionally, this filter includes an ESD protection circuitry which prevents the protected device from destruction when subjected to ESD surges up to $15\,\text{kV}$.

BENEFITS

- 4 lines low-pass-filter
- High efficiency in EMI filtering
- Very low PCB space consuming: < 3.3 mm²</p>
- Very thin package: 0.65 mm
- High efficiency in ESD suppression (IEC61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.

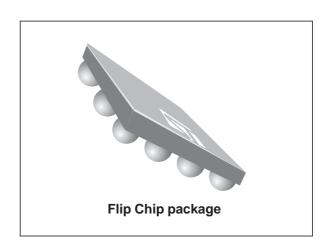
COMPLIES WITH THE FOLLOWING STANDARDS:

IEC 61000-4-2 Level 4:

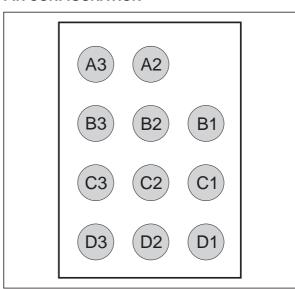
15kV (air discharge) 8 kV (contact discharge)

on input & output pins.

MIL STD 883E - Method 3015-6 Class 3



PIN CONFIGURATION

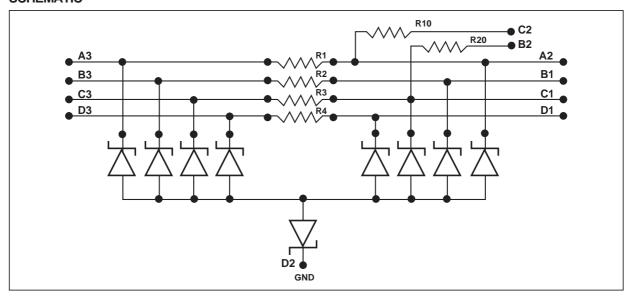


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EMIF04-MMC02F1

SCHEMATIC

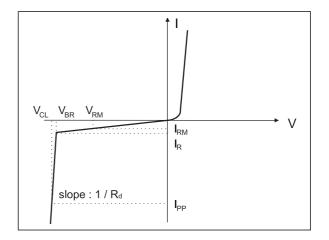


ABSOLUTE MAXIMUM RATINGS $(T_{amb} = 25 \text{ °C})$

Symbol	Parameter and test conditions	Value	Unit
V _{PP}	ESD discharge IEC61000-4-2, air discharge ESD discharge IEC61000-4-2, contact discharge	15 8	kV
Tj	Junction temperature	125	°C
T _{op}	Operating temperature range	-40 to + 85	°C
T _{stg}	Storage temperature range	-55 to +150	°C

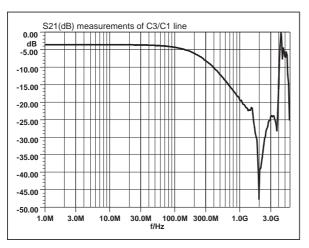
ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C)

Symbol	Parameter		
V_{BR}	Breakdown voltage		
I _{RM}	Leakage current @ V _{RM}		
V _{RM}	Stand-off voltage		
V _{CL}	Clamping voltage		
Rd	Dynamic impedance		
I _{PP}	Peak pulse current		



Symbol	Test conditions	Min.	Тур.	Max.	Unit
V _{BR}	I _R = 1 mA	6			V
I _{RM}	$V_{RM} = 3V$		0.1	0.5	μΑ
C _{line}	@ 0V			20	pF
R ₁ ,R ₂ ,R ₃ ,R ₄	Tolerance ± 5%		47		Ω
R ₁₀	Tolerance ± 5%		13		kΩ
R ₂₀	Tolerance ± 5%		56		kΩ
Р				70	mW

Fig. 1: Filtering measurements



Note: spikes at high frequencies are induced by the PCB layout.

Fig. 3: Line capacitance versus reverse applied voltage.

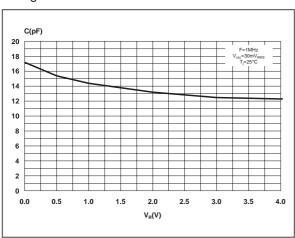
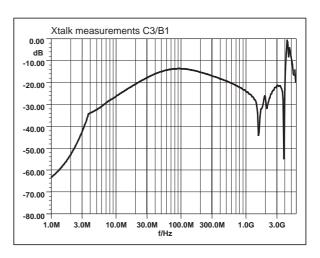


Fig. 2: Cross talk measurements



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Negative Surge

Fig. 4: ESD response to IEC61000-4-2 (+15kV contact discharge).

Positive Surge

APLAC MODEL

Fig. 5: Device structure

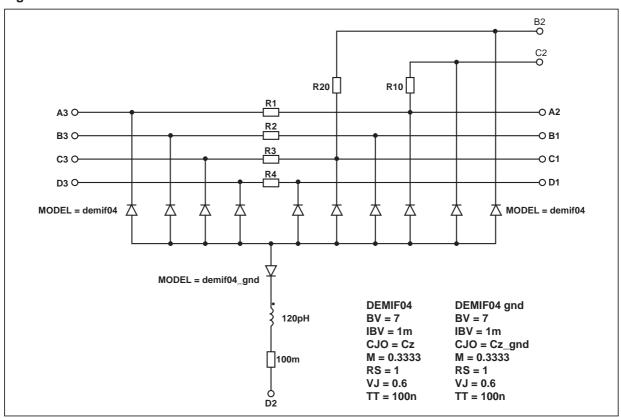


Fig. 6: Aplac model connections

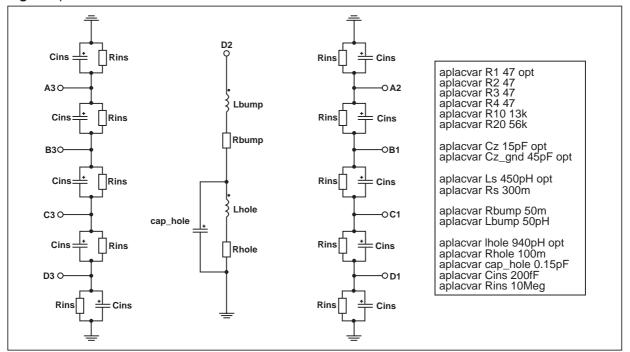
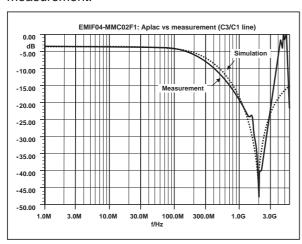
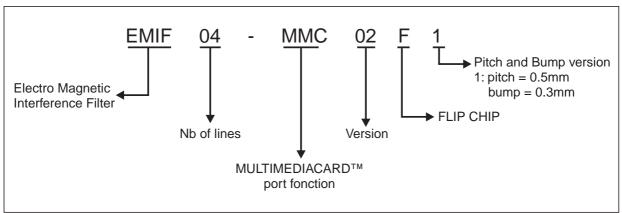


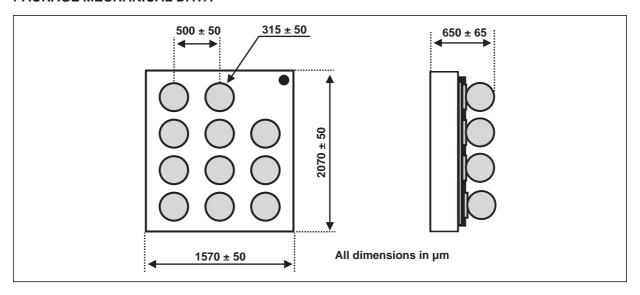
Fig. 7: Aplac simulation versus frequency measurement.



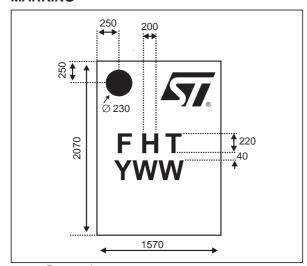
ORDER CODE



PACKAGE MECHANICAL DATA

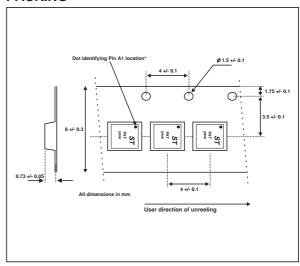


MARKING



- yww: Date code

PACKING



OTHER INFORMATION

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF04-MMC02F1	FHT	Flip-Chip	4.5 mg	5000	Tape & reel (7")

Note: More packing informations are available in the application note AN1235: "Flip-Chip: Package description and recommandations for use"

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