Understanding the value of signal integrity

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Problems between memory and other components often occur at the interfaces between these devices. Often, system-level issues can be subtle and hard to find. This article describes important tools that can easily identify and resolve the issues that may occur with memory interfaces, enabling designers to have a more robust design.

Historically, design engineers have used signal integrity testing in the design of new systems and for sustaining qualifications. Signal integrity, while extremely valuable in the engineering phase, is not a panacea. Its value diminishes as the product design progresses, and temperature and voltage margin testing should supplement or replace signal integrity for sustaining qualifications.

Proper selection of memory design, test and verification tools reduces engineering time and increases the probability of detecting potential problems. **Table 1** is a snapshot of five essential tools for memory design. This is not a complete list of memory design tools, as this article focuses on tools used to validate the functionality and robustness of a design. **Table 2** shows when the tools can be used most effectively.

It is rare to find a debug lab that does not include logic analyzers as an integral part of its design and debug process. However, due to the cost and time involved, logic analyzers are rarely the first tool used to detect a failure or problem in a system. Rather, they are used to debug a problem detected by compatibility or four-corner testing.

Development phases

Design

In this phase, a concept or idea is implemented in hardware. Because no prototype is available, only simulation tools can be used. Therefore, designers rely exclusively on electrical and behavioral simulation tools.

Alpha prototype

An alpha prototype is the first or early prototype. The alpha prototype will likely undergo changes prior to production (BIOS, functionality etc.).

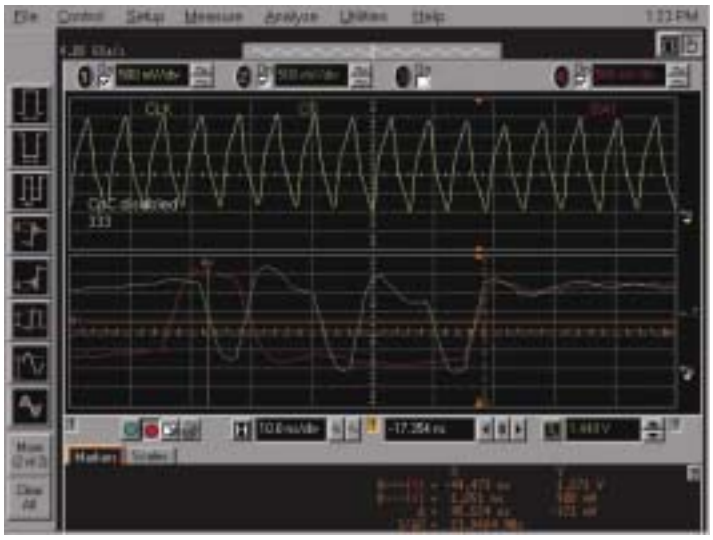

Figure 1: The scope shot shows signals from a single DDR SDRAM component: bank address 1, chip select signal and differential system clock.

Engineers must perform enough testing on the alpha prototype to ensure the next prototype will be nearly production-ready, at least from a hardware perspective. For this, certain tools are more useful than others.

The first tools used in this phase are a boot-up and software check. They yield valuable information and, coupled with basic software checks, provide data that may point to needed changes. A thorough software check may not yet be possible because basic hardware changes are likely.

Signal integrity is invaluable during this phase. It captures analog signals of traces on the circuit board. These captures can be compared to simulation or device specifications to determine if the device meets specifications and has an adequate timing margin. If not, improvements must be made.

One tool that should not be used in this phase, however, is margin testing. Margin testing should only be used after the hardware is stable. After running the appropriate tests, designers will have a list of changes that need to be implemented, including some that may need to be simulated electrically or behaviorally to ensure they have the desired effect.

Beta prototype

Here in this final prototype, the hardware is near production status. Only minor tweaks are expected. A combination of testing is used to make the system production-ready. Software or compatibility testing must be thorough. It can be performed alone or with margin testing. Margin testing should also be extensive. Varying temperature and voltage levels to their extremes is valuable in identifying problems and marginalities. This combination should catch the memory failures that are likely to occur.

Signal integrity has limited value in this phase, but can be used to debug functional failures or to validate changes made in the alpha prototyping phase. Signal integrity testing should not be used to verify signals or nets from the alpha prototype that has not changed. If any additional modifications are made during the beta prototyping phase, electrical and/or behavioral simulation may be necessary to validate them.

Production

Changes to a system are rare when it is in production. The focus turns to sustaining qualifications. Systems may be in production for a few months or for years. They may use hundreds or thousands of components. To remain in production, it is important that companies have a procedure for sustaining qualifications, which means performing a series of qualification tests on a component after a system is in production. These tests ensure that an adequate supply of components is available for uninterrupted production.

Motherboard traces and layouts rarely change in production. Signal integrity is unnecessary because it was already used to validate the changes. Furthermore, signal integrity cannot

Tool	Examples
Electrical simulation	SPICE or IBIS
Behavioral simulation	Verilog or VHDL
Signal integrity	Oscilloscope and probes; possibly mixed mode to allow for more accurate signal capture
Margin testing	Guardband testing and four-corner testing (varying voltage and temperature)
Compatibility testing	Functional software testing or system reboot test

Table 1: It pays to know what tools are needed in testing devices that require critical analysis.

catch failures that have historically caused system/memory-related issues. The preferred tools and the keys for sustaining qualifications are compatibility and margin testing.

Post production

Some systems, such as MP3 players or DVD recorders, require no sustaining qualifications after production ends. However, many other systems may require memory upgrades and support. This is common for notebooks, PCs and other devices, and can be critical for years after production ends. Margin testing and compatibility testing are the keys for sustaining qualifications.

SI testing

Electrical engineers are comfortable using an oscilloscope to look at a circuit design and evaluate the signals. **Figure 1** shows a typical signal integrity capture. In this case, the scope shot shows signals from a single DDR SDRAM component: bank address 1, chip select signal and differential system clock.

Signal integrity testing is the process of taking oscilloscope photographs of system signals to evaluate voltage changes over time. These photographs or "captures" are visually evaluated for out-of-specification conditions, which typically go through a time-consuming process that requires a high level of engineering expertise.

A signal integrity photo can reveal ringing, overshoot/undershoot and timing violations (slew rate, setup/hold time, bus contention etc.). If any of these conditions occur, they will likely cause a system failure that compatibility and margin testing can easily reveal. After the problem is revealed, other tools (logic analyzer, signal integrity etc.) can determine its cause.

Analysis, testing limits

Signal integrity analysis is becoming more difficult and time-consuming. In cases such as FBGA packages, it is impossible to probe signals unless probe points are added to a design. Some designs use multichip modules to combine a variety of chips together in a single package. These packages are either covered with a mold compound or sealed hermetically so internal signals cannot be probed.

Using a probe to measure signal integrity changes the signal being measured. Problems may arise with the addition of capacitance, or they may disappear. Although active or FET probes are available, this condition will become more common as frequency scales, especially in systems with a point-to-point architecture. Moreover, signal integrity is a poor tool for memory qualification or sustaining qualifications.

Signal integrity testing has its limits. Micron has taken quite a number of signal-integrity scope captures during multiple internal qualifications of memory and found out that using signal integrity at an early stage of development helps catch failures. However, signal integrity has little value after the board design becomes stable.

Micron's internal test flow has migrated from signal integrity testing to adopting compatibility and margin testing in validating or testing a system with memory. After compatibility or margin testing detects a failure, various diagnostic tools are used to isolate the failure.

Although a scope can be used, experience shows that other tools are more effective in quickly testing, validating and debugging the systems. These alternative tools let engineers quickly come to the root cause analysis and correction.

Based on Micron's findings, compatibility and margin testing regularly expose problems in a system. Signal integrity, on the other hand, did not find a single issue that was not identified by memory or system-level diagnostics. It found the same failures as the other tests, thus duplicating the capabilities of margin testing and software testing.

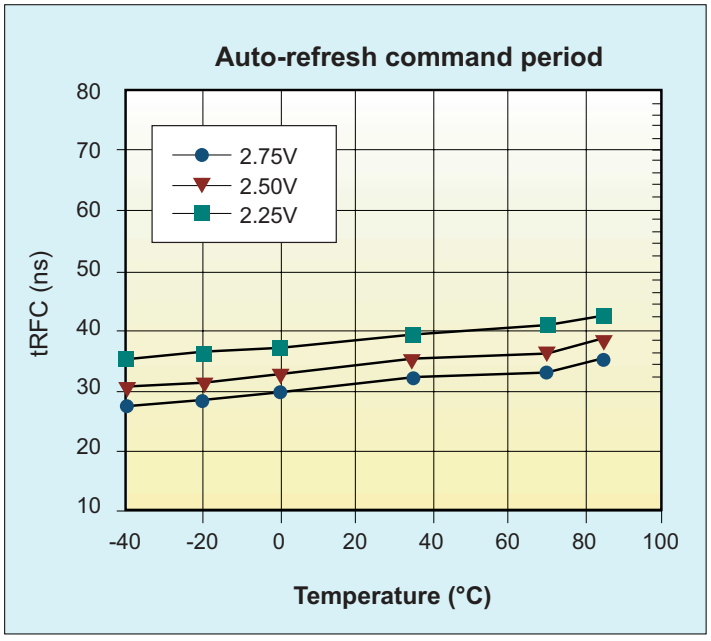

Figure 2: Voltage and temperature variations are evident in most device specifications, thus exposes the possible issues that need to be addressed.

Findings have also shown that signal integrity is time-consuming, costly and takes up valuable engineering resources.

Testing alternatives

The alternatives to signal integrity testing are used for development of systems and for memory qualification and testing. This section provides a brief description of these tools and how to use them.

Software tools or compatibility testing

Computer systems are ideal for software testing. Since computers can use off-the-shelf software, a variety of memory diagnostic tools are available. When considering software tools, companies should look for those that support dynamic upgrading and choose a program that incorporates new diagnostics as needed to catch previously unknown failure mechanisms.

Unlike PCs, other products such as consumer, embedded and networking products are more difficult to test. Designers of these types of applications develop home-grown tools or use none at all. Making home-grown tools more robust give better benefits than signal integrity testing. Note that sometimes a memory-specific test may be impossible in a system. In this case, the other tools described in this section should be used.

Margin testing

This stresses a system to find marginalities or problems. Two types of margin tests are extremely valuable: voltage and temperature stress tests. These stresses expose the DRAM and DRAM controller to conditions likely to reveal potential system issues. **Figure 2** shows an example of how specifications vary over temperature.

The four-corner test is a typical margin test that has proven to be one of the most effective ways of testing memory. It is also reasonable in terms of time to test and resources required. For a system with minimum and maximum voltages and temperatures of 3V and 3.6V and 0 °C and 70 °C, respectively, the four corners are:

- Corner 1–max. voltage, max. temperature: 3V, 70 °C;
- Corner 2–max. voltage, min. temperature: 3.6V, 0 °C;

Tool	Design	Alpha prototype	Beta prototype	Production	Post-production
Simulation – electrical	Essential	Very valuable	Limited value	Rarely used	No value
Simulation – behavioral	Essential	Very valuable	Limited value	Rarely used	No value
Signal integrity	Unavailable	Critical	Limited value	Rarely used	No value
Margin testing	Unavailable	Essential	Essential	Essential	Essential
Compatibility	Unavailable	Valuable	Essential	Essential	Essential

Table 2: There are several test methods to choose from; picking the right one is crucial.

- Corner 3–min. voltage, max. temperature: 3V, 70 °C;
- Corner 4–min. voltage, min. temperature: 3V, 0 °C.

Testing methodologies vary, but a typical procedure is to let the system stabilize (temperature and voltage) inside a temperature chamber. Then a series of tests are run at that corner. If failures occur, they should be investigated.

A variation is a two-corner test. The voltage to the memory may be controlled by a voltage regulator, so there is no way of adjusting the voltage to the DRAM. In this case, a test using maximum and minimum temperatures, or a two-corner test, is done.

Power cycling tests

These stress the system by repeatedly turning it on and off (rebooting). Testing should include cold and warm boots. A cold boot occurs when a system has not been running and is at ambient temperature. A warm boot occurs after a system has been running for a period of time and the internal temperature is stabilized. During boot-up or power-up, unique events take place where errors may occur, including ramp-up of power supply voltages and initialization of the memory. An intermittent problem may only be seen by repeated boot-up attempts.

Self-refresh testing

DRAM cells leak charge and must be refreshed for proper operation. To save power, self-refresh is used when the memory is not being accessed. The memory controller provides the proper commands when entering and exiting self-refresh; otherwise, data could be lost. As power cycling, self-refresh cycling is useful. If an intermittent self-refresh enter or exit problem is present, repeated cycling can help detect it. Applications that do not use self-refresh should skip this test.

Using the right tools at the right time helps designers easily identify potential problems and increase the robustness of a design. Re-evaluating the role of margin testing and compatibility testing in the memory qualification and validation process can lead to an immediate reduction in engineering hours during memory qualifications, more effective and thorough identification of actual failures and faster memory qualifications. □