SPECIFICATION

MULTILAYER CHIP VARISTOR

TYPE : AVL 14K 02 200

July 3, 2001

AMOTECH CO., LTD. 17-2, JAMWON-DONG, SEOCHO-GU, SEOUL, KOREA TEL : 82-2-544-1383 FAX : 82-2-517-7183	DESIGNED	CHECKED	APPROVED

1. Electrical Specification

1-1 Test condition

Varistor voltage	In = 1 mA DC
Leakage current	Vdc = 5 V DC
Maximum clamping voltage	Ic = 1 A
Rated peak single pulse transient current	8 / 20 ㎲ waveform
Capacitance	f = 1KHz, Vrms = 0.5 V
Insulation resistance after reflow soldering	V = 3.6 V DC
Reflow soldering condition	Soldering paste : Tamura (Japan) RMA-20-21L Stencil : SUS, 150 ㎛ thickness Pad size : 0.5 (Width) x 0.6 (Length) 0.5 (Distance between pads) Soldering profile : 230 ℃, 5 sec.

1-2 Electrical specification

Maximum allowable continuous AC voltage at 50-60 Hz	11	V	
Maximum allowable continuous DC voltage	14	V	
Varistor voltage / nomial voltage / breakdown voltage	18	V	
Maximum clamping voltage	35	V	Maximum
Rated peak single pulse transient current	20	A	Maximum
Nonlinearity coefficient	> 15		
Leakage current at continuous DC voltage	< 20	㎂	
Response time	< 1	ns	
Varistor voltage temperature coefficient	< 0.05	%/℃	
Capacitance measured at 1KHz	120	pF	Maximum
Insulation resistance after reflow soldering on PCB	> 10	MΩ	
Operating ambient temperature	-55 to +125	℃	
Storage temperature	-55 to +150	℃	

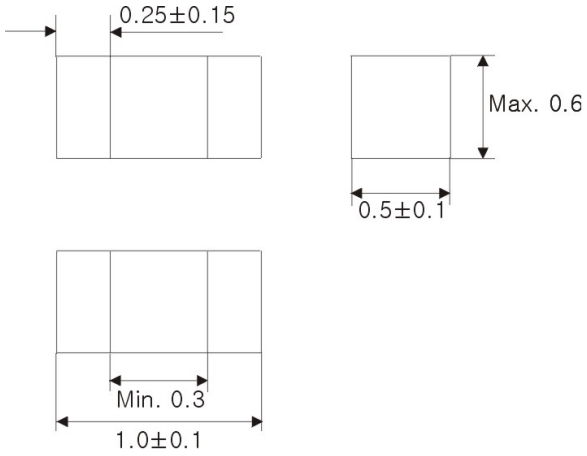
1-3 Reliability testing procedures

Reliability parameter	Test	Test methods and remarks	Test requirement
Pulse current capability	Imax 8/20 μs	IEC 1051-1, Test 4.5. 10 pulses in the same direction at 2 pulses per minute at maximum peak current	d|Vn|/Vn≤10% No visible damage To meet Vn tolerance
Environmental reliability	Thermal shock	IEC 68-2-14 Condition for 1 cycle Step 1 : Min. –40℃, 30±3 min. Step 2 : Max. +85℃, 30±3 min. Number of cycles: 50 times	d|Vn|/Vn≤5% No visible damage To meet Vn tolerance
	High temperature	IEC 68-2-3 Place the chip at 85±3℃ for 500±12hrs. Remove and place for 24±2hrs at room temp. condition, then measure	d|Vn|/Vn≤5% No visible damage To meet Vn tolerance
	Low temperature	IEC 68-2-1 Place the chip at -40±3℃ for 500±12hrs. Remove and place for 24±2hrs at room temp. condition, then measure	d|Vn|/Vn≤5% No visible damage To meet Vn tolerance
	Climatic sequence	IEC 1051-1, Test 4.17 a) Dry heat : 85℃, 16hrs b) Damp heat, cyclic, the first cycle : 55℃, 93%RH, 24hrs c) Cold : -40℃, 2hrs d) Damp heat cyclic, remaining 5 cycles : 55℃, 93%RH, 24hrs/cycle	d|Vn|/Vn≤10% No visible damage To meet Vn tolerance
	Heat resistance	IEC 68-2-3 Apply the rated voltage for 1000±48hrs at 85±3℃. Remove and place for 24±2hrs at room temp. condition, then measure	d|Vn|/Vn≤5% No visible damage To meet Vn tolerance
	Humidity resistance	IEC 68-2-30 Place the chip at 40±2℃ and 90 to 95% humidity for 500±24hrs. Remove and place for 24±2hrs at room temp. condition, then measure	d|Vn|/Vn≤10% No visible damage To meet Vn tolerance
Mechanical Reliability	Solderability	IEC 68-2-20 Solder bath method, 230±5℃, 3±0.5 sec.	At least 95% of terminal electrode is covered by new solder
	Resistance to soldering heat	IEC 68-2-20 Solder bath method, 260±5℃, 10 sec.	d|Vn|/Vn≤5% No visible damage To meet Vn tolerance
	Bending strength	IEC 68-2-21 Warp:2mm, Speed:0.5mm/sec, Duration: 10sec.The measurement shall be made with board in the bent position	d|Vn|/Vn≤10% No visible damage To meet Vn tolerance
	Adhesive strength	IEC 68-2-22 Applied force on SMD chip by fracture from PCB	Strength＞10 N (1 kg) No visible damage

2. Material Specification

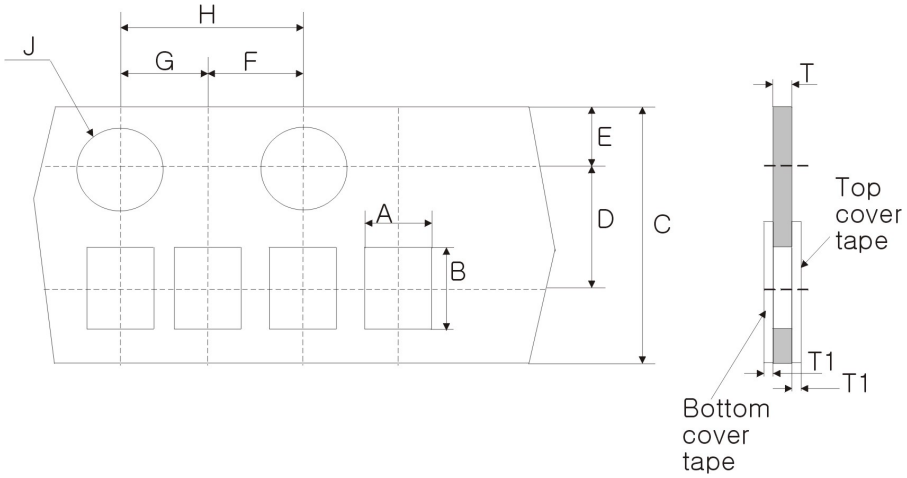
Body	ZnO based ceramics
Internal electrode	Silver – Palladium
External electrode	Silver – Platinum

3. Dimension Specification



Unit : mm

4. Package Specification



	A	B	C	D	E	F	G	H	J	T	T1
Spec.	0.62	1.12	8.00	3.50	1.75	2.00	2.00	4.00	1.50	0.60	0.1
Tolerance	±0.04	±0.04	±0.10	±0.05	±0.10	±0.05	±0.05	±0.10	+0.10 -0.00	±0.05	Max.

4-1 Material for package

4-1-1 Paper carrier tape

Laminated virgin pulp

4-1-2 Top tape

Polyester film

4-1-3 Bottom tape

Adhesive coated paper

4-1-4 Plastic reel

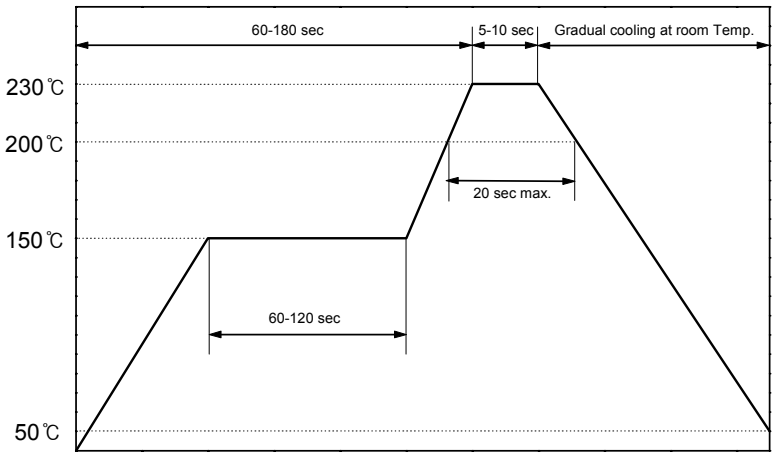
GPPS (General Purpose Poly Styrene) resin

4-1-5 Plastic bag

PE (Poly ethylene)

5. Soldering Recommendations

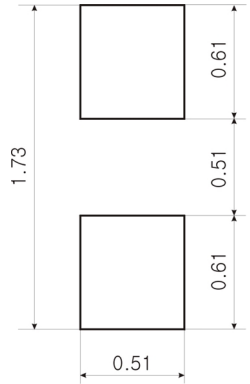
5-1 Soldering profile



5-2 Soldering guidelines

- Our chip varistors are designed for reflow soldering only. Do not use flow soldering
- Use Sn / Pb / Ag (62 / 36 / 2) or equivalent solder.
- Use non-activated flux (Cl content 0.2% max.)
- Follow the recommended soldering conditions to avoid varistor damage.

5-3 Solder pad layout



6. Storage condition

- Storage environment must be at an ambient temperature of 25~35 ℃ and an ambient humidity of 40~60 % RH
- Chip varistors can experience degradation of termination solderability when subjected to high temperature of humidity, or if exposed to sulfur or chlorine gases.
- Avoid mechanical shock (ex. Falling) to the chip varistor to prevent mechanical cracking inside of the ceramic dielectric due to its own weight.
- Use chips within 6 months.
  If 6 months of more have elapsed, check solderability before use.-

7. Description about package label

Type : AVL 14K 02 200

AVL : Series name

14 : Maximum continuous working voltage - Vdc

K : Varistor voltage tolerance – ±10%

02 : Chip size – 02 is 0402 (1.0 x 0.5 mm) size

200 : Maximum surge current – 200 means 20 x 10^0 A

Lot : F01033PD08

F : Powder type – F means formulation powder

01 : Production year – 2001

033 : Ceramic tape batch number

P : Production type – P means mass production

D : Production month – D means April

08 : Production date

Qunatity : 10,000 pcs

- Quantity of shipping chip varistor

Date : August 11, 2001

- Shipping date