




## SPECIFICATION

### MULTILAYER CHIP VARISTOR

TYPE : AVRC 5 S 05 Q 050 100R

January 29, 2004

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## Revision record

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## 1. ELECTRICAL SPECIFICATON

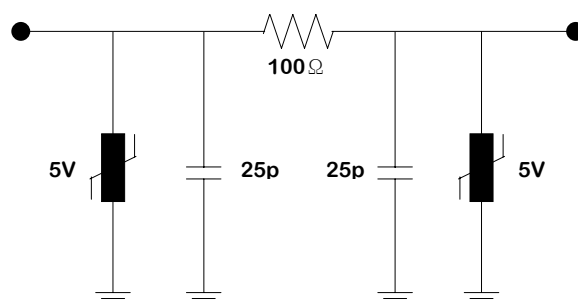
### 1-1 TEST CONDITION

Varistor voltage	$I_n = 1 \text{ mA DC}$
Leakage current	$V_{dc} = 5.5 \text{ V DC}$
Capacitance	$f = 1 \text{ MHz, } V_{rms} = 0.5 \text{ V}$
$R_{I/O}$	$I = 0.05 \text{ mA}$
Insulation resistance after reflow soldering	$V = 3.6 \text{ V DC}$
	Soldering paste : Tamura (Japan) RMA-20-21L
Reflow soldering condition	Stencil : SUS, $120 \mu\text{m}$ thickness
	Soldering profile : $220^\circ\text{C}$ , 5 sec.

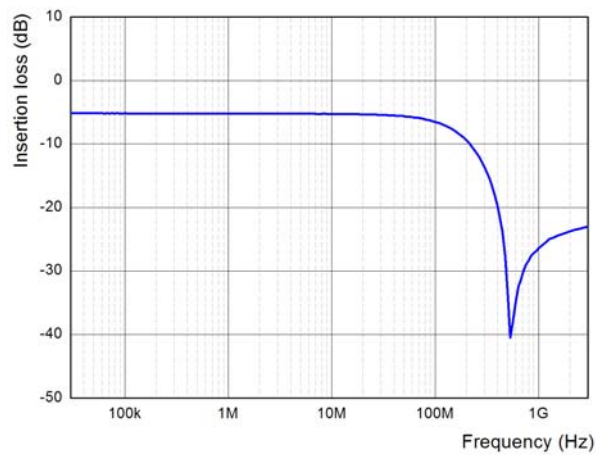
### 1-2 ELECTRICAL SPECIFICATION

Maximum allowable continuous DC voltage	5	V
Varistor voltage / nominal voltage / breakdown voltage	10~14	V
Nonlinearity coefficient	$> 10$	
Leakage current at continuous DC voltage	$< 20$	$\mu\text{A}$
Response time	$< 1$	ns
Series resistance between input and output	100	$\Omega$
Resistance tolerance	-30to +30	%
Capacitance measured at 1MHz	25	pF
Capacitance tolerance	-30to +30	%
Insulation resistance	$> 10$	$\text{M}\Omega$
Operating ambient temperature	-55 to +125	$^\circ\text{C}$
Storage temperature	-55 to +150	$^\circ\text{C}$

### 1-3 EQUIVALENT CIRCUIT



## 1-4 FREQUENCY CHARACTERISTICS

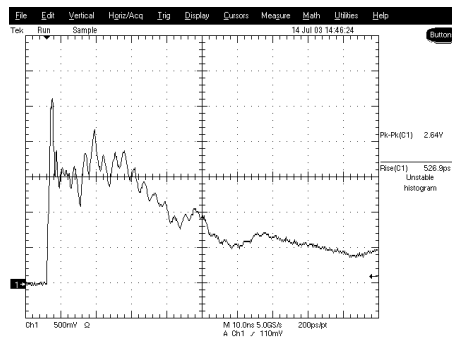


**FIG 1. FREQUENCY vs. INSERTION LOSS CURVE**

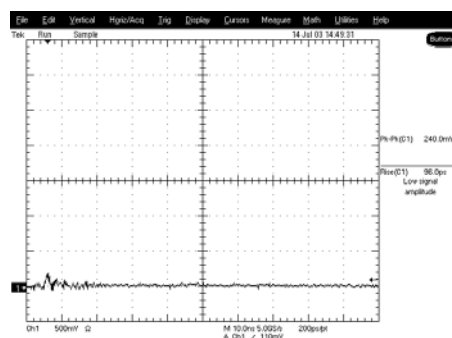
## 1-5 ESD PROTECTION EFFICIENCY

- Contact 8kV ESD strike

**FIG 2. ESD Curve INPUT (IEC61000-4-2 standard waveform)**



**FIG 3. ESD Curve OUTPUT**



## 1-6 Reliability testing procedures

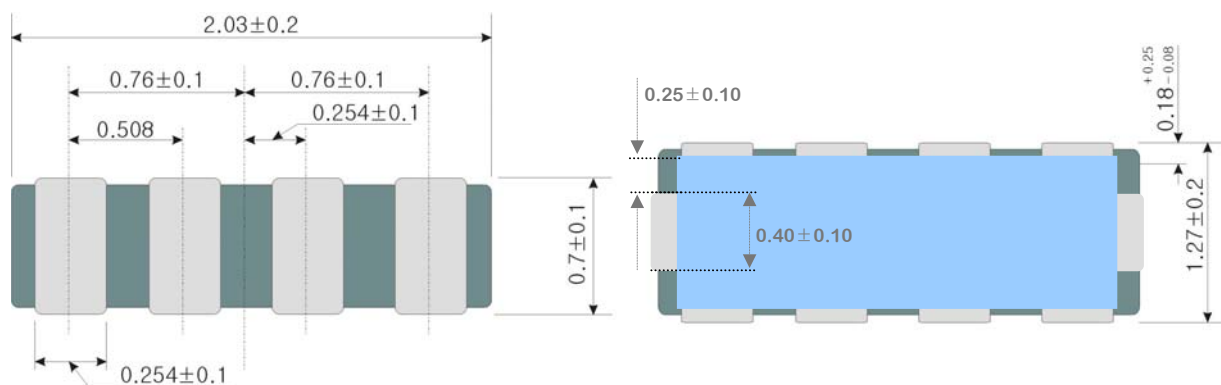
Reliability parameter	Test	Test methods and remarks	Test requirement
Pulse current capability	I <sub>max</sub> 8/20 $\mu$ s	<u>IEC 1051-1, Test 4.5.</u> 10 pulses in the same direction at 2 pulses per minute at maximum peak current	$d V_n /V_n \leq 10\%$ no visible damage
Electrostatic discharge capability	ESD C=150 pF, R=330 $\Omega$	<u>IEC 61000-4-2</u> Each 10 times in positive/negative direction in 10 sec at 8KV contact discharge (Level 4)	$d V_n /V_n \leq 10\%$ no visible damage
Environmental reliability	Thermal shock	<u>IEC 68-2-14</u> Condition for 1 cycle Step 1 : Min. $-40^{\circ}\text{C}$ , $30 \pm 3$ min. Step 2 : Max. $+125^{\circ}\text{C}$ , $30 \pm 3$ min. Number of cycles: 30 times	$d V_n /V_n \leq 5\%$ no visible damage
	Low temperature	<u>IEC 68-2-1</u> Place the chip at $-40 \pm 5^{\circ}\text{C}$ for $1000 \pm 12$ hrs. Remove and place for $24 \pm 2$ hrs at room temp. condition, then measure	$d V_n /V_n \leq 5\%$ no visible damage
	High temperature	<u>IEC 68-2-2</u> Place the chip at $125 \pm 5^{\circ}\text{C}$ for $1000 \pm 24$ hrs. Remove and place for $24 \pm 2$ hrs at room temp. condition, then measure	$d V_n /V_n \leq 5\%$ no visible damage
	Heat resistance	<u>IEC 68-2-3</u> Apply the rated voltage for $1000 \pm 48$ hrs at $85 \pm 3^{\circ}\text{C}$ . Remove and place for $24 \pm 2$ hrs at room temp. condition, then measure	$d V_n /V_n \leq 5\%$ no visible damage
	Humidity resistance	<u>IEC 68-2-30</u> Place the chip at $40 \pm 2^{\circ}\text{C}$ and 90 to 95% humidity for $1000 \pm 24$ hrs. Remove and place for $24 \pm 2$ hrs at room temp. condition, then measure	$d V_n /V_n \leq 10\%$ no visible damage
	Pressure cooker test	Place the chip at 2 atm, $120^{\circ}\text{C}$ , 85%RH for 60 hrs. Remove and place for $24 \pm 2$ hrs at room temp. condition, then measure	$d V_n /V_n \leq 10\%$ no visible damage
	Operating life	Apply the rated voltage for $1000 \pm 48$ hrs at $125 \pm 3^{\circ}\text{C}$ . Remove and place for $24 \pm 2$ hrs at room temp. condition, then measure	$d V_n /V_n \leq 10\%$ no visible damage

<b>Mechanical Reliability</b>	Solderability	<u>IEC 68-2-58</u> Solder bath method, $230 \pm 5^{\circ}\text{C}$ , 2s	At least 95% of terminal electrode is covered by new solder
	Resistance to soldering heat	<u>IEC 68-2-58</u> Solder bath method, $260 \pm 5^{\circ}\text{C}$ , $10 \pm 0.5\text{s}$ , $270 \pm 5^{\circ}\text{C}$ , $3 \pm 0.5\text{s}$	$d   V_n   / V_n \leq 5\%$ no visible damage
	Bending strength	<u>IEC 68-2-21</u> Warp:2mm, Speed:0.5mm/sec, Duration: 10sec. The measurement shall be made with board in the bent position	$d   V_n   / V_n \leq 5\%$ no visible damage
	Adhesive strength	<u>IEC 68-2-22</u> Applied force on SMD chip by fracture from PCB	Strength > 10 N no visible damage

## 2. Material Specification

Body	ZnO based ceramics
Internal electrode	Silver – Palladium
External electrode	Silver – Nickel – Tin
Thickness of Ni/Sn plating layer	Nickel > $1 \mu\text{m}$ , Tin > $2 \mu\text{m}$

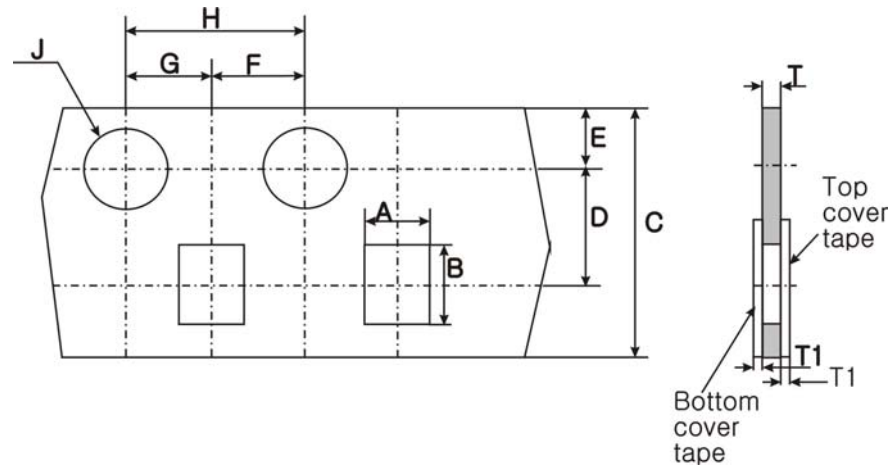
## 3. Dimension Specification



Unit : mm

## 4. Package Specification

### 4-1 Paper carrier tape package



	A	B	C	D	E	F	G	H	J	T	T1
Spec.	1.550	2.30	8.00	3.50	1.75	2.00	2.00	4.00	1.55	0.60	0.1
Tolerance	±0.05	±0.05	±0.10	±0.05	±0.05	±0.05	±0.05	±0.10	±0.03	±0.05	Max.

### 4-1 Material for package

#### 4-1-1 Paper carrier tape

Laminated virgin pulp

#### 4-1-2 Top tape

Polyester film

#### 4-1-3 Bottom tape

Adhesive coated paper

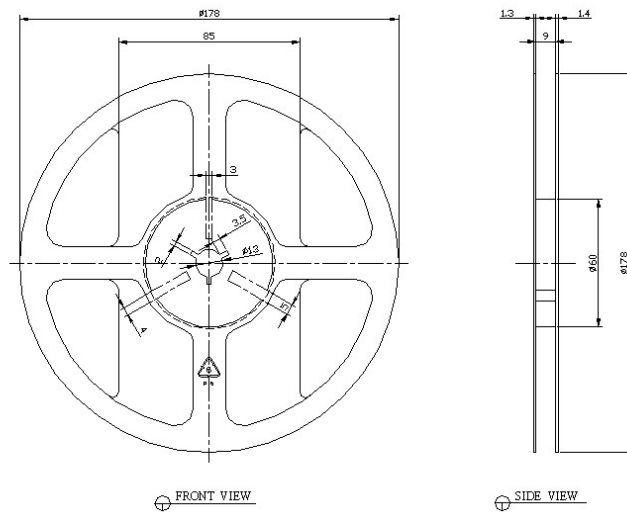
#### 4-1-4 Plastic reel

GPPS (General Purpose Poly Styrene) resin

#### 4-1-5 Plastic bag

PE (Poly ethylene)

## 4-2 Reel package



## 4-3 Box package

### 4-3-1 Small box

85 (W) x 85 (D) x 65 (T) (mm)

5 reel (4,000 ea/reel  $\times$  5 reel = 20,000 ea)

### 4-3-2 Medium box

195 (W) x 335 (D) x 205 (T) (mm)

5 small box (20,000 ea/small box  $\times$  5 small box = 100,000 ea)

### 4-3-3 Large box

370 (W) x 400 (D) x 275 (T) (mm)

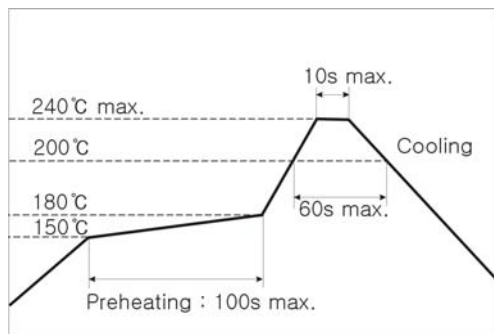
14 small box (20,000 ea/small box  $\times$  14 small box = 280,000 ea)



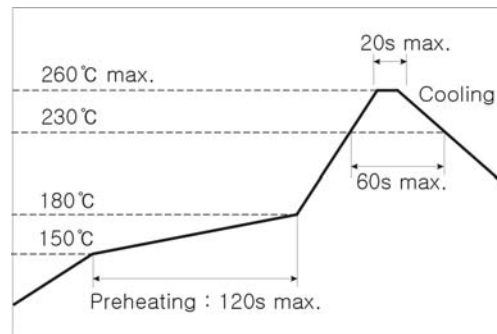
## 5. Soldering Recommendations

### 5-1 Soldering profile

#### 5-1-1 Sn/Pb solder paste



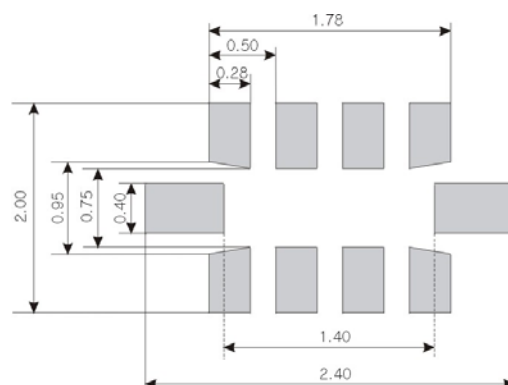
#### 5-1-2 Pb free solder paste



### 5-2 Soldering guidelines

- Our chip varistors are designed for reflow soldering only. Do not use flow soldering
- Use Sn / Pb / Ag ( 62 / 36 / 2 ) or equivalent solder.
- Use non-activated flux (Cl content 0.2% max.)
- Follow the recommended soldering conditions to avoid varistor damage.

### 5-3 Solder pad layout



## 6. Storage condition

- Storage environment must be at an ambient temperature of 25~35 °C and an ambient humidity of 40~60 % RH
- Chip varistors can experience degradation of termination solderability when subjected to high temperature of humidity, or if exposed to sulfur or chlorine gases.
- Avoid mechanical shock (ex. Falling) to the chip varistor to prevent mechanical cracking inside of the ceramic dielectric due to its own weight.
- Use chips within 6 months.  
If 6 months of more have elapsed, check solderability before use.

## 7. DESCRIPTION ABOUT PACKAGE LABEL



### **AVRC 5S 05 Q 050 100R**

AVRC : R-C Type EMI\_ESD filter

5 : Maximum continuous working voltage - Vdc

S : Varistor voltage tolerance – S is special order

05 : Chip size – 05 is 0508 (1.25 x 2.00 mm) size

Q : Configuration – Q means Quad array (4 element)

050 : Capacitance – 050 means 50 pF

R : Typical Resistance

### **Lot : S020AP04A05AA**

S : Tape casting machine indication – S means first machine

Machine name	1 <sup>st</sup> machine	2 <sup>nd</sup> machine	3 <sup>rd</sup> machine
Class	A	B	C

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020 : Ceramic tape batch number

A : Printer type – A means Tepiko printer/stacker

		Printing machine		
		1 <sup>st</sup> machine	2 <sup>nd</sup> machine	3 <sup>rd</sup> machine
Stacking machine	1 <sup>st</sup> machine	A	B	C
	2 <sup>nd</sup> machine	D	E	F
	3 <sup>rd</sup> machine	G	H	I

P : Production type – P means mass production

04 : Production year – 2004

A : Production month – A means January

Month	Jan.	Feb.	Mar.	Apr.	May.	Jun.	Jul.	Aug.	Sep.	Oct.	Nov.	Dec.
Class	A	B	C	D	E	F	G	H	I	J	K	L

05 : Production date

AA : Sequence of stacking – AA means first stacking

## **Qunatity : 4,000 pcs**

- Quantity of shipping chip varistor

## **Date : 2004/01/25**

- Shipping date : January 27, 2004

## 8. Manufacturer and Place

### 8-1. Manufacturer

Amotech Co., Ltd.

### 8-2. Manufacturing place

5B 1L, Namdong Industrial complex, 617 Namchondong, Namdonggu, Incheon, Korea

## 9. Comment

We notice your company when we change design, manufacturing condition and raw material.