Technical Note

Understanding the Value of Signal Integrity

Introduction

Historically, design engineers have used signal integrity (SI) testing as a key part of the design and development of new systems and for sustaining qualifications. Signal integrity, while extremely valuable in the engineering prototype phase, is not a panacea. In fact, its value diminishes as the product design progresses. After debug of early prototypes is complete, powerful tools that perform temperature and voltage margin testing should supplement or replace SI, especially for qualification of memory die shrinks and alternate sourcing.

Proper selection of memory design, test, and verification tools reduces engineering time and increases the probability of detecting potential problems. This technical note describes how these alternate tools can be used to the greatest advantage, from conception of a new product through end of life. It also provides a detailed description of SI, its uses, and limitations. Finally, it presents an overview of margin testing tools and the value they can add.

Tools for Memory Design, Testing, and Verification

Table 1 is a snapshot of five essential tools for memory design. Note that this is not a complete list of memory design tools, as this technical note focuses only on tools that can be used to validate the functionality and robustness of a design.

Table 2 shows at which point during the design and production phases each of these tools can be used most effectively. Compatibility testing, for example, does not occur during the design phase because no board is available to test. When used properly, these tools lead to reduced design time and more robust systems.

Table 1: Memory Design, Test, and Verification Tools

Tool	Examples
Electrical Simulations	SPICE or IBIS
Behavioral Simulations	Verilog or VHDL
Signal Integrity	Oscilloscope and probes; possibly mixed mode to allow for more accurate signal capture
Margin Testing	Guardband testing and 4-corner testing by variation of voltage and temperature
Compatibility Testing	Functional software testing or system reboot test

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How Does the Logic Analyzer (or Mixed-Mode Analysis) Fit In?

You may have noticed that logic analyzers are not included in Table 1. While it is rare to find a debug lab that does not include this tool as an integral part of its design and debug process, logic analyzers are not discussed here. Due to the cost and time involved, they are rarely the first tool used to detect a failure or problem in a system. Rather, they are used to debug a problem that is detected by compatibility or 4-corner testing, or by other means.

Table 2: Tools for Verifying Memory Functionality vs. Design Phase

Tool	Design	Alpha Proto	Beta Proto	Production	Post-Production
Simulation – Electrical	Essential	Very Valuable	Limited Value	Rarely Used	No Value
Simulation – Behavioral	Essential	Very Valuable	Limited Value	Rarely Used	No Value
Signal Integrity	Unavailable	Critical	Limited Value	Rarely Used	No Value
Margin Testing	Unavailable	Essential	Essential	Essential	Essential
Compatibility	Unavailable	Valuable	Essential	Essential	Essential

The Five Phases of Product Development

Phase 1 – Design

In this phase a concept or idea is implemented in hardware. Because no prototype is available, only simulation tools can be used. Therefore, designers rely exclusively on electrical and behavioral simulation tools.

Phase 2 – Alpha Prototype

In this phase the first prototype, or alpha prototype, is manufactured. It should be expected that the alpha prototype will undergo changes prior to production, including some or all of the following:

- Software changes (BIOS, embedded software, operating system, etc.)
- Motherboard changes:
  Impedance/termination
  Component vendor
  Trace length rerouted or shortened
- Functionality changes:
  ASIC, gate array, or FPGA
  Component or package type
  Repair incorrect functionality
- Airflow, power supply, chassis changes

The purpose of the alpha prototype phase is to find most or all of the problems in the system. Engineers must perform enough testing to ensure that the next prototype will be nearly production-ready, at least from a hardware perspective. Certain tools are more useful in accomplishing this than others.

Typically, the first tool employed in this phase is a boot-up and software check. A system boot-up or power-on can yield valuable information and, coupled with basic software checks, can provide data that will point to necessary changes within the system. A thorough software check may not be possible during this phase because basic hardware changes are still likely. Designers may, however, construct a limited number of alpha units for software debug.

SI is also an invaluable tool during this phase. SI incorporates the use of an oscilloscope or mixed-mode analysis to capture the analog signals of traces on the circuit board. These captures can be compared to simulation or device specifications to determine whether the device meets specifications and whether it has an adequate timing margin. If it falls short, this is the ideal development phase to make timing or signal improvements.

One tool that should not be used in this phase, however, is margin testing because the board design is still in a state of flux. Margin testing should only be used after the hardware is stable.

After running the appropriate tests, designers will have a list of changes that need to be implemented, including some that may need to be simulated electrically or behaviorally to ensure they have the desired effect.

Phase 3 – Beta Prototype

In the final stage of prototyping (beta prototype), the hardware is at or near production status and only minor tweaks are expected. A combination of testing is used to finalize the hardware and make the system production-ready. Software or compatibility testing must be thorough at this point. It can be run alone or in conjunction with margin testing. This combination should catch the memory failures that are likely to occur.

The types of software testing that are extremely useful for debugging memory devices are listed below and described in further detail in subsequent sections:

- Reboot or power-up testing
- Memory test patterns, such as checkerboard, inversions, etc.
- System power-down or standby modes that affect memory, such as those that activate self refresh

Margin testing should also be used extensively in the beta prototype phase. Varying temperature and voltage levels to their extremes is very valuable in identifying problems and marginalities.

SI, on the other hand, has limited value in this phase but can be used to understand functional fails and to validate changes made during the alpha prototyping phase. SI testing should not be used to verify signals or nets from the alpha prototype that were validated previously and have not changed.

If any additional modifications are made during the beta prototyping phase, electrical and/or behavioral simulation or SI may be necessary to validate them.

Phase 4 – Production

Ideally, changes to a system are rare when it is ready for production. Instead, the focus turns to performing sustaining qualifications. Systems may be in production for anywhere from six months to ten years or more, and they may use hundreds or thousands of components. For systems to remain in production, it is important that companies have a means of qualifying alternate sources or additional components.

Sustaining qualifications:

Performing a series of qualification tests on a component after a system is in production. These tests ensure that an adequate supply of components will be available for uninterrupted production.

In production, a system is stable and unchanging. The only requalifications needed are sustaining qualifications (i.e., when a component changes, a die shrink occurs, a second source is qualified, etc.). A sustaining qualification will ascertain if a modified component passes or fails in a system.

Motherboard traces and layouts, which were verified by SI in the design phase, rarely (if ever) change in the production phase. Therefore, SI (and simulation testing) is unnecessary. Furthermore, as we will discuss later, SI cannot catch failures that have historically caused system/memory-related issues. For systems that use memory, our experience has shown that SI is a poor test tool for the production phase because it does not catch all problems. The preferred tools and the keys for sustaining qualifications are compatibility and margin testing.

Phase 5 – Post-Production

Some systems, such as MP3 players or DVD recorders, require no testing or qualification after production ends. However, many other systems may require sustaining qualifications and support. Memory upgrades, for example, are common for notebooks, PCs, and other devices, and can be critical for years after production ends. As in Phase 4 above, margin testing and compatibility testing are the keys for sustaining these types of qualifications.

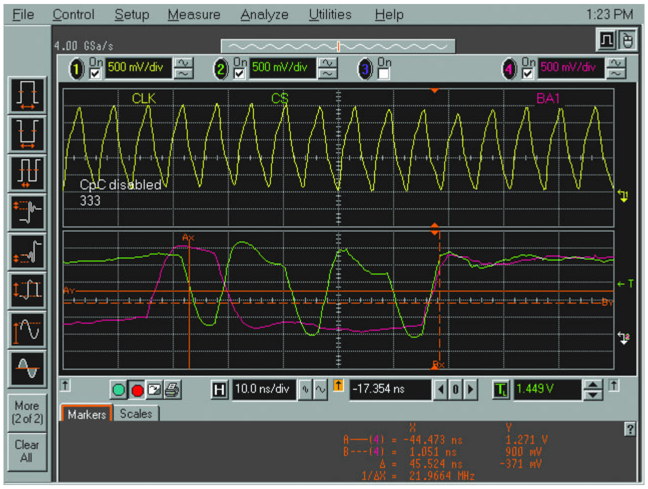
Signal Integrity (SI) Testing

Every electrical engineer is trained to use an oscilloscope. As a result, they are comfortable using one to look at a circuit design and evaluate the signals.

Figure 1 shows a diagram of a typical SI capture taken by an oscilloscope. In this particular case, the scope shot shows several signals from a single DDR SDRAM component:

- BA1 – bank address 1
- CS – chip select signal
- CK – differential system clock (noninverted clock)

Figure 1: Typical Signal Integrity Shot from an Oscilloscope



```
                 X                  Y
A——(4) = -44.473 ns         1.271 V
B---(4) =  1.051 ns          900 mV
     Δ =  45.524 ns         -371 mV
  1/ΔX =  21.9664 MHz
```

SI Testing

The process of taking oscilloscope photographs of system signals to evaluate voltage changes over time. These photographs or "captures" are evaluated visually for out-of-spec conditions, which is typically a time-consuming process that requires a high level of engineering expertise.

From an SI photo such as Figure 1 on page 4, a number of useful things can be observed, including:

- Ringing or overshoot/undershoot: JEDEC specifications for memory components restrict the amount of allowable overshoot and undershoot. SI during alpha prototyping can uncover violations of these specifications.
- Timing violations: Signal timing is easily observed from these scope shots. Examples of timing verifications that can be performed include:

  Slew rate – identification of weakly driven or strongly driven signals

  Setup and hold time

  Clock duty cycle

  Crossing of differential signals (such as CK and CK#)

  Relationship of control and data signals relative to clock; do they meet spec?

  Bus contention; do two signals drive the bus at the same time and cause conflict?

It is important to note that if any of these conditions occur, they will likely cause a system failure that compatibility and margin testing can easily reveal. After these tools have identified the problem, other tools (logic analyzer, SI, etc.) can be used to determine its cause.

DRAM Migration to FBGA Packages

If TSOP packages are cheaper to manufacture than FBGA and engineers can easily probe signals with an oscilloscope, why is the DRAM industry migrating to FBGAs?

Reduced parasitics:

FBGA packages have reduced parasitics over TSOP (capacitance, inductance, and resistance). As system speeds continue to increase, decreasing parasitic values is critical to increasing clock frequencies.

JEDEC mandate for DDR2:

FGBA is now the required package for all DRAM manufacturers.

Size matters:

Many applications have limited space, and FBGA packages reduce both the board footprint and total volume used by the DRAM.

Future upgradeability:

In order to gain headroom for even higher speeds, FBGA packages have the option for flip-chip bonding, which reduces parasitics even further.

Looking at Signals with FBGA Packages

The FBGA package does a great job of improving parasitics, but signal integrity analysis or a logic analyzer cannot probe signals at the balls of the package. New technologies such as DDR2 exclusively use FBGA packages because they are the JEDEC standard for this technology. Users who want to investigate the SI of a DRAM at the FBGA package have a few tools to assist them:

Probing at the connector or other locations:

It may be possible to probe at the connector or a trace on the board or via. However, the signal measured is not representative of the signal at the DRAM. If you see a non-monotonic signal, or noise, is it different at the DRAM. Micron's experience has shown that unless you probe the signal directly at the DRAM, you cannot get a true representation of signal quality.

Using special tools such as Micron Technology snoop modules:

Nexus Technology offers a special software package combined with a Micron Snoop DIMM to enable logic analyzer use with DDR2 (see Figure 3 on page 7). Careful attention has been paid to the design of this module to enable the logic analyzer to probe signals without affecting the operation of the module. For more details on this approach, contact Nexus Technology.

Limitations of SI Analysis

SI analysis has become more difficult and time consuming, and in cases such as FBGA packages, almost impossible. Some of the challenges include:

FBGA Packages

It is virtually impossible to place a scope probe on signals under an FBGA package (Figure 2). Some solutions exist for DDR2, such as Micron® Snoop™ modules, that enable probing of signals (Figure 3). These solutions can provide valuable information during debug or product design, but can also add cost to the development.

Figure 2: Why Scope Probing is Impossible with FBGA Packages

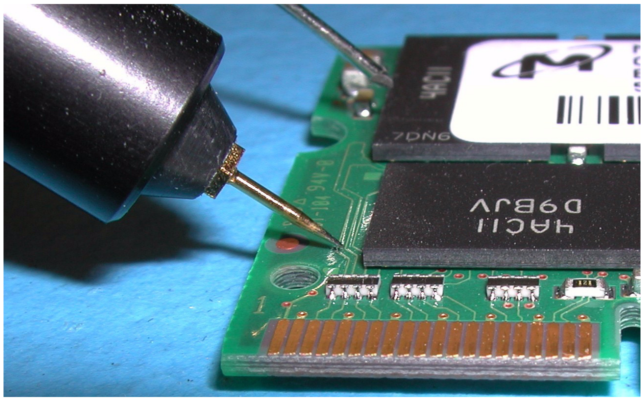
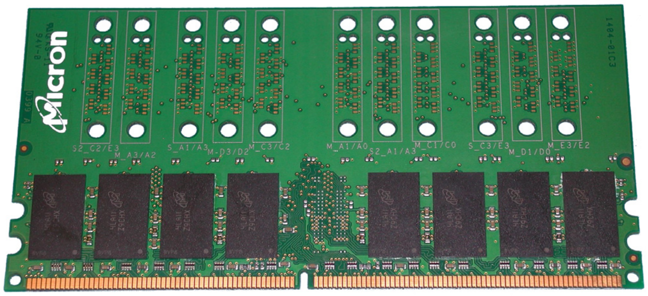


Figure 3: Micron Snoop™ DIMM Used with Nexus Technology Software and Textronic Logic Analyzers



MCM Packages

Some designs use multichip modules or MCMs to combine a variety of chips together in a single package. These packages are either covered with a mold compound or sealed hermetically, so the internal signals are unavailable to be probed.

Interference with Signal Quality

Using a probe to measure the SI of a circuit will change the signal being measured. Problems can be introduced or exacerbated by the addition of capacitance, or they may disappear. Although active or FET probes are available, this condition is likely to become more common as frequency scales, especially in systems that have a point-to-point architecture.

Inability to Detect Many Memory Issues

Although essential for system bring-up and validation, SI is a poor tool for memory qualification or sustaining qualifications.

Limitations of SI Testing

SI testing has its limits. Micron has taken literally hundreds of thousands of SI scope captures during multiple internal qualifications of memory, with the following results:

- SI used at an early stage of development is instrumental in catching fails.
  Glaring errors or issues are resolved.
- SI should be used to verify that board changes improve signals or that they continue to look good.
- SI has little value after the board design is stable.

Micron's internal test flow has migrated away from SI testing. Our extensive experience with self-qualification, qualification of new die revisions or engineering experiments, and debug of customer issues has resulted in the following internal procedure:

- Compatibility and margin testing are used to validate or test a system with memory.
- After compatibility or margin testing detects a fail, various diagnostic tools can be used to isolate the failure:

  If software can determine the fail type in a system (address, row, single cell, etc.), a memory chip or module is isolated and tested. We then attempt to duplicate the failing condition in a memory test fixture.

  If the software cannot provide details of the failure, the memory can be removed from the system. Component or module testing is then performed to find the failure.

  A logic analyzer can be used to determine the failing issue/pattern/out-of-spec condition.

Although a scope can be used, experience has shown that other tools are more effective in quickly testing, validating, and debugging systems. We believe that these alternative tools enable engineers to quickly come to root cause analysis and correction. In the process of performing self-qualifications for customers on systems that are near production level or in production, Micron has generated a database of about 200,000 individual scope captures. Guardband and compatibility testing are also part of the process.

Micron's self-qualifications produced the following results:

- Compatibility testing and margin testing regularly exposed problems or issues that could occur in a system. They were proven to be reliable tests for robustness and for discovering problems.
- SI did not find a single issue that was not identified by memory or system-level diagnostics. In other words, SI found the same failures as the other tests, thus duplicating the capabilities of margin testing and software testing.
- SI is time consuming. Probing 64-bit or 72-bit data buses and taking scope shots requires a great deal of time.
- SI uses costly equipment. To gather accurate scope shots, high-cost oscilloscopes and probes are needed.
- SI takes up valuable engineering resources. A high level of engineering analysis is needed to evaluate scope shots.
- SI does *not* find all errors. Compatibility and margin testing find errors that are not detectable by SI.

As an example, Figure 4 shows two scope shots, one system that passes and one that fails, and it is impossible to determine which system is which.

Alternatives to SI Testing

Alternatives to SI testing can be used for development of systems and for memory qualification and testing. This section provides a brief description of these tools and how to use them.

Software Tools or Compatibility Testing

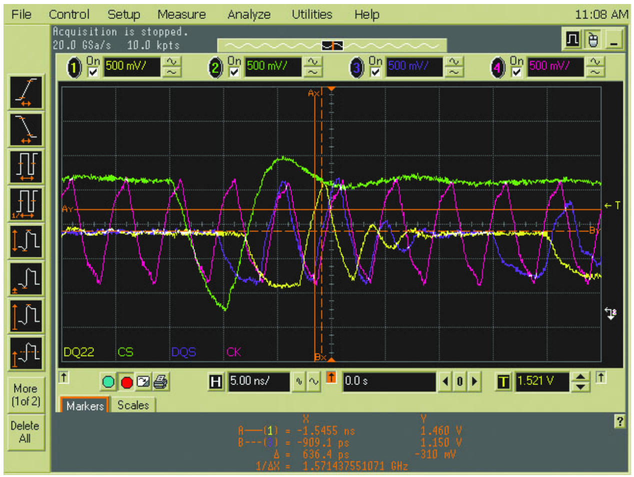
Computer systems are perfect for software testing. Because computers can use off-the-shelf software, a variety of products are available. While Micron does not endorse any off-the-shelf product, we have provided a partial list below as a reference. When considering software tools, companies should look for those that support dynamic upgrading and choose a program that will incorporate new diagnostics as needed to catch previously unknown failure mechanisms.

- PC Doctor
- Winstress
- Quicktech
- RST Pro
- AMI Diag
- PC Certify
- Tuff Test

Unlike PCs, other products are more difficult to test, such as consumer, embedded, and networking products. Designers for these types of applications develop home-grown tools or use none at all. Making home-grown tools more robust can provide greater benefit than SI testing.

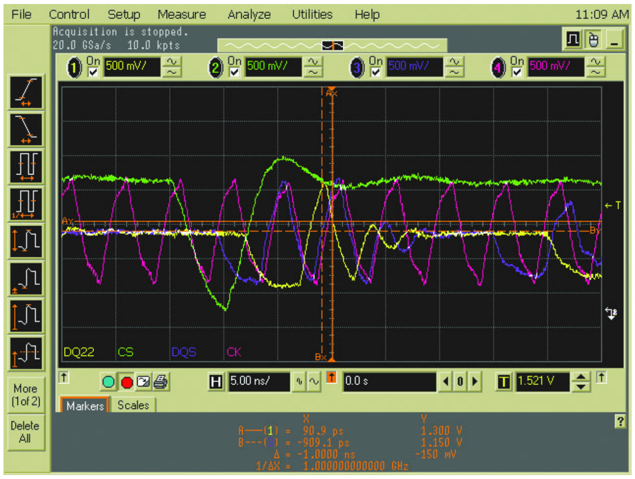
Note that sometimes a memory-specific test may be impossible in a system (such as MPEG decoding or packet transfers for networking). In these cases, the other tools described in this section should be used.

Figure 4: Examples of SI Scope Shots – One Failing, One Passing



```
Acquisition is stopped.
20.0 GSa/s   10.0 kpts
```

```
                    X                       Y
A——(1) = -1.5455 ns              1.460 V
B---(3) = -909.1 ps              1.150 V
      Δ =  636.4 ps             -310 mV
  1/ΔX =  1.571437551071 GHz
```



```
Acquisition is stopped.
20.0 GSa/s   10.0 kpts
```

```
                  X                    Y
A——(1) =    90.9 ps              1.300 V
B---(3) =  -909.1 ps             1.150 V
      Δ =  -1.0000 ns            -150 mV
   1/ΔX =   1.000000000000 GHz
```

Margin Testing

Two types of tests have been extremely valuable in identifying marginalities and system issues: voltage and temperature stress tests. Systems are stressed by applying higher voltage and temperature. Varying temperature and voltage exposes the DRAM and DRAM controller to a variety of conditions that are likely to reveal potential system issues.

Figure 5 and Figure 6 on page 11 show examples of how device timing and device power vary over temperature. Margin testing allows variation of these parameters in order to test or stress a system over rated parameters.

Figure 5: Example of Variation of Device Timing over Voltage and Temperature

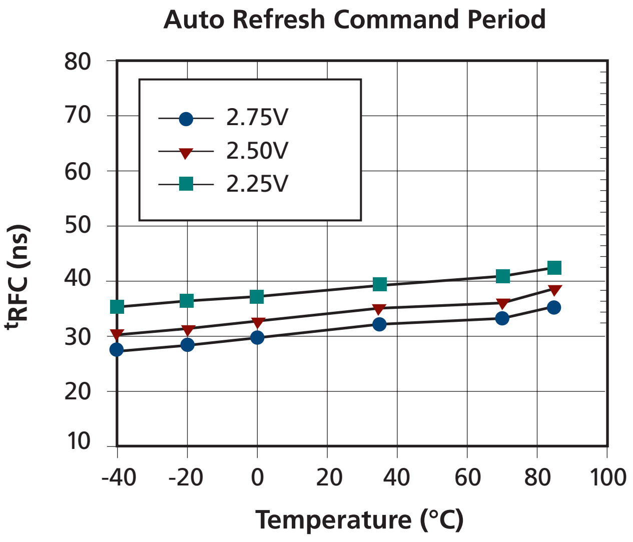
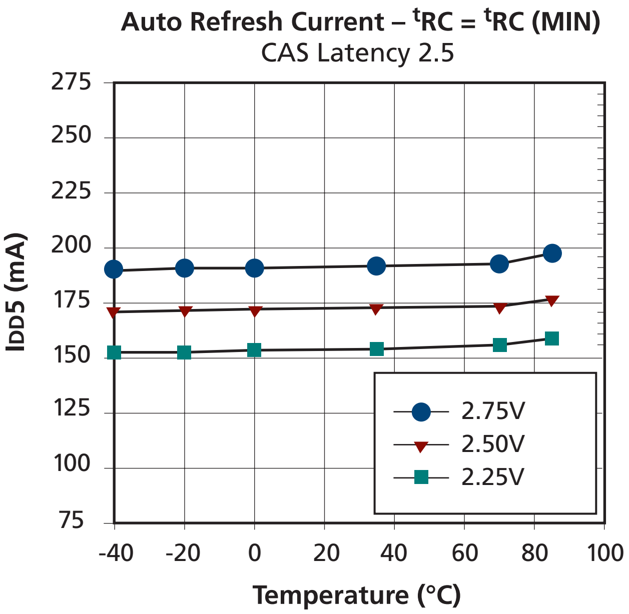


Figure 6: Example of Variation of Device Power over Voltage and Temperature



An example of this is a 4-corner test. In a 4-corner test, a system that has specified MIN and MAX voltages of 3.0V and 3.6V, and MIN and MAX temperatures of 0°C and 70°C undergoes four individual tests, as follows:

- Corner 1
  MAX voltage, MAX temperature: 3.6V, 70°C
- Corner 2
  MAX voltage, MIN temperature: 3.6V, 0°C
- Corner 3
  MIN voltage, MAX temperature: 3.0V, 70°C
- Corner 4
  MIN voltage, MIN temperature: 3.0V, 0°C

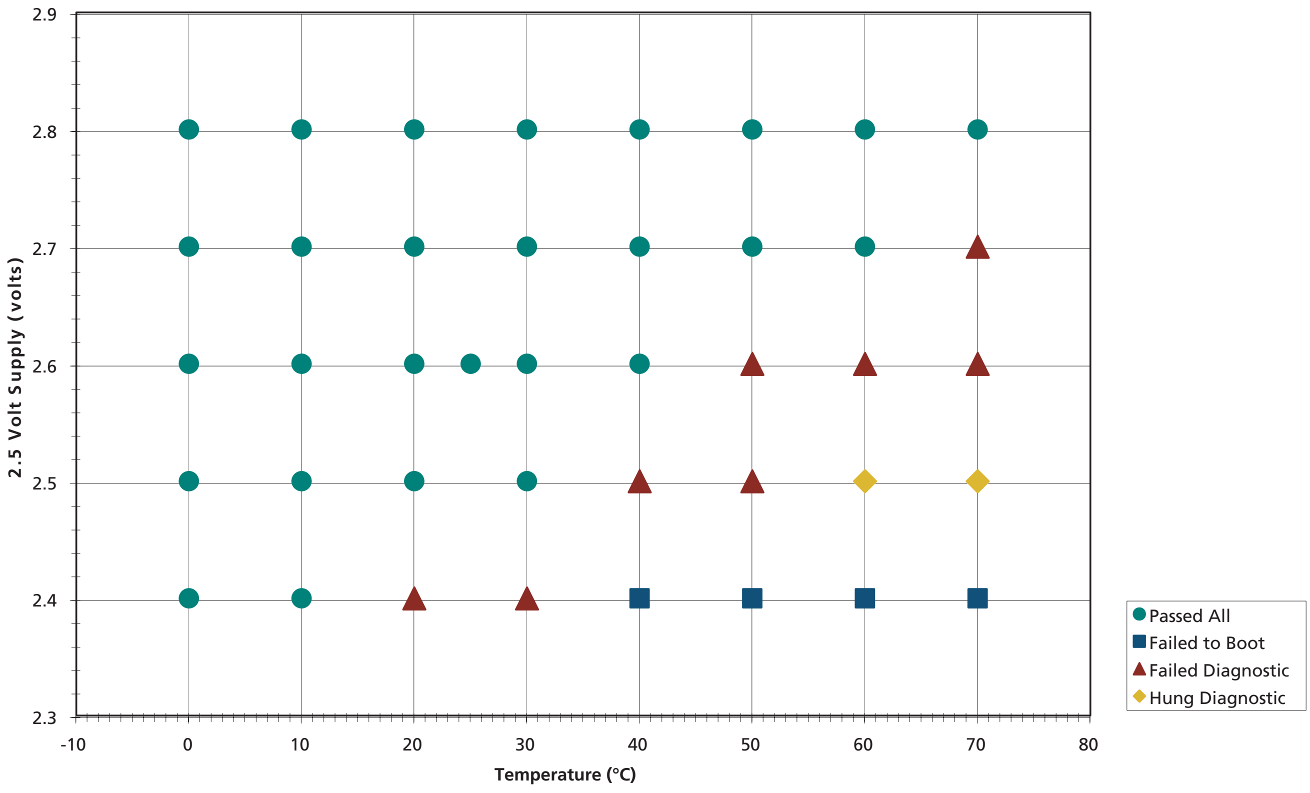
The types of testing done at these corners can vary, but a typical procedure is to let the system stabilize (both temperature and voltage) inside a temperature chamber and then choose a suite of tests to run at that corner. If any failures occur, they should be investigated.

A variation of this type of testing would be a 2-corner test. In some systems, the voltage to the memory is controlled by a voltage regulator, which means there is no way of adjusting the voltage to the DRAM. In this case, a test using MAX and MIN temperatures, or a 2-corner test, is used. Alternately, the voltage to the voltage regulator could be varied to the MIN/MAX levels (a 4-corner test).

Another example of a margin test is a multicorner test, illustrated in Figure 7 on page 12, which relies on a multitude of voltage and temperature test points. This type of testing is more expensive and time-consuming than other methods.

In the alternative, the 4-corner test has proven to be one of the most effective ways of testing memory. It is also reasonable in terms of time to test and resources required.

Figure 7: A Multicorner Guardband or Margin Test



Power Cycling Tests

Another useful tool is stressing the system by repeatedly turning it on and off (booting the system). This should include both cold and warm boots. A cold boot occurs when a system has not been running and is at ambient or room temperature. A warm boot occurs after a system has been running for a period of time and the internal temperature is stabilized.

During boot-up or power-up, a number of unique events take place where errors can occur:

Ramp-up of power supply voltages:

If there is an intermittent voltage ramp-up problem, it might only be detected by repeated cycling.

Initialization of the memory:

In order to meet JEDEC and industry standards, the memory controller must follow a strict initialization sequence. If there is an intermittent error or problem with the initialization sequence, it might only be detected by a series of repeated attempts.

Self Refresh Testing

DRAM cells leak charge and must be refreshed often to ensure proper operation. One of the key means of saving power in a system is to use self refresh when the memory is not used for long periods of time. It is critical that the memory controller provide the proper commands when entering and exiting self refresh; otherwise, data could be lost.

Similar to power-up cycling, self refresh cycling is a useful compatibility test. If an intermittent self refresh enter or exit problem is present, repeated cycling can help detect it.

Note: Applications that do not use self refresh should skip this test completely.

Conclusion: Rewards for Your Company

A re-evaluation of the memory qualification and validation procedures used by your company could provide many rewards.

- An immediate reduction in engineering hours during memory qualifications, especially sustaining qualifications, is achieved.
- Use of compatibility or margin testing results in more effective and thorough identification of actual fails than SI testing.
- Replacing SI with compatibility or margin testing results in faster memory qualifications, especially sustaining qualifications.

Each company has its own methodology for design development and qualification. We encourage each company to find the method that works best for it. Our experience has shown that margin testing and compatibility testing should strongly be considered as tools for the development process.

The Myths of SI

Myths and misconceptions exist about how to use SI testing. Micron has taken ~200,000 SI scope captures and based on that experience, we offer the following responses to some common myths in the industry.

Myth #1

Failures exist that no diagnostics will catch; therefore, SI testing is needed to identify them.

Response to Myth #1:

Our experience has shown that some customer test diagnostics may not be thorough enough to catch failures. Rather than spending many engineering hours on SI testing, our recommendation is to develop a better diagnostic suite or find a commercially available diagnostic program, and add new data patterns as needed.

Myth #2

SI testing provides data on the trends of signal quality, and this information can be used to try to predict failures so as to avoid them in the future.

Response to Myth #2:

A system is designed initially so that signals meet specifications, including rise time, fall time, setup, non-monotonic signals, etc. Experience has shown that SI does not significantly change over time. Continued SI testing does not catch additional fails, nor does it predict the likelihood of failures after a circuit board design has stabilized. Margin and software testing are much better predictors of failures.

Myth #3

Temperature/voltage margin tests (4-corner tests) will not catch obscure failures.

Response to Myth #3:

On the contrary, the stresses of voltage and temperature actually aggravate marginal or obscure failures and are therefore the most effective tools for catching system failures.

Myth #4

Most potential problems can be detected by SI.

Response to Myth #4:

Our experience has shown that most failures are attributed to timing conditions internal or external to the DRAM. SI cannot predict these types of timing failures. Once a failure has been verified by compatibility or margin testing, a logic analyzer can be useful in isolating these types of timing violations.

Myth #5

Variations between memory component vendors and PCB vendors can impact SI.

Response to Myth #5:

PCB differences are minimal in most applications. This is because vendors use common gerbers or board layouts in most cases. Our experience is that any impedance or problem due to parasitics has not been detected through SI, but by other tests.

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