Signal Integrity of High-Speed Printed Circuit Board
高速印刷電路信號完整性設計

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Abstract

Experimental results of interconnect parameters on an 14 layer test-board corroborate those measured with a precision impedance analyzer. In the paper a SPICE model is employed to examine the impedance of a typical signal bus on a multilayer PCB. The technique is validated by good agreement between manufacturer's specifications and complex permittivity calculated from measurements near resonant frequencies for a printed circuit board (PCB). High density interconnect printed circuit board technology enables significant board size and layer count reduction. Thinner inner layer dielectric materials, reduced line widths, and closer spaced components inherent in high density board technology require a change in electrical design methodology. Most notably, the thinner dielectric thickness significantly impacts the electrical performance of the circuit board with respect to cross talk, board capacitance, via inductance, and controlled impedance. Distributed capacitance will tend to increase because of the thinner dielectric layer and crosstalk between signal traces run on adjacent layers may also increase. Using either FR-4 type epoxy or higher performance materials conventional controlled impedance structures such as a strip-line, micro-strip. The frequency-dependent characteristic impedance of transmission lines using Time Domain Reflector (TDR) measurements with an open short and load calibration.

INTRODUCTION

Transmission line structures seen on a typical PCB consist of conductive traces buried in or attached to a dielectric or insulating material with one or more reference planes. The metal in a typical PCB is usually copper and the dielectric is FR4, which is a type of fibreglass. The two most common types of transmission lines used in digital designs are micro-strips and strip-lines. A micro-strip is typically routed on an outside layer of the PCB and has only one reference plane. There are two types of micro-strips, buried and no buried. A buried (sometimes called embedded) micro-strip is simply a transmission line that is embedded into the dielectric but still has only one reference plane. A strip-line is routed on an inside layer and has two reference planes. Figure1 represents a PCB with traces routed between the various components on both internal (strip-line) and external (micro-strip) layers. The accompanying cross section is taken at the given mark so that the position of transmission lines relative to the ground/power planes can be seen. In this paper, transmission lines are represented in the form of a cross section.

This is very useful for calculating and visualizing the various transmission line parameters described later. Multiple-layer PCBs such as the one depicted in Fig1 can provide a variety of strip-line and micro-strip structures. Control of the conductor and dielectric layers (which is referred to as the stack-up) is required to make the electrical characteristics of the transmission line predictable. In high speed systems, control of the electrical characteristics of the transmission lines is crucial.

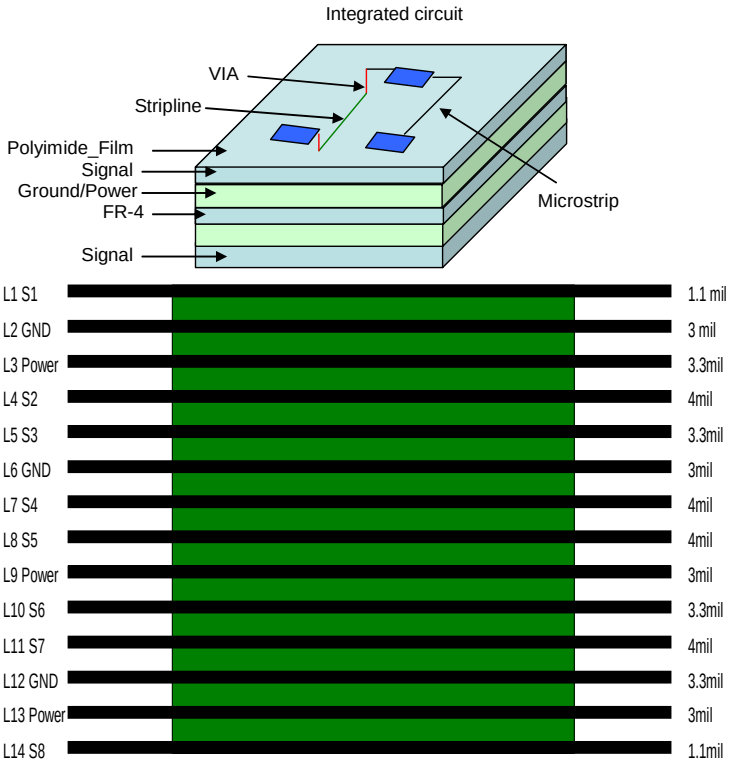
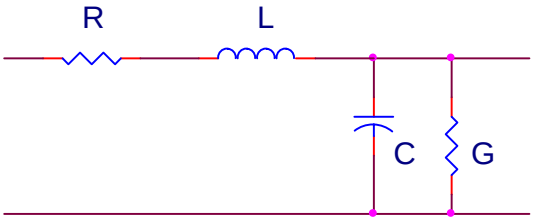


Fig.1. Example transmission lines in a typical design built on a PCB.

Signal Reflection Noise and Termination Schemes with SPICE

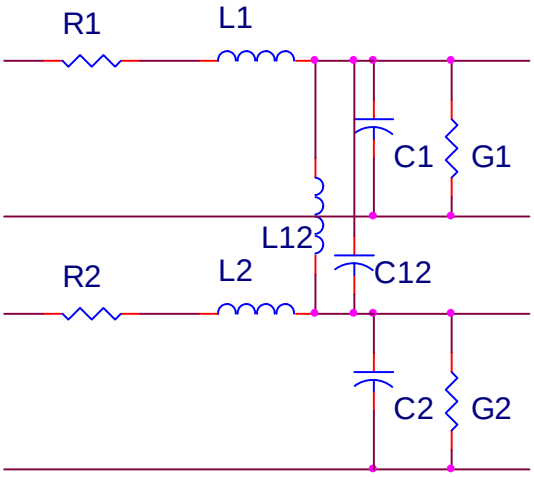
For maximum accuracy, it is necessary to use one of the many commercially available two dimensional electromagnetic field solvers to calculate the impedance of the PCB traces for design purposes. The solvers will typically provide the impedance, propagation velocity, and L and C elements per unit length. This is adequate since R and G

usually have a minimal effect on the impedance. In the absence of a field solver, the formulas presented in Fig2 equivalent circuit model.



(a)

$$Zo\_a = \sqrt{\frac{R + jwL}{G + jwC}}$$



(b)

$$Zo\_b = \sqrt{\frac{L11 - L12}{C11 + C12}}$$

Fig.2. (a)Equivalent circuit model of single lines (b) Equivalent circuit model for two coupled lines.

Will provide good approximations to the impedance values of typical transmission lines as a function of the trace geometry and the dielectric constant(εr). We can know the micro-strip, strip-line, differential micro-strip, differential centerede strip-line in the signal pattern of corresponding. Micro-strip corresponding PCB is the trace which is under FR-4.W means width, T means the depth of print pattern, and H means the depth of trace to GND. Strip-line is in the middle of the trace and between GND and power plane. According to fig.3(c), the differential micro-strip trace is often used in the high speed transmission line. S means edge-to-edge trace separation, the differential centered strip-line of fig. 3(d) is seldom discussed in the paper because it's impedance is difficult to calculate, the print pattern has more inaccuracy of signal and the exist of the noise which in jitter and is in Differential eye diagram.

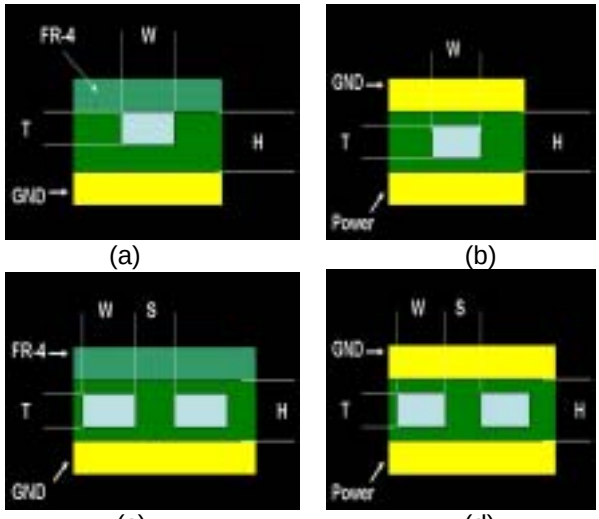


Fig.3. (a) Embedded micro-strip (b) Centered strip-line (c) differential micro-strip (d) differential centered strip-line.

$$Z0 = \frac{87}{\sqrt{\varepsilon r + 1.41}} \ln\left(\frac{5.98H}{0.8W + T}\right) - (1)$$

$$Z0 = \frac{60}{\sqrt{\varepsilon r}} \ln\left[\frac{4H}{0.6\pi(0.8W + T)}\right] - (2)$$

$$Z0\_diff = \frac{30\pi}{\sqrt{\left(\frac{\varepsilon r + 1}{2}\right)}} \frac{K2}{K1} - (3)$$

$$K1 = \tanh\left(\frac{\pi}{4}\frac{W}{H}\right) \tanh\left[\frac{\pi}{4}\left(\frac{W + S}{H}\right)\right]$$

$$K2^{2} = 1 - K1^{2}$$

$$Z0\_diff = 2Zo\left(1 - 0.78\left(e^{-2.9\frac{S}{h}}\right)\right) - (4)$$

$$Z0 = \frac{87 + \left(1 - \frac{W - 4.5}{0.5} * 0.08\right) * \varepsilon 2 * \left(\frac{W}{H}\right)}{\sqrt{\varepsilon r + 1.41}} \ln\left(\frac{5.98H}{0.8W + T}\right) - (5)$$

$$Z0 = \frac{87 + \left(1 - \frac{W - 4.5}{0.5} * 0.08\right) * \varepsilon 2 * \left(\frac{W}{H}\right)}{\sqrt{\varepsilon r + 1.41}} \ln\left(\frac{4H}{0.6\pi(0.8W + T)}\right) - (6)$$

$$Z0\_diff = 2Zo\left(1 - 0.48\left(e^{-0.96\frac{S}{h}}\right)\right) - (7)$$

$$Z0\_diff = 2Zo\left(1 - 0.37\left(e^{-2.9\frac{S}{h}}\right)\right) - (8)$$

In the original calculating the cross sectional geometry of the PCB is exist the inaccuracy impedance matching. In the original equation (1).(2) they calculate each impedance value of micro-strip, strip-line [1].The original equation (3). Is odd-mode effective constants for coupled micro-strip lines [6].The original equation (4) is the manner of calculating odd-mode differential centered strip-line [5]. This paper offered new manner of calculating and comparison which called equation (5).(6).(7).(8) and also make the 14 layer of PCB which compared by the measure number of TDR. We can see the comparison of single-end impedance on the table1. and differential impedance on the table2.It's obviously can see the stack-up of 14 layer of PCB. This paper discussed the different impedance of the width of trace.

Table1:Single-ended Impedance Measurements.

Layout	TDR			Original	New
	Min	Mid	Max		
4 mil L1	87	90	93	78	89
4 mil L4	46	50	54	39	48
4 mil L7	46	50	54	39	48
4 mil L8	46	50	54	39	48
4 mil L11	46	50	54	39	48
4 mil L14	87	90	93	78	89

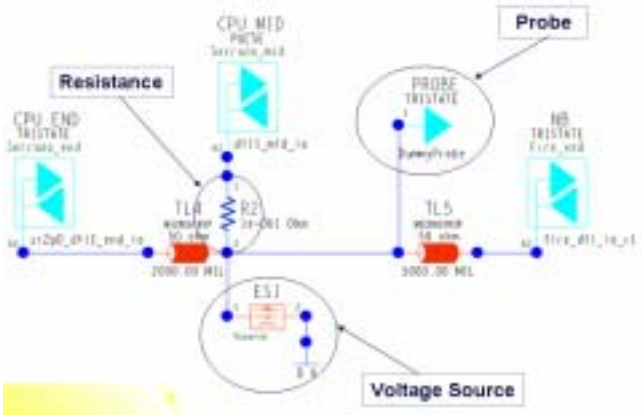
Table2:Differential Impedance Measurements.

Layout	TDR			Original	New
	Min	Mid	Max		
4/6/6_L1	117	122	128	98	120
4/6/4_ L4	96	100	104	86	99
4/6/4_L7	96	100	104	86	99
4/4/4_L4	87	90	93	78	89
4/4/4_L7	87	90	93	78	89
4/4/4_L8	87	90	93	78	89
4/4/4_L11	87	90	93	78	89

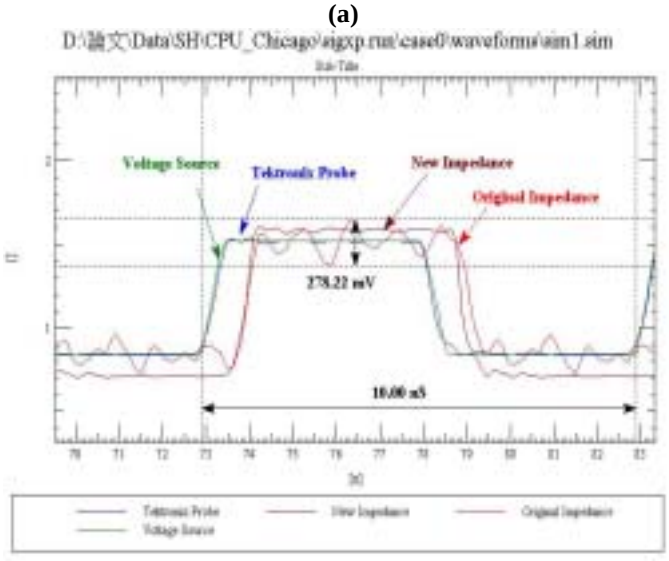
This paper imitate the value of original single-ended and the value of new single-ended by the simulation fool of candence-PSD15.2 to get the difference of signal. There is a connection pattern of driver, Tektronix Probe and Receivers in topology in Fig4.(a).in Fig4(b),it shows driver launched the signal about 1.5V 100MHZ to Receivers. There is a noise wave form 278.22mv in original impedance signal but the noise wave form in the new impedance signal has became smoothly.

This is because the problem of impedance matching is about the original impedance. The same situation is also happened in differential signal.Fig4(c) is a differential topology. Fig4(d) is the differential eye diagram. From this analysis , (see Fig4(d)).

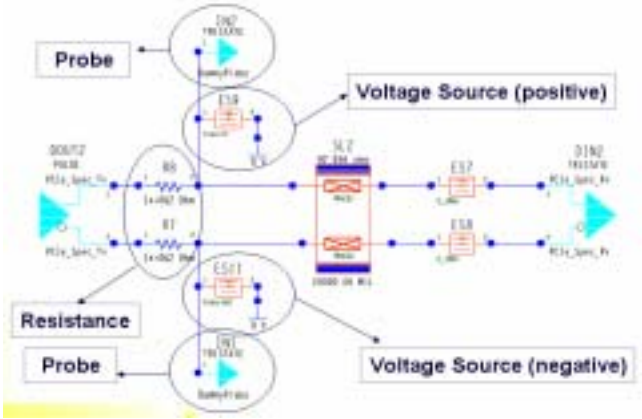
The signal inaccuracy between original model and new one which is 371.64mv is seen by the signal 2.5GHz.The more high speed signal the more important of it's impedance matching. It is hardly to expand to the limit in the eye diagram of original-impedance. Meanwhile, impedance matching already caused the obstruction of signal and can not work out fluently.



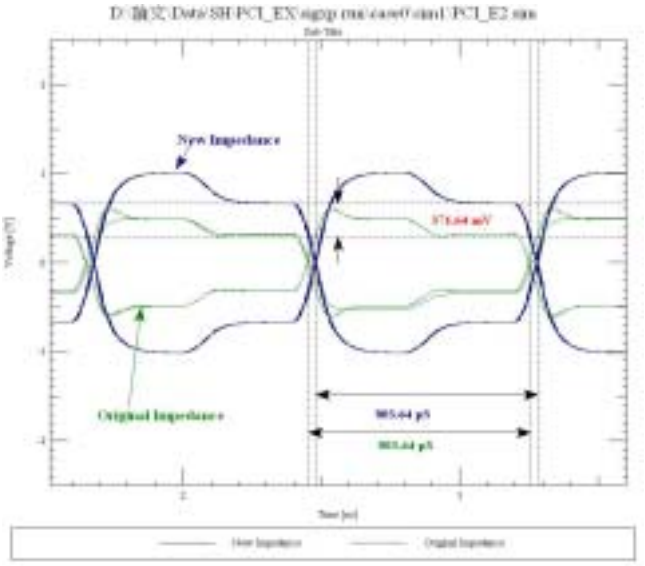
(a)



(b)



(c)

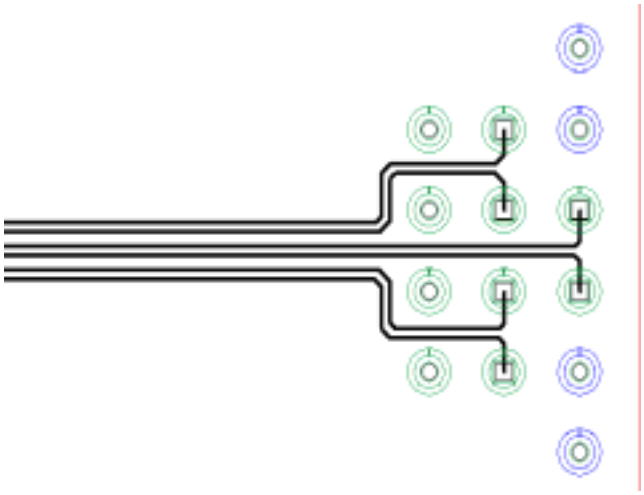


(d)

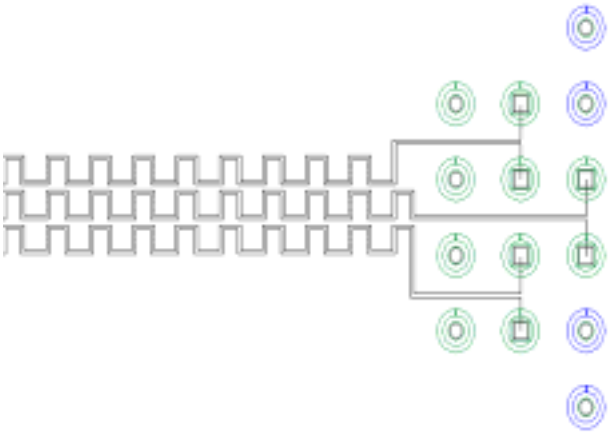
Fig.4. (a) Source Synchronous Topology (b).Source waveform. (c) Differential Topology (e) Differential Eye Diagram.

Crosstalk noise of high speed PCB

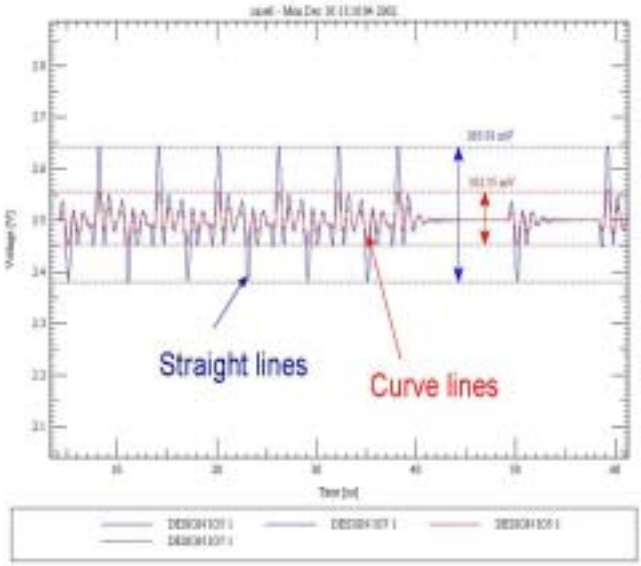
The second layer of PCB in this paper is discussing crosstalk noise. In this layer of PCB layout three different coupled for straight lines and curve lines. Under 2.5v, there is three different coupled send the signal at the same time. To observe the middle one signal between 1→0,0→1 of the crosstalk noise, the driver has sent the signal of "110101010 10101111000.. " in separately. According to Fig5(c), the voltage appeared crosstalk noise from the high changed to low. The curves lines also has crosstalk noise, but it is less than straight lines by comparison. It appeared 263.01mv noise in straight line, and it only has 102.55mv noise in curve lines



(a)



(b)



(c)

Fig.5. (a) Three different coupled for straight lines (b) Three different coupled for curve lines (c) Crosstalk noise waveform

CONCLUSION

Several considerations about power simulation of full populated high speed digital PCB have been presented and discussed. The frequency range (100MHz ~ 3GHz) of interest has been divided into tow sub-ranger. In the lower ring (100MHz ~ 290 MHz) ,where the dimensions of the board are electrically small, the power/ground planes and the on board components have been modelled with lumped circuits. When the distributed effects appear (290MHz ~ 3GHz), the power bus is modelled as a one-dimensional loss transmission line. To handle the high speed signal, the impedance of driver and receiver must consist with termination line. It will have a reflection of signal and the result of noise if the impedance is not match which means the signal will become weak.

When it comes out the crosstalk noise which produced by couple line, the layout of the straight line should be scale down and reduce the noise wave form by the curve line.

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蟻式行動代理人於分散式學習資源搜尋之應用

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摘要

學習資源是分散在不同的學習主機，因此以代理人方式協助學習者搜尋教學資源已成為趨勢。在此我們提出一個方法以行動代理人的技術，讓學習者在分散式學習主機架構下快速找到學習資源。由於行動代理人必須在分散式主機之網路架構下巡行，因此我們該搜索問題轉化成路徑最佳化問題，並提出以蟻式演算法來解決該問題的方法。經實驗模擬結果顯示，學習者的蟻式代理人的數目越多，搜尋能力越強，可較早得到最佳解。學習主機之間的距離越短，越能快速找到最佳化路徑。
關鍵詞：行動代理人、蟻式演算法

Abstract

Learning resources are usually located among distributed learning hosts。The retrieval of distributed learning resources by agent technology for learner becomes more important 。In this paper，a mobile agent method is proposed for the retrieval of learning resources。The retrieval problem is converted into the shortest path optimization problem because the mobile agent has to traverse all of the learning hosts once。A modified ant algorithm is proposed to solve the retrieval problem 。 In our simulation experiments，the more learner's ant agents，the more searching ability and can have better solutions。The less distance from learning hosts，the fast to find the optimal path.。
Keywords：mobile agent、ant algorithm

1. 簡介

近來 e-Learning 的議題在教育上已成一股新興的趨勢，引導學習革命的產生。關於 e-Learning 的定義，大部份學者均將 e-Learning 視為透過網際網路、影音媒體、電腦相關軟硬體系統的同步(Synchronous)或非同步(Asynchronous)工具學習。這樣的學習不受限時間、空間學習，提高學習者的成效。

e-Learning 利用網路技術能即時更新或分享教學資源，因此，當資訊交流量越來越大且資料在不同平台時，學生如何在龐大的資料，快速找到自己需要的資料，已成為重要的研究課題。e-learning 環境是個錯綜複雜的網際網路拓樸(topology)架構，學習教材資訊分散在不同平台主機或是網路上，若以傳統主從架構在運作擷取學習教材時，Client 端要一直與 Server 端保持連線狀態，造成網路頻寬的浪費。對於學習者擷取學習教材閱讀與學習，以行動代理人技術則可以解決這問題，如圖 1，當行動代理人由 Client 端派遣到 Server 端後，Client 端和 Server 端就不需要持續保持連線狀態，對行動代理人而言在 Server 端上執行運作，可以降低網路頻寬流量的資源。

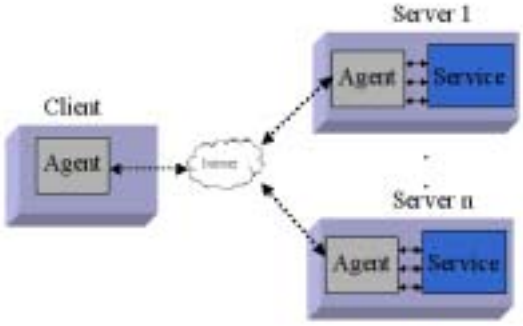

圖 1. 行動代理人架構圖

因此，分散式學習資源之搜尋問題可以使用行動代理人的技術來協助學生快速獲取需要的資訊[1]。行動代理人是一種能夠同時一邊在各電腦終端間移動，一邊能夠自主地分散運算處理的一種程式。它具有提高分散計算系統效率性及便利性，同時又可降低分散式系統上的傳遞延遲與電腦間傳送次數等優點。

目前已有許多研究以行動代理人技術應用於教學資源的分享(Sharing)及擷取(Retrieving)[2,3]，例如 MATHNET System [4,5,6]，它是根據學習者的喜好性(Profile)以智慧型代理人技術搜尋資料。在 FAQFinder System [7]中使用自然語言與 SMART 搜

尋引擎，搜尋儲存在資料庫(Data Base)的 FAQ 資料。由此可見以行動代理人技術應用於教學資料的搜尋是 e-Learning 重要的指標。

本論文旨在提出以蟻式代理人方式應用於分散教學資源的搜尋，使學習者快速獲取資料。本文共分五節，第一節為前言，第二節為分散式學習資源搜尋問題之定義，第三節為蟻式代理人相關研究，第四節為實驗結果探討，第五節為結論。

2. 分散式學習資源搜尋問題之定義

行動代理人根據學習者需要，進行廣泛的資料搜尋，從資料來源分析出符合學習者需求的資訊。資料分散於網路不同主機時，學習者如何能快速獲取資料，以行動代理人能在網路中自主地從一台主機移動到另一台主機，並搜尋學習者需要的資料[8]。因此，路徑策略(Routing)決定行動代理人的移動路徑，行動代理人擷取資訊在網路上路徑決策是個組合最佳化問題(Combinatorial Optimization Problem)，如圖 2，在學習教材分散在網路不同平台主機時，行動代理人所要克服的是路徑決策，這類路徑決策組合最佳化問題即為銷售員旅行(Traveling Salesman Problem)。

圖 2. 分散式學習資源示意圖

銷售員旅行問題為組合最佳化問題中著名的經典問題。銷售員旅行問題是要尋求從某個城市出發，在所有城市皆拜訪一次後又回到起始城市的最短路徑。相對學習者搜尋教學資料問題也是個銷售員旅行問題模型。這樣的問題定義雖然簡單，但求解卻相當困難，已被證明為 NP-complete 問題。

銷售員旅行問題定義如下：設一個圖 $G = (V, E)$，其中 $V = \{v_1, v_2, \ldots, v_n\}$表示頂點的集合，在學習者搜尋模型中表示教學主機集合，$E = \{l_{ij} \mid v_1 、 v_2 \in V\}$表示邊的集合，亦表示教學主機連線之集合，從 G 中找出對 $V = \{v_1, v_2, \ldots, v_n\}$中 $n = |V|$ 個城市拜訪且只拜訪一次的最短路徑。

所以，我們以蟻群算法在行動代理人架構下，對於學習者在分散不同平台或網路的教學教材擷取，提出蟻式代理人模式來協助學習者對資訊或教學教材取得的方法。

3. 蟻式代理人

蟻群算法(Ant Colony System,ACS)是受自然界中螞蟻的行為啟發而發展的一種啟發式算法，由意大利學者 M. Dorigo , V. Maniezzo 等人提出[9,10]。且在求解銷售員旅行問題、指派問題(Assignment Problem)、Job－Shop 調度問題等，都有較好的結果。蟻群算法充分利用了生物螞蟻個體之間經由一種稱之為費洛蒙(Pheromone)的物質進行信息傳遞，螞蟻在搜索過程中，能夠在其往來路徑上留下揮發性化學物質的費洛蒙，其他螞蟻以能夠知道前進的方向，同時，這樣的費洛蒙也會隨著時間逐漸衰減，因此，大量的蟻群產生越大的費洛蒙，即表示路徑上螞蟻越多，選擇該路徑的機率就越大。

在教學搜尋模型中，我們定義學習者的學習歷程或記憶量為費洛蒙值(τ)，蟻式代理人在每個教學主機之間會留下學習歷程記憶量，並隨時間的推進記憶量會慢慢衰退，教學主機之間的傳遞距離或成本的反函數為能見度，蟻式代理人會拜訪每部教學主機。如圖 3。

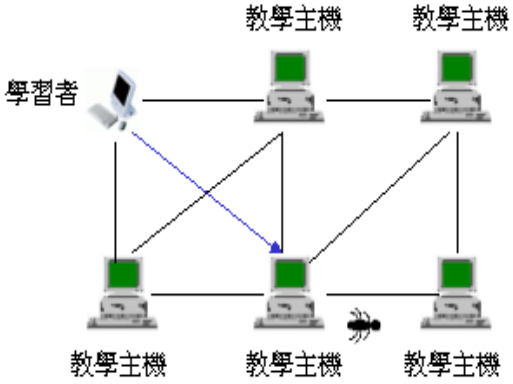

圖 3. 蟻式代理人搜索路徑圖

3.1 蟻式代理人演算法原理

圖 4 為蟻式代理人系統示意圖。假設 D 和 H、H 和 B 之間的距離為 1，D 和 C、C 和 B 之間的距離為 0.5，在一個時間單位內有 30 個蟻式代理人由 A 點到達 B 點，同樣有 30 個蟻式代理人由 E 點到達 D 點，蟻式代理人走的速度均是 1 單位距離/單位時間，每個蟻式代理人走過的路徑上留下一個單位的費洛蒙信息量。假設初始時刻 T=0 時各路徑均無蟻式代理人走過，因此，在 B 點和 D 點的各 30 個蟻式代理人選舉所走路線的機率是相等的，即有 15 個蟻式代理人選擇 DH(BH) 路徑，另外 15 個蟻式代理人選擇 DC(BC)路徑。由於 $d_{DH} = d_{BH} = 2d_{DC} = 2d_{BC}$，所以經過 1 個單位時間後，走過路徑 BCD 的蟻式代理人數目是走過 BHD 路徑蟻式代理人數目的兩倍。在 T=1 時，有 30 個新的蟻式代理人在 B 點和 D 點，根據留下的費洛蒙量的多少，蟻式代理人選擇 DCB 路徑的機率是 DHB 路徑兩倍，也就是選擇 DCB 路徑的蟻式代理人個數為 20 個，選擇 DHB 路徑的個蟻式代理人個數為 10 個。這樣的過

程一直會持續到所有的蟻式代理人最終都會選擇最短路徑，因此，個蟻式代理人演算法的精神：一個蟻式代理人要在不同的路徑中選擇，那麼，那些被先蟻式代理人大量選擇的路徑，也就是費洛蒙物質存留較多的路徑，被選中的機率較高，即較多的費洛蒙物質意味著較短的路徑。

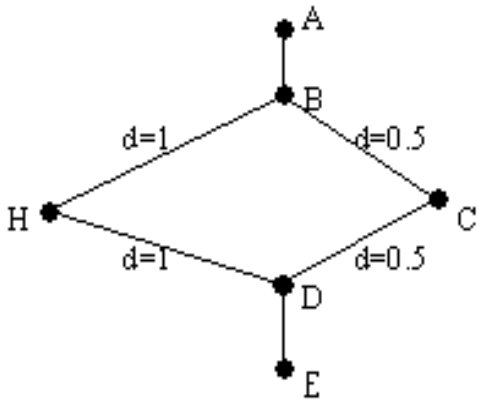

圖 4. 蟻式代理人系統示意圖

3.2 蟻式代理人系統模型

在蟻式代理人的架構, 設有 n 個教學主機的集合，$d_{ij}(i,j=1,2,\ldots,n)$表示教學主機 i 和 j 間的距離；歐幾里德空間中，$d_{ij}=\{(X_i-x_j)^2+(Y_i-Y_j)\}^{1/2}$，$\tau_{ij}(t)$表示在 t 時刻教學主機 i 和教學主機 j 之間的費洛蒙量亦即學習者的學習歷程量，$b_i(t)$表示 t 時刻位於教學主機 i 的蟻式代理人的個數，則有 $m=\Sigma b_i(t)$。每個蟻式代理人在 t 時刻選擇下一個教學主機，並在 $t+1$ 時刻到達。經過 n 個時刻，所有蟻式代理人都完成了一次周遊，在這個時間點，學習者的學習歷程量(費洛蒙)強度根據下面公式進行更新：

$$\tau_{ij}(t+n)=\rho\,\tau_{ij}(t)+\Delta\tau_{ij} \qquad (1)$$

參數 ρ 表示學習歷程的持久性；$1-\rho$ 表示學習歷程的揮發程度，係數 ρ 必須設為小於 1 的數，以避免學習歷程無限制的增加，而無法獲得全區域最佳解(Global optimum)。

$$\Delta\tau_{ij}=\sum_{k=1}^{m}\Delta\tau_{ij}^{k} \qquad (2)$$

$\Delta\tau_{ij}$ 為第 k 個蟻式代理人在 t 時刻與 $t+n$ 時刻之間留在路徑(i,j)上的學習歷程量。

$$\Delta\tau_{ij}^{k}=\begin{cases}Q/L_k & \text{，第 } k \text{ 個蟻式代理人在 } t \text{ 和 } t+n \text{ 時刻之路徑長度}\\ 0 & \text{，其他}\end{cases} \qquad (3)$$

Q 為常數，L_k 是第 k 個蟻式代理人在本次循環中所走過的路徑長度。螞蟻蟻式代理人系統具有記憶功能，隨著進化過程來計算蟻式代理人當前所走路線的長度。

我們定義 $P_{ij}^{k}(t)$表示在 t 時刻蟻式代理人 k 由教學主機 i 到教學主機 j 的機率：

$$P_{ij}^{k}(t)=\begin{cases}\dfrac{[\tau_{ij}(t)]^{\alpha}\cdot[\eta_{ij}]^{\beta}}{\sum_{k\in allowed_k}[\tau_{ik}(t)]^{\alpha}\cdot[\eta_{ik}]^{\beta}} & \text{，教學主機 } j\in allowed_k\\ 0 & \text{，其他}\end{cases} \qquad (4)$$

η_{ij} 為 $1/d_{ij}$(d_{ij} 為教學主機 i 到教學主機 j 的距離)即能見度，α 和 β 為控制學習歷程量和能見度之間重要的參數。因此，若 $\alpha=0$，則較近的教學主機被選中的機率大，這樣類似貪心演算法(Greedy Algorithm)；若是 $\beta=0$，蟻式代理人會漫無目標的進行搜索，難以收斂。一般設置搜索次數計數器 NC, 當達到設定值時結束, 最短路徑為 $L_{min}=min\ L_{k\,min}(l=1,2..,NC)$。

由上述可知，蟻式代理人算法的基本思想為：選擇機制中，費洛蒙量越大的路徑，被選擇的機率越大。更新費洛蒙機制中，路徑上的費洛蒙量會隨蟻式代理人的經過而增加，相對也會隨著時間增加逐漸減少。蟻式代理人算法也有一些缺陷，例如，當群體規模較大時，要找出一條較好的路徑需要較長的搜索時間。因此，M.Dorigo 等人在基本的蟻群算法上提出 Ant-Q System [11]的蟻群算法，對於以費洛蒙量最大的路徑被選中機率較大，充分利用學習機制，以強化整個費洛蒙量。

3.3 Ant-Q 算法

在 Ant-Q 算法中，螞蟻 k 的選擇路徑規則為:

$$j=\begin{cases}\underset{j\notin tabu_k}{args\ max}\{[\tau_{ij}(t)][\eta_{ij}(t)]^{\beta}, & if\ q\le q_0\\ S, & otherwise\end{cases} \qquad (5)$$

上式中 S 是依據 $P_{ij}^{k}(t)$選擇，$tabu_k(k=1,2,..,m)$用以記錄蟻式代理人 k 當前所走過的教學主機，$0\le q_0\le 1$ 是初始設定的參數；q 是一個隨機數。該算法增強了搜索的多樣性，以避免過早陷於搜索停滯狀態。每隻螞蟻選擇一個城市以後，更新路徑上的費洛蒙量，亦即蟻式代理人到達教學主機後，更新學習歷程：

$$\tau_{ij}(t+1)=(1-\rho)\,\tau_{ij}(t)+\rho\,\Delta\tau_{ij}^{k} \qquad (6)$$

$$\Delta\tau_{ij}^{k}=\begin{cases}Q/L_{jb} & \text{，蟻式代理人 } k \text{ 走過教學主機 } i \text{ 與教學主機 } j \text{ 時}\\ 0 & \text{，其他}\end{cases} \qquad (7)$$

L_{jb}是蟻式代理人 k 從開始到當前教學主機已走過的路徑長度。當 m 個蟻式代理人走完所有教學主機以後，計算最佳路徑長度並保留。

4. 實驗

整個系統蟻群演算法之流程如圖 5，本實驗中

演算法的結束條件以執行固定的迭數(Iteration)停止，即不管收斂結果如何，此演算法在執行完固定的迭數就停止繼續往下搜尋。

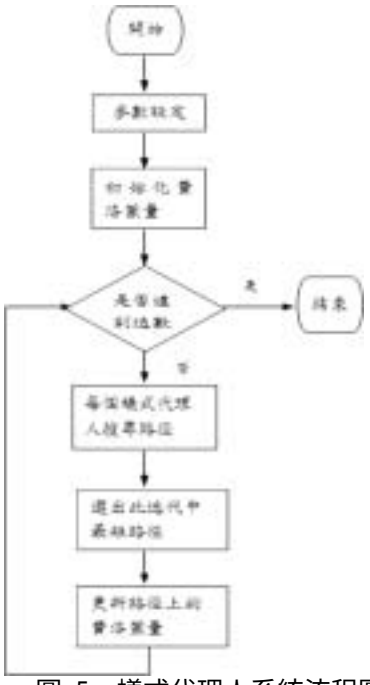

圖 5．蟻式代理人系統流程圖

用上述 Ant-Q 演算法，對由 20 個教學主機組成的問題進行實驗，實驗中，先設定 β =0.7， ρ =0.9，迭代數到達 1500 時，停止演算法繼續搜尋，如圖 6 所示。並調整蟻式代理人數目結果見圖 7。

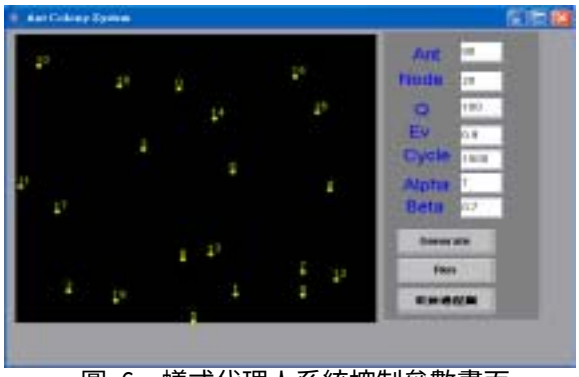

圖 6．蟻式代理人系統控制參數畫面

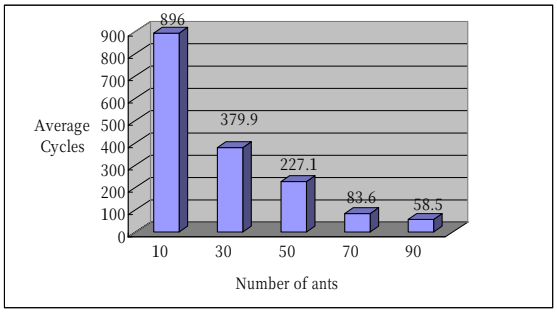

圖 7．蟻式代理人系統調整螞蟻數目結果

對於不同的螞蟻數目實驗中，蟻式代理人數目越少，則整體收斂的時間較長且所花費的迭數也較大，如圖 8 所示，相對蟻式代理人數數目越多時，在此演算中平均收斂的迭數較小，即可較早得到最佳解。因此，蟻式代理人數的數目越多，整體的全局搜索能力越強，但數目加大將使演算法搜尋時間增長，對此我們選取實驗中的蟻式代理人數數目 90 隻，為此實驗的最佳解。

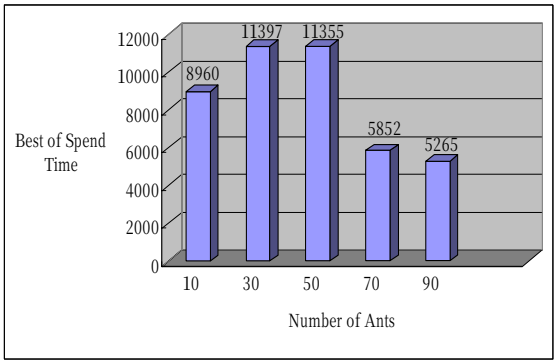

圖 8．蟻式代理人數目不同時的平均搜尋時間

β 值為演算法能見度(η)的控制參數，在本實驗中將調整 β 值，並將蟻式代理人數目改為上述實驗中的 90 個，其他參數不調整。不同的 β 參數值結果如圖 9。

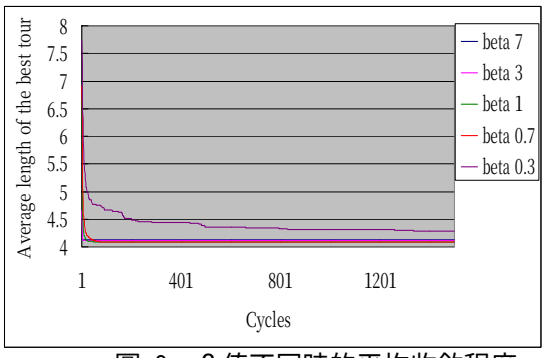

圖 9．β 值不同時的平均收斂程度

β 值的大小影響收斂的速度，過大的 β 值將造成整個演算法陷入停滯狀態，實驗中的 β 值為 7，使得所得到的解並不是最佳解；β 值為 0.3，將使收斂不易，所得到解是區域最佳化(Local optimization)解，如表 1。在此實驗所得到的最佳路徑參數控制組合：β =0.7、ant 數目=90、 ρ =0.9，如圖 10 所示。

表 1　平均收斂所需的迭數

β	ρ	最短路徑長度	平均達到收斂所需的迭數
7	0.9	4.1341574	4
3	0.9	4.1165012	9
1	0.9	4.0805739	121
0.7	0.9	4.0805739	87
0.3	0.9	4.2837828	1500

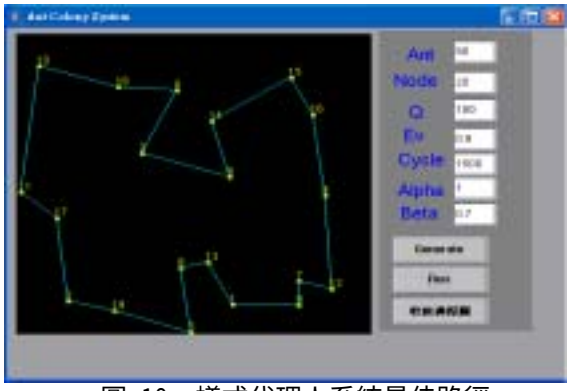

圖 10．蟻式代理人系統最佳路徑

影響 Ant-Q 演算法的因素有以下：蟻式代理人的數量，費洛蒙量，參數控制值(β)。在選擇機制中：費洛蒙越大的路徑，被選擇的機率越高。在更新機制中:路徑上費落蒙量會隨蟻式代理人數目經過數目越多而增加，相對也會隨時間的增進慢慢的衰減。蟻式代理人之間經由費洛蒙來進行通信，這樣具有組織機制使得演算法有啟發最佳解(Global optimization)的能力。

5. 結論

在分散式教學主機，以行動代理人技術來獲取教學資源已成為不可或缺的方式，因此學習者在迫切需要教學資源時，行動代理人能漫遊於教學主機之間擷取教學資源。

本論文提出的蟻式行動代理人具有正迴饋特點。正迴饋是一種強化學習能力，讓學習者對教學資源取得有相當迫切性之時，保證快速性取得教學資源。使學習者將主要精神放在學習與思考上。

此蟻式代理人系統未來可以朝向使用者的喜好性(Profile)發展，例如：由於蟻式代理人系統中的各體具有隨機性，當蟻式代理人群體規模較大時，要找出一條最佳的路徑，就需要較長的搜尋時間，因此，有效調整蟻式代理人數目、控制費洛量來盡量避免其缺陷。因此，未來將可在此基礎上建立使用者喜好性分析系統更完美。

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低電壓大電流多相式降壓型電源轉換器之效率分析與設計
Efficiency Analysis and Design for High Current Low Voltage Multi-phase Buck Converters

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摘要

系統電壓逐漸降低，功率需求日益增加，體積要求輕薄短小，表面溫度不可過高，這是電源轉換器所面臨之艱難挑戰，本文將運用理論分析、模擬與實際量測，找出所有的功率損耗源，再就排名前幾大的損耗源，進行研究與分析，選擇效能最佳的功率元件，以及零電壓的開關切換模式，最佳的印刷電路板佈局，使得功率損耗由 22 瓦（W）降至 12 瓦，效率由 82.78%提昇至 89.46%，讓原本要用 180 瓦電源穩壓器（Adaptor）之筆記型電腦改用 150 瓦，如此成本可降低 10 美元，而且更降低散熱成本，因此效率提昇 6.68%雖然會增加成本，但整體而言，卻是達到降低成本、輕薄短小、符合表面溫度…等等之需求。

關鍵詞：多相式降壓型電源轉換器、效率、零電壓切換。

Abstract

Low voltage and high power consumption dc-dc converter is popular in the future. The challenge of power dissipation and thermal designed is difficult. The proposed high current low voltage multi-phase buck converter can significantly improve efficient. Simulation and experiment results show the advantage of the converter in this paper. In order to find out the several large of power loss for further research and analysis, choosing the best power component in terms of performance, using zero voltage switching for power mode, and adopted the best circuit board print layout will lessen heat wear and tear from 22W to 12W and increasing the efficiency from 82.78% to 89.46%. Thus, it will allow us to replace the 180W mobile computer adapter with a 150W. This will greatly reduce the cost of heat sink. Nevertheless the main goal of reducing product cost and the reduction in the size and weight of the notebook computer, while conforming to surface temperature and other requirements, has been reached.

Keywords: Multi-phase Buck converters, Efficiency, Zero Voltage Switching

1. 前言

低電壓大電流多相式降壓型電源轉換器的功率元件，如功率電晶體與電感的耐電流一般約為 20 安培（A）至 40 安培[1,2]，而且與熱息息相關，電流大消耗功率大就越熱，造成功率元件的效能差，效率當然就不好，因此目前業界單一相以 30 安培為設計準則，若要設計一個 120 安培的電源轉換器，必須採用 4 相式及波寬調變（Pulse Width Modulated, PWM）的技術[3~7]，此技術必須要克服的問題有兩點：(1).其動態電流變化非常的大，因此偵測動態電流的響應時間要非常快，且動態電流變化量的資訊要立刻反應給 PWM 控制器，而 PWM 控制器會調整適當的波寬大小因應，讓動態電壓下降斜率之需求規格，完全符合 Intel VRM10.1 所制定的規範[8]；(2).每一相的電流必須達到完全平衡，則每一相的功率元件方可平均分配消耗功率，使每一功率元件達到最佳性能，進而達到最好的效率。

效率對低電壓大電流降壓型電源轉換器之重要性，以下舉例其計算式及說明可以得知：

$$\text{效率}(\eta) = \frac{\text{輸出功率}(P_o)}{\text{輸入功率}(P_{in})} = \frac{\text{輸出功率}(P_o)}{\text{輸出功率}(P_o) + \text{損耗功率}(P_{total\_losses})} \quad (1)$$

對一個提供 150 瓦的電源轉換器而言，分別試算效率是 80%與 90%之功率損耗，80%之功率損耗是 37.5 瓦而 90%是 16.67 瓦，功率損耗多出 20.83 瓦，這 20.83 瓦就要多出一筆可觀的散熱成本，且增加寸土寸金的空間及重量，由此可知，如何設計高效率的電源轉換器，對電子產品是非常的重要，而且目前產業界已面臨此一問題。

2. 理論分析

將四個降壓型電源轉換器並聯如圖 1 所示，線路中電容（ Co ）有阻止電壓瞬間變化的特性，利用儲存或釋放電荷的方式阻止電壓瞬間變化，電感（ $L_{(n)}$ ）有阻止電流瞬間變化的特性，利用儲存或釋放磁場的方式阻止電流瞬間變化，多相式降壓型電源轉換器巧妙利用這兩個零件的特性，配合波寬調變控制器（PWM Controller）於一個週期內，在不同時間分別控制每一相功率電晶體開關的能量，達到輸出電壓穩定的功能，簡單的說就是負載需要多少能量才給多少能量，不會浪費多餘的能量並提高效率。配合電感應用的兩大原理：(1).電感電壓秒平衡（Inductor Volt-Second Balance），電感電壓在開關導通所得的積分面積加開關截止所得的積分面積等於零；(2).電感電流秒平衡（Inductor Current-Second Balance）的原理，電感電流在開關導通所得的積分面積與開關截止所得的積分面積相等，如圖 2 所示，可得知：

$$\left(V_{in}-V_o\right)DT_S+\left(-V_o\right)\left(1-D\right)T_S=0 \quad (2)$$

$$\frac{V_{in}-V_o}{L}DT_S=\frac{V_o}{L}\left(1-D\right)T_S \quad (3)$$

其中責任週期 $D=V_o/V_{in}$ ，V_{in} 為輸入電壓，V_o 為輸出電壓，T_S 為一個週期，L 為電感。

多相式降壓型電源轉換器之線路設計如圖 3 所示，圖 3(a)是動態電流偵測、輸出電壓誤差偵測與低通濾波之線路設計，其波寬調變控制器及所有偵測器都以內建在控制晶片，圖 3(b)是每一相的開關導通阻抗（SW Rds）內部線路，其中包含開關及驅動控制器，以下就控制晶片之外部零件的計算方式條例說明：(1). R_T 調整 PWM 的工作頻率，如下式：

$$R_T=\frac{1}{n\times f_{sw}\times 4.7pF}-27k\Omega \quad (4)$$

其中 n 代表多少相，f_{sw} 為 PWM 工作頻率設計值，由式（4）得知 R_T 與 PWM 工作頻率成反比。(2). 電感及其直流阻抗 R_L 、R_{CS} 、C_{CS} 、$R_{PH(x)}$ ，構成電流偵測器迴路，偵測流過電感電流且快速反應給 PWM 控制器，以達到動態負載變化很大時，乃可微調每一相的電流平衡，及輸出電壓下降斜率，使符合 Intel 的設計規範小於或等於 $1m\Omega$ ，如下式：

$$R_{droop}=\frac{R_{CS}\times R_L}{R_{PH(x)}}\le 1m\Omega \quad (5)$$

$$R_{CS}=\frac{L}{R_L\times C_{CS}} \quad (6)$$

(3). R_B 微調輸出電壓補償，如下式：

$$R_B=\frac{V_{OFFSET}}{I_{FB}} \quad (7)$$

其中 $V_{OFFSET}=V_{VID}-V_{ONL}$ ，是設定電壓與理想電壓之電壓差，I_{FB} 是補償電流約為 15uA，此設計可微調輸出電壓。(4).回授迴圈之零件設計，如下式：

$$R_E=nR_{droop}+A_DR_{ds}+\frac{R_LV_{RT}}{V_{VID}}+\frac{2L\left(1-nD\right)V_{RT}}{nC_XR_{droop}V_{VID}} \quad (8)$$

$$T_A=C_X\left(R_{droop}-R'\right)+\frac{L_X}{R_{droop}}\times\frac{R_{droop}-R'}{R_X} \quad (9)$$

$$T_B=\left(R_X+R'-R_{droop}\right)C_X \quad (10)$$

$$T_C=\frac{V_{RT}\left(L-\frac{A_D\times R_{ds}}{2f_{sw}}\right)}{V_{VID}\times R_E} \quad (11)$$

$$T_D=\frac{C_X\times C_Z\times R_{droop}^2}{C_X\left(R_{droop}-R'\right)+C_Z\times R_{droop}} \quad (12)$$

$$C_A=\frac{n\times R_{droop}\times T_A}{R_E\times R_B} \quad (13)$$

$$R_A=\frac{T_C}{C_A} \quad (14)$$

$$C_B=\frac{T_B}{R_B} \quad (15)$$

$$C_{FB}=\frac{T_D}{R_A} \quad (16)$$

其中 A_D 為電流平衡器的放大倍率 5 倍 ，V_{RT} 為 0.49V，R' 是印刷電路板的阻抗一般約為 0.5mΩ，V_{VID} 是輸出電壓設定值，T_A 、T_B 、T_C 、T_D 為時間常數，R_X 為輸出電容的 ESR 值，R_{ds} 為功率電晶體下橋之導通阻抗，由式（8）至（16）分別可計算出 C_A 、C_B 、C_{FB} 、R_A 之設計值。(5). C_{DLY} 與 R_{DLY} 可調整軟式起始的延遲時間，如下式：

$$C_{DLY}=\left(20uA-\frac{V_{VID}}{2\times R_{DLY}}\right)\times\frac{t_{SS}}{V_{VID}} \quad (17)$$

其中 t_{SS} 是延遲時間的設計值。(6). R_{LIM} 可設定最大電流限制點，如下式：

$$R_{LIM}=\frac{A_{LIM}\times V_{LIM}}{I_{LIM}\times R_{droop}} \quad (18)$$

其中 A_{LIM} 為 $10.4mV/uA$ ，V_{LIM} 放大倍率設定值 3V，I_{LIM} 為最大電流限制設計值。(7).電感及輸出電容的選擇，與輸出電壓漣波設計有關，如下式：

$$L\ge\frac{V_{VID}\times R_{droop}\times\left(1-\left(n\times D\right)\right)}{f_{sw}\times V_{ripple}} \quad (19)$$

$$C_{x(\min)}\ge\frac{L\times\Delta I_O}{n\times\left(R_{droop}+\frac{\Delta V_{rl}}{\Delta I_O}\right)\times V_{VID}}-C_Z \quad (20)$$

$$C_{x(\max)}\le \frac{L}{nK^2R_{droop}^2}\times\frac{V_V}{V_{VID}}\left(\sqrt{1+\left(t_v\frac{V_{VID}}{V_V}\times\frac{nKR_{droop}}{L}\right)^2}-1\right)-C_Z \quad (21)$$

其中 V_{ripple} 為輸出電壓漣波設計希望值，ΔI_O 是動態負載電流最大變化量，其關係式為

$\Delta V_O = \Delta I_O \times R_{droop} + \Delta V_{rl}$ ，ΔV_{rl} 是暫態負載之最大漣波電壓， $K = \ln\left(V_{ERR} / V_V\right)$ 而 V_V 是設定電壓值，V_{ERR} 為設定電壓之誤差值，t_v 是設定電壓之誤差時間， $C_{x(\min)}$ 、 $C_{x(\max)}$ 為濾除漣波的大容量電容之最小值與最大值，C_Z 濾除高頻雜訊之小容量電容。(8). 功率電晶體的選擇，下橋（Low-side）同步用功率電晶體（SF），最大考量是導通電阻（ $R_{ds(on)}$ ），所產生的傳導損耗（ $P_{C(SF)}$ ），如下式：

$$P_{C(SF)} = (1-D) \times \left[\left(\frac{I_O}{n_{SF}} \right)^2 + \frac{1}{12} \times \left(\frac{nI_R}{n_{SF}} \right)^2 \right] \times R_{DS(SF)} \quad (22)$$

上橋（High-side）為主開關功率電晶體（MF），最大考量是輸入電容值（ C_{iss} ）及導通電阻（ $R_{ds(on)}$ ），所產生的切換損耗（ $P_{S(MF)}$ ）及傳導損耗（ $P_{C(MF)}$ ），如下式：

$$P_{S(MF)} = 2 \times f_{sw} \times \frac{V_{CC} \times I_O}{n_{(MF)}} \times R_G \times \frac{n_{(MF)}}{n} \times C_{iss} \quad (23)$$

$$P_{C(MF)} = D \times \left[\left(\frac{I_O}{n_{MF}} \right)^2 + \frac{1}{12} \times \left(\frac{nI_R}{n_{MF}} \right)^2 \right] \times R_{DS(MF)} \quad (24)$$

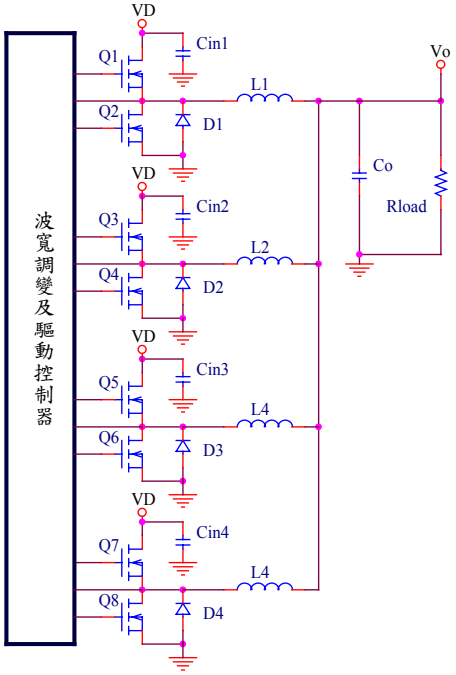


圖 1. 多相式降壓型電源轉換器之基本架構

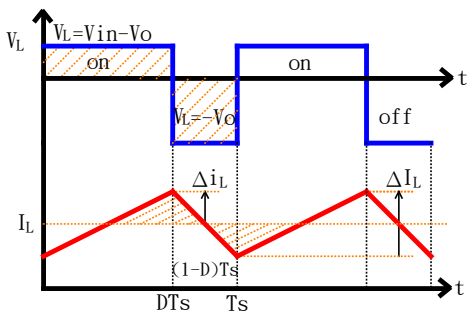
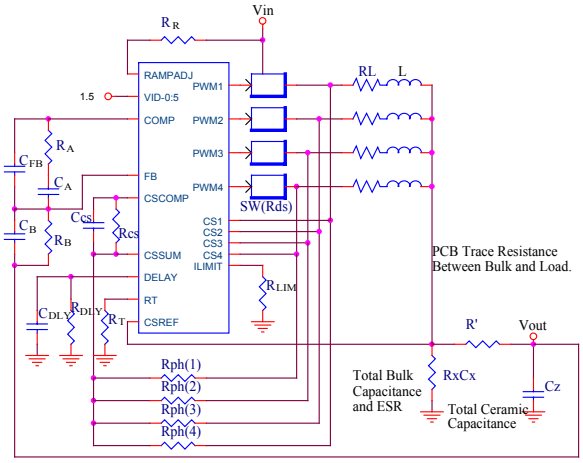
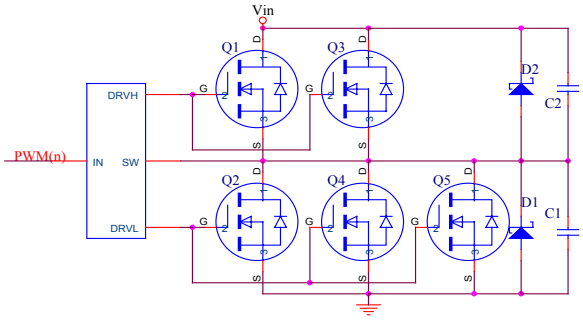


圖 2. 電感之電壓電流波形



3(a) 多相式降壓型電源轉換器



3(b) 開關導通阻抗（SW Rds）內部線路

圖 3. 多相式降壓型電源轉換器之線路設計

3. 效率分析

降壓型電源轉換器的功率損耗源，共分為五大類：(1).控制晶片（PWM and Driver IC）的功率損耗；(2).功率電晶體（Power MOSFET）的功率損耗；(3).電感（Choke）的功率損耗；(4).輸出入電容（Input/Output Capacitor）的功率損耗；(5).印刷電路板（PCB）佈線的功率損耗，以上五大功率損耗若越大則其效率就會越差，由式（1）可得知。

3.1. 控制晶片的功率損耗

控制晶片一般分為波寬調變控制晶片（PWM Controller），及驅動控制晶片（Driver Controller），在規格書內都會註明總功率損耗，驅動功率損耗與 V_{GS} 的電壓設計有關，如下式：

$$V_{GS} = \frac{\frac{1}{SC_{GS}}}{\frac{1}{SC_{GS}} + \frac{1}{SC_{GD}}} \times V_{DS} = \frac{1}{1 + \frac{C_{GS}}{C_{GD}}} \times V_{DS} \quad (25)$$

3.2. 功率電晶體的功率損耗

一般降壓型電源轉換器的功率電晶體，都會採用金屬氧化物半導體之場效應電晶體（Metal-Oxide Semiconductor Field- Effect Transistor, MOSFET），內部結構如圖 4 所示，其製程是將矽半導體參雜擴散形成 P 或 N 的通道，再加氧化物絕緣後，利用金

屬做為閘極控制通道的大小，以電壓控制電阻的方式，因此功率電晶體應用在降壓型電源轉換器，會產生四大類的功率損耗：(1).切換損耗（Switching losses）；(2).傳導損耗（Conduction losses）；(3).驅動損耗（Gate charge losses）；(4).輸出電荷損耗。

切換損耗：功率電晶體在導通與截止瞬間會有很大的能量損耗，如圖 5 所示，開關的上升與下降時間都會產生切換損耗（Switching Losses），其計算式如下：

$$P_S = \frac{ID \times Q_{gd} \times VD \times f_{sw}}{I_G} + \frac{ID \times Q_{gs2} \times VD \times f_{sw}}{I_G}$$

$$= \frac{(ID \times VD \times f_{sw})(Q_{gd} + Q_{gs2})}{I_G} \quad (26)$$

$$P_S = \frac{ID \times VD \times V_{GS} \times C_{iss} \times f_{sw}}{I_G} \quad (27)$$

其中 Q_{gd} 為功率電晶體閘極（Gate）至洩極（Drain）之總充電電荷，Q_{gs2} 為功率電晶體閘極至源極（Source）之總充電電荷，C_{iss} 為功率電晶體的總輸入電容值，以上是兩套不同的計算公式，分別於不同的參考文獻得知，以下章節介紹之傳導損耗及驅動損耗的計算公式亦同。

傳導損耗（Conduction Losses）：功率電晶體在完全導通下的損耗，一般而言電源轉換器的應用都會採用 N-MOS，因為 N-MOS 在相同的製程與相同的體積、導通寬度，具有更低的導通電阻，理由是電子的移動率是電洞的兩倍，計算式如下:

$$P_{C\_CF} = ID_{ave}^{\ 2} \times R_{ds(on)\_CF} \times D \quad (28)$$

$$P_{C\_SF} = ID_{ave}^{\ 2} \times R_{ds(on)\_SF} \times (1-D) \quad (29)$$

$$P_{C\_CF} = ID_{rms\_CF}^{\ 2} \times R_{ds(on)\_CF} \quad (30)$$

$$P_{C\_SF} = ID_{rms\_SF}^{\ 2} \times R_{ds(on)\_SF} \quad (31)$$

$$ID_{rms\_CF} = ID_{Peak} \times \sqrt{D \times \frac{Kp^2}{3} - Kp + 1} \quad (32)$$

$$ID_{rms\_SF} = ID_{Peak} \times \sqrt{(1-D) \times \frac{Kp^2}{3} - Kp + 1} \quad (33)$$

其中電流峰值 $ID_{Peak} = (ID_{ave} \times \Delta ID/2)$，$P_{C\_CF}$ 為上橋的傳導損耗，$R_{ds(on)\_CF}$ 為上橋的導通阻抗，P_{C_SF} 為下橋的傳導損耗，$R_{ds(on)\_SF}$ 為下橋的導通阻抗，$K_P = \Delta ID / ID_{Peak}$ 。

驅動損耗：功率電晶體需要在閘極加電壓才能導通，從閘極看進去有一等效輸入電容（Ciss），當功率電晶體導通時，在閘極加電壓等於對此電容充電，而截止時等於對此電容放電，切換式電源不斷的導通與截止，使閘極不斷的充放電所造成的損耗，稱為驅動損耗（Gate charge loss），其計算式如下：

$$P_G = V_{GS} \times Q_g \times f_{sw} \quad (34)$$

$$P_G = V_{GS}^{\ 2} \times C_{iss} \times f_{sw} \quad (35)$$

其中 Q_g 為功率電晶體閘極之總充電電荷，C_{iss} 為功率電晶體的總輸入電容值。

輸出電荷（Q_{oss}）損耗：功率電晶體的總輸出電容值充放電所造成的損耗，其計算式如下：

$$P_{Qoss} = \frac{VD \times Q_{oss} \times f_{sw}}{2} \quad (36)$$

其中 Q_{oss} 為功率電晶體總輸出之充電電荷。

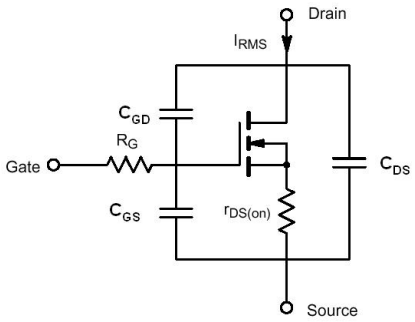


圖 4. 功率電晶體的內部結構

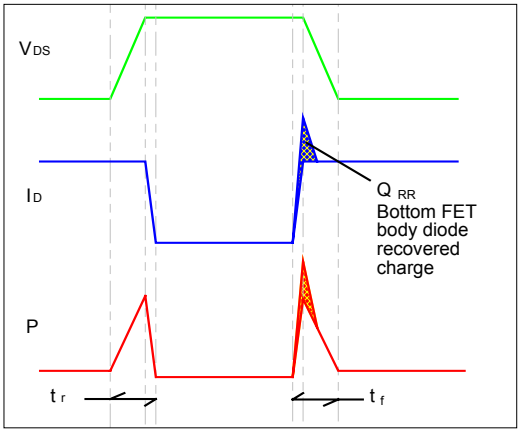


圖 5. 上橋（High-side）功率電晶體的切換損耗

3.3. 電感（Choke）的功率損耗

電感是由鐵心材料（導磁系數）、線徑、鐵心體積（儲能大小）、圈數所設計而成，銅損是繞線的直流阻抗（$R_{dc,Cu}$）所產生，$R_{dc,Cu}$ 值越小銅損越低。由歐姆定律得知如下式：

$$P_{Cu,Losses} = ID_{ave}^2 \times R_{dc,Cu} \quad (37)$$

其中 $R_{dc,Cu} = \rho \times L / A$，$\rho$ 是銅的電阻系數，L 是繞線長度，A 是導線的截面積。金屬材料大多具有正溫度係數的阻抗，銅阻抗亦會隨溫度上升而上升，其關係式為：

$$R_t = R_{25}\left[1 + 0.04(T - 25)\right] \quad (38)$$

R_t 是實際工作溫度下之銅線阻抗，R_{25} 是室溫下的阻抗，T 是實際工作溫度。

在相同磁通密度，頻率越高鐵損（Core Losses）會越大，鐵心溫度增加其磁飽和(當鐵心溫度上升至居禮溫度時，鐵心就不具磁性)機率會增加，一般鐵

損$\left(P_{L,Fe}\right)$包含磁滯損與渦流損，計算式如下：

$$P_{L,Fe}=C_m\times f_{sw}^{x}\times B_m^{y} \quad (39)$$

$$L\times\Delta I=N\times\Delta B\times Ac \quad (40)$$

$$L=\frac{4\pi\times N^2\times\mu_1\times Ac\times10^{-2}}{Le} \quad (41)$$

其中C_m是常數等於 157.88，x為 0.64，y為 2.22，L是鐵心電感值，N是線圈圈數，ΔB是磁通變化量，μ_1是導磁系數，Ac是鐵心的截面積，Le是鐵心有效長度，B_m是磁通密度。

3.4. 輸出入電容的功率損耗

電容的結構為一平行導電板，電壓加在平行導電板上，電荷聚集在導電板的正負之間形成電場，電荷密度與電場強度成正比，且電場強度為電壓的方向梯度（$\vec{E}=-\nabla V$），電容大小與平行導電板間之距離成反比，與平行導電板之面積及介電係數成正比，當電荷固定則電容與電壓成反比，由式(43)可得知，電容越大電壓變化量越小，電容具有阻止電壓變化的特性，由式（44）可得知，電容的串連等效電阻（Equivalent Series Resistance, ESR）值越小電壓變化量越小，且總功率損耗也越小。

$$C=\frac{I\times T}{V}=\frac{Q}{V} \quad (42)$$

$$\Delta Q=C\times\Delta V=\Delta I\times T \quad (43)$$

$$P_{Cap\_Losses}=ID_{ave}^{2}\times C_{ESR} \quad (44)$$

3.5. 印刷電路板佈線的功率損耗

一般印刷電路板（PCB）在走線部份的製程都是以銅為材料，銅的特性其一是越細越長其內阻就越大，由式（45）可得知，其二溫度越高內阻會隨著增加。計算式如下：

$$P_{PCB,Losses}=ID_{ave}^{2}\times R_{dc,PCB} \quad (45)$$

其中印刷電路板佈線的內阻$R_{dc,PCB}=\rho\times L/A$，$\rho$是銅的電阻系數，$L$是印刷電路板布線長度，$A$是印刷電路板布線銅鉑的截面積。

4. 轉換器之設計

轉換器之設計要點簡單而言，就是以最低的成本達到最好的效率並符合設計規格之需求，以下就符合規格需求之設計、如何提昇效率之設計及印刷電路板佈線與散熱之設計，作更進一步的說明：

4.1 設計規格

依據 Intel VRM10.1 所制定的設計規範：(1).當負載需求電流達 101 安培，則其下降斜率阻抗為 1mΩ，亦既是電流每下降 1 安培，電壓只能下降 1mV，如圖 6 所示。(2).暫態響應時間必須低於 350uS，由式(20)與(21)將ΔV_{rl}：38mV，ΔI_O：95A，V_{VID}：1.5V，K：4.6，V_Y：450mV，C_Z：180uF 代入可以計算出，輸出電容的容量必須限制在 7.45mF 至 47.47mF。(3).輸出之最大漣波電壓（ΔV_{rl}）設計：當動態負載電流最大變化量（ΔI_O）是 95A 時為±19mV；55A 時為±25mV。漣波電壓與輸出電容的串連等效電阻（C_{ESR}）成反比，計算式如下：

$$\Delta V_{rl}=\Delta I_O\times C_{ESR} \quad (46)$$

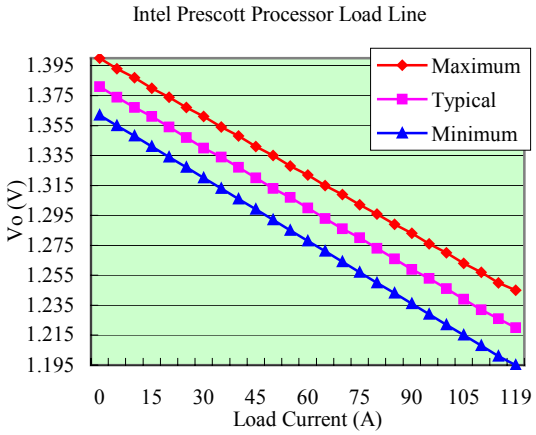


圖 6. 輸出電壓下降斜率設計規範

4.2 提昇效率之設計

如何提昇效率可從兩方面進行，其一是零件的選擇及相關設計技巧，如零電壓 LC 共振之軟性切換模式，其二是印刷電路板佈線技巧，由第三章節所做之效率分析及模擬與量測結果得知，如圖 7 所示，功率電晶體佔總損耗功率的 43%，電感佔總損耗功率的 27%，輸出入電容佔總損耗功率的 23%，此三大主要元件佔總損耗功率的 93%，若要有效的提昇效率必須從此三大主要元件著手：(1).功率電晶體上橋的輸入電容值（C_{iss}）越小越好，由式（27）可得知，若要計算切換損耗必先求出I_G，計算式如下：

$$R_G=t_f/2.2\times C_{iss} \quad (47)$$

$$R_G=7.3\times10^{-9}/2.2\times1.01\times10^{-9}=3.285\Omega$$

又$R_G=V_{GS}/I_G$所以$I_G=5/3.285=1.522A$，求出I_G之後代入式(27)可計算出切換損耗為 1.176 瓦，若加入零電壓之軟性切換模式，應用元件如圖 3(b)中之 D2、C1、C2，利用 LC 共振原理，當V_{DS}等於零時切換開關，將切換損耗降至最低，其損耗由 1.176 瓦降至 0.01 瓦。下橋的$R_{ds(on)}$值要越小越好，因此由改善前之兩並方式改變成三個並聯，新增元件如圖 3(b)中之 Q5，因並聯可以讓$R_{ds(on)}$值變小及熱阻變小，由式（28）可得知增加 Q5，可以讓下橋的傳導損耗由 2.088 瓦降至 1.05 瓦。經設計最佳化之後，功率電晶體的總損耗由 3.912 瓦降至 1.79 瓦，提昇整體效率達 3.53%。(2).電感線圈改為扁平之銅線，直流阻抗由 1.5mΩ降至 1.2mΩ，銅損由 1.35 瓦降至 1.08 瓦，選擇鐵損較低的鐵心材料內鎳鐵(Ni-Fe Core)，鐵損由 0.977 瓦降至 0.58 瓦，電感

的功率損耗由 2.347 瓦降至 1.66 瓦，提昇整體效率達 1.08%。(3).電容改用高分子聚合物（Polymer）加鋁（Aluminum），目前容值最大 330uF 其 C_{ESR} 為 7mΩ，以同樣容值若 470uF 改為 330uF，則輸出電容必須由 4 個增加至 6 個，C_{ESR} 值由 2.25mΩ降至 1.167mΩ，損耗從 2.025 瓦降至 1.05 瓦，提昇整體效率達 1.59%。設計改善前後之效率分析比較，如表 1 所示，效率由 82.78%提昇至 89.46%。

表 1. 效率分析比較表

功率損耗源		改善前(W)	改善後(W)
控制晶片功率損耗		0.1	0.1
上橋功率電晶體	傳導損耗	0.439	0.439
	切換損耗	1.176	0.01
	驅動損耗	0.018	0.018
	輸出電荷損耗	0.024	0.024
下橋功率電晶體	傳導損耗	2.088	1.05
	切換損耗	0.00088	0.0001
	驅動損耗	0.078	0.117
	輸出電荷損耗	0.088	0.132
電感功率損耗		2.327	1.66
輸出入電容功率損耗		2.025	1.05
印刷電路板佈線功率損耗		0.56	0.455
總功率損耗		8.92388	5.055
效率		**82.78%**	**89.46%**

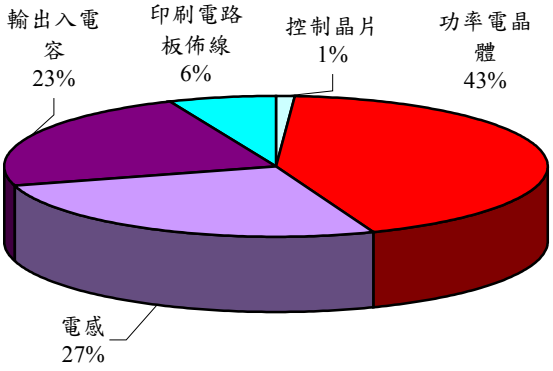


圖 7. 功率損耗分佈之百分比

4.3 印刷電路板佈線與散熱之設計

印刷電路板佈線時必須注意，電源層路徑越短越寬大其壓降就越小，由 $R_{dc,PCB}=\rho\times L/A$ 可得知，印刷電路板佈線的阻抗（$R_{dc,PCB}$）是與走線長度（L）成正比，與銅鉑的截面積（A）成反比，連接層與層之間的導通孔，數量要越多越好，若每一個導通孔可流過的電流為 1 安培，負載電流為 100 安培，就須要 100 個導通孔，導通孔的另一功能是可以排出熱氣，有幫助散熱的效果。

散熱材質若兩端存在溫度差異，則熱流將由高溫端流向低溫端，單位時間內之能量熱流：

$$P_{Loss}=\lambda A\Delta T/d \qquad (48)$$

其中 P_{Loss} 為功率損耗，λ 為導熱系數（thermal conductivity），A 為材質之截面積（m^2），d 為材質之厚度（m）。通常熱必須流經許多不同材質，每一材質有不同之導熱系數、面積及厚度，圖 8(a)所示為穩態下包含散熱片之多層結構的熱流及熱阻；以熱阻表示之等效電路如圖 8(b)所示，建立一矽元件到周圍熱傳導路徑之模式，由元件接面（junction）到周圍（ambient）之總熱阻為：

$$R_{\theta ja}=R_{\theta jc}+R_{\theta cs}+R_{\theta sa} \qquad (49)$$

其中 $R_{\theta jc}$ 為接面到外殼之熱阻，$R_{\theta cs}$ 為外殼到散熱片之熱阻，$R_{\theta sa}$ 為散熱片到周圍之熱阻，一般接面到周圍之熱阻 $R_{\theta ja}$ 設計必須小於 1℃/W。假設功率損耗為 P_{Loss}，則接面之溫度為：

$$T_j=P_{Loss}\left(R_{\theta jc}+R_{\theta cs}+R_{\theta sa}\right)+T_a \qquad (50)$$

$$R_{\theta ja}=\frac{T_{j,\max}-T_{a,\max}}{P_{Loss}} \qquad (51)$$

其中 T_a 為周圍溫度，$T_{a,\max}$ 為周圍溫度之最大值，$T_{j,\max}$ 為接面溫度之最大值。

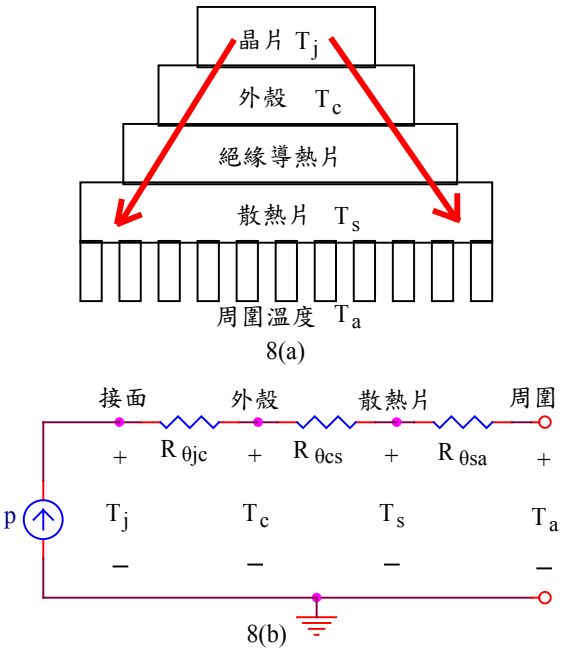


圖 8. (a)包含散熱片之多層結構的熱流及熱阻；(b)熱阻等效電路

5. 模擬與量測

負載電流為 80 安培時，PSpice 模擬效率改善前為 83.84%，改善後為 90.04%，如圖 9 所示，儀器設備量測結果效率改善前為 82.24%，改善後為 89.02%，誤差值為 1.02~1.6%。量測方式是外加電子負載，從 10 安培增加至 100 安培，記錄每增加 10 安培的輸出入電壓及電流，即可算出電流與效率的關係，改善前後用同一方式量測，結果如圖 11 所示，其傳輸線會有損耗（Cable losses），且負載越大損耗越大，所以與 PSpice 模擬結果會有誤差。

功率損耗量測分析，是借用立肯科技 PMA2 功率分析軟體，圖 10 所示之 CH1 是上橋之V_{DS}，是用差動探測器及差動探棒，直接量測功率晶體的洩極至源極間之電壓（V_{DS}），CH2 是電感電流，用 150 安培的電流探棒直接量測流過電感的電流，CH3 是上橋之V_{GS}，P_w是立肯科技 PMA2 功率分析軟體，所運算的結果功率損耗之平均值為 1.87 瓦，下橋之功率損耗平均值為 2.6 瓦。

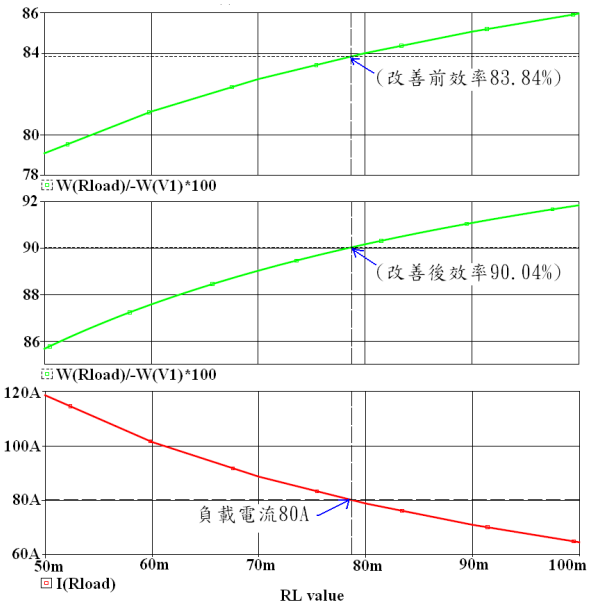


圖 9. PSpice 之效率模擬結果

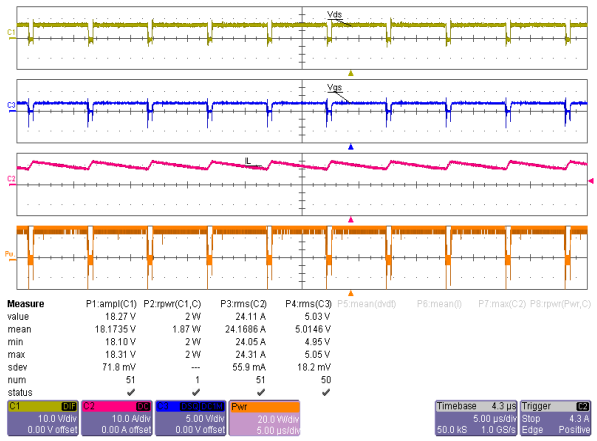


圖 10. 上橋之功率損耗示波器量測平均值 1.87W

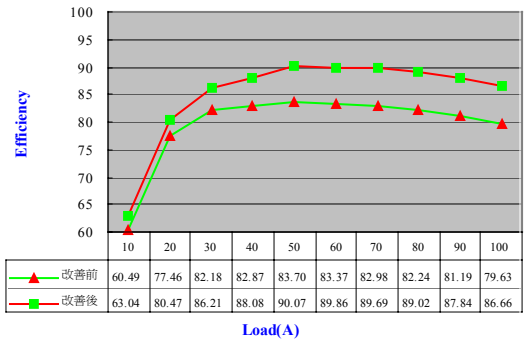


圖 11. 改善前後之效率量測結果

6. 結論

本論文所提出之設計分析及其改善方案，在負載電流為 80 安培時，可將效率由 82.78%提昇至 89.46%，功率損耗由 22 瓦降至 12 瓦，以筆記型電腦而言，負載電流為 80 安培時電壓為 1.3 伏特，則消耗功率為 104 瓦，加上功率損耗 22 瓦及其他系統消耗 40 瓦，整個系統總共消耗 166 瓦，故須使用 180 瓦的電源穩壓器，若功率損耗降至 12 瓦，整個系統總共消耗 156 瓦，可使用 150 瓦的電源穩壓器，150 瓦與 180 瓦的價差約 10 美元。以 10 美元選擇較好的零件來提昇效率應足足有餘，而且具有散熱成本與所需之空間減少的優勢，這對追求輕薄短小的可攜式電子產品而言，是非常的重要。

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Battery Equalization Using Bi-direction Cûk Converters in DCVM Operation
利用電容電壓不連續模式的邱克雙向鋰離子電池等化器

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Abstract – A systematic approach to the analysis and design of a bi-directional Cûk converter for the cell voltage balancing control of a series connected battery strings is presented in this paper. The proposed individual cell equalizers (ICE) are designed to operate at discontinuous-capacitor-voltage mode (DCVM) to achieve the zero-voltage turn-off switching (ZVS) for reducing the switching loss of the bi-directional DC/DC converters. Simulation and experimental results show that the proposed battery equalization scheme can not only enhance the bi-directional battery equalization performance, but also can reduce the switching loss during the equalization period. The switching loss is significantly reduced from MOSFETs by about 52.8% and the equalization efficiency can be improved to 68~72% by the proposed DCVM ZVS battery equalizer under the specified cell equalization process.

I. INTRODUCTION

Because the voltage in a single battery cell is inherently low, battery cells connected in series are usually employed in many practical applications such as electric vehicles (EV), hybrid electric vehicles (HEV), telecom battery energy system. Imbalanced cell voltage within a series string can be attributed to the differences in cell internal resistance, imbalanced state-of-charge (SOC) between cells, degradation and the ambient temperature gradients of the battery pack during charging and discharging. Voltage monitoring and current diverting equalization schemes and battery management system (BMS) have been presented in the literature to prevent imbalances during charging and discharging in series connected battery cells [1-3].

The integrated individual cell equalization schemes (ICE) for battery pack applications have been proposed to equalize battery strings [3-6]. The bidirectional battery equalization scheme has many advantages such as higher equalization efficiency for non-dissipative current diverters, and a modular design approach [3]. The disadvantage of this equalization scheme is that the stored energy in the inductor is transferred to the weaker cell only in the (1-D)Ts duty cycle. The equalization time and efficiency of this equalization scheme are therefore poor for practical battery equalization applications in the smart battery management system (SBMS) [6-11]. Battery equalization control should be implemented to restrict the charge-discharge current to the allowable cell limitations in the battery string. Cell balancing control is designed to obtain the maximum usable capacity from the battery string. Because battery string charging and discharging are limited by any single cell reaching its end-of-charge voltage and low voltage threshold. Cell balancing algorithms search to efficiently remove energy from a strong cell and transfer that energy into a weak one until the cell voltage is equalized to the same level across all cells. This enables additional charging capacity for the entire battery string [4]. Complete cell voltage balancing is performed using a bi-directional dc-dc converter based on the Cûk converter [9,11]. This unit can be designed to operate at the DICM or DCVM to obtain soft switching in MOSFET switches [11-14].

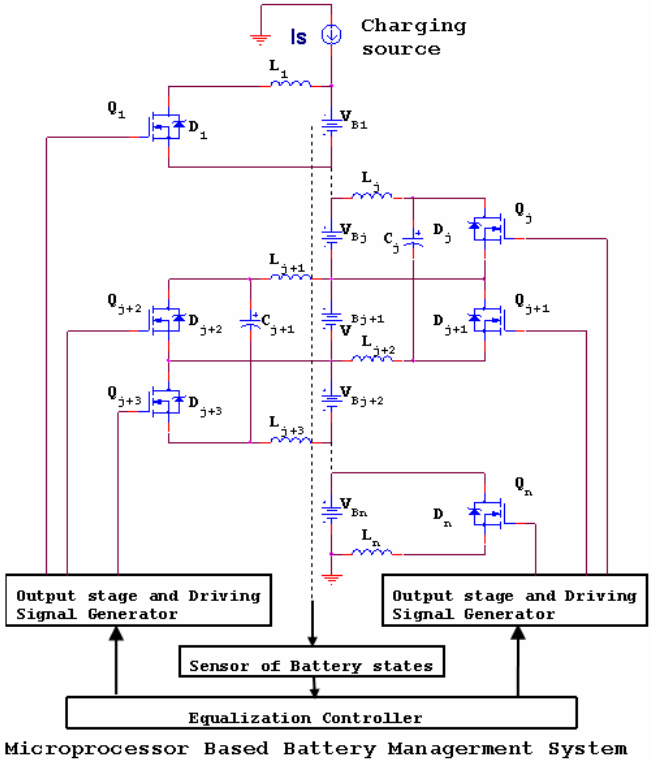


Fig. 1 Studied battery charging system with ICE and microprocessor based BMS

II. TOPOLOGY DESCRIPTIONS

The studied battery charging system with the proposed ICEs and the microprocessor based BMS is shown in fig. 1. The system is composed of N battery cells and (N-1) ICEs. The jth module is comprised of two inductors L_j and L_{j+1}, an energy transfer capacitor C_j, and two power MOSFETs with body diodes as the battery cell-balancing switches. The single module of ICE is redrawn and simplified in fig. 2. The cell voltage balancing control algorithm for this equalization

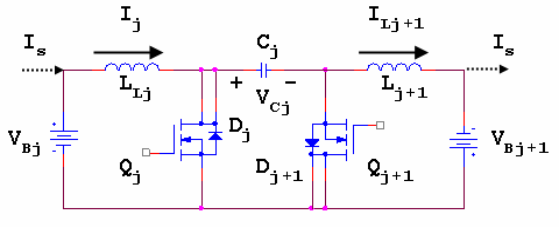


Fig. 2 Single stage of the proposed ICE

scheme is instructed by a microprocessor based BMS. The energy between the adjoining battery cells is transformed through the energy transferring capacitor for cell voltage balancing. The energy transfer direction is determined by the cell voltage and/or SOC difference in the battery string and conduction from the controlled power MOSFET switches [9]. The two adjoining cells voltages are balanced by switching the MOSFETs on/off according to the PWM signals generated from the BMS. The PWM signals correspond to the respective cell voltage through the microprocessor based BMS, which controls the switches Q_j and Q_{j+1}. The initial capacitor voltage V_{Cj} equals $V_{Bj}+V_{Bj+1}$. For example, the PWM control signal turns on/off the Q_j to transfer some of the stronger cell voltage, V_{Bj}, to the weak cell, V_{Bj+1}. The stronger cell energy is transferred from cell V_{Bj} to cell V_{Bj+1}. Conversely, if cell V_{Bj+1} has stronger than the weaker cell V_{Bj}, the energy is transferred from cell V_{Bj+1} to cell V_{Bj} by controlling the Q_{j+1}. The equalization process will be uninterrupted until the voltages in the remaining cells are all equalized to the same end-of-charge or end-of-discharge level. The proposed bidirectional battery equalizer is designed to operate at DCVM for achieving the zero voltage switching to reduce the MOSFETs switching losses. The DCVM operation principle of proposed ICE is described as following section.

III. CIRCUIT ANALYSIS

The inductors L_1 and L_2 are assumed as large as enough to operate in CICM. In addition, the capacitor is also sufficient small so that it is fully discharged during the switching period. Where T_s is the converter switching period, the detail equivalent circuit of the proposed battery equalization schemes are shown in figs. 3 and 4 during the various time intervals for the different cell voltage, $V_{Bj} > V_{Bj+1}$ and $V_{Bj} < V_{Bj+1}$, respectively. The corresponding typical switching waveforms for various operating states are depicted in figs. 5 (a) and 5 (b), respectively. Referring to the capacitor voltage waveform and the dynamic state equations of the ICE in fig. 5 (a) for $V_{Bj} > V_{Bj+1}$ can be explained as follows:

Assumed the capacitor voltage υ_{cj} has reached maximum before the main switch Q_j is turned-on. From the duty cycle 0 to D_1T_s, the switch Q_j is turned-on and diode D_{j+1} is turned-off at the beginning of a switching cycle t = 0 shown as fig. 3 (a). The inductor L_j is charged by input voltage V_{Bj} and the current i_{j+1} thought inductor L_{j+1} is discharged by capacitor C_j. The energy stored in C_j is completely transferred to the cell V_{Bj+1}, and υ_{cj} becomes to zero at $t = D_1T_s$. From the duty cycle D_1T_s to DT_s, the switch Q_{j+1} had still conducted and D_{j+1} starts conducting to allow i_{j+1} to flow since υ_{cj} is equal to zero during this interval shown as fig. 3 (b), V_{Bj} continuous to

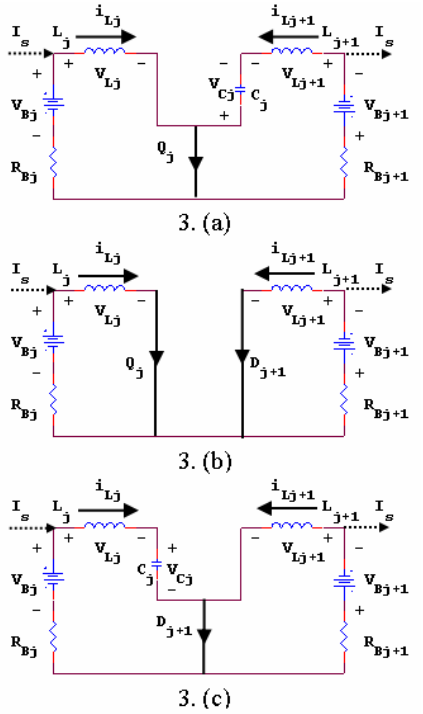


Fig. 3 Equivalent circuit of DCVM for $V_{Bj} > V_{Bj+1}$
(a) Q_j turn-on, (b) Q_j turn-on and $V_{Cj} = 0$, (c) Q_j turn-off and D_{j+1} turn-on

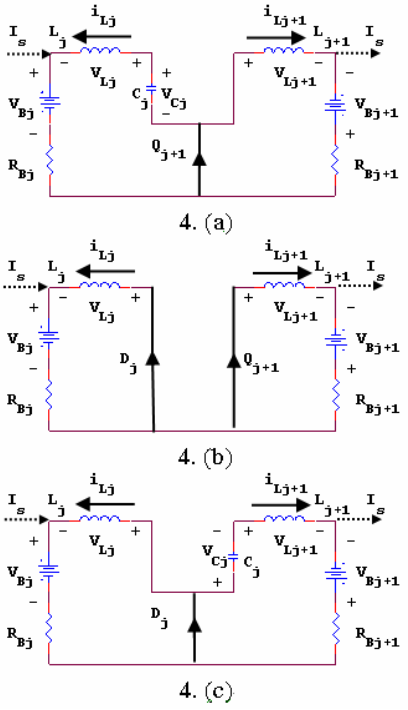
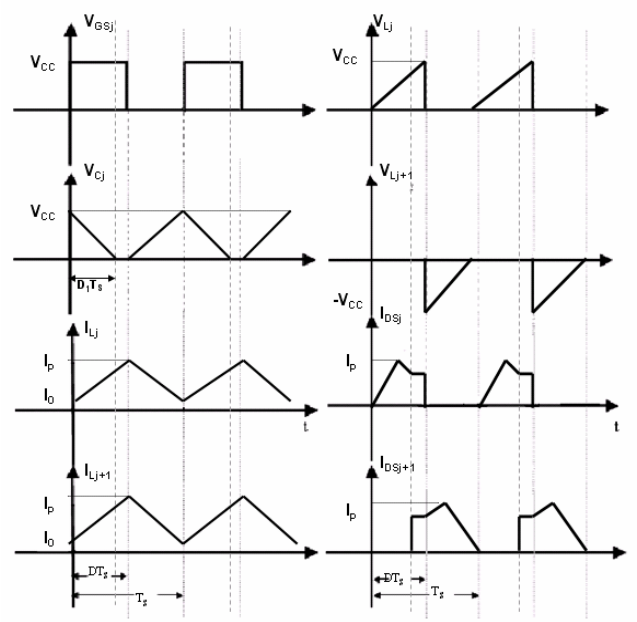
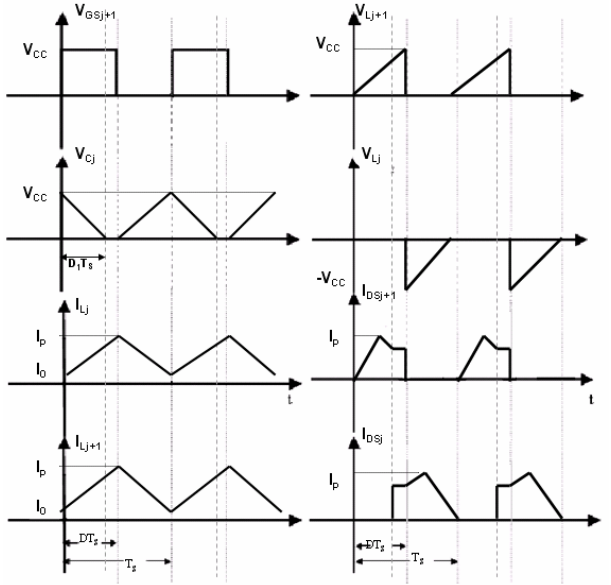


Fig. 4 Equivalent circuit of DCVM for $V_{Bj} < V_{Bj+1}$
(a) Q_{j+1} turn-on, (b) Q_{j+1} turn-on and $V_{Cj} = 0$, (c) Q_{j+1} turn-off and D_j turn-on



5. (a)



5. (b)

Fig. 5 Typical switching waveforms of ICE_j for (a) $V_{Bj}>V_{Bj+1}$, (b) $V_{Bj}<V_{Bj+1}$

charge L_j and the stored energy in L_{j+1} is still discharged to V_{Bj+1} for cell voltage balancing control. From duty cycle DT_s to T_s, the switch Q_j is turned off at $t = DT_s$, and D_{j+1} is still conducted for cell voltage balancing. Capacitor C_j is charged from zero voltage by i_j .The capacitor voltage υ_{cj} reaches maximum value at $t = T_s$ as shown in fig. 3 (c). The proposed ICE has more than one stage compare with a Cûk converter in CICM which both the MOSFET switch Q_j and flywheel diode D_{j+1} are conducting as shown in fig. 3(b) introduced in the DCVM operation. The compact state equation [15] for mentioned descriptions of the three-states can be derived as:

$$\begin{bmatrix} \frac{di_j}{dt} \\ \frac{di_{j+1}}{dt} \\ \frac{dV_C}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_{B_j}}{L_j} & 0 & \frac{-(1-u)(\frac{1}{2}-u)\times 2}{L_j} \\ 0 & -\frac{R_{B_{j+1}}}{L_{j+1}} & \frac{2u(u-\frac{1}{2})}{L_{j+1}} \\ \frac{2(1-u)(\frac{1}{2}-u)}{C_j} & \frac{-2u(u-\frac{1}{2})}{C_j} & 0 \end{bmatrix} \begin{bmatrix} i_j \\ i_{j+1} \\ V_C \end{bmatrix} + \begin{bmatrix} \frac{V_{B_j}+I_sR_{B_j}}{L_j} \\ \frac{V_{B_{j+1}}+I_sR_{B_{j+1}}}{L_{j+1}} \\ 0 \end{bmatrix} \tag{1}$$

where u is a tri-state switching control variable, it is suggested that u = 1 (HIGH state) denoted Q_j turn-on and D_{j+1} turn-off shown as fig. 3 (a), u = 0 (LOW state) denoted Q_j turn-off and D_{j+1} turn-on shown as fig. 3 (c), and u = 0.5 (FLOATING state) denoted Q_j and D_{j+1} are both turn-on and $\upsilon_{cj} = 0$ shown as fig. 3 (b). The internal resistance of battery cell R_B is neglected for simplified the steady state circuit analysis, and the charging/discharging source effect is absent in the principle operation of the converter.

Assume L_j and L_{j+1} are enough large, the ripples in i_j and i_{j+1} are small. Denote the time average value of i_j and i_{j+1} as I_j and I_{j+1}, respectively. From fig. 5(a), we can derive the conditions of DCVM operation as follows:

The instantaneous capacitor voltage in the full duty cycle of the DCVM Cûk converter can be expressed as:

$$v_{Cj} = \begin{cases} \frac{I_j(1-D)T_S - I_{j+1}t}{C_j}, & \text{for } 0 < t < D_1T_S \\ 0, & \text{for } D_1T_S < t < DT_S \\ \frac{I_j(t-DT_S)}{C_j}, & \text{for } DT_S < t < T_S \end{cases} \tag{2}$$

The power MOSFETs of the modified QRZVS battery equalizer are turned off at the zero current. The sub-duty ratio D_1 in terms of the duty ratio D can be governed as:

$$D_1 = (1-D)\frac{I_j}{I_{j+1}} \tag{3}$$

The time-average of voltages of υ_{cj} and υ_{Dj+1}, denoted as V_{cj} and V_{Dj+1}, respectively. It can be determined from (2) as

$$V_{cj} = \frac{T_s}{2C_j} I_j (1-D)(1-D+D_1) \tag{4}$$

$$V_{Dj+1} = -\frac{T_s}{2C_j} I_j (1-D) D_1 \tag{5}$$

Therefore, the terminal voltages of the battery cells and the voltage conversion ratio are

$$V_{Bj+1} = -V_{Dj+1} = \frac{T_s}{2C_j} I_j (1-D) D_1 \tag{6}$$

$$V_{Bj} = V_{Dj+1} + V_{Cj} = \frac{Ts}{2C_j} I_j (1-D)^2 \tag{7}$$

$$\frac{V_{Bj+1}}{V_{Bj}} = \frac{D_1}{1-D} \tag{8}$$

Combining (3), (6) and substituted into (8) to obtain

$$I_j = \frac{2 f_s C_j V_{Bj}}{(1-D)^2} \tag{9}$$

$$D_1 = \sqrt{2 f_s C_j \frac{V_{Bj+1}}{I_{j+1}}} \tag{10}$$

To operate the proposed ICE in DCVM, the inequality should be satisfied, or equivalent

$$D \geq \sqrt{2 f_s C_j \frac{V_{Bj+1}}{I_{j+1}}} \tag{11}$$

$$L_j \geq \frac{V_{Bj+1}(1-D)^2}{2 D f_S I_{j+1}} \tag{12}$$

$$L_{j+1} \geq \frac{V_{Bj+1}(1-D)}{2 f_S I_{j+1}} \tag{13}$$

The switching boundary surface of the converter to operate between DCVM and continuous-capacitor-voltage mode (CCVM) is depicted in fig.6.

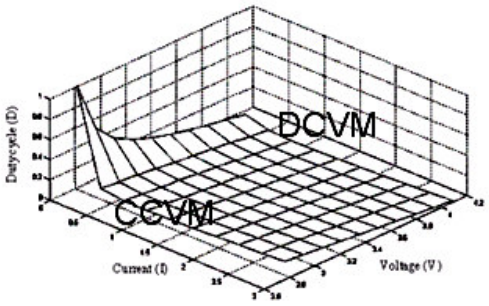


Fig. 6 Switching boundary surface between DCVM and CCVM

However, the proposed converter may not operate in DCVM when V_{Bj} is small due to the cell voltages are not a constant dc voltage and depending on the equalization current of ICE. The inequality (11), (12) and (13) are used to design the proposed ICE that can be guaranteed to operate in DCVM [10].

IV. SIMULATION AND EXPERIMENT RESULTS

In order to validate the performance of the proposed bi-directional battery equalizer, a Matlab/Simulink simulation and experiment are carried out for a three cells battery modular (N=3) with the two proposed battery equalizers (2ICEs). Matlab/Simulink simulation was performed for mathematical model of ICEs. A three-modular battery stack with two fundamental equalization schemes are used to verify the analysis results mentioned above. The simply signal flow graph is defined using for Matlab/Simulink simulation to the proposed ICE Matlab/Simulink model for three battery cell. The ICE_1 (composes of L_1, L_2, C_1, Q_1 and Q_2) and the ICE_2 (composes of L_3, L_4, C_2, Q_3 and Q_4) were comprised the block diagram shown in fig. 7. The battery storage elements were simply assumed to battery charge/discharge model, which established by a battery charge/discharge profile with equivalent series resistor (ESR) in the library of the Matlab/simulink block model. The battery initial voltages, uncoupled inductors and energy transferring capacitor were set V_{B1}=4.0(V), V_{B2}=3.9(V), V_{B3}=3.6(V), battery model with 0.01Ω ESR, L_1=L_2=L_3=L_4=230 μH and C_1=C_2=0.66 μF, respectively. The switching frequency was 16.67 KHz and duty ratio D=0.53 for both $V_{B1}>V_{B2}>V_{B3}$ and $V_{B1}<V_{B2}<V_{B3}$ to ensure the proposed bi-directional dc-to-dc converter can be designed to operate in DCVM. It can obtain a zero voltage switching (ZVS) to reduce the MOSFET switching loss in the proposed ICEs.

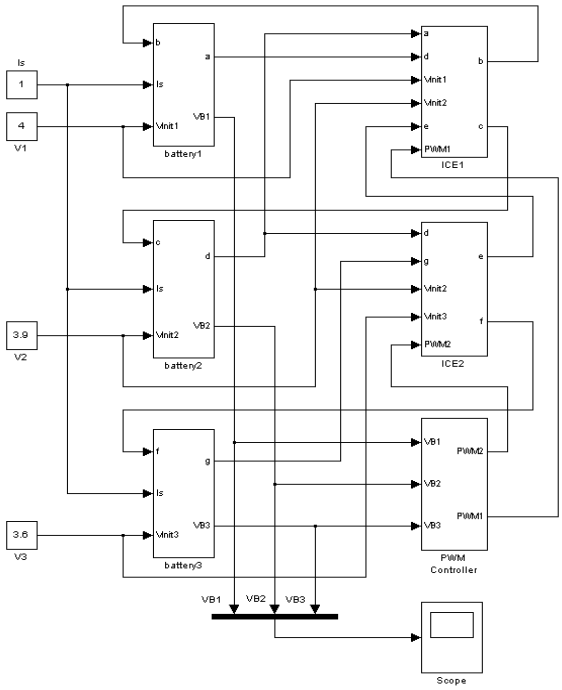


Fig. 7 Configuration of MATLAB/SimuLink model

Fig.8 shows the simulating voltages and currents of the capacitor and inductor in ICE1, respectively. The MOSFET control signal V_{gs} and the corresponding drain-source voltage V_T for $V_{B1}>V_{B2}>V_{B3}$ are shown as fig. 9 (a) and 9 (c). The simulation results of the cell voltage trajectories under floating state, added 1A charging and discharging current states of the proposed battery equalizer are illustrated in the fig. 10 (a), (c) and (e), respectively. The cell balancing process is stopping when cell voltage equalized to the same end-of-charge or end-of-discharge state.

An experimental installation of a three-modular lithium-ion battery stack with the proposed equalization scheme is used to verify the equalization performance of the three cells battery stack with the proposed ICEs. The driving signals for the equalization schemes are controlled using a microprocessor based battery management system according to each cell voltages. The driving signals are constructed using a logical

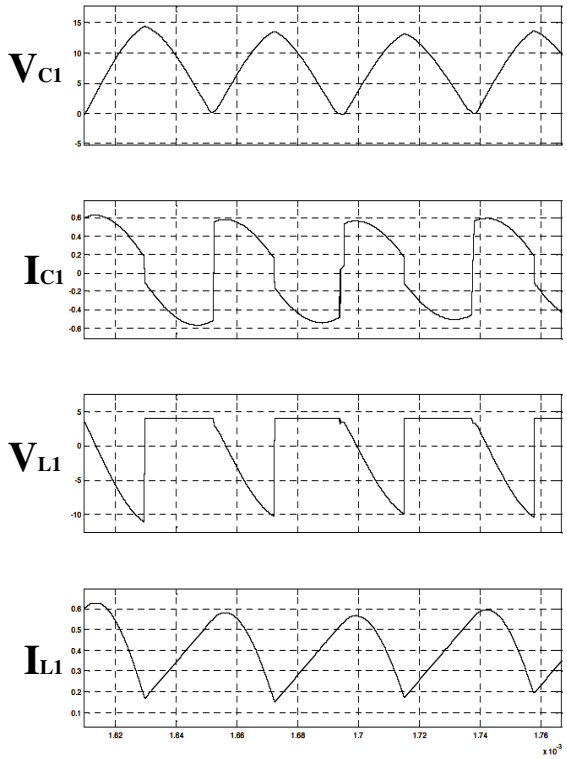
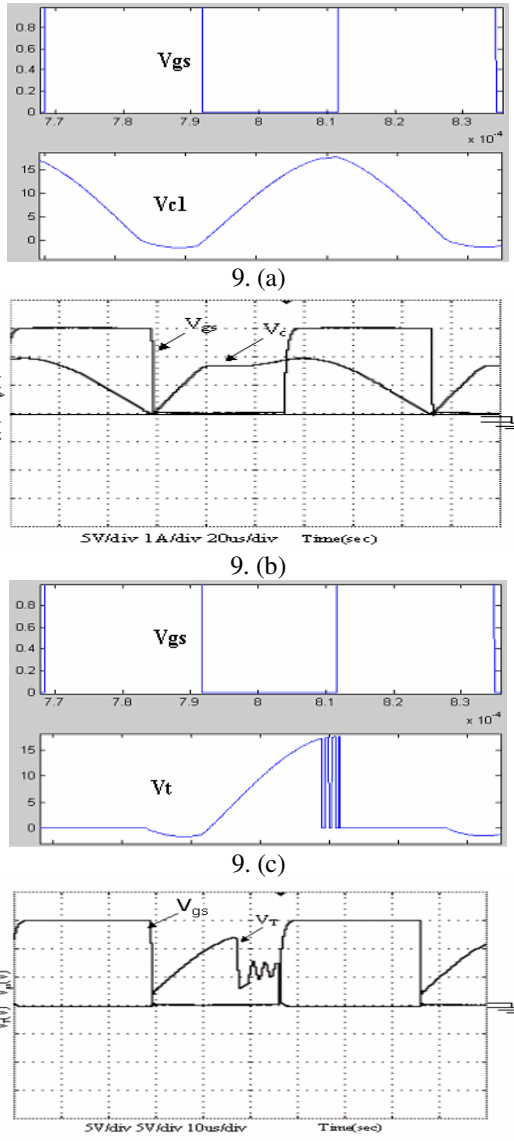


Fig. 8 Simulation results

switching algorithm, and instructed by microprocessor of 8052. Cell voltages were balanced within 0.0196 (V), due to the hardware resolution limited by analog to digital converter (ADC0804). The voltage balancing process is stopped while the BMS send an executable command to cut-off the MOSFET. The experimental parameters of the batteries and the designed ICEs are list as following: The initial voltages of the three lithium-ion batteries MRL/ITRT 10AH are 4.0(V), 3.5(V), and 3.0(V), respectively. The inductances are L_1~L_4=230 μH, C_1=C_2=0.66 μF. The switching frequency and the duty ratio of the battery equalizer are 16.67 kHz and 0.53, respectively. Figs. 9 (b) and 9 (d) show the measured voltage of V_{gs}, V_c, and MOSFET drain-source voltage V_T, respectively. The transient oscillations in the drain-source voltage of MOSFET due to the fast switching transient effect, it can be suppressed by a well designed turned-off DRC snubber circuits in the switching devices. Figs 10 (b), (d) and (f) show the experimental results of the cell voltage trajectories under floating, added 1A charging and discharging current states of the proposed battery equalizers. Therefore, the equalization method can balance the all adjoin cell voltages of the battery string to the same voltage level. Consequently, each cell can be simultaneously charged to the end-of-charge voltage. And battery string would be increased in the total charging capacity.

Fig. 12 shows the equalization efficiency of ICE under various operating modes for the specified equalization processing. Fig. 11 shows the waveform and the corresponding FFT spectrum of MOSFET switching loss P_T (= $V_T * i_T$). Table 1 shows the differential designed results and performance comparison of the ICEs operated at CICM, DICM and DCVM under the specified equalization procession and equalizing current, respectively. Several observation of the proposed battery equalizer can be summarized as follows:

- The power MOSFETs of the proposed battery equalizer are turned off in the zero voltage state. The total switching loss of the MOSFETs in the battery equalizer can be significantly reduced from 33.5% to 52.8% compared with the same equalizer operated at CICM (D=0.53).
- The peak current stress of the MOSFET is significantly reduced compared with the equalizer designed to operate at DICM (D=0.5).
- The average equalization efficiency can be improved from 52% to 68% compared with the equalizer operated at CICM. The maximum equalization efficiency can achieved to 72% for this designed test sample.



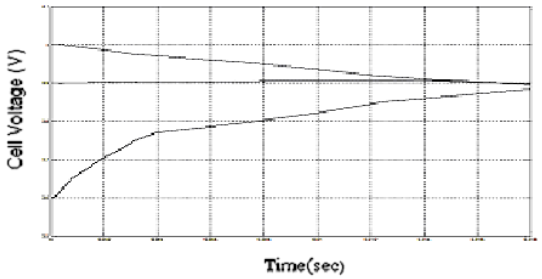
9. (a)

9. (b)

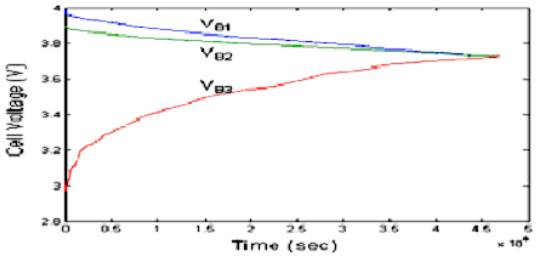
9. (c)

9. (d)

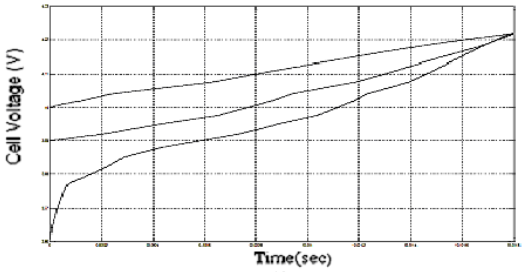
Fig. 9 Simulation and experimental results of MOSFET control signal V_{gs} and drain-source voltage V_T for V_{B1}>V_{B2}>V_{B3}, (a)(c) Simulations, (b)(d) Experiments



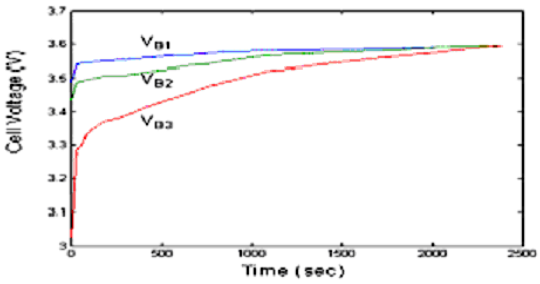
10. (a) Simulation



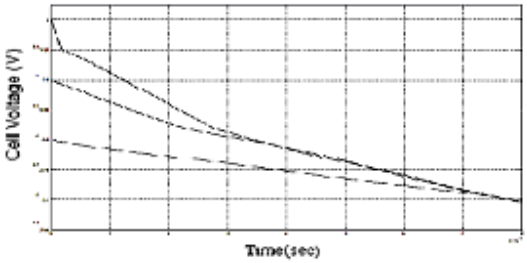
10. (b) Experiment



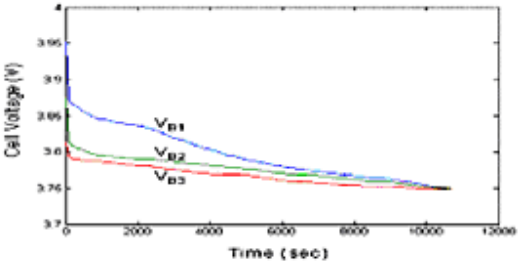
10. (c) Simulation



10. (d) Experiment



10. (e) Simulation



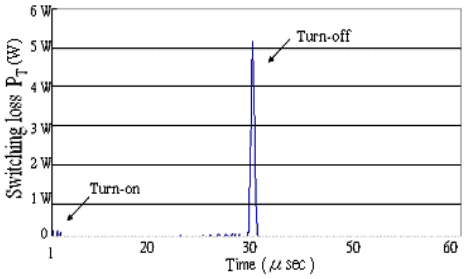
10. (f) Experiment

Fig. 10 Simulation and experimental results of cell voltage trajectories for $V_{B1}>V_{B2}>V_{B3}$, (a) (b) static state, (c) (d) added 1A charging current, (e) (f) added 1A discharging current

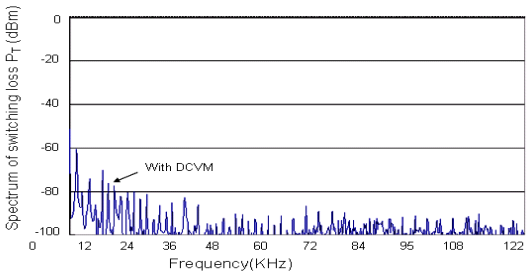
The DCVM ZVS Cûk converter has spent slight more equalization time to balance the cell voltage to equal end-of-charge state. Therefore, it is need to design an equalization controller to speed up the equalization processing for a smart battery management system.

V. CONCLUSION

The proposed ICE for the ZVS soft-switching of DC/DC converter has been developed. It implements the zero-voltage-switching technique and greatly reduces the power loss. The proposed ICE's MOSFET is turned off and body diode is turned on at zero voltage of capacitor in DCVM. Capacitor voltage approaches zero then body diode of MOSFET is turned on until the capacitor energy completely transfers to the weaker cell of batteries. Therefore, the MOSFET switching loss is reduced by about 33% more than that is in CICM. The MOSFET switching power and the corresponding FFT frequency spectrums of the proposed battery equalizer in the DVCM are less than that is in the DICM and CICM. Energy harmonic spectrum concentrates in the low frequency for CICM, and disperses form low to higher frequency in DCVM. Hence, the high frequency EMI emission is improved in a series connected battery energy system with DCVM designed ICEs.



(a)



(b)

Fig. 11 (a) Waveform and, (b) FFT spectrum of MOSFET switching power loss

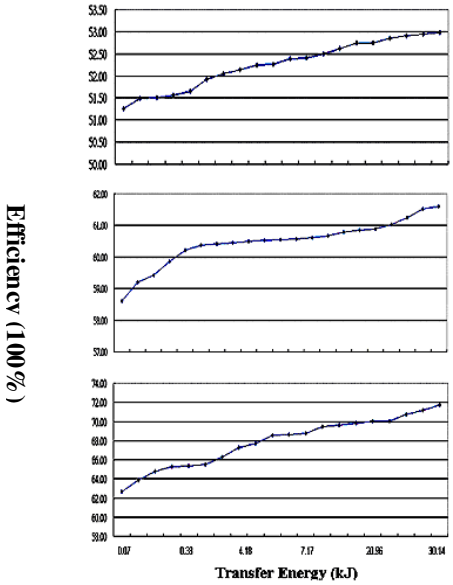


Fig. 12 Equalization efficiency of ICE under various operating modes

TABLE 1 COMPARISON BETWEEN CONTINUOUS AND DISCONTINUOUS MODES

	CICM	DICM	DCVM
Inductor (L_j)	99.1u	99.1u	231.2u
Inductor (L_{j+1})	100.7u	100.7u	231.2u
Capacitor(C_j)	470u	470u	0.66u
Switching frequency(f_s)	18.1K	16.67K	16.67K
Duty cycle (D)	0.53	0.5	0.5
Boundary condition for CICM and DICM	$L_{j+1} \cdot f_s > \frac{V_{i+1}(1-D)}{2I_{j+1}}$ $L_j \cdot f_s > \frac{(1-D)^2 \cdot V_{i+1}}{2D \cdot I_{j+1}}$	$L_{j+1} \cdot f_s < \frac{V_{i+1}(1-D)}{2I_{j+1}}$ $L_j \cdot f_s < \frac{(1-D)^2 \cdot V_{i+1}}{2D \cdot I_{j+1}}$	0.53
Boundary condition for CICM and DMV	$D < \sqrt{2 \cdot \frac{V_{i+1}}{I_{j+1}} f_s C_j}$		$D > \sqrt{2 \cdot \frac{V_{i+1}}{I_{j+1}} f_s C_j}$
Voltage stress	Low	Low	High
Current stress	Low	High	Low
Switching characteristic	*	Soft turn-on	Soft turn-off
Most appropriate applications	*	Low current, high voltage	High current, low voltage

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