Signal Integrity/EMC Pro Tune Up 2007

Pro Tune Up 2007 is a hit list of the critical techniques which must be mastered for consistent SI/EMC success using modern technologies like PCI, PCI Express, USB, USB 2.0, LVDS, and a number of other popular clocked buss and SerDes interfaces. The class is presented in a single day and includes hands on labs. Lab computers & software tools are provided.

We perform a quick review (about 2 hours) of JumpStart 3 information so a student could take this as a first class. Students taking this as a first class must pay special attention to the JumpStart 3 pre class homework video and accept that fact that they will be jumping aboard a fast train that only slows to about 20 mph on the way by.

Who should attend this class?

Any Electrical Engineer, CAD Layout Designer, or EMI GURU who is tired of playing "Whack a Mole" would find this class extremely useful. For those of you who have not attended one of my previous classes, "Whack a Mole" is an arcade game that kids love. There are nine holes and a worm like creature ...a mole ...sticks its head up and the kids whack it with a plastic sledge hammer. After a few seconds the "mole" pops up in another location. The faster the kids whack the mole, the faster it moves to a new location. Kids love the game, but from a high speed design standpoint, it becomes an infuriating game quite rapidly. This class will help you permanently end the EMI version of the "Whack A Mole" game.

The first part of the class is spent reviewing the critical aspects of high speed design and layout which can only be ignored at your peril. These include board stack-up, power delivery, and critical high speed routing requirements. We specifically examine the key mechanisms that disrupt Signal Integrity and generate radiated EMI. This is a fast forward version of JumpStart 3 leaving out the whole notion of budgeting etc.

The second part of that class is spent reviewing popular interconnect mechanisms and how poor implementation can lead to unexpected performance and certification issues. These include analogue digital interfaces on a single board, differential and pseudo differential interfaces like LVDS, PCI Express, USB and USB 2.0. We also cover single ended clocked busses like CPU-SDRAM and PCI. We try to clarify how they work from a Signal Integrity and radiated EMI stand point. We specifically address the issues of common termination and topology methods like using a single resistor in a memory data line or using "T" topologies in address and clock lines. Once you understand how they work and common mistakes, it is much easier to be consistently successful in their implementation.

The third part of the class addresses the issue of going off board through connectors and cables. Whether the signal is on the board on traversing a cable, the requirements for Signal Integrity and EMC are the same.

The fourth part of the class specifically addresses the hit list of checks we must make to prevent radiated EMI due to poor layout practice. There are currently tools that are available to mere mortals to make these checks. You just need to understand what your are looking for. These checks are something that every engineer, EMI Guru, and PCB layout designer should have down cold.

Topics specifically covered in class:

1. **Radiated Emission Sources** Where does EMI come from? Why is it so hard to pass FCC & CISPR tests? Why does filtering or shielding one area result in shifting the radiation source to another area?

2. **The effect of a VIA and routing layer choices on High Speed Signal Propagation**. We use via's all of the time, but what is its affect on high speed signal propagation? It depends on how and where you use it. A bad via can cause enough radiation to prevent an otherwise excellent design from passing FCC / CISPR tests. We will investigate both the safe ways and the insanely detrimental ways designers use via's.

3. **High Speed Signal Topology and Termination** Whether it is the clock, the buss, or a high speed strobe, all signals will ring and radiate if they are not properly routed and terminated. Proper topology and termination will result in solid circuits which have predictable timing margin, high manufacturing yield, low warranty return rate, and will also behave in sane manner when taken to the lab for testing. Properly designed circuits can also be markedly less expensive to manufacture.

4. **Cross Talk** Cross talk can have two nasty ramifications. First it can add noise to the signal and cause data integrity or clock integrity issues. Less well know is that fact that it can couple on to other circuits and cause enough radiated EMI that the product will not pass FCC / CISPR tests.

5. **Power** Your power delivery mechanism must be capable of supplying significant current, i.e. an Amp or more, well into the Giga Hertz region. This will require discrete capacitors and embedded capacitance working in concert to cover this extreme frequency range. A supply that is inadequate will result in both Ground Bounce and Common Mode EMI regardless of anything else you might do to the system. Since there are multiple voltages required on typical boards, one needs to understand that the criticality of the power supply is not directly related to the clock frequency of the part being supplied. We specifically address the issue of multiple power supplies.

6. **PC Board Stack-UP** It is very difficult if not impossible to achieve proper power delivery and adequate high speed routing pairs without understanding how PCB stack-up choices affect their behavior.

7. Common clocked buss topology and termination issues. Meet timing requirements in an intelligent, cost effective, and non radiating way.

8. LVDS & SerDes interconnects. We distinguish between true differential and pseudo differential circuits. We discuss how these types of circuits work and what you need to do to get predictable behavior.

9. Techniques for Managing the Analogue Digital Interface We will discuss techniques for designing boards that have "noisy digital" on one side and "low level analog" on the other side.

10. Cables & I/O There is more to this than simply installing ferrites. We will talk through a number of key issues.

11. The common hit list of checks necessary to avoid radiated EMI in an otherwise solid design. This is a must for any layout designer or engineer reviewing high speed designs.

Viewing the SIEMC JumpStart 3.0 pre-class homework video is a required prerequisite for attending the class. I need to be assure that everyone is at a common starting point for terminology, etc. You can skip the last chapter of the book which explains the in class portion of the JumpStart 3 class.

Tuition?
Tuition is $650 per student as long as the student has made a firm registration ten days in advance of the class and firm payment arrangements five business days in advance of the class. Late registration is $750.

Register on www.SIEMC.com/SIEMC_Reg.htm
More details on class on www.SIEMC.com/PTU.htm
Or simply go to www.SIEMC.com . The main page has all of the links.

This class is also available “on-site” throughout North America for groups of 10 or more students. At a cost of $5,500.

Questions:

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