Comp 526 HW2

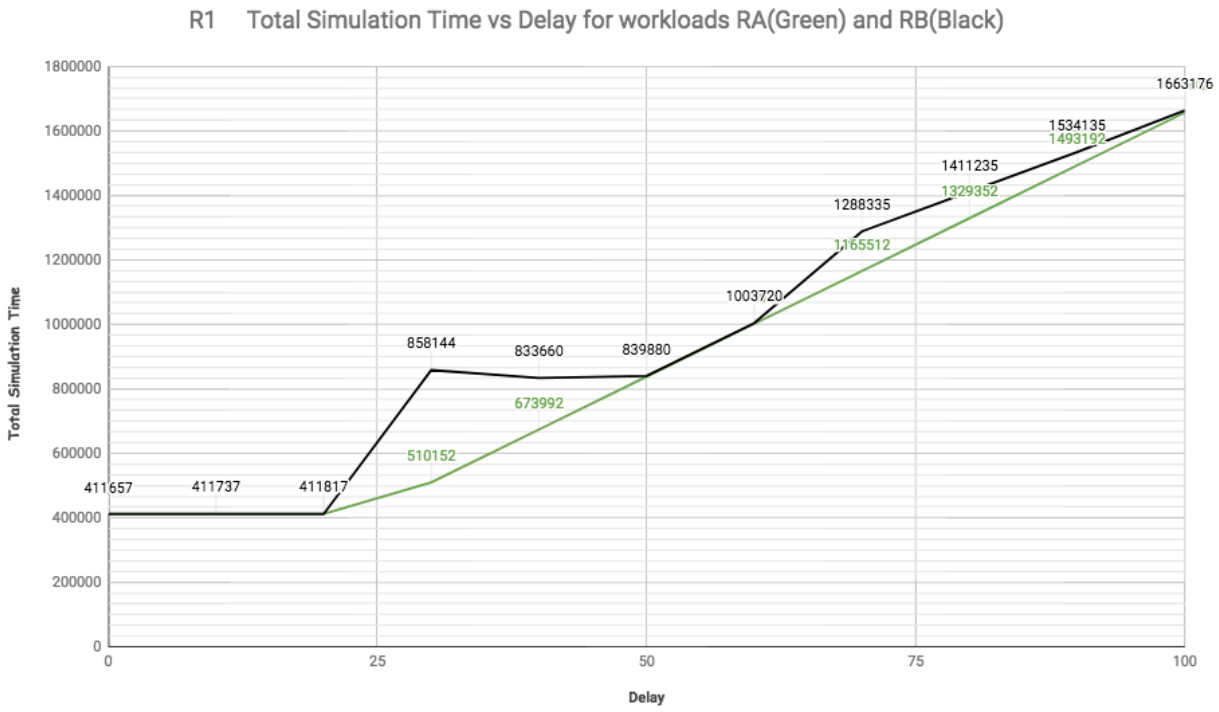
Mo Tang mt60

Data for RA/RB:

RA cpu-delay	Total Simulation Time	Total Memory Read	Total Memory Write T	Total CPU Busy Time	Total Memory Busy Ti	Total Number of Hits	Total Number of Misse	Total Number of Evict	Total Number of Write backs	
0	411657	409600	0	18432	409600	16384	2048	0	0	0
10	411737	409600	0	182272	409600	16384	2048	0	0	0
20	411817	409600	0	346112	409600	16384	2048	0	0	0
30	510152	409600	0	509952	409600	16384	2048	0	0	0
40	673992	409600	0	673792	409600	16384	2048	0	0	0
50	837832	409600	0	837632	409600	16384	2048	0	0	0
60	1001672	409600	0	1001472	409600	16384	2048	0	0	0
70	1165512	409600	0	1165312	409600	16384	2048	0	0	0
80	1329352	409600	0	1329152	409600	16384	2048	0	0	0
90	1493192	409600	0	1492992	409600	16384	2048	0	0	0
100	1657032	409600	0	1656832	409600	16384	2048	0	0	0
RB										
0	411657	409600	0	18432	409600	16384	2048	0	0	0
10	411737	409600	0	182272	409600	16384	2048	0	0	0
20	411817	409600	0	346112	409600	16384	2048	0	0	0
30	858144	819200	0	512000	819200	16384	4096	0	0	0
40	833660	819200	0	675840	819200	16384	4096	0	0	0
50	839880	819200	0	839680	819200	16384	4096	0	0	0
60	1003720	819200	0	1003520	819200	16384	4096	0	0	0
70	1288335	1228800	0	1169408	1228800	16384	6144	0	0	0
80	1411235	1228800	0	1333248	1228800	16384	6144	0	0	0
90	1534135	1228800	0	1497088	1228800	16384	6144	0	0	0
100	1663176	1638400	0	1662976	1638400	16384	8192	0	0	0

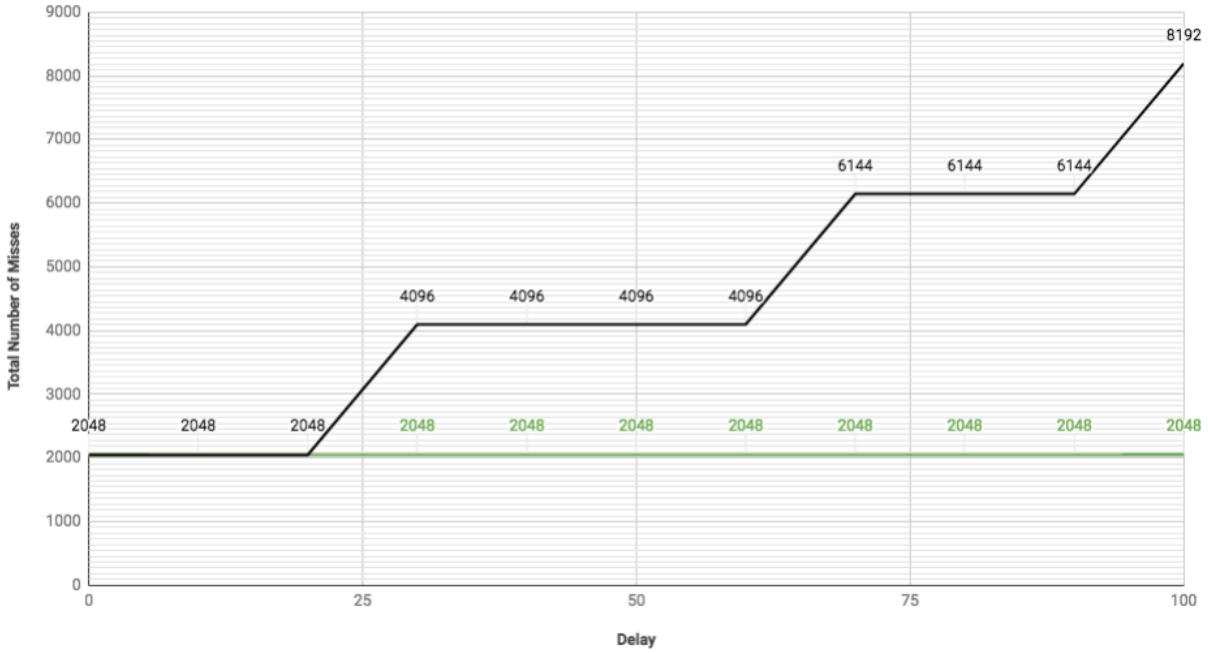
Data for WA/WB:

WA cpu-delay	Total Simulation Time	Total Memory Read	Total Memory Write T	Total CPU Busy Time	Total Memory Busy Ti	Total Number of Hits	Total Number of Misse	Total Number of Evict	Total Number of Write ba	otal number Read Misse
0	818407	409600	408800	18432	818400	16384	2048	2044	2044	0
20	818407	409600	408800	346112	818400	16384	2048	2044	2044	0
40	818791	409600	408800	673792	818400	16384	2048	2044	2044	0
60	1001672	409600	408800	1001472	818400	16384	2048	2044	2044	0
80	1329352	409600	408800	1329152	818400	16384	2048	2044	2044	0
100	1657032	409600	408800	1656832	818400	16384	2048	2044	2044	0
120	1984712	409600	408800	1984512	818400	16384	2048	2044	2044	0
140	2312392	409600	408800	2312192	818400	16384	2048	2044	2044	0
160	2640072	409600	408800	2639872	818400	16384	2048	2044	2044	0
180	2967752	409600	408800	2967552	818400	16384	2048	2044	2044	0
200	3295432	409600	408800	3295232	818400	16384	2048	2044	2044	0
220	3623112	409600	408800	3622912	818400	16384	2048	2044	2044	0
240	3950792	409600	408800	3950592	818400	16384	2048	2044	2044	0
260	4278472	409600	408800	4278272	818400	16384	2048	2044	2044	0
280	4606152	409600	408800	4605952	818400	16384	2048	2044	2044	0
300	4933832	409600	408800	4933632	818400	16384	2048	2044	2044	0
WB										
0	818407	409600	408800	18432	818400	16384	2048	2044	2044	0
20	818407	409600	408800	346112	818400	16384	2048	2044	2044	0
40	819603	409600	410000	673798	819600	16384	2054	2050	2050	6
60	1230403	409600	820800	1228323	1230400	16384	4108	4104	4104	2060
80	2048403	409600	1638800	2046323	2048400	16384	8198	8194	8194	6150
100	2457603	409600	2048000	2455538	2457600	16384	10244	10240	10240	8196
120	2662003	409600	2252400	2642273	2662000	16384	11266	11262	11262	9218
140	2867203	409600	2457600	2865368	2867200	16384	12292	12288	12288	10244
160	3071203	409600	2661600	3030709	3071200	16384	13312	13308	13308	11264
180	3072535	409600	2662800	3052517	3072400	16384	13318	13314	13314	11270
200	3315415	430400	2884400	3307610	3314800	16384	14426	14422	14422	12274
220	3687655	410400	3276000	3637247	3686400	16384	16384	16380	16380	14332
240	3964108	819200	3072000	3963908	3891200	16384	15364	15360	15360	11268
260	4291788	1024000	3072000	4291588	4096000	16384	15364	15360	15360	10244
280	4619468	1228800	3072000	4619268	4300800	16384	15364	15360	15360	9220
300	4947148	1741200	3072000	4946948	4813200	16384	15364	15360	15360	6658

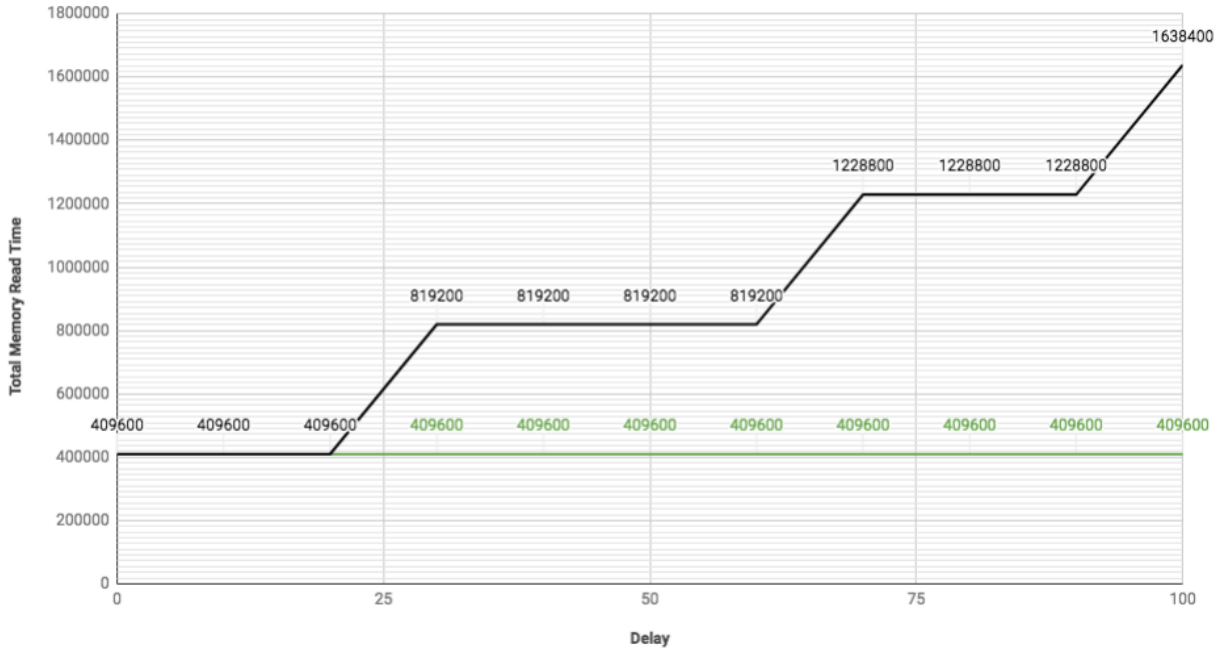


1. For RA and RB, the total CPU busy time is less than total simulation time, which causes the curves between delay0 to delay20 seem flat. Miss occurs when thread read the area(if succeed: cache hit) occupied by others. When the delay is small, the read can read the block and won't conflict other thread's reading. When the delay gets bigger, the other thread's reading will block current thread's reading. By analyzing the result of memtrace0 and memtrace1, we can find there are conflict between two threads. So the RB shows a staircase like pattern.

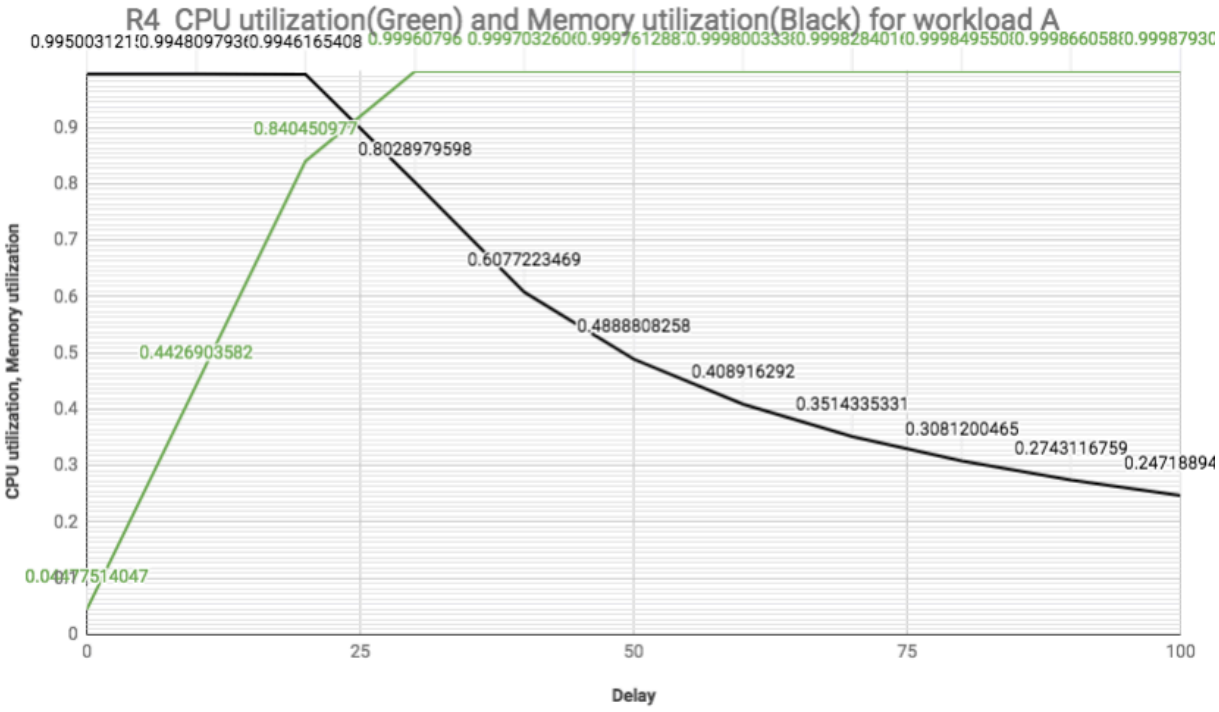
R2 Total Number of Misses vs Delay for workloads RA(Green) and RB(Black)

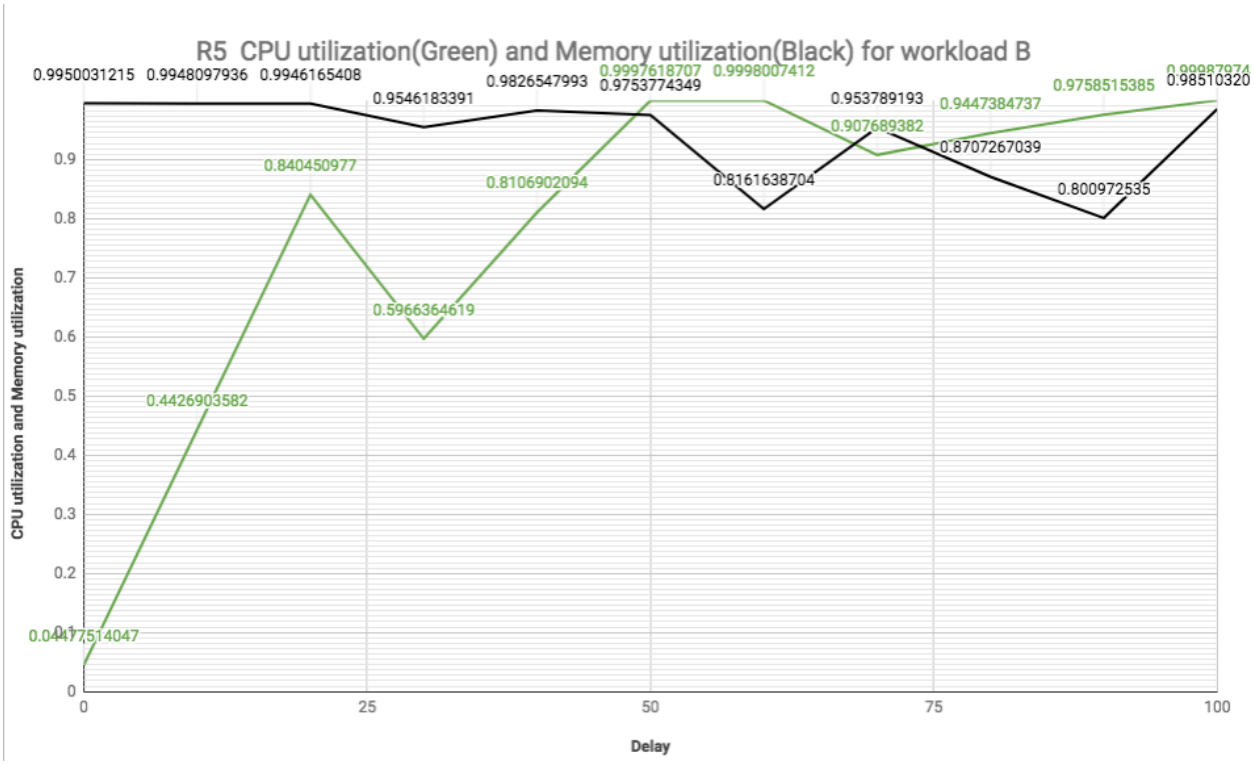


R3 Total Memory Read Time vs Delay for workloads RA(Green) and RB(Black)

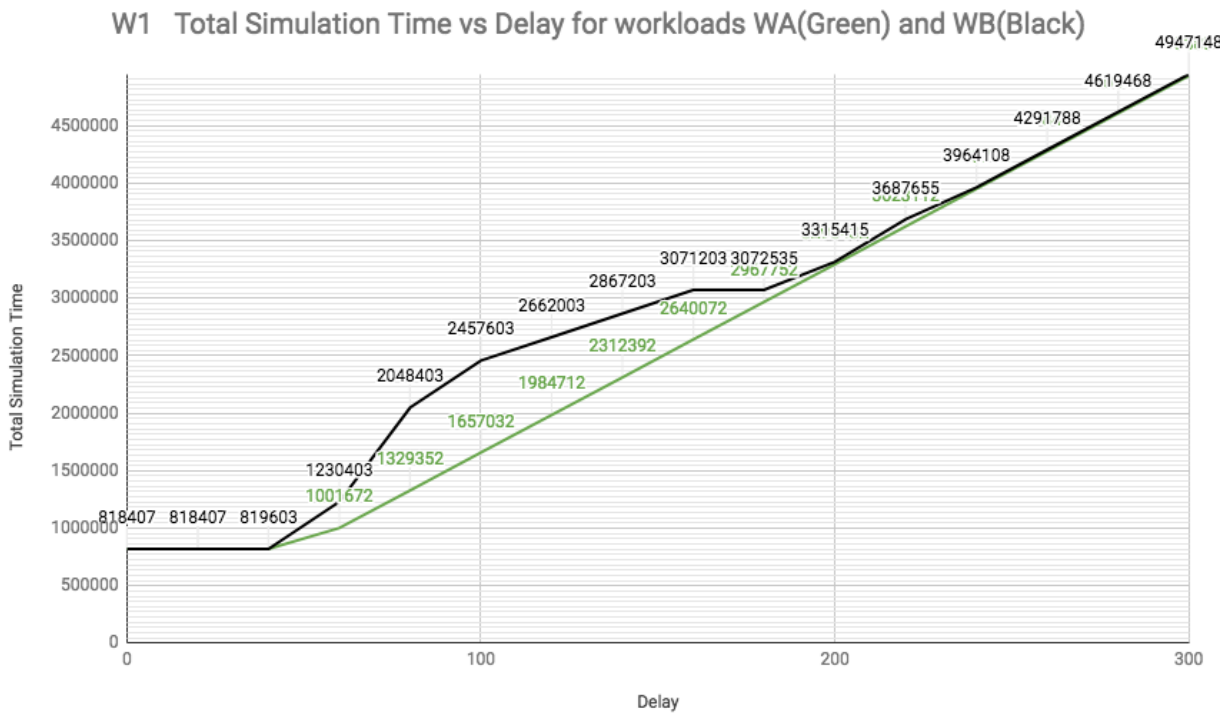


2. R2 and R3 have the same shape of curves. That is because once the miss occurs, data will be read from memory. Therefore, the total number of misses and total memory read time will increase simultaneously.





3. When the CPU delay gets bigger, it is obvious that the CPU utilization for both RA and RB will increase. As the total number of misses remains same for RA, the memory utilization will decrease on the contrast of CPU utilization increasement. At the same time, total number of misses increase for RB, there are more chance for miss and more chance for memory reading, then the memory utilization will increase for RB. When the delay parameter grows very large, the Memory utilization for RA would be 0, and the Memory utilization and CPU utilization for RA and RB would be 1.


W1 Total Simulation Time vs Delay for workloads WA(Green) and WB(Black)
Total Simulation Time
Delay
0
500000
1000000
1500000
2000000
2500000
3000000
3500000
4000000
4500000
0
100
200
300
818407
818407
819603
1230403
2048403
2457603
2662003
2867203
3071203
3072535
3315415
3687655
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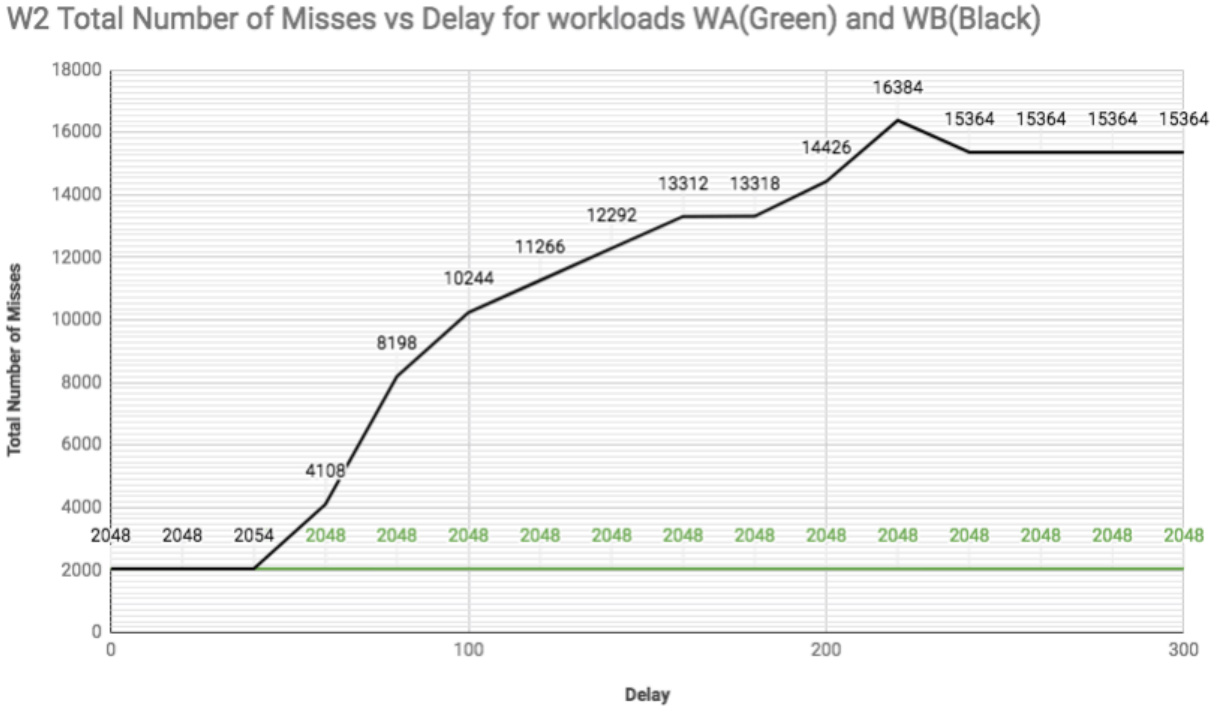
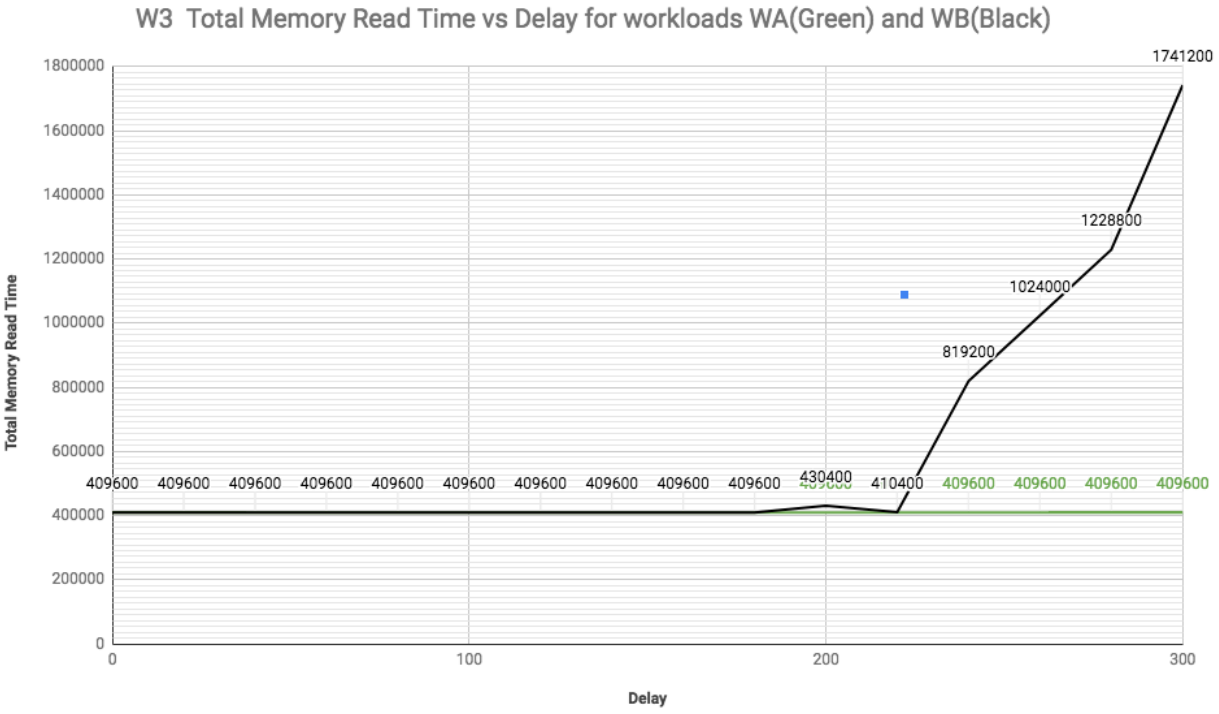
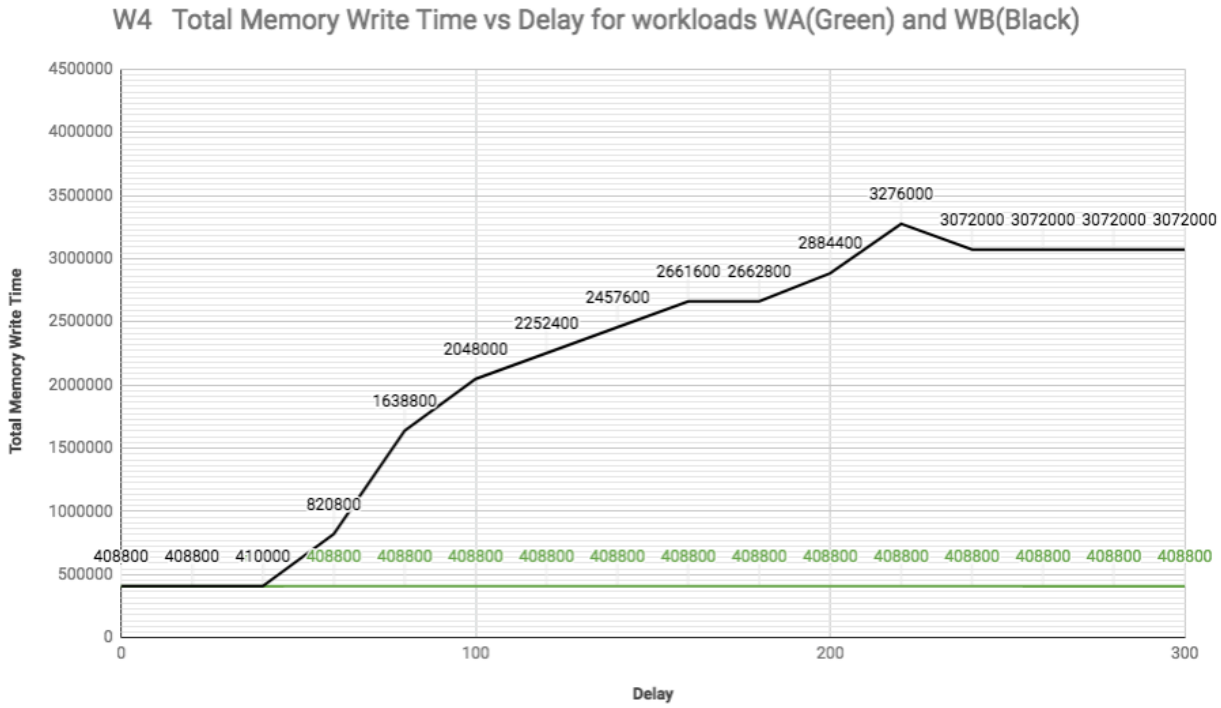
1001672
1329352
1657032
1984712
2312392
2640072


W2 Total Number of Misses vs Delay for workloads WA(Green) and WB(Black)
Total Number of Misses
Delay
18000
16000
14000
12000
10000
8000
6000
4000
2000
0
0
100
200
300
16384
15364 15364 15364 15364
14426
13312 13318
12292
11266
10244
8198
4108
2048 2048 2054 2048 2048 2048 2048 2048 2048 2048 2048 2048 2048 2048 2048 2048


W3 Total Memory Read Time vs Delay for workloads WA(Green) and WB(Black)
Total Memory Read Time
Delay
1800000
1600000
1400000
1200000
1000000
800000
600000
400000
200000
0
0
100
200
300
1741200
1228800
1024000
819200
430400
409600 409600 409600 409600 409600 409600 409600 409600 409600 409600 410400 409600 409600 409600 409600



4. As explained in question1, the increasement of CPU delay will lead to increasement of misses. The data is written into cache block when cache hit, and into memory when cache miss. So this time the total number of misses and total memory write time has the same curves. When the misses increase, the eviction and write back also increase. When misses occur, it will locate a cache block to use. And if it's dirty, its previous data will be written back to memory, otherwise data will be read from memory into cache block. Only when the CPU delay gets large will the memory read time increases. So the total memory read time for RB will have a delay on the contrast of total number of misses.

5. For CPU delay of 100, the total time for WA and WA (concurrent design) are 1657032 and 2457603. If the two threads were run sequentially on CPU, the total running time for WA should be 1034240.