A Micropower Low-Noise Monolithic Instrumentation Amplifier For Medical Purposes

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Abstract—**A CMOS low-power low-noise monolithic instrumentation amplifier (IA) is described. The power drain is reduced by use of current feedback and by use of only single-stage operational transconductance amplifiers (OTA's) in the low-frequency loop. The bandwidth of the IA is designed for medical purposes (0.5–500 Hz) and with variable gains of 14/20/26/40 dB, which are set by software control.**

I. Introduction

THE DESIGN of implantable integrated circuits requires the development of analog signal processing blocks, such as instrumentation amplifiers, with a minimum on external components and total power consumption. The presented circuit is an instrumentation amplifier (IA) for a medical measurement system called the Internal Human Conditioning System (IHCS) [1], [2]. The IHCS system is entirely implantable and performs all essential functions of measurement and stimulation in the human body. The monolithic input section has different independent channels. Each channel (see Fig. 1) consists of an IA with a programmable gain factor, a high-dynamic-range amplifier, an anti-aliasing filter, and a programmable switched-capacitor filter (cutoff frequency 250 Hz–2 kHz). The IA required for this system must have a high pass cutoff frequency in order to suppress the dc voltages of the used transducers.

Designing a micropower IA based on the conventional three-op-amp structure requires op amps with a low output impedance to drive the resistors of the IA network ($1/g_m$ of the output stage $\ll R_{\text{load}}$). This results, especially in CMOS design, in op amps with a large power drain. To solve this problem, an IA has been designed based on the current feedback technique [3], [4] and using only single-stage operational transconductance amplifiers (OTA's) in the low-frequency feedback loop.

To reduce offset, $1/f$ noise, and drift a lower cutoff frequency is used which can be fixed by one external capacitor (300 nF for a 0.5-Hz cutoff frequency). The gain values of the IA are set by software control in four ranges (14/20/26/40 dB). Because the total equivalent input noise is very important for the measurement of medical signals, the circuit has been optimized for low noise. The total equivalent input noise is less than 13-μV rms for a total current drain of 31 μA, which is almost one order of magnitude better than recently published micropower monolithic CMOS IA's (270-μV rms [5], and 80-μV rms [6]). In order to be able to compare more accurately different IA's on noise performance, for the same total current drain and bandwidth, a noise efficiency factor is introduced.

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II. Circuit Configuration

In Fig. 2 a principle circuit diagram of the IA is presented. The circuit has two feedback loops, one realizing the gain and the other the low cutoff frequency. The first feedback loop is based on the current feedback technique, where the structure has been transformed so that only a single-stage OTA is obtained. Further, in this IA circuit, a low cutoff frequency has been realized with an integrator structure (OTA-Int and C_{ext}) and an equivalent resistor made by OTA-g_m ($R \approx 1/g_m$), whereby only single-stage OTA's are used.

III. Amplitude and Phase Characteristics

For the calculation of the small-signal frequency specifications of the IA, the simplified circuit diagram presented in Fig. 2 is used. First the gain factor of the IA is discussed. Further the high f_H and the low f_L cutoff frequencies are calculated.

In the calculation of the gain factor, for frequencies $f_L < f < f_H$, the gate of transistor M_3 becomes an ac ground and the influence of the capacitor C_g can be neglected. The IA has a current feedback network, formed by transistors M_3 and M_4 and resistor R_g. Any ac output voltage creates, in this network, an ac current which flows through resistor R_s. Hence, the ac output voltage v_{out} creates a voltage v_{R_s} across the resistor R_s. The ratio F of

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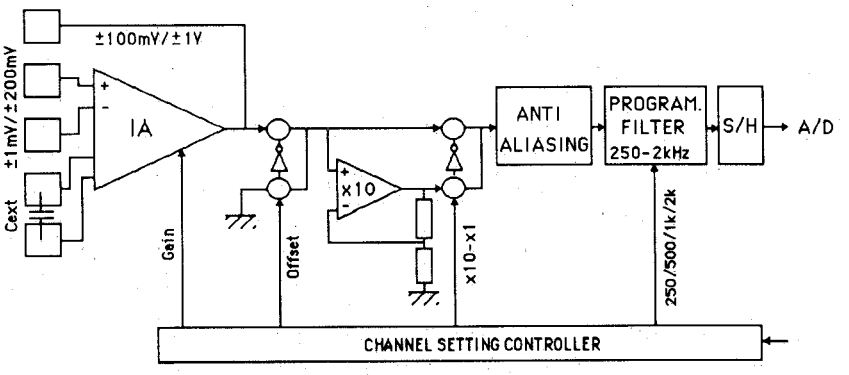

Fig. 1. Block diagram of one channel of the data-acquisition system of IHCS.

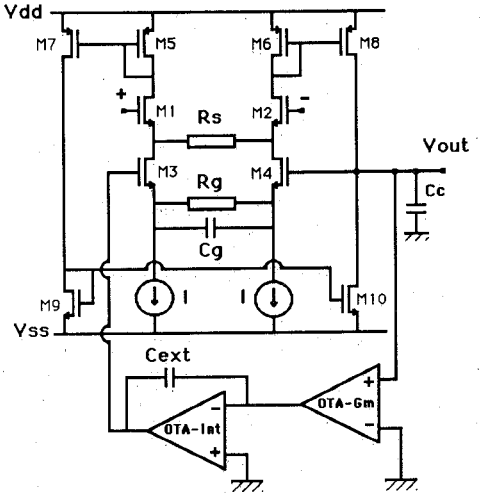

Fig. 2. Principle circuit diagram of the micropower IA.

v_{R_s} and v_{out} is given by

$$F=\frac{v_{R_s}}{v_{\text{out}}}=\frac{R_s\cdot i_{R_s}}{v_{\text{out}}}=\frac{R_s}{v_{\text{out}}}\cdot\frac{v_{\text{out}}}{R_g+\dfrac{1}{g_{m3}}+\dfrac{1}{g_{m4}}}$$

$$=\frac{R_s}{R_g\left(1+\dfrac{2}{g_{m3}\cdot R_g}\right)}. \tag{1}$$

This v_{R_s} voltage drop is fed back to the sources of transistors M_1 and M_2 of the input differential pair. So the differential pair has an ac input voltage given by the signal input voltage minus the voltage drop across R_s, resulting in a negative feedback. Using the theory of feedback networks, the gain factor of the IA is

$$A_c=\frac{A}{1+FA} \tag{2}$$

where A is the open-loop gain from the input to the output. In this circuit, A is ($R_s \ll 1/g_{m1}$)

$$A=\frac{g_{m1}\cdot g_{m8}}{g_{m5}(g_{\text{out}}+s\cdot C_c)}. \tag{3}$$

If A is designed so that $A\cdot F \gg 1$, the relation for the gain factor becomes

$$A_c=\frac{1}{F}=\frac{R_g}{R_s}\left(1+\frac{2}{g_{m3}\cdot R_g}\right) \tag{4}$$

or, by designing $g_{m3} \gg 2/R_g$, it can be simplified to

$$A_c=\frac{R_g}{R_s}. \tag{5}$$

Thus it is possible to change the gain factor of the IA very easily only by changing the ratio of the two resistors.

The high cutoff frequency is realized by adding a capacitor C_g across R_g. Hence R_g in (4) has to be replaced by $R_g//(s\cdot C_g)^{-1}$ or (if $g_{m3}\cdot R_g/2 \gg 1$)

$$A_c(s)=\frac{R_g}{R_s}\cdot\frac{(1+s\cdot 2\cdot C_g/g_{m3})}{(1+s\cdot C_g\cdot R_g)} \tag{6}$$

with a dominant pole (the high cutoff frequency) given by

$$f_H=\frac{1}{2\cdot\pi\cdot R_g\cdot C_g}. \tag{7}$$

In the study of the stability of the IA, the relative positions of the parasitic pole (in this circuit $f_2=g_{m5}/\{2\cdot\pi\cdot C_p\}$ with C_p being the capacitance on the gate node of M_5) and the frequency f_{bw}, whereby $|F\cdot A|=1$, are important. To reach a phase margin of more than 45°, the relative position should conform to $f_{bw} \leqslant f_2$. The loop transfer function is the product of the feedback factor F (using (1) and in calculating the effect of C_g) and the open-loop gain $A(s)$ (using (3) whereby $f \gg g_{\text{out}}/(2\cdot\pi\cdot C_c)$), or

$$F\cdot A(s)=\frac{R_s}{R_g}\cdot\frac{(1+s\cdot C_g\cdot R_g)}{(1+s\cdot 2\cdot C_g/g_{m3})}\cdot\frac{g_{m1}\cdot g_{m8}}{g_{m5}\cdot s\cdot C_c}. \tag{8}$$

At higher frequencies ($f > f_H, f > g_{m3}/\{4\cdot\pi\cdot C_g\}$) the relation becomes ($g_{m8}=g_{m5}$)

$$F\cdot A(s)=R_s\cdot\frac{g_{m1}\cdot g_{m3}}{2\cdot s\cdot C_c}. \tag{9}$$

Thus, the frequency f_{bw} is given by

$$f_{bw} = \frac{R_s \cdot g_{m1} \cdot g_{m3}}{2 \cdot \pi \cdot 2 \cdot C_c} \approx 250 \text{ kHz}. \quad (10)$$

Hence, for realizing a stable system ($f_{bw} \leqslant f_2$) the transconductance of transistor M_5 (g_{m5}) has to be designed higher than

$$g_{m5} \geqslant \frac{R_s \cdot g_{m1} \cdot g_{m3} \cdot C_p}{2 \cdot C_c}. \quad (11)$$

To reduce $1/f$ noise, the influence of offset voltage drift, and polarization effects in the measuring electrodes, a high pass cutoff frequency f_L is introduced. This is realized by adding an extra feedback network consisting of OTA-int and OTA-g_m. The OTA-int together with one external capacitor C_{ext} realizes an integrator. In order to realize an equivalent resistor without resistive loading the IA, an extra OTA (OTA-g_m) has been used. The advantage of this integrator structure, compared with others, is that any parasitic resistance at the output (which results from the use of an external capacitor) will have no effect on the IA circuit. It will thus not increase the output offset voltage of the IA. On the other hand, the influence of a parasitic resistance at the inverting node of OTA-int can be best reduced by guarding the node, because that node is a virtual ground. The OTA-g_m together with the integrator creates a cutoff frequency given by

$$f_L = \frac{g_m}{2 \cdot \pi \cdot C_{\text{ext}}}. \quad (12)$$

Because the lows cutoff frequency of biomedical signals can vary considerably (0.1 Hz for ECG up to 10 Hz for EMG [9]), an external capacitor C_{ext} is used for setting the cutoff frequency of the IA.

IV. CMOS Circuit Realization

In Fig. 3 the total circuit diagram of the realized IA is presented. The circuit has been upgraded at the input with a level shifter (transistor M_a) and a software-controlled switch matrix to set the values of R_s

The level shifters consist of PMOS source followers. They have been added in order to improve the common-mode range (CMR) of the IA. In this situation the positive CMR is limited by the saturation voltage of transistor M_c, the PMOS source follower M_a, and the power supply, or ($V_{dd}, V_{ss} = \pm 2.5$ V; $V_{T\text{pmos}} \approx V_{T\text{nmos}}$):

$$\text{CMR}^+ \approx V_{dd} - V_{T\text{pmos}} - V_{d\,\text{sat},a} - V_{d\,\text{sat},c} \approx 0.76 \text{ V}. \quad (13)$$

The negative CMR is limited by the saturation voltage of transistor M_b and the PMOS source follower, or

$$\text{CMR}^- \approx V_{d\,\text{sat},b} - V_{d\,\text{sat},a} - V_{T\text{pmos}} \approx -1.12 \text{ V}. \quad (14)$$

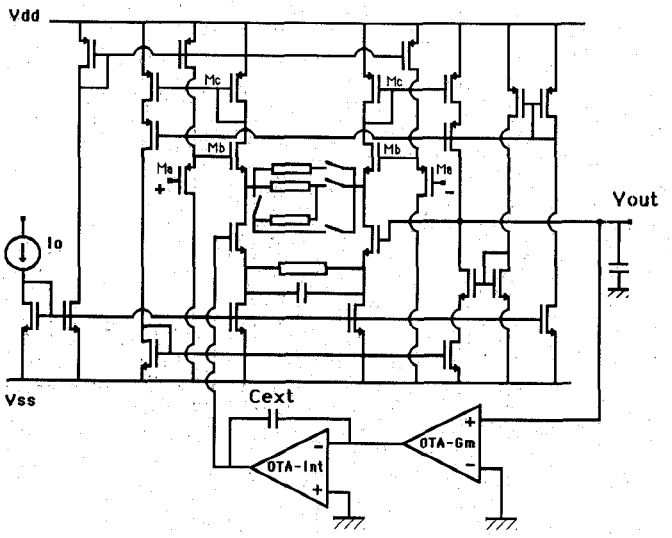

Fig. 3. Circuit schematic of the IA.

TABLE I

THE DIFFERENT INFLUENCES ON THE GAIN FACTOR

	Min		Max	
	%	dB	%	dB
Matching tolerance	-2	-0.17	2	0.17
Switch resistance	-3	-0.28	-1.5	-0.13
Bulk modulation	-2	-0.17	2.5	0.21
Total	-7	-0.62	3	0.25

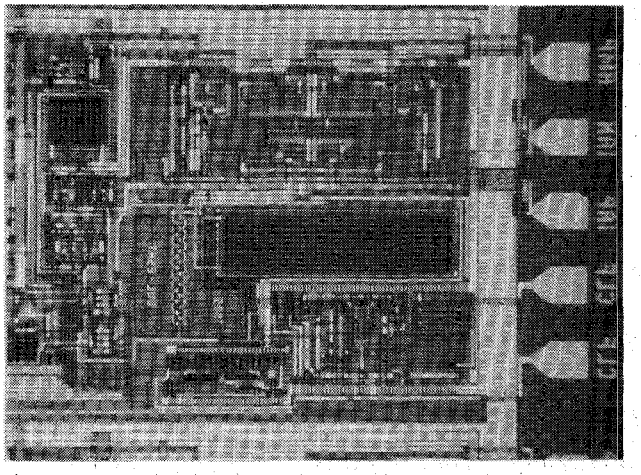

Fig. 4. A microphotograph of the realized IA.

The total CMR is given by $\text{CMR}^+ - \text{CMR}^-$, or

$$\text{CMR} \approx V_{dd} - V_{d\,\text{sat},c} - V_{d\,\text{sat},b} \approx 1.9 \text{ V}. \quad (15)$$

In order to realize a closed-loop gain, which can be set by software control, a switch matrix has been added which changes only the values of R_s. Hence, neither the low nor the high cutoff frequency is influenced by the gain factor of the IA. The gain can be set in four ranges: 14/20/26/40 dB. Using the $\times 10$ gain amplifier of the data-acquisition system (see Fig. 1), the full-scale input sensitivity of the data acquisition system can then be switched between 1/5/10/20 mV. If the $\times 10$ gain amplifier is not selected,

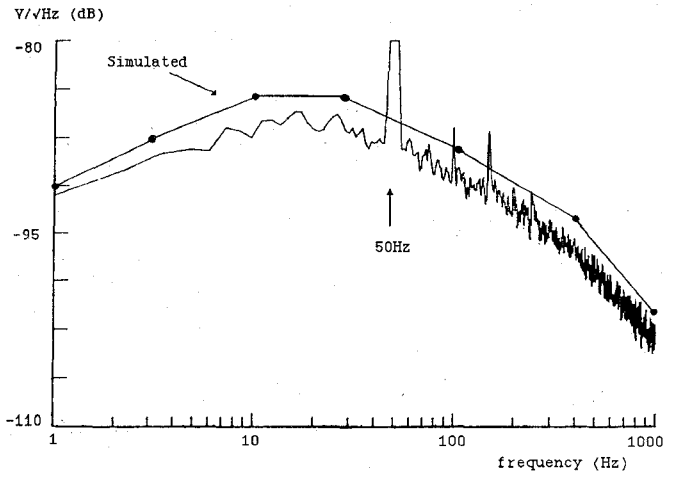

Fig. 5. Measured output noise of the IA.

the input sensitivity is 10/50/100/200 mV. Hence a large dynamic input range is obtained.

The gain accuracy is influenced by the matching tolerance of the used resistors, the finite switch resistance in the switch matrix, and the bulk modulation in the input transistors M_a. For an ion-implanted resistor, the matching tolerance is approximately ± 2 percent. The finite switch resistance of the switch matrix increases the value of R_s. The switches in the matrix are designed in such a way that the switch resistance over the total CMR is less than 1 kΩ and minimum 500 Ω. Hence the worst-case gain accuracy is

$$\frac{R_g}{R_s + \Delta R_s} = \frac{R_g}{R_s}\left(1 - \frac{\Delta R_s}{R_s}\right) \tag{16}$$

which results in a $-3/-1.5$ percent error for $R_s = 30$ kΩ.

Because PMOS source followers are used at the input, the gain of the IA is reduced due to the bulk effect by (common-mode input voltage $V_{com} = 0$ V)

$$\eta = \frac{g_m}{g_m + g_{m_b}} \approx 0.86 \approx -1.4 \text{ dB}. \tag{17}$$

This effect has been compensated by increasing the value of R_g. However, the reduction factor η is influenced by the common-mode input voltage or (where the reduction factor η_0 is at a common-mode input voltage V_{com} equal to zero)

$$\frac{\eta}{\eta_0} + \frac{\gamma + 2 \cdot \sqrt{\phi - V_{bs} + V_{com}}}{\gamma + 2 \cdot \sqrt{\phi - V_{bs}}} \tag{18}$$

which is 1.025 (2.5 percent) for $V_{com} = 0.8$ V and 0.98 (-2 percent) for V_{com} -1.2 V. In Table I the influence of the different effects is presented.

In Fig. 4 a microphotograph of the realized IA is presented. The circuit has been realized in the 3-μm P-well double-poly CMOS process. The total area of the IA, including the different resistors and control logic, measures 1000×1200 μm^2.

TABLE II

PERFORMANCES OF THE DESIGNED INSTRUMENTATION AMPLIFIER

	Calculated	Spice	Measured
Gain (dB)	14/20/26/40	14/20/26/40	13.6/20.1/25.8/39.4
I-Insamp	16μA	16μA	
I-OTA-Int	12μA	12μA	
I-OTA-GM	2μA	2μA	
Itotal	30μA	30μA	31μA
fHF,-3dB	500Hz	500Hz	570Hz
flf,-3dB			
Cext=10nF	16Hz	15Hz	15Hz
Cext=300nF	0.53Hz	0.5Hz	0.5Hz
CMRR (100Hz)	-	>100dB	>90dB
(ΔR=100k 0.5-500Hz)	-	-	>70dB
CMR	+0.76V/-1.12V	+0.76V/-1.12V	+0.73V/-1.15V
PSRR (0.5-500Hz)	-	>60dB	>50dB
THD (500mVpp-out)	<1%	<1%	0.7%

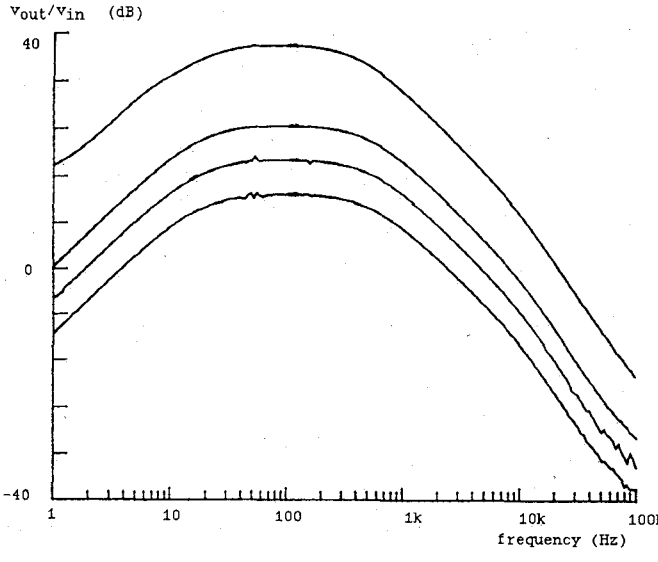

Fig. 6. Measured transfer function for the different programmable gains.

The power consumption of the IA is concentrated in three parts: the IA, the OTA-int, and the OTA-g_m. The IA is biased with a current of 1 μA, which results in a total current drain (cascode biasing network included) of 16 μA. the OTA-int is derived from a cascode OTA with a total current drain of 12 μA. The OTA-g_m consumes approximately 2 μA. So the total current drain of the IA is about 30 μA.

V. Design for Low Noise

In the design of the IA, the noise has been reduced as much as possible with respect to the total current drain. Because the bandwidth of the IA encloses low frequencies, the $1/f$ noise becomes very important. The main $1/f$ noise sources in this circuit are due to the NMOS transistors (flicker noise coefficient NMOS: $KF_n \approx 10 \times 10^{-9}$ V$^2 \cdot \mu$m^2; PMOS: $KF_p \approx 0.2 \times 10^{-9}$ V$^2 \cdot \mu$m^2), and especially to M_1, M_2 and M_9, M_{10} (see Fig. 2). The area of

these transistors has been increased just up to the point that the parasitic pole ($g_m/(2\cdot\pi\cdot C_{ox}\cdot W\cdot L)$) does not impair the stability of the system. Meanwhile, one of these poles compensates the zero which appears in the closed-loop transfer function (see (6)). In Fig. 5 the measured and simulated output noise of the realized IA are presented ($C_{ext}=10$ nF, gain = 40 dB, $V_{rms,in}\approx 10\ \mu$V).

VI. Small-Signal Measurements

In Table II the calculated, simulated (SPICE), and measured specifications of the realized IA are presented. The measured transfer function at the different gains is presented in Fig. 6. The f_{HF}, -3 dB, is realized with an implanted resistor and a double-poly capacitor. Due to the poor knowledge of the absolute values (accuracy 20 percent), the measured cutoff frequency is higher than expected. The values of the measured gains deviate from the calculated ones because of the finite switch resistors and the matching tolerance of the ion-implanted resistors, but they are still within the calculated tolerances (see Table I: $-0.6/0.25$ dB).

The measured CMRR of the IA's at 100 Hz is approximately 93 dB. In many applications where IA's are applied, a significant mismatch exists between the resistive source impedances which degrade the CMRR specs [5]. In Fig. 7 the measured common-mode gain (CMG) with a source resistance unbalance of 100 kΩ is presented (gain factor 40 dB). Hence the CMRR ($= A_c/\text{CMG}$) of the IA is still more than 70 dB over the whole bandwidth (0.5–500 Hz).

VII. Noise Performance Comparison

In order to be able to compare the noise specifications reached with other recently published IA's, a noise efficiency factor (NEF) is introduced. The total equivalent input noise of an ideal bipolar transistor (only thermal noise and no base resistance) is given by

$$V_{rms,in}=\sqrt{\text{BW}\cdot\frac{\pi}{2}\cdot\frac{4\cdot k\cdot T}{gm}}=\sqrt{\text{BW}\cdot\frac{\pi}{2}\cdot\frac{4kT\cdot U_T}{I_C}} \quad (19)$$

with BW being the frequency bandwidth (for a bipolar transistor this is the f_t). The NEF of a system is then defined as

$$\text{NEF}=V_{rms,in}\sqrt{\frac{2\cdot I_{tot}}{\pi\cdot U_T\cdot 4kT\cdot\text{BW}}} \quad (20)$$

where I_{tot} is the total current drain in the system and $V_{rms,in}$ is the total equivalent input noise. The NEF describes how many times the noise of a system with the same current drain and bandwidth is higher compared to the ideal case, e.g., for a CMOS transistor with only white noise, the noise power is given by

$$V^2_{rms,in}=\frac{4kT}{2/3g_m}\cdot\text{BW}\cdot\frac{\pi}{2}=\frac{3kT(V_{gs}-V_T)}{I_D}\cdot\text{BW}\cdot\frac{\pi}{2} \quad (21)$$

or, working on the boundary of strong inversion ($V_{gs}-V_T=2\cdot n\cdot U_T\cdot\sqrt{10}$ with n being the weak inversion slope) and the same bandwidth as the bipolar, the NEF is 2.43. This means that the noise of a CMOS design in strong inversion with the same current drain and bandwidth is approximately five times higher compared to a bipolar design.

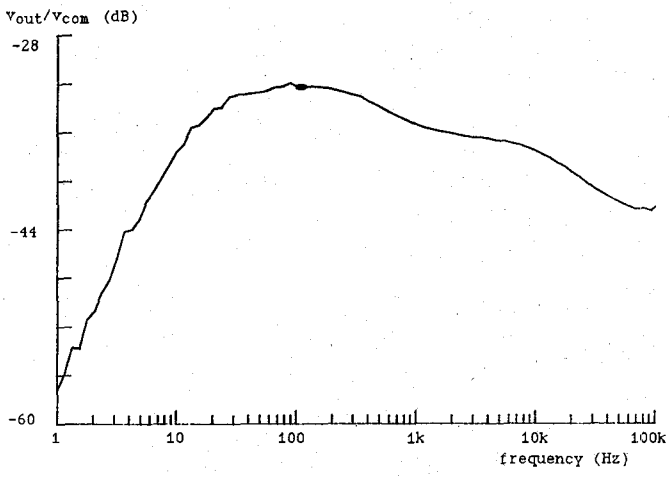

Fig. 7. Measured CMG of the IA with 100-kΩ unbalance in source resistance.

TABLE III

Performances of Different Instrumentation Amplifiers

	1	2	3	4	5	6
Ref	Cext=10nF	Cext=300nF	[5]	[6]	[7]	[8]
Type	CMOS	CMOS	CMOS	CMOS	Bip.	Bip. Discrete
Type	CFB	CFB	SC	SC	3-Opamp	CFB
Itot (A)	31µ	31µ	7.2µ	7µ	300µ	15µ
BW (Hz)	15-570	0.5-570	4k	4k	3.5k	0.1-200
Vrms (V)	8.2µ	9.6µ	270µ	79µ	20µ	0.85µ
NEF	74	87	440	130	225	9

In Table III different IA's are compared with the realized IA discussed in this paper (no. 1 and no. 2). The third and fourth IA's are the same IA circuits involving switched-capacitor techniques to reduce offset. They are designed in two different CMOS processes. No. 3 has been realized and optimized in the same 3-µm CMOS process as the presented IA. So column 2 can be best compared with column 3. As can be concluded from the table, the circuit presented has the best performance of all monolithic integrated IA's.

VIII. Conclusion

In this paper a new monolithic instrumentation amplifier is presented to be used in a medical implantable system. The small-signal parameters of the presented instrumentation amplifier have been analyzed. Further, the circuit

has been optimized to reduce the total equivalent input noise. Measurements have been obtained to compare the specifications of the circuit. A noise efficiency factor is introduced in order to be able to compare the design with other realized instrumentation amplifiers. It is shown that the circuit has the best performances of all monolithic integrated instrumentation amplifiers available up until now.

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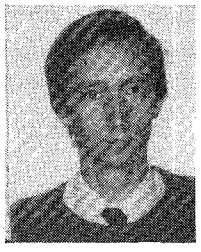

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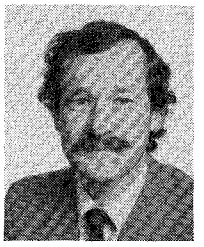

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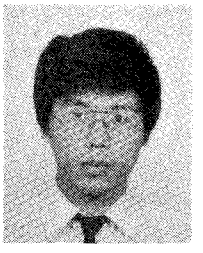

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