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Introduction to CPU Function

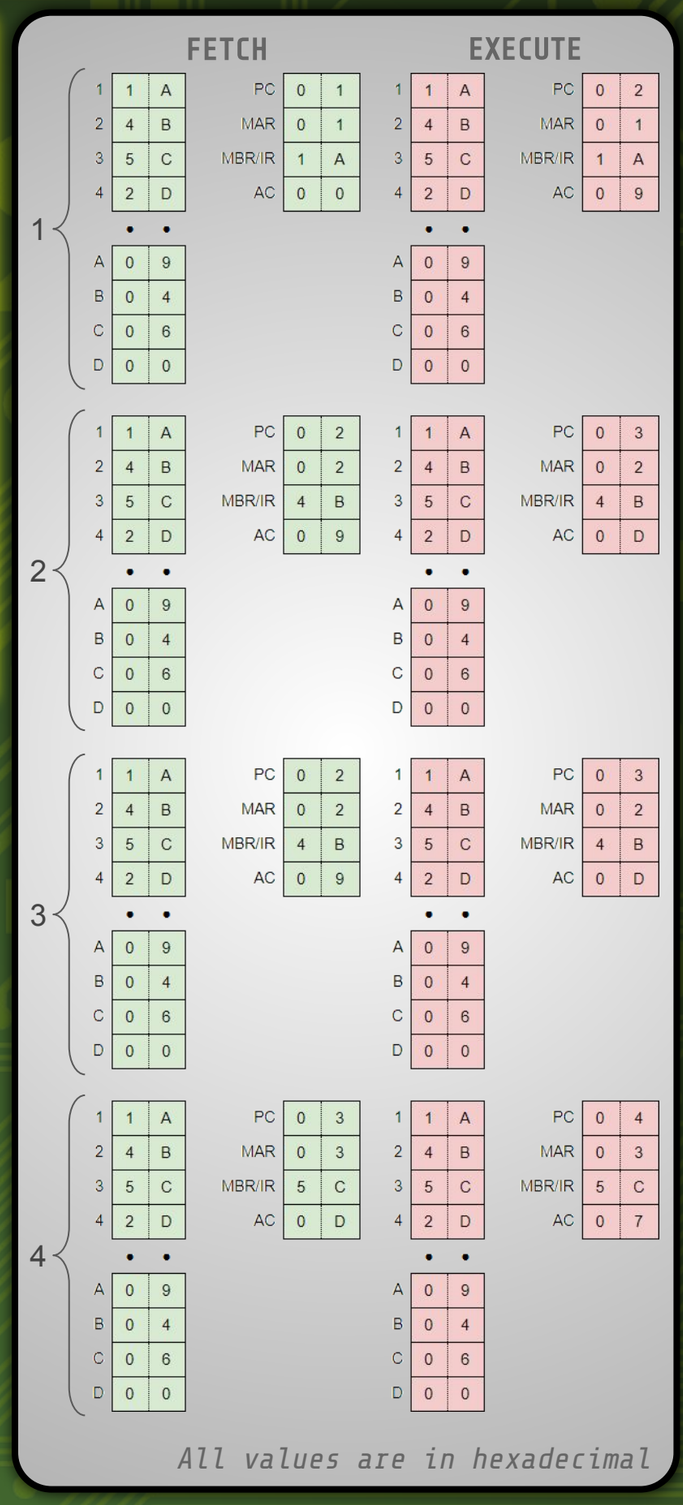
Abstract
This poster explores the concepts surrounding the IAS/von Neumann computer, particularly regarding the function of the CPU. We cover the fundamental ideas that have influenced the way in which computers are designed today and discuss the way in which the CPU functions within a computer.

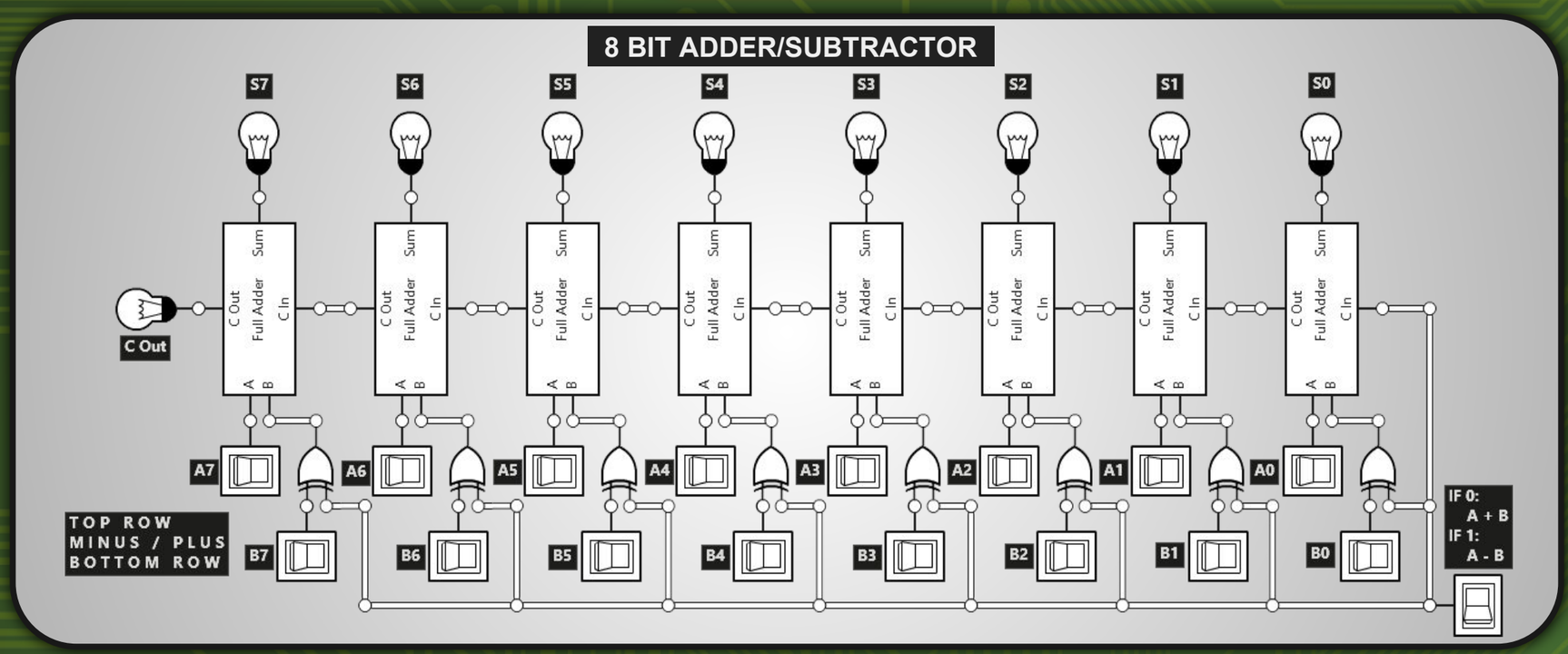
Opcodes
001 (1) - **LOAD** word from memory to AC
010 (2) - **STORE** word in AC to address

100 (4) - **ADD** word from memory to AC
101 (5) - **SUBTRACT** word from memory from AC

The fetch execute cycle is the core of how programs are executed in von Neumann architecture. Instructions are "fetched" from memory and are then interpreted (the instruction cycle) and executed. This creates a repeating operation made up of the fetch cycle and the execute cycle. The cycle only halts if it runs out of instructions, an error occurs or the instruction requests a halt.

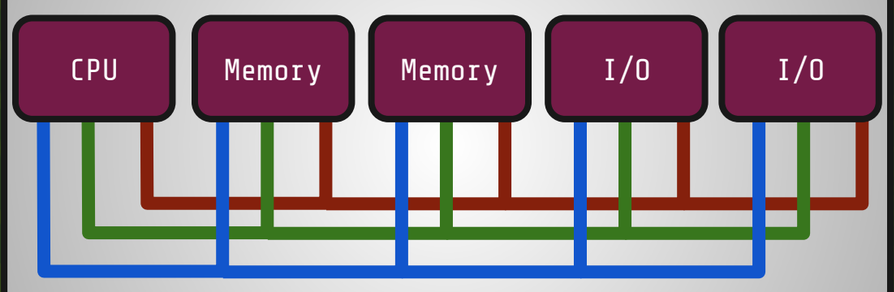
Each fetch cycle starts with moving the instruction address from the PC to the MAR, the word at the address in the MAR is then copied to the MBR (and then to the IR, or sometimes directly to the IR). The execute cycle then increments the PC before executing the instruction in the IR, this could result in the word in the AR changing, the memory being written to, or another operation of the processor being performed.





Cache
Cache memory is designed to provide a high capacity, low access time and low cost solution for a computer's main memory.
The leveled cache design means that blocks of data can be prioritised such that more frequently accessed data can be accessed faster.

Bus Interconnection Scheme



The bus interconnection is the component that connects all of the internal components together, allowing them to transfer data and communicate between each other. It is made out of several lines for different data types. See the diagram to the left.

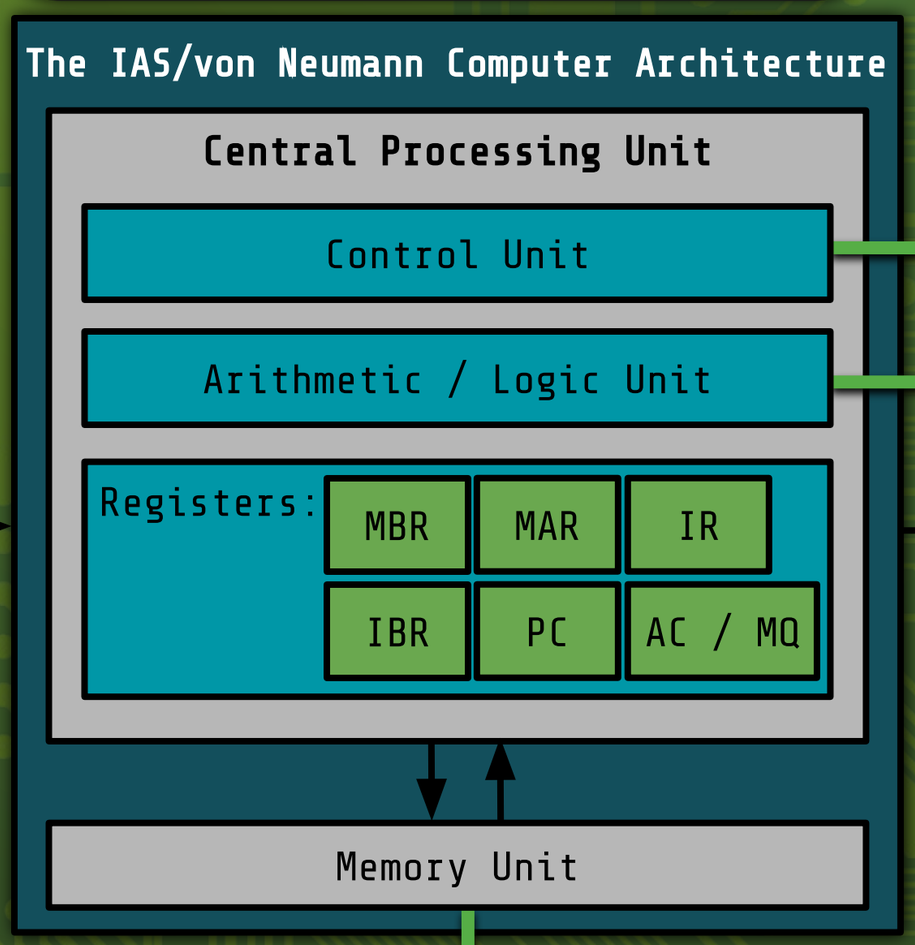
MBR
The Memory Buffer Register is a storage location in which and data can be sent to and from other components in the computer such as the input/output device or the computer's memory.

MAR
The Memory Address Register is the storage place which contains the memory address in which data needs to be sent too or received from.

IR
The Instruction Register holds the opcode instruction for the process being executed.

PC
The Program Counter is the register which contains the address of the next instruction which needs to be received from memory.

AC & MQ
The Accumulator and the Multiplier Quotient are storage locations that are utilised for the temporary holding of the data for the ALU operations along with the results of the operations.



The program control unit interprets the instructions stored in memory and executes them, passing data to and from the ALU and the memory unit.
The control unit also dictates the sequence at which operations are carried out.

Three Key Concepts of von Neumann Architecture:
- Data and instructions are stored in a singular read/write memory.
- Data contained within the memory is addressable by location.
- The execution of instructions run sequentially unless explicitly modified.

The arithmetic logic unit performs the fundamental binary operations as instructed by the program control unit.

A significant design aspect within Von Neumann architecture is storing of both instructions and data within the same memory.
Through the use of a stored program the instruction set can be directly accessed by the computer allowing for easier program alterations by changing the values of portions of the memory through I/O equipment.

Stored Program Functionality
The von Neumann architecture allows for the arrangement of general purpose hardware which can accept control signals, used to supply a set of instructions.
The instruction interpreter is the component at which the provided codes, which are stored in memory, generate control signals to execute the arithmetic and logic functions.

The I/O equipment facilitates the means in which data and instructions are input into the computer and how computational results are output. This acts as the interface for human manipulation of data and instructions which enables greater computational flexibility compared to the manual modification of physical components, required with older computers.