Final Exam

● Graded

Student

PO-YUN) 鄭博允 (CHENG

Total Points

62 / 100 pts

Question 1

Question 1

24 / 28 pts

- ✔ **+ 28 pts** Correct
  - **– 2 pts** A mistake in Q1.1
  - **– 2 pts** A mistake in Q1.2
  - **– 2 pts** A mistake in Q1.3
  - **– 2 pts** A mistake in Q1.4
  - **– 2 pts** A mistake in Q1.5
  - **– 2 pts** A mistake in Q1.6
  - **– 2 pts** A mistake in Q1.7
- ✔ **– 4 pts** Multiple mistakes in Q1.1
  - **– 4 pts** Wrong in Q1.6
  - **– 4 pts** Wrong in Q1.7

Question 2

Question 2

0 / 6 pts

+ 6 pts Correct

+ 4 pts Correct when L = 1 and H = 1 (Cycles 1, 2, 3, 5)

+ 4 pts Correct when L = 1 and (L, H) = (0, 0) (Cycles 1, 4, 5)

+ 2 pts Correct when L = 1 (Cycles 1, 5)

+ 2 pts Correct when H = 1 (Cycles 2, 3)

+ 2 pts Correct when (L, H) = (0, 0) (Cycle 4)

✔ **+ 0 pts** Totally wrong or empty

Question 3

Question 3

8 / 8 pts

✔ **+ 8 pts** Correct (C, 0, C'+DE, C'D'+CE)

+ 6 pts 1 minor mistake (not minimum or wrong for (A, B) = (1, 1))

+ 6 pts 1 minor mistake (floating or wrong for (A, B) = (0, 1))

+ 4 pts 2 minor mistakes or 1 major mistake

+ 2 pts Reasonable effort

+ 0 pts Totally wrong or empty

Question 4

Question 4

12 / 12 pts

✔ **+ 8 pts** 4.1. Correct

+ 6 pts 4.1. One mistake (one of A+, B+. or Z)

+ 4 pts 4.1. Two mistakes (two of A+, B+. or Z)

+ 2 pts 4.1. Reasonable effort

✔ **+ 4 pts** 4.2. Correct

+ 2 pts 4.2. One mistake or no output

+ 0 pts Totally wrong or empty

Question 5

Question 5

8 / 8 pts

+ 8 pts Correct

✔ **+ 8 pts** Correct (with equivalent states)

+ 6 pts 1 minor mistake

+ 4 pts 1 major mistake or 2 minor mistakes

+ 2 pts Reasonable effort

+ 0 pts Totally wrong or empty

Question 6

Question 6

0 / 8 pts

+ 8 pts Two solutions

+ 6 pts Two solutions and one without sufficient explanation

+ 4 pts Two solutions and both without sufficient explanation

+ 4 pts Two equivalent or similar solutions

+ 4 pts One solution

+ 2 pts Some reasonable effort (e.g., increase the propagation delay of the combinational circuit)

✔ **+ 0 pts** Totally wrong or empty

Question 7

Questions 7.1-7.3

4 / 6 pts

+ 6 pts Correct

✔ **+ 4 pts** One mistake

+ 2 pts Two mistakes

+ 0 pts Totally wrong or empty

Question 8

Question 7.4

0 / 6 pts

+ 6 pts True with correct explanation

+ 4 pts True with almost-correct explanation

+ 2 pts True only

+ 2 pts False with reasonable effort

✔ **+ 0 pts** False only or empty

Question 9

Question 8

2 / 8 pts

+ 8 pts Yes with correct explanation

+ 6 pts Yes with almost-correct explanation

+ 6 pts Yes with almost-correct explanation (gate/propagation delay)

+ 4 pts Yes with reasonable explanation

+ 4 pts Yes with reasonable explanation (useless if changing during the first half)

+ 4 pts Yes with reasonable explanation (similar to S-R FF)

+ 2 pts Yes only

✔ **+ 2 pts** No with reasonable explanation

+ 0 pts No only or empty

Question 10

Question 9

4 / 10 pts

+ 10 pts "T flip-flops last" with correct explanation

+ 8 pts "T flip-flops last" with almost-correct explanation

+ 6 pts "T flip-flops last" with reasonable effort

+ 4 pts "T flip-flops last" without explanation

+ 6 pts "T flip-flops middle" with good explanation

✔ **+ 4 pts** "T flip-flops middle" with reasonable effort

+ 2 pts "T flip-flops middle" with wrong explanation

+ 2 pts "T flip-flops first" with reasonable effort

+ 0 pts "T flip-flops first" without explanation

+ 0 pts Empty

CSIE 2344, Spring 2023: Final Exam

Name: 鄭博允 SID: B11902038 Email: b11902038@csie.ntu.edu.tw

1 Counter Design (28pts)

Design a 3-bit counter which counts CBA in the sequence: 001, 010, 110, 111, 100, 011, and repeats. If the counter is initialized as 101, it should count to 001 and then follow the sequence.

1. (4pts) Complete the following truth table.
2. (4pts) Complete the following Karnaugh map for B^+.
3. (4pts) Complete the following Karnaugh map for A^+.
4. (4pts) Use an S-R flip-flop and complete the following Karnaugh map for R_B.
5. (4pts) Use a J-K flip-flop and complete the following Karnaugh map for K_A.
6. (4pts) Derive a minimum sum-of-products expression for R_B. $R_B = BC$
7. (4pts) Derive a minimum sum-of-products expression for K_A. $K_A = B'C'$

No explanation is needed.

C	B	A	C^+	B^+	A^+
0	0	0	X	X	X
0	0	1	0	1	0
0	1	0	1	1	0
0	1	1	1	1	1
1	0	0	1	0	0
1	0	1	0	1	1
1	1	0	0	0	1
1	1	1	X	X	X

BA \ C	0	1
00	X	0
01	1	1
11	1	X
10	1	0

B^+

BA \ C	0	1
00	X	0
01	0	1
11	1	X
10	0	1

A^+

BA \ C	0	1
00	X	X
01	0	0
11	0	X
10	0	1

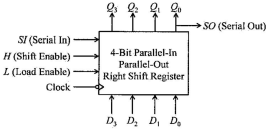
R_B

BA \ C	0	1
00	X	X
01	1	0
11	0	X
10	X	X

K_A

2 Parallel-In Parallel-Out (PIPO) Right Shift Register (6pts)

Given the following PIPO right shift register, complete the following table. No explanation is needed.

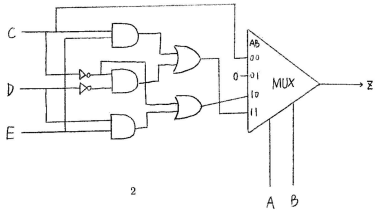


Clock Cycle	L	H	SI	D_3	D_2	D_1	D_0	Q_3	Q_2	Q_1	$Q_0 = SO$
1	1	0	0	1	0	0	0	1	0	0	0
2	0	1	1	0	1	0	1	0	1	0	0
3	0	1	0	1	0	1	0	1	0	1	0
4	0	0	1	1	1	1	1	0	1	0	1
5	1	0	0	0	0	0	0	1	0	1	0

3 Multiplexer (8pts)

Draw a circuit for $F(A, B, C, D, E) = A'B'C + AB'C' + AB'DE + ABC'D' + ABD'E + ABCE$ with the following requirements. No explanation is needed.

- There is exactly one multiplexer, and the multiplexer has 2 control inputs and 4 data inputs.
- The control inputs are A and B.
- Each data input is a minimum sum-of-products (AND-OR) circuit of C, D, and E.

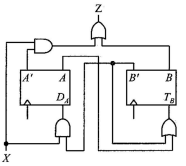


4 Circuit Analysis (12pts)

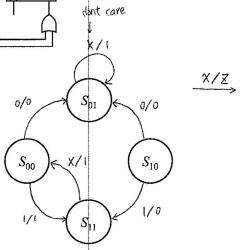
Given the circuit including one D flop-flop and one T flop-flop.

1. (8pts) Complete the following transition table.
2. (4pts) Draw the corresponding state graph where a state S_{ij} represents the state $(A, B) = (i, j)$.

No explanation is needed.



AB	A^+B^+		Z	
	$X=0$	$X=1$	$X=0$	$X=1$
00	01	11	0	1
01	01	01	1	1
11	00	00	1	1
10	01	11	0	0

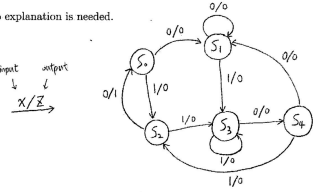


5 State Graph Derivation (8pts)

Draw the state graph of a Mealy machine with one input and one output. If the input is 0 following a sequence of "exactly" one 0 input (not two or more 0's) and one 1 input (not two or more 1's), the output is 1; otherwise, the output is 0. Example:

Input 010010101
Output 001000010

No explanation is needed.

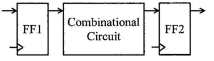


S_0 : 10|0
S_1 : ~00
S_2 : 101
S_3 : ~11 (initial state)
S_4 : ~110

6 Setup Time (8pts)

Setup time is the amount of time that a flip-flop must be stable before the active edge. Considering the following sequential circuit, if the setup time of the second flip-flop (FF2) is violated, how to fix it without changing the flip-flops?

1. (4pts) List two solutions.
2. (4pts) Explain the reasons.



7 State Equivalence and Circuit Equivalence (12pts)

Answer if the statements are True or False by circling the correct choices. No explanation is needed.

(T) F 1. (2pts) For a 1-bit input X, if the outputs of two states are not equal, then the two states are not equivalent.

T (F) 2. (2pts) For a 1-bit input X, if the next states of two states are not equal ("equal" means "the same"), then the two states are not equivalent.

(T) F 3. (2pts) Two equivalent sequential circuits always have the same number of states.

Answer if the statement is True or False and explain the reason.

4. (6pts) Two states p and q are equivalent if and only if for each 2-bit input X and Y,

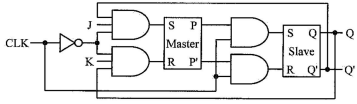
$$\lambda(p, X) = \lambda(q, X) \text{ and } \lambda(\delta(p, X), Y) = \lambda(\delta(q, X), Y) \text{ and } \delta(\delta(p, X), Y) \equiv \delta(\delta(q, X), Y),$$

where $\lambda()$ is the output and $\delta()$ is the next state.

8 J-K Flip-Flop (8pts)

In the slides of Unit 11, it is mentioned that we should only allow the S and R inputs of a S-R flip-flop to change during the first half of a clock cycle.

1. (2pts) Given the following implementation of a J-K flip-flop, do we have the same constraint?
2. (6pts) Explain the reason.



1. No

2. This implementation forced two S-R flip-flop working at different period of clock cycle. That is, in the first half of a clock cycle, only the Master S-R flip-flop work, and the Slave S-R flip-flop stay unchanged because both it's inputs are 0. In the second half of a clock cycle, the situation reverse.

   Therefore, we don't have to ristrict the period of change inputs since it doesn't affect the circuit.

9 State Assignment (10pts)

In the slides of Unit 15, it is mentioned that the guidelines for state assignment (for example: placing 1's together on an input map) only works for specific flip-flops.

1. (4pts) Sort D, T, and J-K flip-flops by their fitness for the guidelines (for example: answering "D > T > J-K" means that D flip-flops best fit the guidelines, better than T flip-flops, and J-K flip-flops least fit the guidelines).
2. (6pts) Explain the reason. Note that we are not expecting an answer which discusses a specific example.

1. J-K > T > D

2. J-K flip-flop is best fit the guidelines since it has more input-output situations, that is, we can identify different state more easily.
For T flip-flop and D flip-flop, the possible situations are less than J-K flip-flop. Moreover, T > D.