PEC Punjab Engineering College (Deemed to be University)

Chandigarh

Mid Term Examination(18192)

Programme: B.Tech (ECE) | Year/Semester: 1st/2nd
Course Name: Digital Design | Course Code: ECN 103
Maximum Marks:25 | Time allowed:1:30 Hours

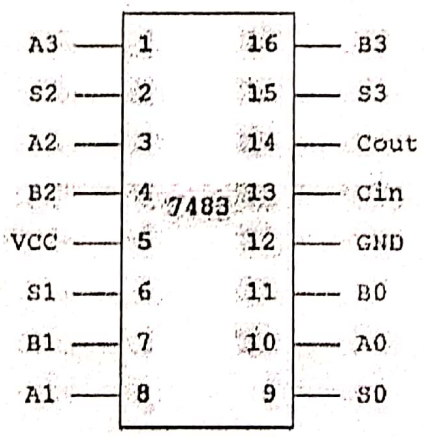
1) How many bits would be required to encode decimal numbers from 0 to 9999 in straight binary and BCD codes. What would be the BCD equivalent of decimal number 27 in 16 bit representation. 2

2) Using Q M (Quine McCluskey) method find the minimum SOP for
f(A,B,C,D)=Σ(1,2,3,9,12,13,14) + d(0,7,10,15).
Implement the simplified expression using following two level implementations:
(i) AND NOR (ii) NAND AND (iii) OR NAND (iv) NOR OR 10

3) What are parity generator and parity checker circuits? Explain an odd parity generator and checker circuit for a 3 bit data input using truth table and logical implementation. Only two input XOR and XNOR gates are available. 6

4) Implement the function F(A,B,C)=Π(1,2,5) using (i) 4:1 Mux (ii) Suitable Decoder 4

5) IC 7483 is a 4 bit adder. Show how can you build 8 bit adder subtractor using IC 7483.Pin configuration of IC 7483 is as under:



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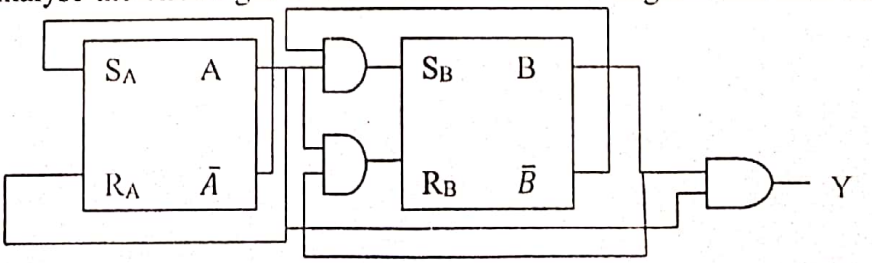
EXPLORE INNOVATE EXCEL **Punjab Engineering College (Deemed to be University)**
Chandigarh
End-Term Examination(18192)

Programme: **B.Tech (ECE)** Year/Semester: **1st/2nd**
Course Name: Digital Design Course Code: **ECN 103**
Maximum Marks:80 Time allowed: **3 Hours**

Notes

- All questions are compulsory.
- Unless stated otherwise, the symbols have their usual meanings in context with subject. Assume suitably and state, additional data required, if any.
- The candidates, before starting to write the solutions, should please check the question paper for any discrepancy, and also ensure that they have been delivered the question paper of right **course code**

Q. No.			Marks
1.	a)	Implement (i) a three input Ex-NOR function using only two input Ex NOR gates(ii) a three input NAND gate using two input NAND gates.	4
	b)	Prove that $\bar{L}(M+\bar{N})+\bar{L}\bar{P}Q=(L+\bar{P}Q)(\bar{L}+M+\bar{N})$ using Boolean rules and laws.	2
	c)	List the eight degenerate two level forms and show that they reduce to a single operation.	4
2	a)	Given the Boolean function Y(A,B,C,D)=ΠM(1,2,3,8,9,10,11,14) +d(7,15) .Simplify using K maps and obtain the answer in Product of Sums form.	6
	b)	$\bar{A}B+CD$ is a simplified expression of the expression $ABCD+\bar{A}\bar{B}CD+\bar{A}B$. Determine if there are any don't cares.	4
3.	a)	Show that how 2 two bit numbers can be compared using (i) 16:1 MUX (ii) 8:1 MUX (iii) Suitable Decoder.	6
	b)	Show the implementation of a four bit adder subtractor using full adders and with a provision of detecting overflow. Explain the operation of circuit for signed as well as unsigned numbers.	4
4.	a)	Derive the characteristic equation of RS flip flop. Give excitation table of RS flip flop. Analyse the circuit given below. Draw the state diagram and state analysis table. 	7

	b)	Convert JK flip flop to D flip flop.	3
5	a)	Show and explain the logic arrangement for a parallel in parallel out shift register. Also show the wiring arrangement to effect a shift left operation.	4
	b)	The IC 74LS174 datasheet gives a set up time of 20 ns and a hold Time of 5 ns .What is the minimum required width of data input levels for 74LS174.Also define set up time and hold time.	3
	c)	What is a decade counter? Design Mod 5 counter and then build decade counter by cascading mod 5 and mod 2 counter. From the cascaded circuit, draw the output waveforms and write the count sequence obtained..	5
	d)	Draw the block diagram of Mealy and Moore Finite State Machines. Compare the two	3
6.	a)	Draw a PLA circuit to implement the function by making the PLA programming table $F_1 = \bar{A}B + A\bar{C} + \bar{A}B\bar{C}$ $F_2 = \overline{(AC + AB + BC)}$	6
	b)	Define propagation delay, power dissipation , fanout and Noise Margin Parameter logic family.	6
	c)	How many inputs of a low power Schottky TTL NAND gate can be reliably driven from a single output of Schottky TTL NAND gate given the following parameters.	3

	I_{OH}	I_{OL}	I_{IH}	I_{IL}
Schottky TTL	1 mA	20 mA	0.05 mA	2 mA
Low Power Schottky TTL	0.4 mA	8 mA	0.02 mA	0.4 mA

7	a)	Explain parallel comparator type A/D converter for a 3 bit digital Output.	6
	b)	What are the output voltages caused by each bit in 5 bit ladder if input levels are 0 = 0V and 1= 10 V. Calculate the output that has a digital input 11010.Can output reach 10V.If yes, for what digital input combination.	4