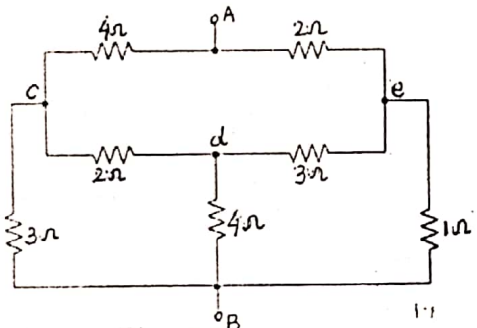
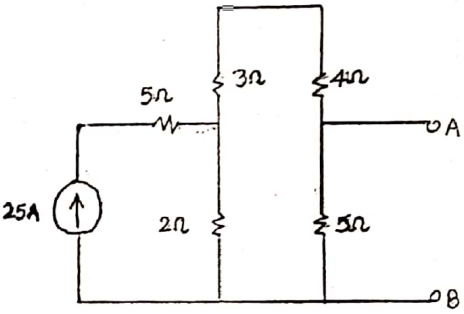
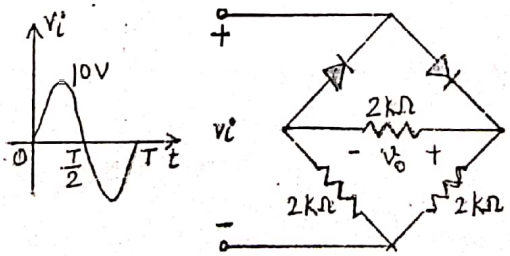
PUNJAB ENGINEERING COLLEGE
(Deemed to be University)
Mid-Term Examination, Feb, 2019

Programme: B.Tech (ECE)
Course Name: Analog Electronic Circuit -I
Maximum Marks: 40

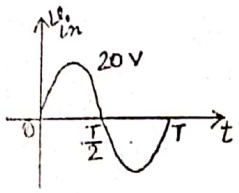
Year/Semester: First/2nd
Course Code: ECN 102
Time allowed: 1 hr 30 min

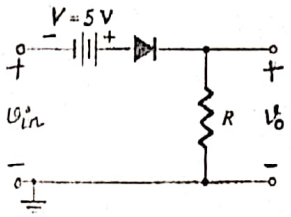
Notes:

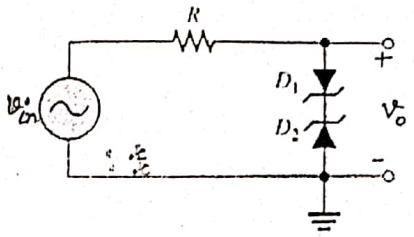
1. All questions are compulsory.
2. Unless stated otherwise, the symbols have their usual meanings in context with subject. Assume suitably and state, additional data required, if any.
3. STUDENT ARE NOT ALLOWED TO SHARE THE CALCULATOR.

Q. No		Marks
1 a)	Obtain the equivalent resistance between nodes A and B by doing star to delta conversion in the circuit shown in Fig.1.1.	3
b)	Determine the Norton's equivalent circuit (across AB) for the given circuit in fig. 1.2	3
	 Fig. 1.1  Fig. 1.2	
2 a)	What are the differences between p-n diode and Schottky diode? Why Schottky diode is suitable for high frequency applications?	3
b)	Enlist the differences between Zener breakdown and Avalanche breakdown.	3
c)	What makes tunnel diode to operate at low forward biases? Explain with the help of energy band diagram.	2
3 a)	Sketch the output voltage for the network and determine the average output voltage. Assume diodes to be ideal.	5
		

b)	Sketch the output waveforms for the given circuits. Show the equivalent circuits during positive and negative half cycles. Consider diodes to be non-ideal. For fig 3.2(b) circuit, Zener voltage of both diodes is 5V.	5

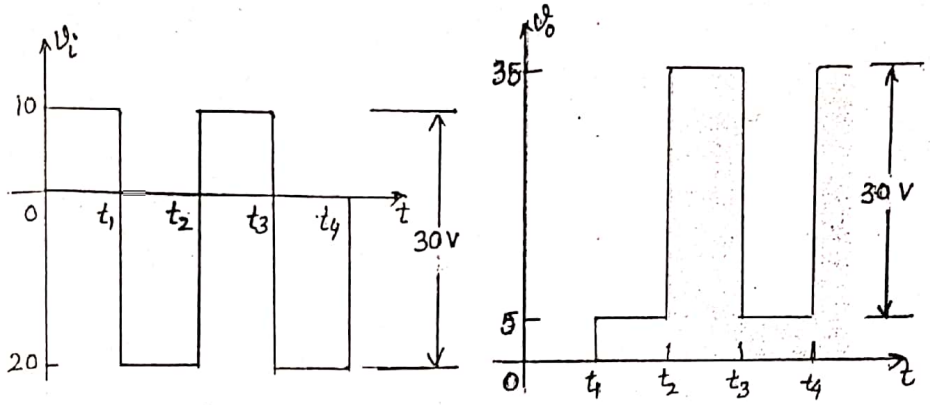






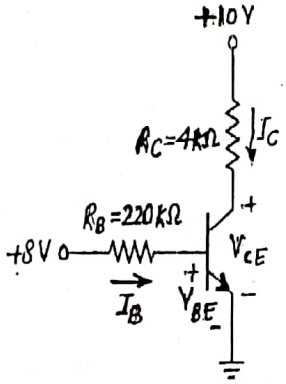
3.2 (a) 3.2 (b)

c)	Design a clamper circuit which can perform the function indicated.	3



Input Output

4 a)	Explain the collector current in CE configuration, when (i) I_B=0 (ii) I_E=0. Also draw the circuit for both the cases.	4
b)	Calculate I_C, I_B and V_{CE} for the given circuit. The transistor parameters are: ß=100 and V_{BE} = 0.7V. If the transistor is biased in saturation, assume V_{CE} (sat) = 0.2V.	4



(a)

c)	Design (calculate R_E and R_C) a pnp transistor in common base configuration such that I_E= 0.50 mA and V_{EC} = 4.0 V. Assume transistor parameters of ß=120 and V_{EB} = 0.7 V, R_B=10 Kohms. Also draw the circuit.	5

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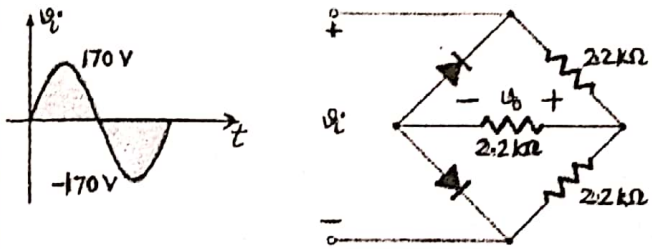
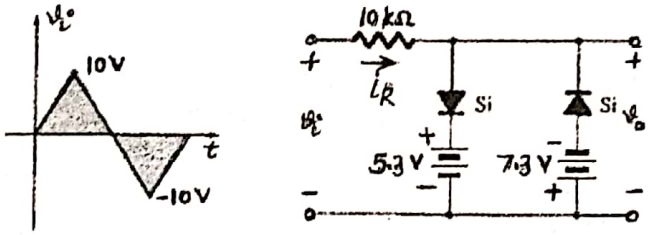
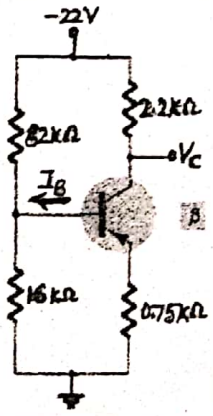
Punjab Engineering College
(Deemed to be University)
End-Term Examination
April-May 2019

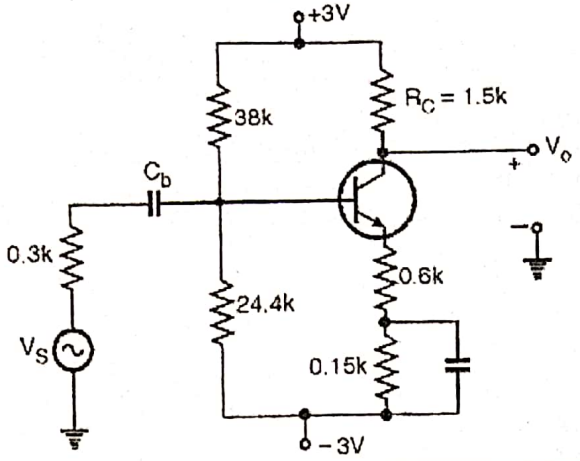
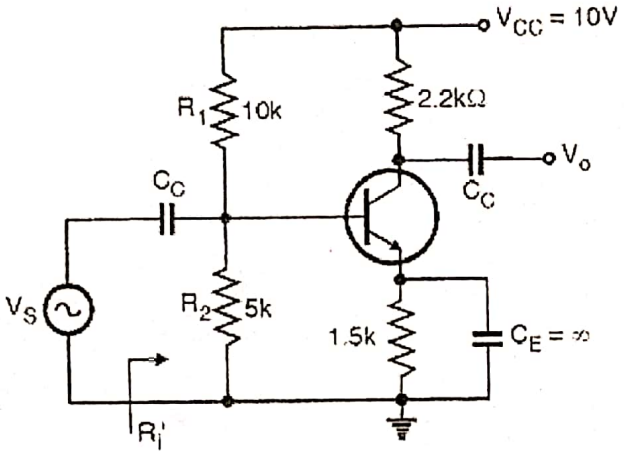
Programme: **B.E (Electronics & Communication)**
Course Name: **Analog Electronic Circuits-I**
Maximum Marks: **80**

Year/Semester: **First/2nd**
Course Code: **ECN 102**
Time allowed: **3 Hours**

Notes:

1. All questions are compulsory.
2. Unless stated otherwise, the symbols have their usual meanings in context with subject. Assume suitably and state, additional data required, if any.
3. The candidates, before starting to write the solutions, should please check the question paper for any discrepancy, and also ensure that they have been delivered the question paper of right course code.

Q. No			Marks
1	(a)	 Calculate the average output voltage for the above rectifier. Assume diodes to be non-ideal. (Show the equivalent circuit during both half cycles)	5
	(b)	a) Sketch i_R and v_o for the network below for the input shown. 	5
	(c)	Write a short notes on Light emitting diode.	4
2	(a)	Determine V_{CEQ}, I_{CQ} and I_{BQ} for the given circuit. ($\beta = 220$) 	6
	(b)	If β increase to 135, what will be the percentage change in operating point collector voltage and current?	4
	(c)	Draw and explain input output characteristics of common collector configuration. Why this configuration is commonly known as emitter follower?	6

3	(a)	The transistor has h_{ie} = 2.5 K , h_{fe}=200 and R_L=1 K. Calculate overall voltage gain. Assume h_{re}= h_{oe}=0. Illustrate the small signal equivalent of the amplifier. 	5
	(b)	For the above circuit if C_{be}= 36 pF, C_{bc}= 4 pF, C_{ce}= 1 pF, C_{wi}= 6 pF and C_{wo}= 8 pF, determine high cut off frequency. Draw the frequency response.	6
	(c)	For the transistor amplifier shown find h_{ie} and h_{fe} if device voltage gain A_V = -150 and R_i'= 1K. Assume h_{re}= h_{oe}=0. 	5
	(d)	If C_c(input) = 10 uF and C_c(output)= 1uF, find out the lower cut off frequency. (ignore cut off frequency due to emitter bypass capacitor)	5
4	(a)	Show the structure of a JFET and MOSFET and list the differences. Describe why input impedance of an FET is very high.	5
	(b)	Differentiate between an FET and BJT.	4
	(c)	For an N channel JFET drain current with gate shorted = 10 mA, pinch off voltage = -6 V. sketch two characteristic curves for this JFET corresponding to V_{GS} = 0 V and V_{GS} = -2V.	4
5	(a)	Show that maximum conversion efficiency of class B push pull amplifier circuit is 78.5%. Draw its circuit as well.	6
	(b)	A transformer coupled class A amplifier draws a current of 200 mA from a collector supply of 10 V, when no input signal is applied to it. Assuming that amplifier is set to deliver maximum power to the load, so determine (i) maximum output ac power (ii) maximum conversion efficiency (iii) power dissipated.	6
	(c)	Briefly describe harmonic distortion in power amplifiers.	4