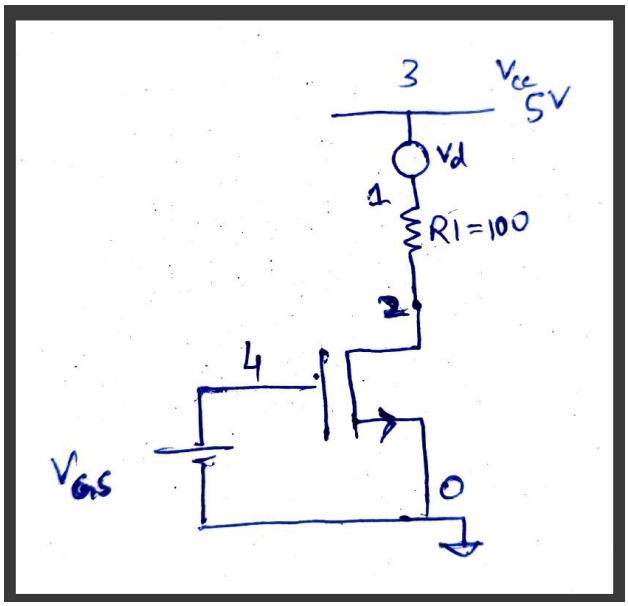
Devices and Circuits Laboratory
Experiment-4
NMOS Common Source Amplifier Characteristics

Group : 1
Aditya Kalyani - 200020003
Tanish H Talapaneni - 200020050

Software Simulation

Q1:



Q2:

Netlist

Question-2

Vcc 3 0 5V
Vgs 4 0 5V
Vd 3 1 0
R1 1 2 100
M1 2 4 0 0 MN4007

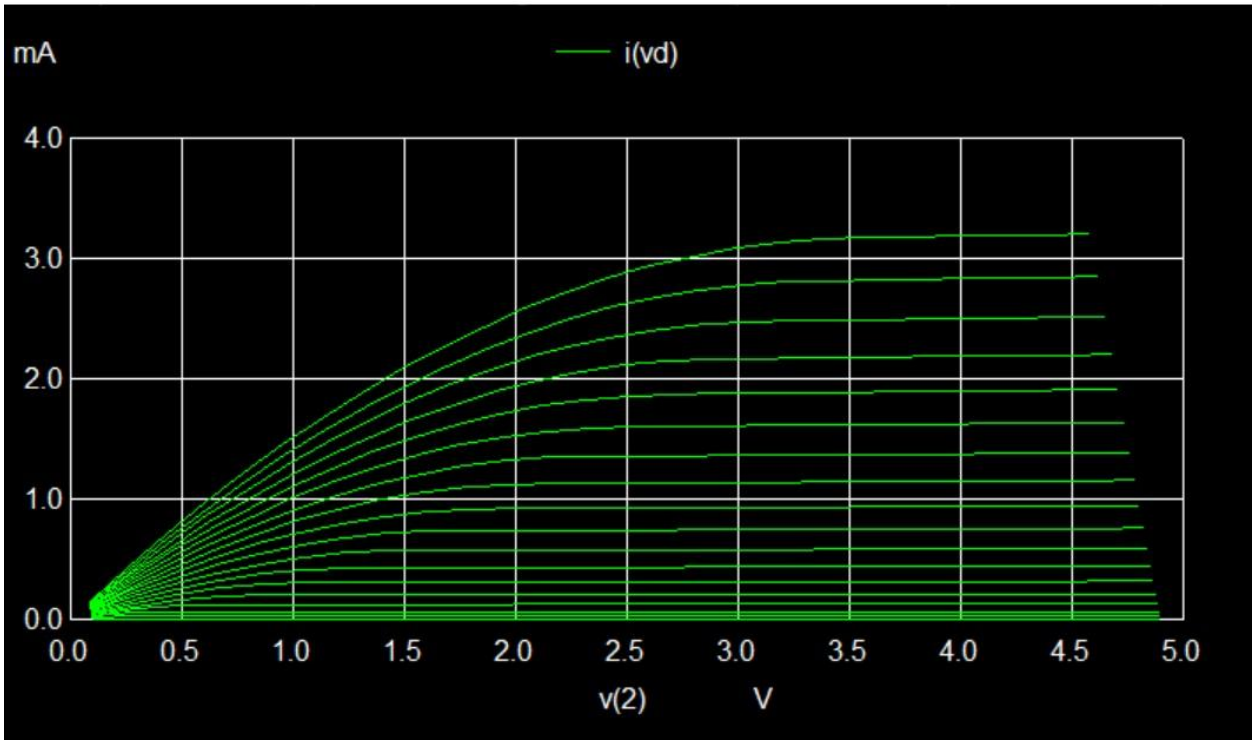
.model MN4007 NMOS(Kp=500u Vto=1.5 Lambda=0.01 Gamma=0.6 Tox=1200n Phi=.6 Rs=0 Rd=0 Cbd=2.0p Cbs=2.0p Pb=.8 Cgso=0.1p Cgdo=0.1p Is=16.64p)

.dc Vcc 0.1 5 0.2 Vgs 0 5 0.2
*.tran 0.001ms 1ms
.control
run

plot i(Vd) vs v(2)
plot v(2)/i(Vd)

.endc
.end

Q3:
Plots:



Q4:

a) From graph, we observe:

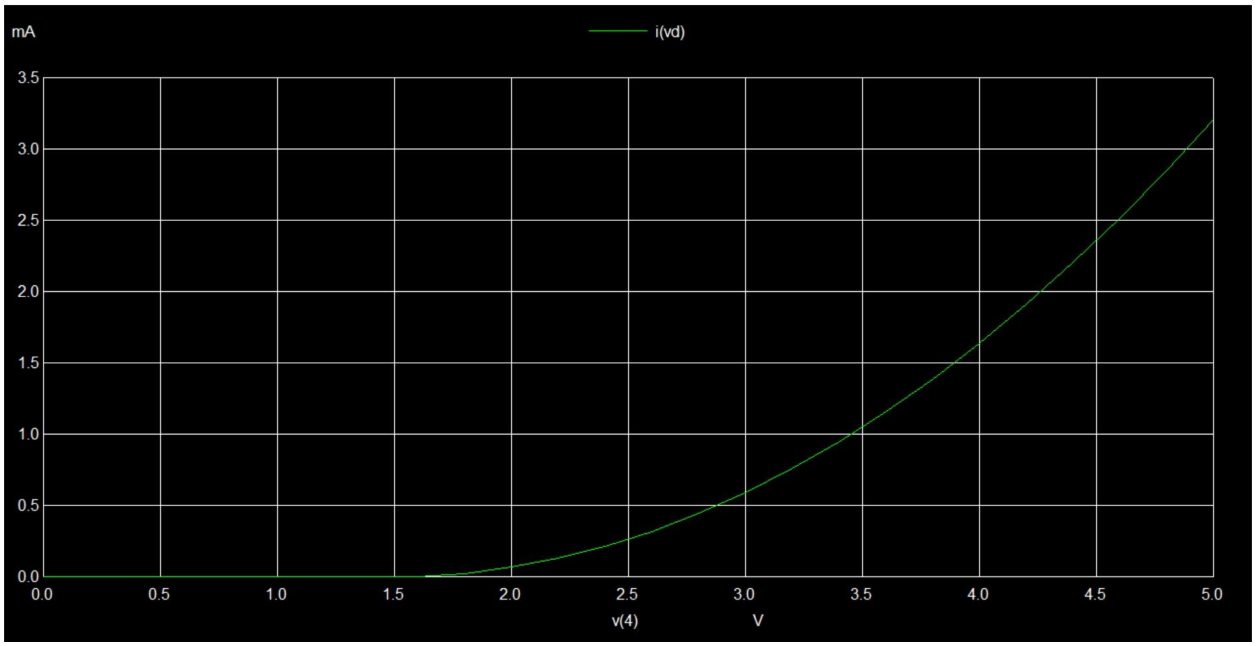
Vgs(V)	Rds(k-ohm)
1.1	846
1.2	943
1.4	1074
1.6	1217
1.7	1706

b) r0 in saturation region

Vgs(V)	r0(M-ohm)
1.1	6.2
1.2	9.4
1.4	11.9
1.6	15.5
1.7	18.6

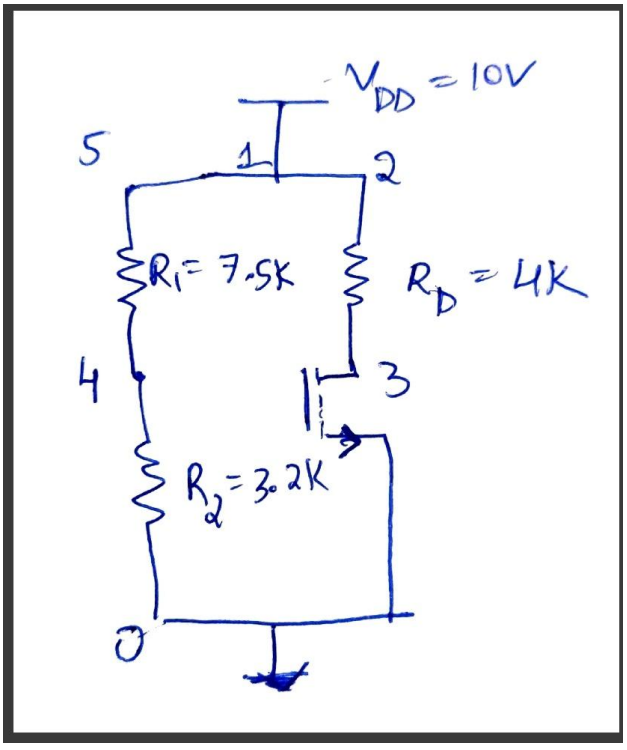
Q5:
Question 5

```
Vcc 3 0 5V
Vgs 4 0 5V
Vd 3 1 0
R1 1 2 100
M1 2 4 0 0 MN4007

.model MN4007 NMOS(Kp=500u Vto=1.5 Lambda=0.01 Gamma=0.6 Tox=1200n Phi=.6 Rs=0
Rd=0 Cbd=2.0p Cbs=2.0p Pb=.8 Cgso=0.1p Cgdo=0.1p Is=16.64p)

.dc  Vgs 0 5 0.2
*.tran 0.001ms 1ms
*Vcc 0.1 5 0.2
.control
run

plot i(Vd) vs v(4)
.endc
.end
```



Thus, from the plots, we conclude threshold voltage= 1.85V

Q6:



```
Circuit: question 6

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

No. of Data Rows : 1
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

i(vd) = 5.977808e-04
v(3) = 7.608877e+00
v(4) = 2.990654e+00
i(vd1) = 9.345794e-04
```

Q7:
Netlist:
Question 7

Vdd 1 0 10
vd 1 2 0
rd 2 3 4k
vd1 1 5 0
r1 5 4 7.5k
r2 4 0 3.2k
M1 3 4 0 0 MN4007

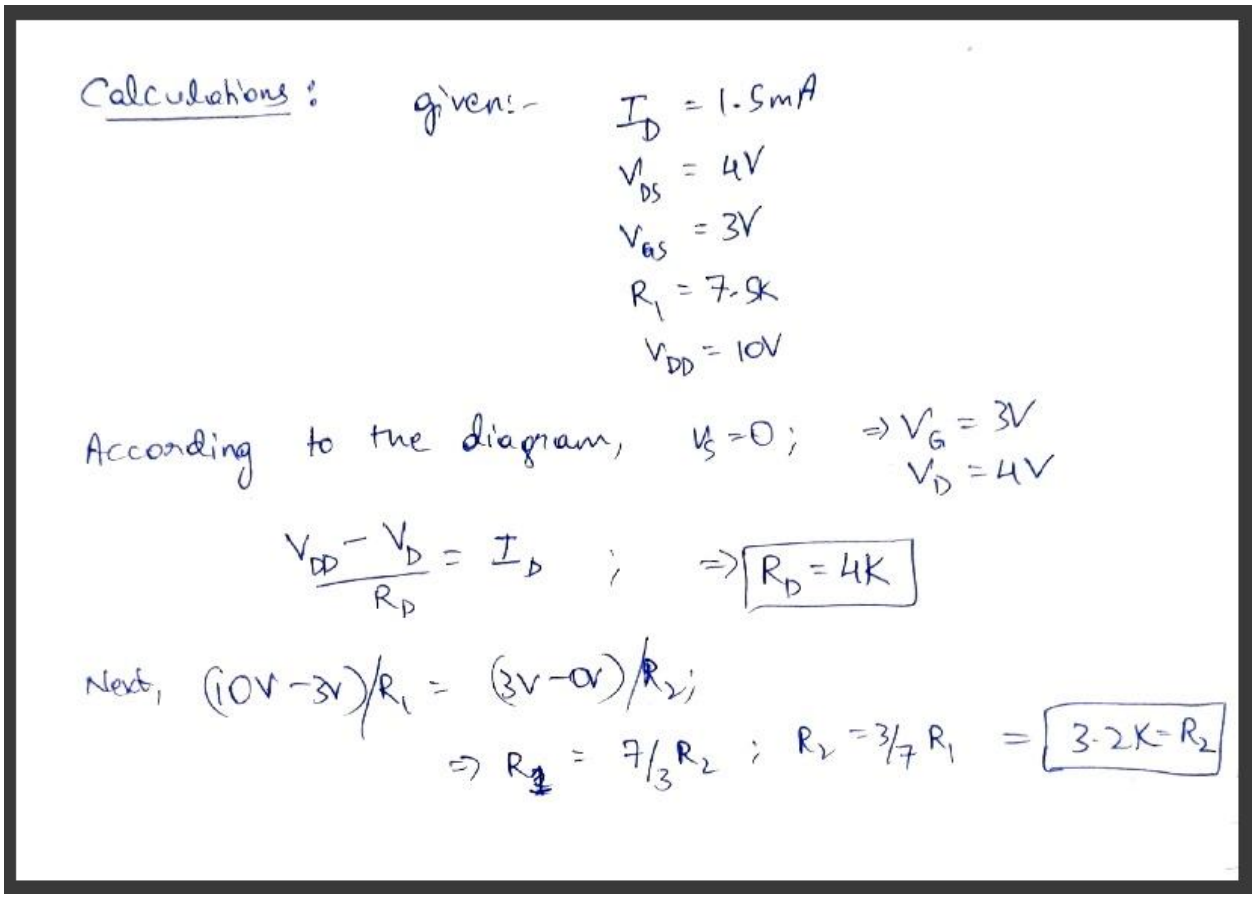
.model MN4007 NMOS(Kp=500u Vto=1.5 Lambda=0.01 Gamma=0.6 Tox=1200n Phi=.6 Rs=0 Rd=0 Cbd=2.0p Cbs=2.0p Pb=.8 Cgso=0.1p Cgdo=0.1p Is=16.64p)

.control
op
run

print i(vd) v(3) v(4) i(vd1)

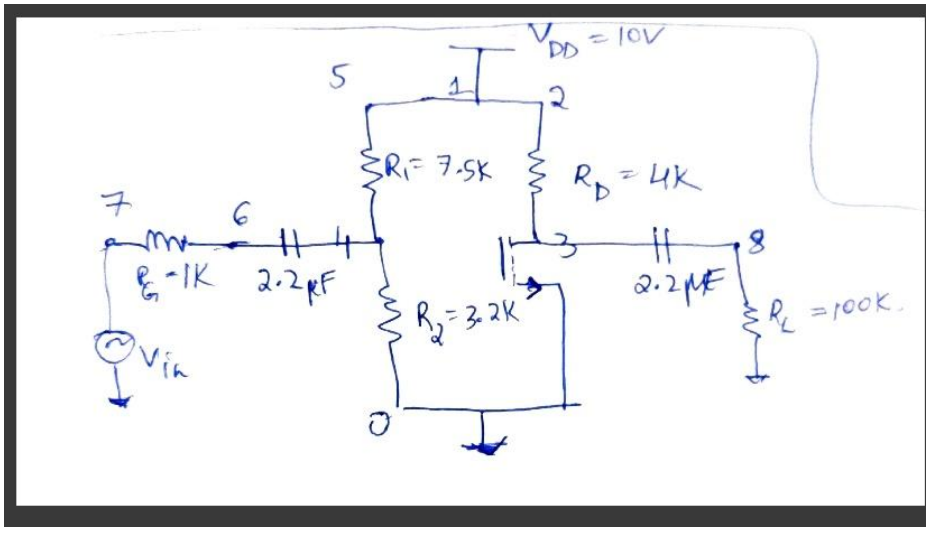
.endc
.end

Q8:
Calculations:



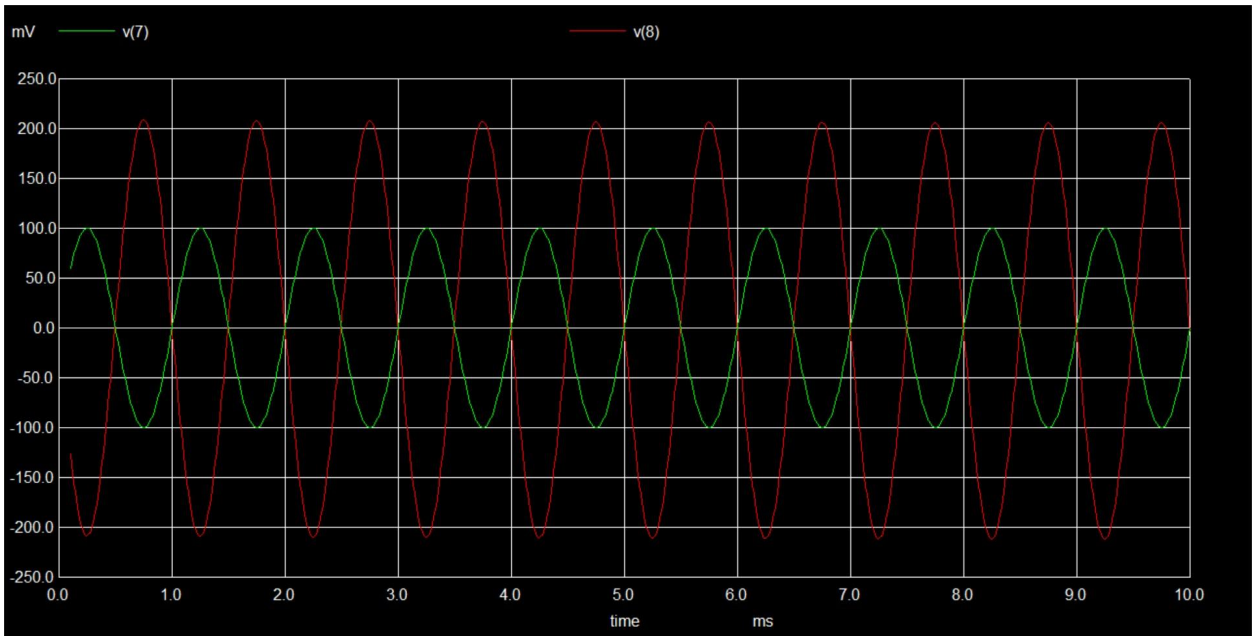
Values obtained from simulation:
id= 0.6 mA
Vout= 7.6V
Vin= 3V
i(R1)= 0.93mA

Q9:

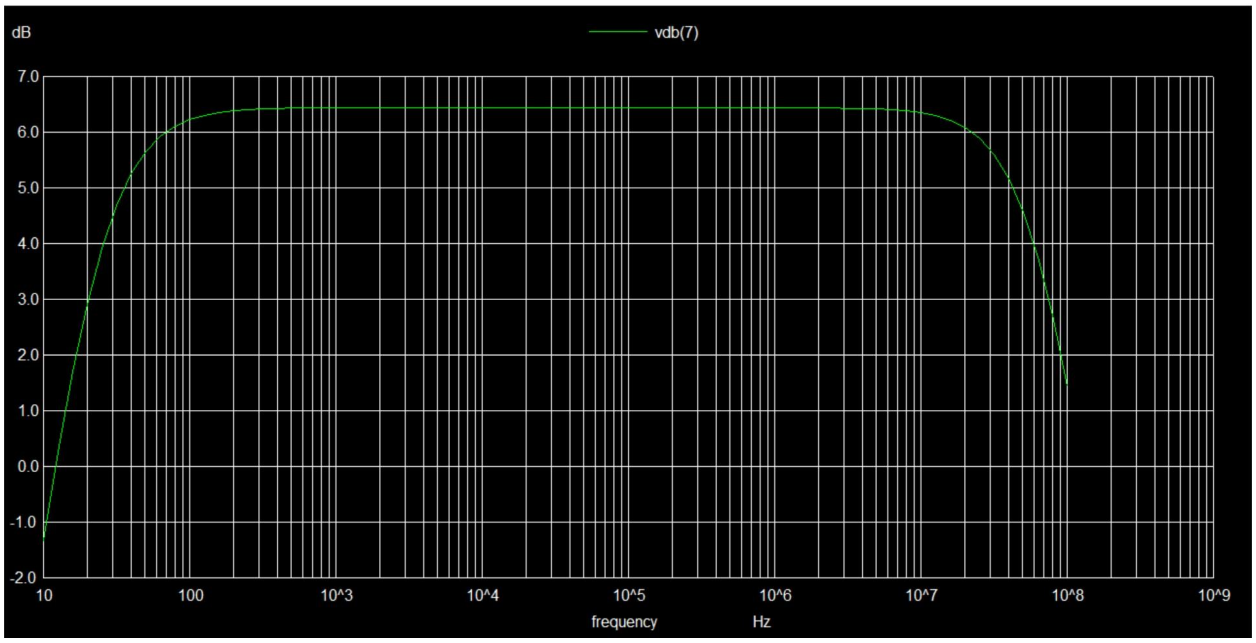


Question 9

```
Vdd 1 0 10
vd 1 2 0
rd 2 3 4k
vd1 1 5 0

r1 5 4 7.5k
r2 4 0 3.2k
c1 4 6 2.2u
c2 3 8 2.2u
rl 8 0 100k
rg 6 7 1k

vin 7 0 sin (0 100m 1k 0 0 0)

M1 3 4 0 0 MN4007

.model MN4007 NMOS(Kp=500u Vto=1.5 Lambda=0.01 Gamma=0.6 Tox=1200n Phi=.6 Rs=0
Rd=0 Cbd=2.0p Cbs=2.0p Pb=.8 Cgso=0.1p Cgdo=0.1p Is=16.64p)
.tran 0.01ms 10ms 0.1ms
.control
op
run

plot v(7) v(8)
.endc
.end
```

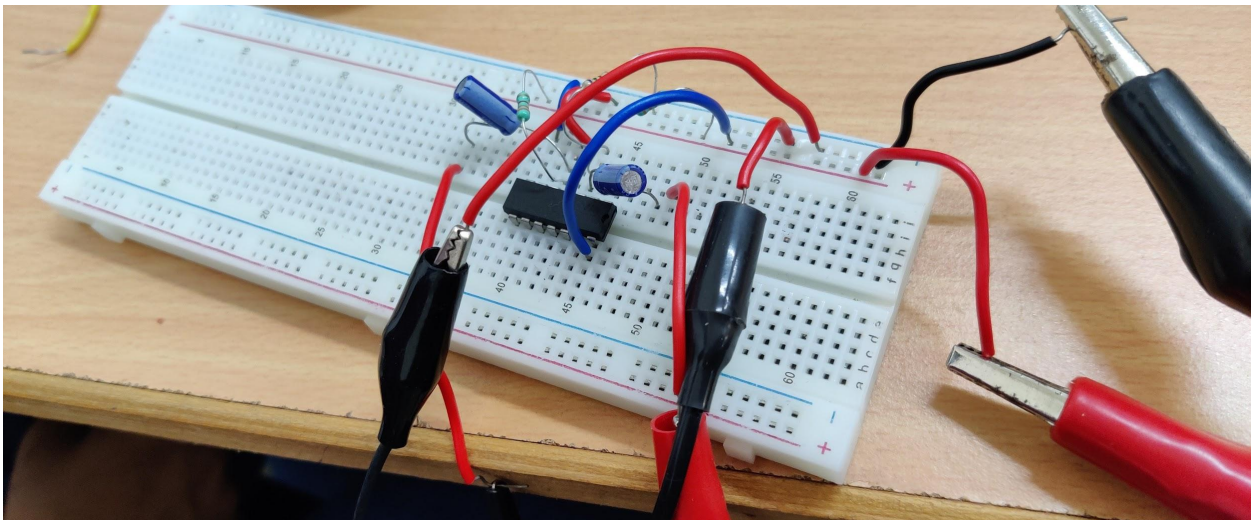


Q10: Frequency Response of Amplifier:



Hardware Simulation

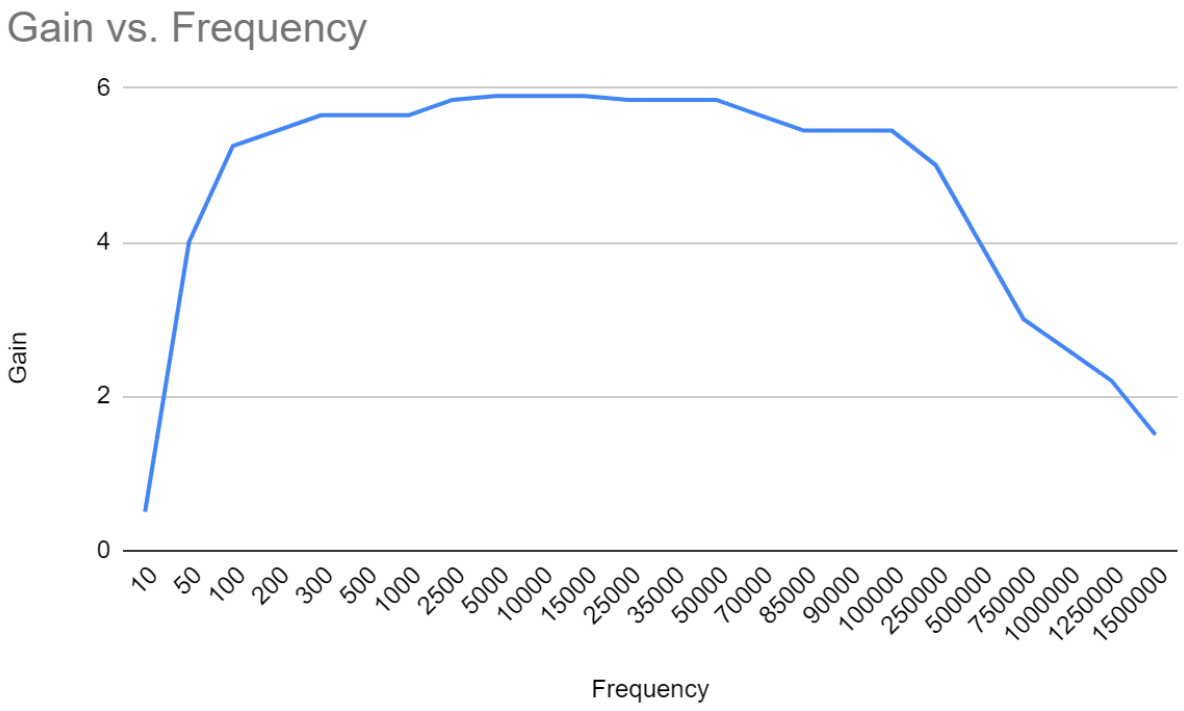
Breadboard Connections:



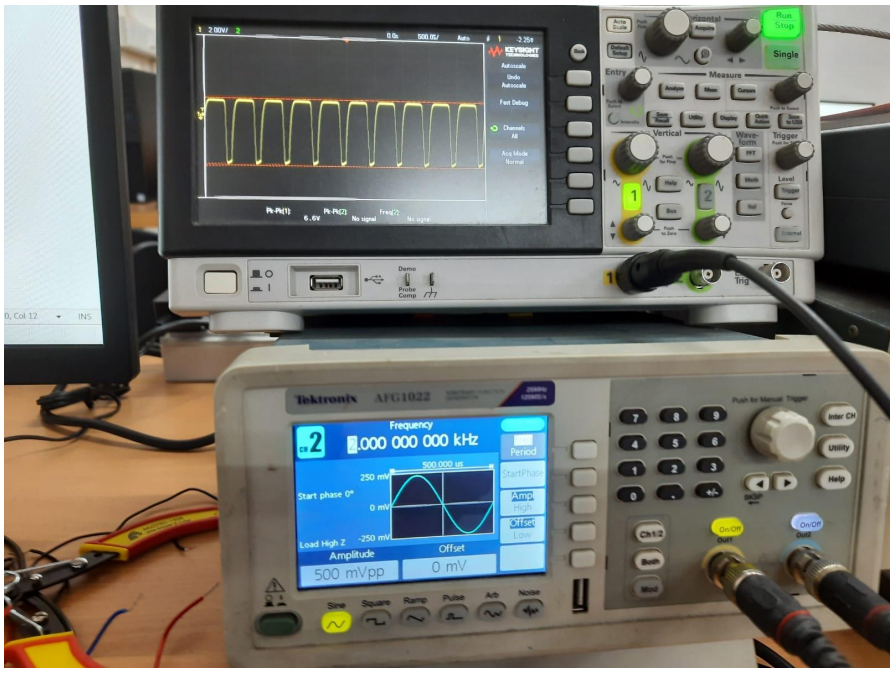
Reading:

Q4:
Observations:

Input(V)	Output(V)	Frequency(Hz)	Gain
0.2	0.1	10	0.5
0.2	0.8	50	4
0.2	1.05	100	5.25
0.2	1.09	200	5.45
0.2	1.13	300	5.65
0.2	1.13	500	5.65
0.2	1.13	1000	5.65
0.2	1.17	2500	5.85
0.2	1.18	5000	5.9
0.2	1.18	10000	5.9
0.2	1.18	15000	5.9
0.2	1.17	25000	5.85
0.2	1.17	35000	5.85
0.2	1.17	50000	5.85
0.2	1.13	70000	5.65
0.2	1.09	85000	5.45
0.2	1.09	90000	5.45
0.2	1.09	100000	5.45
0.2	1	250000	5
0.2	0.8	500000	4
0.2	0.6	750000	3
0.2	0.52	1000000	2.6
0.2	0.44	1250000	2.2
0.2	0.3	1500000	1.5



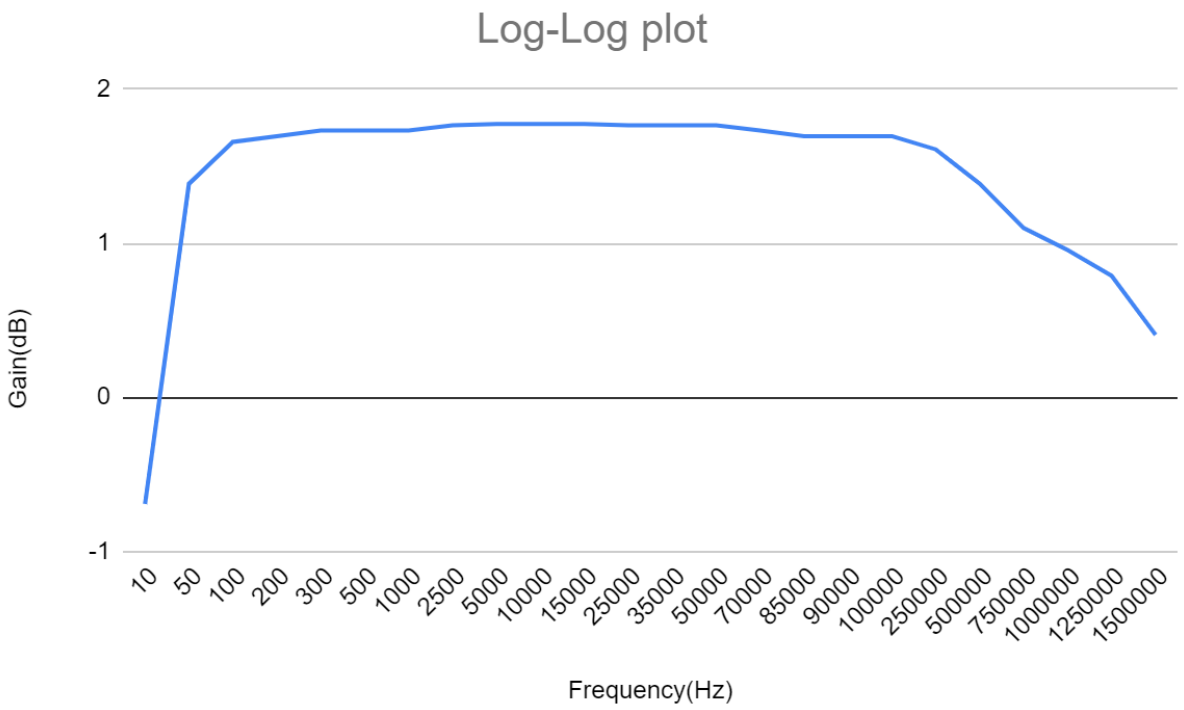
Q5: Simulation bw $200mV_{P-P}$ and $2V_{P-P}$



Yes, the output signal gets distorted because we exceed the limits of the diode parameters. The diode reaches saturation and thus, the corresponding output gets trimmed.

Q6:

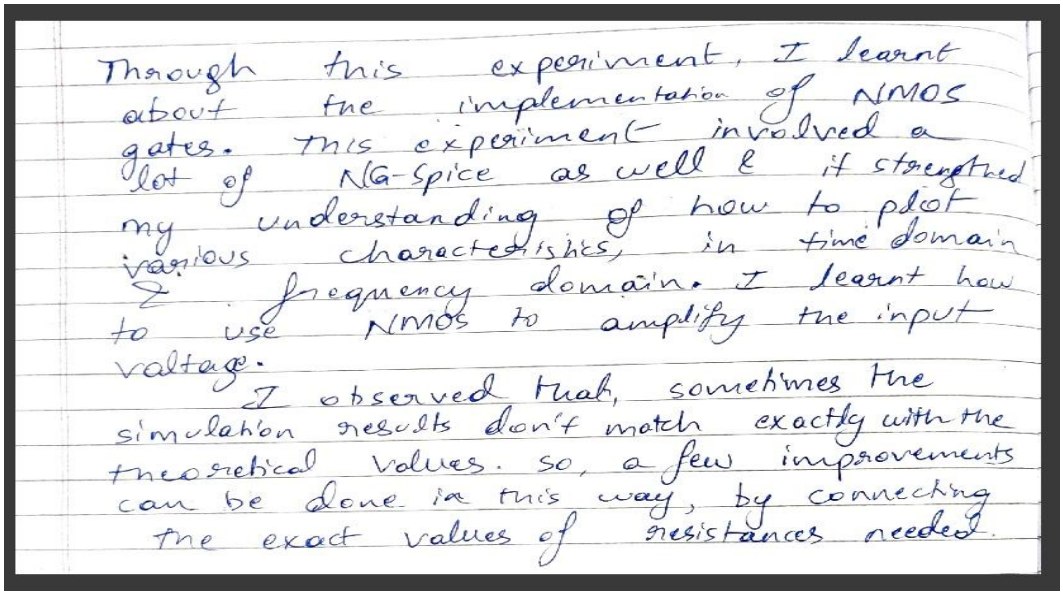
Log-Log Plot:



We observe that the gain vs frequency graph is plateau shaped. Within a large range of frequencies in between, the gain remains almost constant and then drops off for higher frequencies.

Discussion:

Tanish H Talapaneni:


Through this experiment, I learnt about the implementation of NMOS gates. This experiment involved a lot of NG-Spice as well & it strengthened my understanding of how to plot various characteristics, in time domain ⇒ frequency domain. I learnt how to use NMOS to amplify the input voltage.

I observed that, sometimes the simulation results don't match exactly with the theoretical values. So, a few improvements can be done in this way, by connecting the exact values of resistances needed.

Aditya Kalyani:

Discussion :-

Through the following experiment, I gained an practical insight of implementation of a NMOS circuit. I learnt to write a netlist for a simple common source amplifier. I saw the Id vs Vds graph for a simple common source amplifier after simulation which matched the theoretical graph. From this I understood the characteristics of Id vs of the NMOS circuit. I also understood the graph for various values of Vgs, the saturation current, cutoff voltage etc. I learnt estimation of threshold voltage from the graph. I also learnt to design a common source amplifier and found out the gain of the circuit and various other parameters. Then for a specified load and input capacitance, fo. I understood the small signal gain of the circuit at a specific frequency. Also I found out the gain of the circuit for a range of frequencies from which I understood the behaviour of the gain fo(a circuit) for a wide frequency range.

Practically designing, I learnt the way to choose various resistor and capacitance values for a required gain and output. I also saw how the voltage clipping happens when the output goes higher then a specific value.

I had a great working time with all the hardware components, which strengthened my knowledge and confidence on working with MOS circuits. It was a great experience working with a fabricated Ic. I learnt a lot by this experiment.