DIGITAL CIRCUITS LABORATORY
Experiment-10
Asynchronous Counters

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Aim: To design a circuit for a mod-8 Asynchronous up-counter and a mod-6 Asynchronous up-counter, using only NAND gates(if required)

Summary: Implementation of the mod-8 Asynchronous up-counter and a mod-6 Asynchronous up-counter

Components used: SN-5476(JK Flip-flop), LED Display, Breadboard, Power supply, Arbitrary Function Generator, 1k ohm resistor.

Procedure:

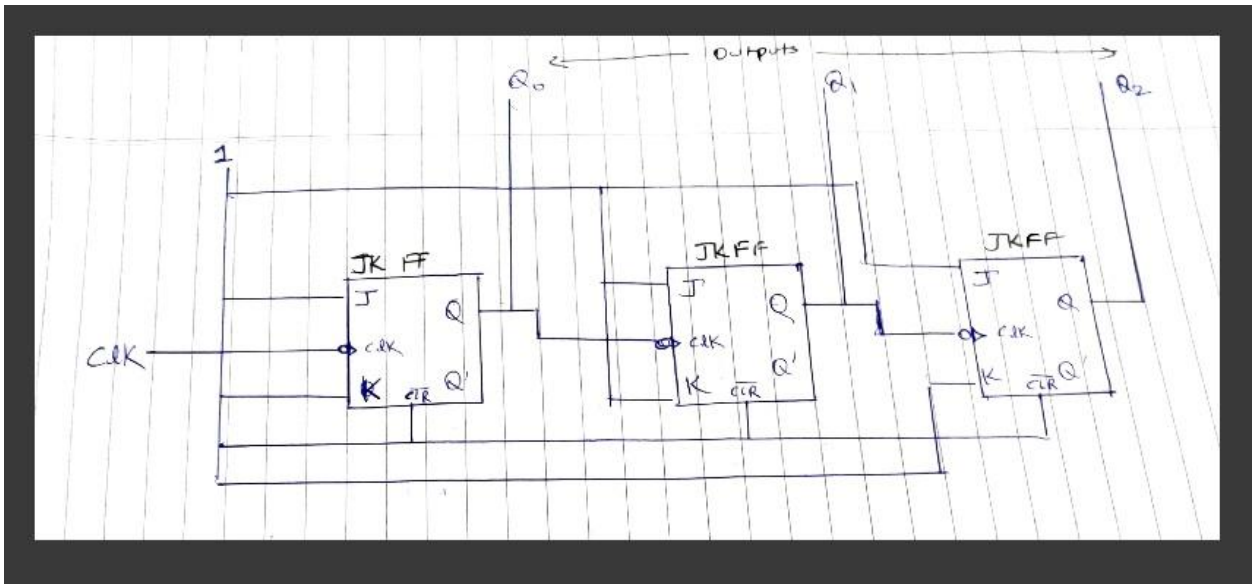
- Connect the circuit as shown in diagrams and give it power input.
- Give Clock signal to the circuit using the AFG with frequency between 1-2Hz
- Glowing LED implies that output was 1, otherwise 0.
- Verify if the simulation matches with the expected values.

Logic Design:
Mod-8 design is the same as the regular asynchronous up-counter which consists of 3 JK Flip-flops.

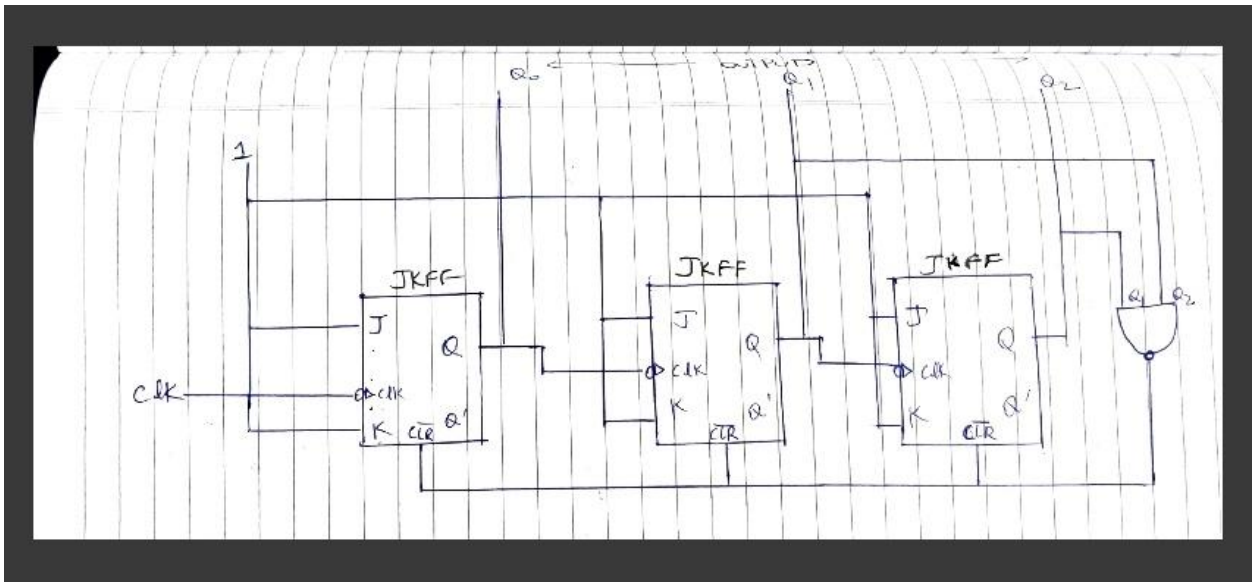
Meanwhile, in order to obtain the mod-6 design, we keep in mind that Decimal-6 and Decimal-7 should not appear as output. Q_2 and Q_1 both are 1 only in these two cases. Thus NAND of Q_2 and Q_1 is 0 only for this case

Gate Design:

Mod-8 Asynchronous up-counter:

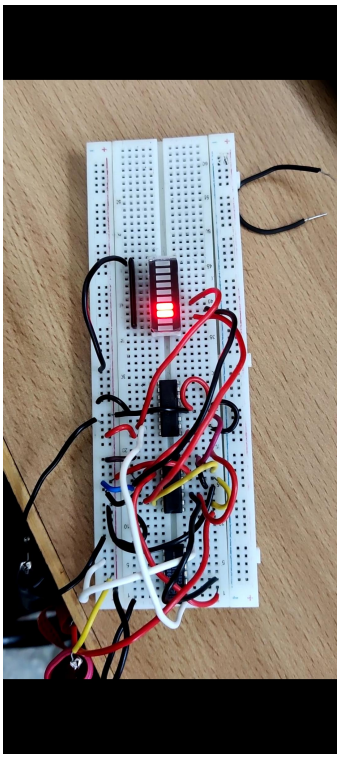


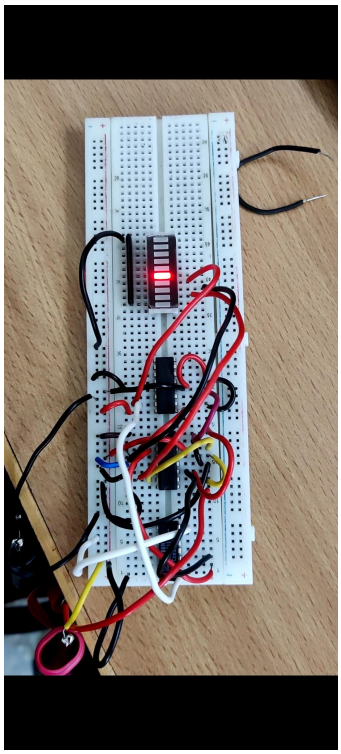
Mod-6 Asynchronous up-counter:

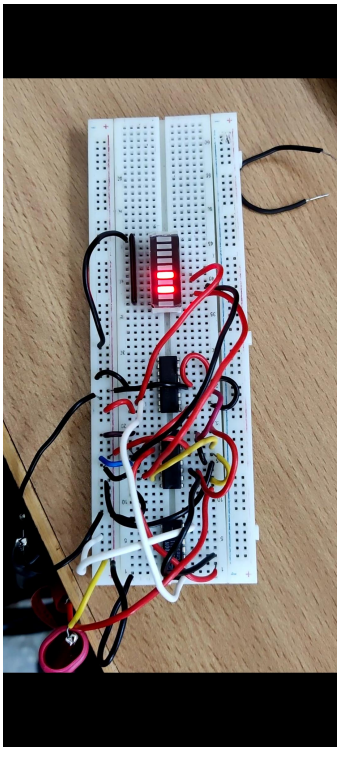


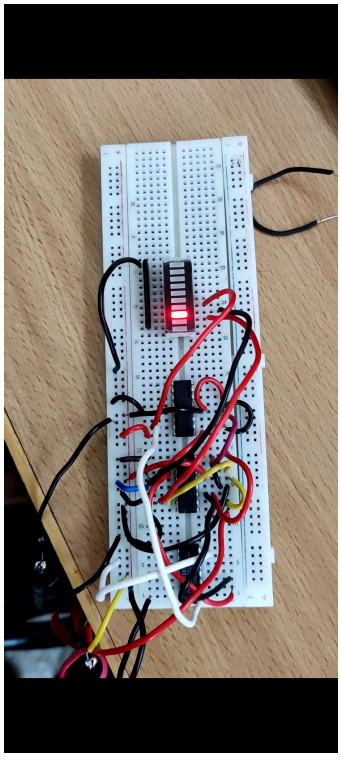
Hardware:

Mod-6 Asynchronous up-counter:

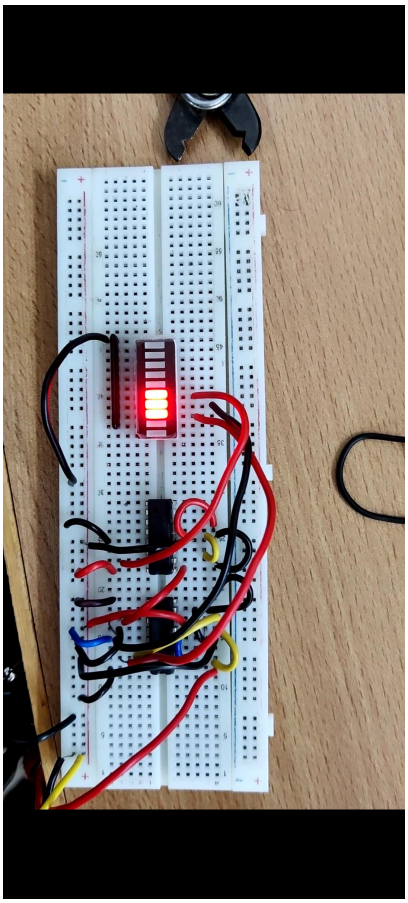
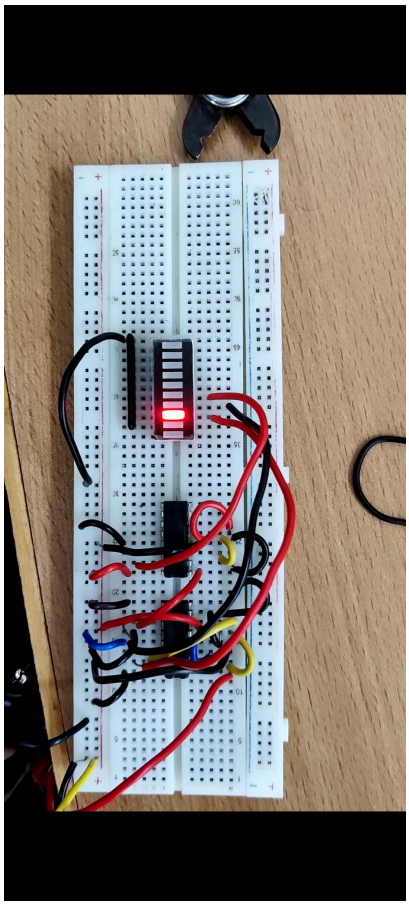
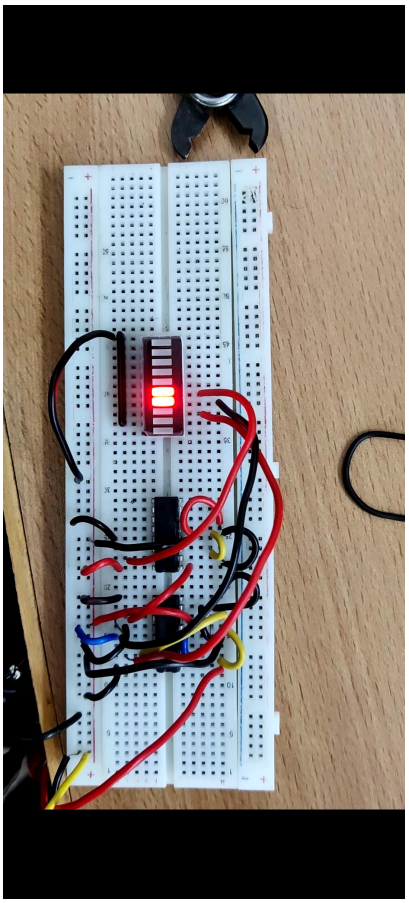
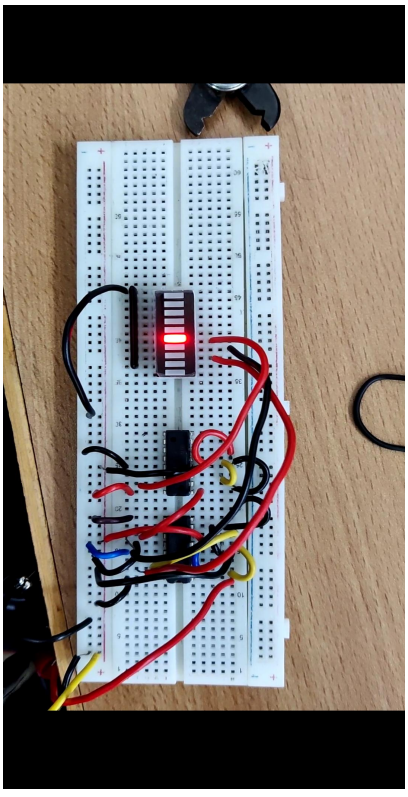
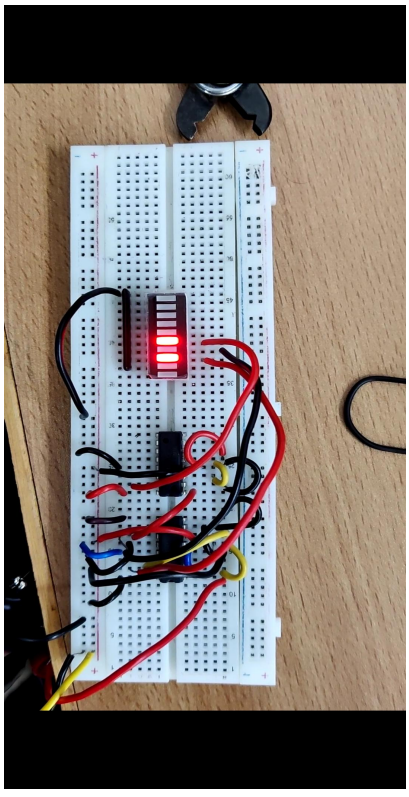
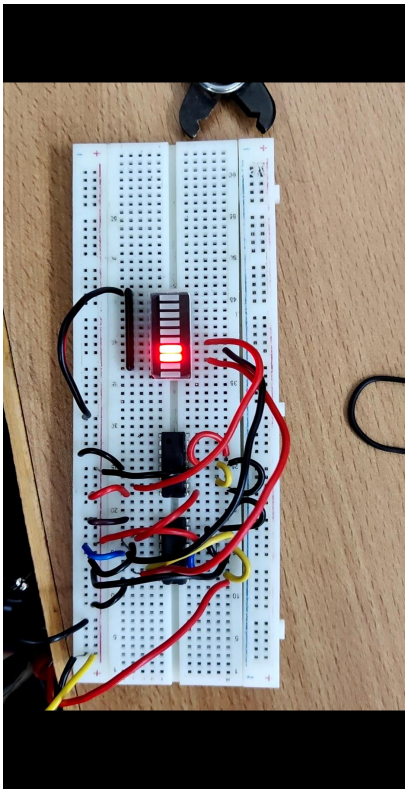








Mod-8 Asynchronous up-counter:

Results and Discussions: We finally understood how to practically implement the Mod-8 and Mod-6 Asynchronous up-counters. The mod-6 design was a little more complicated compared to the mod-8 design, but the changes involved were less. We had to use the Arbitrary Function Generator with appropriate frequency in order to generate the clock signal. The connections involved were less compared to the previous experiments. It was nice to come up with the logic in order to not display Decimal-6 and Decimal-7. Designing the circuits strengthened our understanding of gate-logic of the Asynchronous Up-counters and implementing it on the breadboard was fun.

Conclusion: I was able to verify the logic of mod-6 and mod-8 Asynchronous up-counter theoretically along with its practical implementation. It involved 3 JK Flip-Flops in series, with the Q output connected as the clock to the next flip-flops, for up-counting to work. For mod-6, NAND of Q_2 and Q_1 is 0 only for the case of Decimal-6 and Decimal-7, and 1 for other cases. Keeping this in mind, we use the output of this NAND gate as the clear signal. Clear=0 clears any present output being displayed