Report : Operational Amplifier

I. Introduction

The objective of this project is to study the internal structure of opamp in order to gain deeper insights into its working and how the circuit is synthesized. So we will be designing the three stages of the opamp namely : Differential Amplifier Stage , Gain Stage (Level Shifter) and Buffer Stage (Emitter Follower Stage). After this we will find out the various parameters of the opamp like its frequency response , CMRR,Slew Rate, Bandwidth , input and output impedance etc.

The Second part of this project will be fabricating and designing a PCB board on which the board will be practically implemented and can be used for various applications.The details on this part will be present in the second report.

The third part is still in progress and can be implemented in the future which integrates a high current gain along with the high voltage gain of the opamp in order to make a power operational amplifier which can be used to run loads on it and therefore can be used for example as an audio amplifier.

II. List of Components

The components required for this project are as follows :

1) 2N2222 NPN BJTs
2) 2N3906 PNP BJTs
3) 400p Farad Capacitor
4) 9.31 kilo ohm resistor ,4.753 kilo ohm resistor and a 20 ohm resistor
5) 1N914 diode
6) 2 Pin Screw Connector Terminal Blocks

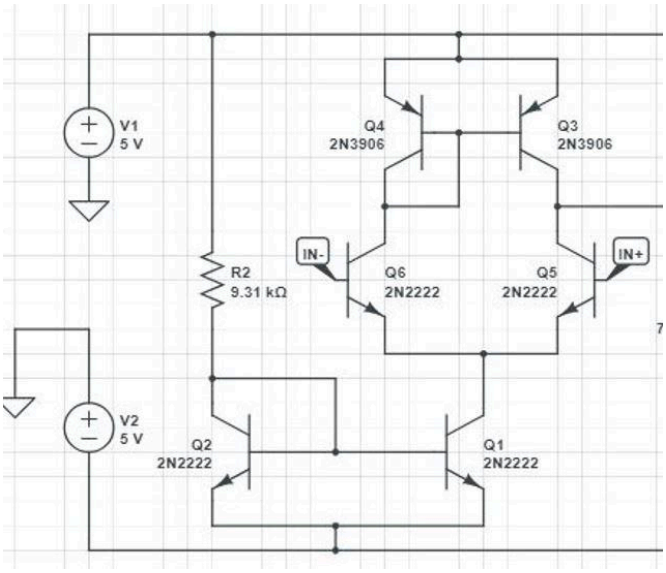
III. Three Stages of the opamp :-

Stage 0: Reference Current and Current Mirror Stage

The opamp certainly needs a power supply in order to run it and according to our design we have used a power supply of 5 volt DC because it leads to less power dissipation and also serves our need.

The stage 1 of the circuit also needs a current source in order to run and the current can be mirrored using the reference current provided.

The R2 resistor here provides the reference current and the Q1 and Q2 BJT form a current with a copied current of 1.03mA. The same has been verified with LTspice as well. This will act as the current source for the differential amplifier stage.

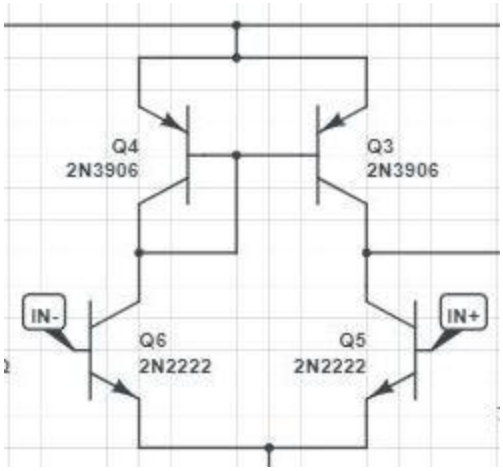


Stage1: Differential Amplifier Stage

The differential amplifier is the most widely used design in today's world ICs and it is used as stage number one in op amps because it provides high gain but that's not its primary ability ; its main task is to remove the differential noise present in the input AC signals and also remove any noise present in the DC supply of the amplifier. The differential amplifier we will be using is single ended and made of active load. Inspite of being single ended one would think its CMRR is low but its actually quite high and the same will be shown later. Also the active load is used here in order to provide high intrinsic gain.

The output of the amplifier is taken from between the collector of Q3 and Q5.

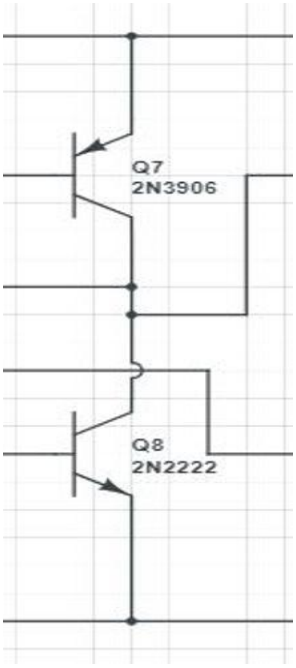
The Q4 and Q5 transistors form the active load while The AC Signal input is given via the base terminals of Q6 and Q5.
The gain of this stage is 1933.94=65.72 decibels and the output impedance is 97.57 kilo ohm.Also this gain is not the effective gain i.e. it is without considering the loading effects of input and output impedance. It will be calculated at last.



Stage2: Level Shifter Stage

The AC signal from the output of stage 1 is DC shifted and it needs to be level shifted to 0 volt DC so that the signal can swing in both positive and negative direction. Also this stage also provides a gain to the incoming signal.

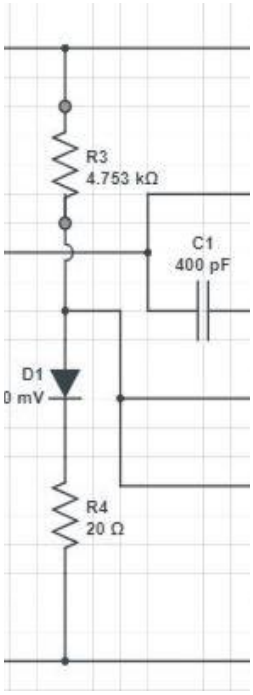
The Q8 transistor acts as a current source for the Q7 pnp transistor and also helps in achieving the high intrinsic gain along with biasing the Q7 transistor.
The base of Q8 is biased using a voltage divider circuit and should be handled carefully because even a decimal change in the base voltage of Q8 can lead Q7 BJT to go in saturation region instead of active region.
The gain of this stage is 1940.056=65.76 decibel but again this is not the effective gain. The output impedance of the stage is 61.16 kilo ohm and the input impedance is 6.3 kilo ohm.



Voltage Divider Circuit and Miller Capacitor

Used to bias both Q8 and Q10 BJT and the circuit is as follows :-

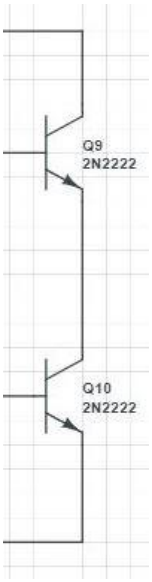
The threshold voltage of the diode ranges from 0.64 volt-0.7 volt. The Miller Capacitor is also known as compensation capacitor and it adds an extra pole in the system leaving it with one dominant pole only and therefore making the system more stable. If the compensation capacitor is not used then it leads to several break frequencies in the frequency response of the opamp and thus making it unstable for use.



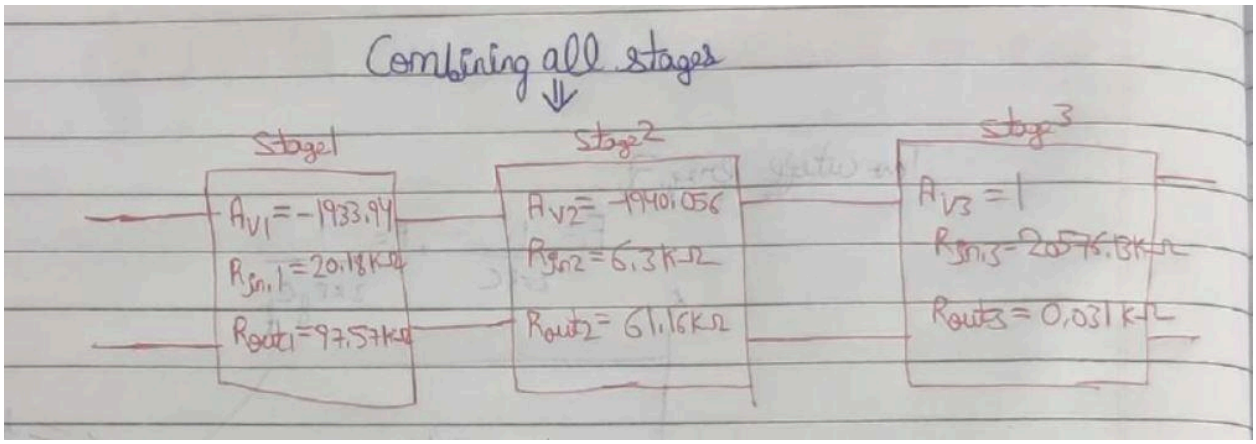
Stage3: Buffer Stage (Common Collector Stage)

The buffer stage is the last stage of the opamp and it is used in order to get rid of the loading effect as this has unity gain and low output impedance which adds to our advantage.

The input impedance of this stage is 20576.13 kilo ohm and the output impedance is 0.031 kilo ohm.



Combined Stages in order to find overall gain

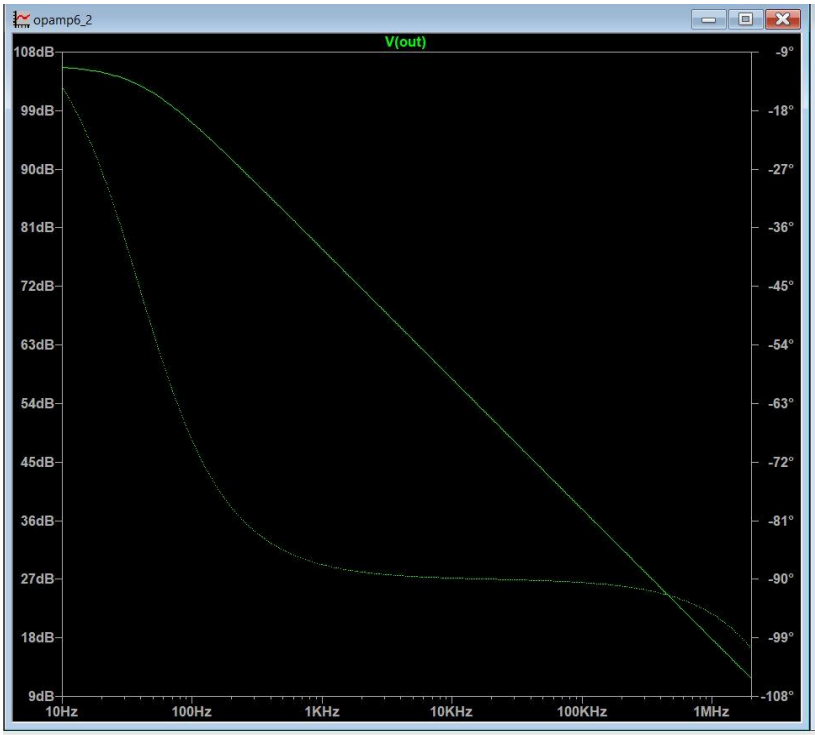


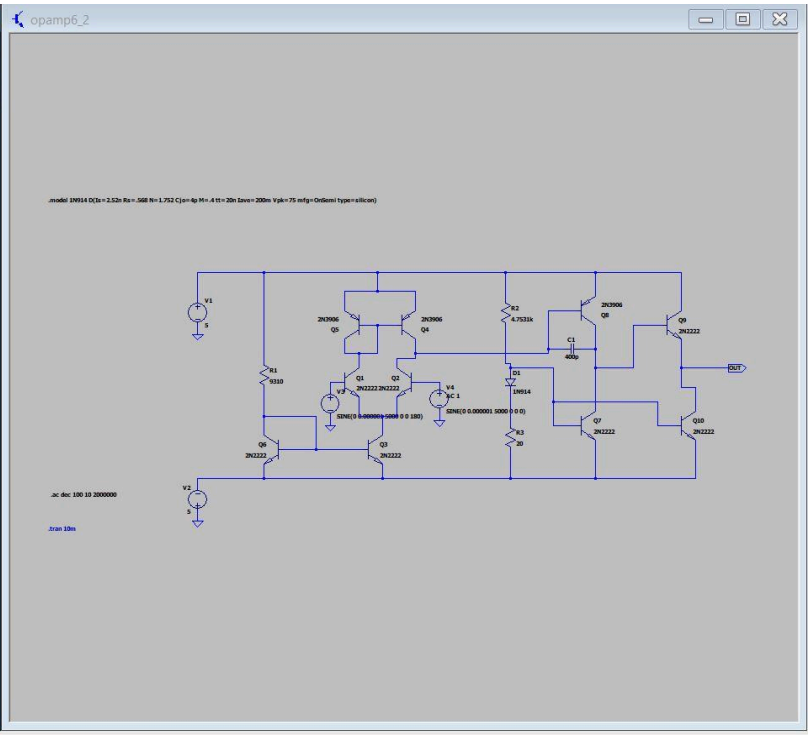
On combining all the stages we get the effective gain as 2,26,952 which is approximately 108 decibels. The whole thing has been calculated in the handwritten pdf on github.

IV. Various Parameters of Op Amp :-

1) Open Loop Gain

   The open loop gain as calculated earlier is 108 decibels and on simulating on LTspice gave a gain of around 106 decibels.

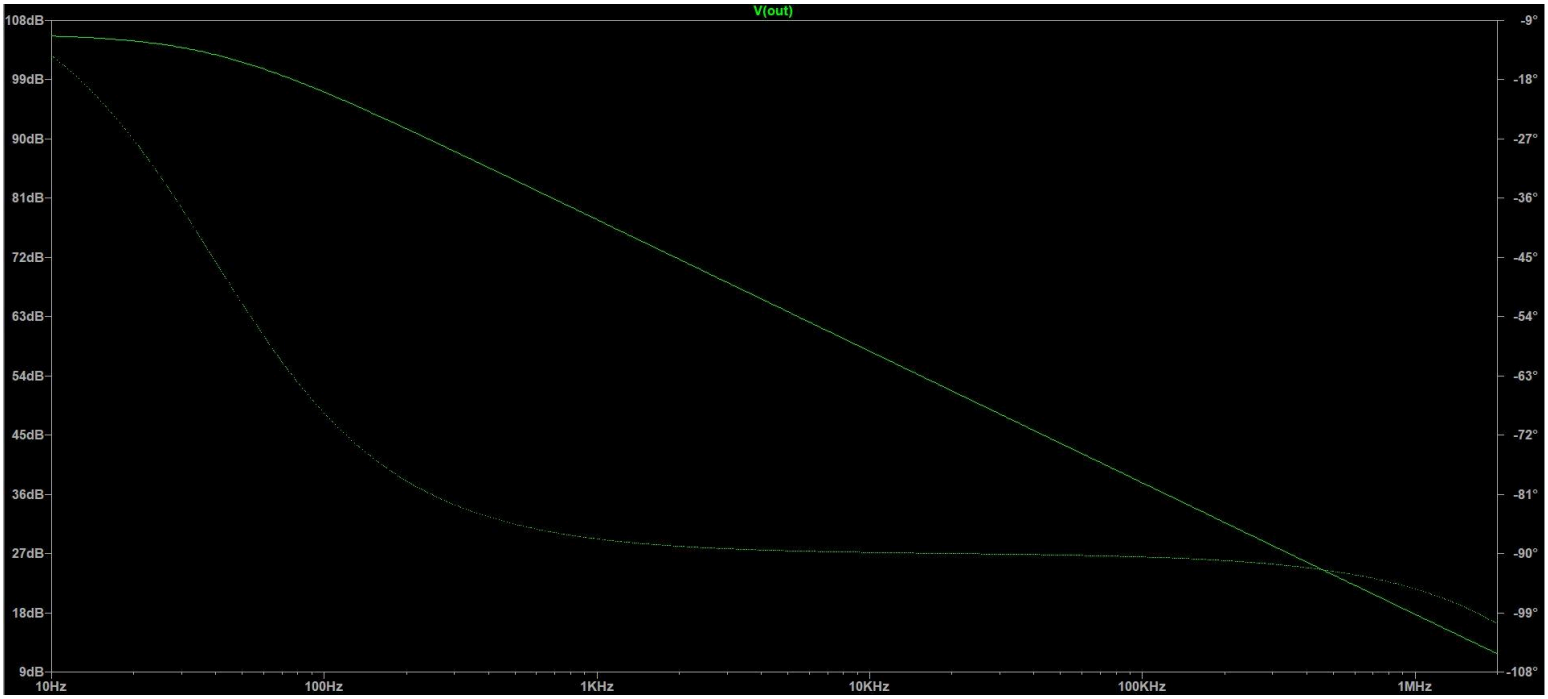




Right-Click to set up phase/group delay plotting parameters

2) Frequency Response and Bandwidth

The bandwidth of op amps is usually very small, around in the range of 100 ohms. The cut off frequency for our opamp is around 20 Hz. Also notice it is a three stage circuit still its phase response is not unstable , it is because of the compensation capacitor.



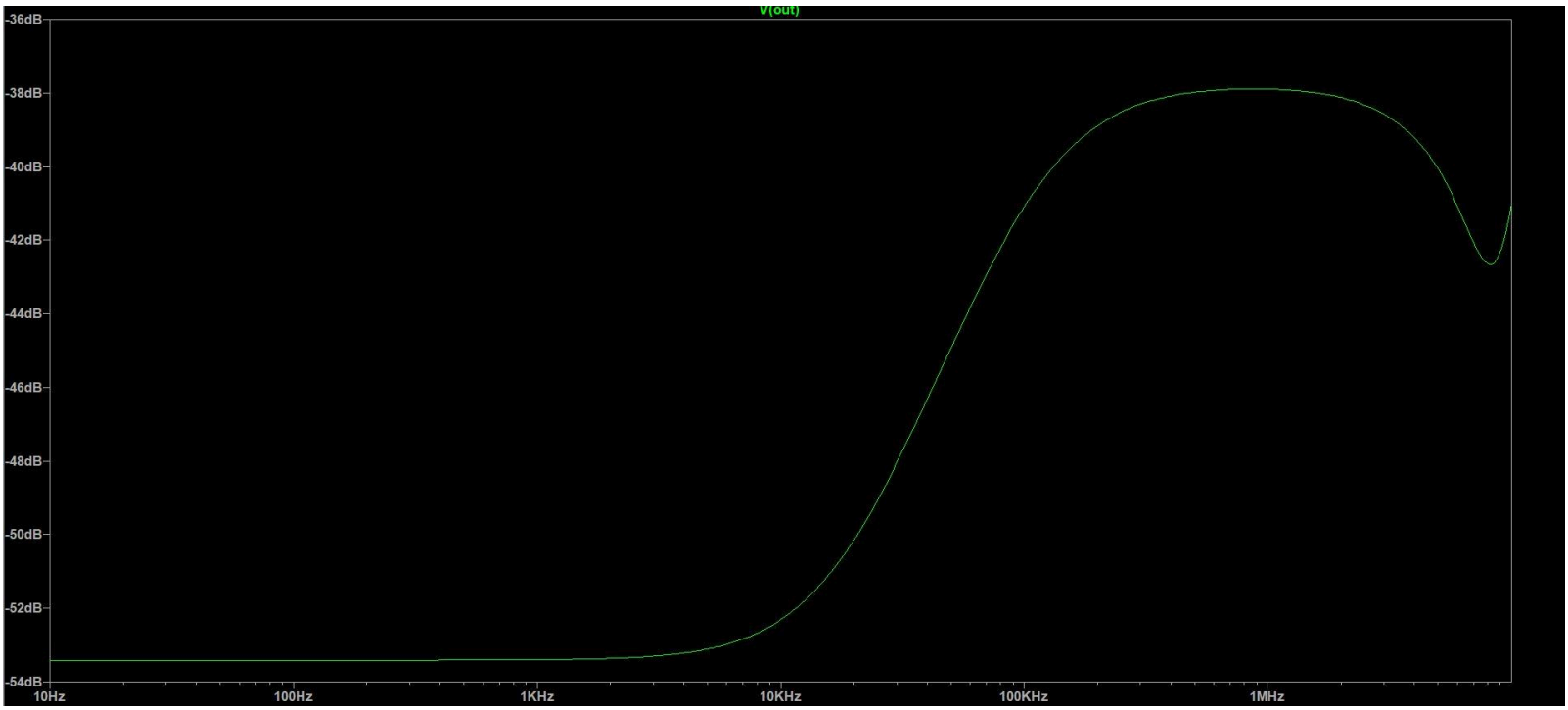
3) Input and Output Impedance

The input and output impedance of the opamp as calculated earlier is 20.18 kilo ohm and 310 ohms respectively. The value of input differential impedance of BJT is less than MOSFET because of the base current in the BJT while MOSFETs have zero gate current giving them infinite input impedance.

4) Common Mode Rejection Ratio

The CMRR is how well this circuit can suppress any noise in it and the CMRR for our circuit is 110-119 db. The differential voltage gain is around

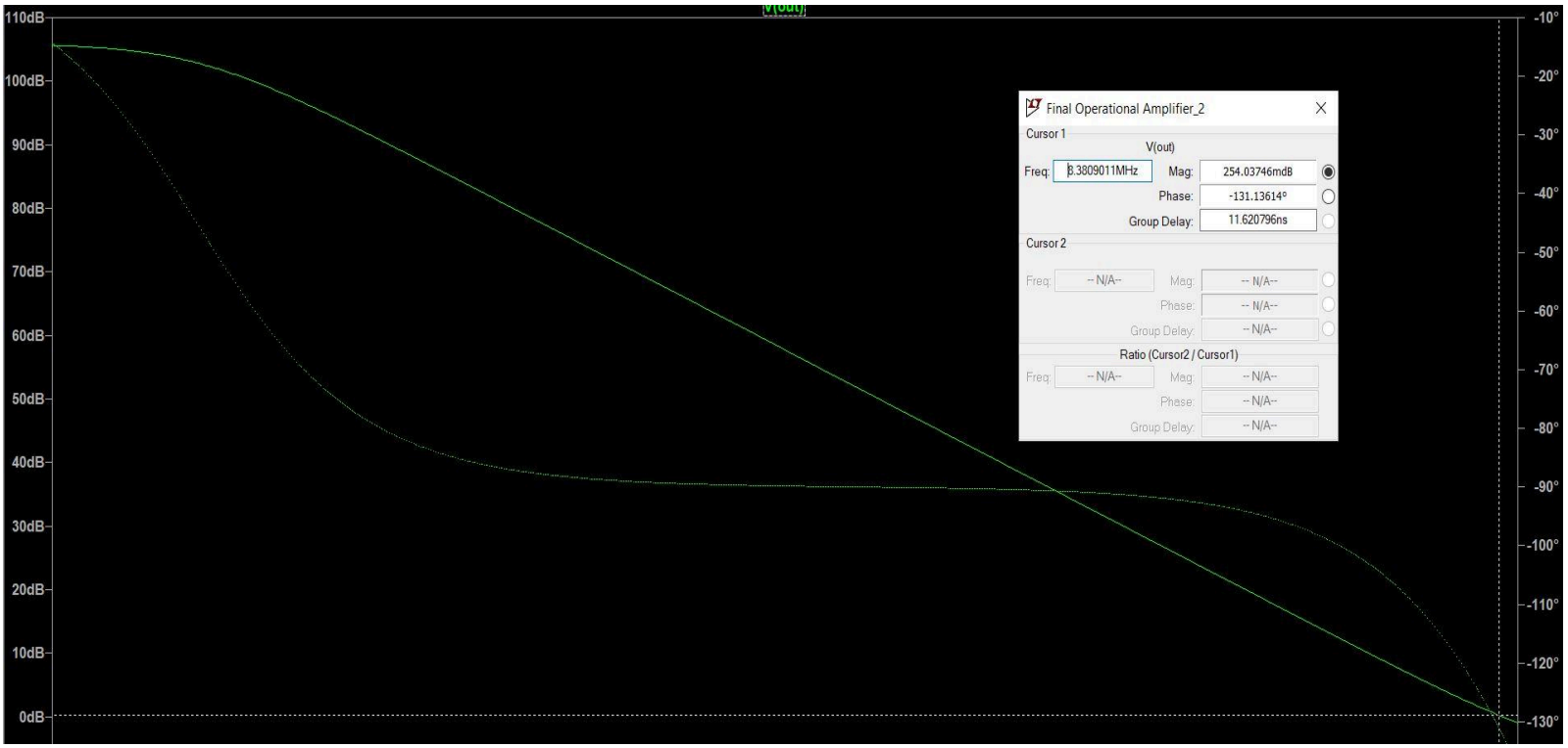
67 decibels and on simulating on LTspice it gives a common mode gain of -53.45 decibels which shows that it attenuates any noise signal in it.



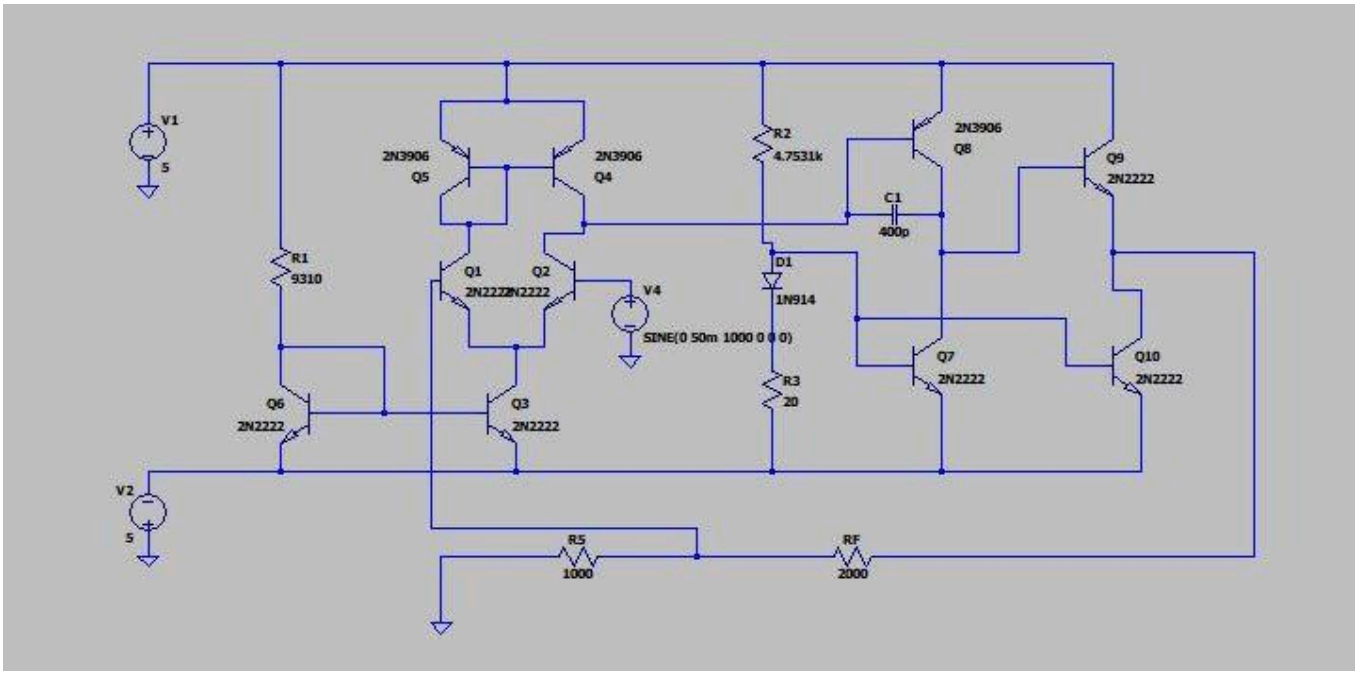
Notice that as frequency increases the ability to suppress common mode signal also decreases.

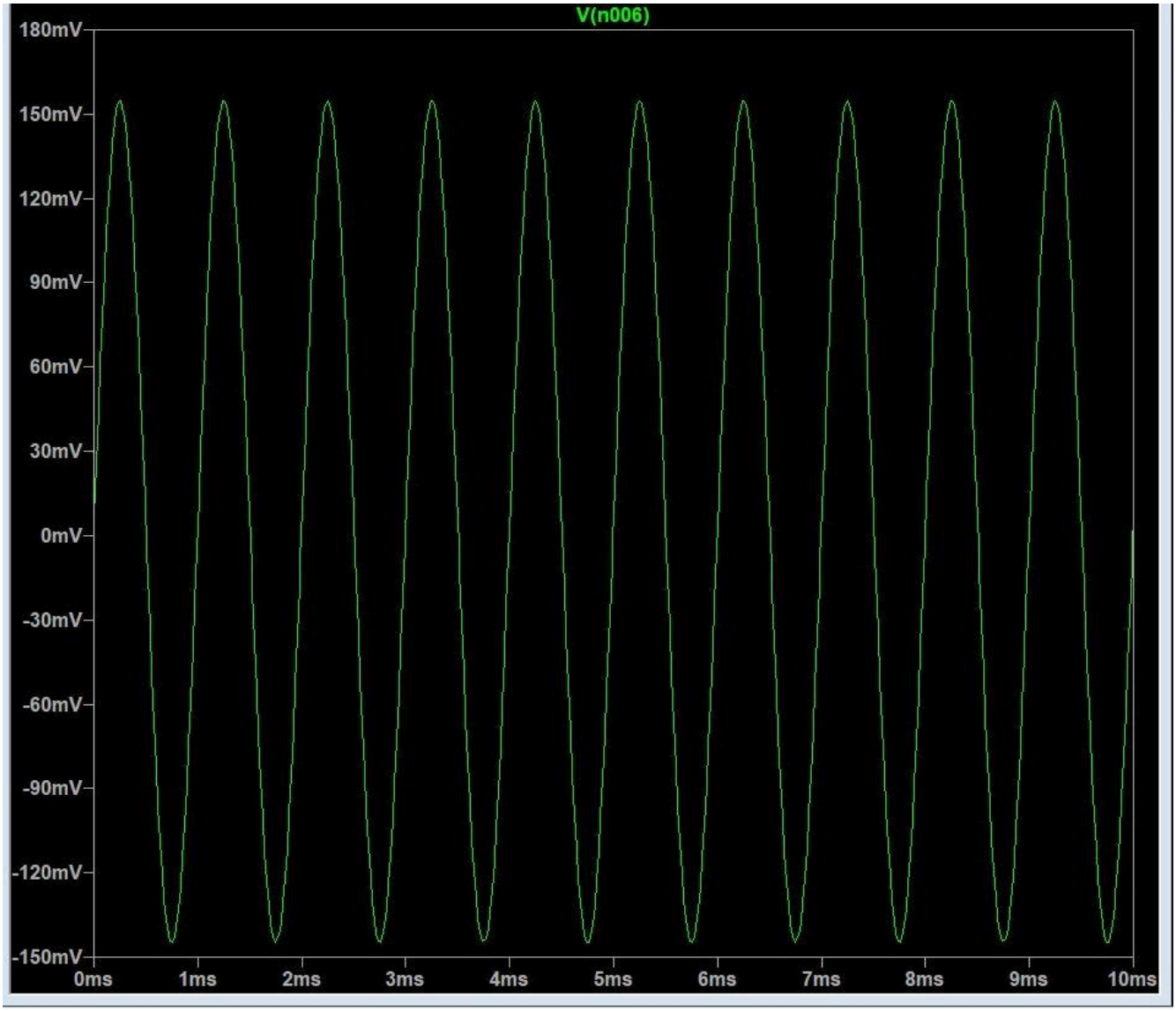
5) Gain Bandwidth Product

The frequency at which the gain becomes unity i.e. 0 decibels is the unity gain frequency and therefore the unity gain of our circuit is 8.38 MHz.



V. Closed Loop Configuration Implementation

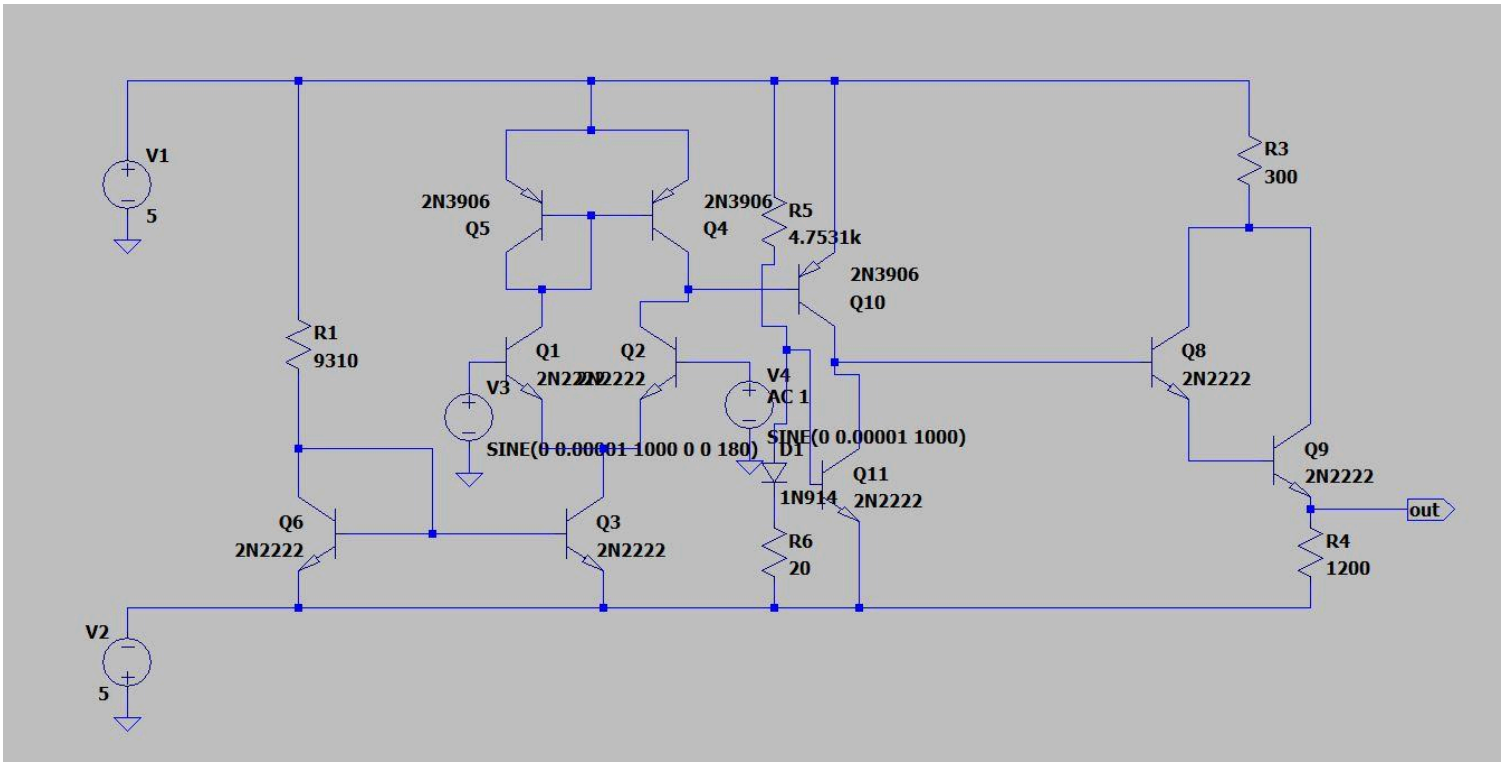




The circuit was implemented in non-inverting configuration with an input signal of 50mV and it gave a correct gain of 3 times the input signal equal to 150 mV.
I tested the circuit in other configurations also and it performed remarkably.

VI. Future Scope : Power Operational Amplifier :-

The last stage of the op amp can be replaced with a darlington pair as it has all properties of buffer stage : unity gain , high input impedance and low output impedance and along with that it also has high current gain to receive a signal with high power for running load.



VII. References :

1) Sedra and Smith Microelectronics book
2) https://www.researchgate.net/figure/Op-amp-Functional-Block-Diagram_fig1_354376031#:~:text=This%20article%20explains%20how%20to,phase%20margin%20of%2070%200
3) https://hackaday.io/project/176860-homemade-operational-amplifier