CS 301
High-Performance Computing

Lab 01 - CPU Architecture, Triad and Measuring Performance

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Contents

1 Introduction

In this lab, we measure the CPU performance of the Lab PC and the HPC Cluster. We study system architecture by implementing vector operations: copy, scale, sum, triad, and an energy kernel to understand memory bandwidth limitations.

2 Hardware Details

2.1 Hardware Details for LAB207 PCs

- Architecture: x86_64
- CPU(s): 12
- Thread(s) per core: 2
- Core(s) per socket: 6
- Model name: 12th Gen Intel(R) Core(TM) i5-12500
- CPU max MHz: 4600
- L1d cache: 288K
- L1i cache: 192K
- L2 cache: 7.5M
- L3 cache: 18M

2.2 Hardware Details for HPC Cluster

- Architecture: x86_64
- CPU(s): 16
- Thread(s) per core: 1
- Core(s) per socket: 8
- Socket(s): 2
- Model name: Intel(R) Xeon(R) CPU E5-2640 v3 @ 2.60GHz
- L1d cache: 32K
- L1i cache: 32K
- L2 cache: 256K
- L3 cache: 20480K

3 Benchmarking Methodology

We measured execution time, throughput, and FLOPs for varying problem sizes.

$$\text{Throughput} = \frac{\text{sizeof(double)} \times N \times Total}{alg\_time}$$

$$\text{FLOPs} = \frac{M \times Total}{alg\_time}$$

4 Graphical Results

4.1 Vector Copy Operation: $a[i] = b[i]$

4.1.1 Lab PC Results

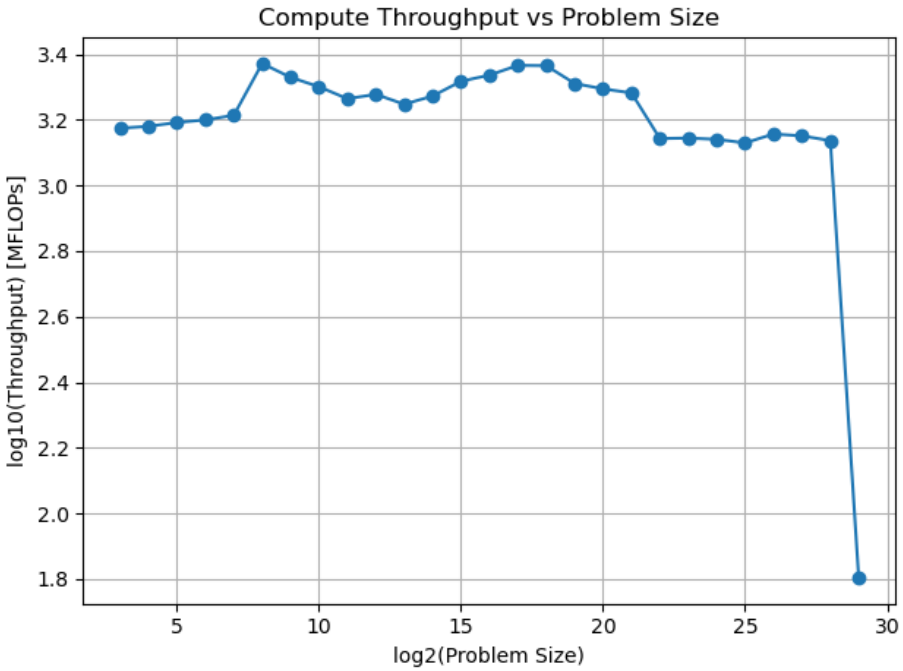

Figure 1: Throughput vs Problem Size (Lab PC)

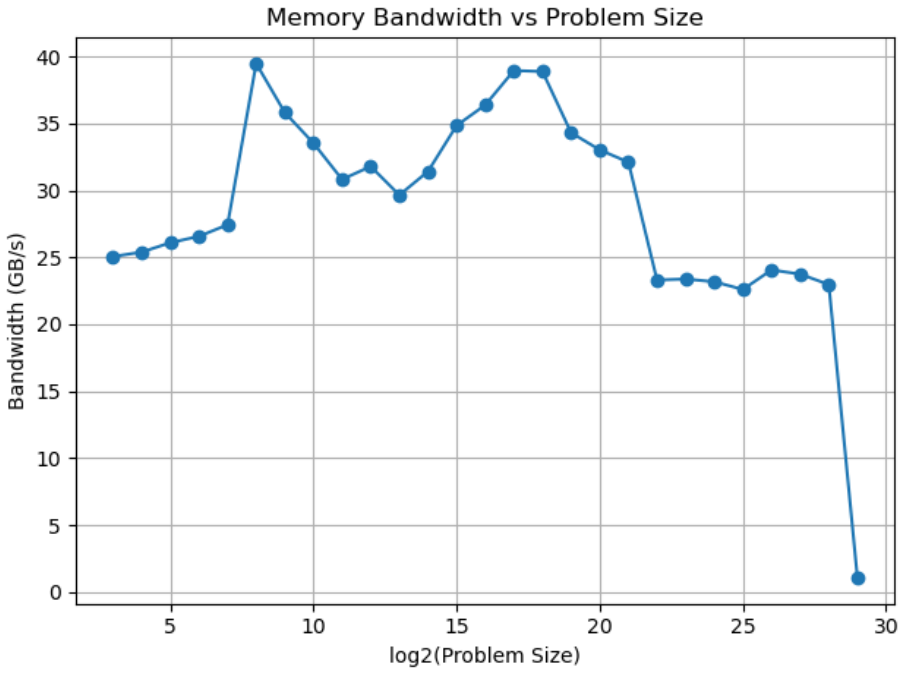

Figure 2: Bandwidth vs Problem Size (Lab PC)

4.1.2 HPC Cluster Results

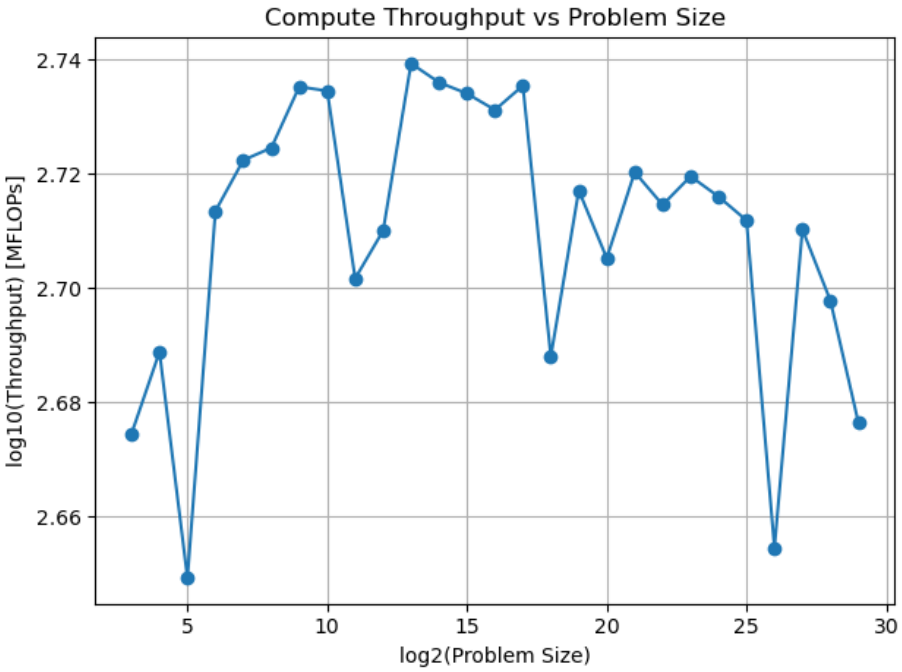

Figure 3: Throughput vs Problem Size (HPC Cluster)

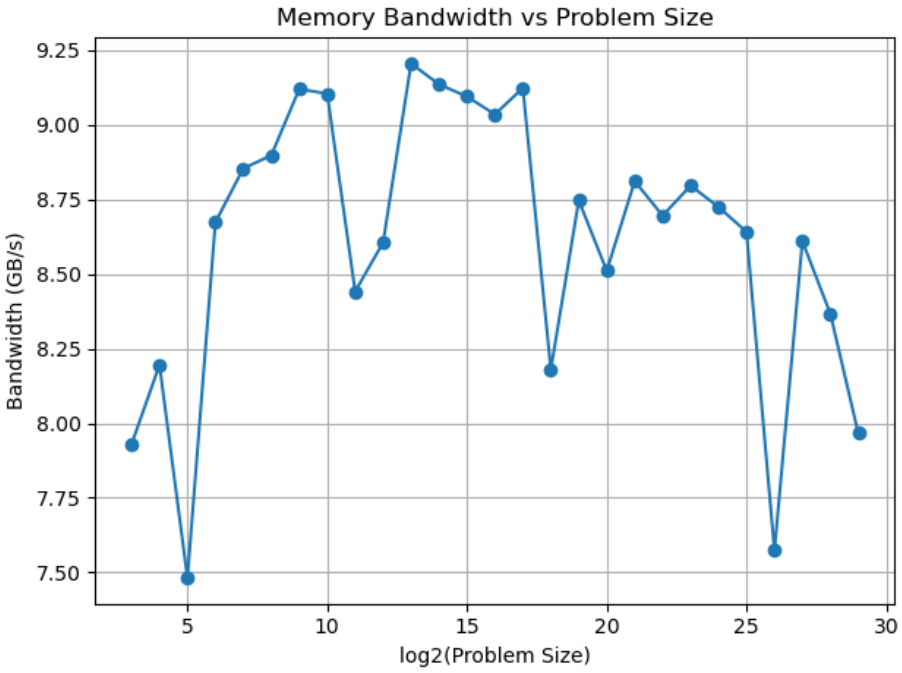

Figure 4: Bandwidth vs Problem Size (HPC Cluster)

4.2 Vector Scaling Operation: $a[i] = k \times b[i]$

4.2.1 Lab PC Results

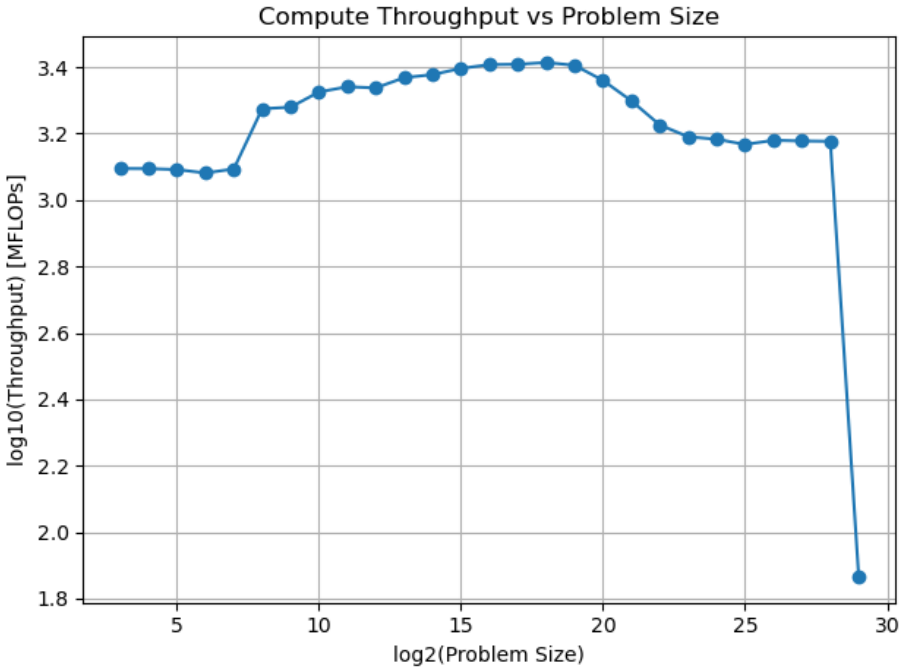

Figure 5: Throughput vs Problem Size (Lab PC)

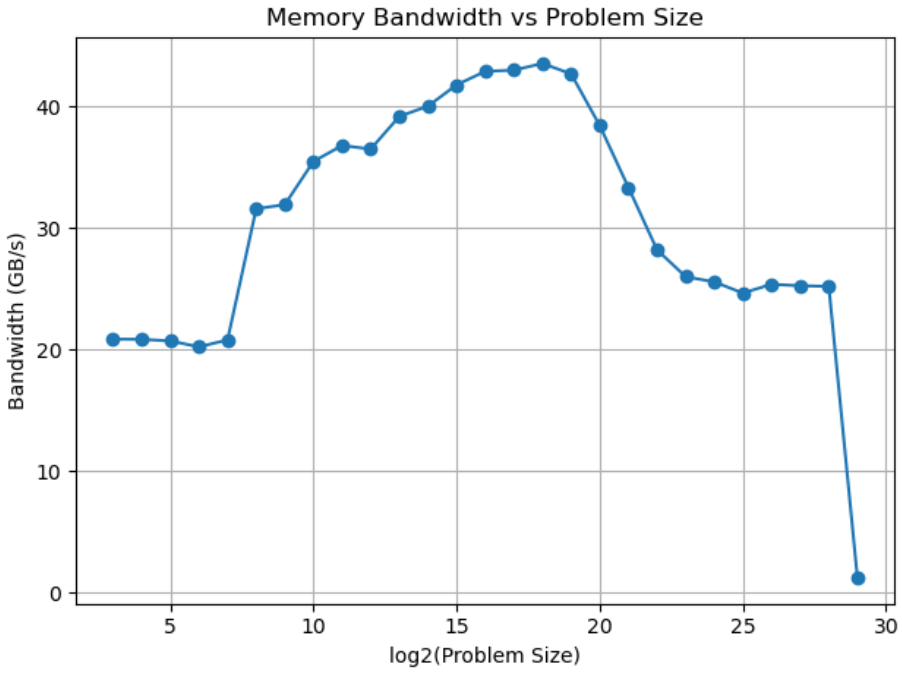

Figure 6: Bandwidth vs Problem Size (Lab PC)

4.2.2 HPC Cluster Results

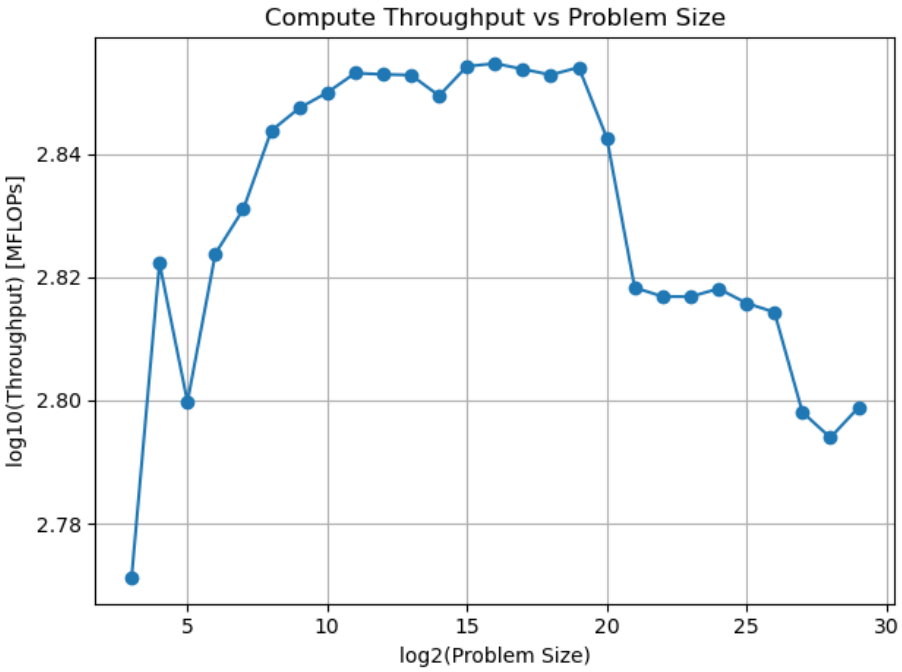

Figure 7: Throughput vs Problem Size (HPC Cluster)

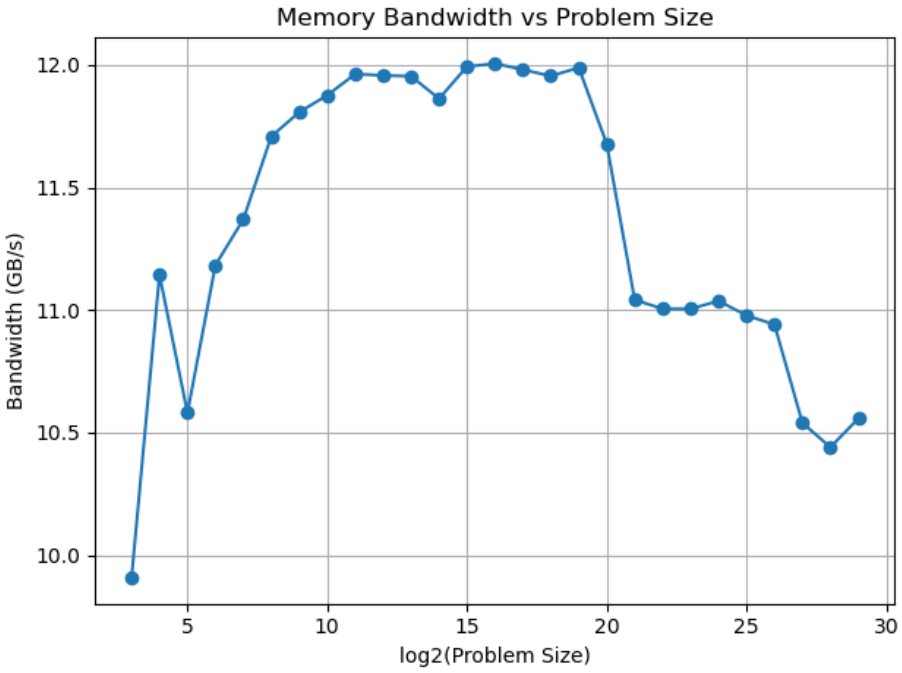

Figure 8: Bandwidth vs Problem Size (HPC Cluster)

4.3 Vector Sum Operation: $a[i] = b[i] + c[i]$

4.3.1 Lab PC Results

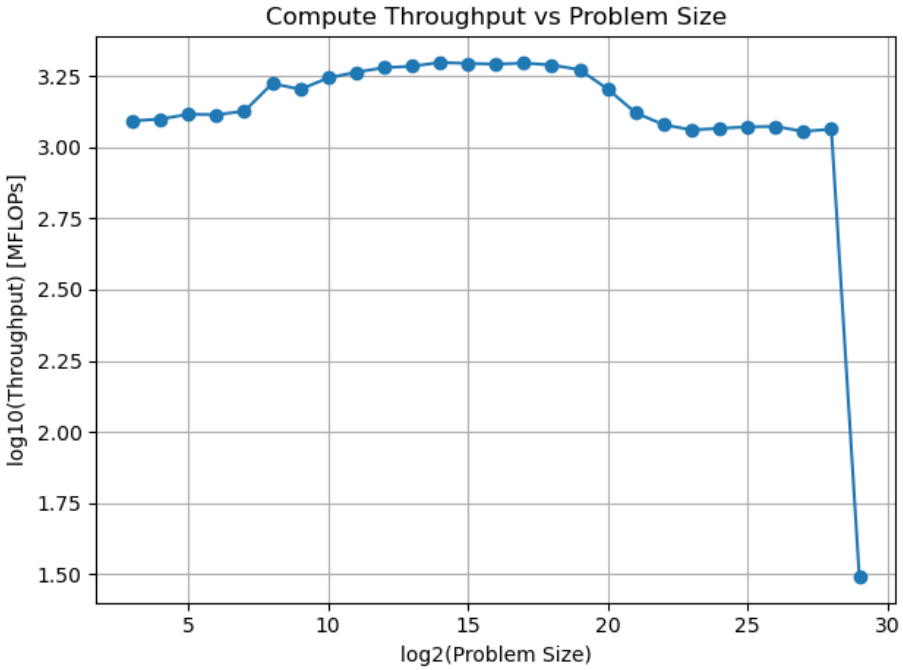

Figure 9: Throughput vs Problem Size (Lab PC)

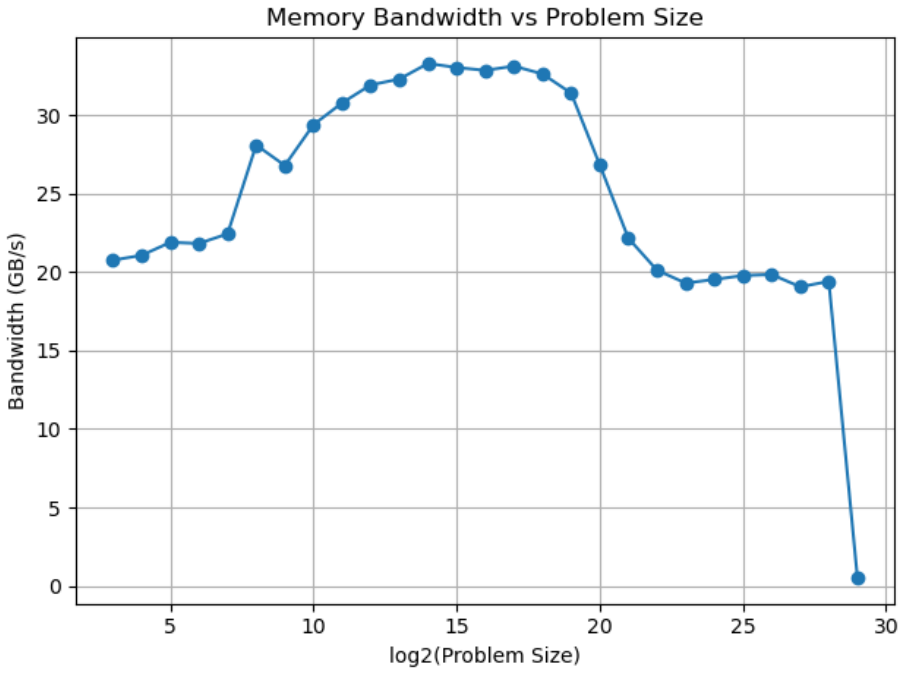

Figure 10: Bandwidth vs Problem Size (Lab PC)

4.3.2 HPC Cluster Results

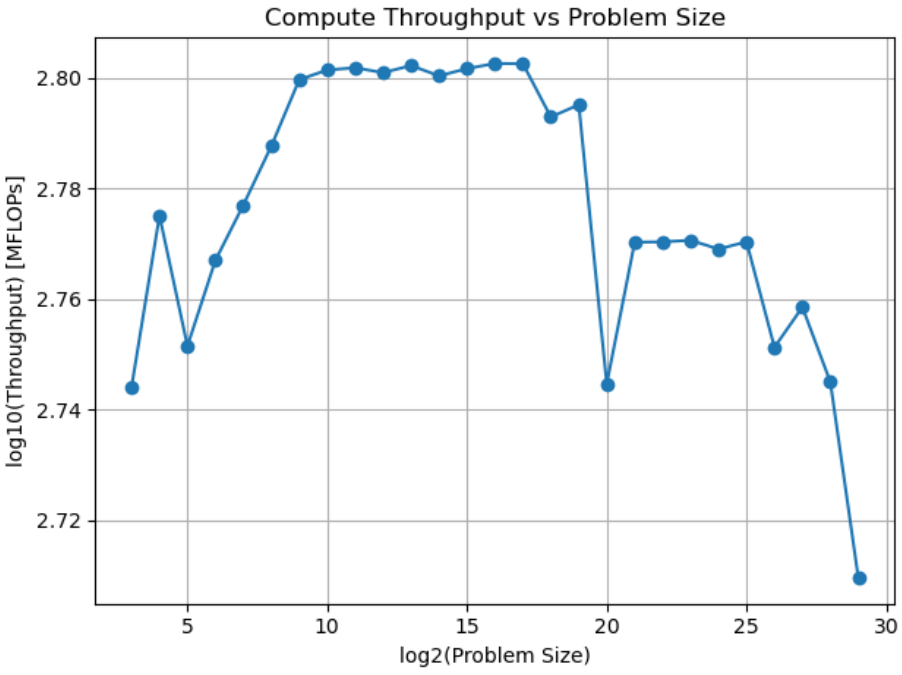

Figure 11: Throughput vs Problem Size (HPC Cluster)

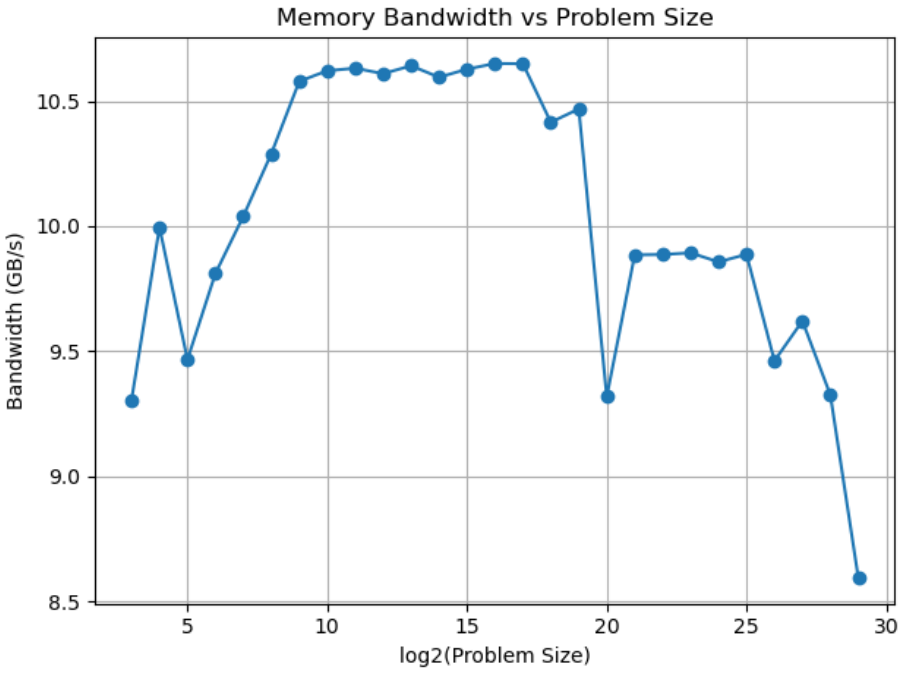

Figure 12: Bandwidth vs Problem Size (HPC Cluster)

4.4 Vector Triad Operation: $a[i] = b[i] + c[i] \times d[i]$

4.4.1 Lab PC Results

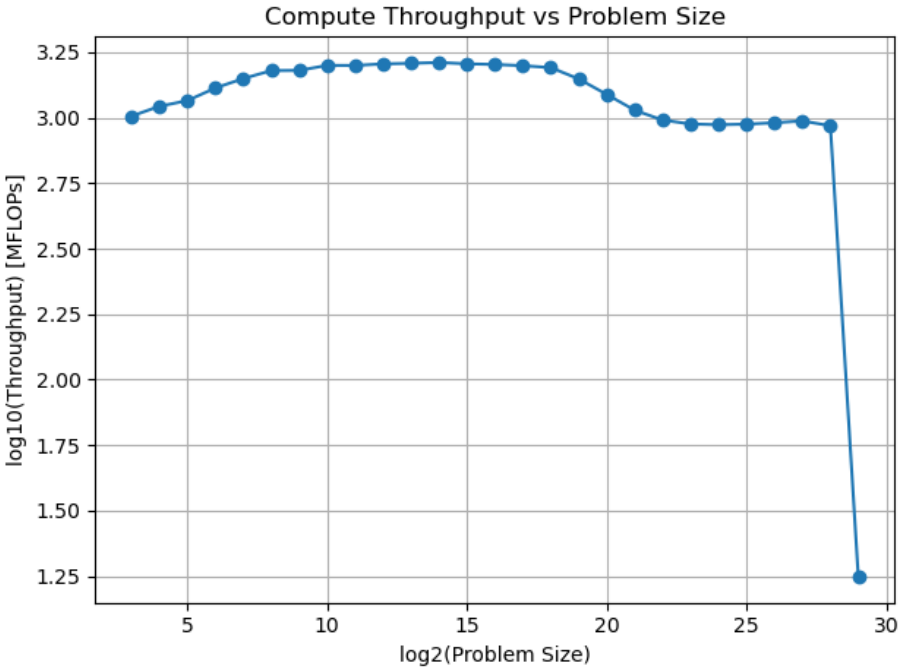

Figure 13: Throughput vs Problem Size (Lab PC)

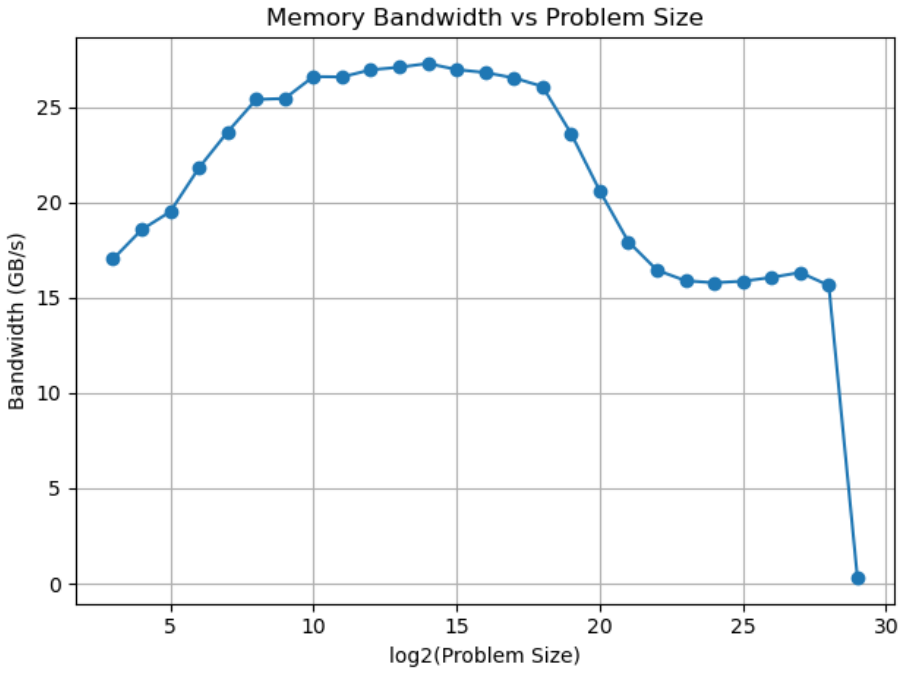

Figure 14: Bandwidth vs Problem Size (Lab PC)

4.4.2 HPC Cluster Results

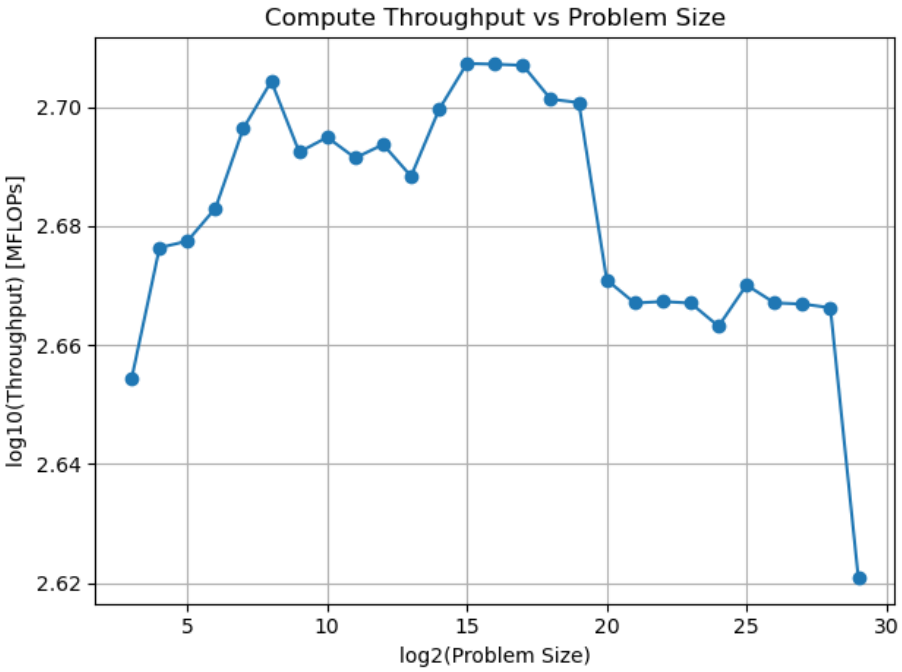

Figure 15: Throughput vs Problem Size (HPC Cluster)

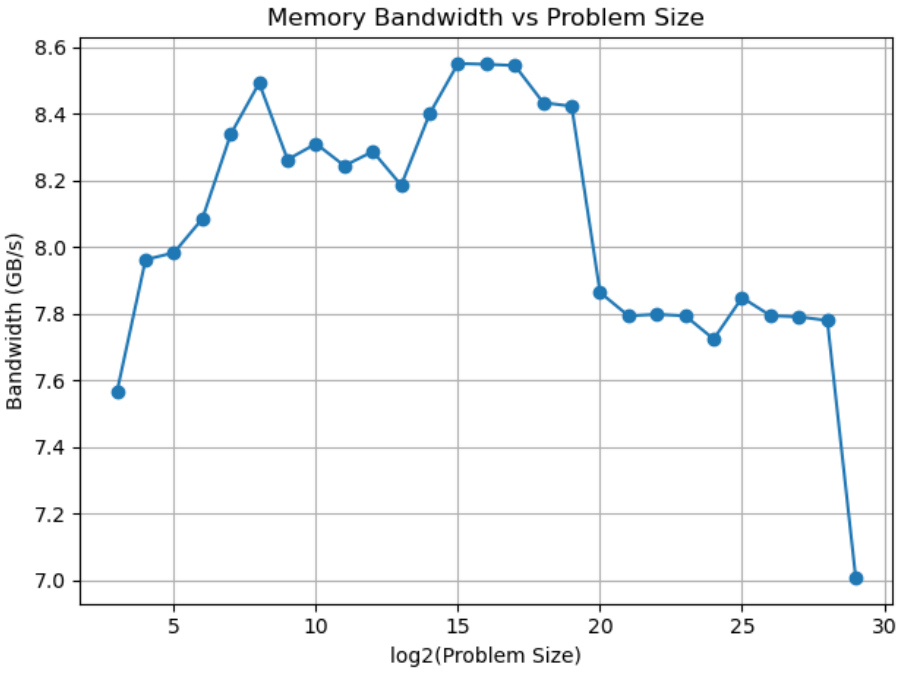

Figure 16: Bandwidth vs Problem Size (HPC Cluster)

4.5 Energy Kernel Operation: $E[i] = 0.5mv[i]^2$

4.5.1 Lab PC Results

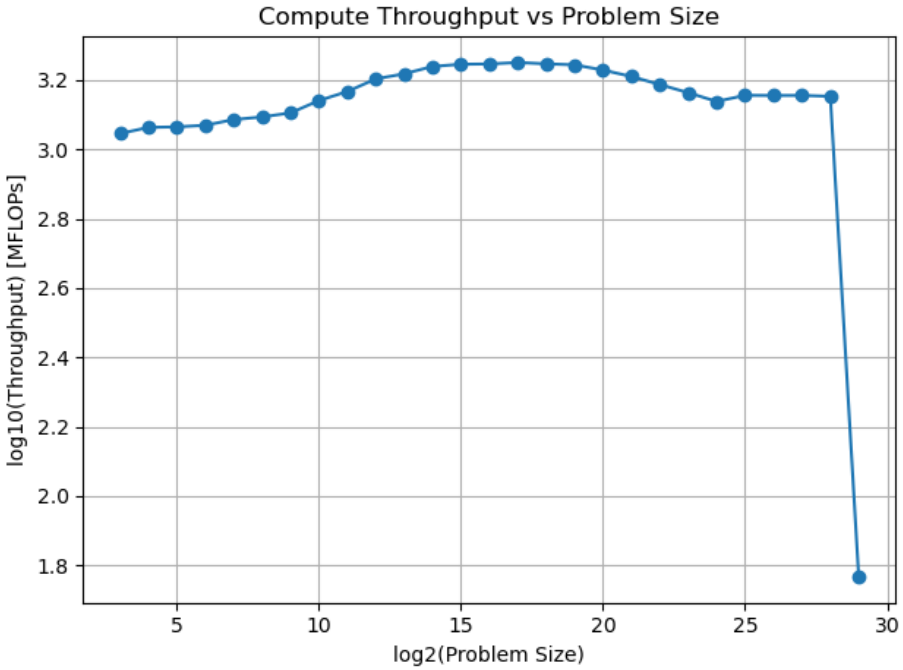

Figure 17: Throughput vs Problem Size (Lab PC)

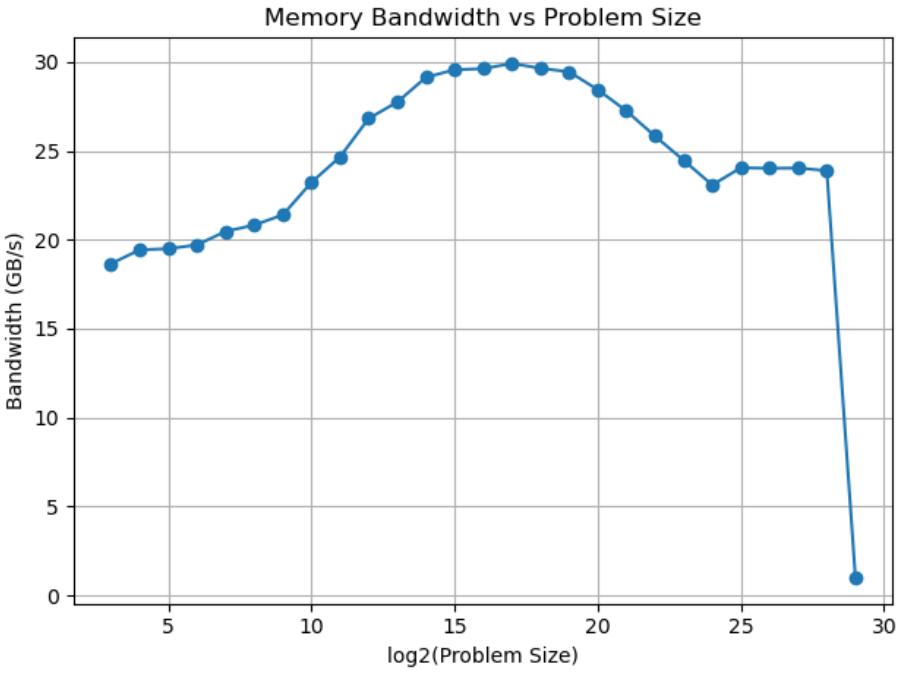

Figure 18: Bandwidth vs Problem Size (Lab PC)

4.5.2 HPC Cluster Results

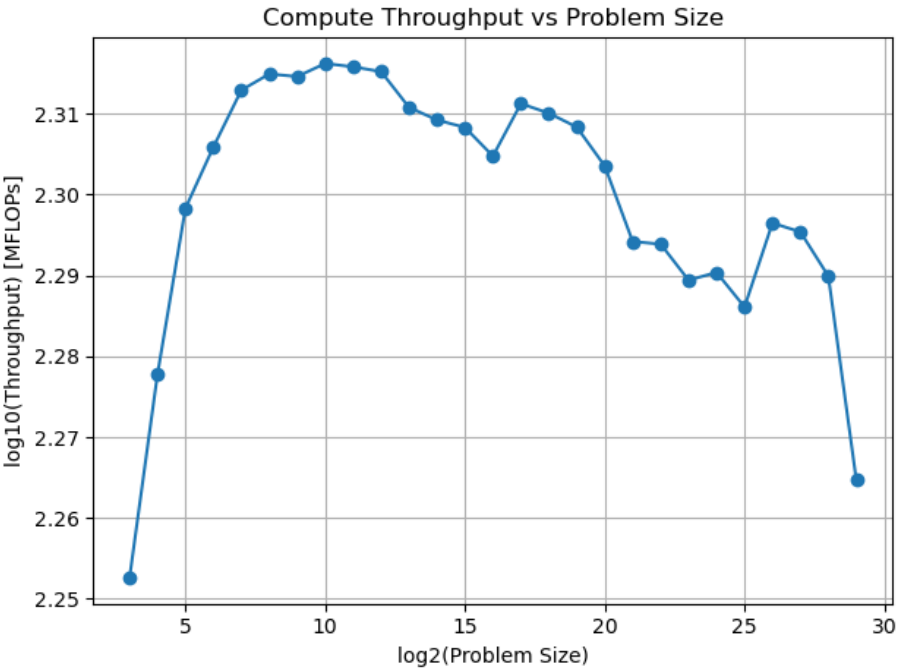

Figure 19: Throughput vs Problem Size (HPC Cluster)

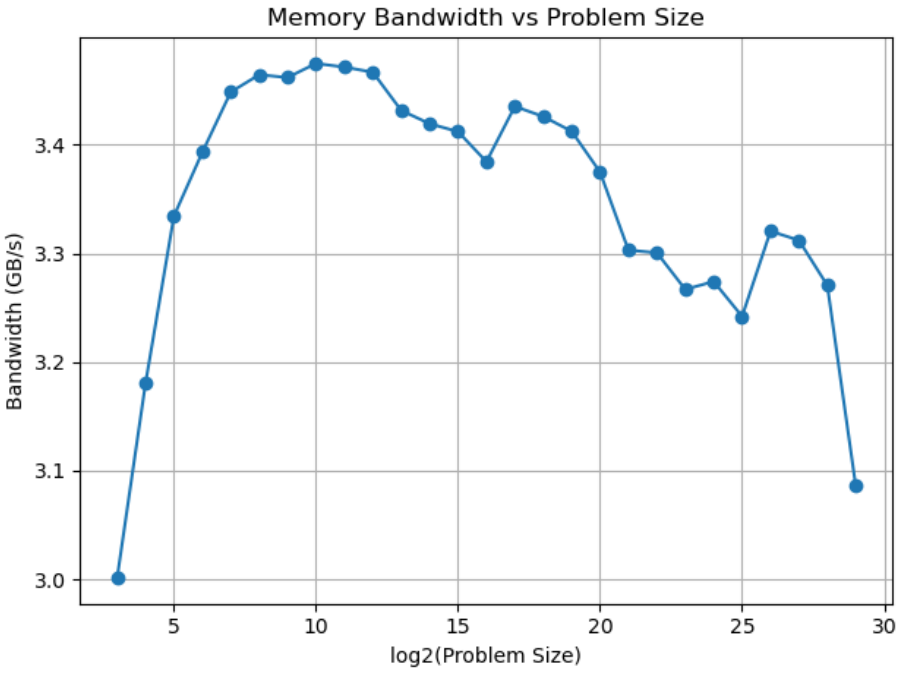

Figure 20: Bandwidth vs Problem Size (HPC Cluster)

5 Conclusion

The throughput decrease of HPC cluster v/s Lab PC may be due to lower clock speed of HPC cluster 2.6GHz compared to 3 to 4.6 GHz of Lab PC. The bandwidth of HPC cluster is low compared to Lab PC is due to fact that HPC is designed with multi thread output in mind and thus it only peaks at 8 GBps rather than 26 GBps of Lab PC. Also we can see that at the largest size the fall is not that sharp in HPC compared to Lab PC due to larger RAM size in HPC.