VIT®

Vellore Institute of Technology

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Lab Manual

ELECTRICAL & ELECTRONICS ENGINEERING LAB MANUAL (EEE1001L / EEE1019L)

(20 - 20)

(B.Tech/M.Tech. _____)

____ SEMESTER

Name:	
Reg. No:	
Slot:	
Faculty Name :	

SCHOOL OF ELECTRICAL ENGINEERING

A Place to Learn; A Chance to Grow

INDEX Simulation

Experiments

Sl.No	Date	Name of the Experiment	Remark
1		Verifications of KCL AND KVL	
2		Verification of NETWORK THEOREMS (Thevenin's Theorem)	
3		Maximum Power Transfer Theorem using Parametric Sweep Method	
4		Response of RLC series circuit	
5		Design of Half Adder and Full Adder circuits	
6		Design of Single phase Half-wave and Full wave Rectifier	
7		**Design of Regulated Power Supply	

Sl.No	Date	Name of the Experiment	Remark
1		Verification of Thevevnin's Theorem	
2		Design of Half Adder Circuit using gates.	
3		Lamp Dimmer Circuit (Darlington Pair)	
4		**Line and Load Regulation using Zener Diode	
5			
6			

Ex. No.: 1 Date:

Verification of KIRCHHOFF'S LAWS

(Mesh and Nodal Analysis)

Aim:

Apparatus/Tool required:

Sl. No.	Components Name	Range	Quantity
1	Resister	330Ω, 270Ω, 390Ω, 220Ω, 180Ω	Each 1 No.
2	Ammeter	0-50mA (DC)	1 No.
3	Voltmeter	0-30V (DC)	1 No.
4	RPS	0-32 V (DC)	1 No.
5	Connecting Wires	-	Few
6	Bread Board	-	1 No.

Circuit Diagram:

Theory:

Kirchhoff's Current Law (KCL):

Kirchhoff's Voltage Law (KVL):

Practical Circuit and output:

Mesh Analysis:

Manual Calculations:

Mesh Analysis

Practical Circuit and output:

Node Analysis:

Manual Calculations:

Nodal Analysis

Procedure:

Result:

Mesh Analysis:

Manual Calculations Practical output

Node Voltage Analysis:

Manual Calculations Practical output

Inference:

Reg. No:	**Name:**	**Date:**

Ex. No.:2 Date:

Verification of NETWORK THEOREMS

(Thevenin's Theorem)

Aim:

Apparatus/Tool required:

ORCAD / Capture CIS --> **Analog Library – R,**
Source Library – Vdc, Idc &
Ground (GND) – 0 (zero)

Simulation Settings: **Analysis Type - Bias Point**

Circuit Diagram

Statement: Thevenin's Theorem

Manual Calculations:
To Find V_{th}:

To Find R_{th}:

To Find I_L:
Equivalent Circuit

Simulation Circuit:

To Find V_{th}:

To Find R_{th}:

To Find I_L:

Procedure:

Result:

Thevenin's Theorem

Manual Calculations Simulated Result

Inference:

Reg. No:	**Name:**	**Date:**

Ex. No.:3 Date:

Verification of NETWORK THEOREMS

(Maximum Power Transfer Theorem)

Aim:

Apparatus/Tool required:

ORCAD / Capture CIS --> **Analog Library – R,**
Source Library – Vdc, Idc &
Ground (GND) – 0 (zero)

Simulation Settings: **Analysis Type - Bias Point**

Circuit Diagram

Statement: Maximum Power Transfer Theorem

Manual Calculations:

To Find V_{th}:

To Find R_{th}:

To Find Power:

Simulation Circuit:

To Find V_{th}:

To Find R_{th}:

To Find Power:

Procedure:

Result:

Maximum Power Transfer Theorem

Manual Calculations Simulated Result

Inference:

Reg. No:	**Name:**	**Date:**

Ex. No.:4 Date:

Response of RLC Series Circuit

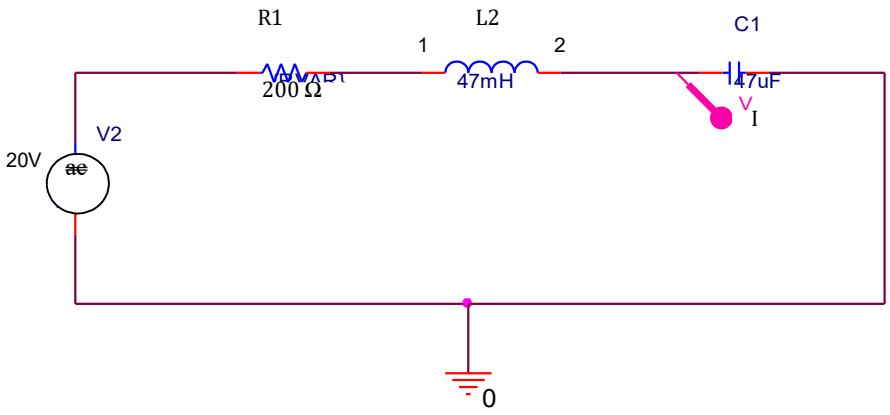
Aim:

Apparatus/Tool required:

ORCAD / Capture CIS --> **Analog Library – R, L & C**
Source Library – Vac
Ground (GND) – 0 (zero)

Simulation Settings: **Analysis Type – Transient (Time Domain)**
Run to time: 20ms

Circuit Diagram:

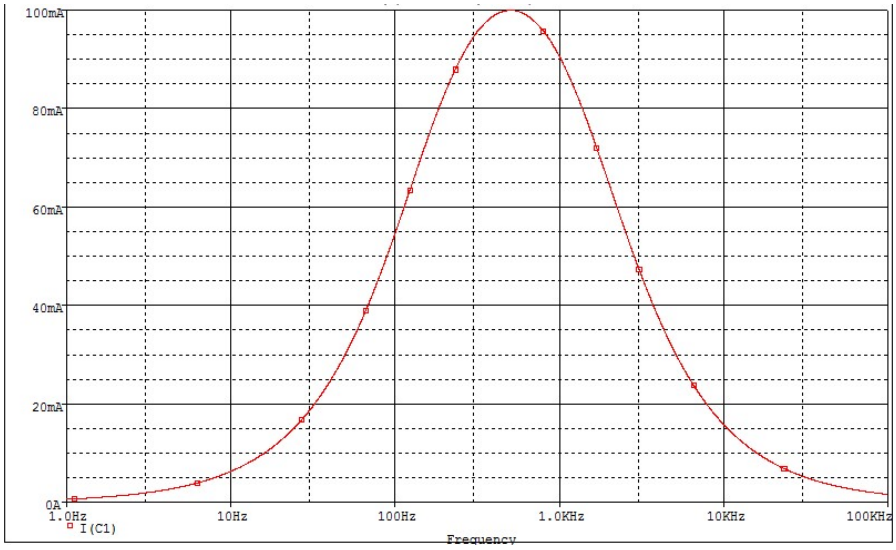


Theory:

Formulae :

Calculation:

Model Graph:



Simulation Circuit Diagram and Output:

Procedure:-

Result:-

Inference:-

Reg. No:	Name:	Date:

Ex. No.: 5 Date:

Design of Half Adder and Full Adder circuits

Aim:

Apparatus/Tool required:

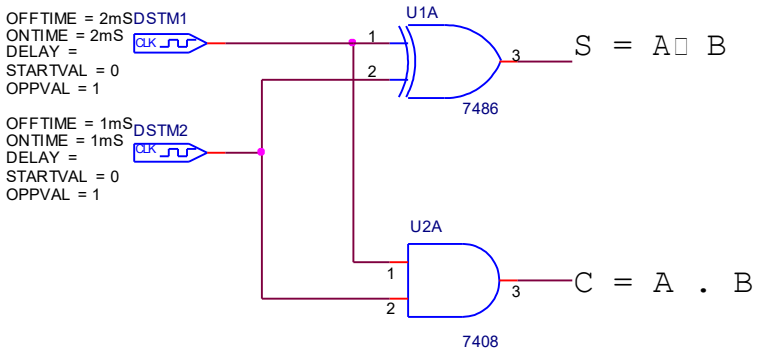
ORCAD / PSpice simulator - > **7400 Library – 7408, 7432 & 7486**
Source Library - Digclock

Simulation Settings: **Analysis Type - Time Domain**

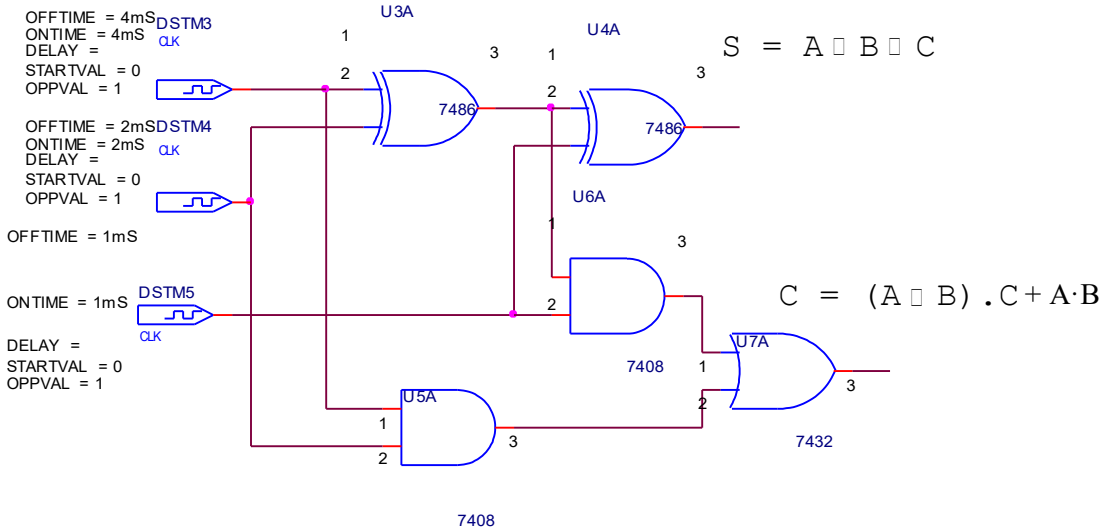
Run to time: 4ms (for Half Adder)
Run to time: 8ms (for Full Adder)

Circuit Diagram:

Half – Adder Circuit



Full – Adder Circuit



Theory:

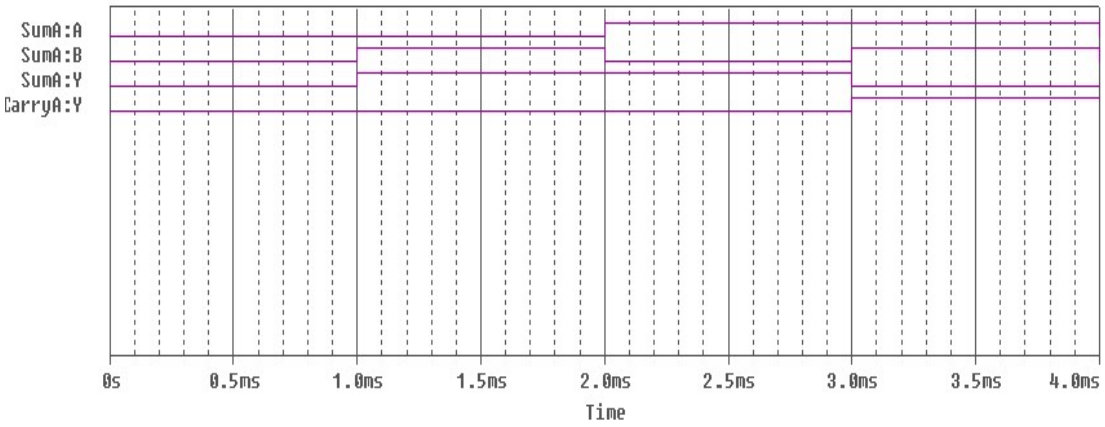
Half Adder Circuit:

Truth Table

A	B	S=A⊕B	C=A.B
0	0		
0	1		
1	0		
1	1		

Model Timing Diagram:

Half – Adder



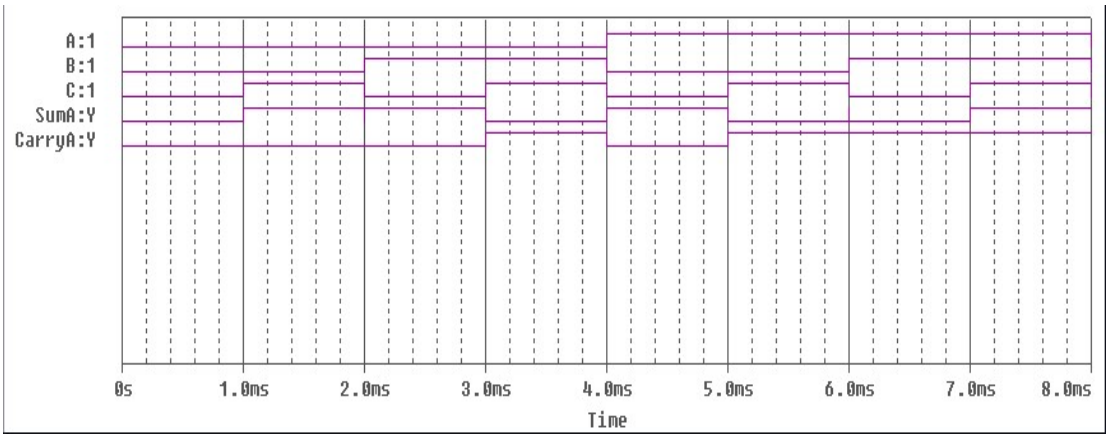
Full Adder Circuit

Truth Table

A	B	C	S=A□B□B	C= (A□B).C+A.B
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Model Timing Diagram:

Full – Adder



Procedure:

Result:

Inference:

Reg. No:	Name:	Date:

Ex. No. 6 Date:

Design of Single phase Half wave and Full wave Rectifiers

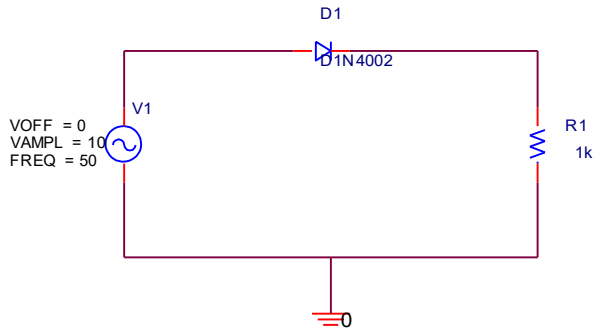
Aim:

Apparatus/Tool required:

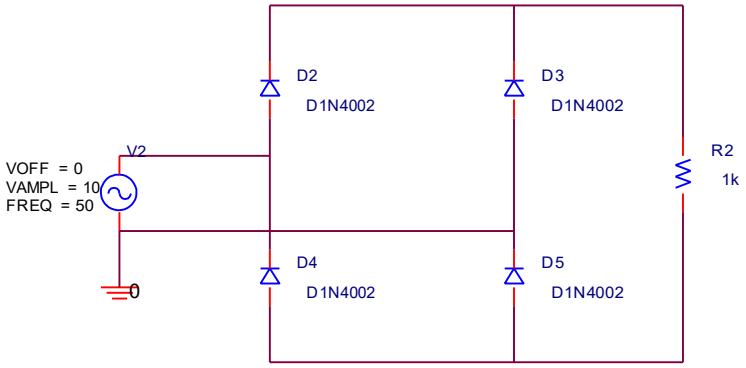
ORCAD / PSpice simulator -> **Diode Library - D1N4002/4007,**
Source Library – Vsin & Ground (GND) – 0(zero)
Analog Library – R
Simulation Settings: **Analysis Type - Time Domain**
Run to time: 40ms (for 2 cycles)

Circuit Diagram:

Single phase Half – wave Rectifier



Single phase Full – Wave Rectifier



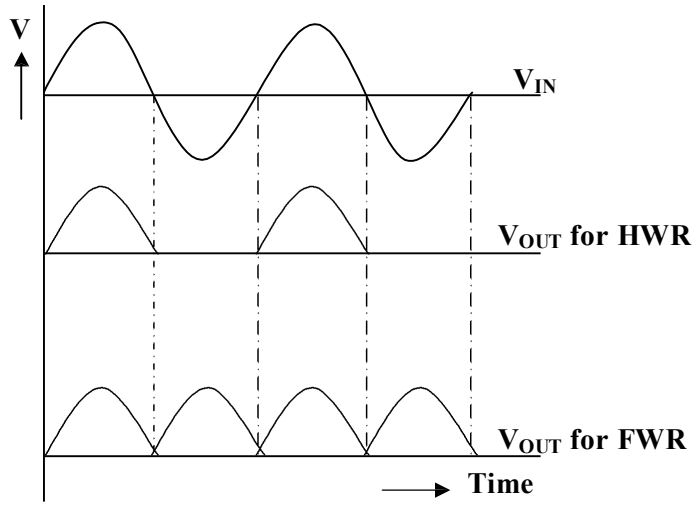
Theory:

Half – wave Rectifier

Full – wave Rectifier

Procedure:

Model Graph:



Result

Inference

Reg. No:	Name:	Date:

Ex. No.:7 Date:

Design of Regulated Power supply

Aim:

Apparatus/Tool required:

ORCAD / PSpice simulator -> **Analog Library – R, L & C**
Diode Library - D1N4007 & Zener diode
Source Library – Vsin, Vdc &
Ground (GND) – 0 (zero)
Simulation Settings: **Analysis Type - Time Domain (Run to time: 100ms)**

Circuit Diagram:

Theory:

Simulation Circuits and Model output graph:

Procedure:

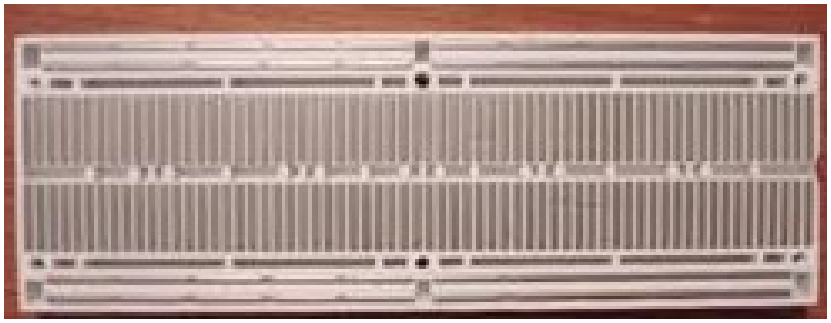
Result:

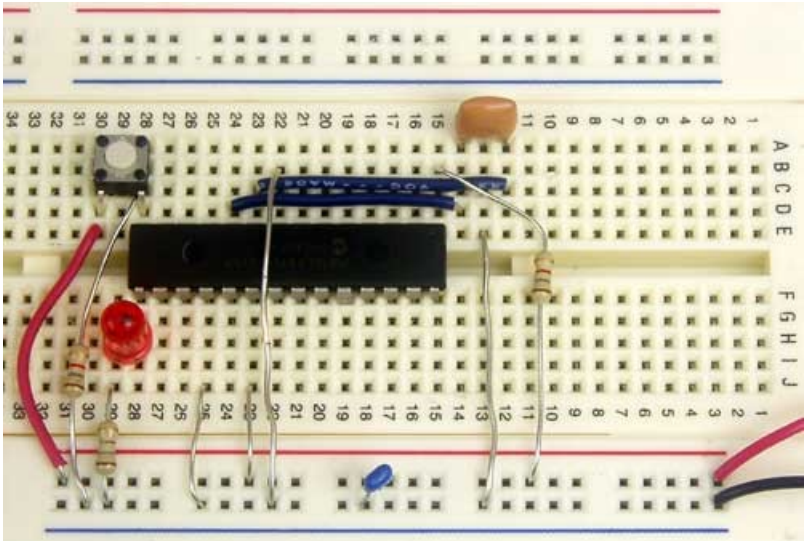
Inference:

Reg. No:	Name:	Date:

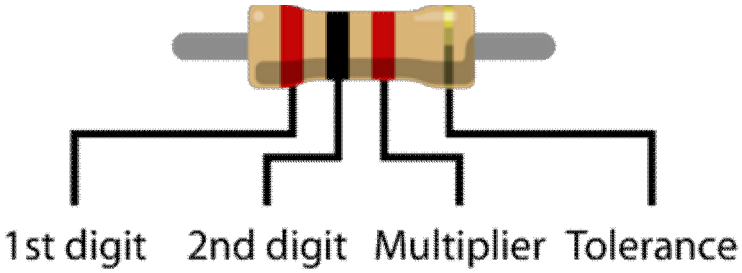
Hardware Experiments

Sample Bread Board



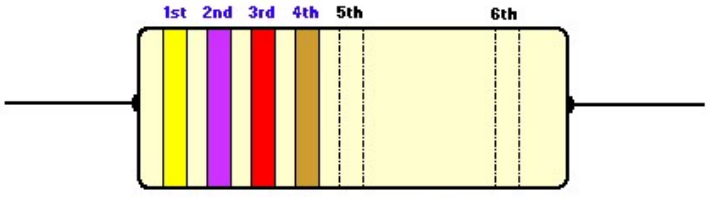


Resistor Color Coding



Color	Digit	Multiplier	Tolerance (%)
Black	0	10^0 (1)	
Brown	1	10^1	1
Red	2	10^2	2
Orange	3	10^3	
Yellow	4	10^4	
Green	5	10^5	0.5
Blue	6	10^6	0.25
Violet	7	10^7	0.1
Grey	8	10^8	
White	9	10^9	
Gold		10^{-1}	5
Silver		10^{-2}	10
(none)			20

Example: 4.7K or 4700 ohms (Carbon)



Band 1, 2, 3
Black = 0
Brown = 1
Red = 2
Orange = 3
Yellow = 4
Green = 5
Blue = 6
Violet = 7
Gray = 8
White = 9
Gold = 0.1

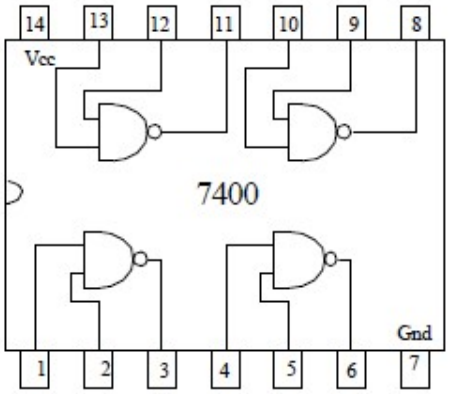
Band 1: Yellow - 4 4
Band 2: Violet - 7 7
Band 3: Red - 2 00
Band 4, Gold, 5% Tolerance 4700 Ohms

Band 1, first #
Band 2, secnd #
Band 3, multiplier with '0's
Band 4, tol. in %

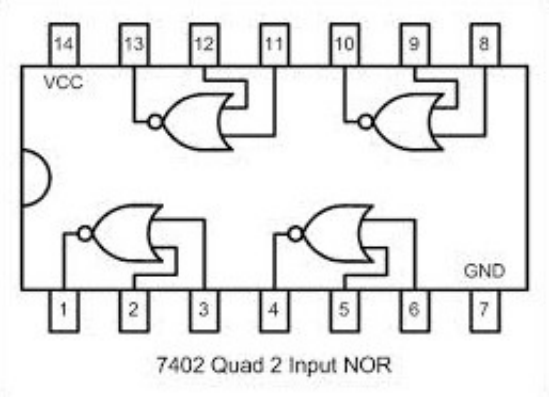
Tolerance: Brown = 1%
Red = 2%
Band 4 Gold = 5%
Silver = 10%
None = 20%

Band 5 & 6 usually for 1% metal film types. Band 6 for temp. coefficient.

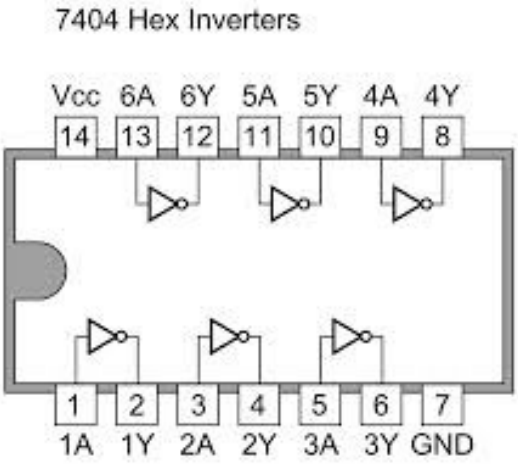
PIN Diagram of 7400



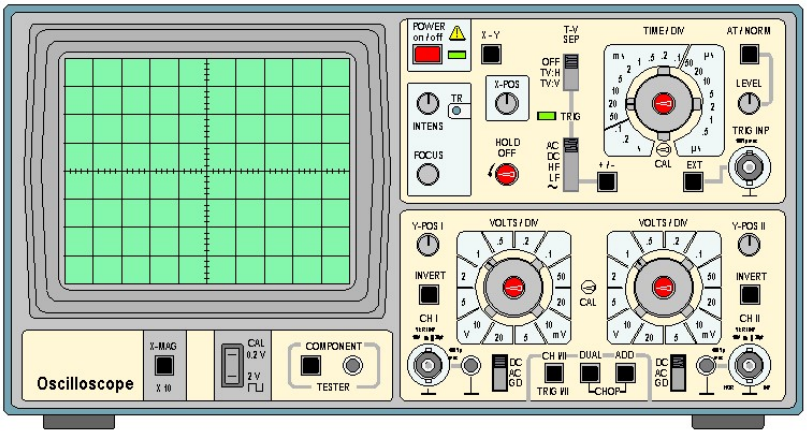
PIN Diagram of 7402



PIN Diagram of 7404



Meters & CRO


POWER on / off
X - Y
T-V SEP
TIME / DIV
AT / NORM
X-POS
INTENS
FOCUS
TR
HOLD OFF
TRIG
LEVEL
TRIG INP
CAL
EXT
Y-POS I
VOLTS / DIV
Y-POS II
INVERT
CH I
CH II
DUAL
ADD
CHOP
Oscilloscope
X-MAG
COMPONENT
TESTER


B1
B2
L
M
COM
W


DCV
ACV
DCA
OFF
hFE
NPN
PNP
DT-838
DIGITAL
MULTIMETER
COM


V
MADE IN CHINA

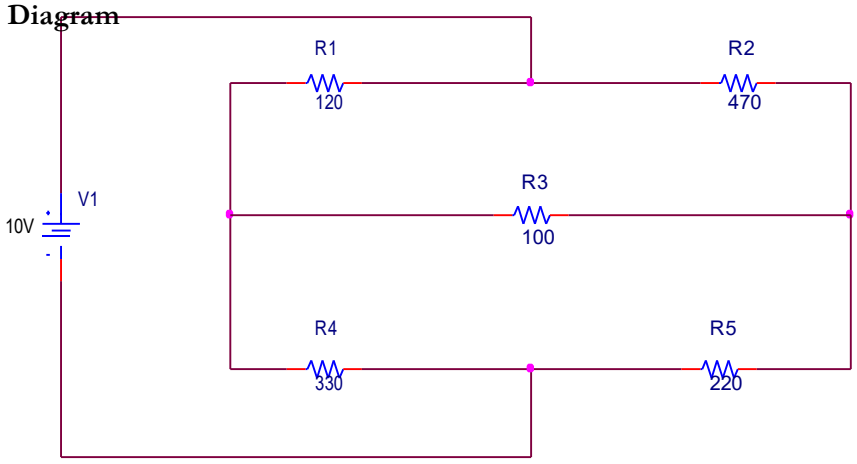

A

Ex. No.:8 Date:

Verification of Thevenin's Theorem

Aim:

Circuit Diagram



Apparatus/Tool required:

Sl. No.	Components Name	Range	Quantity
1	Resister	120Ω, 330Ω, 470Ω, 220Ω, 100Ω	Each 1 No.
2	Ammeter	0-50mA (DC)	1 No.
3	Voltmeter	0-10V (DC)	1 No.
4	RPS	0-32 V (DC)	1 No.
5	Connecting Wires	-	Few
6	Bread Board	-	1 No.

Theory

Statement: Thevenin's Theorem

Hardware Circuit:

To Find V_{TH}:

Reading:

Applied Voltage (Volts)	V_{TH} (Volts)

To Find R_{TH}:

Reading:

Applied Voltage	Voltmeter Reading	Ammeter Reading	R_{TH} = V/I ohms

Average of R_{TH} = _____ Ohms.

To Find I_L :

Reading:

Applied Voltage (Volts)	Ammeter Reading (Amps)

Manual Calculations:

To Find V_{TH}:

To Find R_{TH}:

To Find I_L:

Procedure:

Result:

Thevenin's Theorem

Manual Calculations Practical Output

Inference:

Reg. No: Name: Date:

Ex. No.:10 Date:

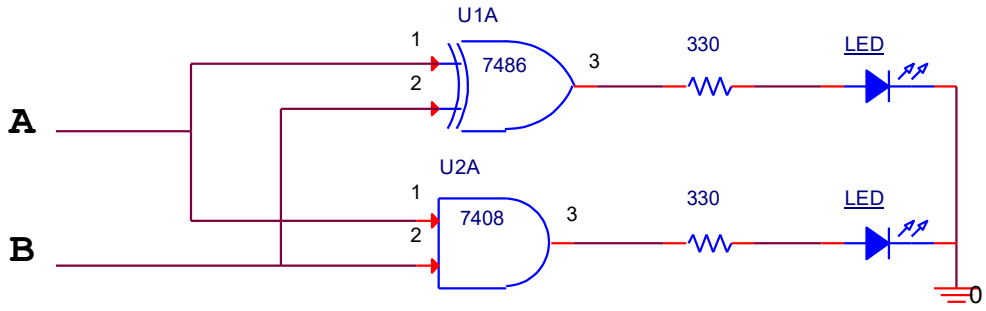
Design of Half Adder Circuit using gates

Aim:

Apparatus Required:

S. No.	Name of the apparatus	Range / Type	Quantity
1	7486 gate	-	1 No.
2	7408 gate	-	1 No.
3	LED	-	2 Nos.
4	RPS	0 – 15 V	1 No.
5	Resistor	330 Ω	2 Nos.
6	Breadboard	-	1 No.
7	Wires	-	Few

Circuit Diagram:



Theory:

Truth Table

A	B	S=A⊕B	C=A.B
0	0		
0	1		
1	0		
1	1		

Observation:

Procedure:

Result:

Reg. No:	Name:	Date:

Ex. No.:11 Date:

Line and Load Regulation using zener diode

Aim

Apparatus Required

S. No.	Name of the apparatus	Range / Type	Quantity
1	Zener diode	-	1 No.
2	RPS	0 – 30 V	1 No.
3	Ammeter	0 – 10 A	2 No.
4	Voltmeter	0 – 30 V	2 No.
5	Resistor	330 Ω	1 No.
6	Resistor	1 kΩ	1 No.
7	Breadboard	-	1 No.
8	Wires	-	Few

Theory

Zener diodes are generally used in the reverse bias mode. You have seen already in one of your previous experiments that the zener diode has a region of almost a constant voltage in its reverse bias characteristics, regardless of the current flowing through the diode. This voltage across the diode (zener Voltage, V_Z) remains nearly constant even with large changes in current through the diode caused by variations in the supply voltage or load. This ability to control itself can be used to great effect to regulate or stabilize a voltage source against *supply* or *load* variations. The zener diode maintains a constant output voltage until the diode current falls below the minimum Iz value in the reverse breakdown region, which means the supply voltage, V_S, must be much greater than V_Z for a successful breakdown operation. When no load resistance, R_L, is connected to the circuit, no load current ($I_L = 0$), is drawn and all the circuit current passes through the zener diode which dissipates its maximum power. So, a suitable current limiting resistor, (R_S) is always used in series to limit the zener current to less than its maximum rating under this "no-load" condition.

From the previous experiments on rectifiers, you know that the d.c. output voltage from the half or full-wave rectifiers contains ripples superimposed on the d.c. voltage and that the average output voltage changes with load. As shown in the circuit diagram, a more stable reference voltage can be produced by connecting a simple zener regulator circuit across the output of the rectifier. The breakdown condition of the zener can be confirmed by calculating the Thevenin voltage, V_{TH}, facing the diode is given as:

$$V_{TH} = \frac{R_L}{R_S + R_L} V_S$$

This is the voltage that exists when the zener is disconnected from the circuit. Thus, V_{TH} has to be greater than the zener voltage to facilitate breakdown. Now, under this breakdown condition, irrespective of the load resistance value, the current through the current limiting resistor, Is, is given by

$$I_S = \frac{V_S - V_Z}{R_S}$$

The output voltage across the load resistor, V_L, is ideally equal to the zener voltage and the load current, I_L, can be calculated using Ohm's law:

$$V_L = V_Z \text{ and } I_L = \frac{V_L}{R_L}$$

Thus the zener current, I_Z, is

$$I_Z = I_S - I_L .$$

Now that you have constructed a basic power supply, its quality depends on its load and line regulation characteristics as defined below.

Load Regulation: It indicates how much the load voltage varies when the load current changes. Quantitatively, it is defined as:

$$\text{Load regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%$$

where V_{NL} = load voltage with no load current ($I_L = 0$) and V_{FL} = load voltage with full load current. The smaller the regulation, the better is the power supply.

Line Regulation: It indicates how much the load voltage varies when the input line voltage changes. Quantitatively, it is defined as:

$$\text{Line regulation} = \frac{V_{HL} - V_{LL}}{V_{LL}} \times 100\%$$

where V_{HL} = load voltage with high input line voltage, and V_{LL} = load voltage with low input line voltage. As with load regulation, the smaller the regulation, the better is the power supply.

Procedure:

1. Use the full-wave rectifier circuit configured in your previous lab (with capacitor filter minus the load). Connect the primary of a variable transformer to a.c. mains and the secondary as the a.c. source for the rectifier circuit. This will facilitate to change the magnitude of input voltage to rectifier by choosing different secondary terminals. You can use only those secondary terminals whose voltage is much more than the zener breakdown voltage you are using.
2. Complete the rest part of the circuit as shown in the circuit diagram. Note down all the values of the components being used including the zener breakdown voltage.
3. Keeping input voltage suitably fixed, use different values of R_L and measure both the output d.c. voltage and current using multimeter (in d.c. mode). Measure input unregulated d.c. voltage across capacitor. Calculate V_{TH} before each measurement and ensure that the zener is operating in breakdown region.
4. Similarly, keeping R_L fixed, vary the input voltage and measure again the output d.c. voltage, current and input unregulated d.c. voltage across capacitor. Calculate V_{TH} before each measurement.
5. Tabulate all your data and calculate percentage regulation in each case.

Observations:
Specifications of zener diode: Breakdown voltage = _____ V
Rs = _____Ω

Circuit Diagram

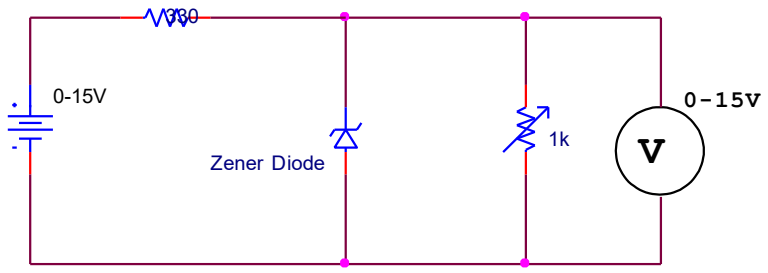


Table (i) Line Regulation: Load Resistor = _____Ω

Sl.No	Input DC Voltage (Vi) in Volts	Output DC Voltage (V_L) in Volts
1		
2		
3		
4		
5		

Table (ii) Load Regulation: Input d.c. voltage = _____V

Sl.No	Load Resistance in ohms	Output DC Voltage (V_L) in Volts
1		
2		
3		
4		
5		

Result:

Ex. No.:12 Date:

Lamp Dimmer Circuit (Darlington Pair)

Aim

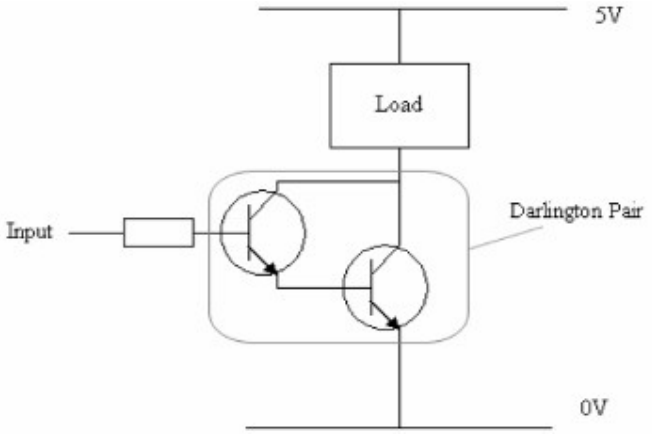
To design a circuit to vary the intensity of the lamp using darlington pair of BJT

Apparatus Required

S. No.	Name of the apparatus	Range / Type	Quantity
1	BJT	BC547	2 Nos.
2	RPS	0 – 30 V	1 No.
3	Diode	1N4007	1 No.
4	Potentiometer	1 kΩ	1 No.
5	LED	-	1 No.
6	Breadboard	-	1 No.
7	Wires	-	Few

Theory:

A Darlington pair is two transistors that act as a single transistor but with a much higher current gain. This mean that a tiny amount of current from a sensor, micro-controller or similar can be used to drive a larger load. An example circuit is shown below:



The Darlington Pair can be made from two transistors as shown in the diagram or Darlington Pair transistors are available where the two transistors are contained within the same package.

Transistors have a characteristic called current gain. This is referred to as its hFE. The amount of current that can pass through the load in the circuit above when the transistor is turned on is:

Load current = input current x transistor gain (hFE)

The current gain varies for different transistors and can be looked up in the data sheet for the device. For a normal transistor this would typically be about 100. This would mean that the current available to drive the load would be 100 times larger than the input to the transistor. In some applications the amount of input current available to switch on a

transistor is very low. This may mean that a single transistor may not be able to pass sufficient current required by the load. As stated earlier this equals the input current x the gain of the transistor (hFE). If it is not possible to increase the input current then the gain of the transistor will need to be increased. This can be achieved by using a Darlington Pair.

A Darlington Pair acts as one transistor but with a current gain that equals:

Total current gain (hFE total) = current gain of transistor 1 (hFE t1) x current gain of transistor 2 (hFE t2)

So for example if you had two transistors with a current gain (hFE) = 100:

(hFE total) = 100 x 100

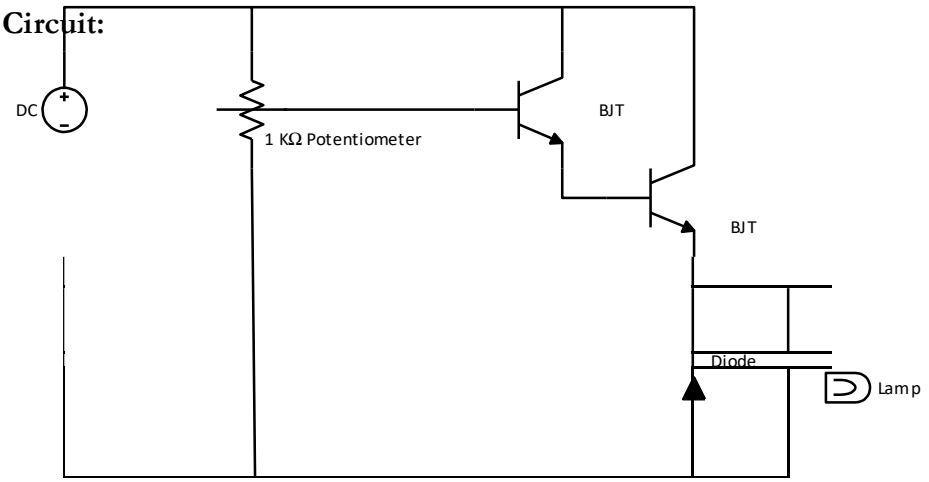
(hFE total) = 10,000

You can see that this gives a vastly increased current gain when compared to a single transistor. Therefore this will allow a very low input current to switch a much bigger load current.

Normally to turn on a transistor the base input voltage of the transistor will need to be greater than 0.7V. As two transistors are used in a Darlington Pair this value is doubled. Therefore the base voltage will need to be greater than 0.7V x 2 = 1.4V.

It is also worth noting that the voltage drop across collector and emitter pins of the Darlington Pair when the turn on will be around 0.9V Therefore if the supply voltage is 5V (as above) the voltage across the load will be will be around 4.1V (5V – 0.9V)

Circuit:



Result: