Bangladesh University of Engineering and Technology

Department of Computer Science and Engineering

Academic Year 2020 - 2021

CSE 206
Digital Logic Design Sessional
Offline 2

Group No 2

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Date of Submission:
April 03, 2021

Problem 1

1.1 Problem Specification

Design using basic gates, a 2-bit comparator to comapre 2-bit numbers X and Y. The circuit should provide 3 output lines to indicate $X > Y, X = Y,$ and $X < Y$.

1.2 Required Instruments

1. IC-7404 (Quantity: 1)
2. IC-7408 (Quantity: 2)
3. IC-7432 (Quantity: 1)
4. IC-7486 (Quantity: 1)
5. Input Pins (Quantity: 4)
6. Output Pin (Quantity: 3)
7. Wires
8. Software : Logisim

1.3 Truth Table

A_1	A_0	B_1	B_0	G	L	E
0	0	0	0	0	0	1
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	0	1	0	0	1
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	0	1
1	0	1	1	0	1	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	0	1

1.4 Boolean Expressions

$$
\begin{aligned}
&L(A_1, A_0, B_1, B_0) \\
&= A_1'A_0'B_1'B_0 + A_1'A_0'B_1B_0' + A_1'A_0'B_1B_0 + A_1'A_0B_1B_0' + A_1'A_0B_1B_0 + A_1A_0'B_1B_0 \\
&= A_1'B_1(A_0'B_0' + A_0'B_0 + A_0B_0' + A_0B_0) + A_1'B_1'A_0'B_0 + A_1B_1A_0'B_0 \\
&= A_1'B_1(A_0'(B_0' + B_0) + A_0(B_0 + B_0')) + A_1'B_1'A_0'B_0 + A_1B_1A_0'B_0 \\
&= A_1'B_1((B_0' + B_0)(A_0' + A_0)) + (A_1'B_1' + A_1B_1)A_0'B_0 \\
&= A_1'B_1 + \overline{(A_1 \oplus B_1)}A_0'B_0 \qquad [Since, A + A' = 1; AB + A'B' = \overline{(A \oplus B)}]
\end{aligned}
$$

$$
\begin{aligned}
&G(A_1, A_0, B_1, B_0) \\
&= A_1'A_0B_1'B_0' + A_1A_0'B_1'B_0' + A_1A_0'B_1'B_0 + A_1A_0B_1'B_0' + A_1A_0B_1'B_0 + A_1A_0B_1'B_0 \\
&= A_1B_1'(A_0'B_0' + A_0'B_0 + A_0B_0' + A_0B_0) + A_1'B_1'A_0B_0' + A_1B_1A_0B_0' \\
&= A_1B_1'(A_0'(B_0' + B_0) + A_0(B_0 + B_0') + A_1'B_1'A_0B_0' + A_1B_1A_0B_0' \\
&= A_1B_1'((B_0' + B_0)(A_0' + A_0)) + (A_1'B_1' + A_1B_1)A_0B_0' \\
&= A_1B_1' + \overline{(A_1 \oplus B_1)}A_0B_0' \qquad [Since, A + A' = 1; AB + A'B' = \overline{(A \oplus B)}]
\end{aligned}
$$

$$
\begin{aligned}
&E(A_1, A_0, B_1, B_0) \\
&= A_1A_0B_1B_0 + A_1A_0B_1'B_0' + A_1'A_0'B_1'B_0' + A_1'A_0'B_1B_0 \\
&= A_1B_1(A_0B_0 + A_0'B_0') + A_1'B_1'(A_0B_0 + A_0'B_0') \\
&= (A_1B_1 + A_1'B_1')(A_0B_0 + A_0'B_0') \\
&= \overline{(A_0 \oplus B_0)}\ \overline{(A_1 \oplus B_1)}
\end{aligned}
$$

1.5 Circuit Diagram

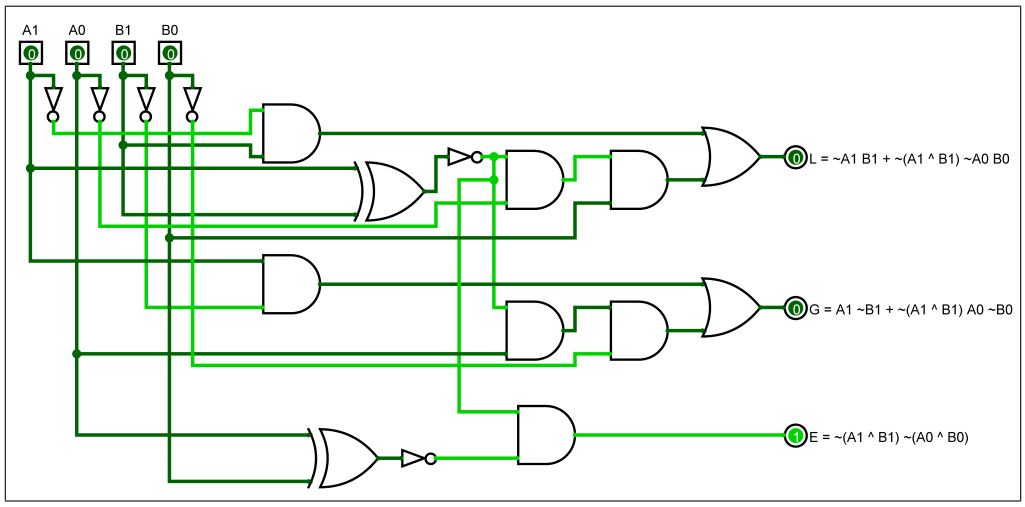

Figure 1: Circuit diagram for problem 1

Problem 2

2.1 Problem Specification

Design a 1-bit full subtractor circuit using basic logic gates. Inputs are P, Q and R denoting minuend, subtrahend and previous borrow respectively. The outputs are D and B representing the difference and output borrow.

2.2 Required Instruments

1. IC-7404 (Quantity: 1)
2. IC-7408 (Quantity: 1)
3. IC-7432 (Quantity: 1)
4. IC-7486 (Quantity: 1)
5. Input Pins (Quantity: 3)
6. Output Pin (Quantity: 2)
7. Wires
8. Software: Logisim

2.3 Truth Table

P	**Q**	**R**	**D**	**B**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

2.4 Boolean Expression (with Simplification)

$$
\begin{aligned}
D &= P'Q'R + P'QR' + PQ'R' + PQR \\
&= P'(Q'R + QR') + P(Q'R' + QR) \\
&= P'(Q'R + QR') + P(Q'R' + QR) \\
&= \overline{P}(Q \oplus R) + P\overline{(Q \oplus R)} \\
&= P \oplus Q \oplus R
\end{aligned}
$$

$$
\begin{aligned}
B &= P'Q'R + P'QR' + P'QR + PQR \\
&= P'R(Q + Q') + P'Q(R + R') + QR(P + P') \\
&= P'R + P'Q + QR
\end{aligned}
$$

2.5 Circuit Diagram

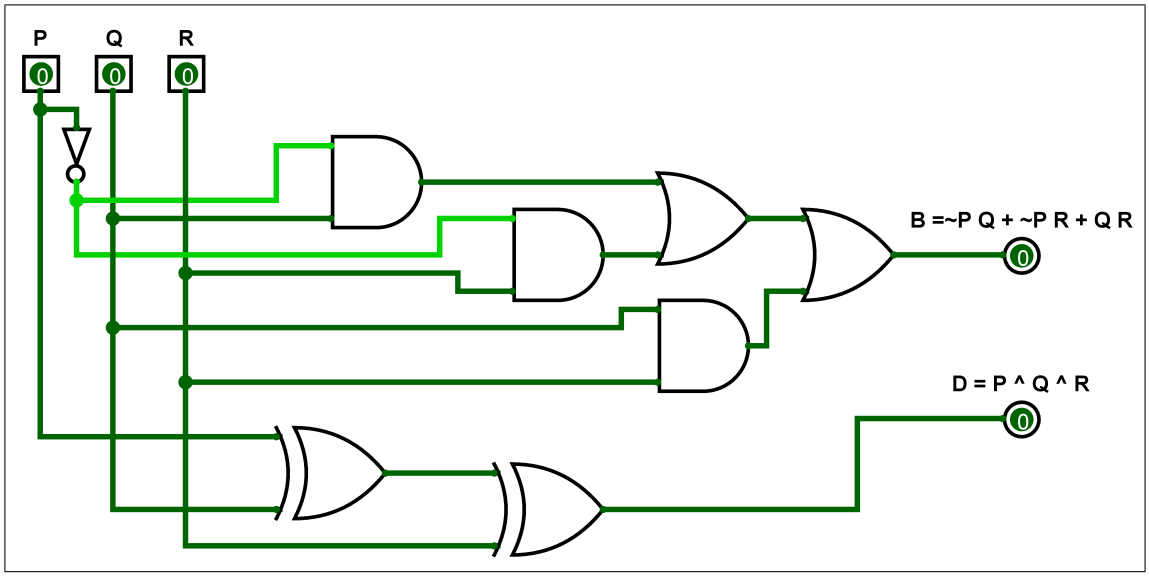

Figure 2: Circuit diagram for problem 2