Bangladesh University of Engineering and Technology

Department of Computer Science and Engineering

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CSE 206
Digital Logic Design Sessional
Offline 3

Group No 2

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Problem 1

1.1 Problem Specification

Design and implementation of a **master-slave JK** flip-flop using only **NAND** gates.

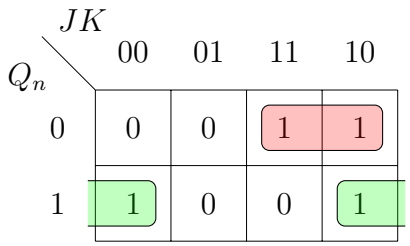
1.2 Required Instruments

1. IC-7400 (Quantity: 4)
2. Input Pins (Quantity: 2)
3. Output Pin (Quantity: 2)
4. Clock signal (Quantity: 1)
5. Wires
6. Software : Logisim

1.3 Excitation Table

C	J	K	Q_n	Q_{n+1}
0	x	x	0	0
0	x	x	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

1.4 Karnaugh Map:



$$Q_{n+1} = K'Q_n + JQ_n'$$

1.5 Circuit Diagram

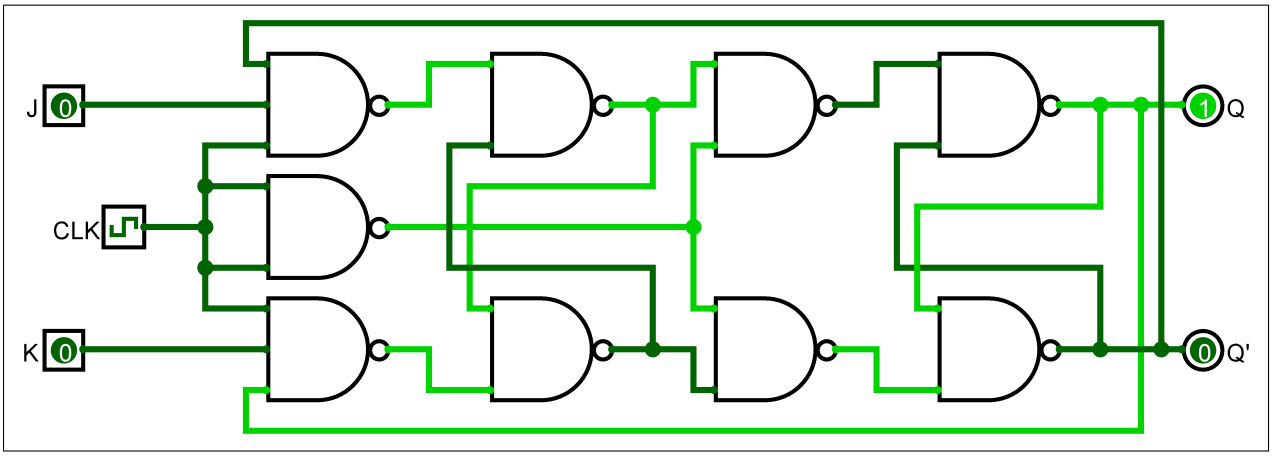


Figure 1: Circuit diagram for problem 1

1.6 Observations

1. Initially, the circuit is stuck in an infinite error loop. This is because, in the beginning, the gates have no output; and since an output of one gate is the input of another, this error propagates in a loop. In such a state, an outside input is provided to give an initial acceptable state to the NAND gates. Then operations resume as intended.

2. When the clock signal is set high, the "Master" will act like a normal JK flip-flop, except for when both J and K are set 1. Since there are feedback lines from the "slave", the "Toggle" occurs only once in this case.

3. When the clock signal is set low, all further changes in the "Master" are prevented ie. it enters "Hold" state. At the same time, the "Slave" Flip-Flop uses the Q and Q' of the "Master" as its J and K inputs (so, both cannot be 1 at the same time). This allows it to settle on a single output per clock pulse, which was a problem for the general JK Flip-Flop.

Problem 2

2.1 Problem Specification

Design and implementation a 4-bit universal shift register.

2.2 Required Instruments

1. IC-7402 (Quantity: 1)
2. IC-7404 (Quantity: 1)
3. IC-7408 (Quantity: 4)
4. IC-7427 (Quantity: 2)
5. IC-7474 (Quantity: 2)
6. Input Pins (Quantity: 9)
7. Output Pin (Quantity: 4)
8. Wires
9. Software: Logisim

2.3 Excitation Table

Clear	S_0	S_1	Clock	D_A	D_B	D_C	D_D	Mode
H	X	X	X	0	0	0	0	Async Clear
L	L	L	X	D_A	D_B	D_C	D_D	Clock Inhibit
L	L	H	1	D_B	D_C	D_D	L_i	Shift Left
L	H	L	1	R_i	D_A	D_B	D_C	Shift Right
L	H	H	1	A	B	C	D	Parallel Load

$$CK = \overline{Clock + \overline{S_0} \cdot \overline{S_1}}$$

$$D_A = Q_B\overline{S_0} + R_i\overline{S_1} + AS_0S_1$$
$$D_B = Q_C\overline{S_0} + Q_A\overline{S_1} + BS_0S_1$$
$$D_C = Q_D\overline{S_0} + Q_B\overline{S_1} + CS_0S_1$$
$$D_D = L_i\overline{S_0} + Q_C\overline{S_1} + DS_0S_1$$

2.4 Circuit Diagram

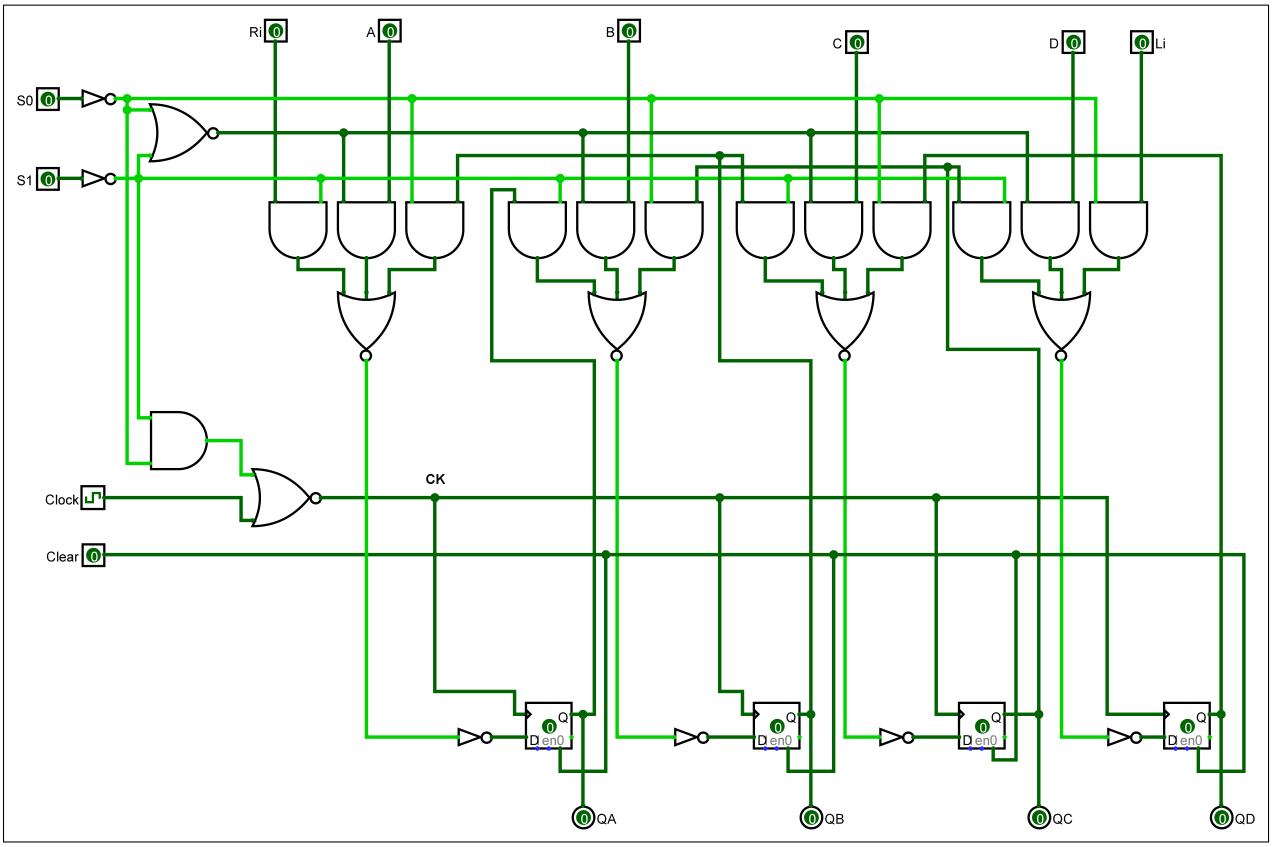


Figure 2: Circuit diagram for problem 2

2.5 Observations

1. The D Flip-Flop ICs used (IC-7474) in our circuit are positive edge-triggered.
2. We have used active-high signal for our clear bit, i.e, the output bits will be set 0 when *Clear=1*. This will override all other inputs.
3. We had to apply negative clock-pulse to the ICs before manipulating our mode selection bits. Otherwise, the circuit would behave abnormally. This might be a limitation of Logisim.
4. Both 2 input NOR (IC-7402) and 3 input NOR (IC-7427) were used to reduce complexity.