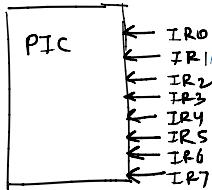


**PIC**

1. [2+2=4 points] Suppose, you need to service 48 hardware interrupts on your 8086 microprocessor. Explain how many 8259 (PIC) chips you'd need to service the above number of interrupts. Further, explain why only a total of 64 interrupts can be serviced with the help of cascading.

We need a total of 7 PICs to service 48 hardware interrupts.



We can connect 6 PICs from IR0 to IR5 since we know each cascaded PIC can provide 8 interrupt signals. IR6 and IR7 are grounded.

Therefore cascading 6 PICs gives  $6 \times 8 = 48$  sources of interrupt signals.

The 7<sup>th</sup> PIC is the original one that is connected to the 8086.

(Note: Saying we need 6 PICs is also okay as we can ignore the 7<sup>th</sup> one connected to the 8086.)

With cascading, we can connect up to 8 PICs, each being able to provide 8 different interrupts. Therefore, total  $8 \times 8 = 64$  sources of interrupt signals.

**Memory Banks**

1. [4 points] Explain in how many different ways data can be accessed from the Memory, assuming the memory is divided into even and odd banks? You must explain using the proper values of A0 and BHE' pins. Why does accessing 16-bit data with an odd starting address require 2 bus cycles instead of 1?

- One byte of data from even address. eg: mov AH, [1234h]. 1 Cycle.  
 $A_0 = 0, BHE' = 0$ . This accesses the byte of data from the low bank and transfers the data in  $D_0 - D_7$ .
  - One byte of data from odd address. eg: - mov AH, [1233h]. 1 Cycle.  
 $A_0 = 1, BHE' = 0$ . This accesses the byte of data from the high bank and transfers the data in  $D_8 - D_{15}$ .
  - Two bytes of data from even address. eg: - mov AX, [4432h]. 1 Cycle.  
 $A_0 = 0, BHE' = 0$ . This accesses the one byte data in [4432h] and transfers to  $D_0 - D_7$  and one byte in [4433h] and transfers to  $D_8 - D_{15}$ .
  - Two bytes from odd address. eg: - mov AX, [4433h]
- |                                                                                         |                                                                                                      |
|-----------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|
| <u>1<sup>st</sup> Cycle</u><br>$A_0 = 1, BHE' = 0$ . Transfers data in $D_8 - D_{15}$ . | <u>2<sup>nd</sup> Cycle</u><br>$A_0 = 0, BHE' = 1$ . Transfers data in $D_0 - D_7$ from the odd bank |
|-----------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|
- We can provide the argument here that if we wish to access two bytes in one cycle, then we need to set  $A_0 = 0$  and  $BHE' = 0$ . However, this will always default to accessing 2 bytes from the even bank.

## Timing Diagram

1. [1 + 1.5 + 1.5 = 4 points] Assume an 8086 has been set to operate at 30 Mhz and at 40% duty cycle. Calculate:

- Time for 1 clock pulse
- Time for 1 bus cycle
- Total time in nanoseconds each clock pulse stays low

- one clock pulse  $\rightarrow \frac{1}{30 \times 10^6}$  s
- one bus cycle  $\rightarrow \frac{4}{30 \times 10^6}$  s
- If duty cycle is 40%, then the clock pulse stays low for 60% of the time.

$$\text{time} = \frac{4}{30 \times 10^6} \times 0.6 \times 10^9 \text{ ns}$$

2. [4 points] Draw the timing diagram of the Write cycle of an Intel 8086 that is trying to write data to an external I/O. Your diagram must show the states of the following pins:

*Ignore.*

## Interrupt

1. [2 points] Calculate the locations of CS and IP of the ISR for the interrupt **TYPE 123**  $\leftarrow 123$
2. [2 points] Suppose, the CS of the ISR of an interrupt is found to be in the memory location ~~2B3h~~  
~~2BEh~~. What could be the type of the interrupt?

Type 123

- $123 \times 4 = 492$       ∴ lower byte of IP in 001EC<sub>h</sub>, upper byte in 001ED<sub>h</sub>.
- lower byte of CS in 001EE<sub>h</sub>, upper byte in 001EF<sub>h</sub>.
- $492 = 001EC\text{h}$

Assume CS lower byte is found in 2BE<sub>h</sub>.  
Therefore IP " " " " 2BC<sub>h</sub>.

$$2BC\text{h} = 700$$

$$\text{Then } \frac{700}{4} = 175 \quad \therefore \text{Interrupt type 175.}$$