Ans: to the que no: 01

a)

$$\text{Time for 1 clock pulse} = \frac{1}{11.5 \times 10^6} \times \frac{1}{10^{-9}}$$

$$= 86.95 \text{ ns}$$ Ans

b)

$$\text{Time for 1 bus cycle} = 86.95 \times 4$$

$$= 347.8 \text{ ns}$$ Ans

c)

$$T_{on} = 86.95 \times 40\% = 34.78 \text{ ns}$$

$$T_{off} = 86.95 - 34.78 = 52.17 \text{ ns}$$

$$\text{Total } T_{off} = 52.17 \times 4 = 208.68 \text{ ns}$$ Ans

d)

$$1 \text{ bus cycle} = 347.8 \text{ ns}$$

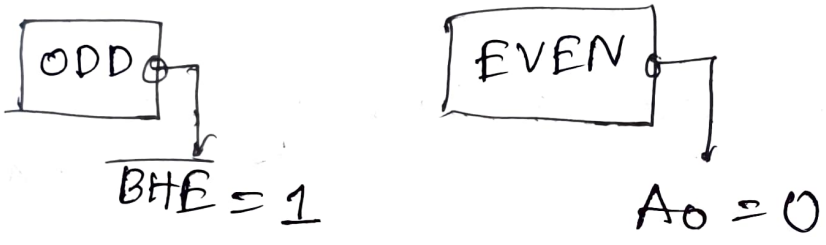
$$2 \text{ " " } = 347.8 \times 2$$

$$= 695.6 \text{ ns}$$ Ans

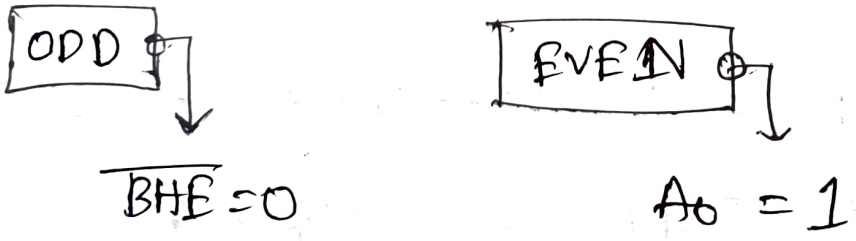
Ans: to the que no: 3

a) There are 4 ways it is possible.

① 8 bit from Even Bank



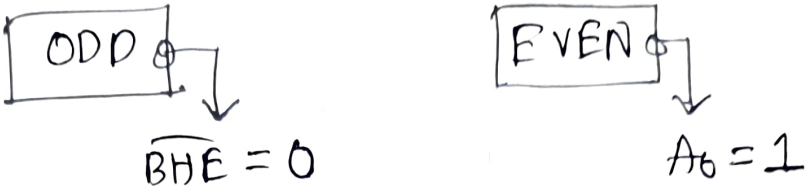
② 8 bit from ODD Bank



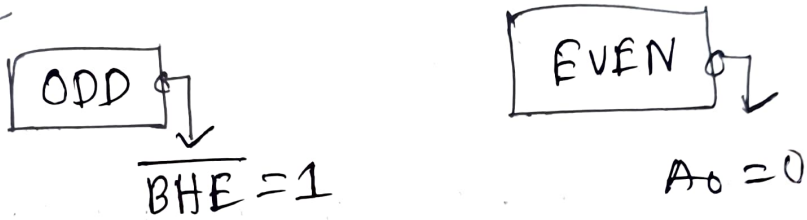
③ 16 bit from EVEN - ODD (Aligned)

④ 16 bit from ODD Bank (Unaligned)

1st cycle:



2nd cycle:



b) When we want to access 16-bit data with an odd starting address we have to first get the odd part from odd bank and then in another cycle from even bank. As the data is unaligned it is not possible to access both banks at one go if it starts from an odd location.

Ans: to the que no: 4

nn = 123

IP = (123 × 4)

= 492

= 001ECh

IP = lower → 001ECh

IP higher → 001EDh

CS = (123 × 4) + 2

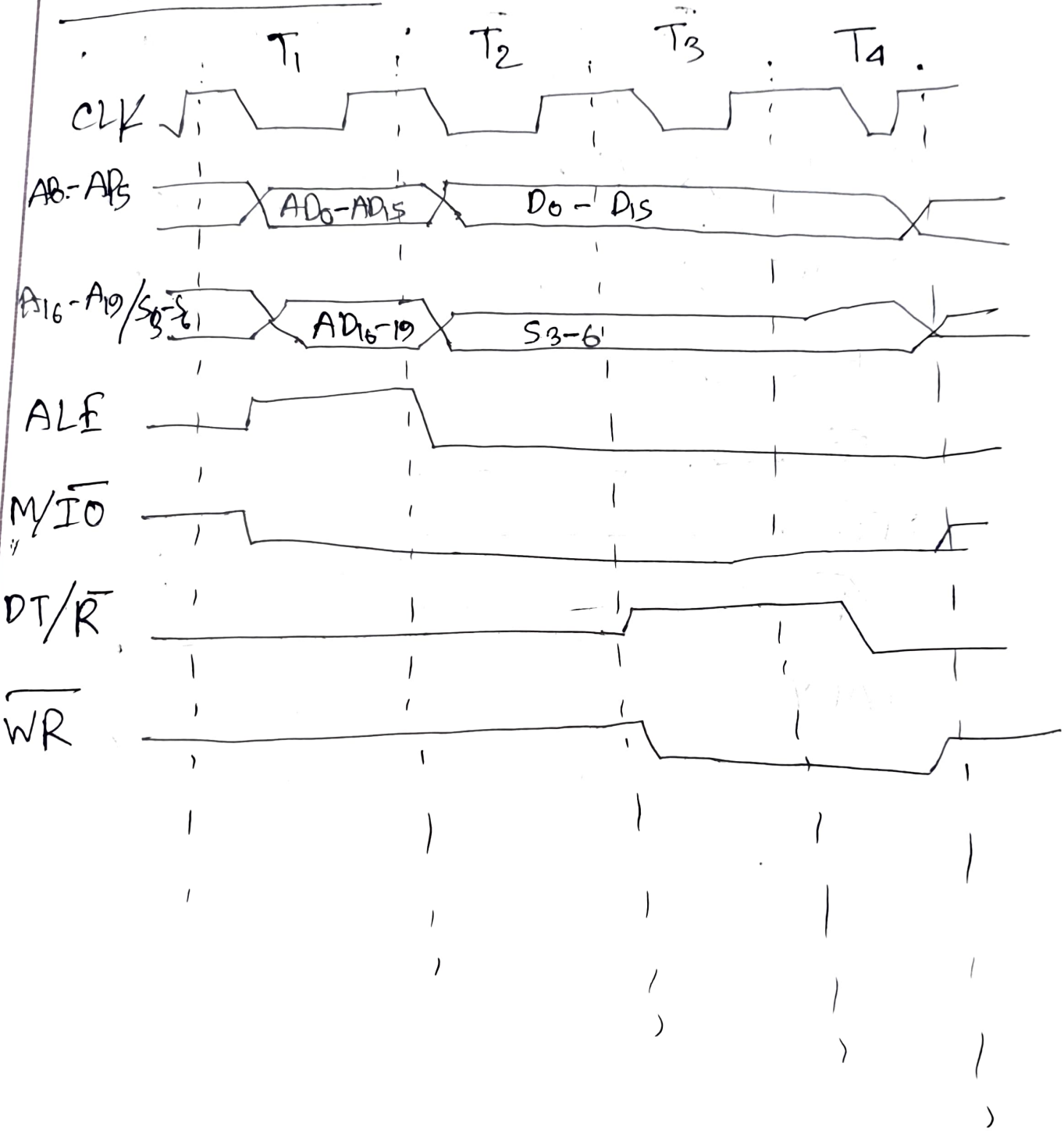
= 494

= 001EEh

∴ CS low → 001Ef

Ans: to the que no: 02 (a)

WRITE to I/O



(b) Read to memory: