CHAPTER 14

Semiconductor Electronics

Energy Band in Solids and Basics of Semiconductor

1. The solids which have the negative temperature coefficient of resistance are: **[RC]** *(2020)*

a. Insulators only
b. Semiconductors only
c. Insulators and semiconductors
d. Metals

Intrinsic and Extrinsic Semiconductor (P and N types)

2. The electron concentration in an n-type semiconductor is the same as hole concentration in a p-type semiconductor. An external field (electric) is applied across each of them. Compare the currents in them. *(2021)*

a. current in p-type > current in n-type.
b. current in n-type > current in p-type.
c. No current will flow in p-type, current will only flow in n-type.
d. current in n-type = current in p-type.

3. An intrinsic semiconductor is converted into n-type extrinsic semiconductor by doping it with *(2020-Covid)*

a. Aluminium b. Silver
c. Germanium d. Phosphorous

4. For a p-type semiconductor, which of the following statements is true? *(2019)*

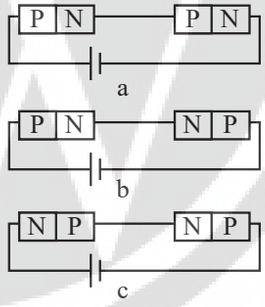
a. Electrons are the majority carriers and trivalent atoms are the dopants.
b. Holes are the majority carriers and trivalent atoms are the dopants.
c. Holes are the majority carriers and pentavalent atoms are the dopants.
d. Electrons are the majority carriers and pentavalent atoms are the dopants.

5. In a n-type semiconductor, which of the following statement is true? *(2013)*

a. Holes are majority carriers and trivalent atoms are dopants
b. Electrons are majority carriers and trivalent atoms are dopants
c. Electron are minority carriers and pentavalent atoms are dopants
d. Holes are minority carriers and pentavalent atoms are dopants

P-N Junction Diode (forward and reverse bias), Diffusion and Drift Current

6.



In the given circuits (a), (b) and (c), the potential drop across the two p-n junctions are equal in: *(2022)*

a. Both circuits (a) and (c) b. Circuit (a) only
c. Circuit (b) only d. Circuit (c) only

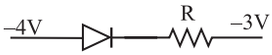
7. Out of the following which one is a forward biased diode? *(2020-Covid)*

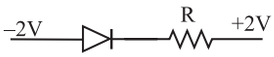
a. 2V ——▷|—/\/\/\— 5V
b. –2V ——▷|—/\/\/\— +2V
c. 0V ——▷|—/\/\/\— –3V
d. –4V ——▷|—/\/\/\— –2V

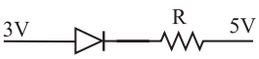
8. The increase in the width of the depletion region in a p-n junction diode is due to : *(2020)*

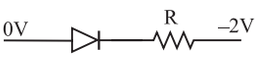
a. Reverse bias only
b. Both forward bias and reverse bias
c. Increase in forward current
d. Forward bias only

9. Which one of the following represents forward bias diode? *(2017-Delhi, 2006)*

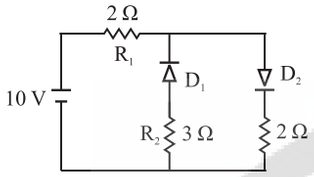
a. 

b. 

c. 

d. 

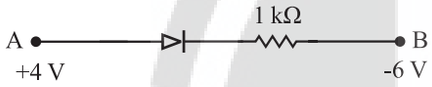
10. The given circuit has two ideal diodes connected as shown in the figure below. The current flowing through the resistance R_1 will be: *(2016-II)*



a. 1.43 A b. 3.13 A

c. 2.5 A d. 10.0 A

11. Consider the junction diode as ideal. The value of current flowing through AB is: *(2016-I)*

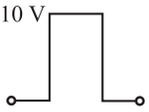


a. 0 A b. 10^{-2} A

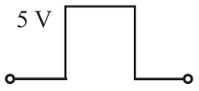
c. 10^{-1} A d. 10^{-3} A

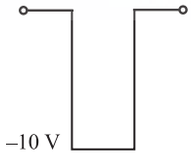
12. If in a p-n junction, a square input signal of 10 V is applied, as shown

then the output across R_L will be: *(2015)*

a. 

b. 

c. 

d. 

Characteristics of P-N Junction

13. In a p-n junction diode, change in temperature due to heating *(2018)*

a. Does not affect resistance of p-n junction

b. Affects only forward resistance

c. Affects only reverse resistance

d. Affects the overall V–I characteristics of p-n junction

14. The barrier potential of a p-n junction depends on: *(2014)*

a. Type of semiconductor material

b. Amount of doping

c. Temperature

Which one of the following is correct?

a. a and b only

b. b only

c. b and c only

d. a, b and c

Diode as a Rectifier

15. In half wave rectification, if the input frequency is 60 Hz, then the output frequency would be: *(2022)*

a. 120 Hz b. 0

c. 30 Hz d. 60 Hz

Zener Diode

16. Consider the following statements (A) and (B) and identify the correct answer. *(2021)*

(A) A zener diode is Connected in reverse bias, when used as a voltage regulator.

(B) The potential barrier of p-n junction lies between 0.1 V to 0.3 V.

a. (A) and (B) both are incorrect.

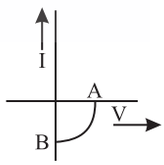
b. (A) is correct and (B) is incorrect.

c. (A) is incorrect but (B) is correct.

d. (A) and (B) both are correct.

Optoelectronic Devices

17. The given graph represents V-I characteristic for a semiconductor device. *(2014)*



Which of the following statement is correct?

a. It is V–I characteristic for solar cell where point A represents open circuit voltage and point B short circuit current

b. It is for a solar cell and points A and B represent open circuit voltage and current, respectively

c. It is for a photo diode and points A and B represent open circuit voltage and current, respectively

d. It is for a LED and points A and B represents open circuit voltage and short circuit current respectively

Transistor

18. For transistor action, which of the following statements is correct? **[RC]** *(2020)*

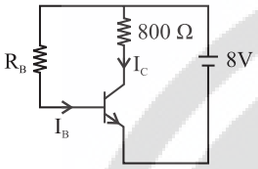
a. Base, emitter and collector regions should have same size.

b. Both emitter junction as well as the collector junction are forward biased.

c. The base region must be very thin and lightly doped.

d. Base, emitter and collector regions should have same doping concentrations.

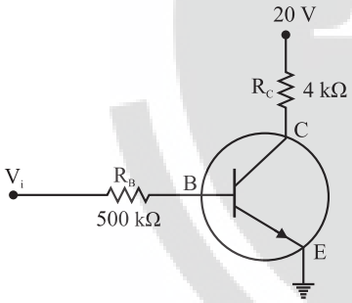
19. A n-p-n transistor is connected in common emitter configuration (see figure) in which collector voltage drop across load resistance (800 Ω) connected to the collector circuit is 0.8 V. The collector current is, **[RC]** *(2020-Covid)*



a. 0.1 mA b. 1 mA

c. 0.2 mA d. 2 mA

20. In the circuit shown in the figure, the input voltage V_i is 20 V, V_{BE} = 0 and V_{CE} = 0. The values of I_B, I_C and β are given by **[RC]** *(2018)*



a. I_B = 20 μA, I_C = 5mA, β = 250

b. I_B = 25 μA, I_C = 5mA, β = 200

c. I_B = 40 μA, I_C = 10 mA, β = 250

d. I_B = 40 μA, I_C = 5mA, β = 125

21. In a common emitter transistor amplifier the audio signal voltage across the collector is 3 V. The resistance of collector is 3 kΩ. If current gain is 100 and the base resistance is 2 kΩ, the voltage and power gain of the amplifier is: **[RC]** *(2017-Delhi)*

a. 15 and 200 b. 150 and 15000

c. 20 and 2000 d. 200 and 1000

22. A npn transistor is connected in common emitter configuration in a given amplifier. A load resistance of 800 Ω is connected in the collector circuit and the voltage drop across it is 0.8 V. If the current amplification factor is 0.96 and the input resistance of the circuit is 192 Ω, the voltage gain and the power gain of the amplifier will respectively be: **[RC]** *(2016-I)*

a. 4, 3.84 b. 3.69, 3.84

c. 4, 4 d. 4, 3.69

23. The input signal given to a CE amplifier having a voltage gain of 150 is $V_i = 2\cos\left(15t + \frac{\pi}{3}\right)$. The corresponding output signal will be: **[RC]** *(2015 Pre)*

a. $300\cos\left(15t + \frac{4\pi}{3}\right)$

b. $300\cos\left(15t + \frac{\pi}{3}\right)$

c. $75\cos\left(15t + \frac{2\pi}{3}\right)$

d. $2\cos\left(15t + \frac{5\pi}{6}\right)$

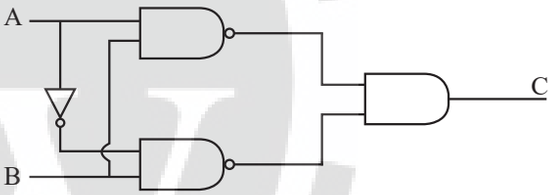
24. In a common emitter (CE) amplifier having a voltage Gain G, the transistor used has transconductance 0.03 mho and current gain 25. If the above transistor is replaced with another one with transconductance 0.02 mho and current gain 20, the voltage gain will be: **[RC]** *(2013)*

a. 5/4 G b. 2/3 G

c. 1.5 G d. 1/3 G

Digital Electronics and Logic Gates

25.



The truth table for the given logic circuit is: *(2022)*

a.

A	B	C
0	0	0
0	1	1
1	0	0
1	1	1

b.

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

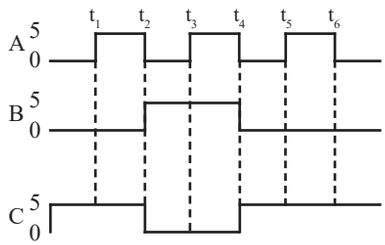
c.

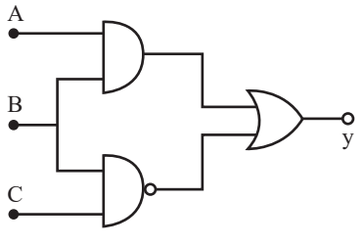
A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

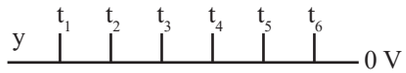
d.

A	B	C
0	0	1
0	1	0
1	0	1
1	1	0

26. For the given circuit, the input digital signals are applied at the terminals A, B and C. What would be the output at the terminal y? *(2021)*





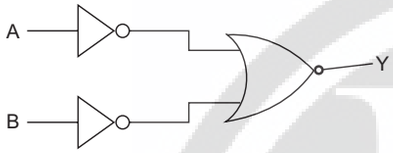
a. 

b. 

c. 

d. 

27. For the logic circuit shown, the truth table is: *(2020)*



a.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

b.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

c.

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

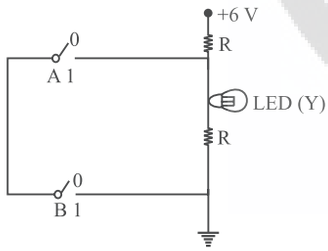
d.

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

28. Which of the following gate is called universal gate? *(2020-Covid)*

a. AND gate
b. NAND gate
c. NOT gate
d. OR gate

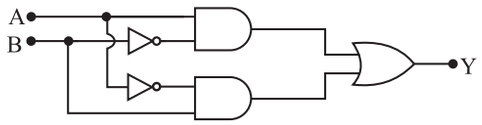
29.



The correct Boolean operation represented by the circuit diagram drawn is: *(2019)*

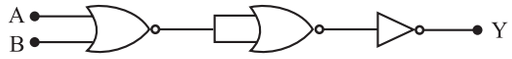
a. AND
b. OR
c. NAND
d. NOR

30. In the combination of the following gates the output Y can be written in terms of inputs A and B as *(2018)*



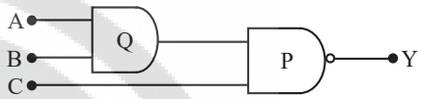
a. $\overline{A.B} + A.B$
b. $A.\overline{B} + \overline{A}.B$
c. $\overline{A.B}$
d. $\overline{A+B}$

31. The given electrical network is equivalent to: *(2017-Delhi)*



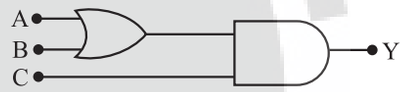
a. OR gate
b. NOR gate
c. NOT gate
d. AND gate

32. What is the output Y in the following circuit, when all the three inputs A, B, C are first 0 and then 1? *(2016-II)*



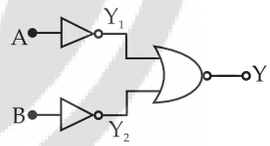
a. 1, 0
b. 1, 1
c. 0, 1
d. 0, 0

33. To get output 1 for the following circuit, the correct choice for the input is: *(2016-I, 2012 Mains, 2010 Pre)*



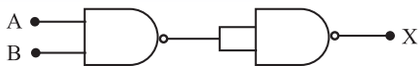
a. A = 0, B = 1, C = 0
b. A = 1, B = 0, C = 0
c. A = 1, B = 1, C = 0
d. A = 1, B = 0, C = 1

34. Which logic gate is represented by the following combination of logic gates? *(2015)*



a. NAND
b. AND
c. NOR
d. OR

35. The output (*X*) of the logic circuit shown in figure will be: *(2013)*



a. $X = \overline{A+B}$
b. $X = \overline{\overline{A}.\overline{B}}$
c. $X = \overline{A.B}$
d. X = A.B

Answer Key

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
c	b	d	b	d	a	c	a	d	c	b	c	d	d	d	b	a
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
c	b	d	b	a	a	b	d	c	d	b	c	b	b	a	d	b
35																
d																