

Assignment: Lets Design an FSM

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Implement an FSM with the following specification:

- The set of input symbols is $\Sigma = \{a, b\}$.
- The set of output symbols is $\Lambda = \{Y, N\}$.

The behaviour of the FSM is as follows:

- The FSM outputs a Y at time instant k only if the last 4 inputs were either

abab
baba

(that is, either $x(k) = a, x(k-1) = b, x(k-2) = a, x(k-3) = b$ or $x(k) = b, x(k-1) = a, x(k-2) = b, x(k-3) = a$). Otherwise the FSM outputs N.

Suppose you are given the following building blocks:

- Inverters, NAND2, NOR2 gates each with a delay of 2 units.
 - D-flipflops with clock \rightarrow q delay of 3 units, set-up time of 2 units and hold-time of 2 units.
1. Design an abstract Mealy machine (identify a potential set of states and next-state, output functions) which implements the required behaviour.
 2. Encode the input, output and state symbols using binary encoding.
 - Try two state encodings: the one-hot encoding and a compact encoding using $\log_2|Q|$ state variables.
 3. Complete the logic network for the FSM based on your encodings. Don't forget to add the reset signal. You may assume that the output is a don't-care when the reset signal is applied.
 4. Confirm, using a VHDL model, that your implementations are correct. Check the following test-case

k	0	1	2	3	4	5	6	7	8	9
x	reset	a	b	b	a	b	a	b	a	a
y	–	N	N	N	N	N	Y	Y	Y	N

5. Characterize the timing of your FSM implementations (find the minimum and maximum values of the input to flop, flop to flop, flop to output and input to output delays).