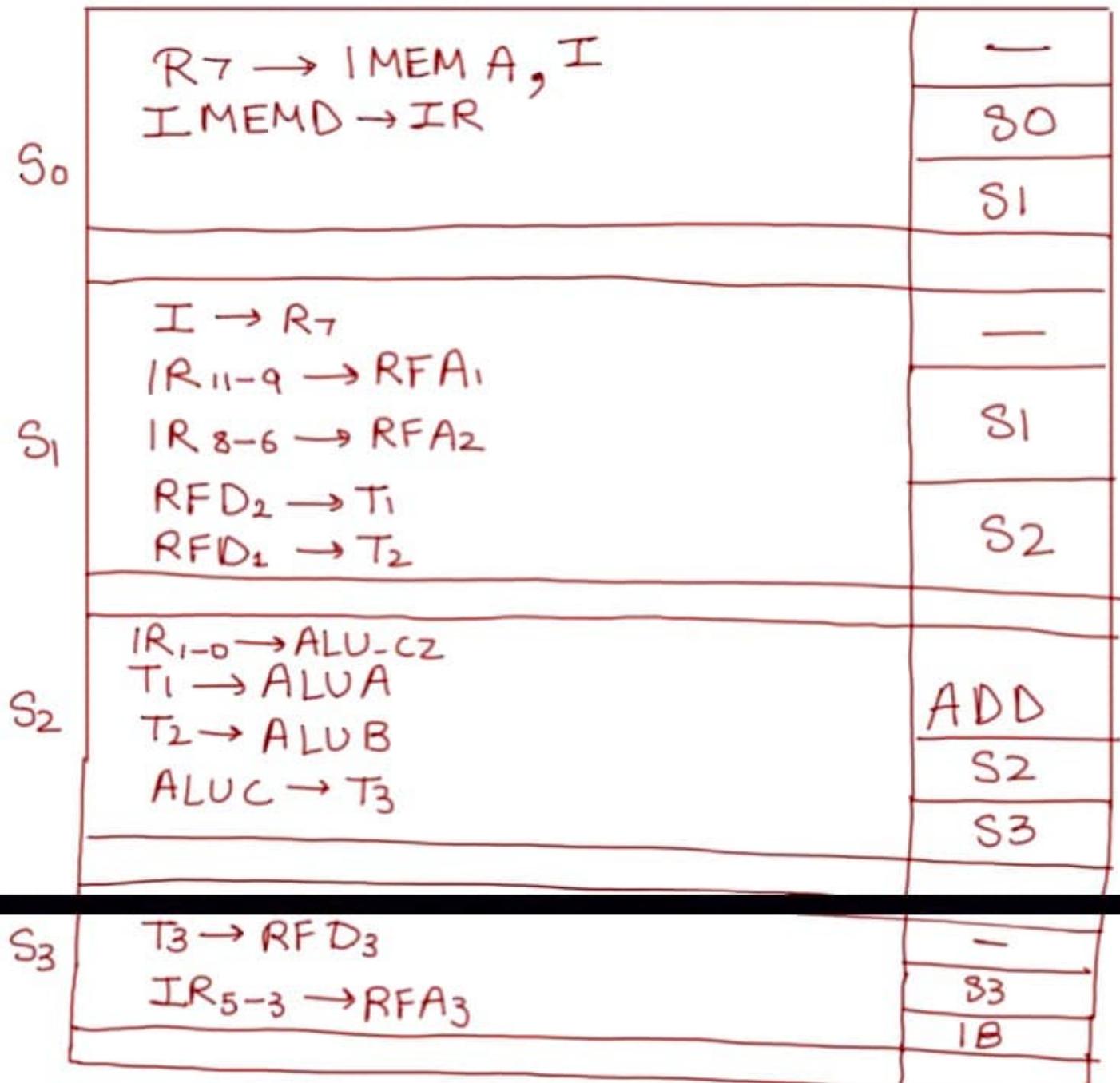


1) ADD - add r_c, r_a, r_b

15	12 11	9 8	6 5	3 2	1	0
Opcode	Register A	Register B	Register C	Unused	CZ	

1 3 3 3 1 2

Add content of reg B to reg A and store result in reg C

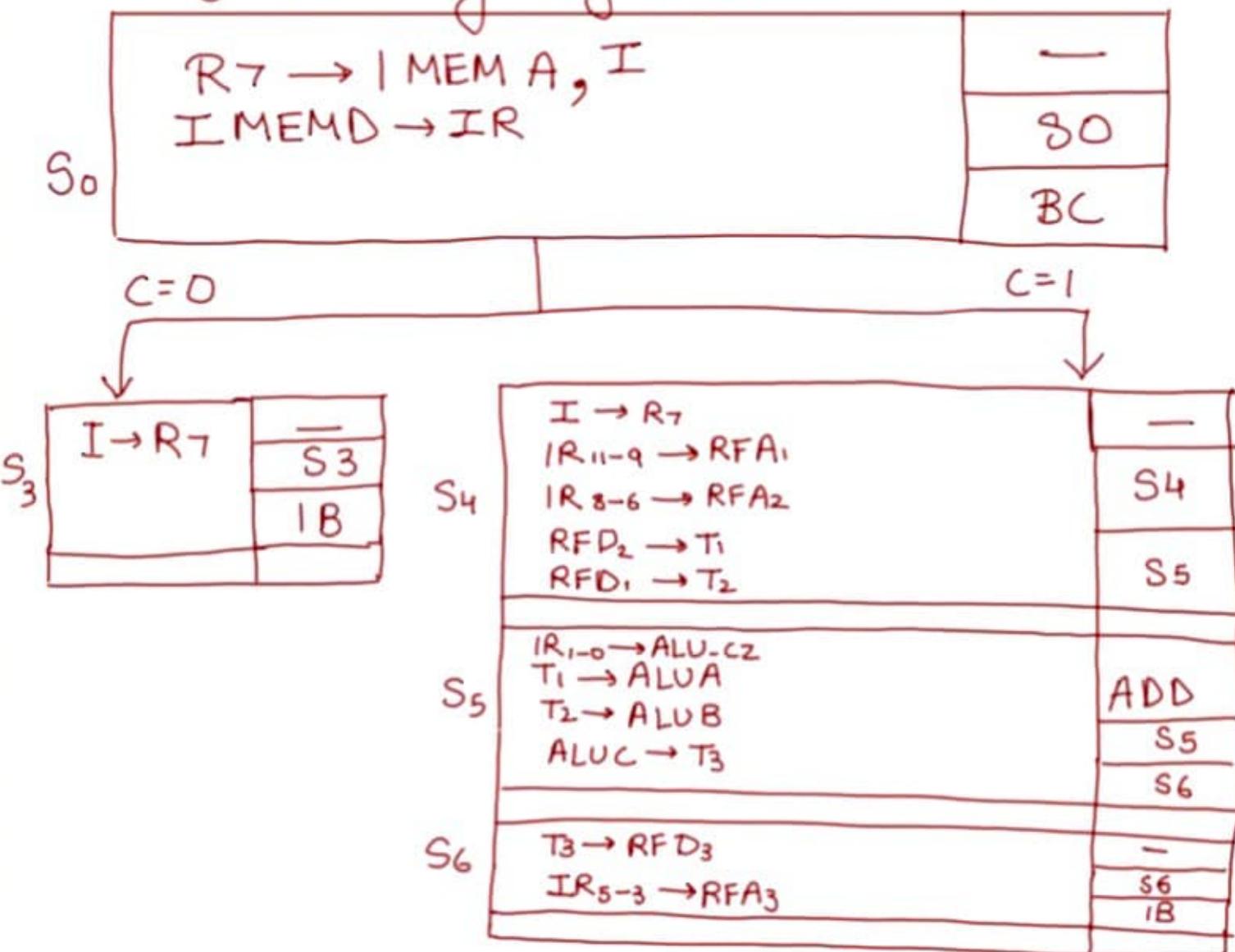


2) ADC - adc rc,ra,rb

15	12 11	9 8	6 5	3 2	1	0
Opcode	Register A	Register B	Register C	Unused	CZ	

1 3 3 3 1 2

Add content of reg B to reg A and store result in reg C, if carry flag is set.

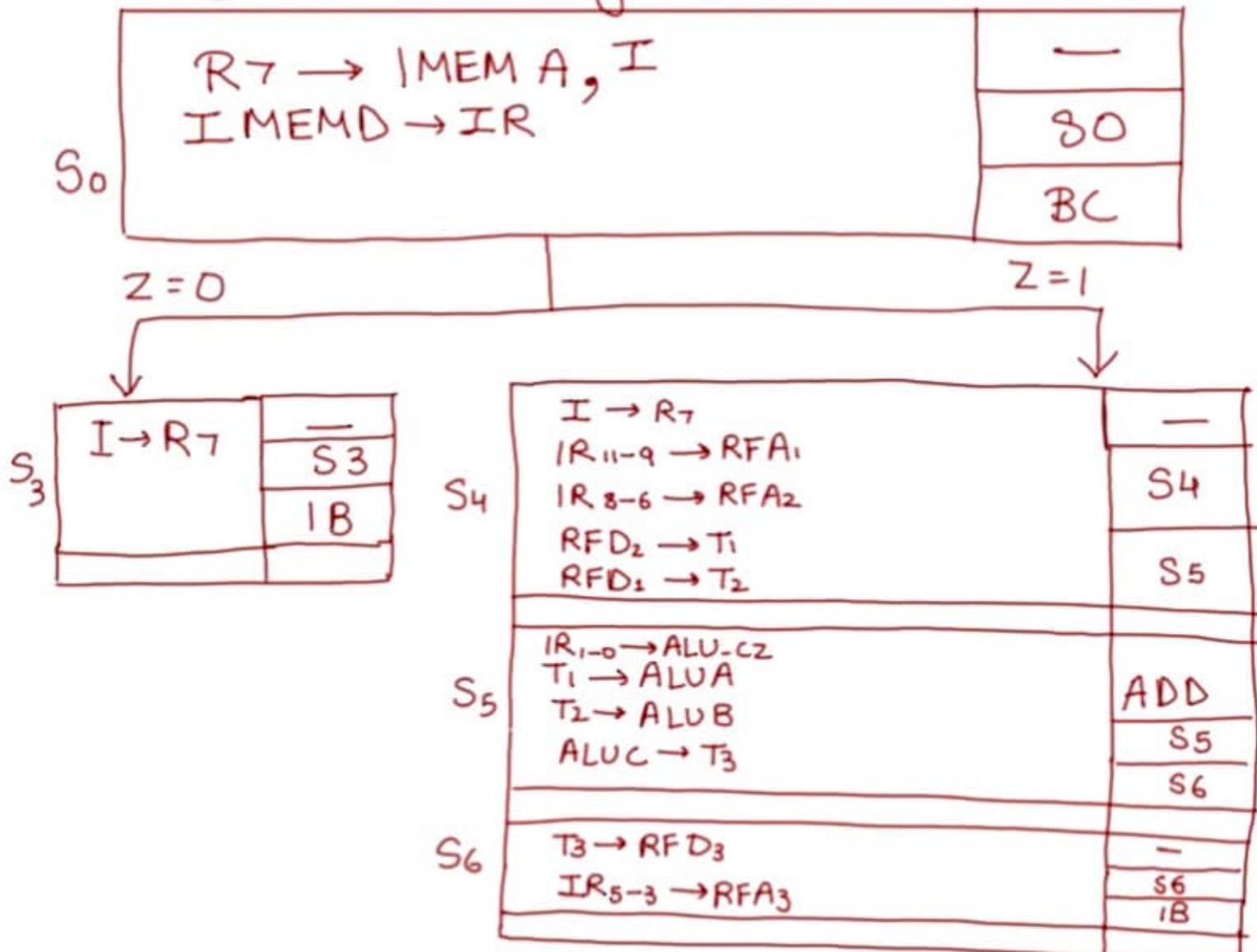


3) ADZ - add regA, regB, regC

15	12 11	9 8	6 5	3 2	1	0
Opcode	Register A	Register B	Register C	Unused	CZ	

1 3 3 3 1 2

Add content of reg B to reg A and store result in reg C, if zero flag is set.

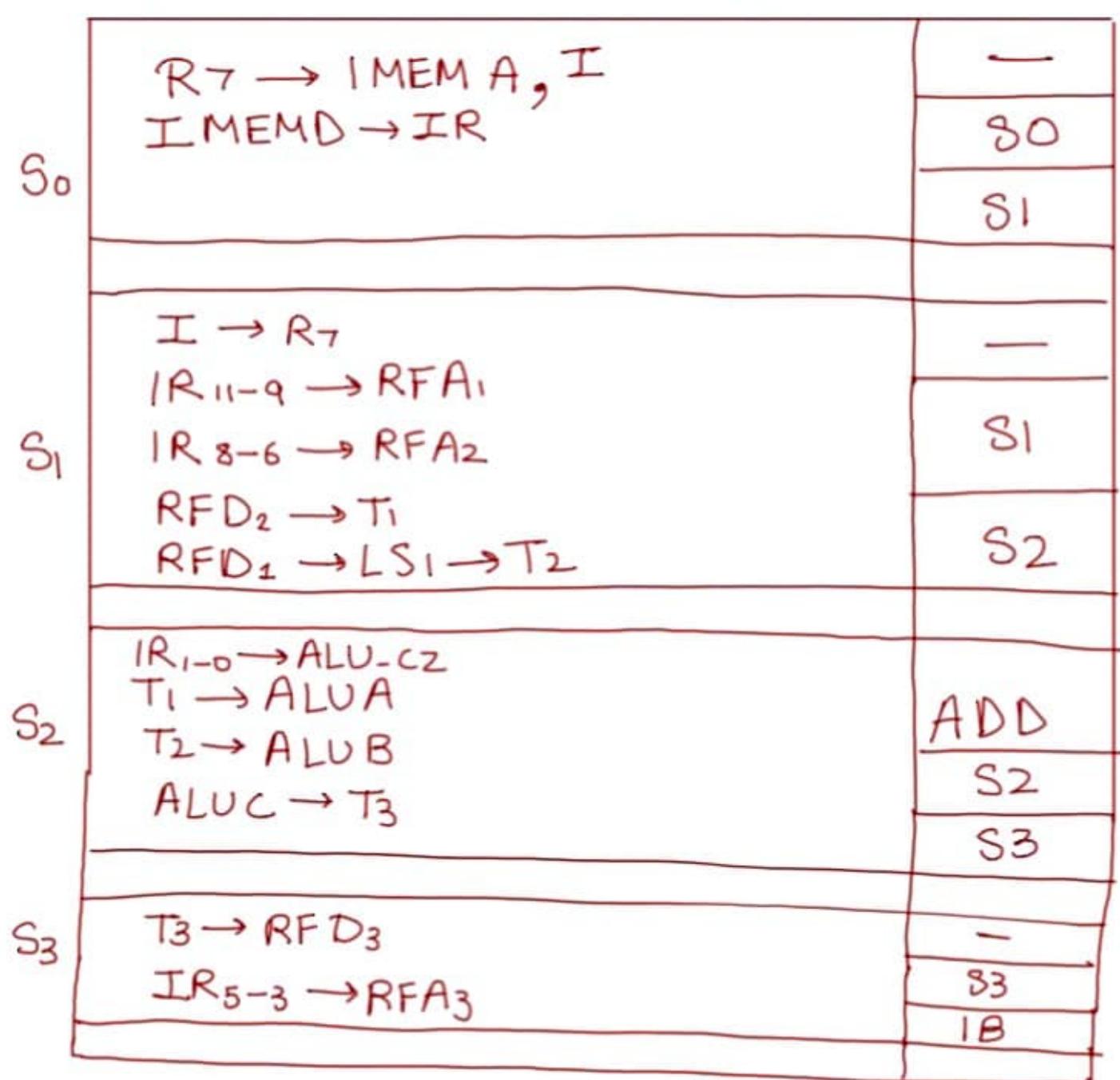


4) ADL - add rc,ra,rb

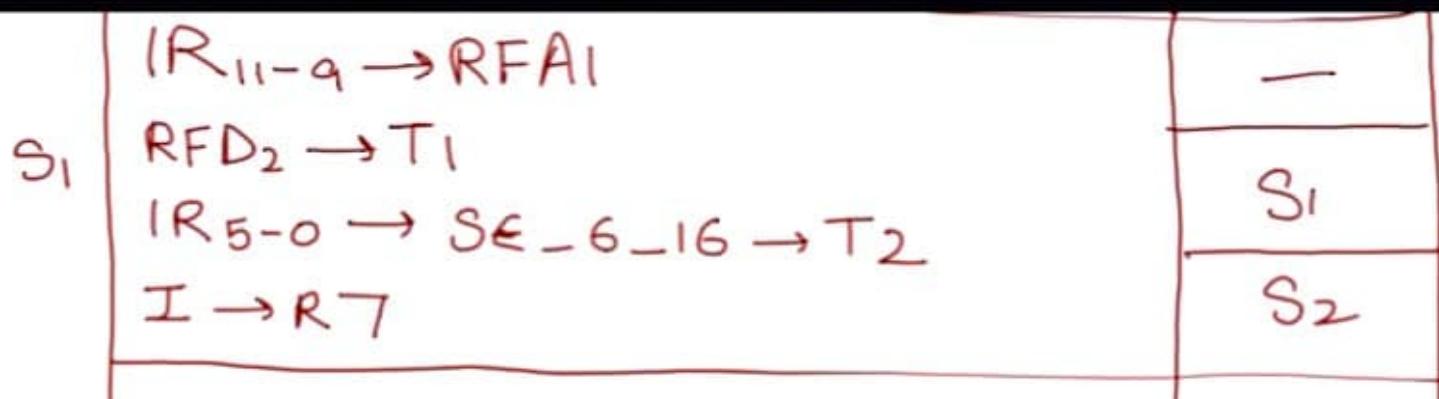
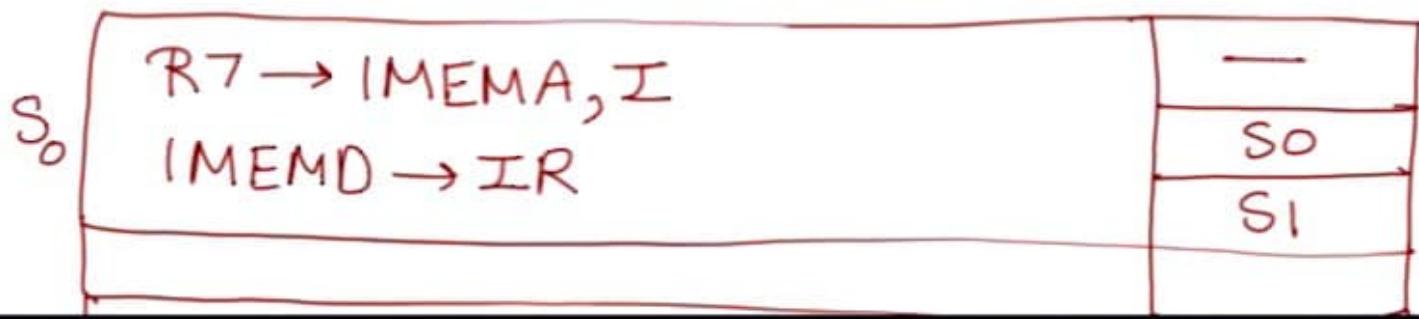
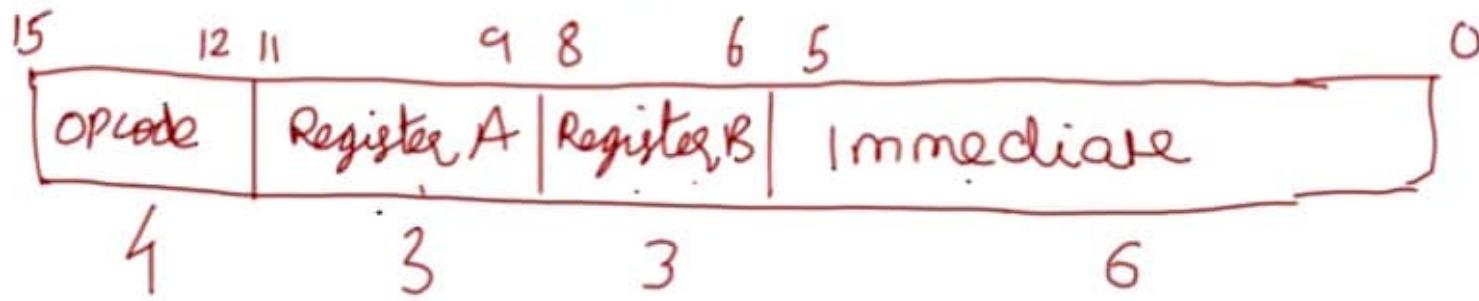
15	12 11	9 8	6 5	3 2	1	0
Opcode	Register A	Register B	Register C	unused	C Z	

1 3 3 3 1 2

Add content of reg B (after one bit left shift)
to reg A and store result in reg C



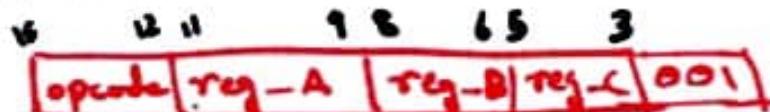
5) ADI - add r_b, r_a, imm_6



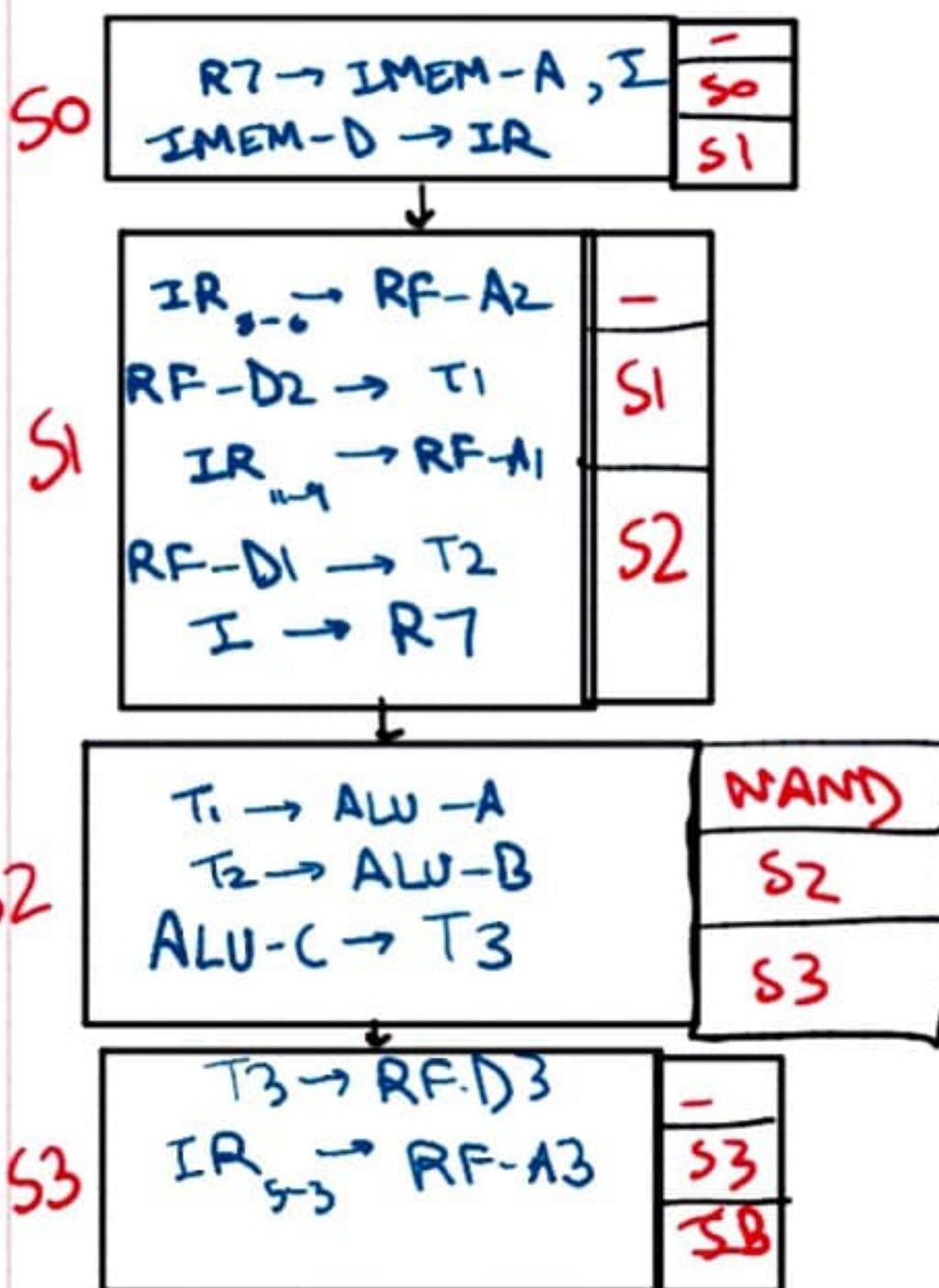
6)

NDU

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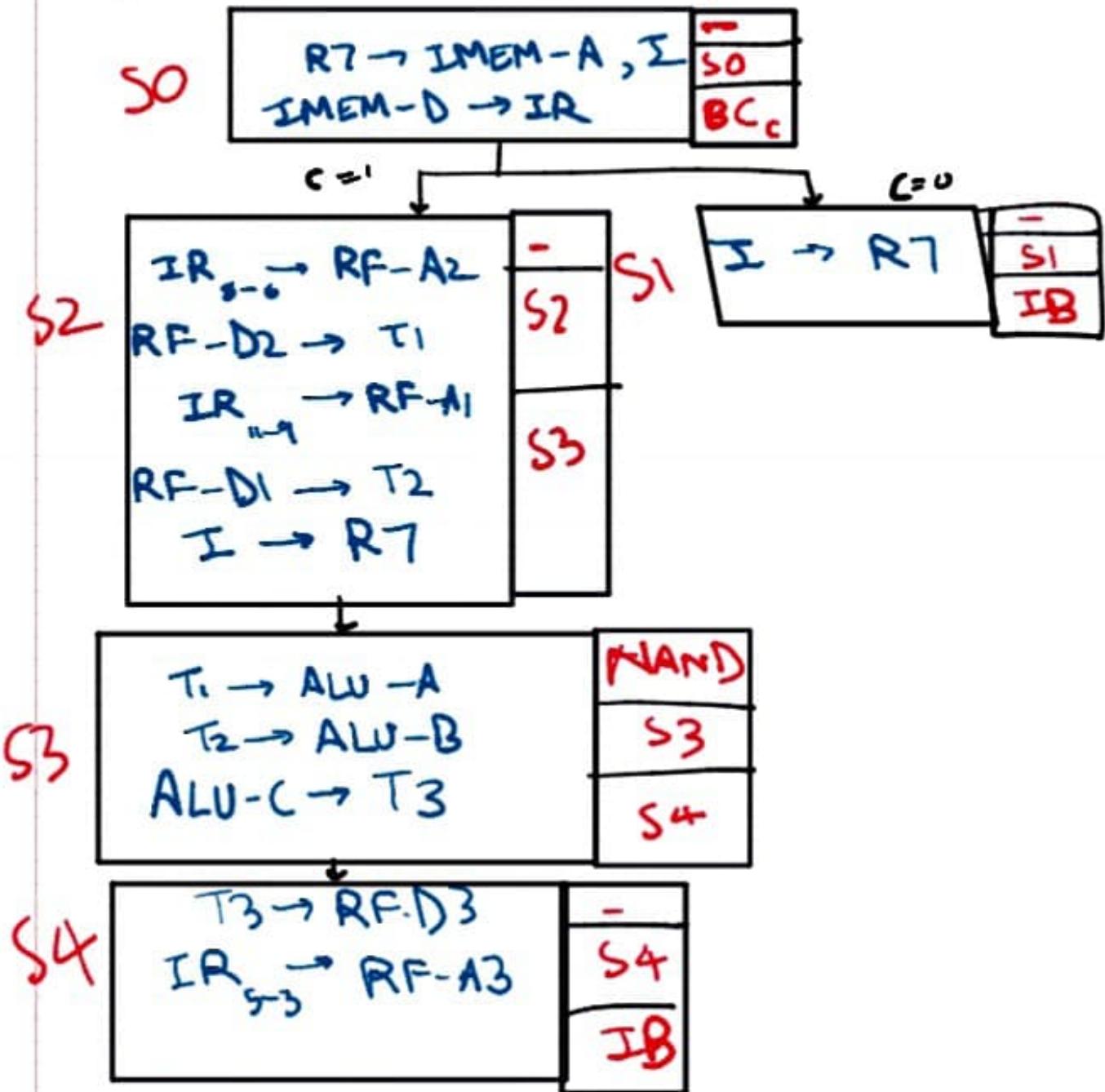
$ND2 \quad TA \quad TB \quad TC \Rightarrow T_C \leftarrow TA \quad NAND \quad rb$



NDC

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6 21 18 65 3
opcode reg-A reg-B reg-C 001
NDC TA TB TC \Rightarrow if C=1, Tc \leftarrow TA NAND rb



8)

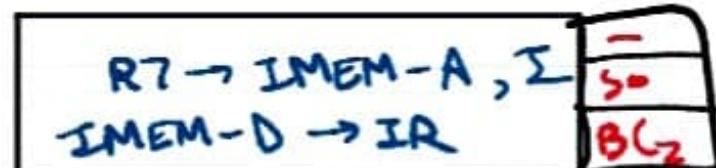
NDZ

Sunday, April 10, 2022 12:58 PM

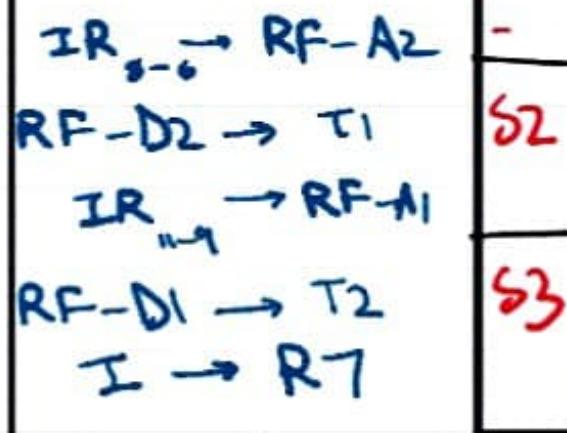
6	11	11	10	65	3
opcode	reg-A	reg-B	reg-C	001	

NDZ TA TB TC \Rightarrow if $z=1$, $T_C \leftarrow T_A$ NAND T_B

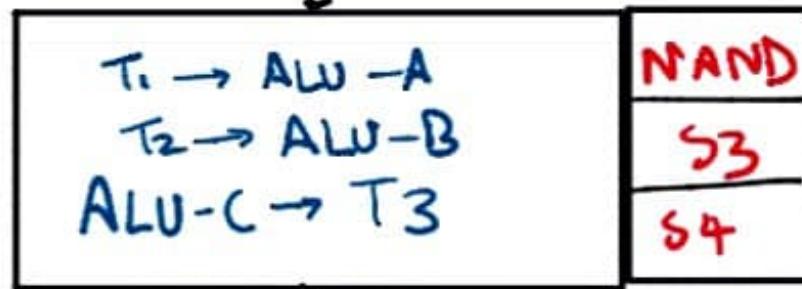
S0



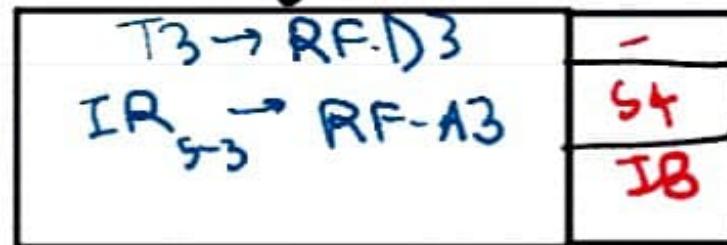
S2



S3



S4



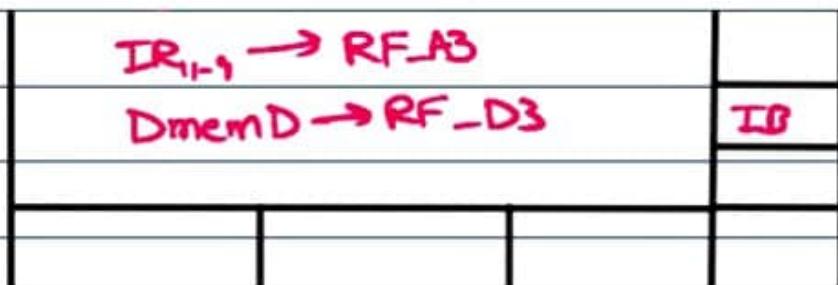
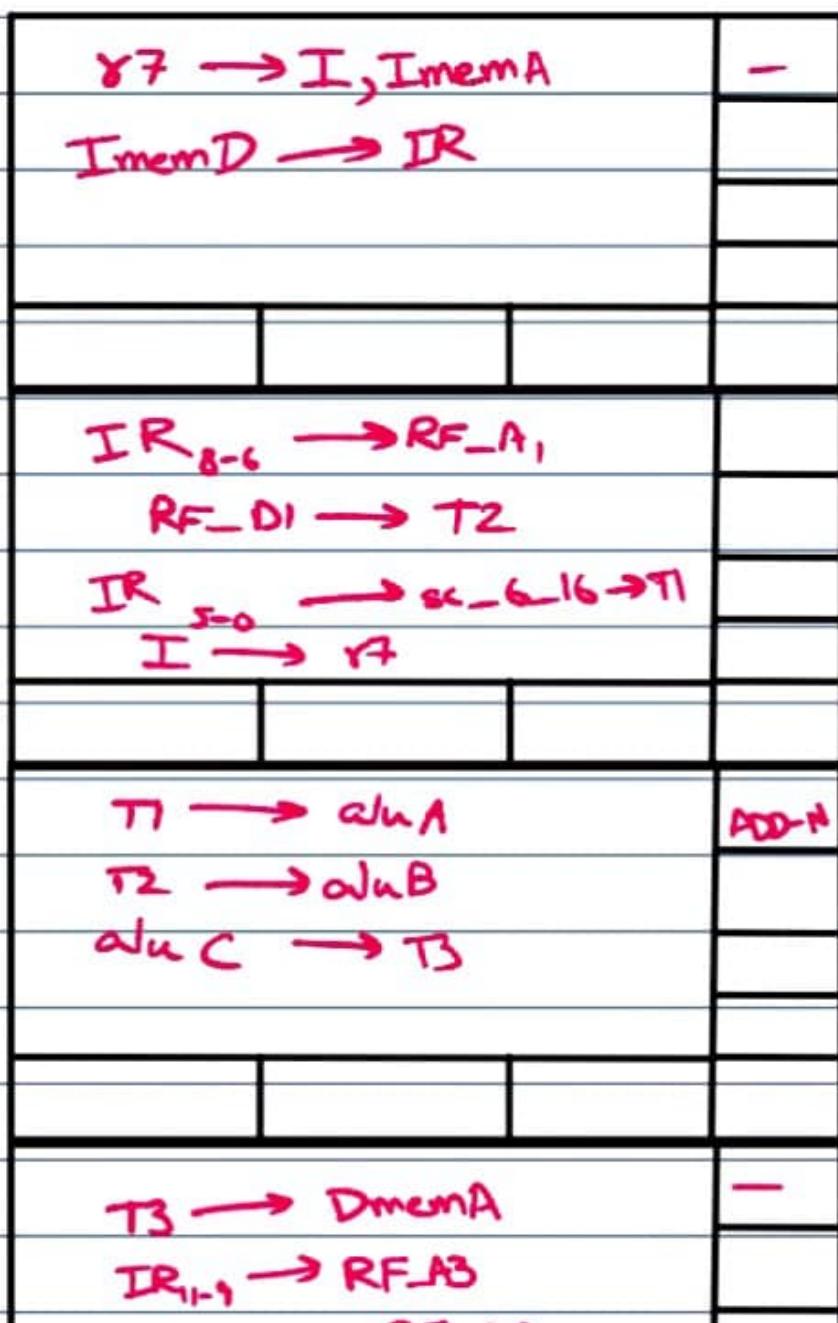
Q) LW:

01-11	RA	RB	6 Immediate
15	1211	98	65

 (I)

Load @ (rb+imm) in ra

lw ra, rb, Imm

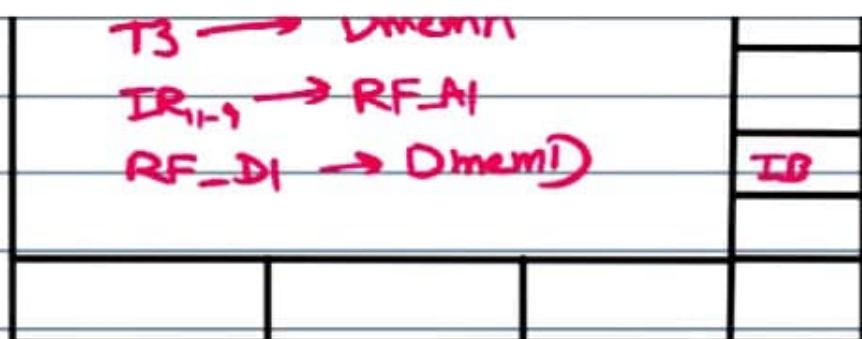
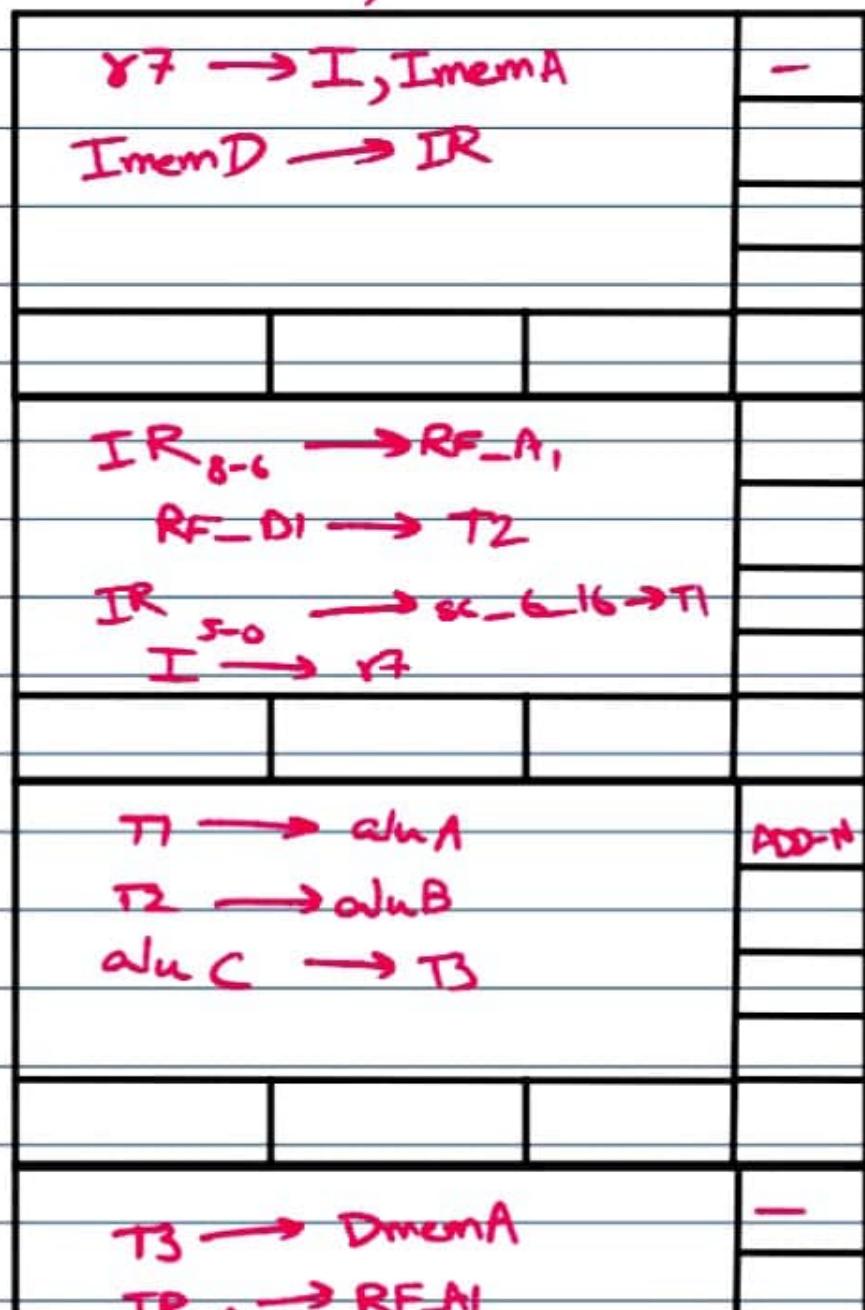


10) SW :

01-0	RA	RB	6 Immediate
15	1211	98	65

 (I)

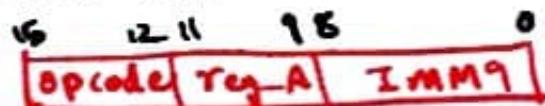
Store value in ra @ (rb+imm) SW ra, rb, Imm



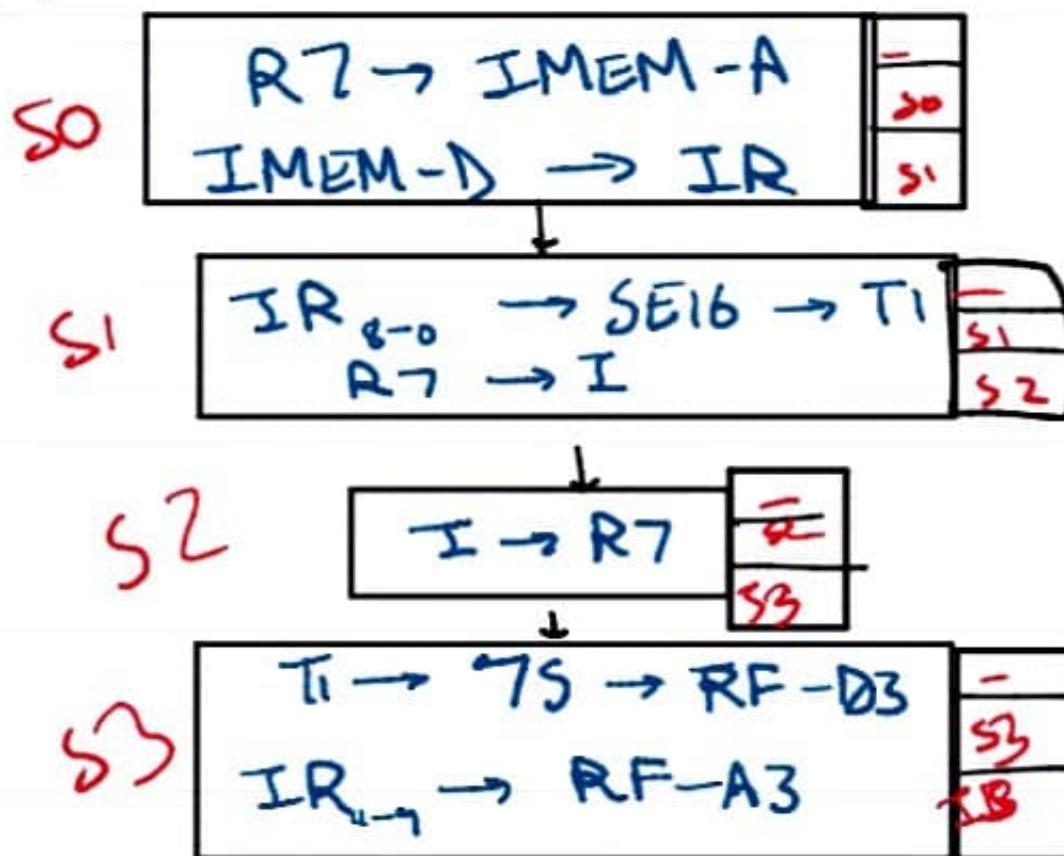
11)

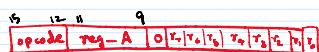
LHI

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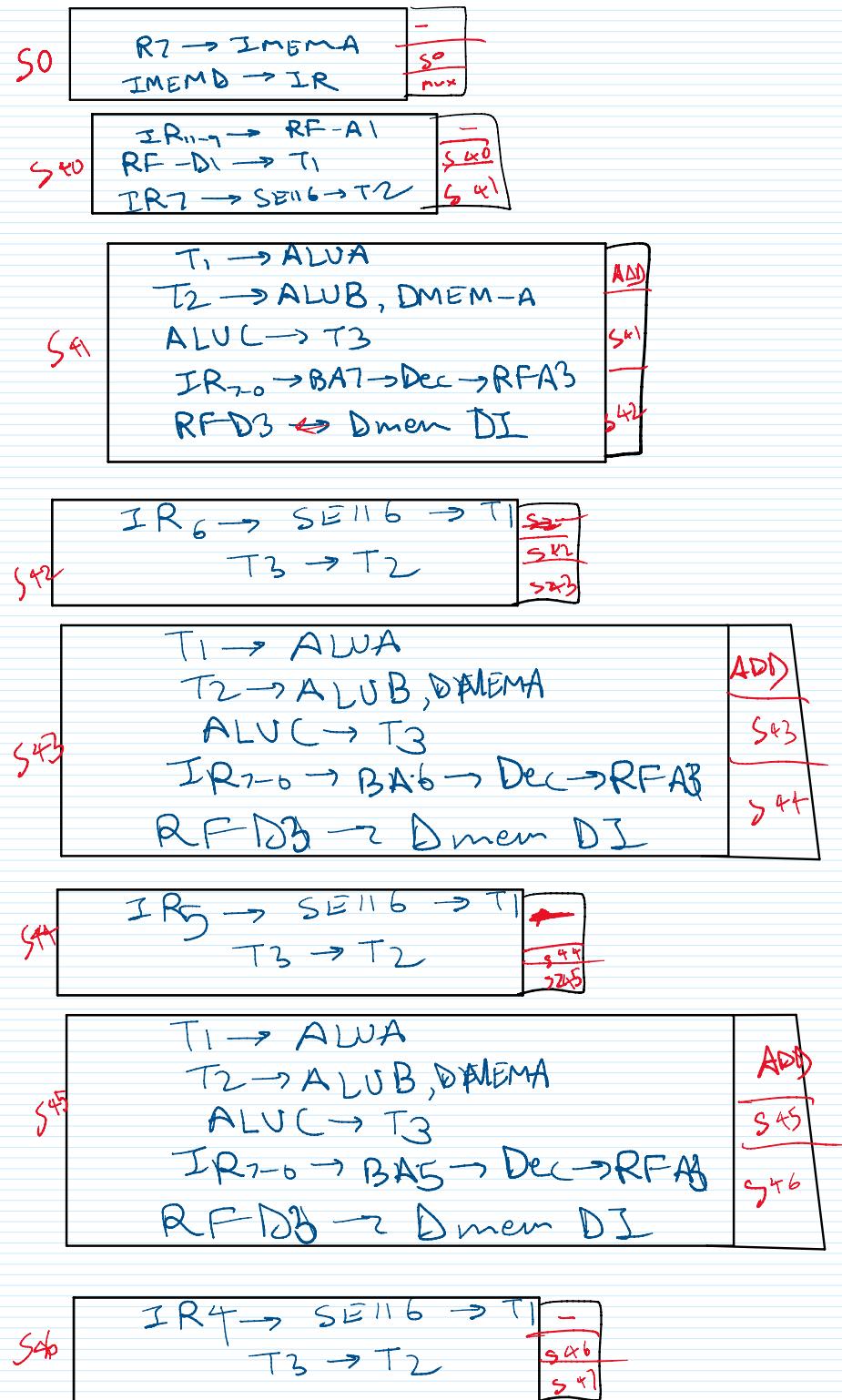
LHI reg-A Imm9.

for IMM9 = b₈b₇b₆b₅b₄b₃b₂b₁b₀then reg-A becomes b₈b₇b₆b₅b₄b₃b₂b₁b₀ 00000000



L M reg-A 0 r₇ r₆ r₅ r₄ r₃ r₂ r₁ r₀

L loads registers in addresses (consecutive) starting from "reg-A", if their corresponding bit is set high.



S47

$T_1 \rightarrow ALWA$	
$T_2 \rightarrow ALUB, D\cancel{MEMA}$	ADD
$ALVC \rightarrow T_3$	
$IR_{7-0} \rightarrow BA_7 \rightarrow Dec \rightarrow RFAB$	
$RF-D3 \rightarrow D_{mem} DJ$	

~~ADD~~

~~S47~~

~~S48~~

S48

$IR_3 \rightarrow SE116 \rightarrow T_1$	-
$T_3 \rightarrow T_2$	S48
	S49

S49

$T_1 \rightarrow ALWA$	
$T_2 \rightarrow ALUB, D\cancel{MEMA}$	ADD
$ALVC \rightarrow T_3$	
$IR_{7-0} \rightarrow BA_3 \rightarrow Dec \rightarrow RFAB$	
$RF-D3 \rightarrow D_{mem} DJ$	

~~ADD~~

~~S49~~

~~S50~~

S50

$IR_2 \rightarrow SE116 \rightarrow T_1$	-
$T_3 \rightarrow T_2$	S50
	S51

S51

$T_1 \rightarrow ALWA$	
$T_2 \rightarrow ALUB, D\cancel{MEMA}$	ADD
$ALVC \rightarrow T_3$	
$IR_{7-0} \rightarrow BA_2 \rightarrow Dec \rightarrow RFAB$	
$RF-D3 \rightarrow D_{mem} DJ$	

~~ADD~~

~~S51~~

~~S52~~

S52

$IR_1 \rightarrow SE116 \rightarrow T_1$	-
$T_3 \rightarrow T_2$	S52
	S53

S53

$T_1 \rightarrow ALWA$	
$T_2 \rightarrow ALUB, D\cancel{MEMA}$	ADD
$ALVC \rightarrow T_3$	
$IR_{7-0} \rightarrow BA_1 \rightarrow Dec \rightarrow RFAB$	
$RF-D3 \rightarrow D_{mem} DJ$	

~~ADD~~

~~S53~~

~~S54~~

S54

$IR_0 \rightarrow SE116 \rightarrow T_1$	-
$T_3 \rightarrow T_2$	S54
	S55

S55

$T_1 \rightarrow ALWA$	
$T_2 \rightarrow ALUB, D\cancel{MEMA}$	ADD
$ALVC \rightarrow T_3$	
$IR_{7-0} \rightarrow BA_0 \rightarrow Dec \rightarrow RFAB$	
$RF-D3 \rightarrow D_{mem} DJ$	

~~ADD~~

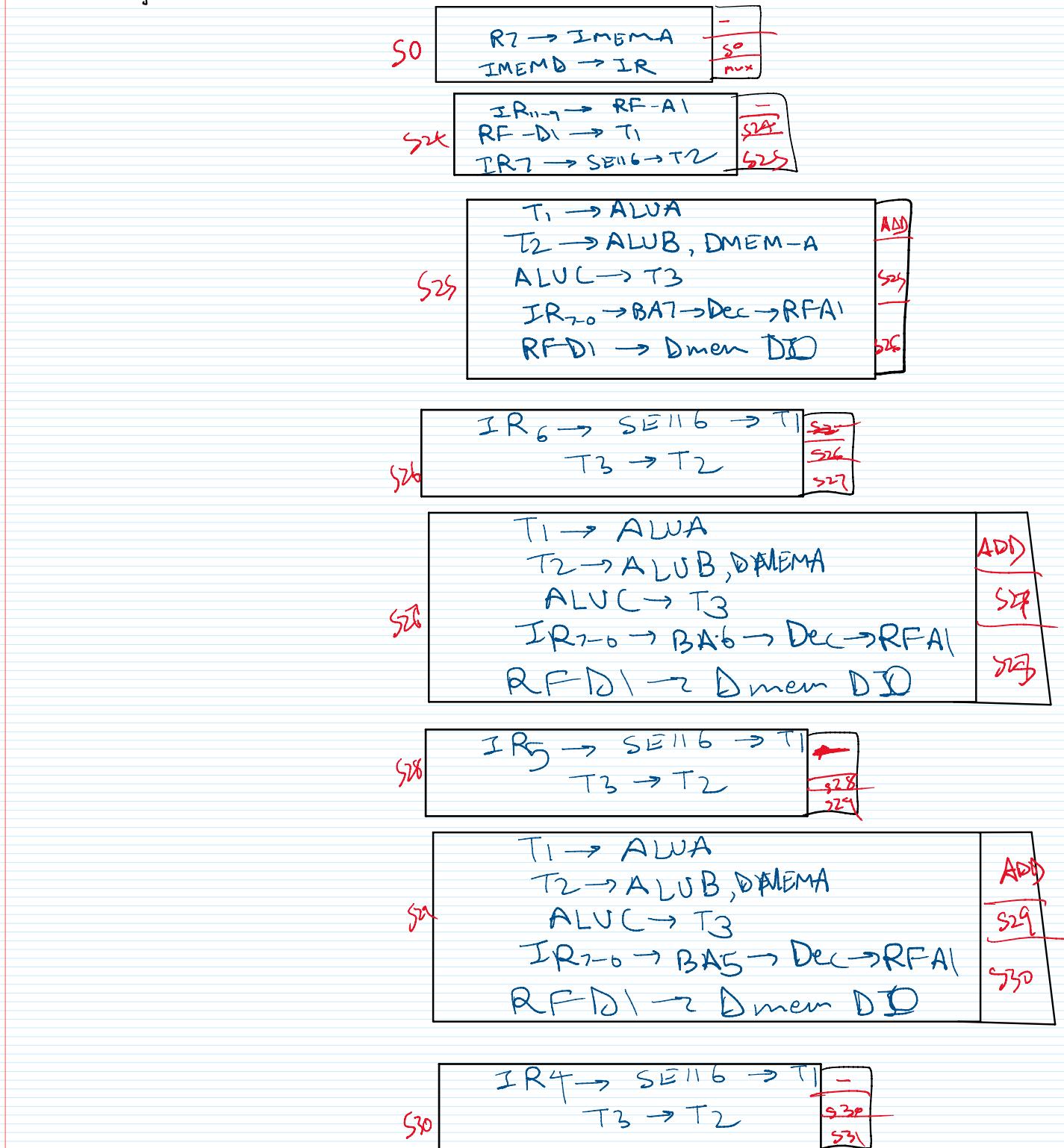
~~S55~~

~~I8~~



SM reg-A 0 R₇-R₀

Stores registers in addresses (consecutive) starting from "reg-A", if their corresponding bit is set high.



$T_1 \rightarrow ALWA$
 $T_2 \rightarrow ALUB, D\cancel{MEMA}$
 $ALVC \rightarrow T_3$
 $IR_{7-0} \rightarrow BA_7 \rightarrow Dec \rightarrow RFAI$
 $RFDI \rightarrow D_{mem} DD$

ADD

S31

S32

$IR_3 \rightarrow SE116 \rightarrow T_1$
 $T_3 \rightarrow T_2$

ADD

S33

S34

$T_1 \rightarrow ALWA$
 $T_2 \rightarrow ALUB, D\cancel{MEMA}$
 $ALVC \rightarrow T_3$
 $IR_{7-0} \rightarrow BA_3 \rightarrow Dec \rightarrow RFAI$
 $RFDI \rightarrow D_{mem} DD$

$IR_2 \rightarrow SE116 \rightarrow T_1$
 $T_3 \rightarrow T_2$

ADD

S35

S36

$T_1 \rightarrow ALWA$
 $T_2 \rightarrow ALUB, D\cancel{MEMA}$
 $ALVC \rightarrow T_3$
 $IR_{7-0} \rightarrow BA_2 \rightarrow Dec \rightarrow RFAI$
 $RFDI \rightarrow D_{mem} DD$

$IR_1 \rightarrow SE116 \rightarrow T_1$
 $T_3 \rightarrow T_2$

ADD

S37

S38

$T_1 \rightarrow ALWA$
 $T_2 \rightarrow ALUB, D\cancel{MEMA}$
 $ALVC \rightarrow T_3$
 $IR_{7-0} \rightarrow BA_1 \rightarrow Dec \rightarrow RFAI$
 $RFDI \rightarrow D_{mem} DD$

$IR_0 \rightarrow SE116 \rightarrow T_1$
 $T_3 \rightarrow T_2$

ADD

S39

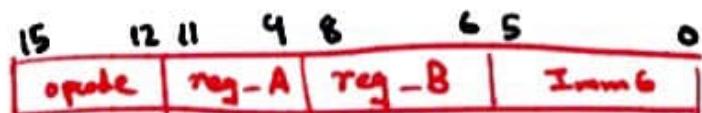
S38

$T_1 \rightarrow ALWA$
 $T_2 \rightarrow ALUB, D\cancel{MEMA}$
 $ALVC \rightarrow T_3$
 $IR_{7-0} \rightarrow BA_0 \rightarrow Dec \rightarrow RFAI$
 $RFDI \leftarrow D_{mem} DD$

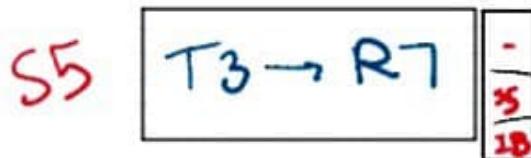
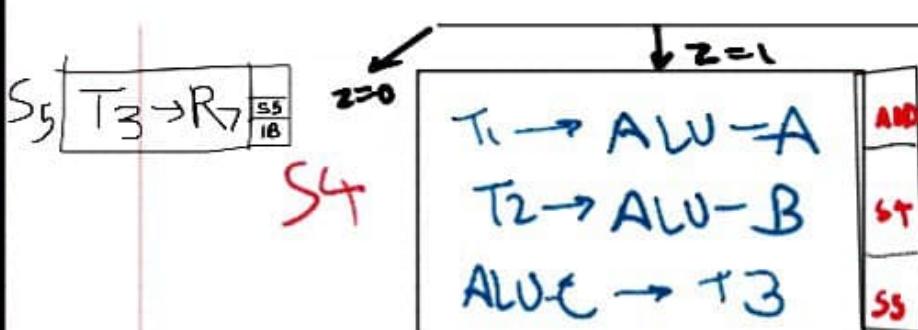
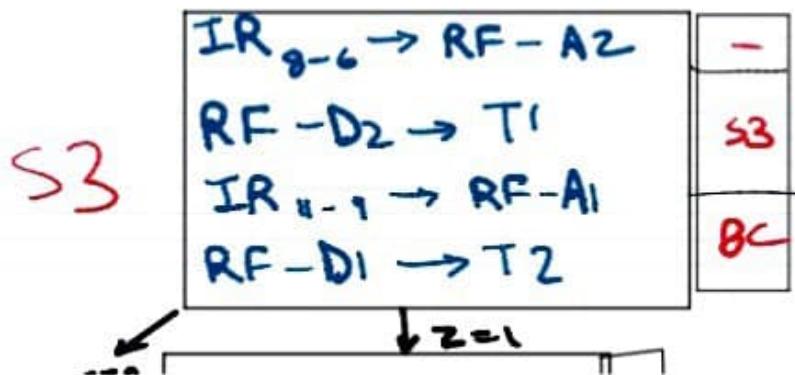
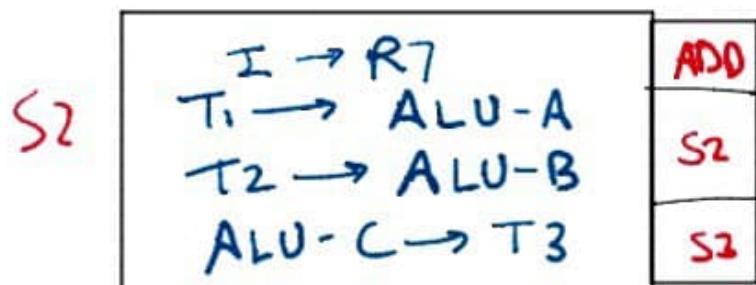
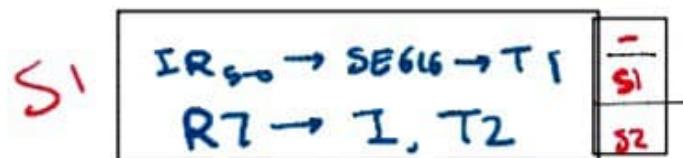
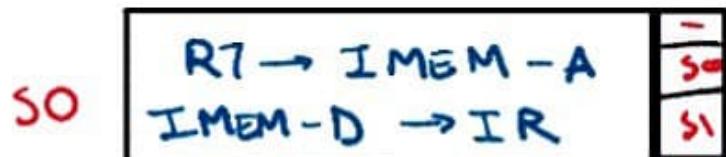
14)

BEQ

Sunday, April 10, 2022 11:49 AM



BEQ RA RB IMM6

if RA = RB, PC \rightarrow PC + IMM6

15)

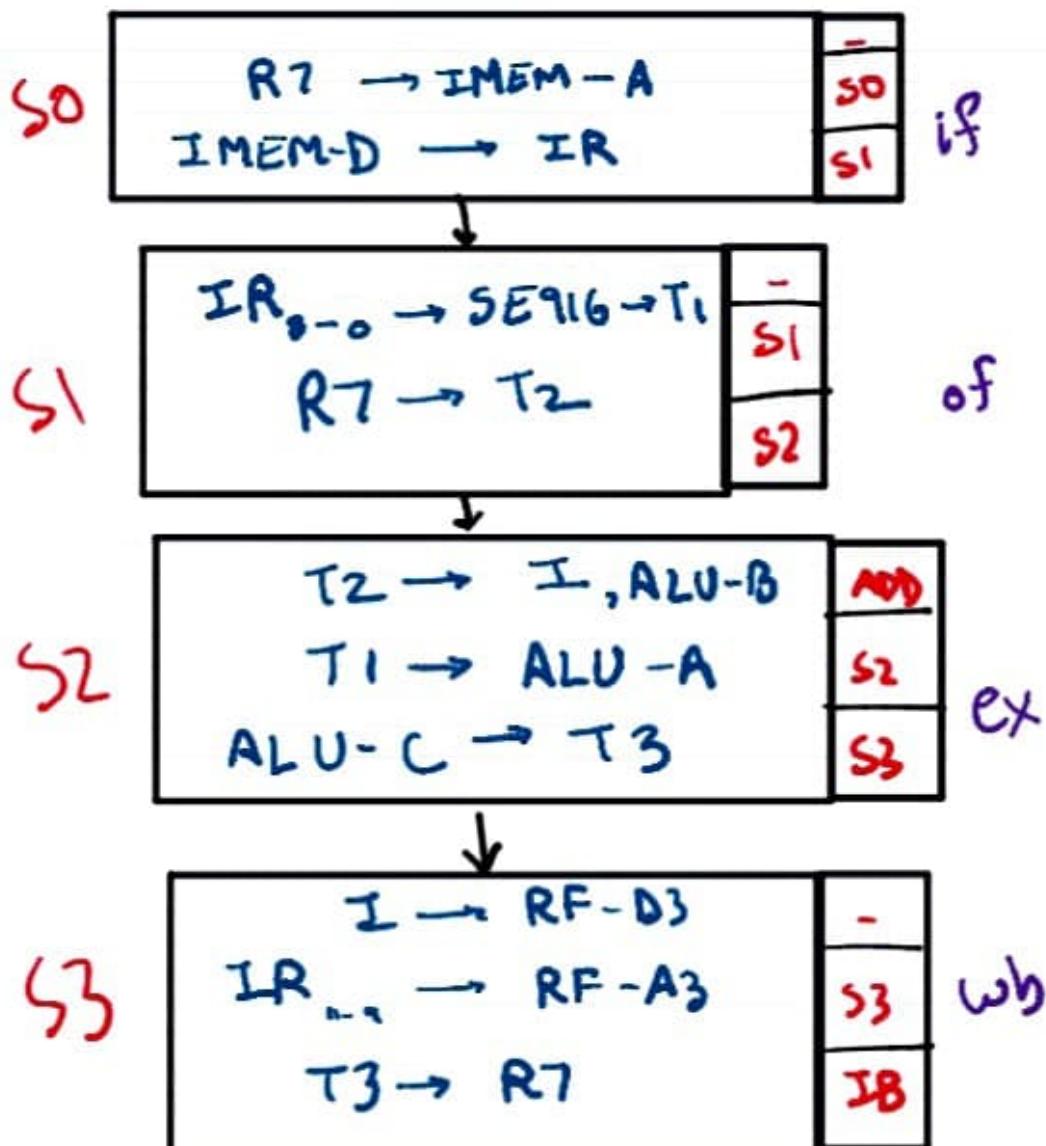
JAL

Sunday, April 10, 2022 11:18 AM



JAL RA Imm9

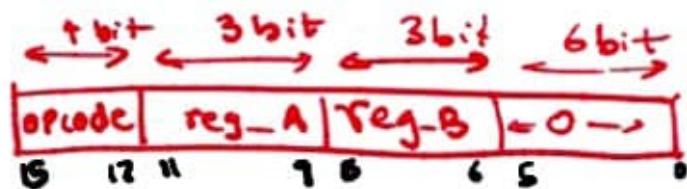
Branch to Imm9+PC & store PC+1 in reg-A.



16)

JLR

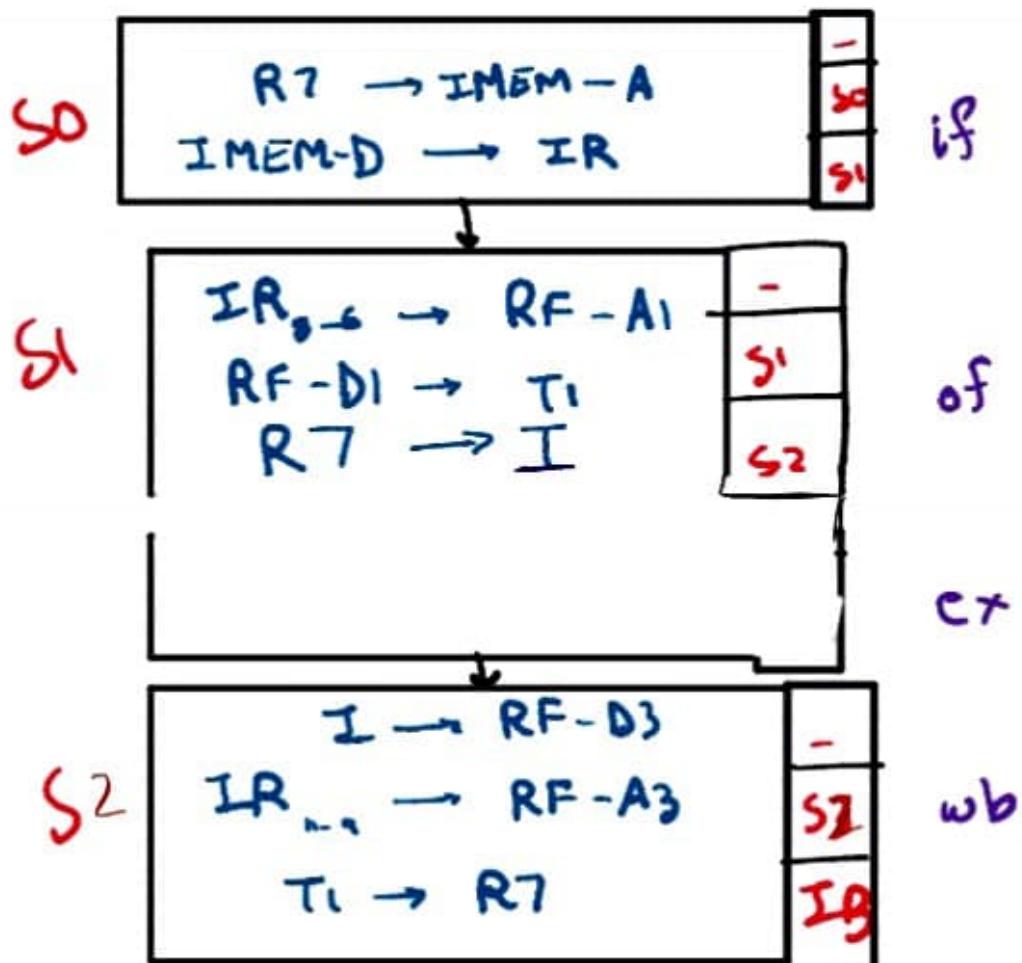
Friday, April 8, 2022 6:35 PM



(J)

JLR RA RB

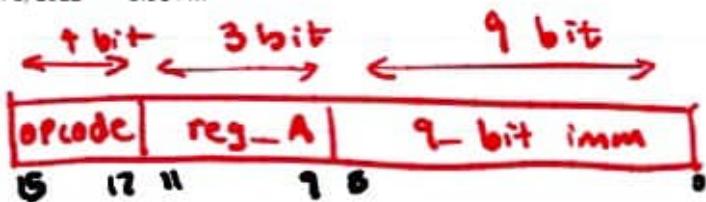
→ Branches to RB, stores PC+1 in RA



17)

JRI

Friday, April 8, 2022 5:51 PM



(J)

JRI RA

⇒ Branches to memory location pointed by
RA + Imm16

