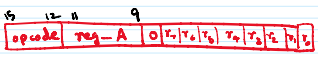
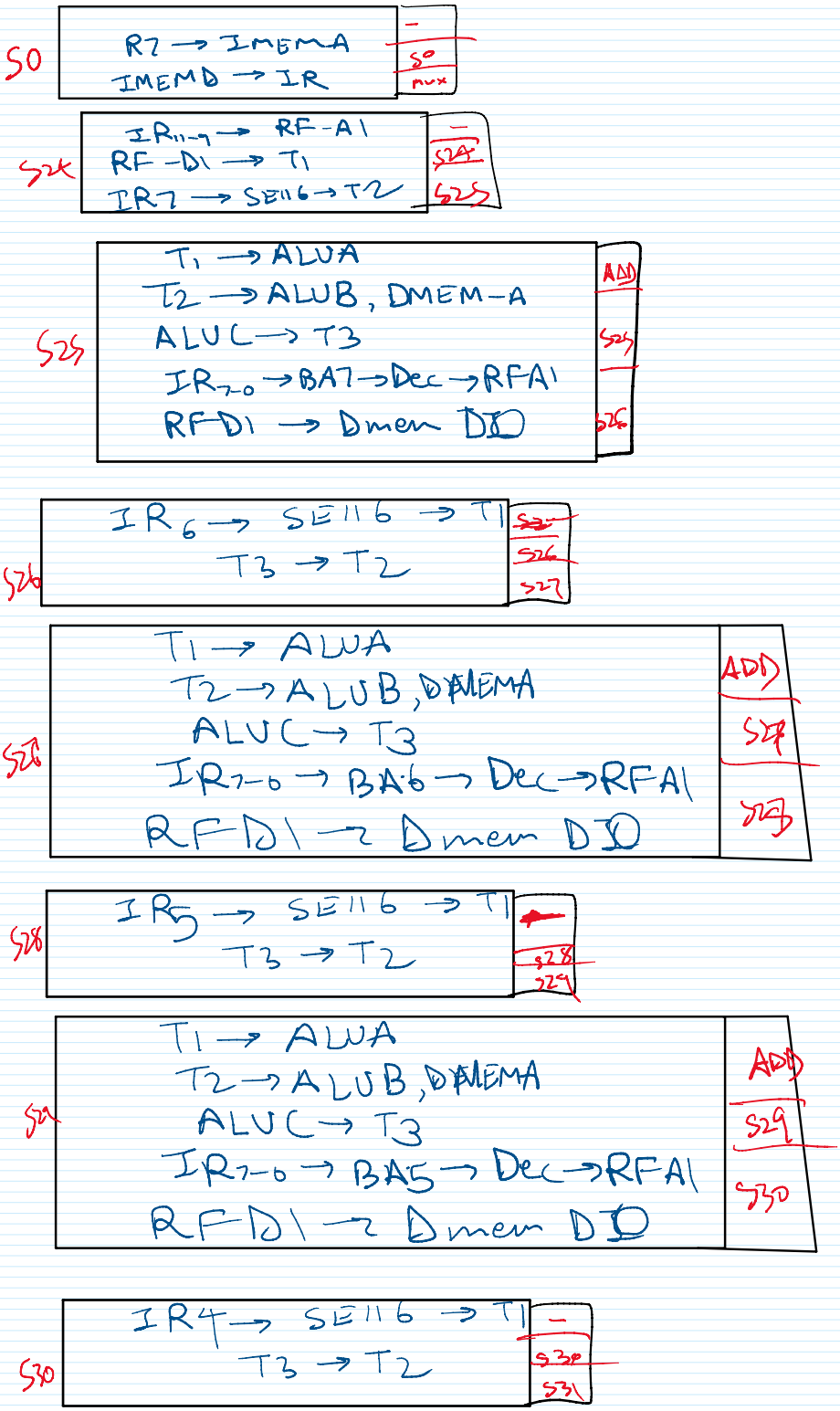
SM_updated

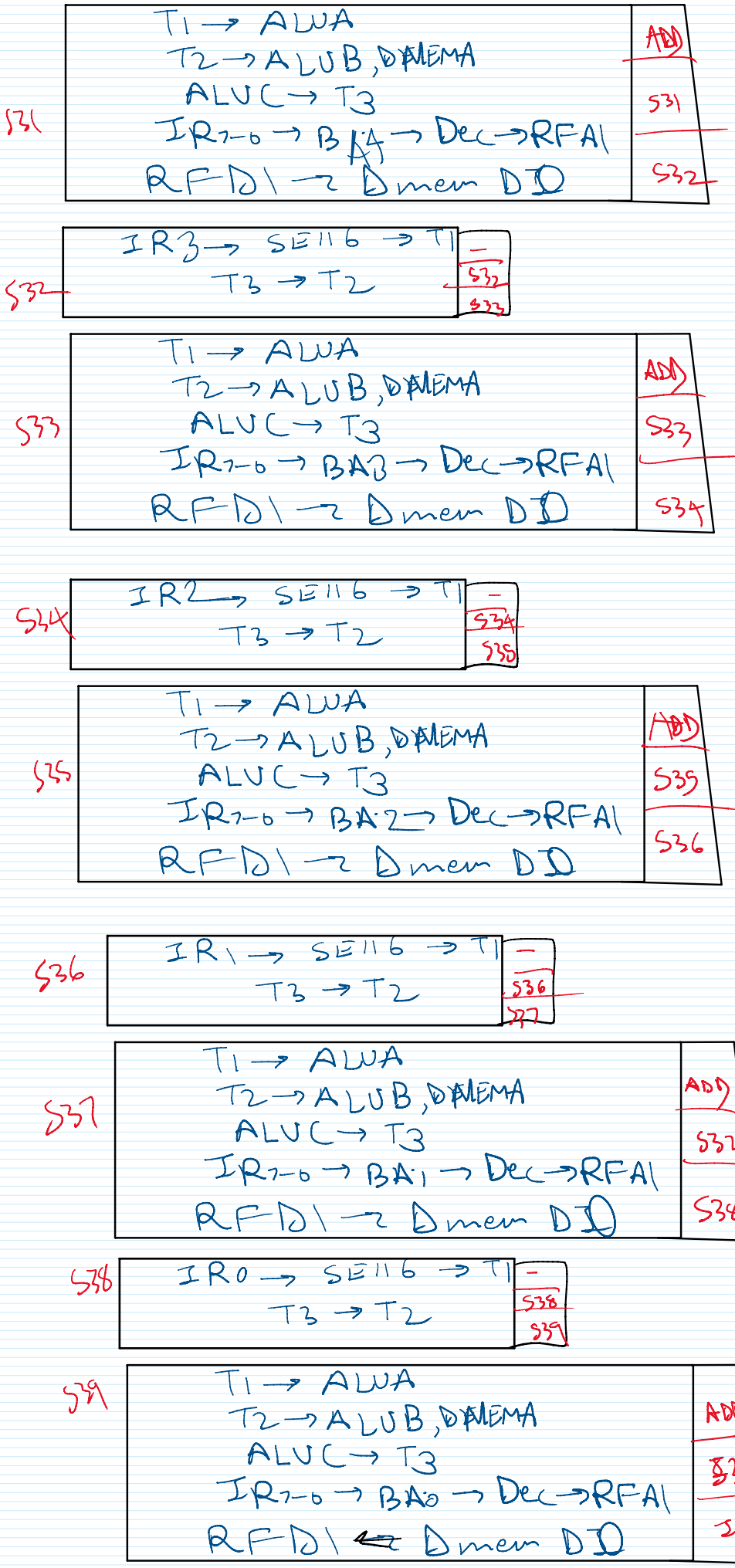
Sunday, April 17, 2022 3:11 PM



SM reg_A 0 r7 r6 r5 r4 r3 r2 r1 r0

Stores registers in addresses (consecutive) starting from "reg_A", if their corresponding bit is set high.




S31
T1 → ALUA
T2 → ALUB, DMEMA
ALUC → T3
IR7-0 → BA4 → Dec → RFA1
RFD1 → Dmem DI
ADD
S31
S32
S32
IR3 → SE16 → T1
T3 → T2
–
S32
S33
S33
T1 → ALUA
T2 → ALUB, DMEMA
ALUC → T3
IR7-0 → BA3 → Dec → RFA1
RFD1 → Dmem DI
ADD
S33
S34
S34
IR2 → SE16 → T1
T3 → T2
–
S34
S35
S35
T1 → ALUA
T2 → ALUB, DMEMA
ALUC → T3
IR7-0 → BA2 → Dec → RFA1
RFD1 → Dmem DI
ADD
S35
S36
S36
IR1 → SE16 → T1
T3 → T2
–
S36
S37
S37
T1 → ALUA
T2 → ALUB, DMEMA
ALUC → T3
IR7-0 → BA1 → Dec → RFA1
RFD1 → Dmem DI
ADD
S37
S38
S38
IR0 → SE16 → T1
T3 → T2
–
S38
S39
S39
T1 → ALUA
T2 → ALUB, DMEMA
ALUC → T3
IR7-0 → BA0 → Dec → RFA1
RFD1 ← Dmem DI
ADD
S39
JB