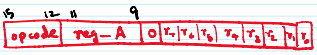
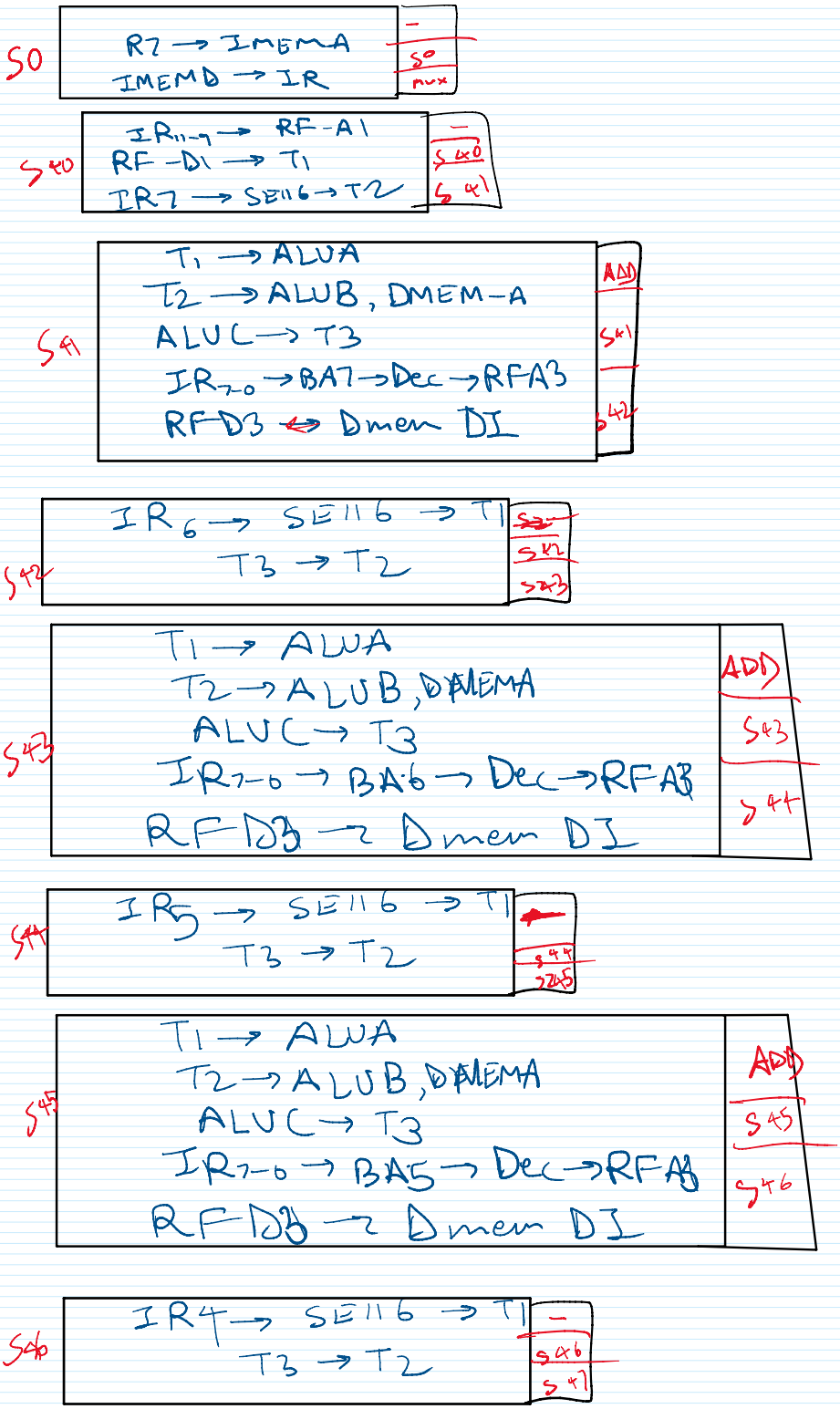
LM_updated

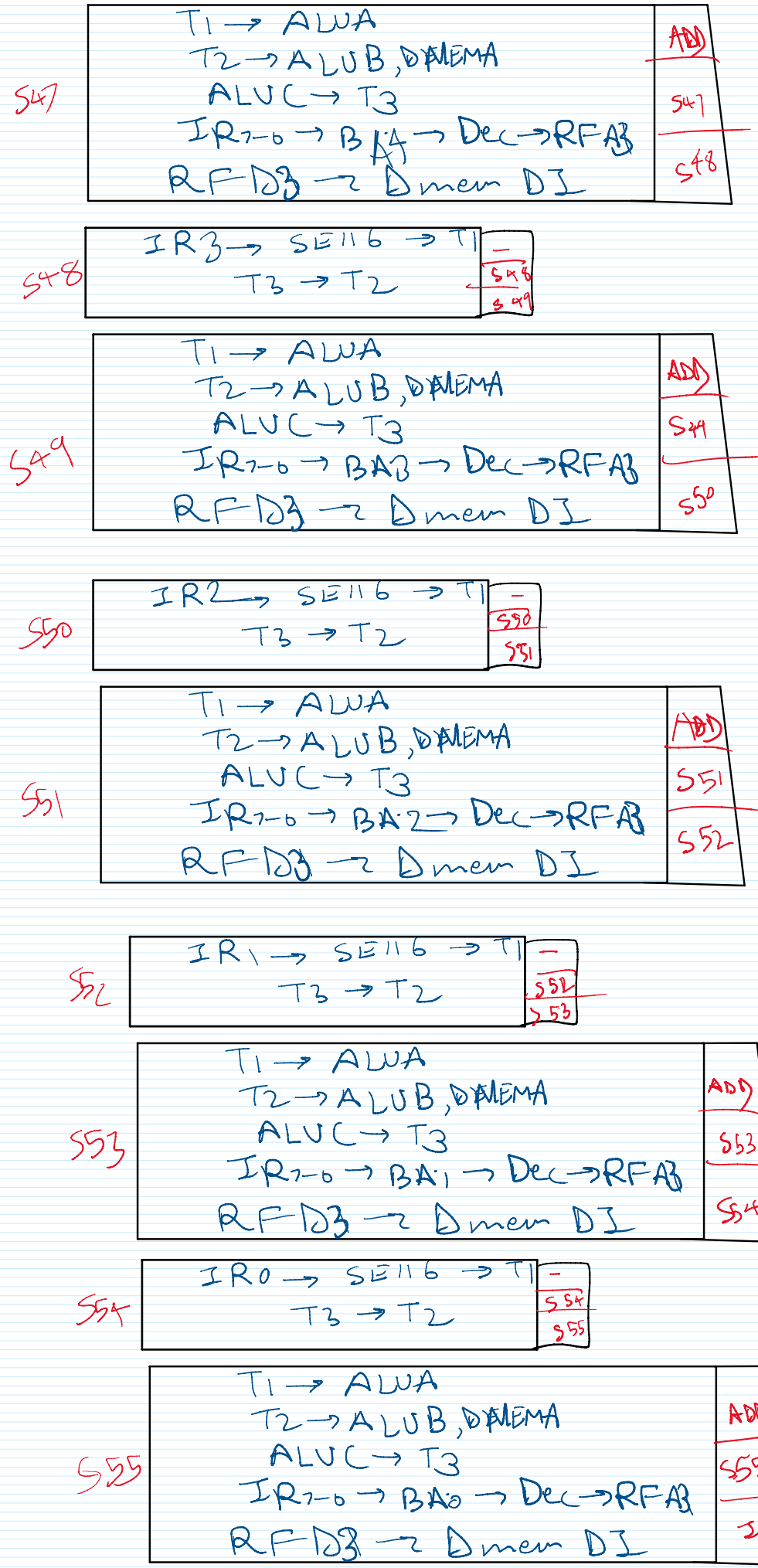
Sunday, April 17, 2022 3:11 PM



LM reg_A R7 R6 R5 R4 R3 R2 R1 R0

Loads registers in addresses (consecutive) starting from "reg_A", if their corresponding bit is set high.




S47
T1 → ALUA
T2 → ALUB, DAMEMA
ALUC → T3
IR7-0 → BA4 → Dec → RFAB
RFDB → Dmem DI
ADD
S47
S48
S48
IR3 → SE116 → T1
T3 → T2
–
S48
S49
S49
T1 → ALUA
T2 → ALUB, DAMEMA
ALUC → T3
IR7-0 → BA3 → Dec → RFAB
RFDB → Dmem DI
ADD
S49
S50
S50
IR2 → SE116 → T1
T3 → T2
–
S50
S51
S51
T1 → ALUA
T2 → ALUB, DAMEMA
ALUC → T3
IR7-0 → BA2 → Dec → RFAB
RFDB → Dmem DI
ADD
S51
S52
S52
IR1 → SE116 → T1
T3 → T2
–
S52
S53
S53
T1 → ALUA
T2 → ALUB, DAMEMA
ALUC → T3
IR7-0 → BA1 → Dec → RFAB
RFDB → Dmem DI
ADD
S53
S54
S54
IR0 → SE116 → T1
T3 → T2
–
S54
S55
S55
T1 → ALUA
T2 → ALUB, DAMEMA
ALUC → T3
IR7-0 → BA0 → Dec → RFAB
RFDB → Dmem DI
ADD
S55
JB