



LM reg-A 0 r₇ r₆ r₅ r₄ r₃ r₂ r₁ r₀

L loads registers in addresses (consecutive) starting from "reg-A", if their corresponding bit is set high

S0

R7 → IMEMA	-
IMEMB → IR	S0 mux

S40

IR ₁₁₋₉ → RF-A1	-
RF-D1 → T1	S40
IR7 → SE116 → T2	S41

S41

T1 → ALUA	ADD
T2 → ALUB, DMEM-A	S41
ALUC → T3	S42
IR ₂₋₀ → BA7 → Dec → RFA3	
RF-D3 → DMEM DI	

S42

IR ₆ → SE116 → T1	S42
T3 → T2	S43

S43

T1 → ALUA	ADD
T2 → ALUB, DMEMA	S43
ALUC → T3	S44
IR ₇₋₀ → BA6 → Dec → RFA3	
RF-D3 → DMEM DI	

S44

IR ₅ → SE116 → T1	S44
T3 → T2	S45

S45

T1 → ALUA	ADD
T2 → ALUB, DMEMA	S45
ALUC → T3	S46
IR ₇₋₀ → BA5 → Dec → RFA3	
RF-D3 → DMEM DI	

S46

IR ₄ → SE116 → T1	-
T3 → T2	S46 S47

S47	T1 → ALWA	ADD
	T2 → ALUB, DLEMA	
	ALUC → T3	S47
	IR70 → BA4 → Dec → RFAB	
	RFDB → Dmem DI	S48

S48	IR3 → SE116 → T1	-
	T3 → T2	S48 S49

S49	T1 → ALWA	ADD
	T2 → ALUB, DLEMA	
	ALUC → T3	S49
	IR70 → BAB → Dec → RFAB	
	RFDB → Dmem DI	S50

S50	IR2 → SE116 → T1	-
	T3 → T2	S50 S51

S51	T1 → ALWA	ADD
	T2 → ALUB, DLEMA	
	ALUC → T3	S51
	IR70 → BA2 → Dec → RFAB	
	RFDB → Dmem DI	S52

S52	IR1 → SE116 → T1	-
	T3 → T2	S52 S53

S53	T1 → ALWA	ADD
	T2 → ALUB, DLEMA	
	ALUC → T3	S53
	IR70 → BA1 → Dec → RFAB	
	RFDB → Dmem DI	S54

S54	IR0 → SE116 → T1	-
	T3 → T2	S54 S55

S55	T1 → ALWA	ADD
	T2 → ALUB, DLEMA	
	ALUC → T3	S55
	IR70 → BA0 → Dec → RFAB	
	RFDB → Dmem DI	S56