become the new values of present state. For other types of flip-flops, such as JK, T and the relationship between the next-state variable and inputs to a flip-flop is not as straightforward as D flip-flop. For other types of flip-flops we have to refer excitation table of flip-flop to find flip-flop iputs. This is illustrated in the following example.

Example 8.1 : *A sequential circuit has one input and one output. The state diagram is shown in Fig. 8.8. Design the sequential circuit with a) D-flip-flops b) T flip-flops c) RS flip-flops, and d) JK- flip-flops.*

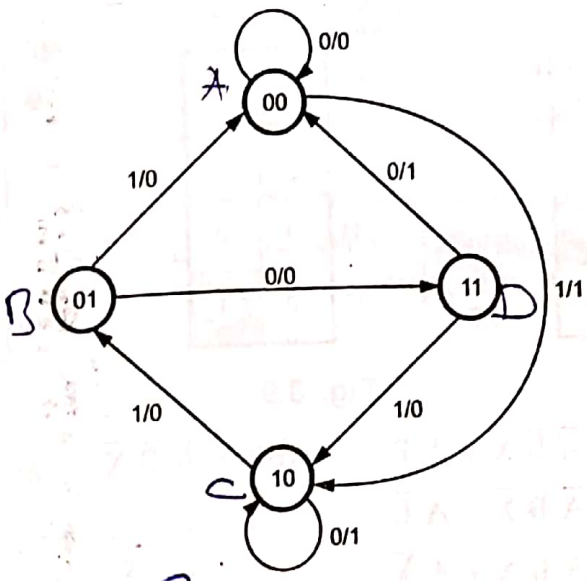

Fig. 8.8

Solution : The state table for the state diagram shown in Fig. 8.8 is as given in Table 8.5.

Present state		Next state		Output	
		X = 0	X = 1	X = 0	X = 1
A	B	AB	AB	Y	Y
0	0	0 0	1 0	0	1
0	1	1 1	0 0	0	0
1	0	1 0	0 1	1	0
1	1	0 0	1 0	1	0

Table 8.5

As seen from the state table there are no equivalent states. Therefore, no reduction is the state diagram. The state table shows that circuit goes through four states, therefore we require 2 flip-flops (number of states = 2^m, where m = number of flip-flops). Since two flip-flops are required first is denoted as A and second is denoted as B.

i) Design using D Flip-Flops

As mentioned earlier, for D flip-flops next states are nothing but the next states. Thus, we can directly use next states to determine the flip-flop input with the help of K-map simplification.

K-map Simplification

For flip - flop A

AB \ X	0	1
00	0	(1)
01	(1)	0
11	0	(1)
10	(1)	0

For flip - flop B

AB \ X	0	1
00	0	0
01	(1)	0
11	0	0
10	0	(1)

For output

AB \ X	0	1
00	0	1
01	0	0
11	(1)	0
10	(1)	0

Fig. 8.9

$$D_A = \overline{A}\,\overline{B}\,X + \overline{A}\,B\,\overline{X} + ABX + A\,\overline{B}\,\overline{X} \quad \text{and}$$

$$D_B = \overline{A}\,B\,\overline{X} + A\,\overline{B}\,X$$

$$Y = \overline{A}\,\overline{B}\,X + A\,\overline{X}$$

With these flip-flop input functions and circuit output function we can draw the diagram as follows

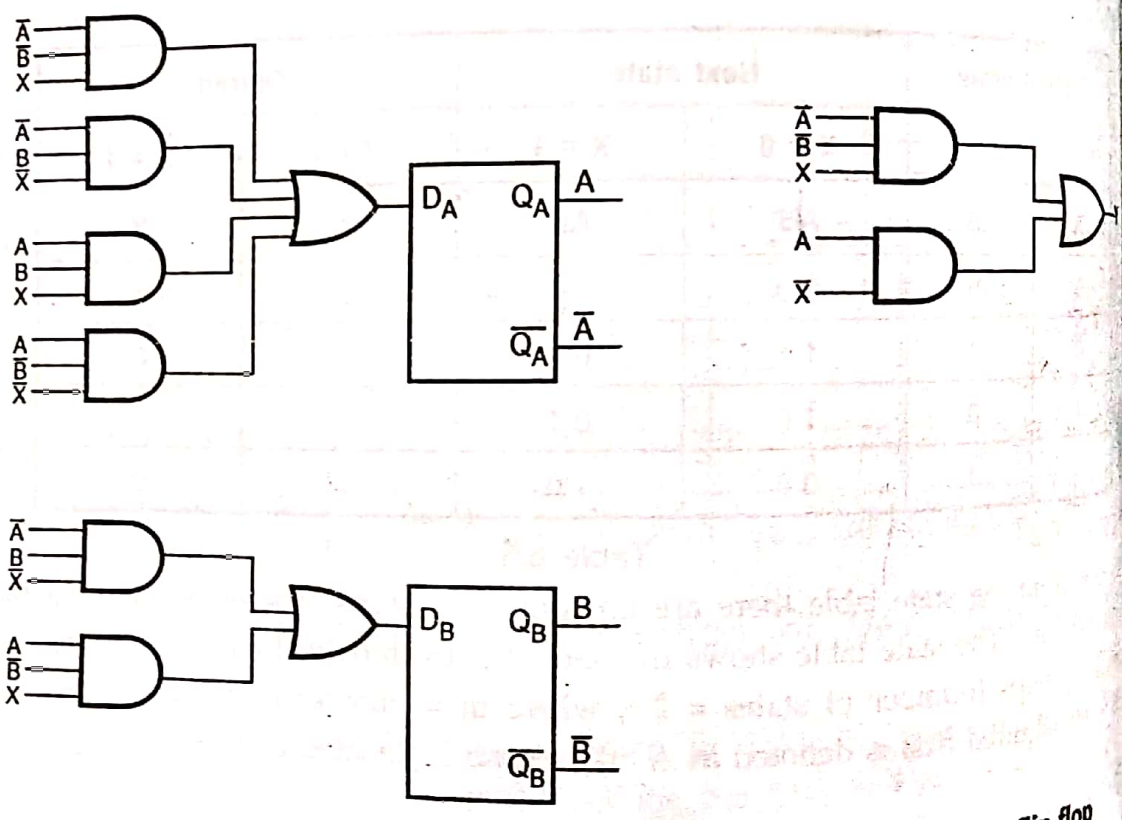

Fig. 8.10 Logic diagram of given sequential circuit using D flip-flop

Design using T flip-flops

Using the excitation table for T flip-flop shown in Table 8.6 we can determine the citation table for the given circuit as shown in Table 8.7.

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Table 8.6 Excitation table for T flip-flop

Present state		Input	Next state		Flip-flop inputs		Output
A	B	X	A	B	T_A	T_B	Y
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	1
0	1	0	1	1	1	0	0
0	1	1	0	0	0	1	0
1	0	0	1	0	0	0	1
1	0	1	0	1	1	1	0
1	1	0	0	0	1	1	1
1	1	1	1	0	0	1	0

Table 8.7 Circuit excitation table

The first row of circuit excitation table shows that there is no change in the state for th flip-flops. The transition from $0 \Rightarrow 0$ for T flip-flop requires input T to be at logic 0. he second row shows that flip-flop A has transition $0 \rightarrow 1$. It requires the input T_A to be logic 1. It requires the input T_A to be at logic 1. Similarly, we can find inputs for each p-flop for each row in the table by referring present state, next state and excitation table.

Let us use K-map simplification to determine the flip-flop input functions and circuit tput functions.

K-map simplification

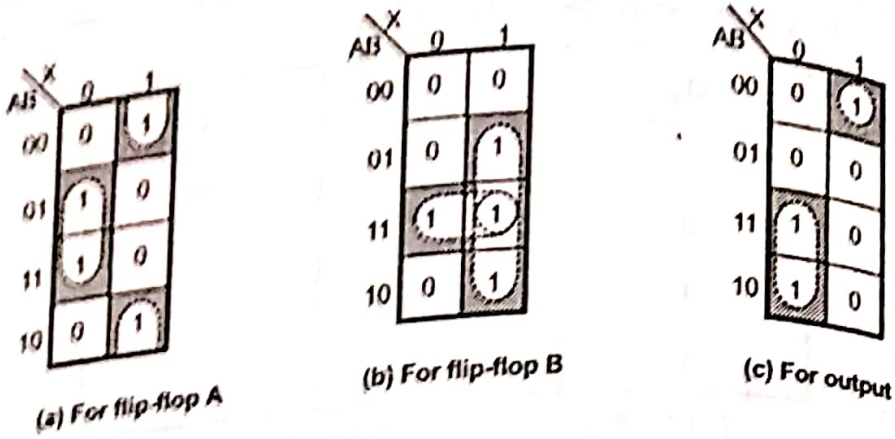

Fig. 8.11

Therefore, input function for $T_A = B\bar{X} + \bar{B}X$,

$T_B = AB + BX + AX$, and

Circuit output function $= A\bar{X} + \bar{A}\bar{B}X$

With these flip-flop input functions and circuit output function we can draw the logic diagram as follows :

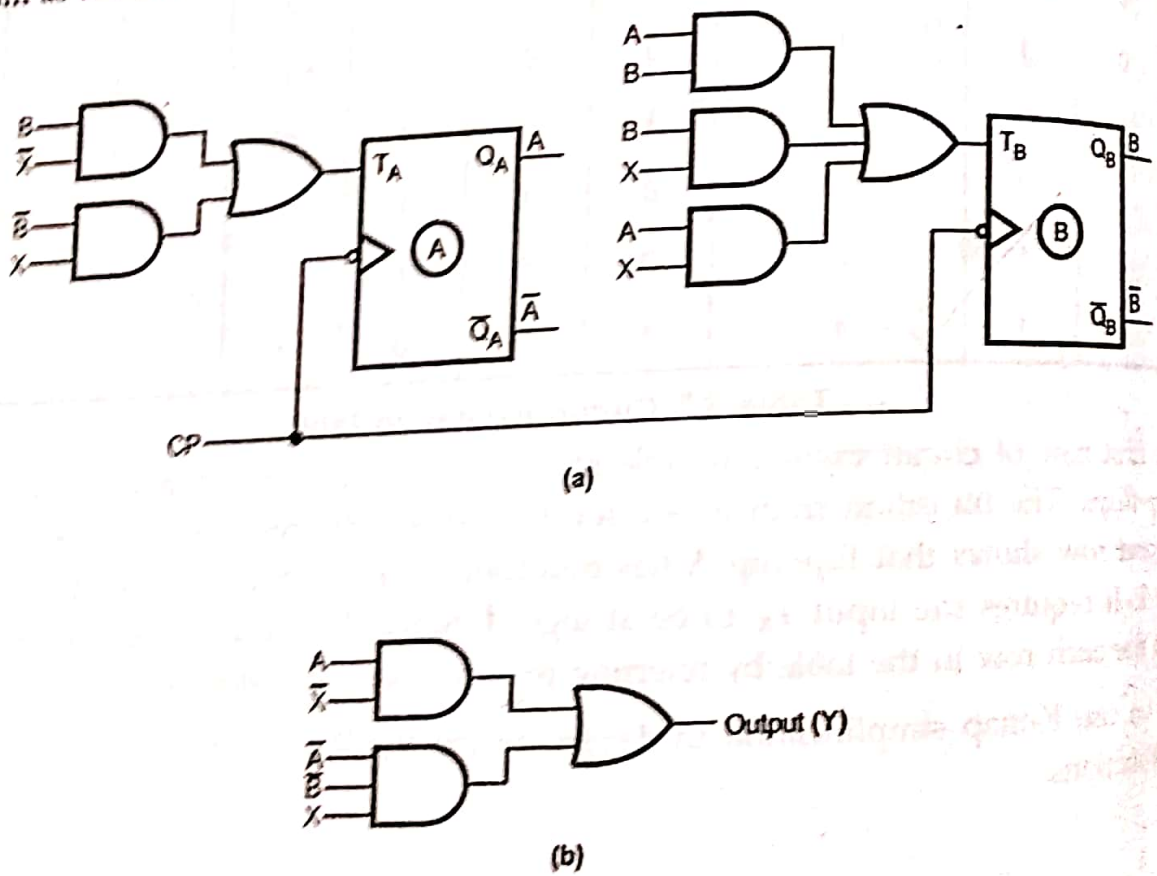

Fig. 8.12 (a) & (b) Logic diagram of given sequential circuit using T flip-flops

Design using RS Flip-Flops

Using the excitation table for RS flip-flop shown in Table 8.8 we can determine the citation table for the given circuit as shown in Table 8.9.

Q_n	Q_{n+1}	R	S
0	0	X	0
0	1	0	1
1	0	1	0
1	1	0	X

Table 8.8 Excitation table for RS flip-flop

Present state		Input	Next state		Flip-flop inputs				Output
A	B	X	A	B	R_A	S_A	R_B	S_B	Y
0	0	0	0	0	X	0	X	0	0
0	0	1	1	0	0	1	X	0	1
0	1	0	1	1	0	1	0	X	0
0	1	1	0	0	X	0	1	0	0
1	0	0	1	0	0	X	X	0	1
1	0	1	0	1	1	0	0	1	0
1	1	0	0	0	1	0	1	0	1
1	1	1	1	0	0	X	1	0	0

Table 8.9

The first row of circuit excitation table shows that there is no change in the state for flip-flops. The transition from $0 \rightarrow 0$ for RS flip-flop requires inputs R and S to be X 0, respectively. Similarly, we can determine inputs for each flip-flop for each row in table by referring present state, next state and excitation table. Let us use K-map plification to determine the flip-flop input functions and circuit output functions.

K-map simplification :

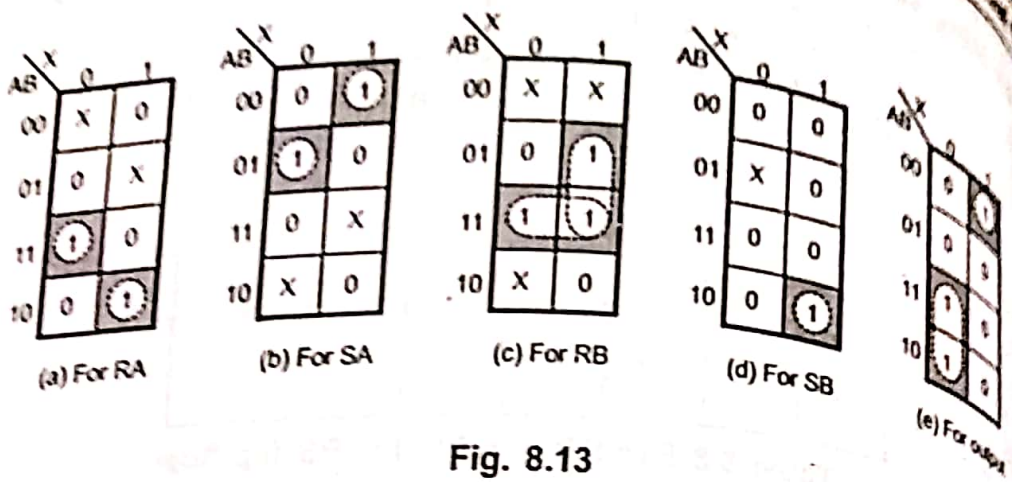

Fig. 8.13

Therefore input function for

$$R_A = AB\overline{X} + A\overline{B}\overline{X}$$

$$S_A = \overline{A}B\overline{X} + \overline{A}\overline{B}X$$

$$R_B = AB + BX$$

$$S_B = A\overline{B}X \text{ and,}$$

$$\text{Circuit output function} = A\overline{X} + \overline{A}\overline{B}X$$

With these flip-flop input functions and circuit output function we can draw the diagram as follows :

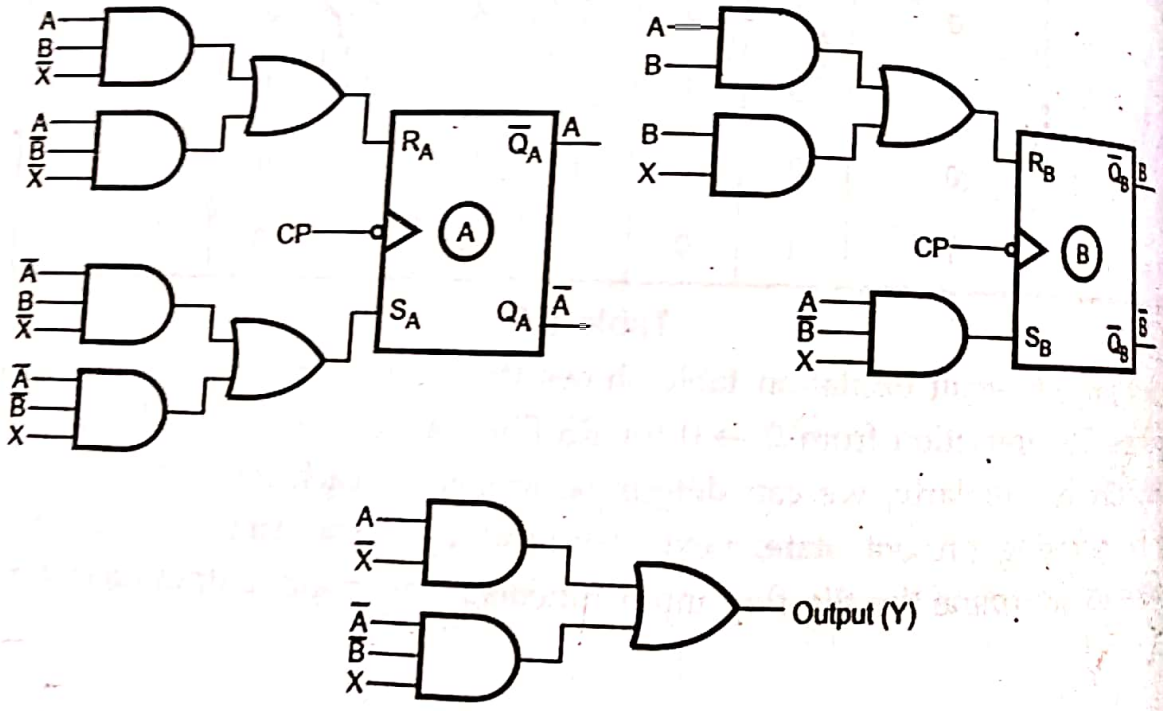

Fig. 8.14 Logic diagram of given sequential circuit using RS flip-flop

Design using JK Flip-Flops

Using the excitation table for JK flop-flop shown in Table 8.10 we can determine the excitation table for the given circuit as shown in Table 8.11.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Table 8.10 Excitation table for JK flip-flop

Present state		Input	Next state		Flip-flop inputs				Output
A	B	X	A	B	J_A	K_A	J_B	K_B	Y
0	0	0	0	0	0	X	0	X	0
0	0	1	1	0	1	X	0	X	1
0	1	0	1	1	1	X	X	0	0
0	1	1	0	0	0	X	X	1	0
1	0	0	1	0	X	0	0	X	1
1	0	1	0	1	X	1	1	X	0
1	1	0	0	0	X	1	X	1	1
1	1	1	1	0	X	0	X	1	0

Table 8.11

The first row of circuit excitation table shows that there is no change in the state for flip-flops. The transition from $0 \rightarrow 0$ for JK filp-flop requires inputs J and K to be 0 X, respectively. Similarly, we can determine inputs for each flip-flop for each row in table by referring present state, next state and excitation table. Let us use K-map plification to determine the flip-flop input functions and circuit output functions.

K-map simplification :

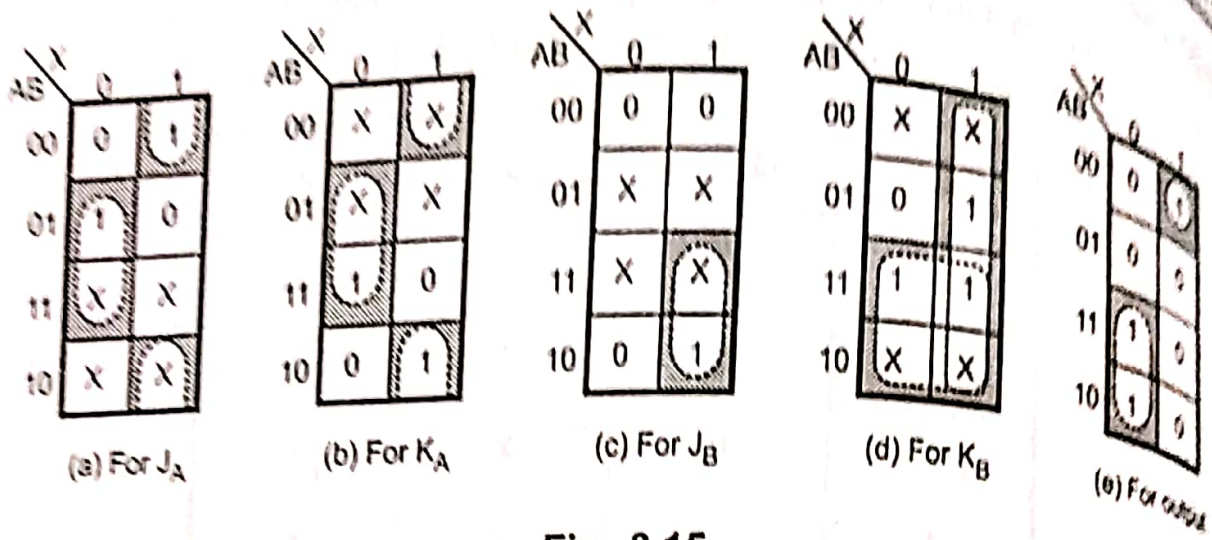

Fig. 8.15

Therefore, input function for

$$J_A = B\overline{X} + \overline{B}X$$

$$K_A = B\overline{X} + \overline{B}X$$

$$J_B = AX$$

$$K_B = A+X$$

Circuit output function $= A\overline{X} + \overline{A}\,\overline{B}X$

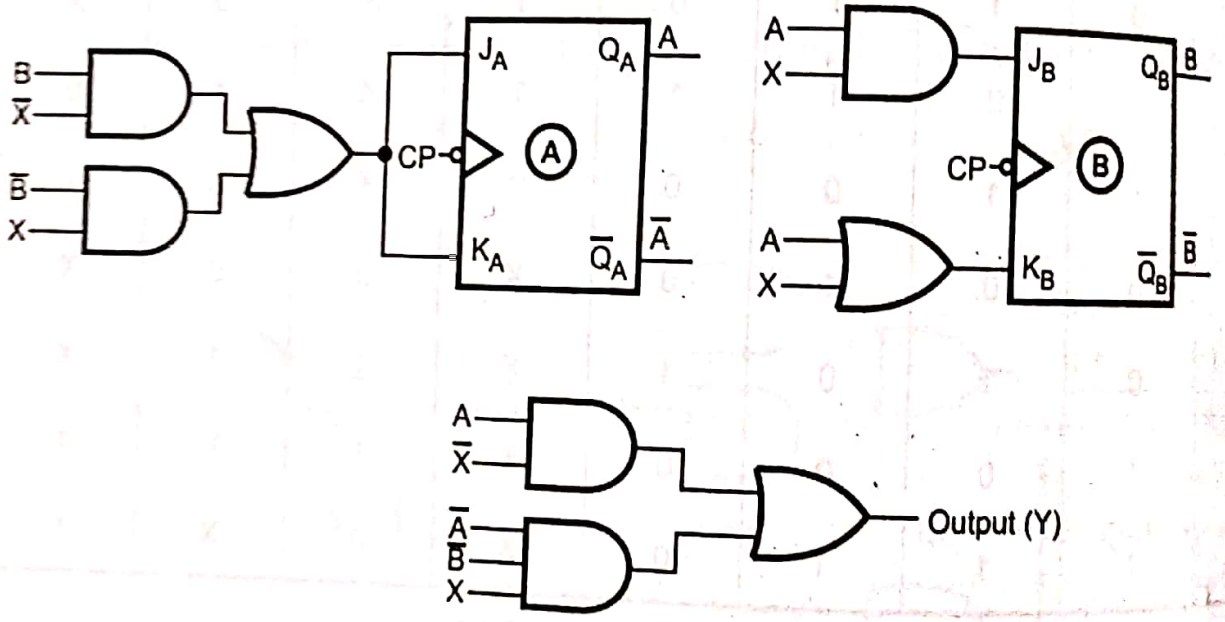

Fig. 8.16 Logic diagram of given sequential circuit using JK flip-flop

8.3 Serial Binary Adder

Serial adder is a circuit in which bits are added a pair at a time. When speed is not great importance, it is a cost-effective option to use serial adder.

Mealy-type FSM for Serial Adder

The Fig. 8.17 shows the

may produce a false output. To eliminate this problem, the external inputs must be allowed to change their state in synchronization with the active edge of clock.

6.40.2 Performance Comparison of Moore and Mealy Models

Table 6.61. Performance Comparison of Moore and Mealy models

S. No.	Moore model	Mealy model
1.	The final output depends only on the present state of memory elements.	The final output depends on the present state of memory elements and the external inputs.
2.	The output changes only after the active clock edge.	Output can change in between the clock edges if the external inputs change.
3.	The implementation of a logic function needs more number of states than Mealy circuit.	Implementation of the same logic function requires less number of states than Moore circuit.

State Diagram of a Moore Circuit

The state diagram of a Moore circuit is slightly modified than the basic state diagram as shown in figure 6.171. The labelling of the directed line now contains only one binary number corresponding to x in which causes the state transition. The output state is now indicated inside the circle. This is because the output Y depends only the present state and independent on input x.

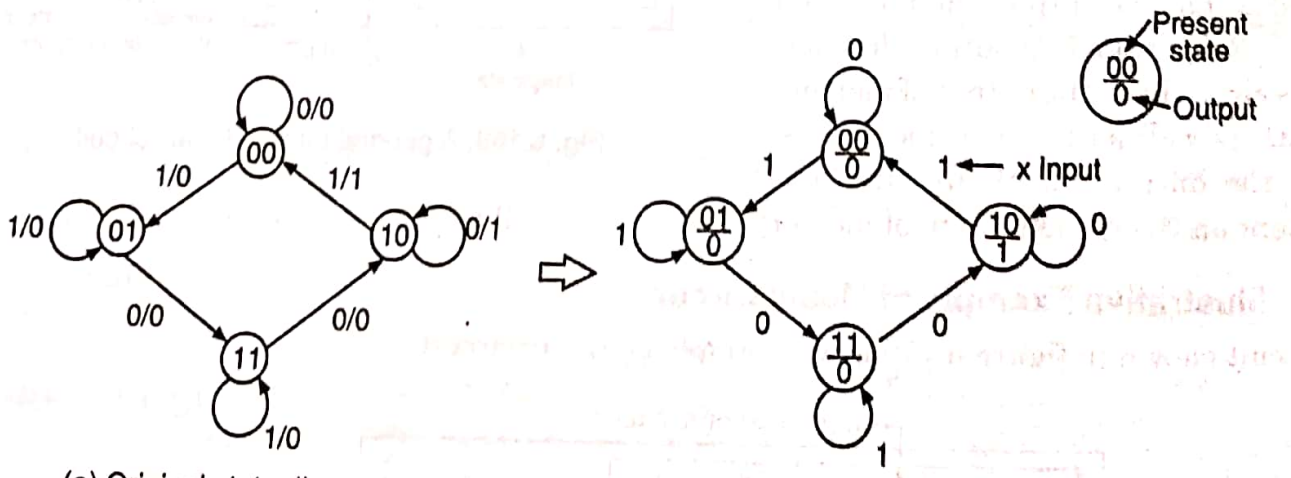

Fig. 6.171.