# unit - 4 Logic Families

Various digital IC are available in the market belongs to various types. These types are known as Logic Families.

Based on the components & devices the digital IC families are named as RTL (Resistor transistor Logic)

TTL (Transistor Transistor Logic)

DTL (Diode Transistor Logic)

CMOS

* characteristic of Logical Families:

1. Voltage & current Parameters -

$V_{IL}$(Max) : low level input voltage

this is the Max. value of input voltage which will be consider as a Logic 0 level.

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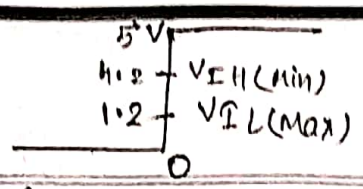



If the input voltage is higher than $V_{IL(max)}$ then it will not be treated as a Low level input.

2. $V_{IH(min)}$ : (Higer level Input voltage) This is the min. value of Input voltage which will be consider as the logic 1 level. If the input voltage is lower than $V_{IH(min)}$ then it will not be consider as the high input.

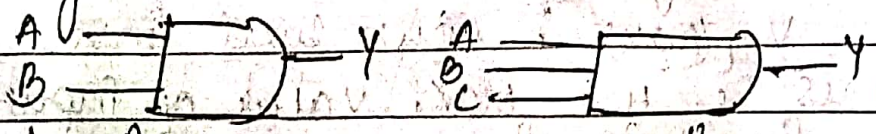
3. $V_{OH(min)}$ : (High Level output voltage) This is the min. value of output voltage which will be considered as the logic high level. If the output voltage is lower then the this level then it is not treated as a high output.

4. $V_{OH(Max)}$ : (Low Level output voltage) This is the max. value of the output voltage which will consider as a logic low level. If the output voltage is higher than this value then it will not be treated as low output.

# Current Parameters:

1. $I_{IL(Max)}$ : Lower level input current
2. $I_{IH(Min)}$ : High level Input current
3. $I_{OH(Min)}$ : High level output current
4. $I_{OL(Max)}$ : Low level output current

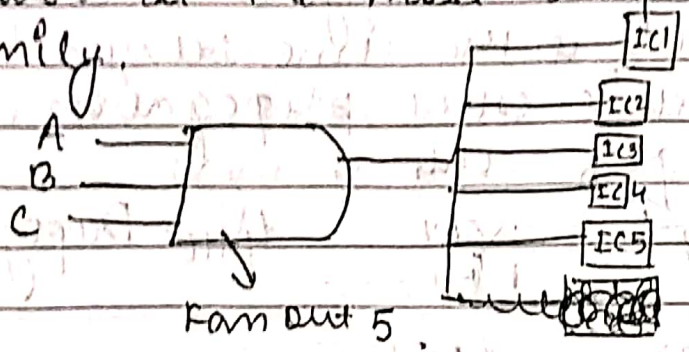
* Fan in and fan out: Fan in is defined as the no. of input a gate has. for eg: Two input gate will have a fan in = 2



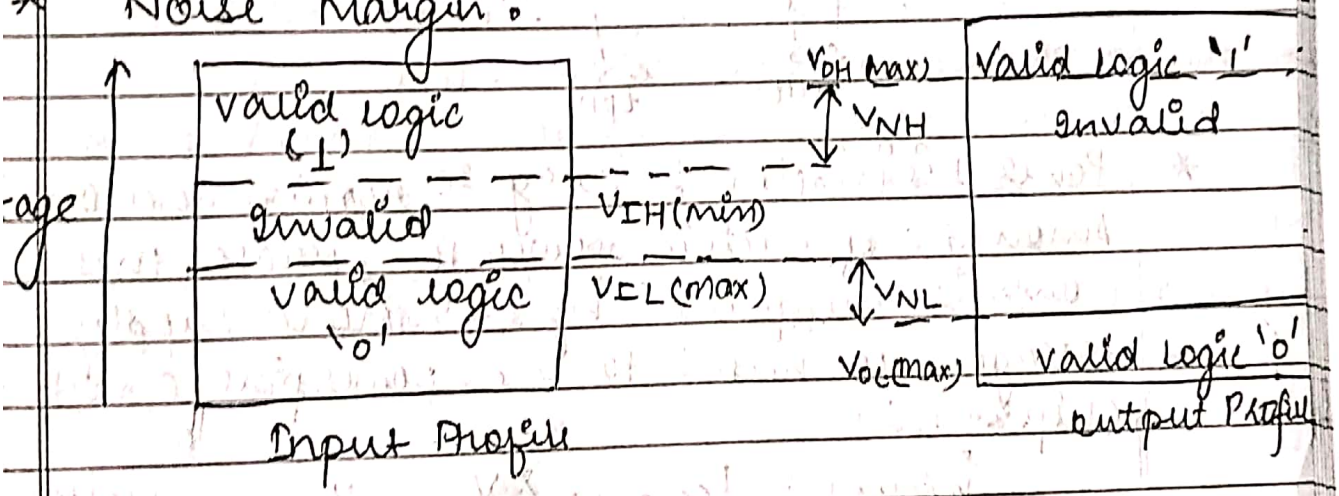

Fan in = 2 Fan in = 3

Fanout is defined as a max. no of inputs of the same IC families can write without falling outside the specified output voltage limits.

For eg: a fan out of 5 indicates that gate can drive at the most 5 input of the same IC family.




* Noise Margin:




$V_{NH}$ → higher level Noise Margin

$$V_{NH} = V_{OH(min)} - V_{IH(min)}$$

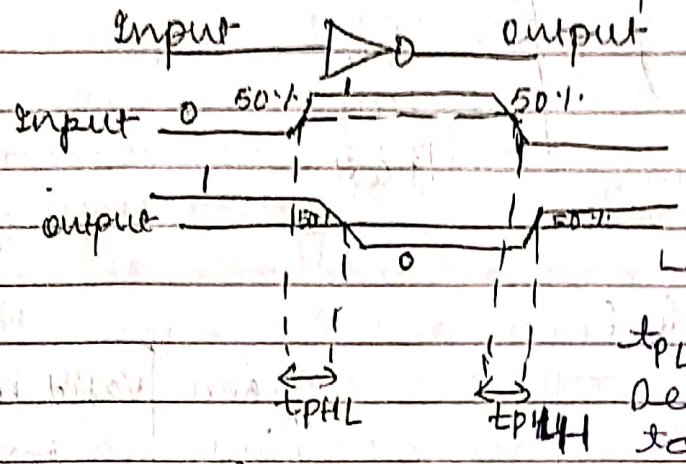
$V_{NL}$ → Low level Noise Margin

$$V_{NL} = V_{IL(max)} - V_{OL(max)}$$

Noise immunity of any digital IC is defined as Ability of logic circuit to tolerate Noise without causing any unwanted changes in the output.

A quantitive measure of noise immunity is called noise margin.

# Propogation Delay: The output of logic gate doesnot change its state instantaneously in response to the change in the state of its input. This is the time delayed b/w two events which is called propogation Delay.

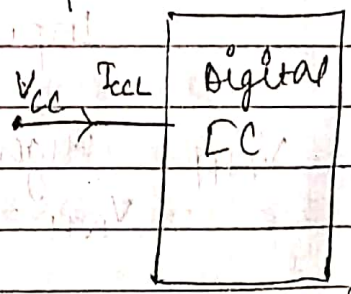



$t_{PHL}$ = Propogation Delay for High Logic to Low Logic

$t_{PLH}$ ⇒ Propogation Delay for Low Logic to High Logic

* Power Dissipation: Every IC require certain Amount of electric power to operate this power is supplied by 1 or more supply voltage connected to the powerpins on the chip.

$$P_D(avg) = I_{CC}(avg) \times V_{CC}$$




$$I_{CC}(avg) = \frac{I_{CCH} + I_{CCL}}{2}$$

$V_{CC}$ = Supply voltage

$V_{CCH}$ = current drawn from power supply for logic 1

As a result of applied voltage & current flow through the logic IC _____ some power will be dissipated from it in the form of heat. This power is in the

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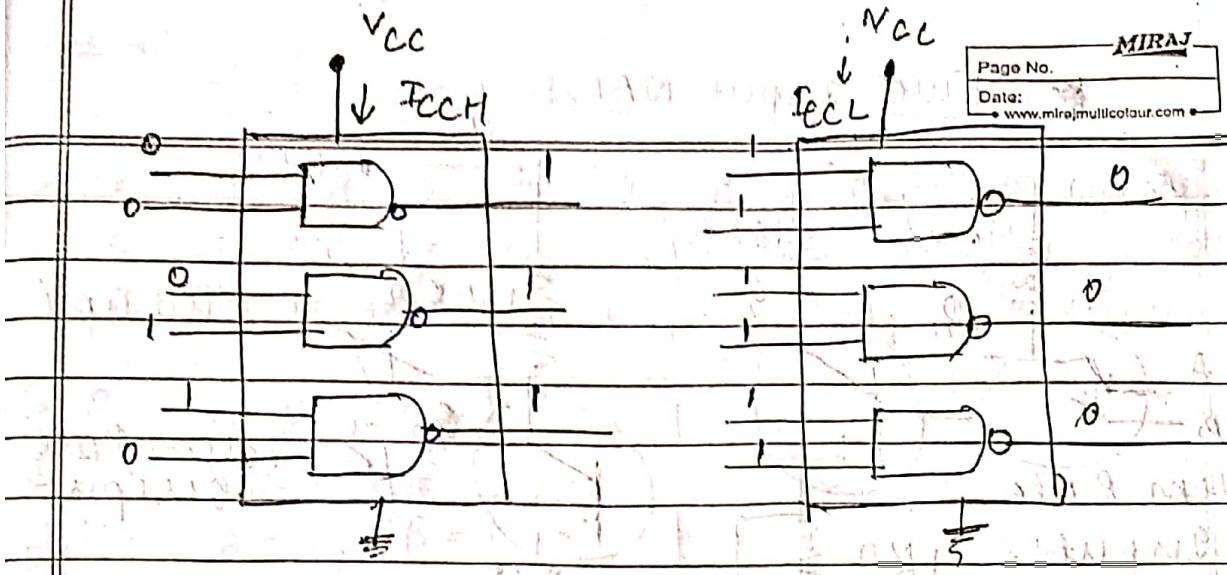


$V_{CCL}$ = current Drawn from power Supply for logic 0 from Supply voltage.

# Speed of power product (figure Merit):
In general for any digital IC it is desirable to have shorter propogation delay & lower value of power dissipation.
This is usually trade-off b/w ~~overall performance of IC family~~ switching of power dissipation so, that speed is gain at the expense of ↑ing power dissipation. ∴ common means for measuring & comparing the overall performance of IC family is the speed of power product. It is also known as a figure of merit.

Speed of Power Product = Production delay × Power dissipation

$= \text{Second} \times \frac{\text{Joule}}{\text{Sec.}}$

unit of speed of Power Product = Joule.

# Logical Families:
1. TTL → Transistor - Transistor logic
   (A) Multiple Emitter Transistor:

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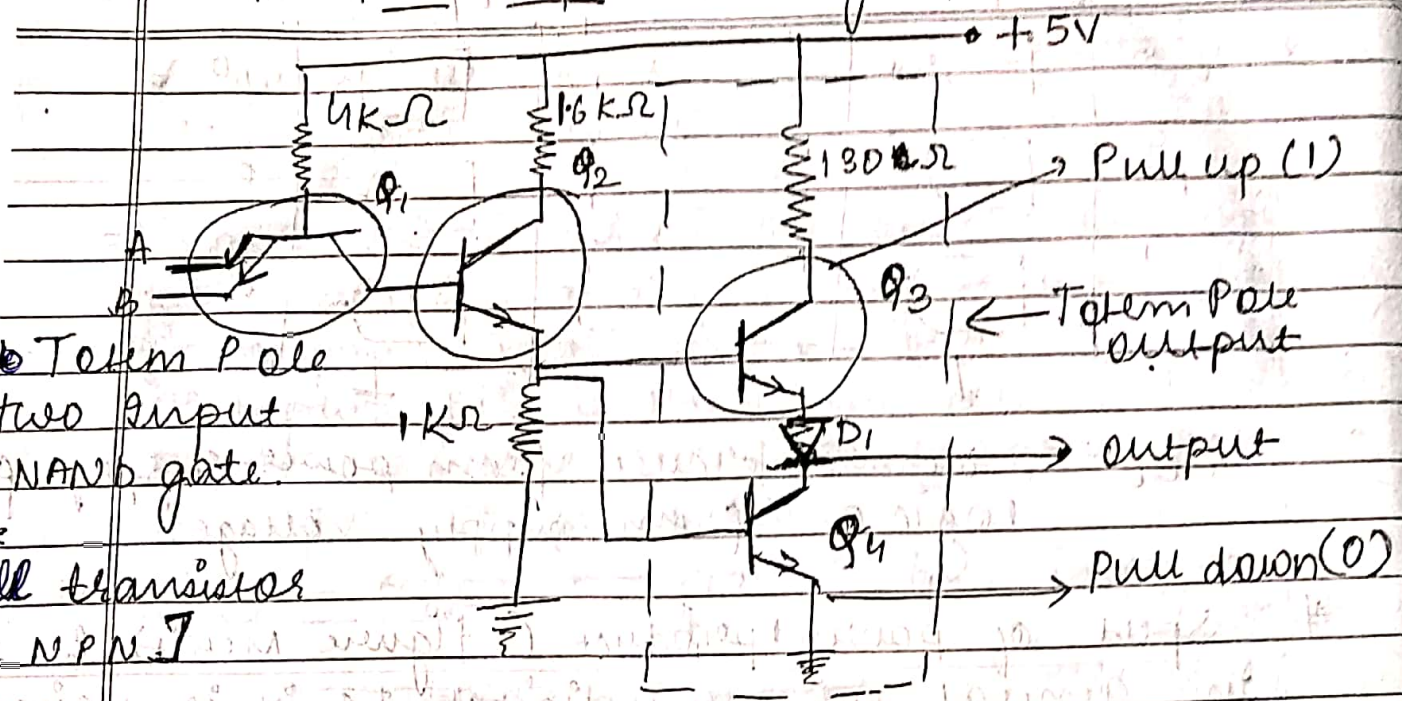
# Two Input NAND gate



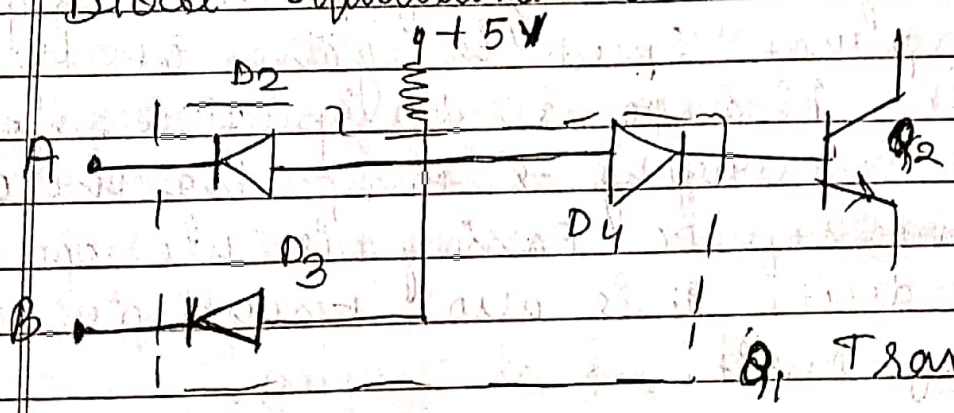

Totem Pole two Input NAND gate.

Pull transistor (NPN)

$Q_3 \rightarrow$ Emitter Follower Transistor

$Q_3, Q_4 \rightarrow$ Totem Pole Transistor

Diode Equivalent circuit for $Q_1$ Transistor:




If transistor is Forward biased then it is ON

If " " Reverse " " " " OFF

| A | B | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | output = Y |
|---|---|---|---|---|---|---|
| 0 | 0 | ON | OFF | ON | OFF | 1 |
| 0 | 1 | ON | OFF | ON | OFF | 1 |
| 1 | 0 | ON | OFF | ON | OFF | 1 |
| 1 | 1 | OFF | ON | OFF | ON | 0 |

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Ans 1. If A = 0, B = 0, then Totem Transistor $Q_1$ is ON, $Q_2$ transistor is OFF, $Q_3$ is ON & $Q_4$ is OFF, so that output is high

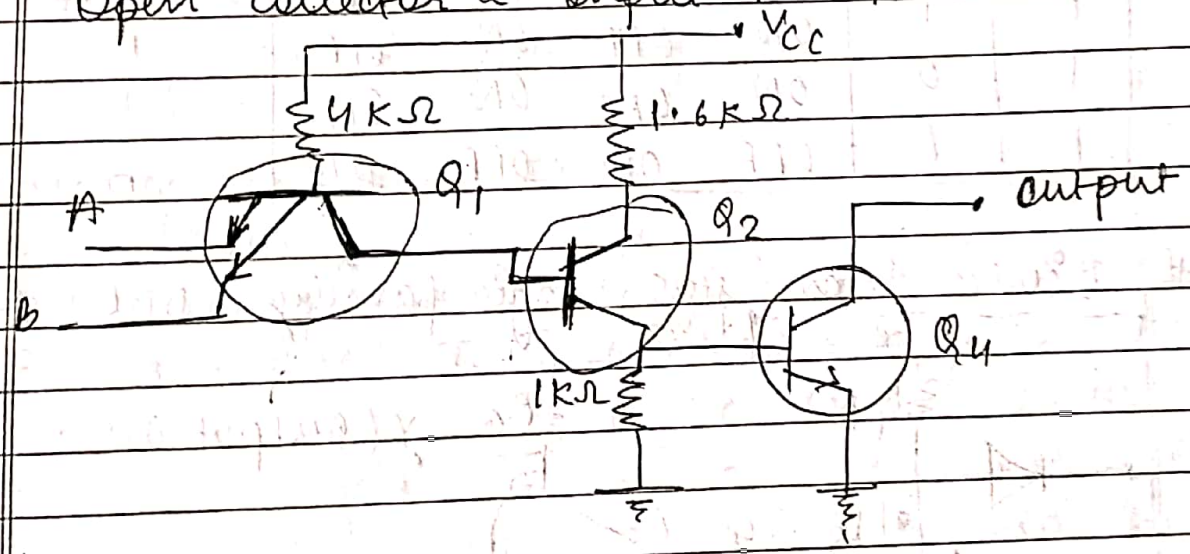
Ans 2. A = 0, B = 1

Ans 3. A = 1, B = 0

Ans 4. A = 1, B = 1

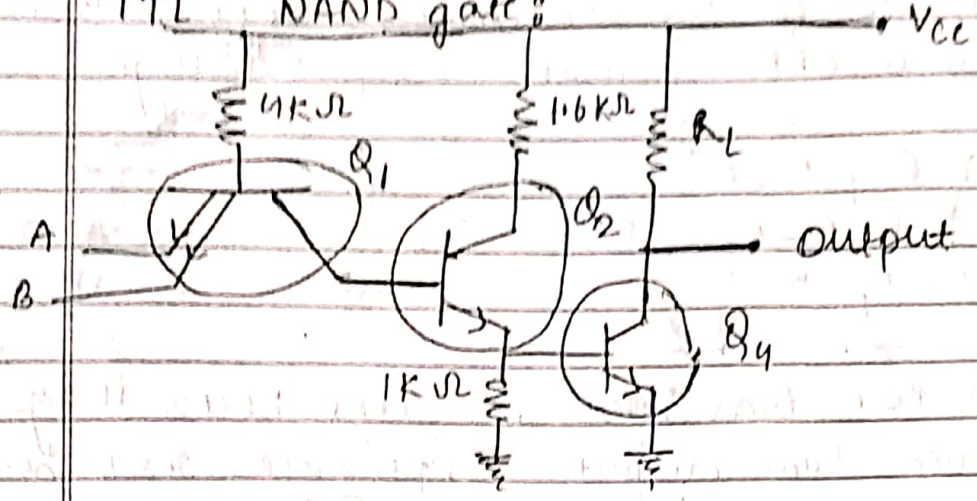
Totem Pole transistor are used becoz they produce low output impedence. It means output voltage can change quickly.

B. Open collector 2-Input TTL NAND Gate:



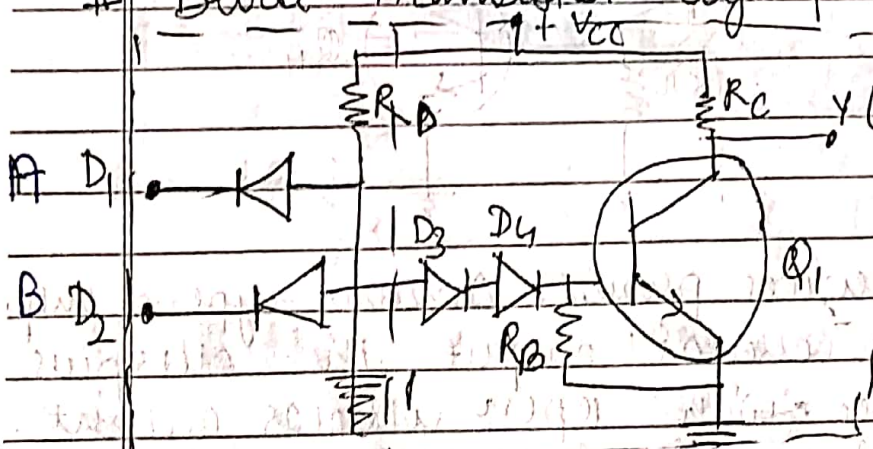

Some TTL Devices provide another type of output called open collector output. The outputs 2 of diff gate with open collector output can be tied together, this is known as wired logic. Becoz the collector of Q-code transistor is open. The gate like this will not work properly until you connected external pull up resistor.

c. Open collector with pull up Resistor 2 Input TTL NAND gate:




| A | B | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | output = Y |
|---|---|---|---|---|---|---|
| 0 | 0 | ON | OFF | ON | OFF | 1 |
| 0 | 1 | ON | OFF | ON | OFF | 1 |
| 1 | 0 | ON | OFF | ON | OFF | 1 |
| 1 | 1 | OFF | ON | OFF | ON | 0 |

# Diode Transistor Logic family (DTL) :-




A, B → Input of NAND gate

Y → output of NAND gate.

A logic circuit working as a 2 input NAND gate

It consist of 2 input stage comprising of Diode $D_1$, $D_2$ & $R_D$ Resistance working as an AND gate.

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It is followed by transistorized NOT gate.

Working of circuit:

| A | B | $D_1$ | $D_2$ | $D_3$ | $D_4$ | Q | Y = output |
|---|---|---|---|---|---|---|---|
| 0 | 0 | ON | ON | ON | ON | OFF | 1 |
| 0 | 1 | ON | OFF | ON | ON | OFF | 1 |
| 1 | 0 | OFF | ON | ON | ON | OFF | 1 |
| 1 | 1 | OFF | OFF | OFF | OFF | ON | 0 |

Emitter coupled logic family (ECL): The TTL family use transistor operating in saturating mode. As a result there switching speed is very slow. In ECL family has been developed that prevent transistor operated in saturation mode. thereby, ↑ing overall switching speed.

* characteristics of ECL:
→ It is the Fastest logic family.
→ The propogation delay is less than 1 ns.
→ Transistor are not allowed to go into the saturation, so that logical levels are kept close to each other. So, that noise margin is reduced. So, it is easily affected by noisy environment.
→ Another disadvantage is that power consumption is more.

* Basic ECL circuit of inverter/Buffer circuit:

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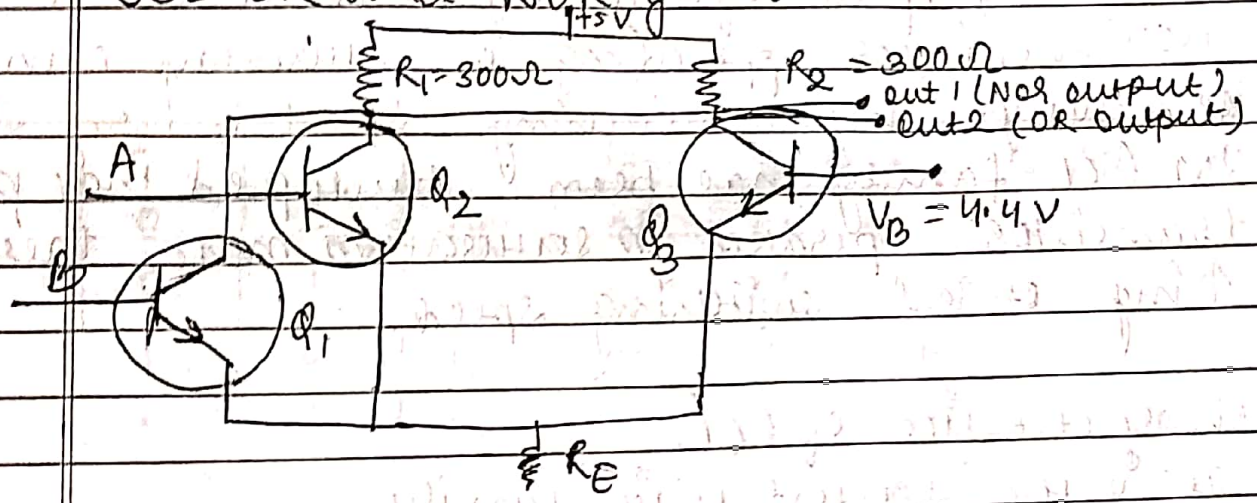
The fig. shows the basic Inverter & Buffer circuit in ECL family. It consist of two transistor connected in differential single ended Input mode, with a common emitter Resistance. The circuit has two outputs, Inverting output (out 1) & non Inverting output (out 2).

## * ECL OR and NOR gate:




$Q_1, Q_2, Q_3 \rightarrow$ BJT Transistor
A, B $\rightarrow$ Input of OR & NOR gate circuit.
out 1 $\rightarrow$ output of NOR gate
out 2 $\rightarrow$ output of OR gate
At Input side voltage level
logic 1 $\rightarrow$ 4.4V
logic 0 $\rightarrow$ 3.6V
At output side voltage level
logic 1 $\rightarrow$ 5V
logic 0 $\rightarrow$ 4.2V

The figure shows 2 input ECL OR and NOR gate. It is consist of 2 Transistor $Q_1$ & $Q_3$ connected in differential single ended input. It consist of one additional transistor $Q_2$

parallel with $Q_1$ Transistor. The out1 represents the NOR gate output & out2 represents the OR gate output.

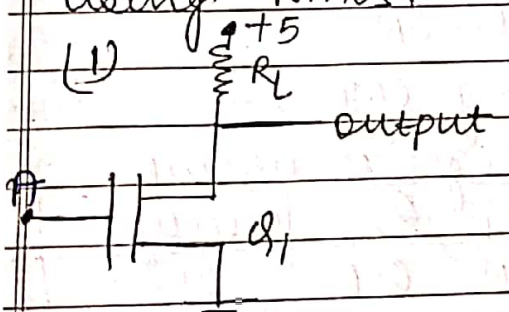
Working of circuit:

| A | B | $Q_1$ | $Q_2$ | $Q_3$ | out1 | out2 |
|---|---|---|---|---|---|---|
| 0 | 0 | OFF | OFF | ON | 1 | 0 |
| 0 | 1 | OFF | ON | OFF | 0 | 1 |
| 1 | 0 | ON | OFF | OFF | 0 | 1 |
| 1 | 1 | ON | ON | OFF | 0 | 1 |

## MOSFET Families:

1. NMOSFET:- Implementation of Not gate using NMOS.

(i)

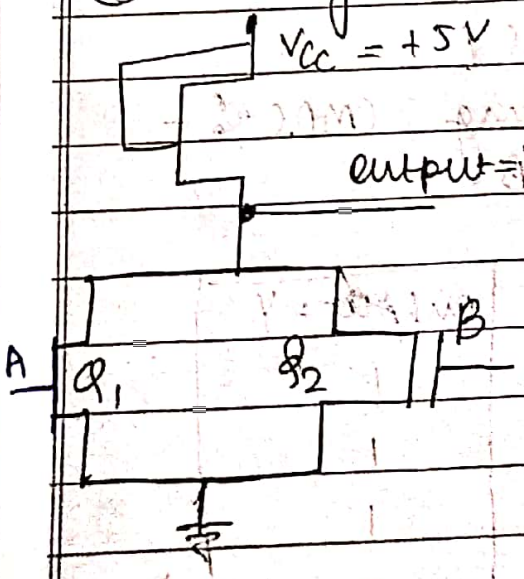



| A | $Q_1$ | Y = output |
|---|---|---|
| 0 | OFF | 1 |
| 1 | ON | 0 |

Act as Inverter

$Q_1$ is OFF when A is 0.

(ii) NOR gate using NMOSFET:-




| A | B | $Q_1$ | $Q_2$ | output |
|---|---|---|---|---|
| 0 | 0 | OFF | OFF | 1 |
| 0 | 1 | OFF | ON | 0 |
| 1 | 0 | ON | OFF | 0 |
| 1 | 1 | ON | ON | 0 |

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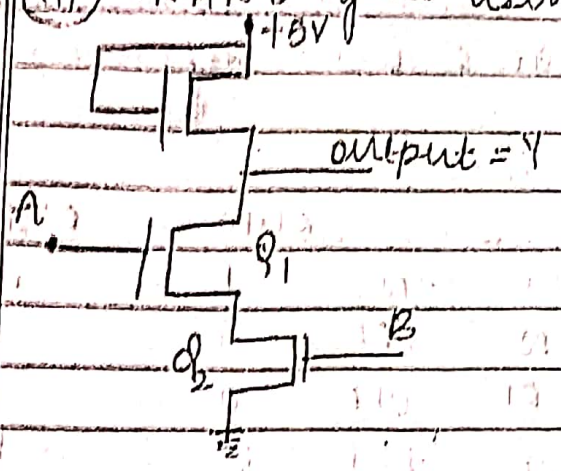
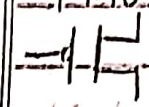
(iii) NAND gate using NMOSFET :




| A | B | $Q_1$ | $Q_2$ | output = Y |
|---|---|---|---|---|
| 0 | 0 | OFF | OFF | 1 |
| 0 | 1 | OFF | ON | 1 |
| 1 | 0 | ON | OFF | 1 |
| 1 | 1 | ON | ON | 0 |

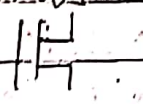
(i) PMOS



0 → ON

1 → OFF

(ii) NMOS

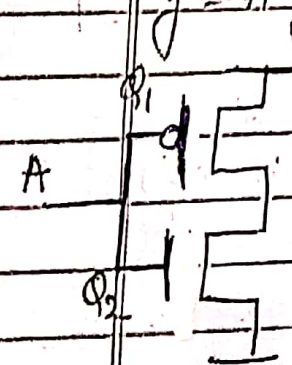


0 → OFF

1 → ON

Implement NOT gate using CMOS :-

$y = \bar{A}$




Working of circuit

| A | $Q_1$ | $Q_2$ | output = Y |
|---|---|---|---|
| 0 | ON | OFF | 1 |
| 1 | OFF | ON | 0 |

| | AND | OR |
|---|---|---|
| NMOS | Series | Parallel |
| PMOS | Parallel | Series |

Implement NAND gate using CMOS :-

$y = \overline{A \cdot B}$ $\quad \bar{y} = A \cdot B$

Working of circuit

| A | B | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | output = Y |
|---|---|---|---|---|---|---|
| 0 | 0 | ON | ON | OFF | OFF | 1 |
| 0 | 1 | ON | OFF | OFF | ON | 1 |
| 1 | 0 | OFF | ON | ON | OFF | 1 |
| 1 | 1 | OFF | OFF | ON | ON | 0 |

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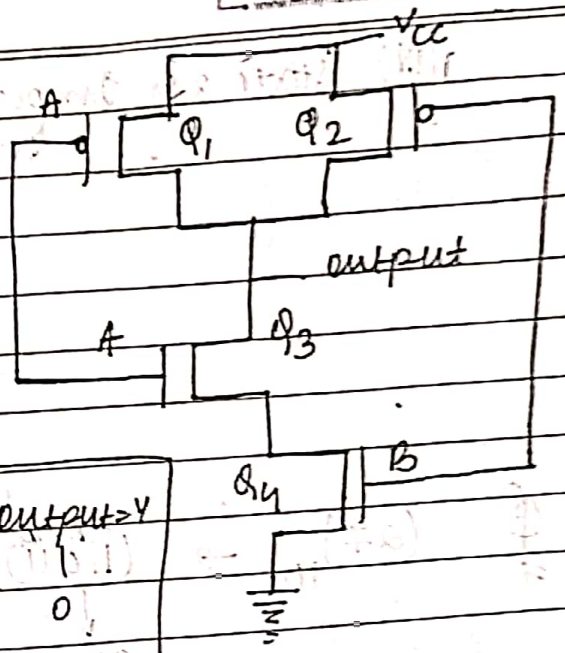
Implement 2 input NOR gate :-

$Y = \overline{A+B}$

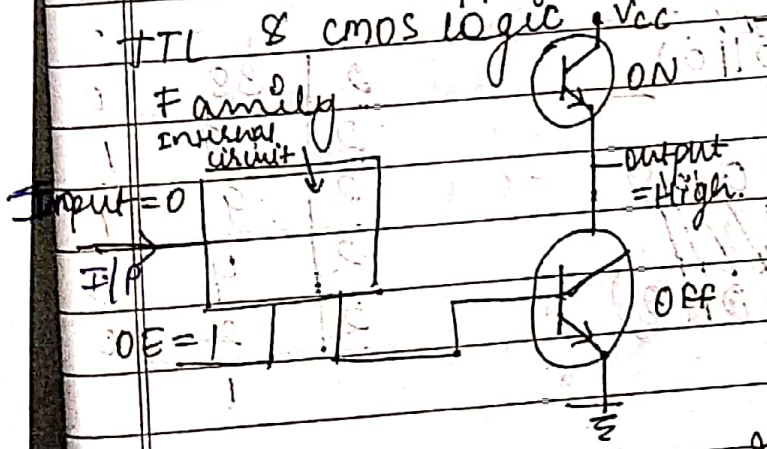
$\overline{Y} = A+B$

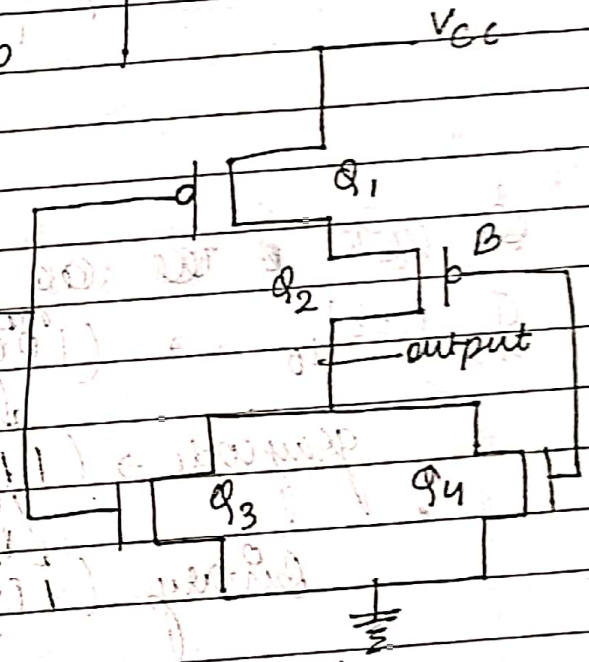



Working of NOR gate

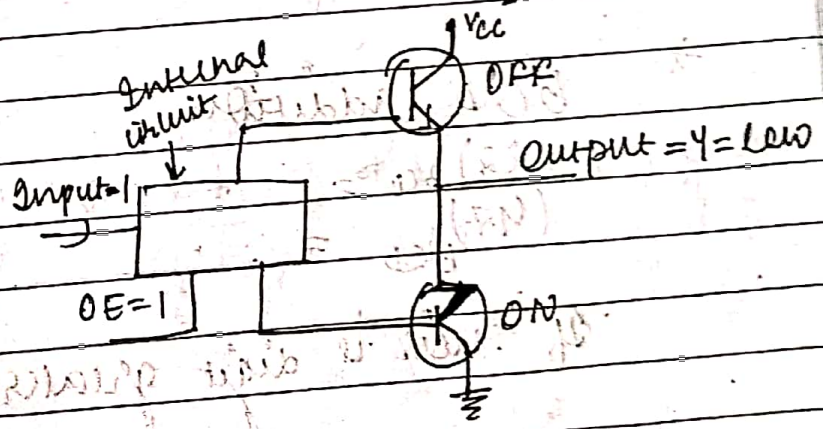
| A | B | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | output=Y |
|---|---|---|---|---|---|---|
| 0 | 0 | ON | ON | OFF | OFF | 1 |
| 0 | 1 | ON | OFF | OFF | ON | 0 |
| 1 | 0 | OFF | ON | ON | OFF | 0 |
| 1 | 1 | OFF | OFF | ON | ON | 0 |

Three state output of TTL & CMOS logic Family

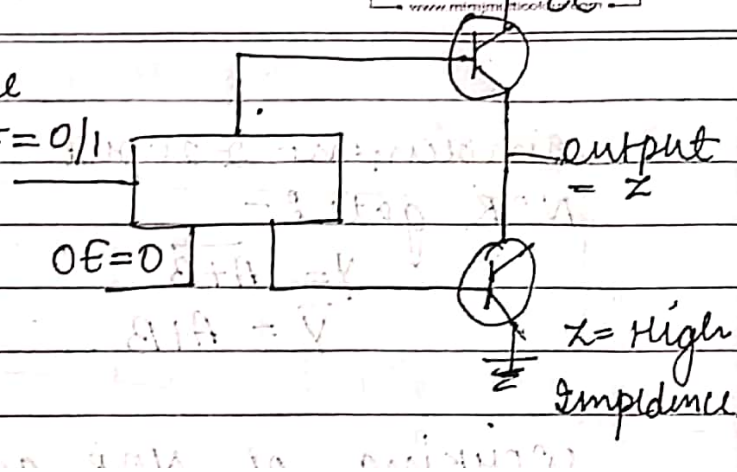



(II) State 2 : Low



(III) State 3: Impedence

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## 3.16 REALIZATION OF LOGIC GATES IN RESISTOR TRANSISTOR LOGIC (RTL)

### 1. Basic Aspects

RTL logic is the earliest logic family but it has becomes obsolete now. The long form of RTL is resistor transistor, logic which suggests that it uses resistors and transistors. The basic RTL gate is a NOR gate as shown in figure 3.66.

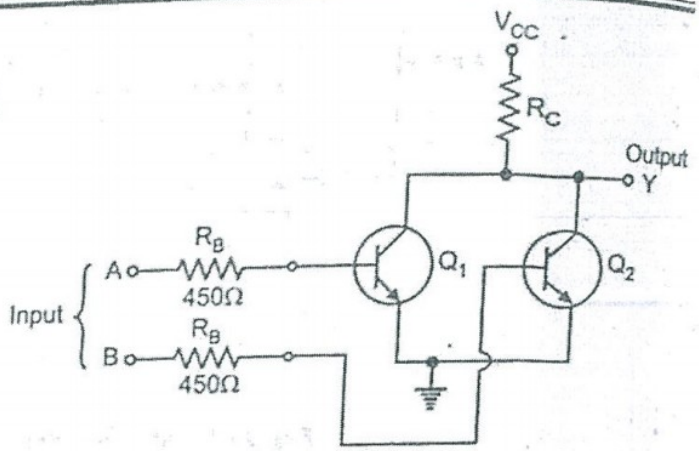


Fig. 3.66. 2 Input RTL NOR gate

### 2. Working Operation

1. A = B = 0
   (i) With A = B = 0, both the transistors remain off. The current through $R_C$ is zero, so drop across it is zero.
   (ii) The output voltage is equal to $V_{CC}$ i.e., 1.
   Therefore, for A = B = 0, Y = 1

2. A = 0, B = 1
   (i) With A = 0 and B = 1, transistor $Q_1$ is off and $Q_2$ goes into saturation.
   (ii) Hence, the output voltage $V_o = V_{CE2(sat)}$ i.e., 0.
   Therefore, for A = 0, B = 1, Y = 0

3. A = 1, B = 0:
   (i) With A = 1 and B = 0, transistor $Q_1$ is saturated and $Q_2$ is turned off.
   (ii) Hence, the output voltage $Y = V_{CE1\ (sat)}$ i.e., 0.
   Therefore, for A = 1, B = 0, Y = 0

4. A = B = 1
   (i) With A = B = 1, both the transistors saturate and output voltage is equal to saturation voltage
   Therefore, A = B = 1, Y = 0

| A | B | $Q_1$ | $Q_2$ | Y |
|---|---|---|---|---|
| 0 | 0 | OFF | OFF | 1 |
| 0 | 1 | OFF | ON | 0 |
| 1 | 0 | ON | OFF | 0 |
| 1 | 1 | ON | ON | 0 |

### 3. Important characteristics of RTL family

(i) Poor noise margin
(ii) Poor fan out
(iii) Low speed
(iv) High power dissipation

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### 3.7.2. Performance Comparison of Totem-pole and Open Collector Outputs

Table 3.1. Performance comparison of totem-pole and open collector outputs

| S.No. | Parameter of comparison | Totem-pole | Open collector |
|---|---|---|---|
| 1. | Circuit components on the output side | $Q_3$ (pull up transistor), D and $Q_4$ (pull down transistor) are used. | Only the pull down transistor $Q_4$ is used. |
| 2. | Wired ANDing | Cannot be done | Easily be done |
| 3. | External pull up resistor | Not required | Required to be connected. |
| 4. | Power Dissipation | Low due to presence of pull up transistor $Q_3$. | High due to current flowing through $R_3$. |
| 5. | Speed | Operating speed is high. | Operating speed is low |

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## Comparision between Various Logic Family

| Parameter | RTL | DCTL | DTL | TTL | ECL | CMOS |
|---|---|---|---|---|---|---|
| Component Use | Resistor and Transistor | Resistor and Transistor | Resistor, Diode and Transistor | Resistor, Diode and Transistor | Transistor and Resistor | PMOSFET and NMOSFET |
| Circuit | Simple | Simple | Moderate | Complex | Medium | Complex |
| Noise Margin. | Poor | Poor | High | Medium | Low | Medium |
| Fan-out | Low (4) | Low (4) | Medium (8) | Medium (10) | Large (45) | Large (50) |
| Power Dissipation in mV | 30 | 30 | 8-12 | 10 | 40-45 | 0.01 |
| Basic gate | NOR | NOR | NAND | NAND | OR-NOR | CMOS Inverter |
| Propagation Delay in ms | 12 | 10 | 30 | 10 | 2 | 0.1 |
| Speed Power Product | 144 | 130 | 300 | 100 | 40 (ECL 100K) 100 (ECL 10K) | 10-5 |

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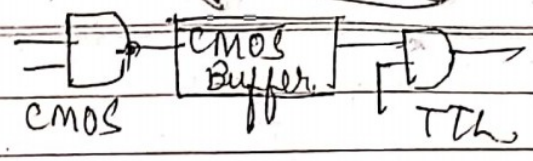
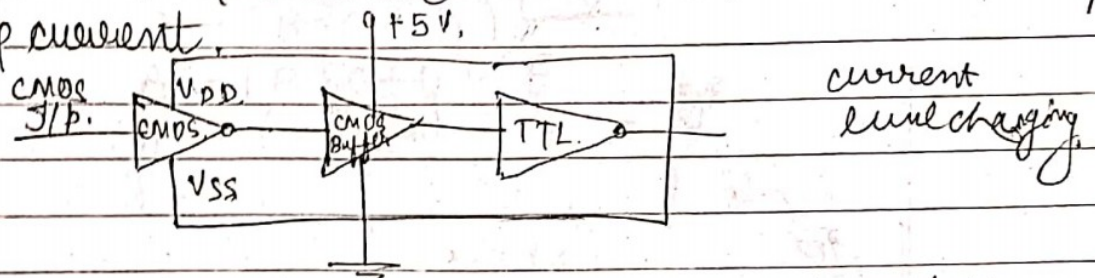
## (i) CMOS & TTL Interfacing

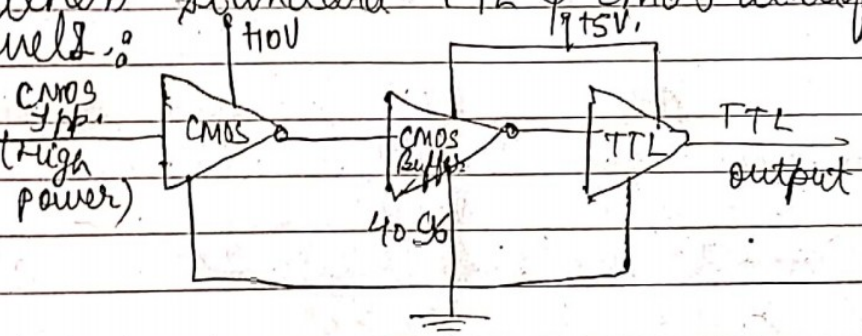



To drive a standard TTL device from a CMOS IC requires the CMOS Buffer as the Intermediate stat to Increase the current capability of CMOS Transistor.

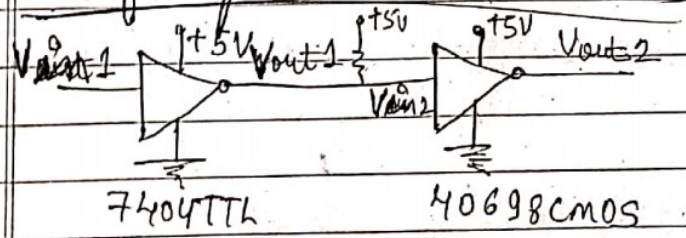
(a) When TTL & CMOS are connected to the same Voltage & current.




(b) When standard TTL & CMOS at diff. Voltage levels :




### Interfacing b/w TTL & CMOS




When a TTL is driving CMOS gates. condition at TTL output must match condition at CMOS input. The problem arise because $V_{OH}$ of TTL is less than $V_{IH}$ of CMOS. $V_{IH}$ of CMOS cannot be lowered. Therefore, pull up of $V_{OH}$ of TTL gates.

Where $V_{OH}$ of TTL 3.8 ↓ $V_{IH}$ of CMOS 5.0

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