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Encoder.

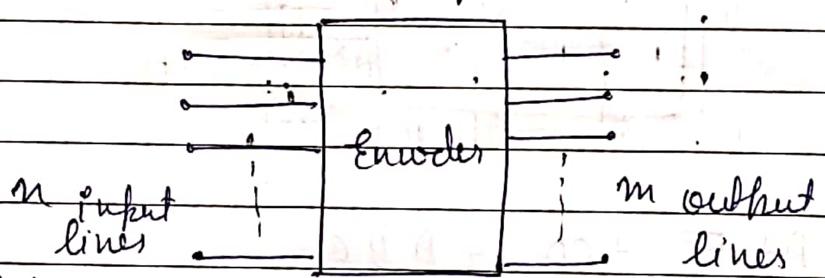
Encoder is a combinational circuit which is designed to perform to convert one number system to another number system format.

Encoder has a 'n' numbers of input lines and 'n' number of output lines.

There are 4 types of encoders.

i) Octal to Binary encoder.
ii) Hexadecimal to Binary Encoder.
(iii) Priority Encoder.
(iv) BCD to excess 3 Encoder

Block diagram of Encoder

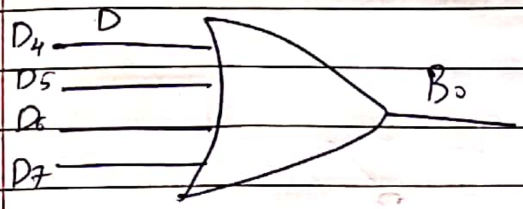


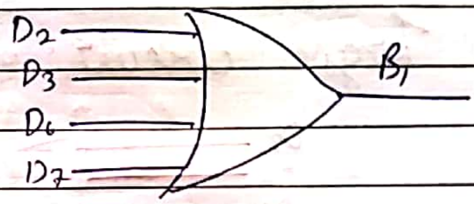
i) Octal to Binary Encoder.

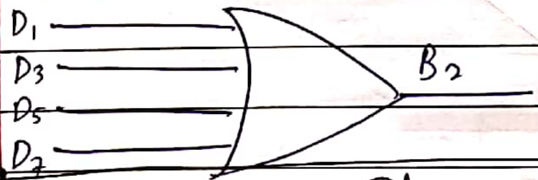
Digit	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	B_0	B_1	B_2
0	1	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	1
2	0	0	1	0	0	0	0	0	0	1	0
3	0	0	0	1	0	0	0	0	0	1	1
4	0	0	0	0	1	0	0	0	1	0	0
5	0	0	0	0	0	1	0	0	1	0	1
6	0	0	0	0	0	0	1	0	1	1	0
7	0	0	0	0	0	0	0	1	1	1	1

Logical Expression.

$$B_0 = D_4 + D_5 + D_6 + D_7$$
$$B_1 = D_2 + D_3 + D_6 + D_7$$
$$B_2 = D_1 + D_3 + D_5 + D_7$$







	I/P																O/P			
Digits	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	B_0	B_1	B_2	B_3
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
3	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1
8	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1
10	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0
11	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1	1
12	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0
13	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1
14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0
15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

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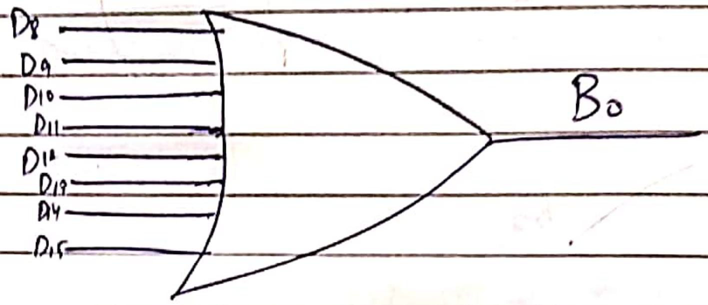
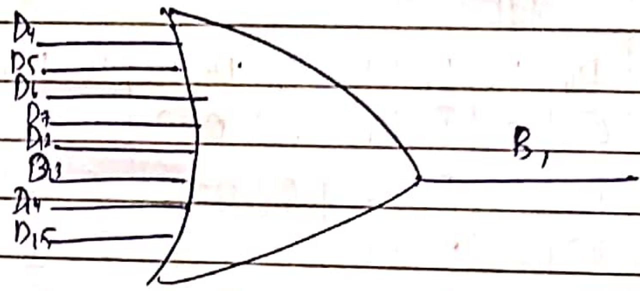
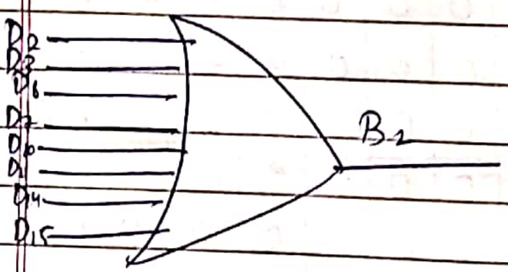
Logical Expression

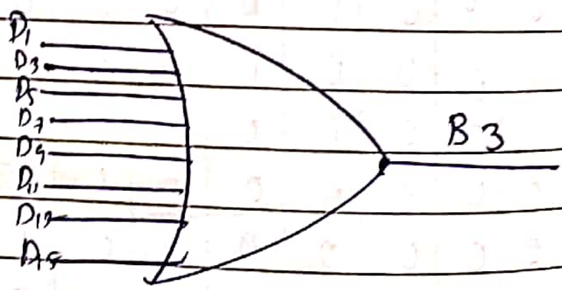
$B_0 = D_8 + D_9 + D_{10} + D_{11} + D_{12} + D_{13} + D_{14} + D_{15}$
$B_1 = D_4 + D_5 + D_6 + D_7 + D_{12} + D_{13} + D_{14} + D_{15}$
$B_2 = D_2 + D_3 + D_6 + D_7 + D_{10} + D_{11} + D_{14} + D_{15}$
$B_3 = D_1 + D_3 + D_5 + D_7 + D_9 + D_{11} + D_{13} + D_{15}$

Logic circuit:









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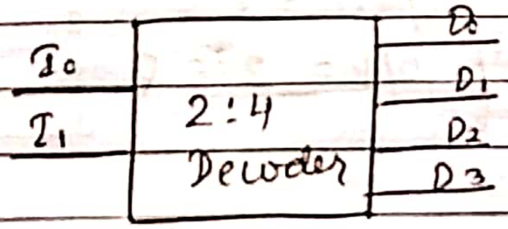
Decoder

Decoder is a combinational circuit, it convert n- bit binary input into the 2^n outputs.

1) 2 : 4 Decoder.
If Number of line is input $n=2$

output lines are $2^n = 2^2 = 4$



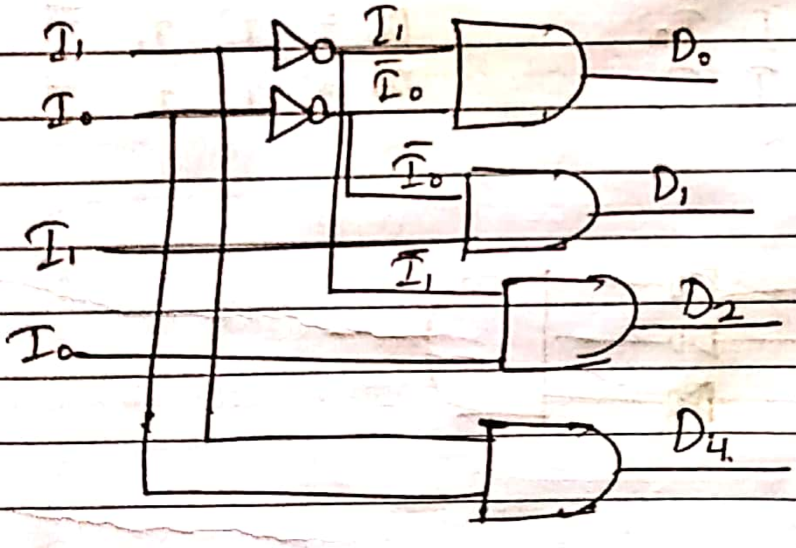
	I/P		O/P			
Digit	I_0	I_1	D_0	D_1	D_2	D_3
0	0	0	1	0	0	0
1	0	1	0	1	0	0
2	1	0	0	0	1	0
3	1	1	0	0	0	1

logical Expression of :-

$D_0 = \overline{I_0}\,\overline{I_1}$ $\quad$ $D_1 = \overline{I_0}\, I_1$

$D_2 = I_0\, \overline{I_1}$ $\quad$ $D_3 = I_0\, I_1$

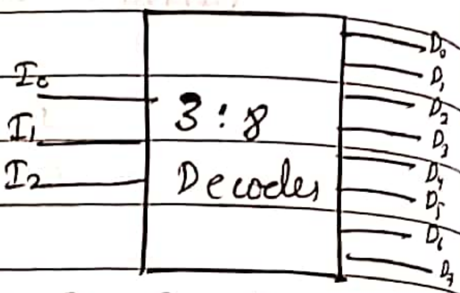
Circuit



2 : 4 Decoder

2) 3:8 Decoder.

If No. of input = 3
No. of o/p = $2^3 = 8$



Digits	I_0	I_1	I_2	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
2	0	1	0	0	0	1	0	0	0	0	0
3	0	1	1	0	0	0	1	0	0	0	0
4	1	0	0	0	0	0	0	1	0	0	0
5	1	0	1	0	0	0	0	0	1	0	0
6	1	1	0	0	0	0	0	0	0	1	0
7	1	1	1	0	0	0	0	0	0	0	1

⇒ Logical Expression of

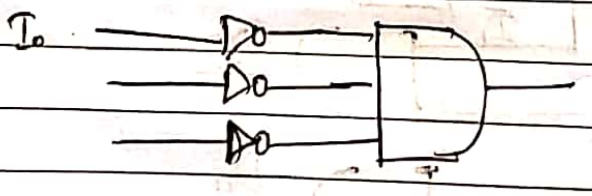
$D_0 = \overline{I_0}\,\overline{I_1}\,\overline{I_2}$ $\quad D_4 = I_0\,\overline{I_1}\,\overline{I_2}$

$D_1 = \overline{I_0}\,\overline{I_1}\,I_2$ $\quad D_5 = I_0\,\overline{I_1}\,I_2$

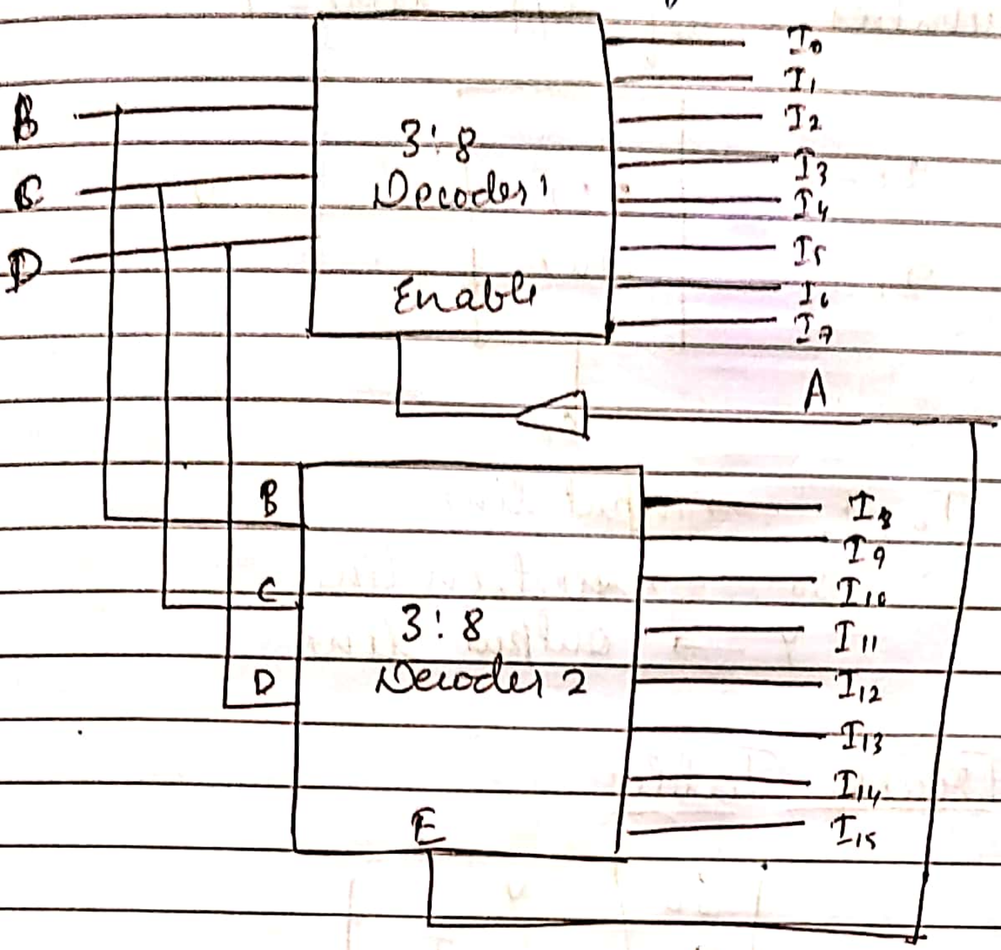
$D_2 = \overline{I_0}\,I_1\,\overline{I_2}$ $\quad D_6 = I_0\,I_1\,\overline{I_2}$

$D_3 = \overline{I_0}\,I_1\,I_2$ $\quad D_7 = I_0\,I_1\,I_2$

Circuits



Implement 4:16 decorder using 3:8 decoder.



Working

i) If A = 0, the Decoder 1 is enable & Decoder 2 is disable procedure output I_0 to I_7

(ii) If A = 1, The Decoder 1 is disable & Decoder 2 is enable. Procedure output I_8 & I_{15}

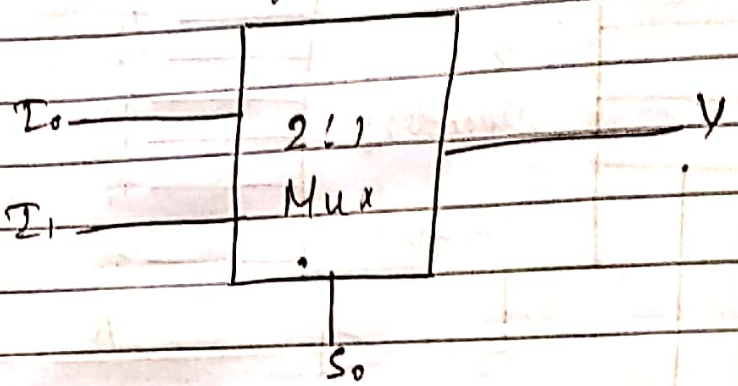
<u>Multiplexer</u>:-

Multiplexer is a special type of combinational circuit it contain n selection lines, 2^n input lines and 1 output line.

i) 2:1 Mux.

Number of i/p lines $= 2^1 = 2$.

Number of selection lines = 1
Number of O/P line = 1

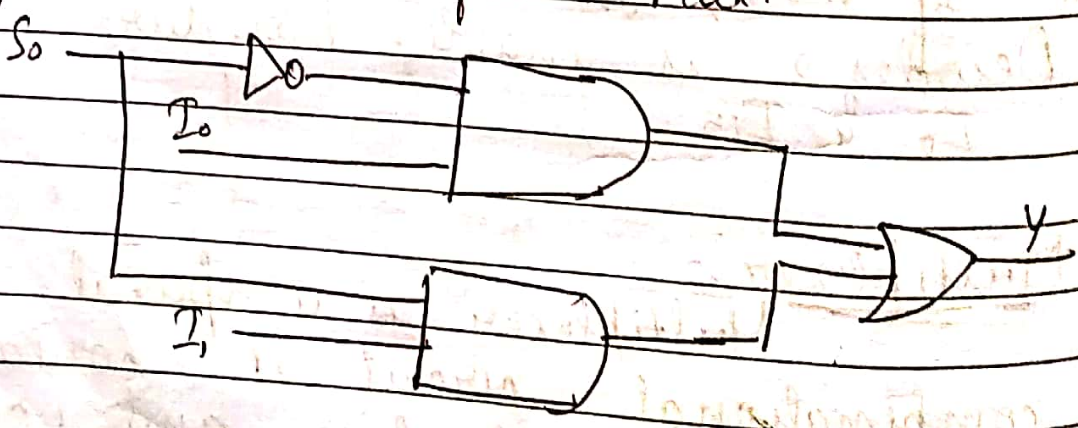


I_0 ; I_1 → input line.
S_0 → selection line
Y → output line.

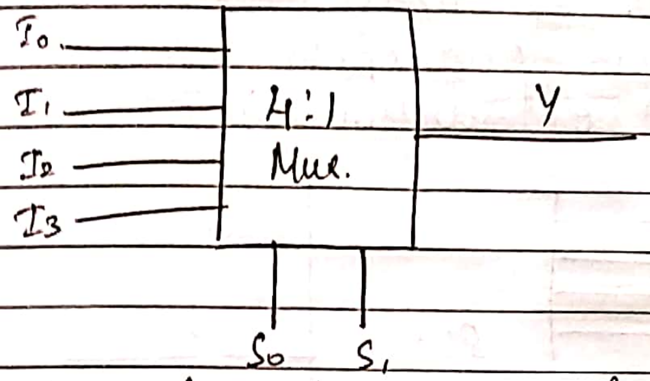
Truth Table

S_0	Y
0	$Y = I_0$
1	$Y = I_1$

Logical Expression
$$Y = \bar{S_0} I_0 + S_0 I_1$$
Logical circuit of 2:1 Mux.



(ii) 4:1 Mux.



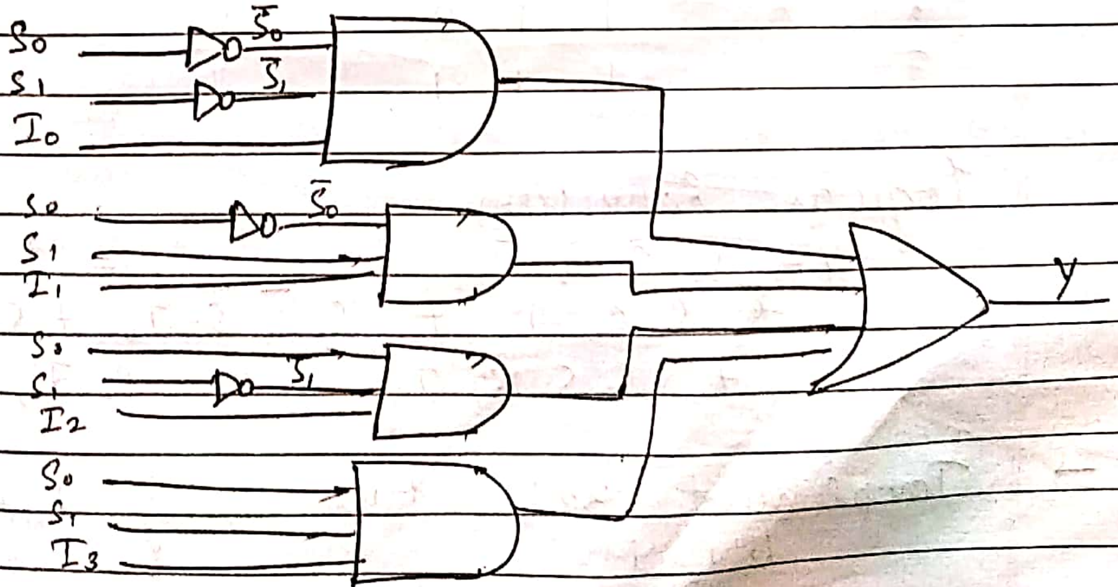
Number of i/p lines $= 4 = 2^2$
Number of ~~o/~~ selection lines = 2.
Number of output lines = 1

~~Tr~~
Truth table.

S_0	S_1	Y
0	0	$Y = I_0$
0	1	$Y = I_1$
1	0	$Y = I_2$
1	1	$Y = I_3$

Logical Expression

$$Y = \bar{S}_0 \bar{S}_1 I_0 + \bar{S}_0 S_1 I_1 + S_0 \bar{S}_1 \bar{I}_2 + S_0 S_1 I_3$$

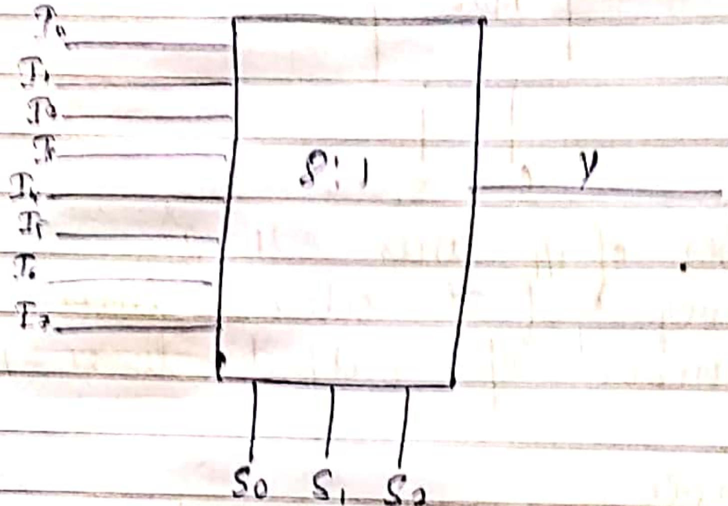


8:1 Mux.

Number of Inputs = 8 = 2^3

Number of outputs = 1

Number of selection lines = 3



Digit	I/P S_0	S_1	S_2	O/P Y
0	0	0	0	$Y = I_0$
1	0	0	1	$Y = I_1$
2	0	1	0	$Y = I_2$
3	0	1	1	$Y = I_3$
4	1	0	0	$Y = I_4$
5	1	0	1	$Y = I_5$
6	1	1	0	$Y = I_6$
7	1	1	1	$Y = I_7$

Logical Expression.

$$Y = \bar{S}_0 \bar{S}_1 \bar{S}_2 \bar{I}_0 + \bar{S}_0 \bar{S}_1 S_2 I_1 + \bar{S}_0 S_1 \bar{S}_2 I_2 + \bar{S}_0 S_1 S_2 I_3 + S_0 \bar{S}_1 \bar{S}_2 I_4 + S_0 \bar{S}_1 S_2 I_5 + S_0 S_1 \bar{S}_2 I_6 + S_0 S_1 S_2 I_7$$

⇒ Implement 32:1 Mux using 8:1 and 4:1 Mux.

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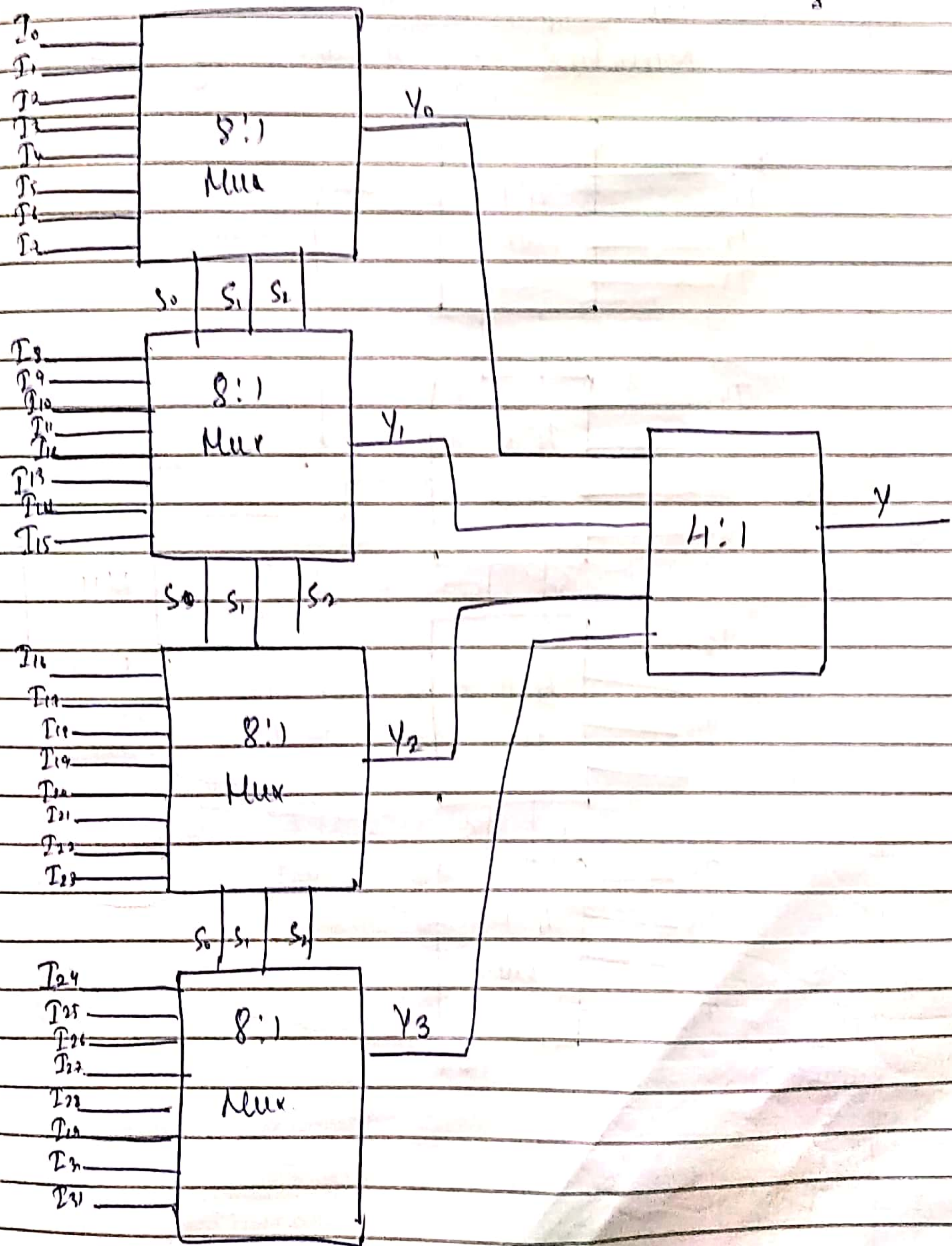
Implement 32:1 Mux :

Number of I/P = 32.

using 8:1 Mux.

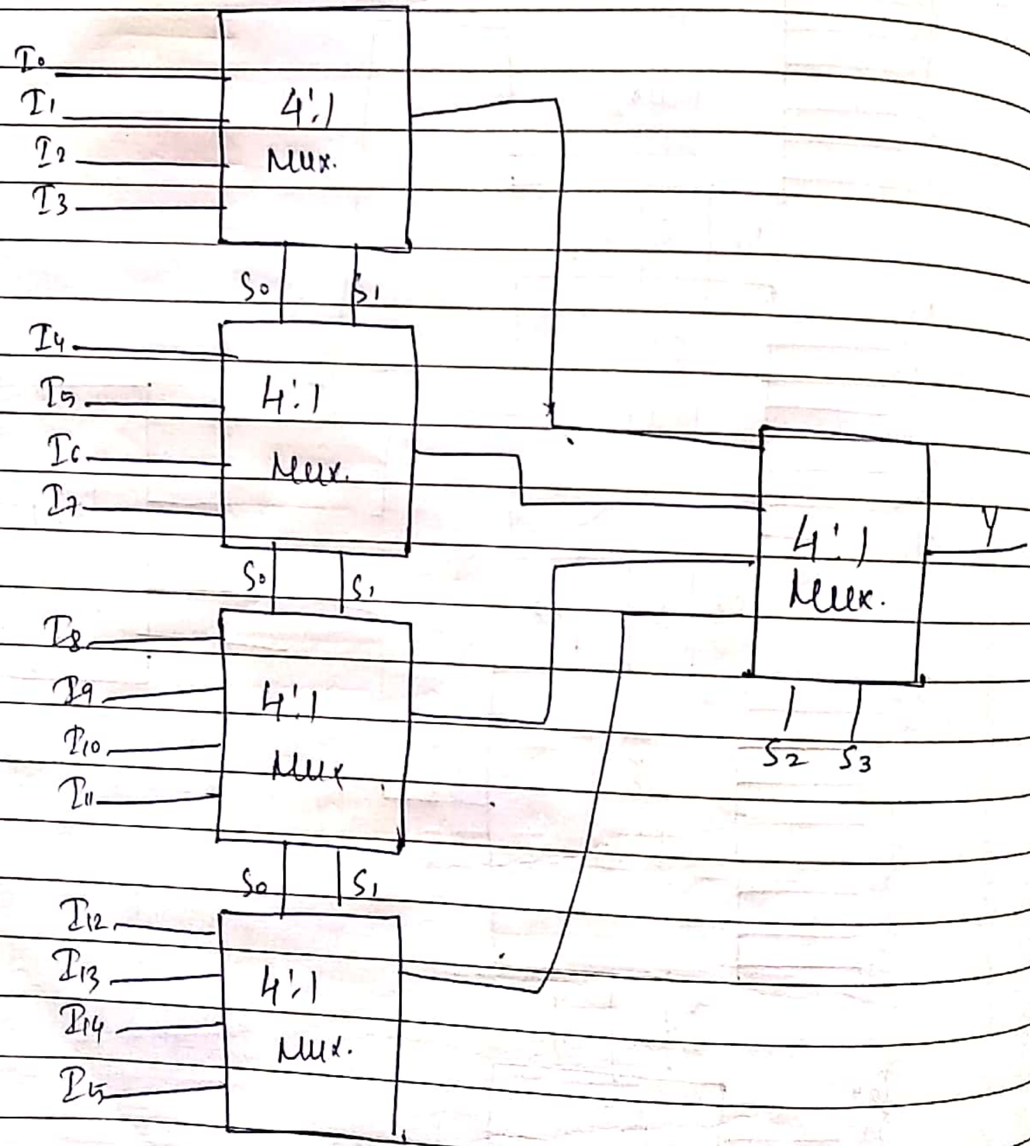
Number of I/P = 8.

Require Number of 8:1 Mux $= \frac{32}{8} = 4$.



⇒ Implement 16:1 Mux using 4:1 Mux.

In 16:1 Mux
No. of I/p = 16.
In 4:1 Mux.
No. of I/p = 4.
Number of 4 Mux = $\frac{16}{4}$ = 4.



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Q) Implement following expression using Mux

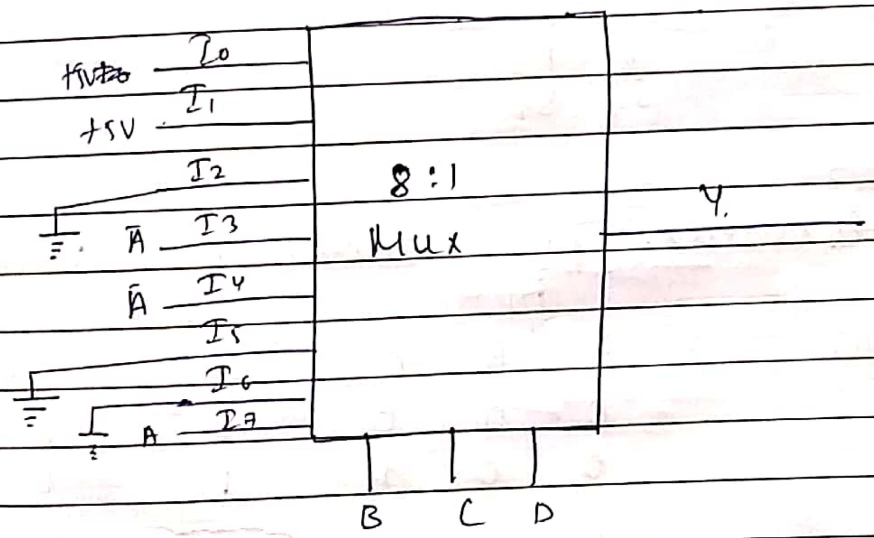
$f(A,B,C,D) = \Sigma m(0,1,3,4,8,9,15)$

Sol If min term greater than 7, we use 8:1 mux.

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
	1	1	0	$\bar{A}$	$\bar{A}$	0	0	A

Note

$\left.\begin{matrix}\bar{A} & 0 \\ A & 0\end{matrix}\right\} \rightarrow 1$, $\left.\begin{matrix}\bar{A} & 0 \\ A & 1\end{matrix}\right\} \rightarrow \bar{A}$, $\left.\begin{matrix}\bar{A} & 1 \\ A & 1\end{matrix}\right\} \rightarrow 0$



Q. Implement following logical expression.

i) $Y = A\bar{B}\bar{C} + \bar{A}BC + AB\bar{C} + ABC.$

Solu $y = A\bar{B}\bar{C} + \bar{A}BC + AB\bar{C} + ABC$

following expression in SOP form :- $\boxed{\text{min term}}$

$A\bar{B}C = 101 = 5$

$\bar{A}BC = 011 = 3$

$AB\bar{C} = 110 = 6.$

$ABC = 111 = 7.$

Value	Mux used
≥ 3	2:1
≥ 7	4:1
≥ 15	8:1

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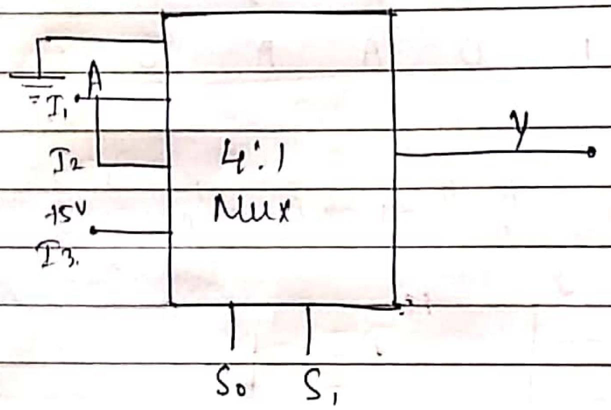
$\overrightarrow{}$ selection lines

$y(A, \overline{B, C}) = \Sigma m(3, 5, 6, 7)$

maximum value is 7 so we use 4:1 mux

	I_0	I_1	I_2	I_3
$\bar{A}$	0	1	2	3
A	4	5	6	7
	0	A	A	1



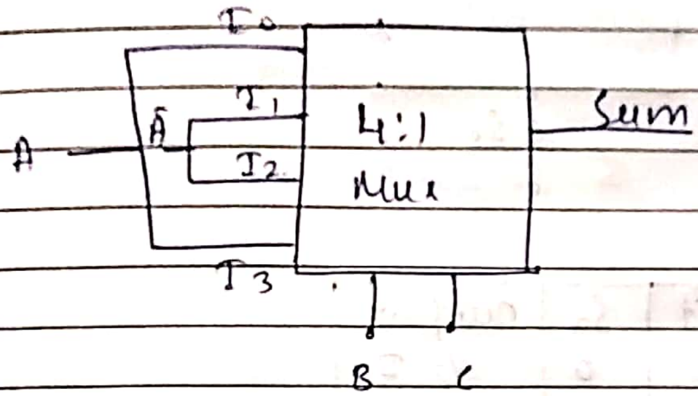
Q.3 implement full adder using mux.

Digit	A (i/p)	B	C	Sum (o/p)	Carry
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1

Value (min term) is less than 7 so we use 4:1 mux.

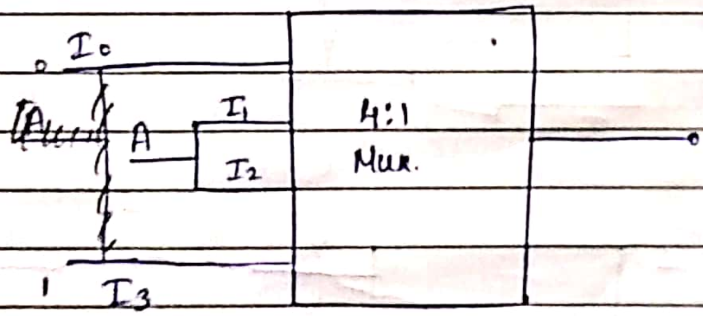
$Sum = \Sigma m(1, 2, 4, 7)$

	I_0	I_1	I_2	I_3
$\bar{A}$	0	1	2	3
A	4	5	6	7
	A	$\bar{A}$	$\bar{A}$	A



Carry = $\Sigma m(3, 5, 6, 7)$

	I_0	I_1	I_2	I_3
$\bar{A}$	0	1	2	3
A	4	5	6	7
	0	A	A	1



Demultiplexer :- Demultiplexer is a combinational circuit which contain single input, n- selection lines and 2^n output lines.

i) 1:2 Demux.

No. of input line = 1
No. of o/p line = $2^1 = 2$
No. of Selection line = 1

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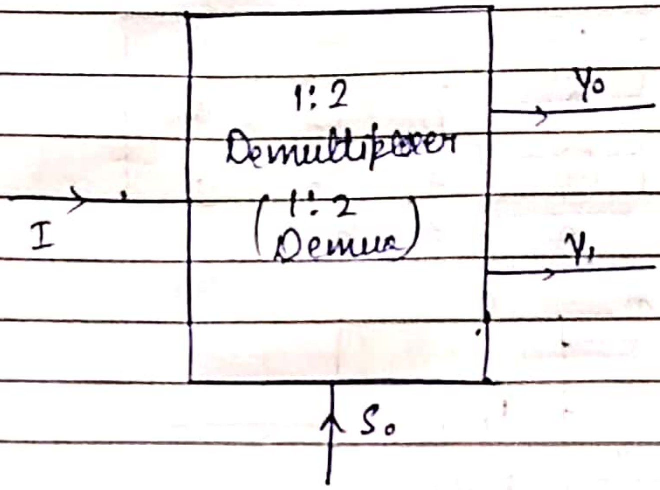


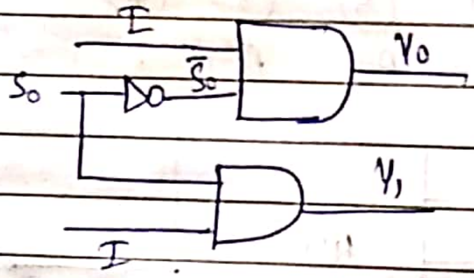
Truth table

Digit	S_0	output
0	0	$Y_0 = I$
1	1	$Y_1 = I$

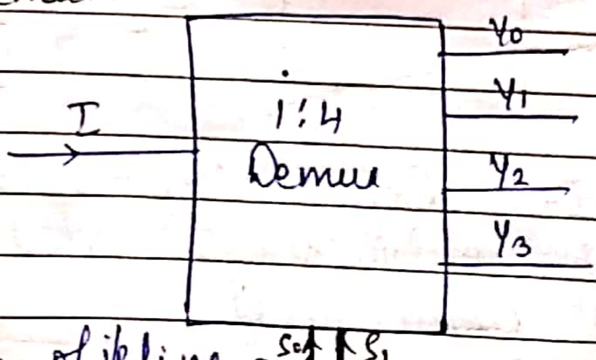
logical expression

$$Y_0 = I\bar{S_0}$$
$$Y_1 = IS_0$$

ckt dig :-



(ii) 1:4 Demux.



No. of i/p line = 1

No. of o/p lines = $2^2 = 4$

No. of selection line = 2

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Truth Table.

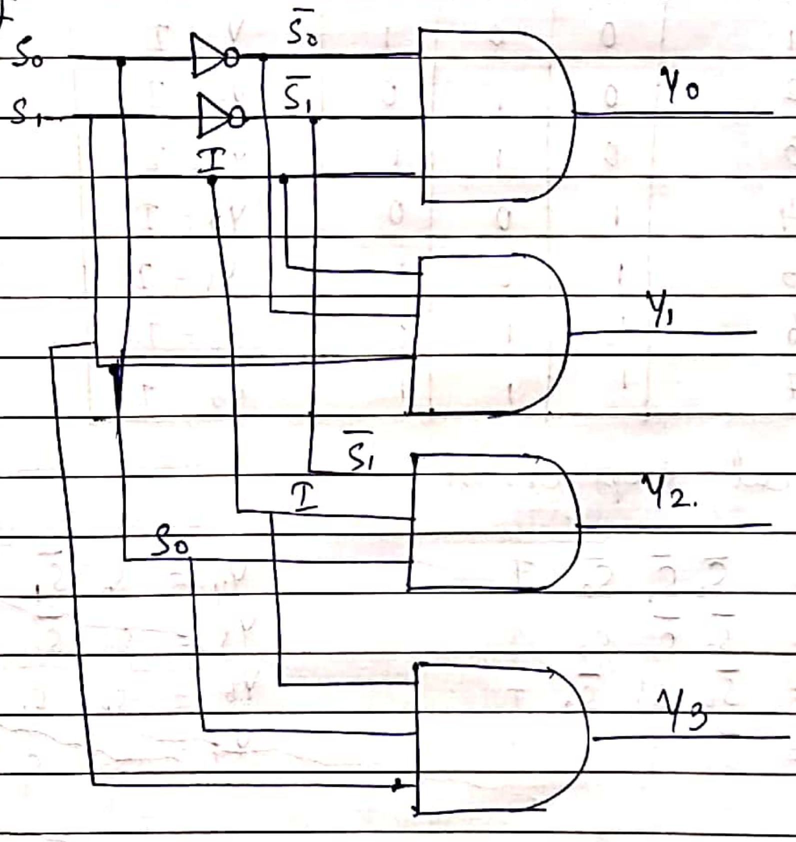
Digit	S_0	S_1	output.
0	0	0	$Y_0 = I$
1	0	1	$Y_1 = I$
2	1	0	$Y_2 = I$
3	1	1	$Y_3 = I$

logical expression

$Y_0 = \bar{S}_0 \bar{S}_1 I$ $\qquad$ $Y_2 = S_0 \bar{S}_1 I$

$Y_1 = \bar{S}_0 S_1 I$ $\qquad$ $Y_3 = S_0 S_1 I$

Ckt dig

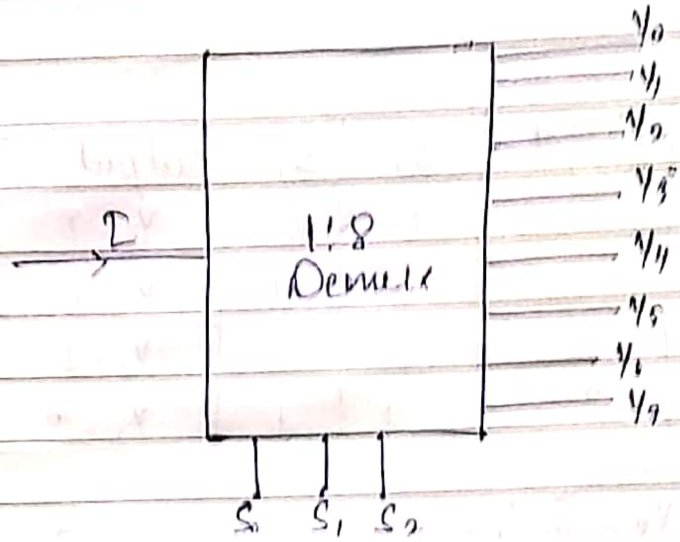


(iii) 1 : 8 Demux.

No. of i/p lines = 1

No. of o/p lines = $2^3 = 8$

No. of Selection line. = 3



Digit	S_0	S_1	S_2	Y
0	0	0	0	$Y_0 = I$
1	0	0	1	$Y_1 = I$
2	0	1	0	$Y_2 = I$
3	0	1	1	$Y_3 = I$
4	1	0	0	$Y_4 = I$
5	1	0	1	$Y_5 = I$
6	1	1	0	$Y_6 = I$
7	1	1	1	$Y_7 = I$

Logical expression:

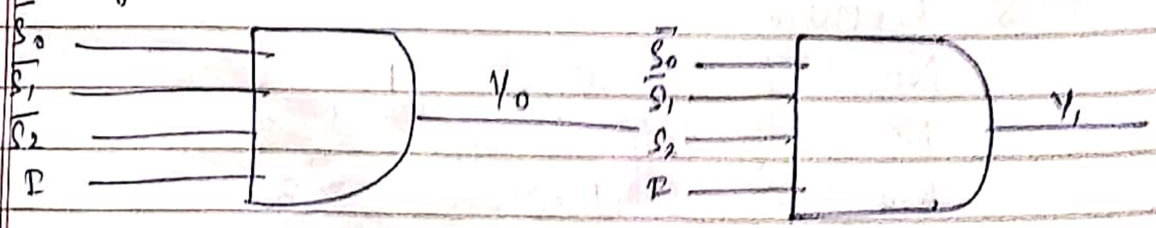
$Y_0 = \bar{S}_0 \bar{S}_1 \bar{S}_2 I$ $\qquad$ $Y_4 = S_0 \bar{S}_1 \bar{S}_2 I$

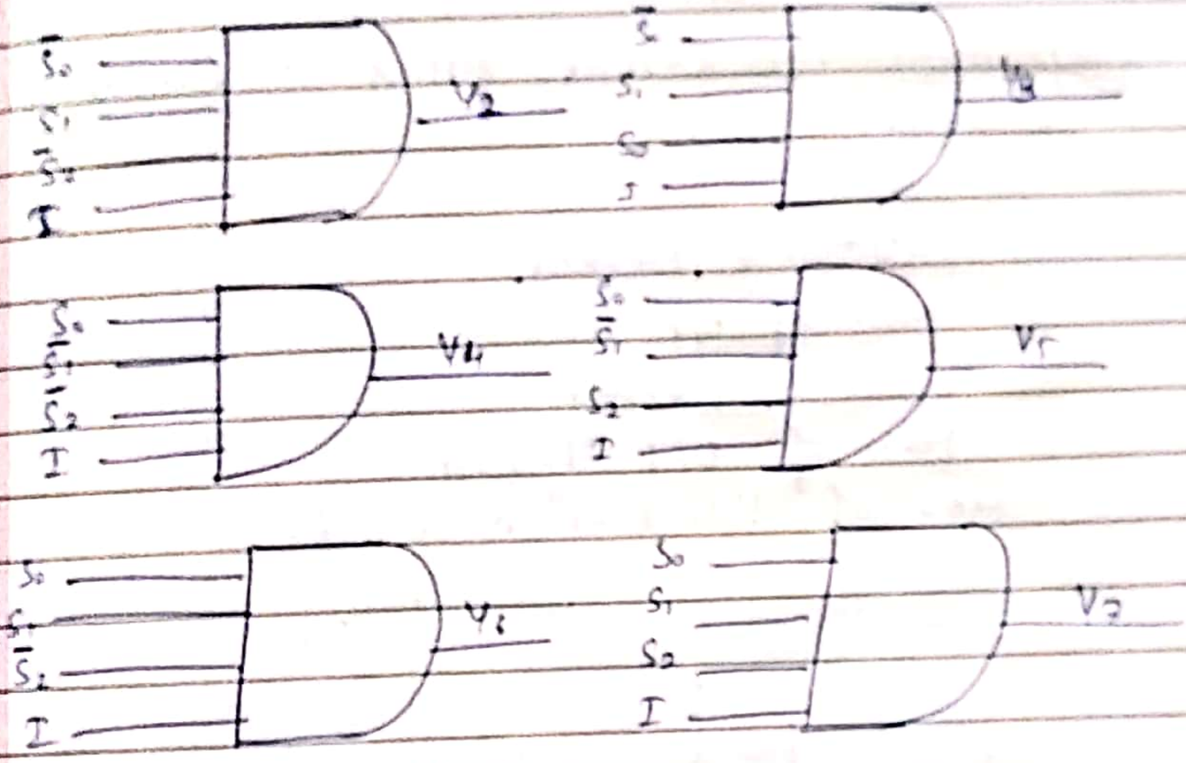
$Y_1 = \bar{S}_0 \bar{S}_1 S_2 I$ $\qquad$ $Y_5 = S_0 \bar{S}_1 S_2 I$

$Y_2 = \bar{S}_0 S_1 \bar{S}_2 I$ $\qquad$ $Y_6 = S_0 S_1 \bar{S}_2 I$

$Y_3 = \bar{S}_0 S_1 S_2 I$ $\qquad$ $Y_7 = S_0 S_1 S_2 I$

Logical ckt:





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Q.1 Implement 1:4 Demux using 1:2 Demux.

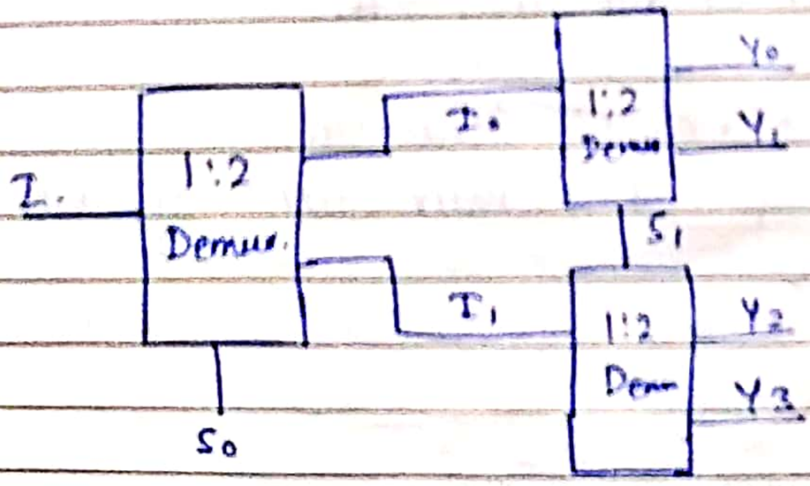
Soln In 1:4 Demux.

⇒ No. of O/P line = 4

In 1:2 Demux.

No. of o/p line = 2.

Number of Demux used = $\frac{4}{2}$ = 2



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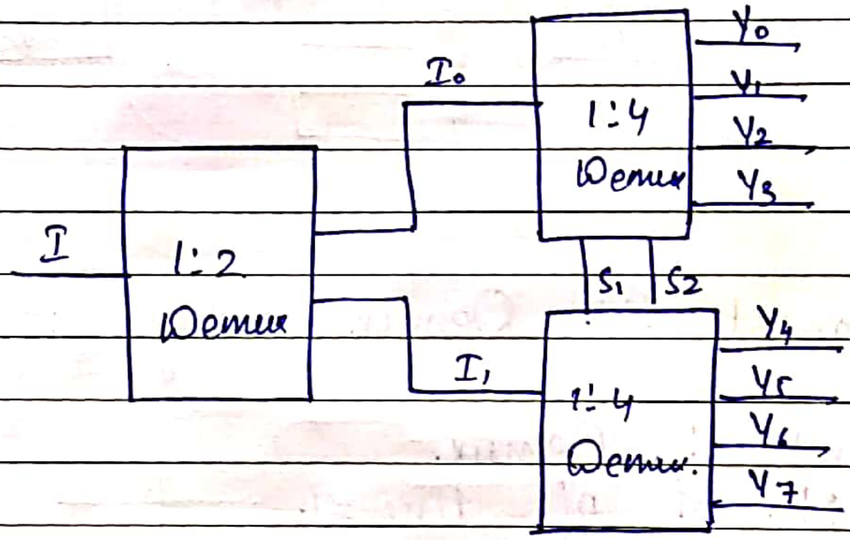
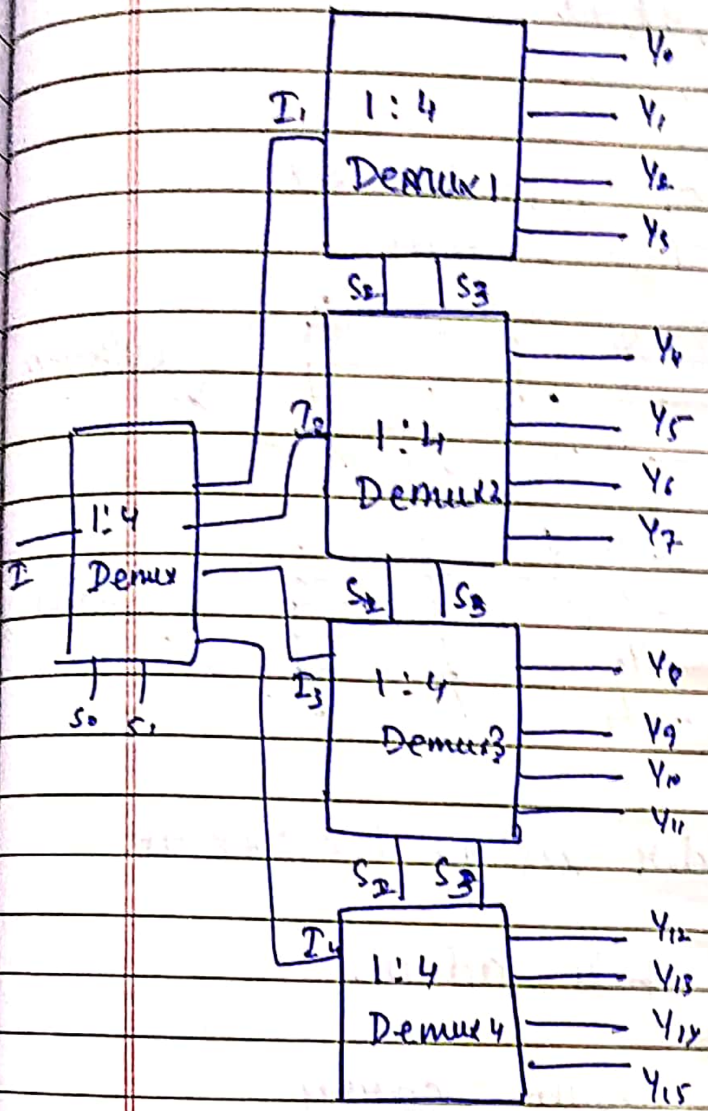
Q.2 Implement 1:8 Demux using 1:4 Demux & 1:2 Demux.

Sol: In ~~:~~ 1:8 Demux.
No. of o/p line = 8.
In 1:4 Demux.
No. of o/p line = 4.
No. of 1:4 Demux used = $\frac{8}{4} = 2$



(3). Implement 1:16 Demux using 1:4 Demux.

Sol: In 1:16 Demux.
No. of o/p line = 16.
In 1:4 Demux.
No. of o/p line = 4.
No. of 1:4 Demux use = $\frac{16}{4} = 4$



Q.4 Implement full subtractor using 1:8 Demux.

Soln:

Truth table For Full subtractor

Digit	A	B	C	Difference	Borrow
0	0	0	0	0	0
1	0	0	1	1	1
2	0	1	0	1	1
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	0
6	1	1	0	0	0
7	1	1	1	1	1

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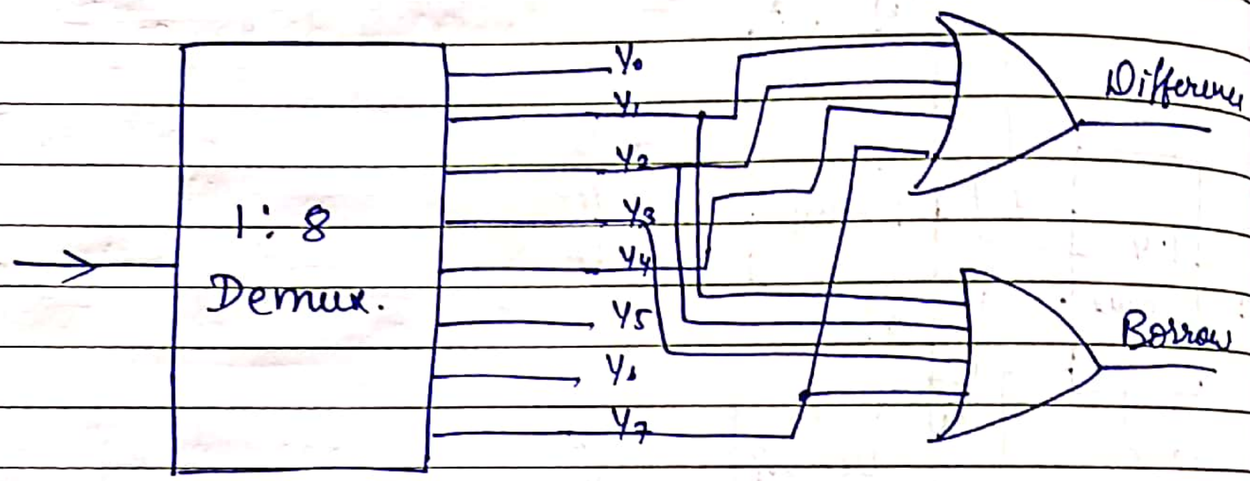
Difference $= \Sigma m(1, 2, 4, 7)$.
Borrow $= \Sigma m(1, 2, 3, 7)$

Maximum value of min term = 7
So we used 1:8 Demux.



Q.2 Implement full adder using 1:8 Demux.

Solⁿ: Truth table of full adder.

Digit	A	B	C	Sum	carry
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1

Sum $= \Sigma m(1, 2, 4, 7)$
Carry $= \Sigma m(3, 5, 6, 7)$.

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Code convertor:-

Binary to grey code convertor.

$\boxed{Ex\text{-}01}$

$0 \oplus 0 = 0$
$0 \oplus 1 = 1$
$1 \oplus 0 = 1$
$1 \oplus 1 = 0$

	Input				Output			
Digit	B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	~~0~~1	0
13	1	1	0	1	1	0	~~0~~1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

K Map for G_3

B_3B_2 \ B_1B_0	00	01	011	10
00	0 0	0 1	0 3	0 2
01	0 4	0 5	0 7	0 6
101	1 12	1 13	1 15	1 14
10	1 8	1 9	1 11	1 10

$G_3 = B_3$

K Map for G_2.

$B_3B_2 \backslash B_1B_0$	00	01	11	10
00	0_{0}	0_{1}	0_{3}	0_{2}
01	1_{4}	1_{5}	1_{7}	1_{6}
11	0_{12}	0_{13}	0_{15}	0_{14}
10	1_{8}	1_{9}	1_{11}	1_{10}

$\rightarrow \overline{B_3}B_2$

$\rightarrow B_3\overline{B_2}$

$$G_2 = \overline{B_3}B_2 + B_3\overline{B_2}$$
$$= B_3 \text{ exor } B_2.$$

K Map for G_1

$B_3,B_2 \backslash B_1,B_0$	00	01	11	10
00	0_{0}	0_{1}	1_{3}	1_{2}
01	1_{4}	1_{5}	0_{7}	0_{6}
11	1_{12}	1_{13}	0_{15}	0_{14}
10	0_{8}	0_{9}	1_{11}	1_{10}

$B_2\overline{B_1} \rightarrow$

$\rightarrow \overline{B_2}B_1$

$$G_1 = \overline{B_2}B_1 + B_2\overline{B_1}$$
$$G_1 = B_2 \text{ exor } B_1$$

K Map for G_0

$B_3,B_2 \backslash B_1,B_0$	00	01	11	10
00	0_{0}	1_{1}	0_{3}	1_{2}
01	0_{4}	1_{5}	0_{7}	1_{6}
11	0_{12}	1_{13}	0_{15}	1_{14}
10	0_{8}	1_{9}	0_{11}	1_{10}

$\rightarrow \overline{B_1}B_0$

$\rightarrow B_1\overline{B_0}$

$$G_0 = \overline{B_1}B_0 + B_1\overline{B_0}$$
$$G_0 = B_1 \text{ exor } B_0$$

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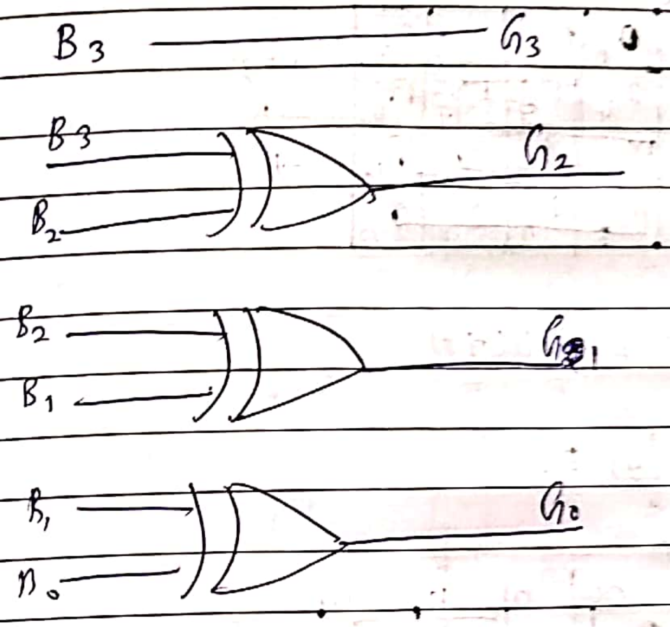
Logical circuit For Binary to Grey code converter.



(ii) BCD to Excess 3 Code converter.

Digit	Input				Output			
	A	B	C	D	E3	E2	E1	E0
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0
10	1	0	1	0	X	X	X	X
11	1	0	1	1	X	X	X	X
12	1	1	0	0	X	X	X	X
13	1	1	0	1	X	X	X	X
14	1	1	1	0	X	X	X	X
15	1	1	1	1	X	X	X	X

(i) K Map for F_3

AB \ CD	00	01	11	10
00	0 (0)	0 (1)	0 (3)	0 (2)
01	0 (4)	1 (5)	1 (7)	1 (6)
11	X (12)	X (13)	X (15)	X (14)
10	1 (8)	1 (9)	X (11)	X (10)

→ BD
→ BC
→ A

$$F_3 = BD + BC + A.$$

(ii) K Map for E_2

AB \ CD	00	01	11	10
00	0 (0)	1 (1)	1 (3)	1 (2)
01	1 (4)	0 (5)	0 (7)	0 (6)
11	X (12)	X (13)	X (15)	X (14)
10	0 (8)	1 (9)	X (11)	X (10)

→ $\bar{A}\bar{B}C$
$B\bar{C}\bar{D}$ →
→ AD
→ $\bar{B}D$

$$E_2 = AD + \bar{B}D + \bar{A}\bar{B}C + B\bar{C}\bar{D}$$

K Map for E_1

→ $\bar{C}\bar{D}$
→ CD

AB \ CD	00	01	11	10
00	1 (0)	0 (1)	1 (3)	0 (2)
01	1 (4)	0 (5)	1 (7)	0 (6)
11	X (12)	X (13)	X (15)	X (14)
10	1 (8)	0 (9)	X (11)	X (10)

$E_1 = \bar{C}\bar{D} + CD$
$= C \text{ exnor } D$

K Map for E_0

AB \ CD	00	01	11	10
00	1 (0)	0 (1)	0 (3)	1 (2)
01	1 (4)	0 (5)	0 (7)	1 (6)
11	X (12)	X (13)	X (15)	X (14)
10	1 (8)	0 (9)	X (11)	X (10)

$E_0 = \bar{D}$

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