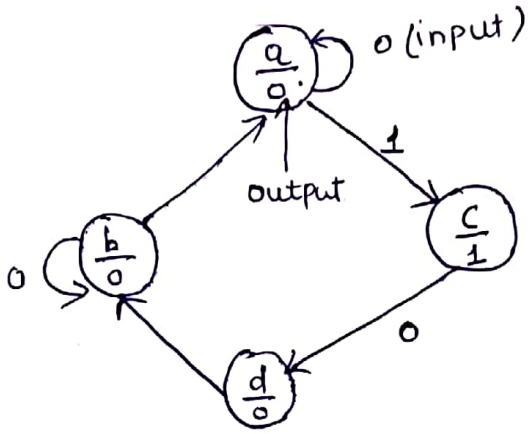
FSM

Model for synchronous sequential circuit
There are two types of schronous sequential circuit

a) moore circuit
b) melay circuit

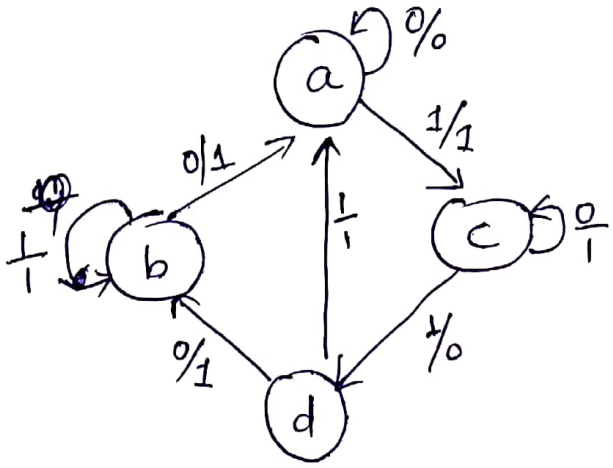
a) moore circuit :→ The syn. seq. ckT is called moore ckT. if the output depends only on the present state of flip-flop.

State diagram for moore ckT



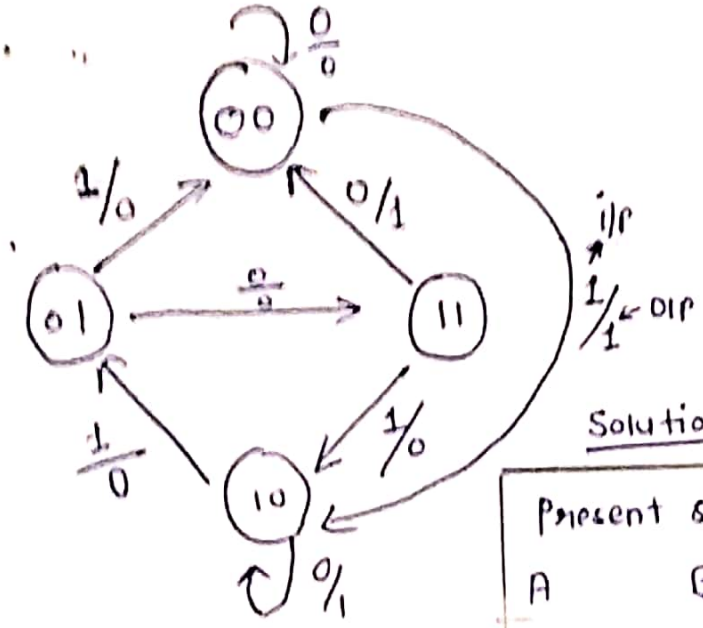
a, b, c, d = present state

b) melay circuit :→
if the output of the syn. sequential Circuit depends on the present state of flip flop & the input of the present state then it is called melay circuit.



a, b, c, d states of melay machine

Q.1 Design a sequential circuit has one i/p & one o/p. The state diagram is shown in figure. Design sequential melay circuit using JK flip-flop. The state diagram is shown in figure.



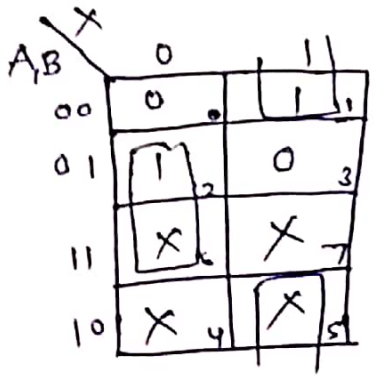
Solution

Present state A	B	Next state x=0 A+1	B+1	x=1 A+1	B+1	output x=0 Y	x=1 Y
0	0	0	0	1	0	0	1
0	1	1	1	0	0	0	0
1	0	1	0	0	1	1	0
1	1	0	0	1	0	1	0

Excitation table for J-K flip-flop

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

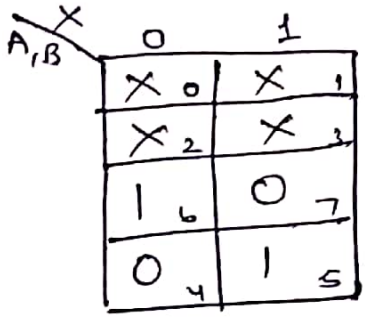
① K-map for J_A



$J_A = B\bar{X} + \bar{B}X$

$B \oplus X$

② K-map for K_A

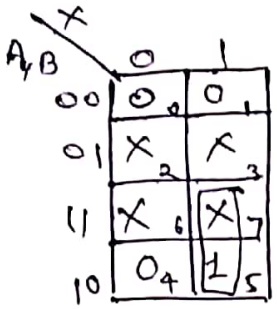


$K_A = B\bar{X} + \bar{B}X$

$B \oplus X$

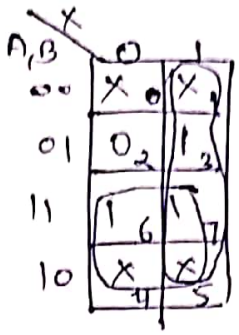
Digit	Present state		i/p	Next state		flip-flop i/p				o/p
	A	B	X	A_{+1}	B_{+1}	J_A	K_A	J_B	K_B	Y
0	0	0	0	0	0	0	X	0	X	0
1	0	0	1	1	0	1	X	0	X	1
2	0	1	0	1	1	1	X	X	0	0
3	0	1	1	0	0	0	X	X	1	0
4	1	0	0	1	0	X	0	0	X	1
5	1	0	1	0	1	X	1	1	X	0
6	1	1	0	0	0	X	1	X	1	1
7	1	1	1	1	0	X	0	X	1	0

(3) K-map for J_B



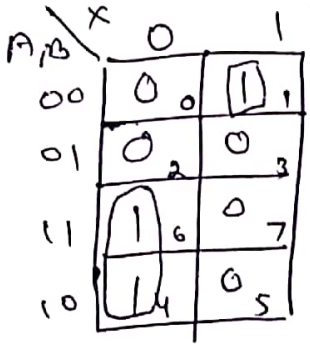
$J_B = AX$

(4) K-map for K_B



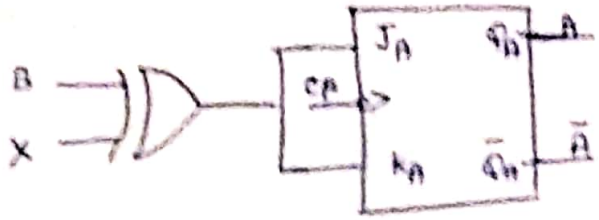
$K_B = X + A$

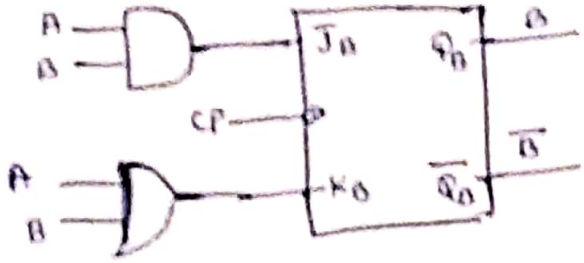
(5) K-map for y

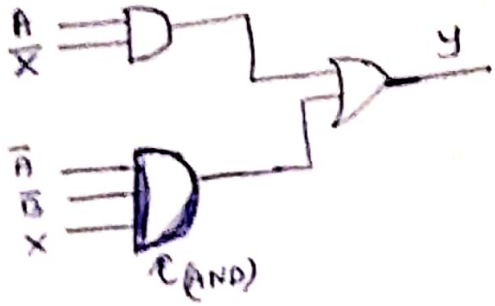


$Y = A\bar{X} + \bar{A}\bar{B}X$

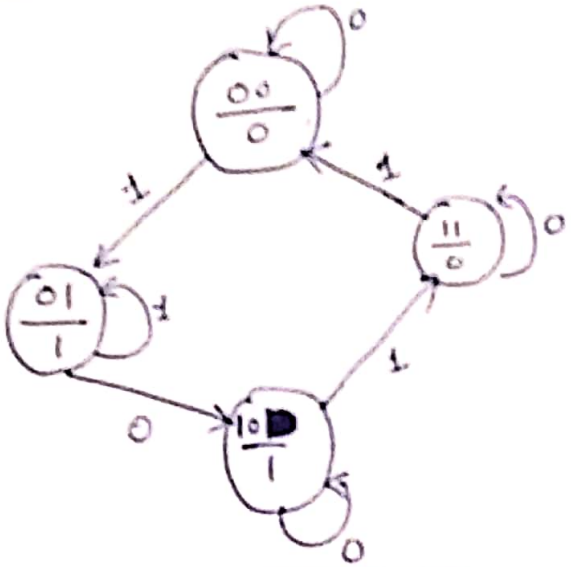
(1) K-maps







moore machine :→



obtain the state table and design the ~~cir~~ circuit using minimum number of JK-flip-flop

Present state		Next state				output
A	B	x=0		x=1		Y
		A_{t+1}	B_{t+1}	A_{t+1}	B_{t+1}	
0	0	0	0	0	1	0
0	1	1	0	0	1	1
1	0	1	0	1	1	1
1	1	1	1	0	0	0

excitation table for JK flip-flop			
Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

(1) K-maps

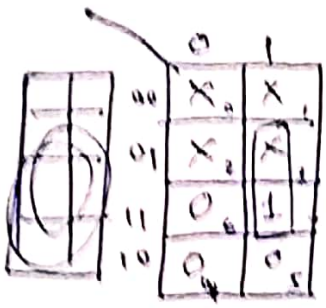
J_A

$J_A = AX$

J_B

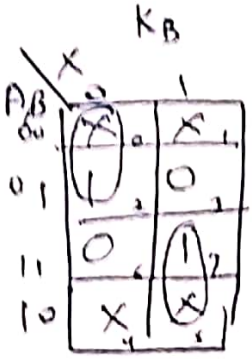
$J_B = X$

K_A



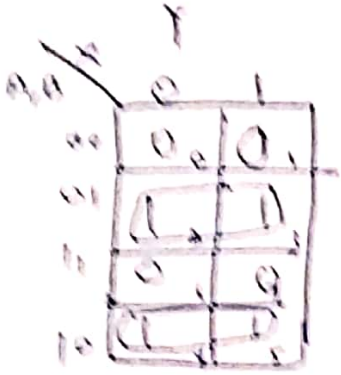
$K_A = BX$

K_B



$K_B = \bar{A}\bar{X} + AX$

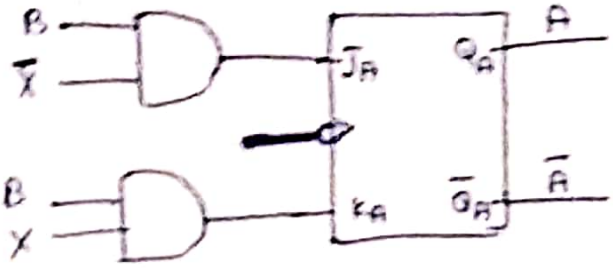
Y

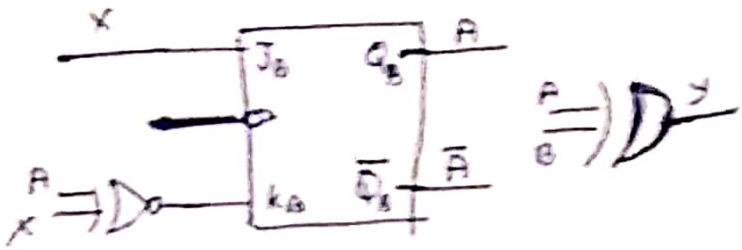


$Y = A\bar{B} + \bar{A}B$

$Y = A \oplus B$

Clock	Present state		I/P	Next state		JK flip-flop i/p				O/P
	A	B	X	A_{t+1}	B_{t+1}	J_A	K_A	J_B	K_B	Y
0	0	0	0	0	0	0	X	0	X	0
1	0	0	1	0	1	0	X	1	X	0
2	0	1	0	1	0	1	X	X	1	1
3	0	1	1	0	1	0	X	X	0	1
4	1	0	0	1	0	X	0	0	X	1
5	1	0	1	1	1	X	0	1	X	1
6	1	1	0	1	1	X	0	X	0	0
7	1	1	1	0	0	X	1	X	1	0

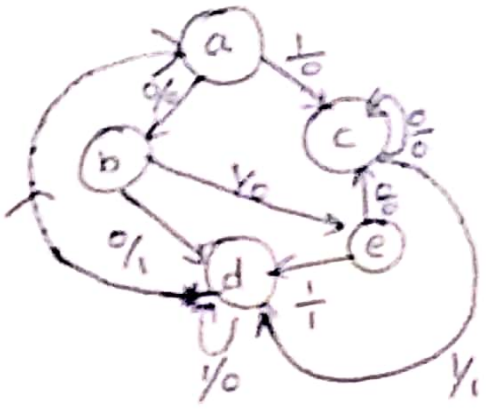




State Reduction

FSM of melay machine

Step-1 → State table for state diagram



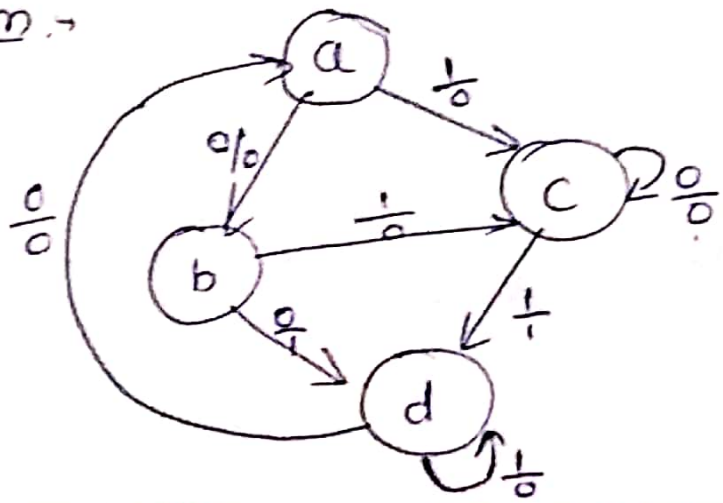
Ques →

Present state	Next state x=0	Next state x=1	Output x=0	Output x=1
a	b	c	0	0
b	d	e	1	0
c	c	d	0	1
d	a	d	0	0
e	c	d	0	1

Step-2 : Reduced state

Present state	Next state x=0	Next state x=1	Output x=0	Output x=1
a	b	c	0	0
b	d	c	1	0
c	c	d	0	1
d	a	d	0	0

Reduced state diagram →



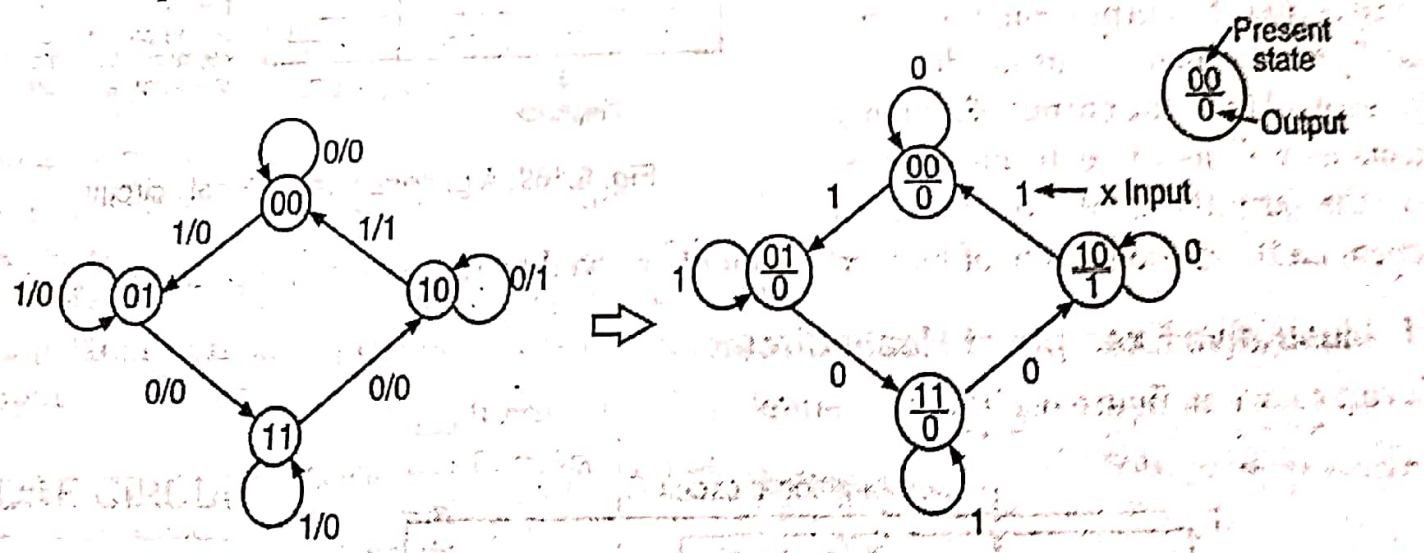
6.40.2 Performance Comparison of Moore and Mealy Models

Table 6.61. Performance Comparison of Moore and Mealy models

S. No.	Moore model	Mealy model
1.	The final output depends only on the present state of memory elements.	The final output depends on the present state of memory elements and the external inputs.
2.	The output changes only after the active clock edge.	Output can change in between the clock edges if the external inputs change.
3.	The implementation of a logic function needs more number of states than Mealy circuit.	Implementation of the same logic function requires less number of states than Moore circuit.

State Diagram of a Moore Circuit

The state diagram of a Moore circuit is slightly modified than the basic state diagram as shown in figure 6.171. The labelling of the directed line now contains only one binary number corresponding to x in which causes the state transition. The output state is now indicated inside the circle. This is because the output Y depends only the present state and independent on input x.



(a) Original state diagram

(b) Modified state diagram for a Moore circuit

Fig. 6.171.