Course Code	Course Name	Theory	Practical	Tutorial	Theory	Oral & Practical	Tutorial	Total
ITC404	Computer Organization and Architecture	04	--	--	04	--	--	04

Course Code	Course Name	Examination Scheme						
		Theory Marks				Term Work	Oral & Practical	Total
		Internal assessment			End Sem. Exam			
		Test1	Test 2	Avg. of two Tests				
ITC404	Computer Organization and Architecture	20	20	20	80	--	--	100

Course Objectives: Students will try to:

1. Conceptualize the basics of organizational and architectural issues of a digital computer.
2. Analyze processor performance improvement using instruction level parallelism.
3. Learn the function of each element of a memory hierarchy.
4. Study various data transfer techniques in digital computer.
5. Articulate design issues in the development of processor or other components that satisfy design requirements and objectives.
6. Learn microprocessor architecture and study assembly language programming.

Course Outcomes: Students will be able to:

1. Describe basic organization of computer and the architecture of 8086 microprocessor.
2. Implement assembly language program for given task for 8086 microprocessor.
3. Demonstrate control unit operations and conceptualize instruction level parallelism.
4. Demonstrate and perform computer arithmetic operations on integer and real numbers.
5. Categorize memory organization and explain the function of each element of a memory hierarchy.
6. Identify and compare different methods for computer I/O mechanisms.

Prerequisite: Fundamentals of Computer, Digital Logic Design

Detailed syllabus:

Sr. No.	Module	Detailed Content	Hours	CO Mapping
0	Prerequisite	basic combinational and sequential logic circuits, binary numbers and arithmetic, basic computer organizations	02	
I	Overview of Computer Architecture &	Introduction of Computer Organization and Architecture. Basic organization of computer and block level description of the functional	07	CO1

	Organization	units. Evolution of Computers, Von Neumann model. Performance measure of Computer Architecture. Architecture of 8086 family, 8086 Hardware Design, Minimum mode & Maximum mode of Operation. Study of bus controller 8288 & its use in Maximum mode.		
II	Programming 8086	Addressing modes, Instruction Set, Assembly Language Programming, Mixed Language Programming, Programs based on Stacks, Strings, Procedures, Macros, Timers, Counters & delay.	10	CO2
III	Processor Organization and Architecture	CPU Architecture, Register Organization, Instruction formats, basic instruction cycle. Instruction interpretation and sequencing. Control Unit: Soft wired (Micro-programmed) and hardwired control unit design methods. Microinstruction sequencing and execution. Micro operations, concepts of nano programming. Introduction to parallel processing concepts, Flynn's classifications, pipeline processing, instruction pipelining, pipeline stages, pipeline hazards.	11	CO3
IV	Data Representation and Arithmetic Algorithms	Number representation: Binary Data representation, two's complement representation and Floating-point representation. Integer Data arithmetic: Addition, Subtraction. Multiplication: Unsigned & Signed multiplication- Add & Shift Method, Booth's algorithm. Division of integers: Restoring and non-restoring division, signed division, basics of floating point representation IEEE 754 floating point(Single & double precision) number representation. Floating point arithmetic: Addition, subtraction	10	CO4
V	Memory Organization	Introduction to Memory and Memory parameters. Classifications of primary and secondary memories. Types of RAM and ROM, Allocation policies, Memory hierarchy and characteristics. Cache memory: Concept, architecture (L1, L2, L3), mapping techniques. Cache Coherency, Interleaved and Associative memory.	07	CO5
VI	I/O Organization	Input/output systems, I/O modules and 8089 IO processor. Types of data transfer techniques: Programmed I/O, Interrupt driven I/O and DMA.	05	CO6

Text Books:

1. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, “Computer Organization”, Fifth Edition, Tata McGraw-Hill.
2. William Stallings, “Computer Organization and Architecture: Designing for Performance”, Eighth Edition, Pearson.
3. 8086/8088 family: Design Programming and Interfacing: By John Uffenbeck (Pearson Education)
4. Microprocessor and Interfacing: By Douglas Hall (TMH Publication).

References:

1. B. Govindarajulu, “Computer Architecture and Organization: Design Principles and Applications”, Second Edition, Tata McGraw-Hill.
2. Dr. M. Usha, T. S. Srikanth, “Computer System Architecture and Organization”, First Edition, Wiley-India.
3. John P. Hayes, “Computer Architecture and Organization”, McGraw-Hill.,Third Edition.
4. K Bhurchandi, “Advanced Microprocessors & Peripherals”, Tata McGraw-Hill Education

Assessment:

Internal Assessment for 20 marks:
Consisting of **Two Compulsory Class Tests**
Approximately 40% to 50% of syllabus content must be covered in First test and remaining 40% to 50% of syllabus contents must be covered in second test.

End Semester Examination: Some guidelines for setting the question papers are as:

- Weightage of each module in end semester examination is expected to be/will be proportional to number of respective lecture hours mentioned in the syllabus.
- Question paper will comprise of total **six questions**, **each carrying 20 marks.**
- **Q.1** will be **compulsory** and should **cover maximum contents of the syllabus**.
- **Remaining question will be mixed in nature** (for example if Q.2 has part (a) from module 3 then part (b) will be from any other module. (Randomly selected from all the modules.)
- Total **four questions** need to be solved.