29/5/2014 (Comp & IT)

COA Sem-IV (SE comp)

QP Code :NP-19761 IT

(3 Hours) [Total Marks :80

N.B.:— (1) Question no.1 is **compulsory.**
(2) Solve any **three** questions out of remaining **five** questions.
(3) Assume suitable data if **necessary.**
(4) Answer to **each** new question to be started on a **fresh page.**

1. (a) What is stored program concept? 3
   (b) Show IEEE 754 Standards for Binary Floating-Point Representation for 32 bit single format and 64 bit double format. 3
   (c) What are applications of Microprogramming? 3
   (d) What is Virtual Memory? 4
   (e) Explain in brief function of 8089 I/O Processor. 4
   (f) Name the Flynn's Classification of Parallel Processing Systems. 3

2. (a) Draw the flow chart for Booth's Algorithm for Twos Complement Multiplication. 5
   (b) Using Booth's Algorithm show the multiplication of 7×5. 7
   (c) Explain with diagram functioning of Microprogrammed Control Unit. 8

3. (a) What are the differences between RISC and CISC processors? 5
   (b) Describe hardwired control unit and specify its advantages. 7
   (c) What are characteristics of memory devices? 8

4. (a) Explain in details Memory Hierarchy with examples. 6
   (b) What are elements of cache design? Explain in details. 8
   (c) What are major requirements for an I/O module? 6

5. (a) Explain the DMA based data transfer techniques for I/O devices. 8
   (b) Explain concepts of nanoprogramming. 6
   (c) What is instruction pipelining? 6

6. Write short notes on:
   (a) Touch Pad 7
   (b) L1, L2 and L3 Cache memory. 7
   (c) Programmed I/O 6

Con. 12218-14.

S.E. I T (IV)(CBGS) 10/12/15

COA

Q.P. Code : **5461**

(3 Hours) [Total Marks :80

N.B. : (1) Question **No.1** is **compulsory**
(2) Solve any **three** questions out of remaining **five** questions.
(3) Assume suitable data if necessary.

1. Solve any **four** out of **five.** 20
   (a) Differentiate between RISC and CISC
   (b) What are the functions of following registers?
      (i) PC (ii) SP (iii) MAR (iv) MDR (v) IR
   (c) Write a note on interrupt execution.
   (d) Define Stored Program Concept and draw Von-Neumann's architecture.
   (e) What is meant by nanoprogramming?

2. (a) Multiply (-3) and (4) using Booth's Algorithm. 10
   (b) Explain 6 stage instruction pipeline with suitable diagram. 10

3. (a) Compare SRAM & DRAM.
   (b) Consider the string 1,3,2,4,2,1,5,1,3,2,6,7,5,4,3,2,4,2,3,1,4 10
   Find the page faults for 3 frames using FIFO and LRU page replacement algorithms. 10

4. (a) Divide 11 by 2 using restoring division algorithm. 10
   (b) What is meant by Fetch cycle, Instruction cycle, Machine cycle and interrupt cycle? Explain in brief. 10

5. (a) Explain different mapping techniques of Cache memory. 10
   (b) What is virtual memory? Explain the role of paging and segmentation in virtual memory. 10

6. (a) Explain different addressing modes with example. 10
   (b) What is the need of DMA? Explain its various techniques of data transfer. 10

COMP
T.E. Sem IV (CBGS) 3/12/14.
COA

QP Code :12476

(3 Hours) **[Total Marks : 80**

N.B. (1) Question No. 1 is **compulsory**.
(2) Attempt any **three** questions from remaining **five** questions.
(3) Assume suitable data if **required.**
(4) Draw neat diagram wherever **necessary.**

1. Solve any **four :** **20**
   (a) What are the types of pipeline hazards ?
   (b) Explain in brief memory mapped I/O.
   (c) Explain in detail cache coherence.
   (d) Draw flow chart of Booth's algorithm.
   (e) Define stored program concept and draw Von Neumann's Architecture.

2. (a) Explain in detail different types of addressing modes. **10**
   (b) Multiply $(-2)_{10}$ and $(-5)_{10}$ using Booth's Algorithm. **10**

3. (a) Explain Wilke's Engine (Hardwired Control Unit) in detail. **10**
   (b) Explain virtual memory with reference to memory hierarchy, segments and pages. **10**

4. (a) Explain features of RISC and CISC processors. **10**
   (b) Explain six stage instruction pipeline with suitable diagram. **10**

5. (a) Explain various high speed memories such as interleaved memories and caches. **10**
   (b) Explain LRU page replacement policy with suitable example. **10**

6. (a) What is Bus Arbitration ? Explain any two techniques of Bus Arbitration. **10**
   (b) Write short note (any two) : **10**
      (i) Nano programming
      (ii) DMA (Direct Memory Access)
      (iii) Plotter.

GN-Con.:9620-14.

S.E. Sem IV (CBGS). (Computers & I.T.)
COA

27/5/15

QP Code : 3546

(3 Hours) Total Marks: 80

N.B.:- (1) **Question no.1 is compulsory.**
(2) Solve any **three** questions out of remaining **five** questions.
(3) Assume suitable data if necessary.

1.	(a) What are applications of Microprogramming?	3
	(b) What is stored program concept in digital computer?	3
	(c) List the Flynn's Classification of Parallel Processing Systems.	3
	(d) Draw flowchart for Booth's Algorithm for Twos Complement Multiplication.	3
	(e) What is Associative memory?	4
	(f) Explain in brief Programmed I/O.	4
2.	(a) Explain with diagram functioning of Hardwired Control Unit.	8
	(b) Using Unsigned Binary Division method, divide 7 by 3.	6
	(c) Explain IEEE 754 standards for Floating Point number representation.	6
3.	(a) Describe what are the features of cache design?	8
	(b) What are the differences between RISC and CISC processors?	6
	(c) Explain concepts of Nano programming.	6
4.	(a) What are major requirements for an I/O module?	6
	(b) Explain in details Virtual Memory, Segmentation and Paging.	7
	(c) Explain in details Cache Coherency.	7
5.	(a) What is instruction pipelining? What are advantages of pipelining?	6
	(b) Explain DMA based data transfer technique for I/O devices.	7
	(c) Explain Microinstruction sequencing and execution.	7
6.	Write short note on:	
	(a) Pipeline Hazards.	7
	(b) Scanner.	7
	(c) Interrupt driven I/O.	6

JP-Con. 10819-15.

Q.P. Code :23710

[Time: Three Hours] **[Marks:8**

Please check whether you have got the right question paper.

N.B:
1. Question.No.1 is compulsory.
2. Solve any **three** questions out of remaining five questions.
3. Assume suitable data if necessary
4. Figures to right indicate marks

Q. 1 Attempt **any 4** sub questions.

a) Define the terms Computer Organization and Computer Architecture. (05
b) Draw and explain single and double precision IEEE 754 binary floating point representation formats. (05
c) List and Explain important parameters significant in choosing a computer memory. (05
d) Draw and explain five stage instruction pipelining. (05
e) Explain Programmed I/O technique of Data transfer. (05

Q. 2 a) Calculate the number of page hits and faults using FIFO, LRU and OPTIMAL page replacement algorithms for the following page frame Sequence: 5,6, 6, 3, 8, 5, 7, 8, 6, 5, 8, 5. (FRAME SIZE = 3). (10
b) Draw and explain basic instruction execution cycle. (10

Q. 3 a) Explain memory hierarchy of a computer. (10
b) Describe Flynn's classification in detail. (10

Q. 4 a) Describe different addressing modes. (10
b) Draw the flowchart of Booths algorithm and multiply (6)*(-4) using Booths algorithm. (10

Q. 5 a) Explain interrupt driven I/O technique of Data transfer. (10
b) Explain hardwired approach to the design of a control unit. (10

Q. 6 Write notes on **(any three)** (20
a) Register Organization of a processor
b) Von Neumann architecture
c) Associative memory
d) Nano Programming
e) Pipeline Hazards

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Q.P. Code : 09892

[Time: Three Hours] **[Marks:80]**

Please check whether you have got the right question paper.

N.B:
1. Question No.1 is compulsory.
2. Attempt any THREE out of the remaining questions.
3. Assume suitable data if necessary.

Q.1 Solve any Four sub questions

a) Draw and explain Memory hierarchy. 05

b) Represent $(12.25)_{10}$ in double precision IEEE 754 binary floating point representation format. 05

c) Draw and explain basic instruction execution cycle. 05

d) What are the types of pipeline hazards? 05

e) What are the major functions of an I/O module? 05

Q.2 a) Explain the functioning of Wilke's Microprogrammed control unit with its advantages. 10

b) Draw the flowchart of Booths algorithm and multiply (4)*(-3) using Booths algorithm. 10

Q.3 a) Differentiate between RISC and CISC in detail with example. 10

b) Draw flowchart of binary Restoring division and use it to divide 16/4. 10

Q.4 a) Calculate the number of page hits and faults using FIFO, LRU and OPTIMAL page replacement algorithms for the following page frame sequence : 2, 3, 1, 2, 4, 3, 2, 5, 3, 6, 7, 9, 3, 7. (FRAME SIZE = 3). 10

b) What is instruction pipelining? Explain with suitable diagram. 10

Q.5 a) What are the elements of a cache design? 10

b) Explain DMA in detail. 10

Q.6 Write detailed notes on (any two) 20

a) Microinstruction formats

b) Programmed I/O

c) Interleaved and Associative memory

d) Evolution of Computers

SE - Sem - IV (CBKS) - I.T. 31/05/16

Computer Organization & Architecture

Q.P. Code : 549802

(3 Hours) **| Total Marks : 80**

N.B. : (1) Question No .1 is **compulsory.**
(2) Solve any **three** questions out of remaining **five** questions.
(3) Assume suitable data if necessary.

1. Solve any **four** out of **five :-** **20**
   (a) Explain the types of microinstruction formats.
   (b) Draw and explain the flowchart of Add and Shift method of integer multiplication.
   (c) What the functions of following registers ?
   (i) Z (ii) SP (iii) MAR (iv) MDR (v) Y
   (d) Compare SRAM and DRAM.
   (e) With the help of diagram, explain Von-Neumann architecture.

2. (a) Multiply (-9) and (4) using Booth's algorithm. **10**
   (b) Explain different addressing modes with example. **10**

3 (a) Express $(28.75)_{10}$ in the IEEE 754 single and double precision standard of floating point representation. **10**
   (b) Explain design of control unit w.r.t. microprogrammed and hardwired approach. **10**

4. a) Explain different mapping techniques of Cache memory. **10**
   b) Explain Flynn's classification in detail. **10**

5 a) Draw and explain six stage instruction pipeline and the various hazards. **10**
   b) What is the need of DMA? Explain its various techniques of data transfer. **10**

6. a) Find out page hit and miss for the following string using FIFO, LRU and OPTIMAL page replacement policies considening a frame size of three. 2, 3, 3, 1, 5, 2, 4, 5, 3, 2, 5, 2. **10**
   b) Divide 15 by 4 using restoring division algorithm. **10**

IT/IV/CBGS/COA/Comp. Organization Architecture

15-12-16

QP Code :549803

MAX MARKS:80 TIME:03 HRS

N.B. 1. Question No 1 is compulsory.

2. Solve any three questions out of remaining five questions.

3. Assume suitable data if necessary.

Q. 1. Solve any **four** out of five. (4*5=20)

a. What are the major requirements of I/O module?

b. Draw the flowchart of non-restoring division algorithm and explain the same.

c. With the help of diagram, explain Von-Neumann architecture.

d. Compare SRAM & DRAM.

e. Note on pipeline hazards.

Q. 2. a) Explain Flynn's classification in detail. (10)

b) Discuss the various characteristics of Memory. (10)

Q. 3. a) Multiply (-4) and (2) using Booth's algorithm. (10)

b) Explain Instruction cycle with Interrupt execution with example. (10)

Q. 4. a) Express $(4.50)_{10}$ in IEEE 754 single & double precision standard of floating point number representation. (10)

b) Explain design of control unit wrt softwired and hardwired approach. (10)

Q. 5. a) Divide 13 by 3 using restoring division algorithm. (10)

b) Explain different addressing modes with example. (10)

Q. 6. Write a note on any **two**. (2*10=20)

a. Comparison of RISC & CISC

b. Programmed I/O

c. Mapping techniques of Cache memory