DESIGN AND COMPARITIVE STUDY OF INMEMORY COMPUTING USING DIFFERENT SRAM TOPOLOGIES(6T,7T,8T)

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ABSTRACT:

In light of the growing demand for faster and more energy-efficient computing solutions, in-memory computation (IMC) has emerged as an alternative solution to traditional Von Neumann architecture. Specifically, SRAM-based IMC schemes, with an emphasis on identifying efficient SRAM cell designs that offer high noise margin and low power consumption is studied. Through a thorough comparative analysis, various SRAM cell topologies, including 6T, 7T, and 8T, are examined to evaluate their power consumption and noise margin characteristics. Balancing considerations such as power consumption, space utilization, and noise margin, the 8T SRAM cell is selected as the optimal choice for in-memory computing applications. Utilizing the 8T SRAM cell, the feasibility of performing logic operations such as NAND, NOR, AND, OR, XOR, and XNOR within the context of in-memory computing is demonstrated.

ORIGIN OF THE PROBLEM:

The von Neumann computing architecture has been a cornerstone of computing systems for several decades but faces challenges like the memory wall problem and the von Neumann bottleneck due to increasing data-intensive computing demands. To mitigate these issues, researchers have explored in-memory Boolean computation as a potential solution. This approach involves performing Boolean operations directly within memory units, reducing the need for data movement between memory and processing units and thus alleviating the bottleneck caused by the traditional von Neumann architecture's separation of memory and processing.

RELEVANCE IN THE AREA OF MEMORY

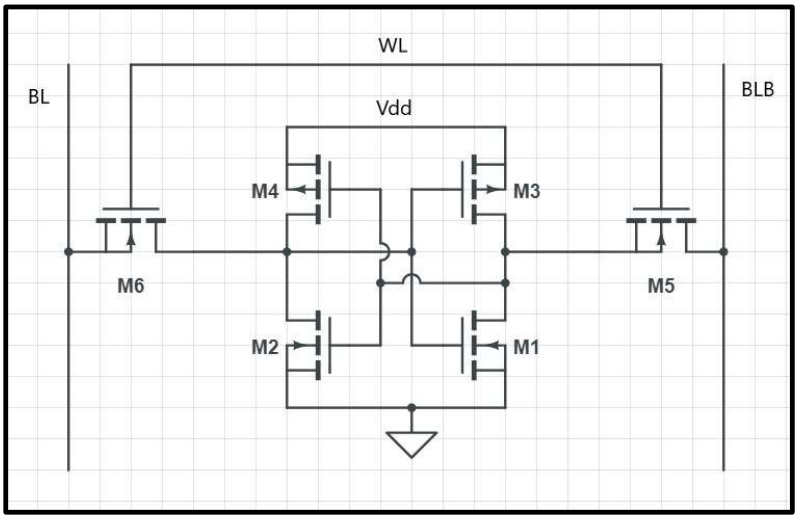
Using SRAM cell architectures like 6T, 7T and 8T in in-memory computing is crucial for memory and neuromorphic devices. In-memory computing performs calculations directly within memory, saving energy. Choosing the right SRAM design is vital for optimizing performance. Different designs offer trade-offs in power consumption and noise margins. For instance, the 6T design prioritizes performance and area efficiency, while the 8T design emphasizes energy efficiency and noise margin. In neuromorphic devices, mimicking brain functions, SRAM choice is critical for efficient parallel processing. Understanding design trade-offs helps in developing better, more energy-efficient computing systems, from memory tasks to brain-like computing.

METHODOLOGY

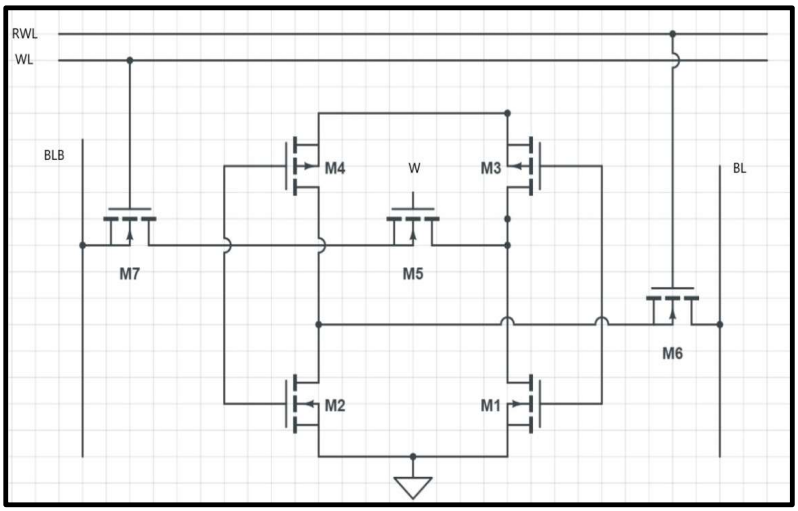
The study employed LTspice for modeling and analyzing various SRAM cell designs, ensuring the reliability of simulations by accurately reflecting real-world behavior. Based on the findings, different logic operations such as NAND, NOR, OR, AND, XOR, and XNOR were implemented using in-memory computing and simulated using an 8T SRAM cell. Transistors were configured to mimic typical SRAM cell functions, including weak pull-up, strong pull-down, and medium pass transistors. By simulating power usage and noise margins in LTspice, different SRAM designs were compared to assess their suitability. Each architecture, such as the 6T, 7T, and 8T SRAM cells, exhibited distinct characteristics regarding power consumption, noise margins, and area efficiency.

The Designs of the various SRAM topologies are as follows:

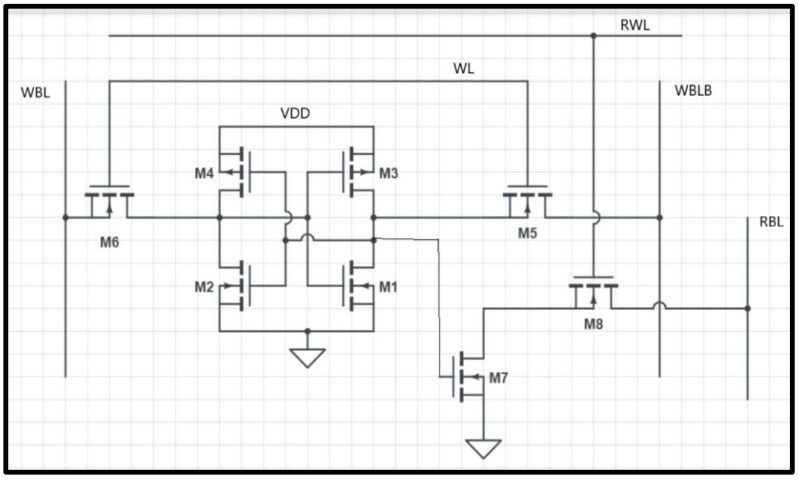
6T SRAM CELL:



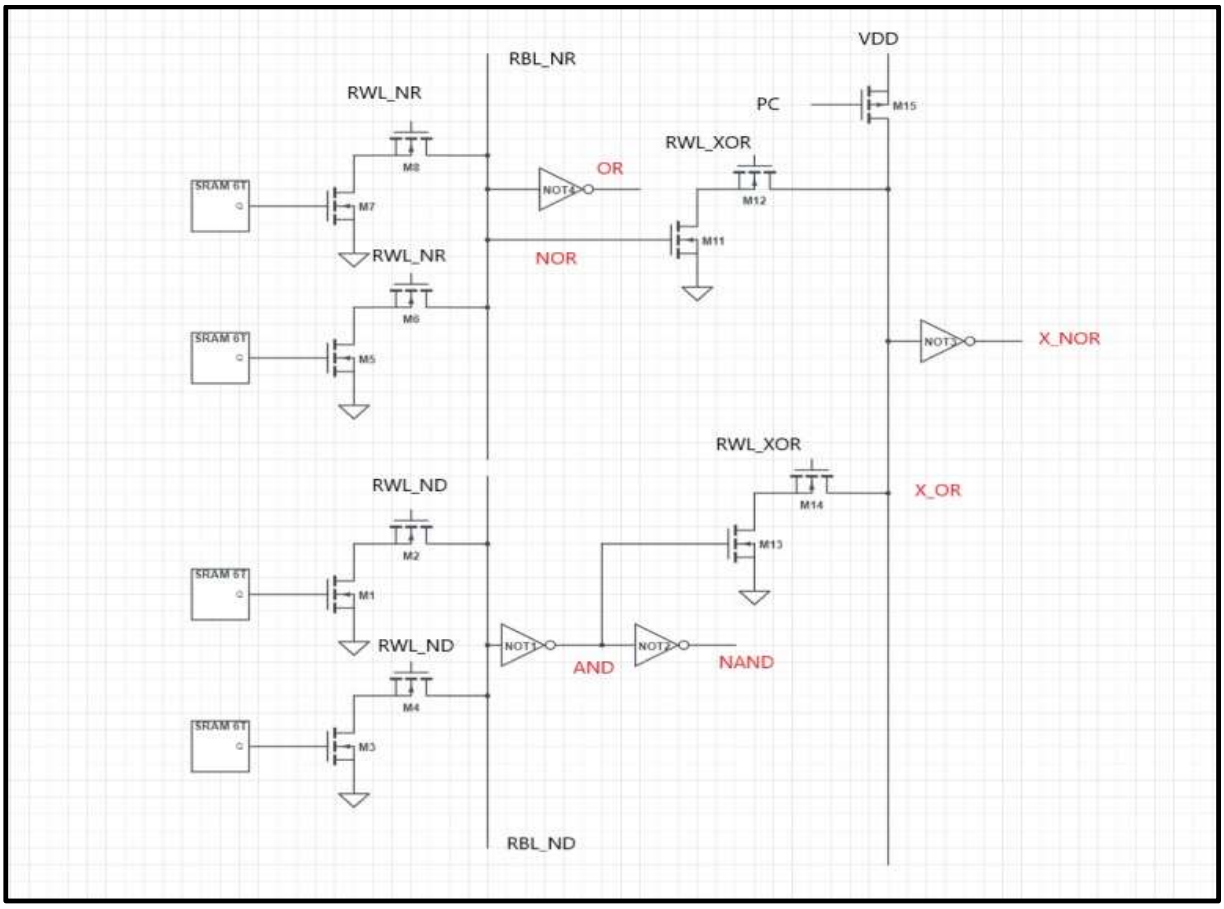
7T SRAM CELL:



8T SRAM CELL:



LOGIC FOR INMEMORY COMPUTING:



NOR:

To obtain NOR logic, the read bit lines (RBL_NR) are wired together forming the wired nor logic .RWL_NR is high so as to activate the Read Bit lines.

Case 00: The Read bit line is precharged to vdd, and when both the cells have 0,0, the transistors M7 and M6 are off. Hence the RBL_NR remains at Vdd.

Case 01/10: when any of the cells has 1, then either of M6 or M7 is on. As a result, there is a path for discharge. The value of 0, is sensed at RBL_NR.

Case 11: When both the cells have 1, both M6,M7 are on. There is a path for discharge and at RBL_NR, 0 can be sensed.

OR can be Obtained from NOR using an inverter

NAND:

To obtain NAND Logic, the read bit lines (RBL_ND) are wired together in a way similar to the NOR logic. But in this case RWL_ND is on for a shorter duration.

Case 00: The Read bit line is precharged to Vdd, and when both the cells have 0,0, the transistors M2 and M4 are off. Hence the RBL_NR remains at Vdd.

Case 01/10: when any of the cells has 1, then either of M2 or M4 is on. As a result, there is a path for discharge. But there is no complete discharge because the width of the WBL_ND is very small. Hence using two inverters , the value can be pulled to Vdd.

Case 11: When both the cells have 1, both M2,M4 are on. Since both the transistors are on, there is discharge path and the amount of voltage that appears across the RBL_ND is such that, when given to the inverters, logic 0 can be obtained.

AND can be obtained from NAND using an inverter

XOR:

XOR logic can be obtained by utilising both AND and NOR as follows:

XOR=(output of NOR) NOR (output of AND).

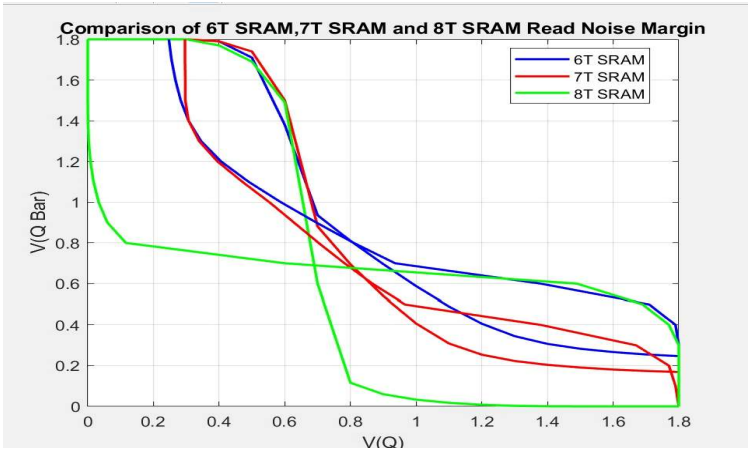
XNOR can be obtained from XOR using inverter.

TRUTH TABLE:

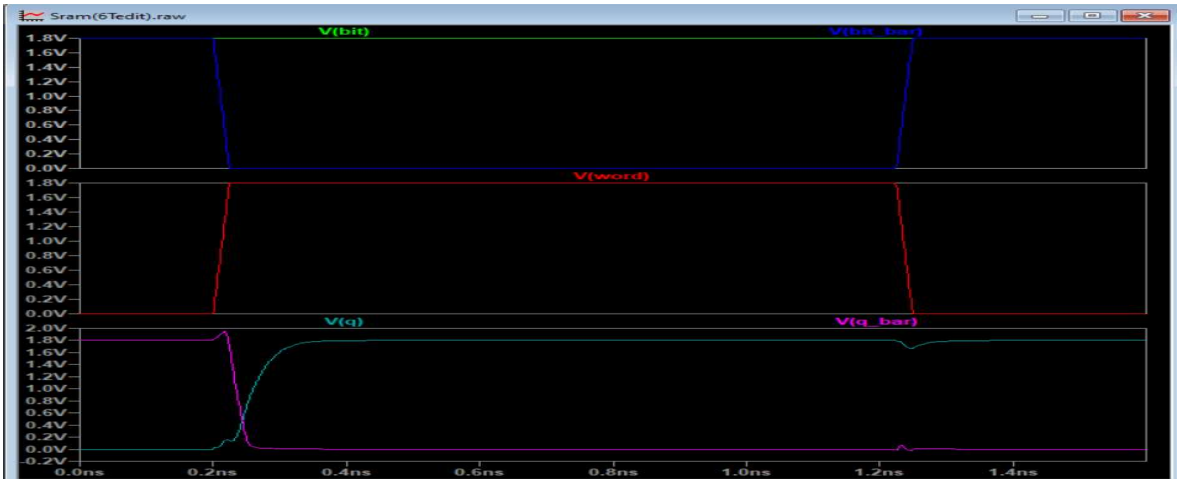
INPUTS	NOR	NAND	XOR
00	1	1	0
01	0	1	1
10	0	1	1
11	0	0	0

RESULTS:

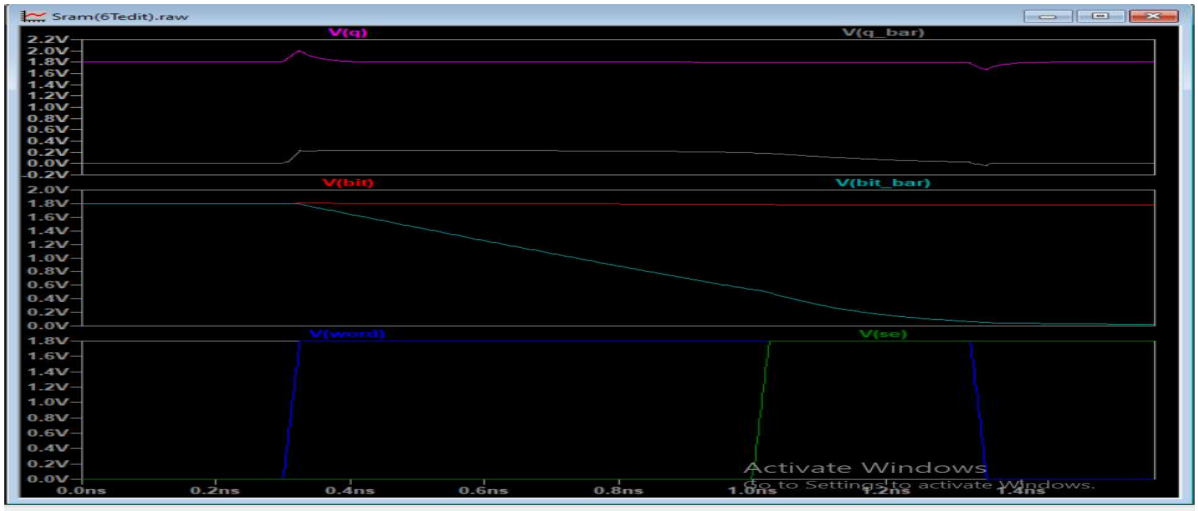
Comparison Between 6T,7T and 8T SRAM Read Noise Margin



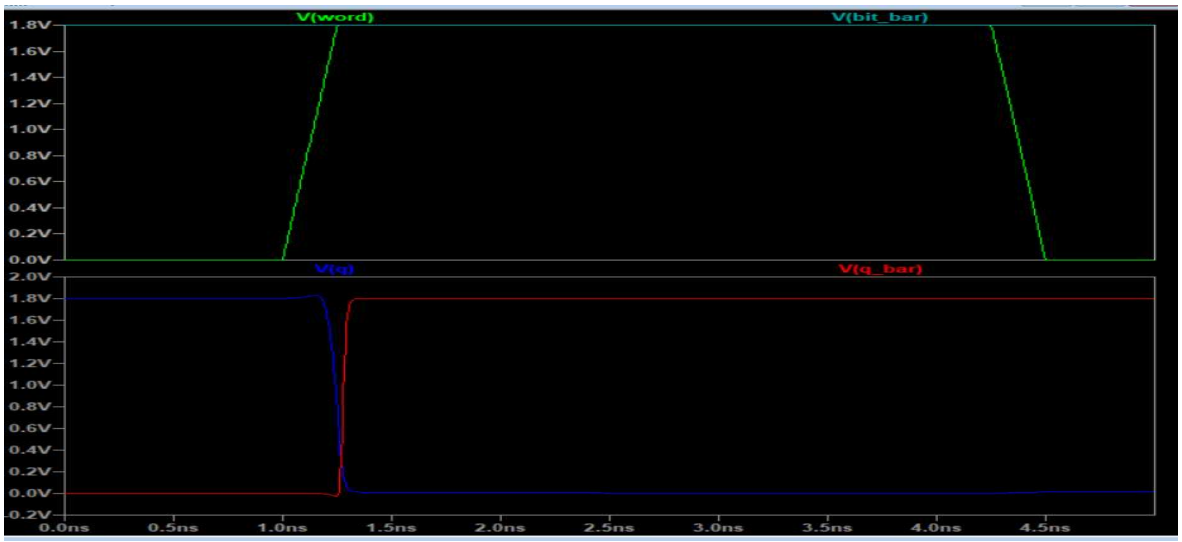
6T-SRAM (Write Operation)



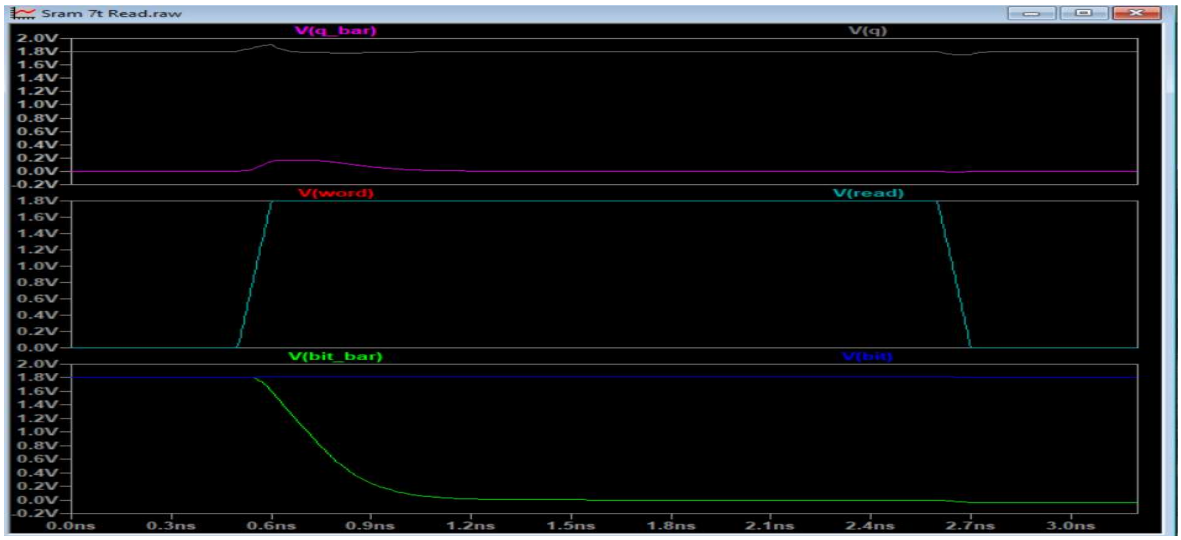
6T-SRAM (Read Operation)



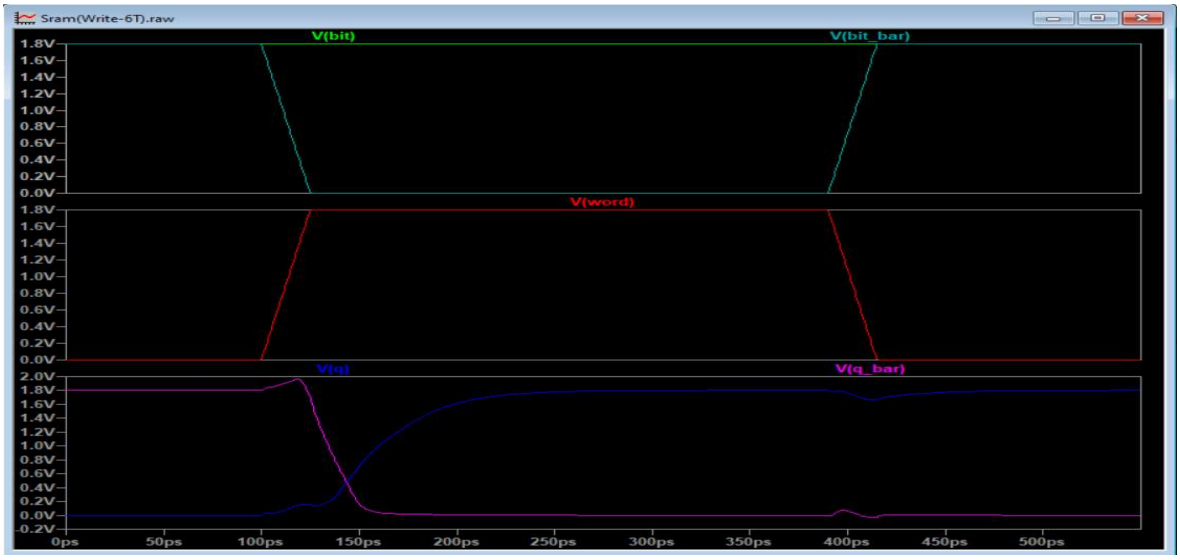
7T-SRAM (Write Operation)



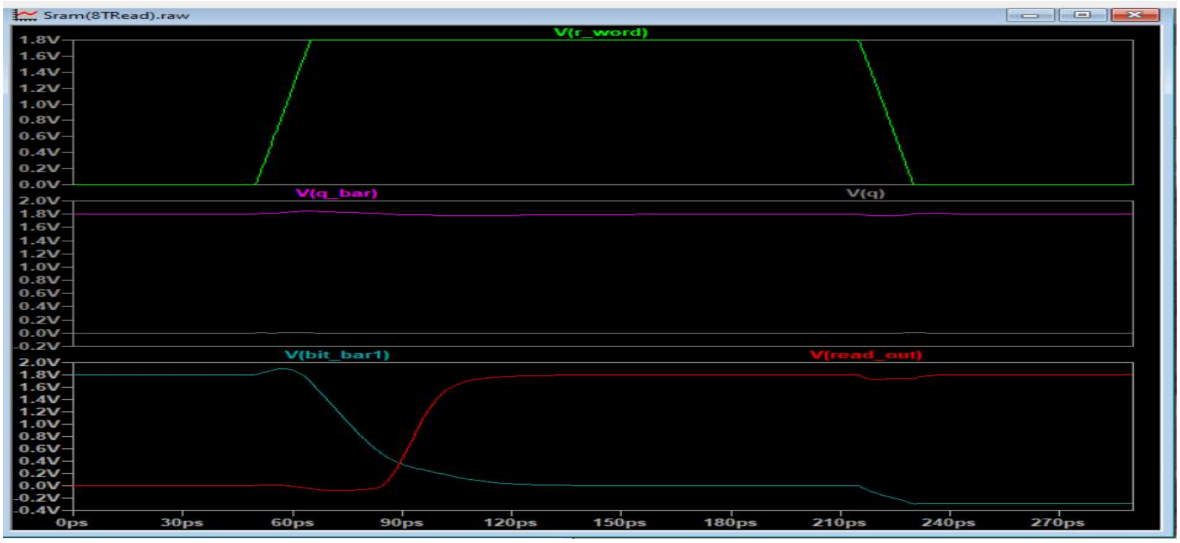
7T-SRAM (READ Operation)



8T-SRAM (Write Operation)

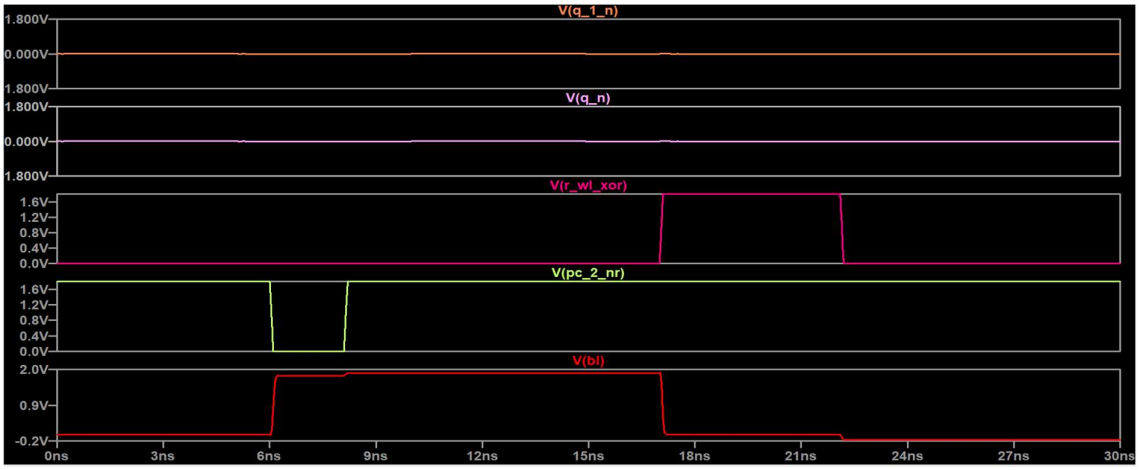


8T-SRAM (READ Operation)

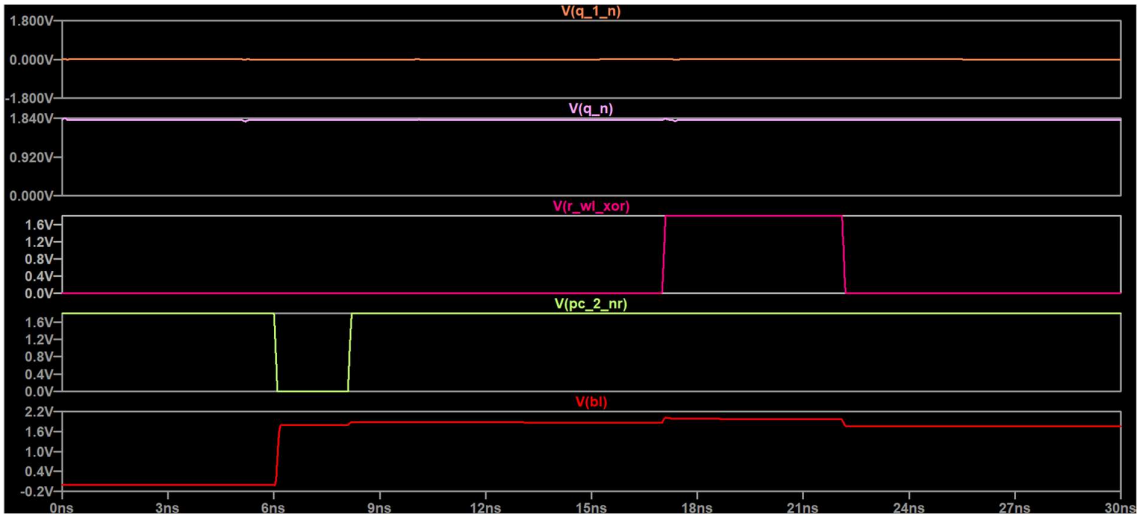


The following are the results obtained for XOR Gate using in-memory-computing

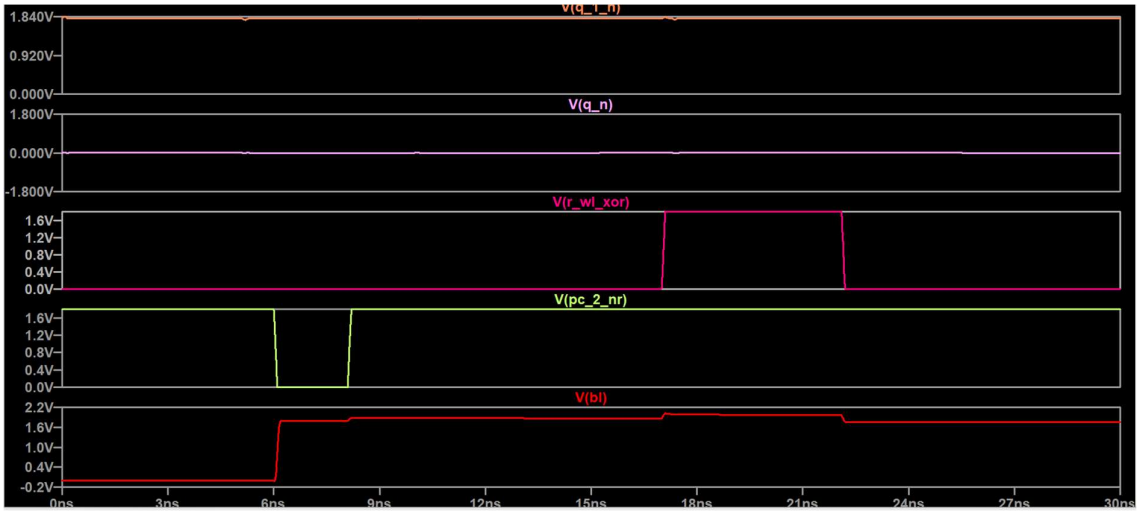
CASE 00:



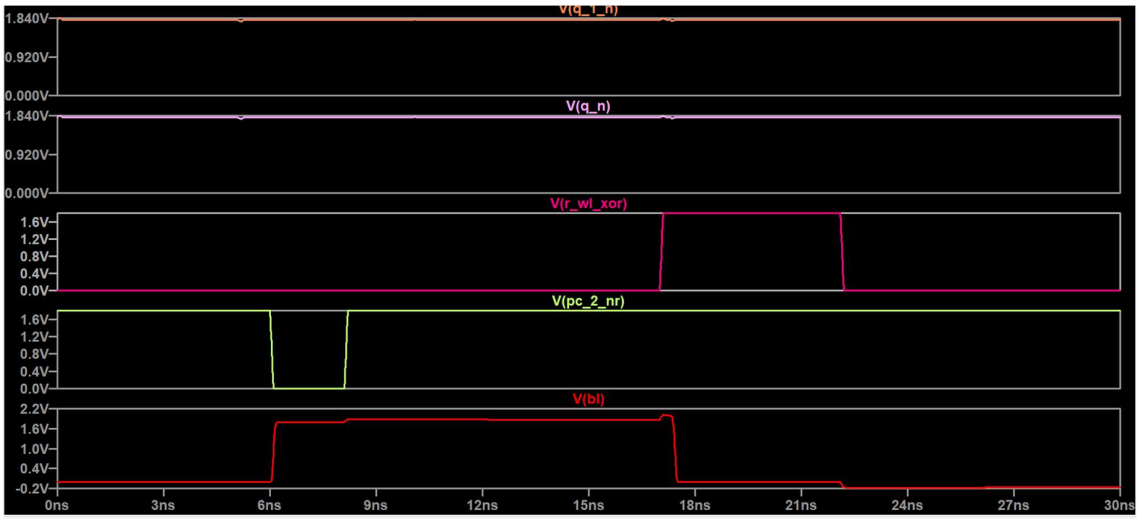
CASE 01:



CASE 10:



CASE 11:



CONCLUSION:

TOPOLOGY	POWER
6T SRAM	8.9µW
7T SRAM	2.5µW
8T SRAM	4.69µW

From the read noise margin figures and the above table, we can see that the 8T SRAM cell has the best noise margin and moderate power consumption compared to 6T and 7T SRAM cell topologies. So 8T SRAM Cell has been chosen to design various logic gates for In memory computing. Even though the complexity and the area increase in case of 8T SRAM cell, because of the better noise margin and comparatively lesser power consumption, it can provide better stability and energy efficiency while performing logical operations in the memory.

REFERENCES:

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2. Neeraj Kr.Shukla,Manisha Pattnaik, R.K.Singh, Shilpi Birla et. al. / International Journal of Engineering Science and Technology Vol. 2(7), 2010, 2936-2944