3. UGBW = 3dB BW × gain

$= 5 \times 10^3 \times 2\pi \times 10^3$

$= 314 \times 10^5$

$\frac{g_{m_1}}{C_C} = UGB$

$g_{m_1} = UGB \times C_C = 314 \times 10^5 \times 0.5\,pF \times 25 =$

$= 98.6 \times 10^{-6}\,S.$

$\left(\frac{W}{L}\right)_{1,2} = \frac{g_{m_1}^2}{2 I_{D_1} \times \beta_n} = 4.2$ $\boxed{\left(\frac{W}{L}\right)_{1,2} = 4.2}$

4. $\left(\frac{W}{L}\right)_{3,4} = \frac{2\,I_{D_3}}{\beta_p (V_{DD} - I_{CMR} - V_{tmax} + V_{tmin})^2}$

$= \frac{.2 \times 5\mu A}{75\mu C [1.8 - 1.6 - 0.5 + 0.5]^2} = \boxed{3.33}$

5. $V_{dsat} \leq I_{CMR}(min) - \sqrt{\frac{2 I_{D_1}}{\beta_1 \left(\frac{W}{L}\right)_1}} - V_{t,min}$

$\leq 0.8 - \sqrt{\frac{10\mu}{23\mu \times 4.2}} - 0.5$

≤ 0.199

$\left(\frac{W}{L}\right)_{5,8} = \frac{2 I_5}{\beta_n \times (V_{dsat})^2} = \boxed{2.199 = \left(\frac{W}{L}\right)_{5,8}}$

6.

$$V_{SG_4} = V_{SG_6}$$

$$g_m \propto V_{GS}$$

$$\frac{g_{m_6}}{\left(\frac{W}{L}\right)_6} = \frac{g_{m_4}}{\left(\frac{W}{L}\right)_4}$$

$$g_{m_6} > 10\, g_{m_1}$$

$$g_{m_6} > 986\,\mu S$$

$$g_{m_{3,4}} = \sqrt{2\beta_1 I_{D_3}\left(\frac{W}{L}\right)_3} = \sqrt{2 \times 75\mu \times 5\mu \times 3.33}$$

$$= 49.97$$

$$\frac{g_{m_6}}{\left(\frac{W}{L}\right)_6} = \frac{g_{m_4}}{\left(\frac{W}{L}\right)_4}$$

$$\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_4 \times \frac{g_{m_6}}{g_{m_4}} = \frac{986\,\mu S}{49.97\,\mu S} \times 3.33$$

$$\boxed{\left(\frac{W}{L}\right)_6 = 65.1}$$

Current mirror.

7. $$\left(\frac{W}{L}\right)_7 = \frac{I_7}{I_5}\left(\frac{W}{L}\right)_5$$

$$\frac{I_6}{I_4} = \frac{\left(W/L\right)_6}{\left(W/L\right)_4}, \quad I_6 = \frac{\left(\frac{W}{L}\right)_6 \times I_4}{\left(\frac{W}{L}\right)_4}$$

$$I_6 = \frac{65 \times 5}{3.33} = 97.59$$

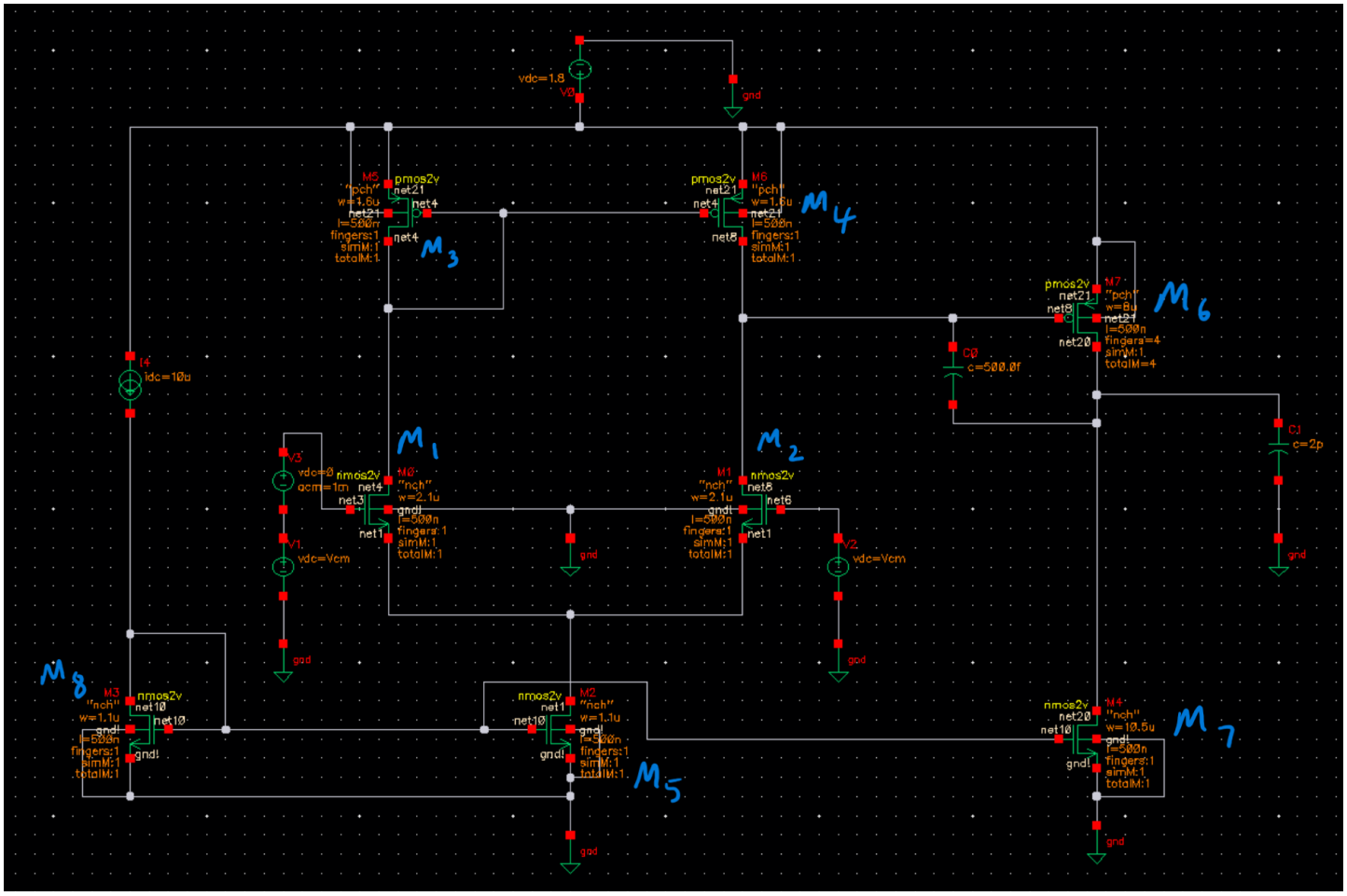
or

$$I_6 = I_7 = \frac{g_{m6}^2}{2 \beta_p \left(\frac{W}{L}\right)_6} = \frac{98^2}{2 \times 75 \times (65)} = 99.5 \mu A$$

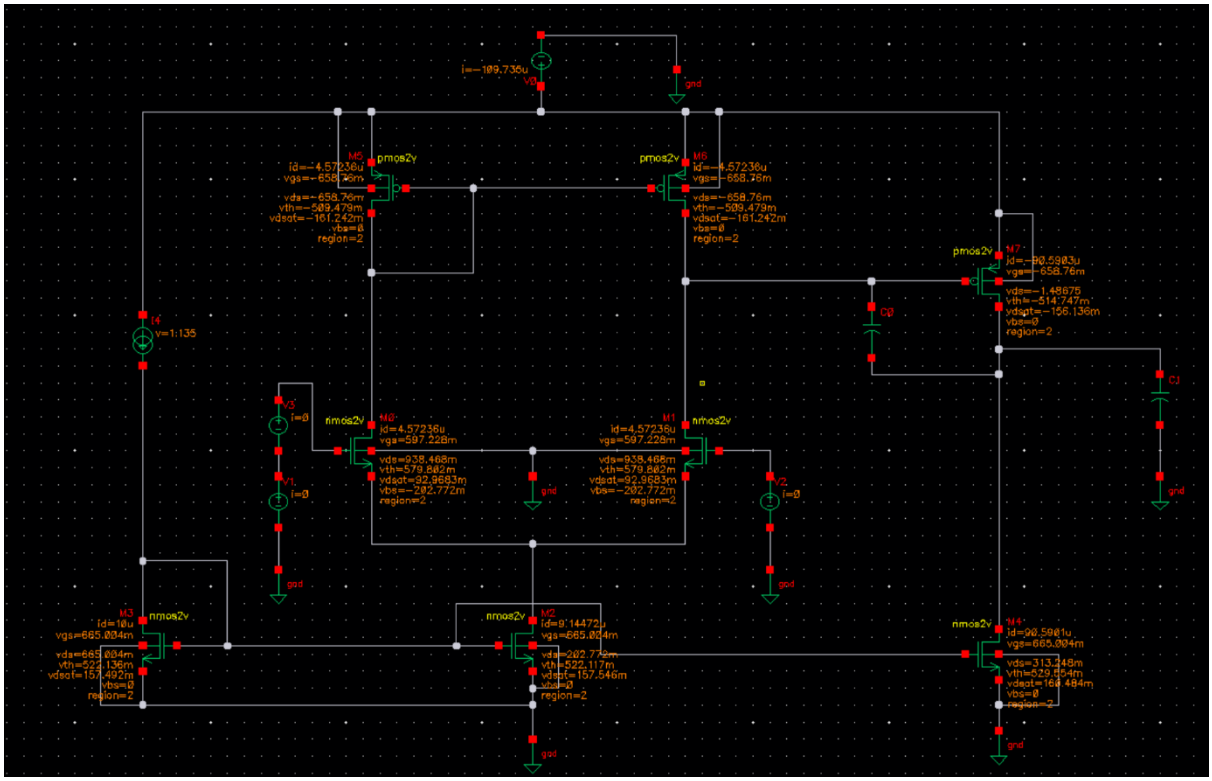
$$\left(\frac{W}{L}\right)_7 = \frac{99.5}{10} \times 2.2$$

$$\boxed{\left(\frac{W}{L}\right)_7 = 21.9}$$

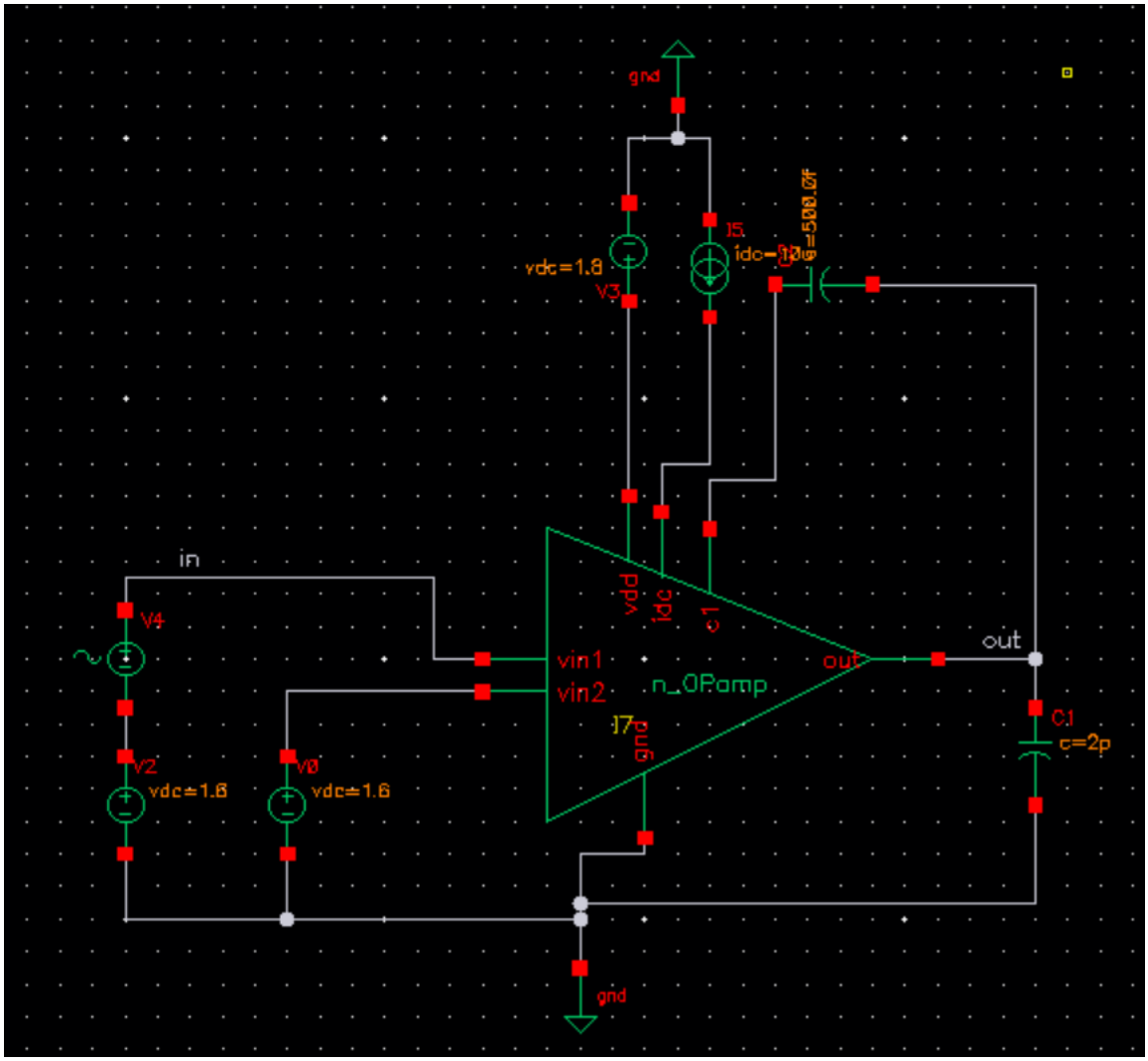
Schematic:



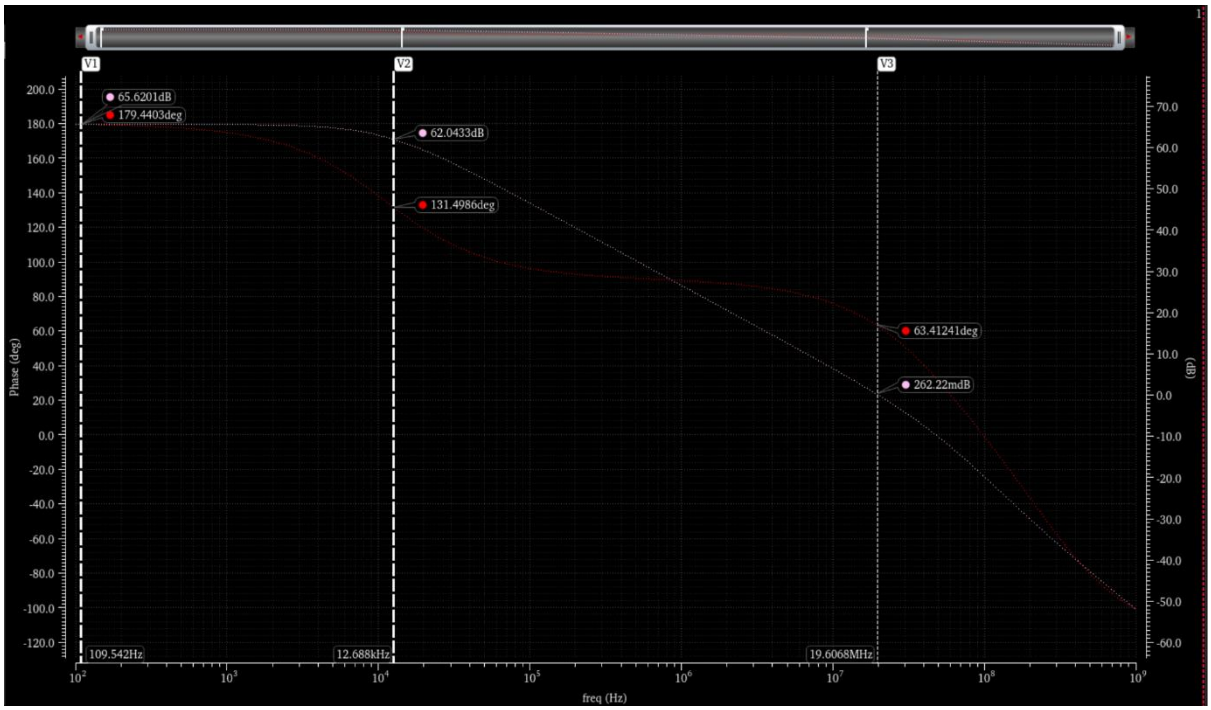
The W/L values of all the transistors are kept as calculated above and all the transistors are in saturation region (below picute) fom common mode voltage of 0.8V to 1.6V .



Symbol and Test bench without feedback



Gain,UGB and Phase margin:



From the above graph we can see that

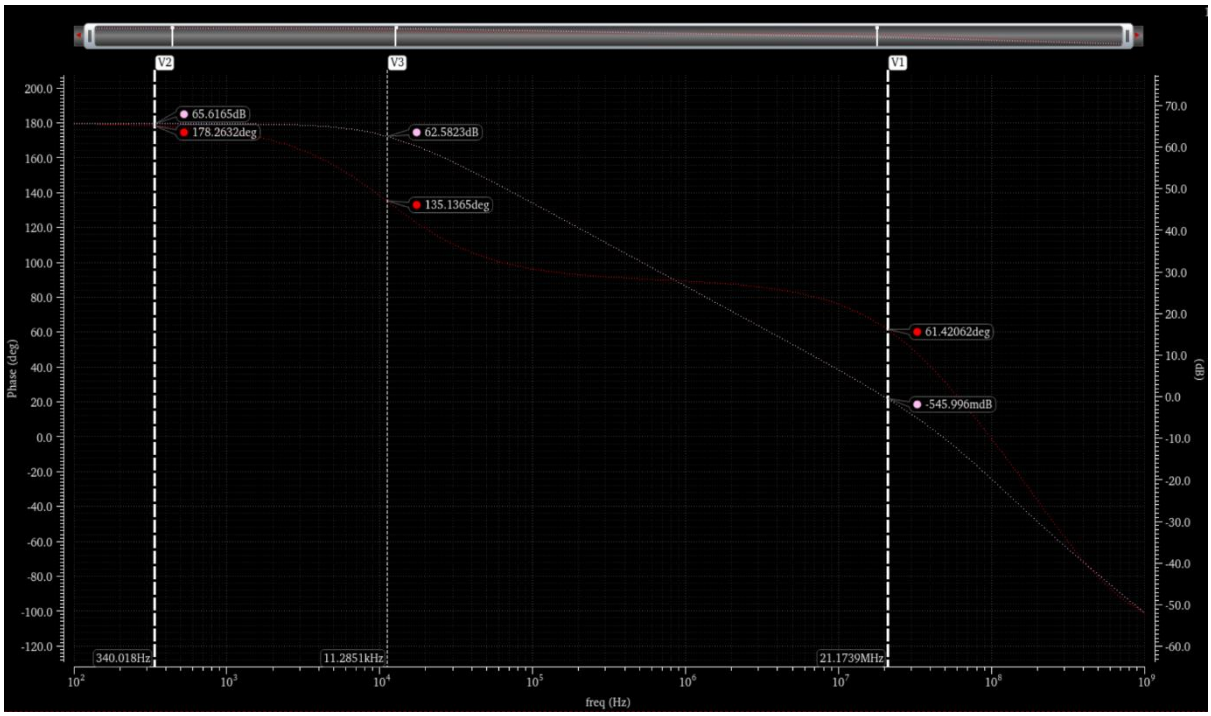
Gain = 65.6dB

Unity Gain Bandwidth = 19.6 MHZ

3dB Bandwidh = 12.6 Khz

Phase margin = 63.4degrees

Gain,UGB and Phase margin with parasitics:



From the above graph we can see that

Gain = 65.6dB

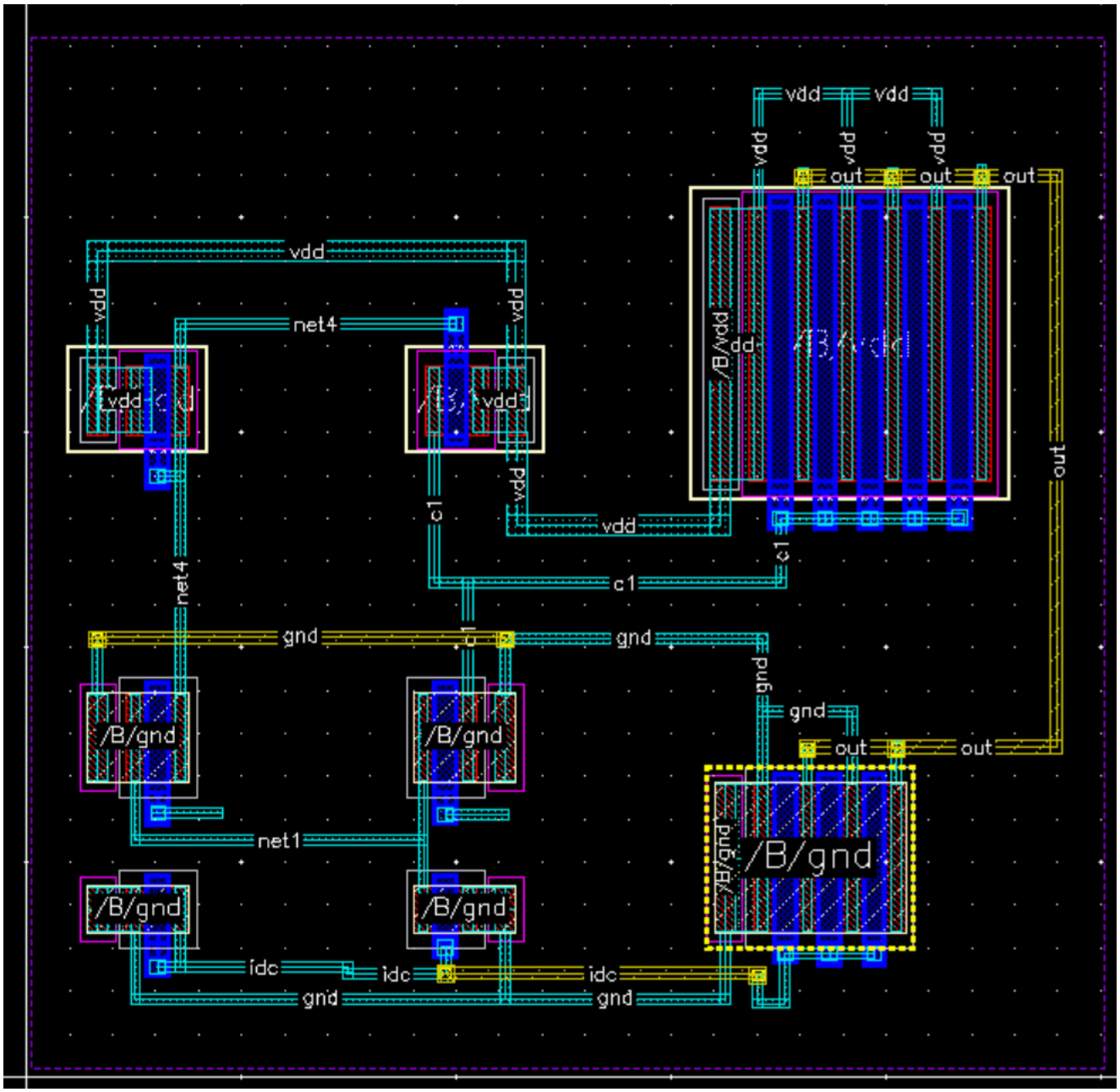
Unity Gain Bandwidth = 21.1 MHZ

3dB Bandwidh = 11.2 Khz

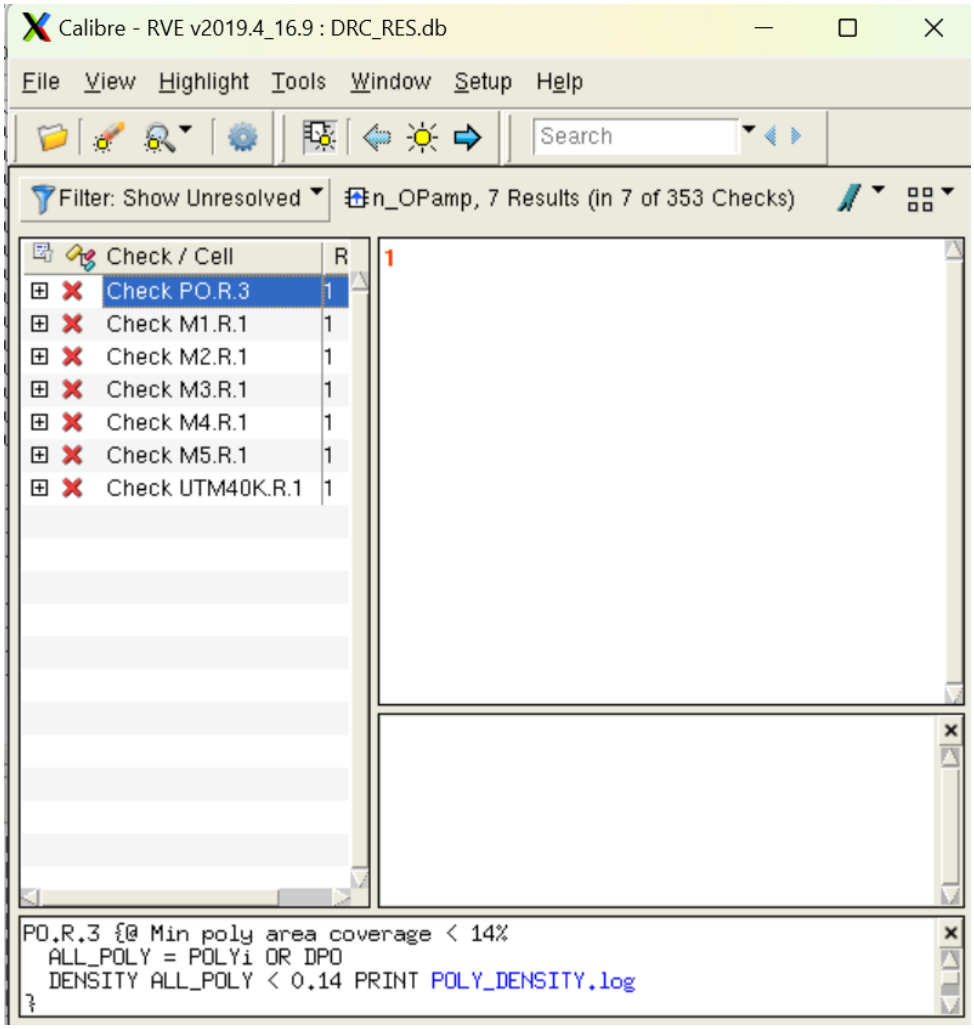
Phase margin = 61.4 degrees

We can see that gain and phase margin is not affected much due to parasitics

Layout

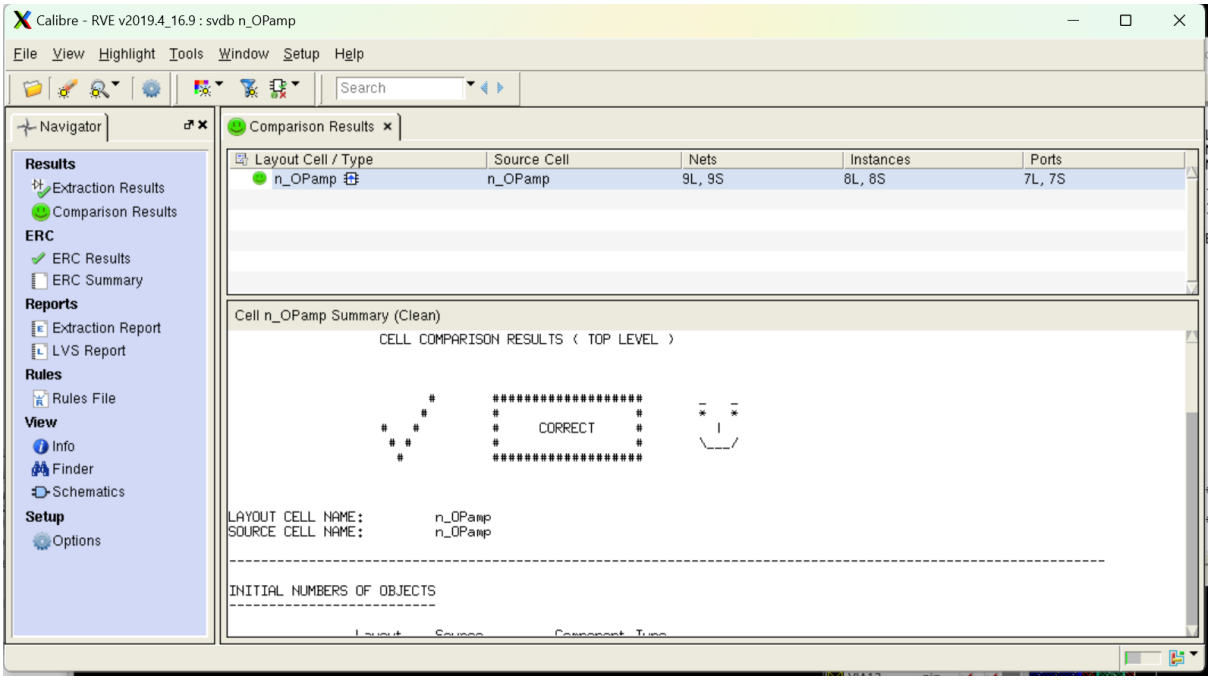


DRC Check:



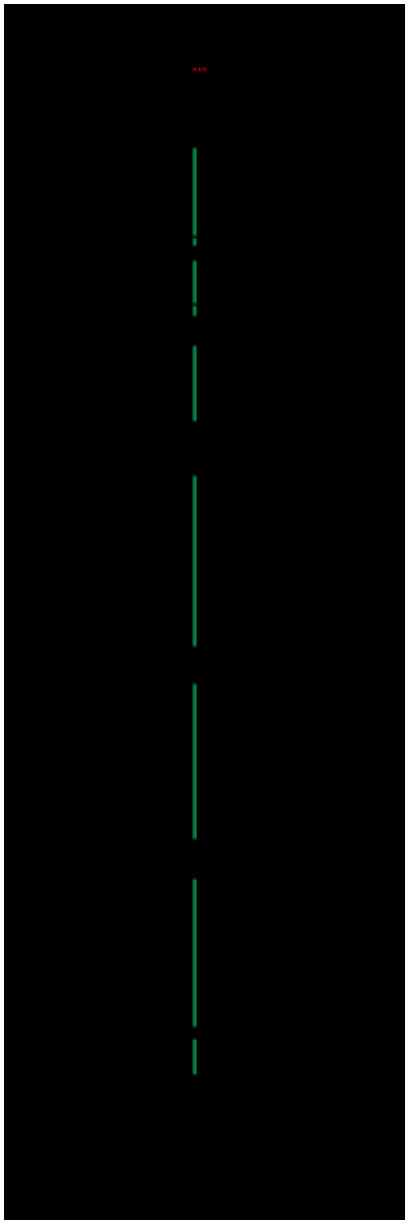
The drc is error free for the layout, the above errors are densty errors which can be ignored.

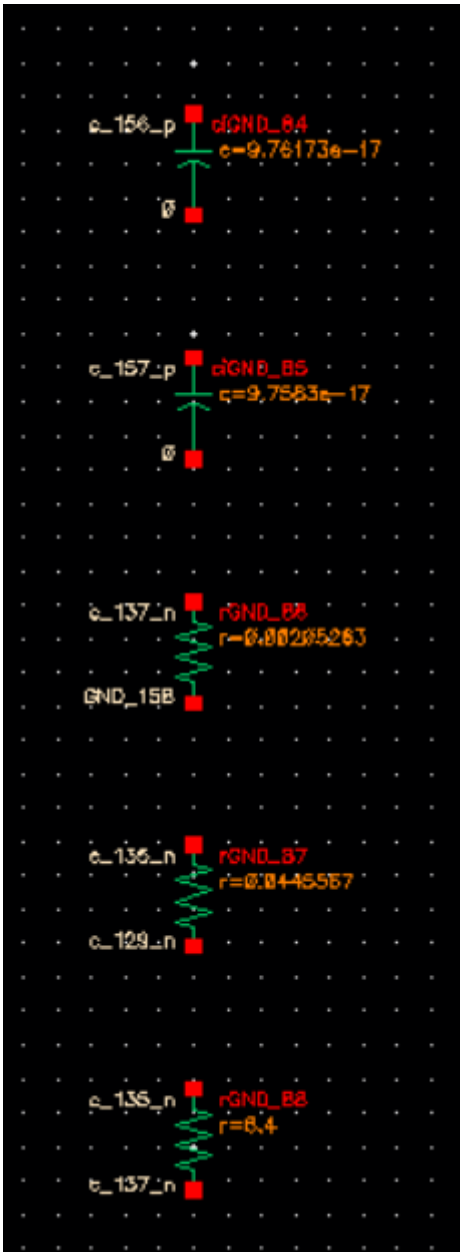
LVS



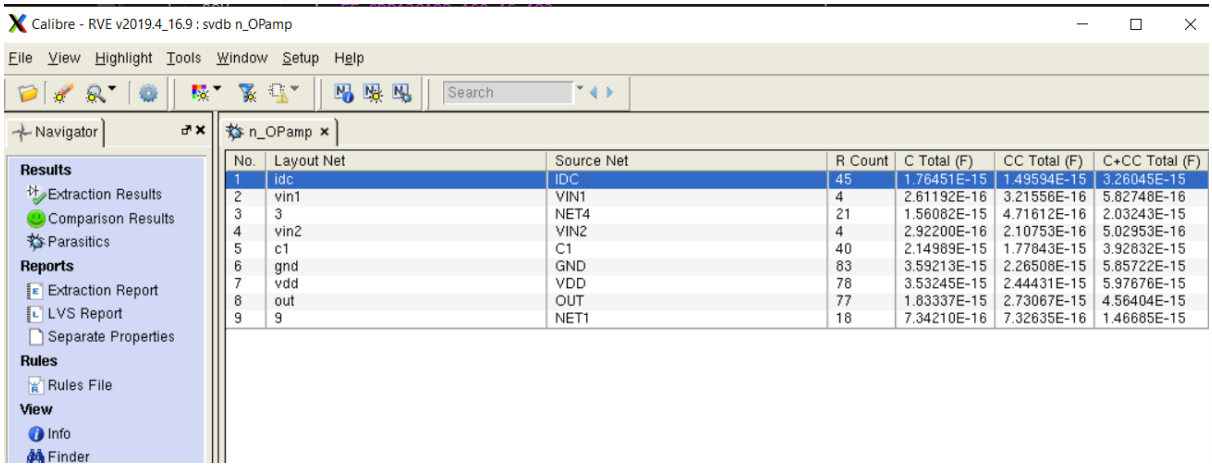
The LVS is correct for the layout without errors.

PEX:



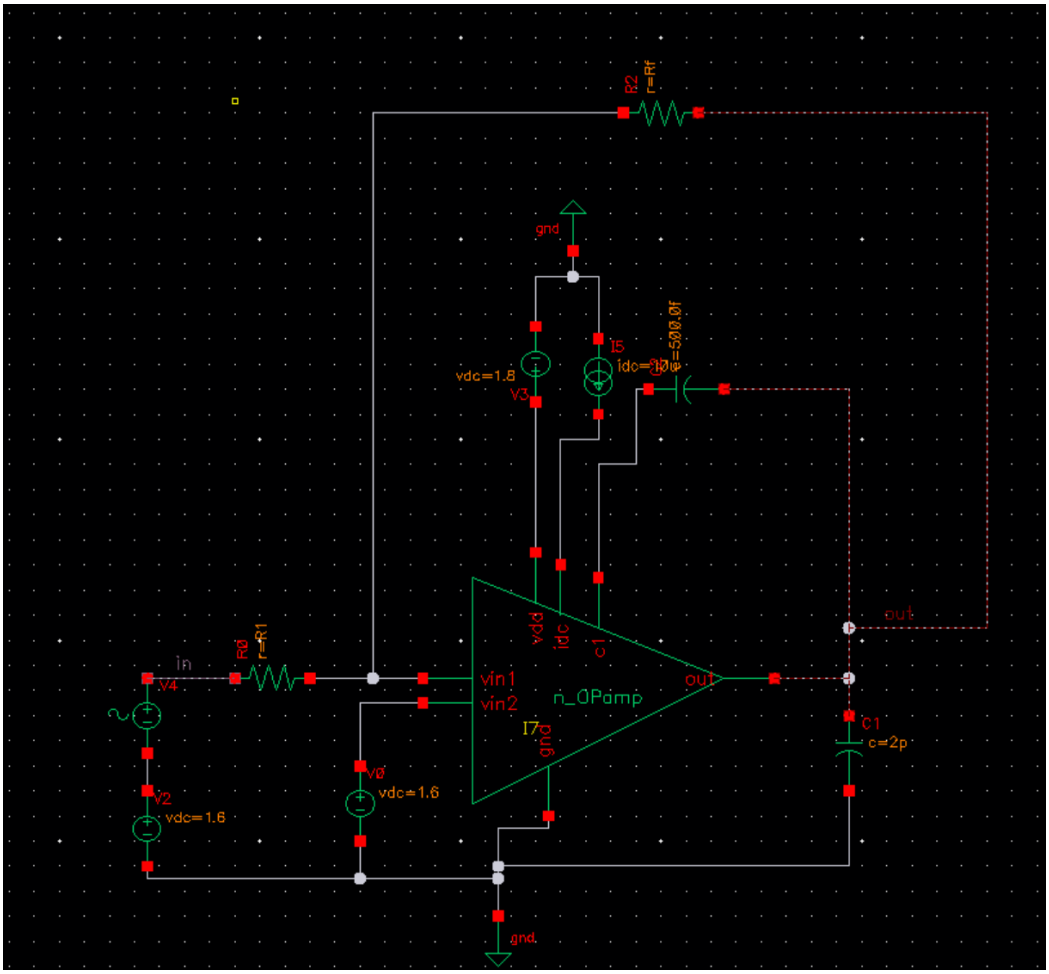


The above 2 images shows the parasitic resistance and capacitances extracted from the layout, the number of parasitics and their values can be seen in the below image.

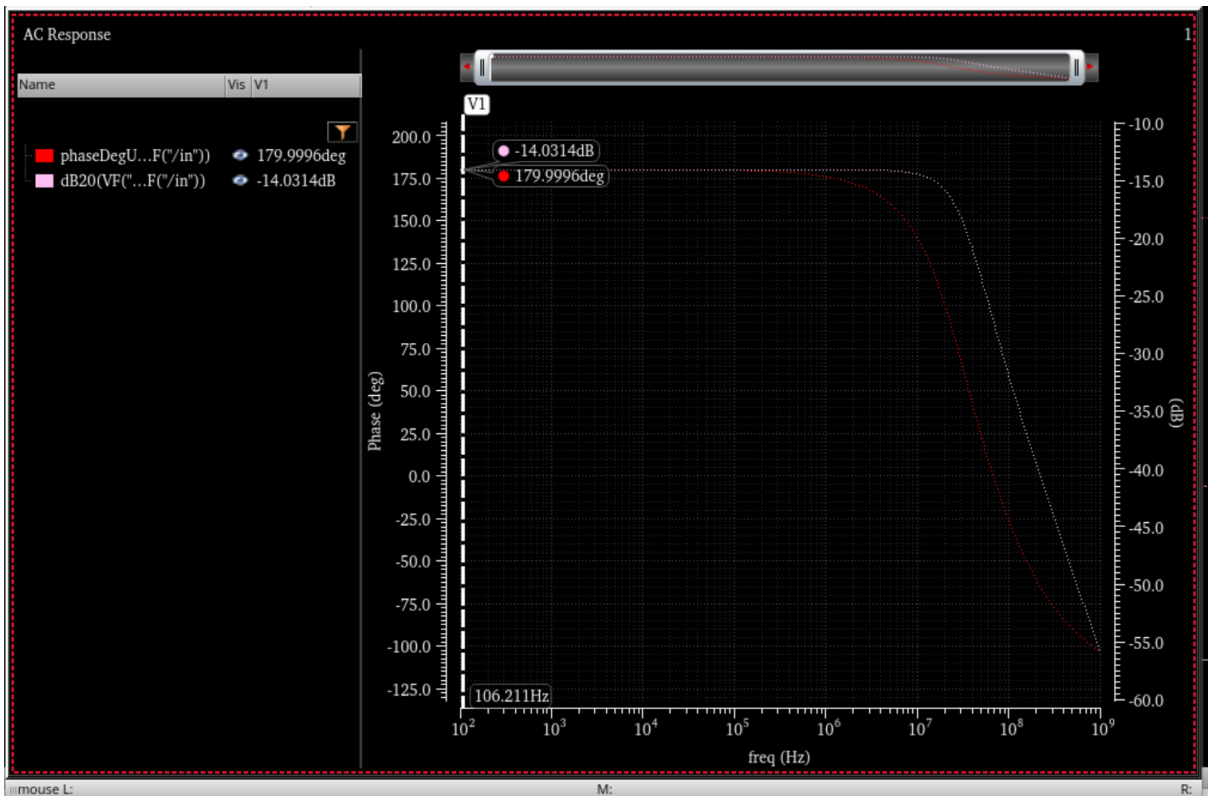


No.	Layout Net	Source Net	R Count	C Total (F)	CC Total (F)	C+CC Total (F)
1	idc	IDC	45	1.76451E-15	1.49594E-15	3.26045E-15
2	vin1	VIN1	4	2.61192E-16	3.21556E-16	5.82748E-16
3	3	NET4	21	1.56082E-15	4.71612E-16	2.03243E-15
4	vin2	VIN2	4	2.92200E-16	2.10753E-16	5.02953E-16
5	c1	C1	40	2.14989E-15	1.77843E-15	3.92832E-15
6	gnd	GND	83	3.59213E-15	2.26508E-15	5.85722E-15
7	vdd	VDD	78	3.53245E-15	2.44431E-15	5.97676E-15
8	out	OUT	77	1.83337E-15	2.73067E-15	4.56404E-15
9	9	NET1	18	7.34210E-16	7.32635E-16	1.46685E-15

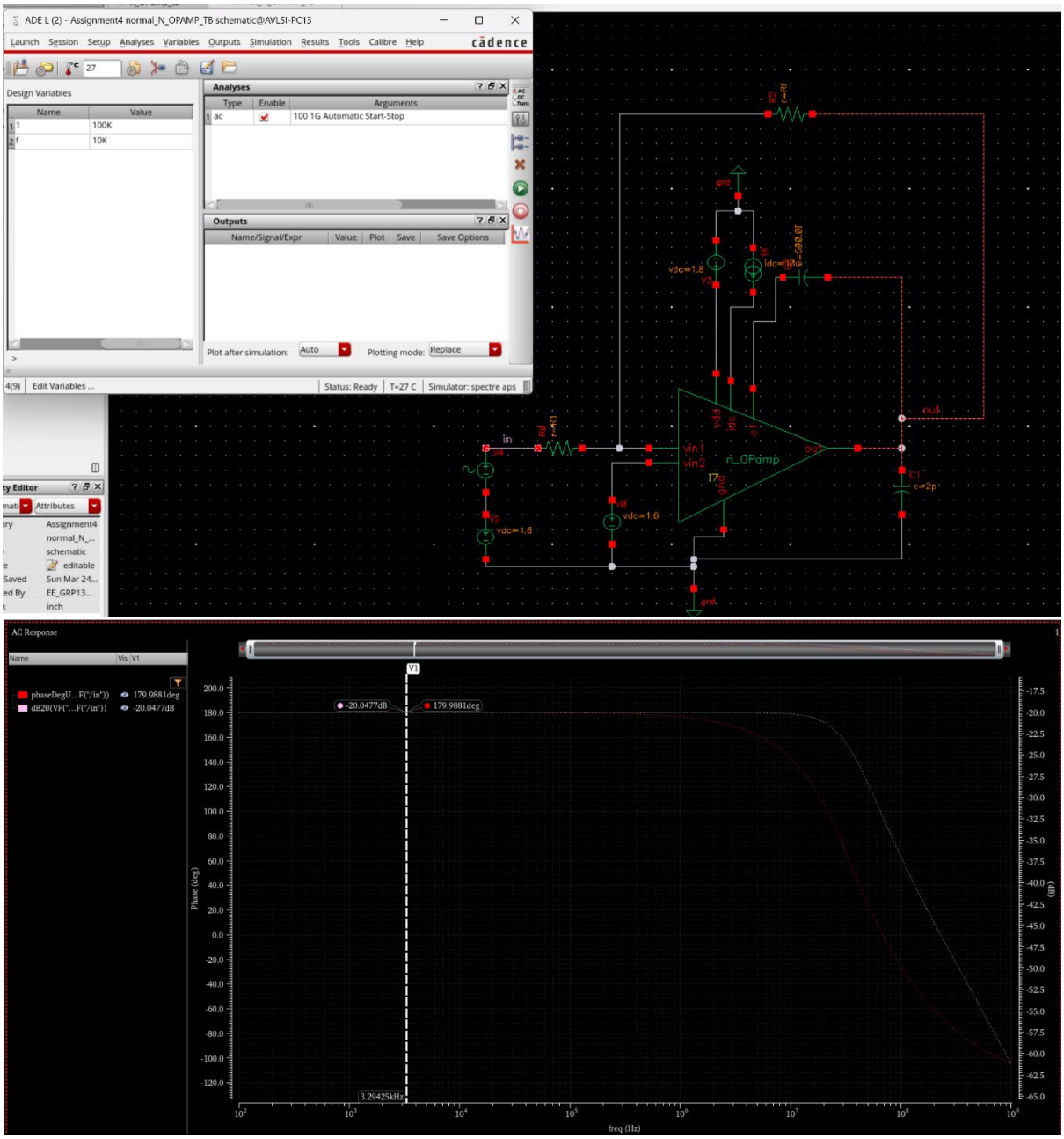
OPAMP inf Negative Feedback



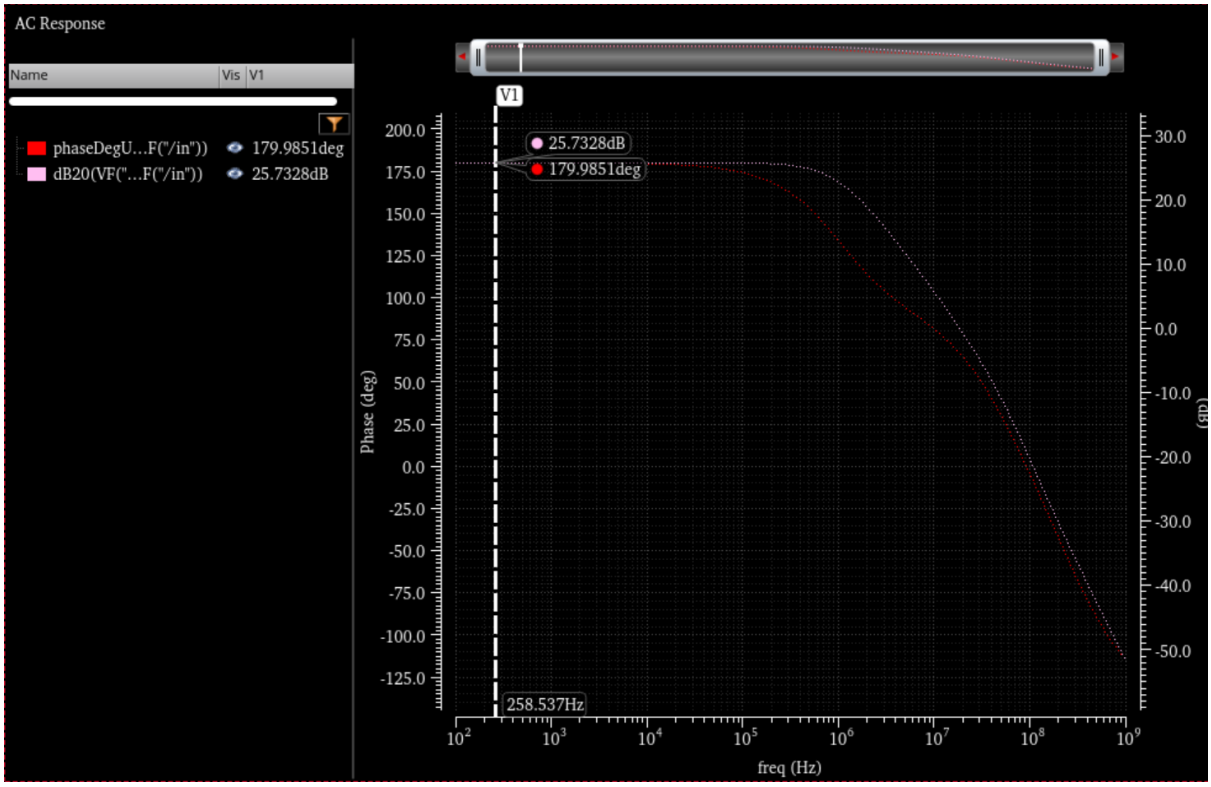
Gain of 5 V/V (14dB) when r1=10k and Rf=50k, so gain = -r1/rf = -5. Which can be seen in the below graph



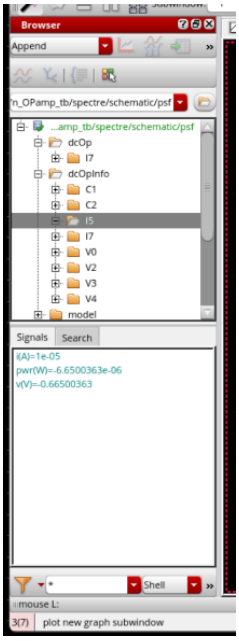
Gain of 10 V/V (20dB) when r1=10k and Rf=110k, so gain = -r1/rf = -10. Which can be seen in the below graph

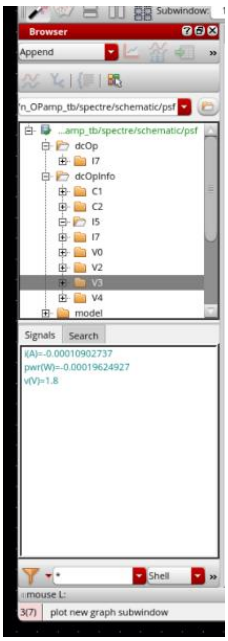


Gain of 20 V/V (24dB) when r1=10k and Rf=200k, so gain = -r1/rf = 20. Which can be seen in the below graph



Power consumption for OPAMP:

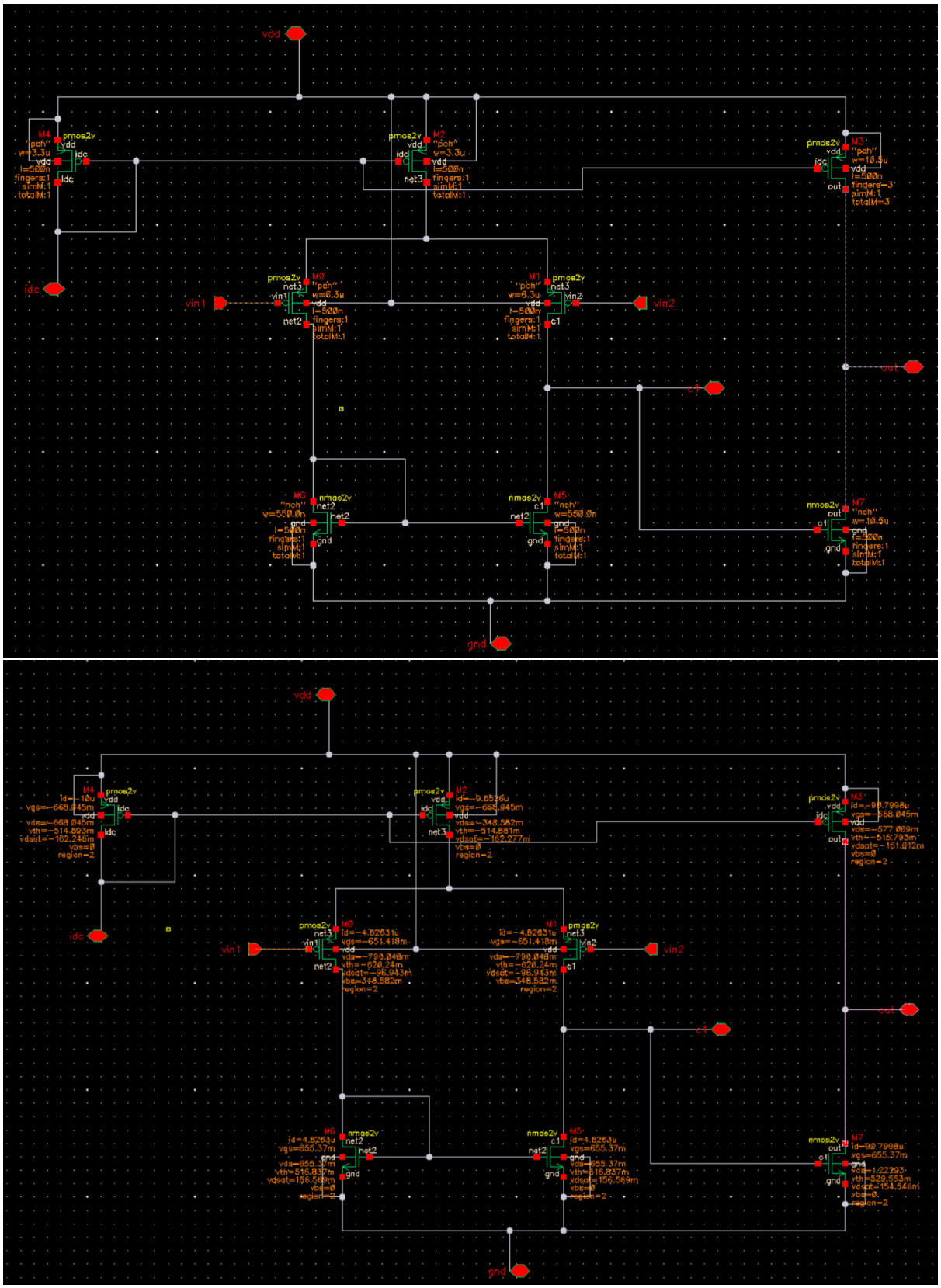




The current source and the voltage source (VDD) are the power sources in the circuit, the power consumption = -0.19mW + 6.65uW= 0.2mW

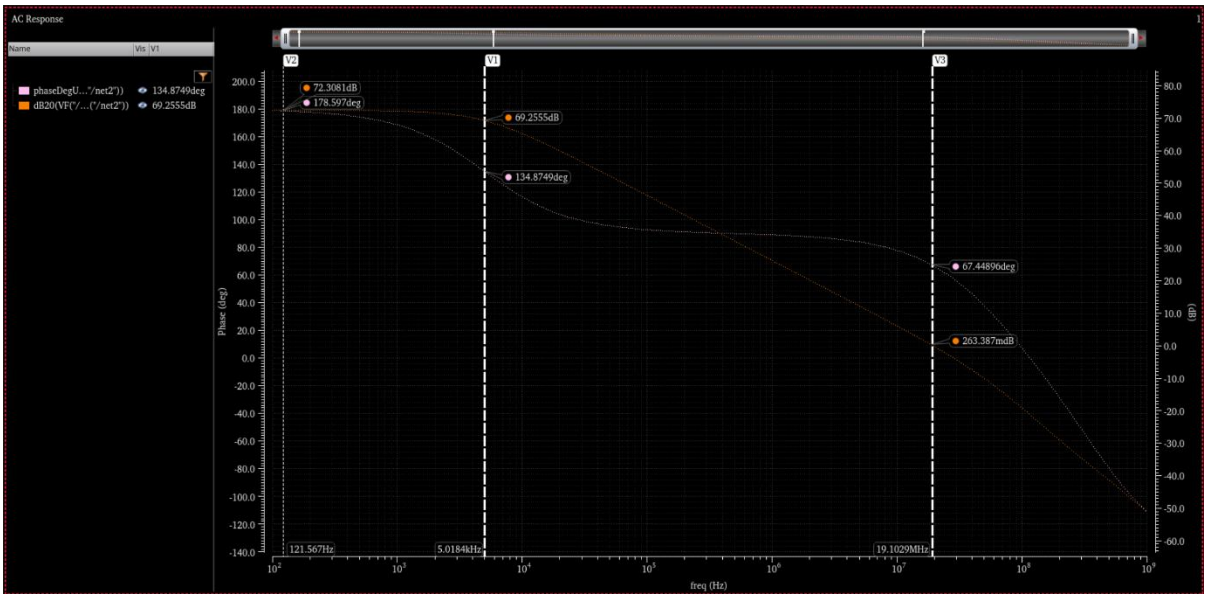
PMOS Architecture OPAMP

Schematic



All the transistors are in region 2(saturation), can be seen in the above image.

Gain,UGB and Phase margin :



From the above graph we can see that

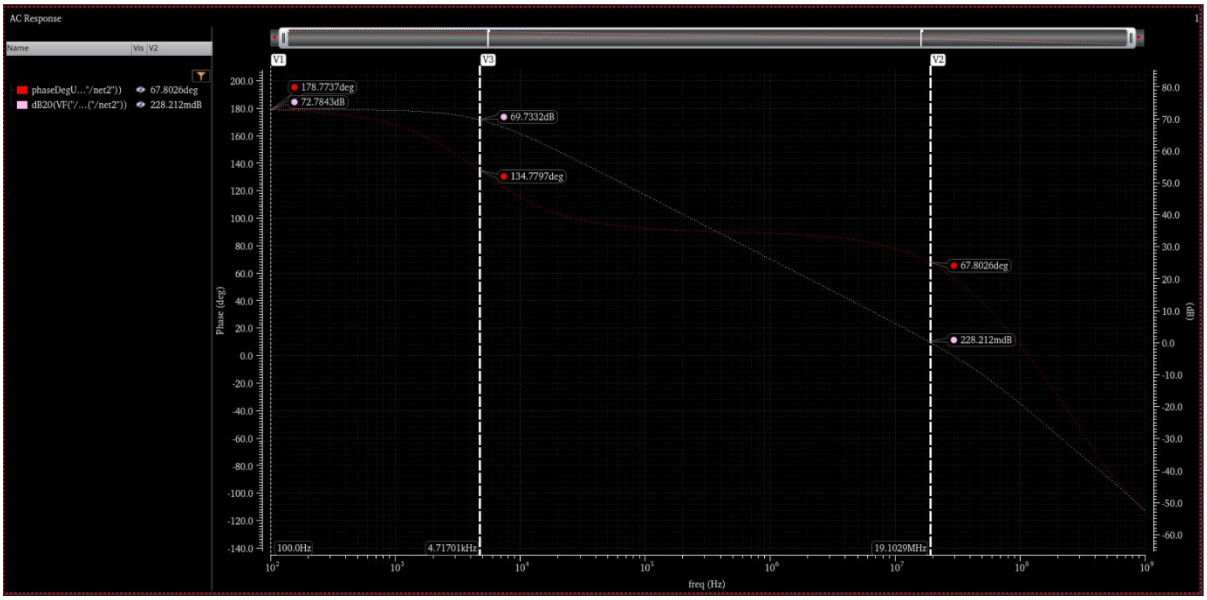
Gain = 72dB

Unity Gain Bandwidth = 19MHZ

3dB Bandwidh = 5 Khz

Phase margin = 67.4degrees

Gain,UGB and Phase margin with parasitics:



From the above graph we can see that

Gain = 72dB

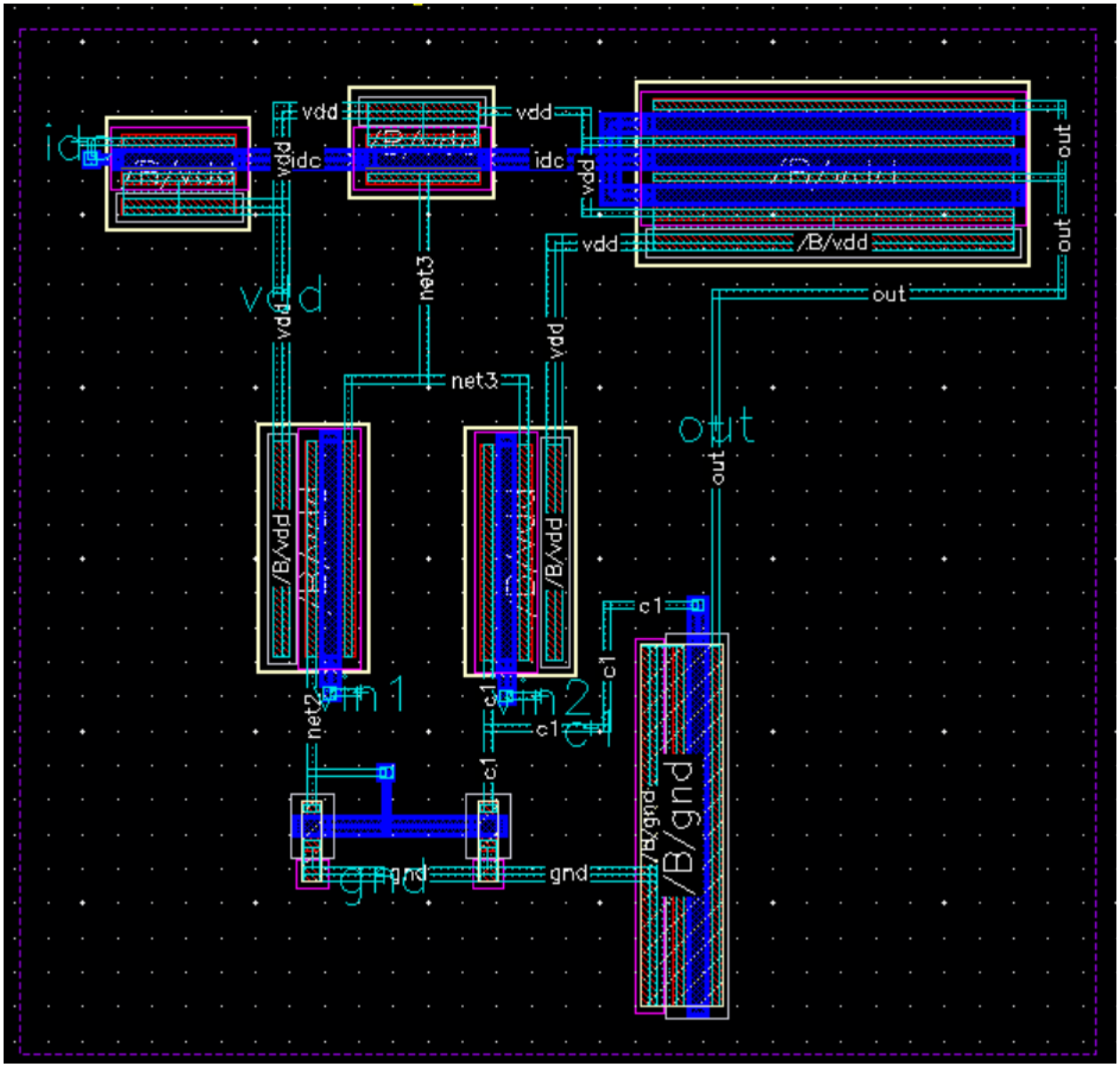
Unity Gain Bandwidth = 19.19 MHZ

3dB Bandwidh = 4.7 Khz

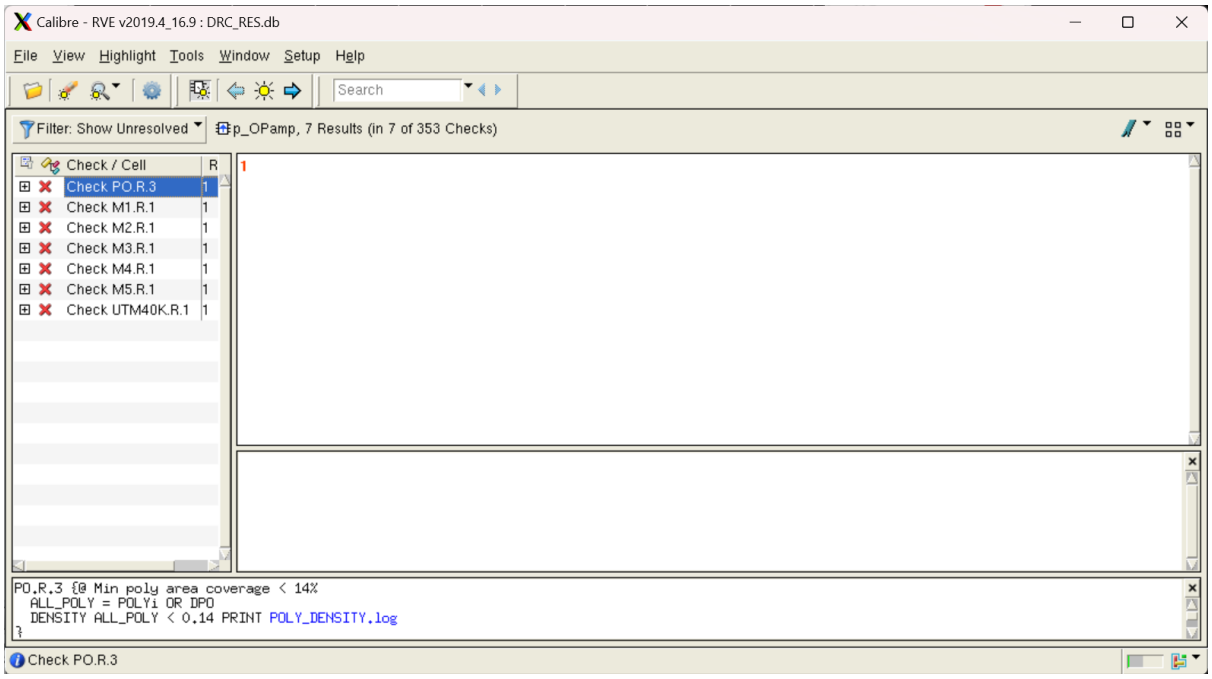
Phase margin = 67degrees

We can see that gain is not affected much and phase margin is increased as it increase the pole.

Layout

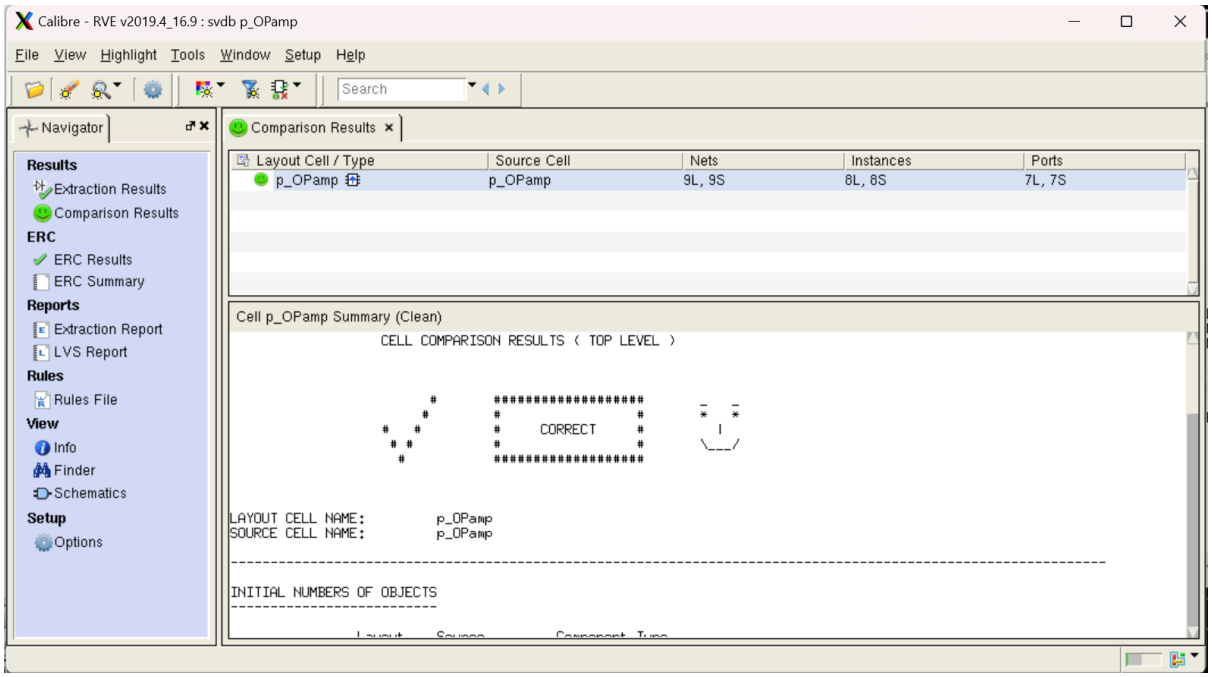

vdd
vdd
idc
idc
vpd
vpd
out
out
/B/vdd
vdd
net3
vpd
net3
out
/B/vdd
/B/vdd
c1
c1
c1
c1
net2
c1
gnd
gnd
/B/gnd
/B/gnd
out

DRC



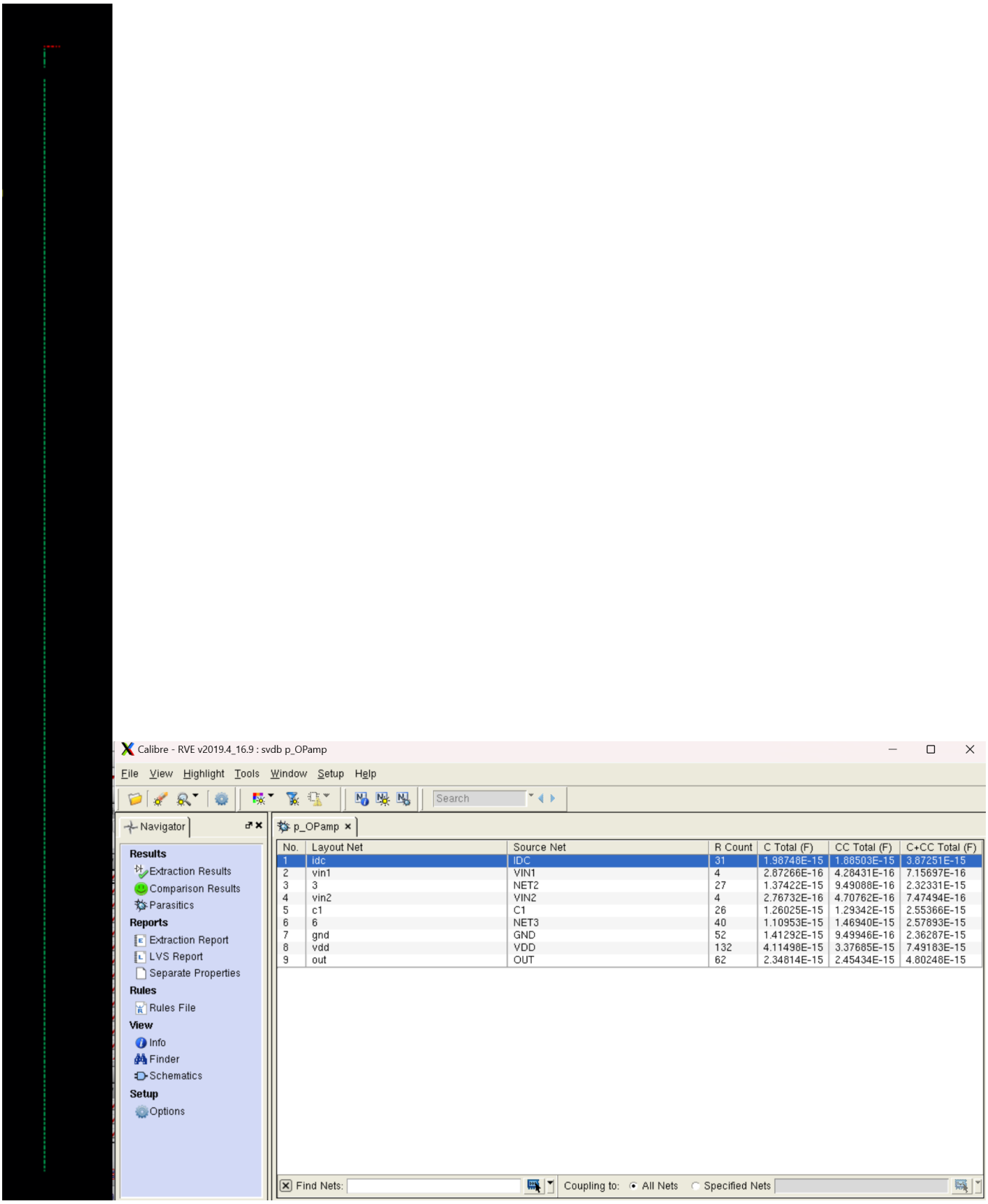
The drc is error free for the layout, the above errors are densty errors which can be ignored.

LVS



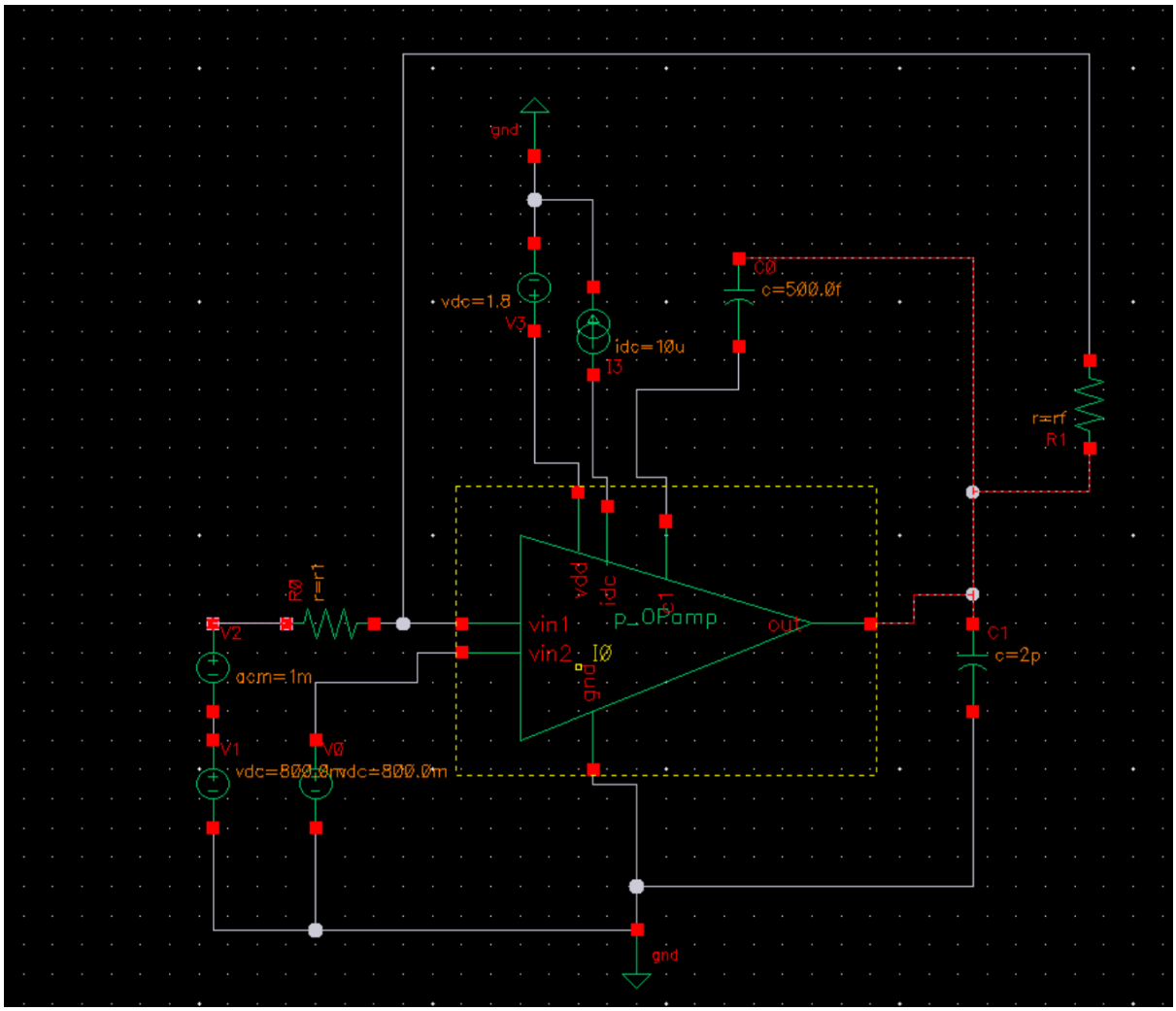
The LVS is correct for the layout without errors.

PEX

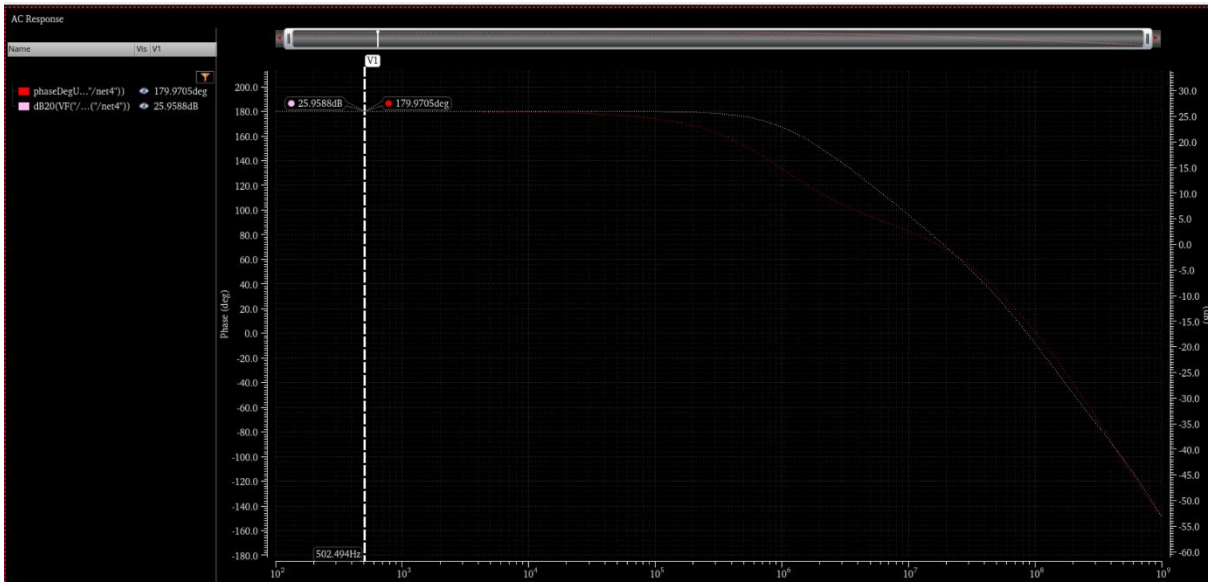


The above 2 images shows the parasitic resistance and capacitances extracted from the layout, the number of parasitics and their values can be seen in the above image.

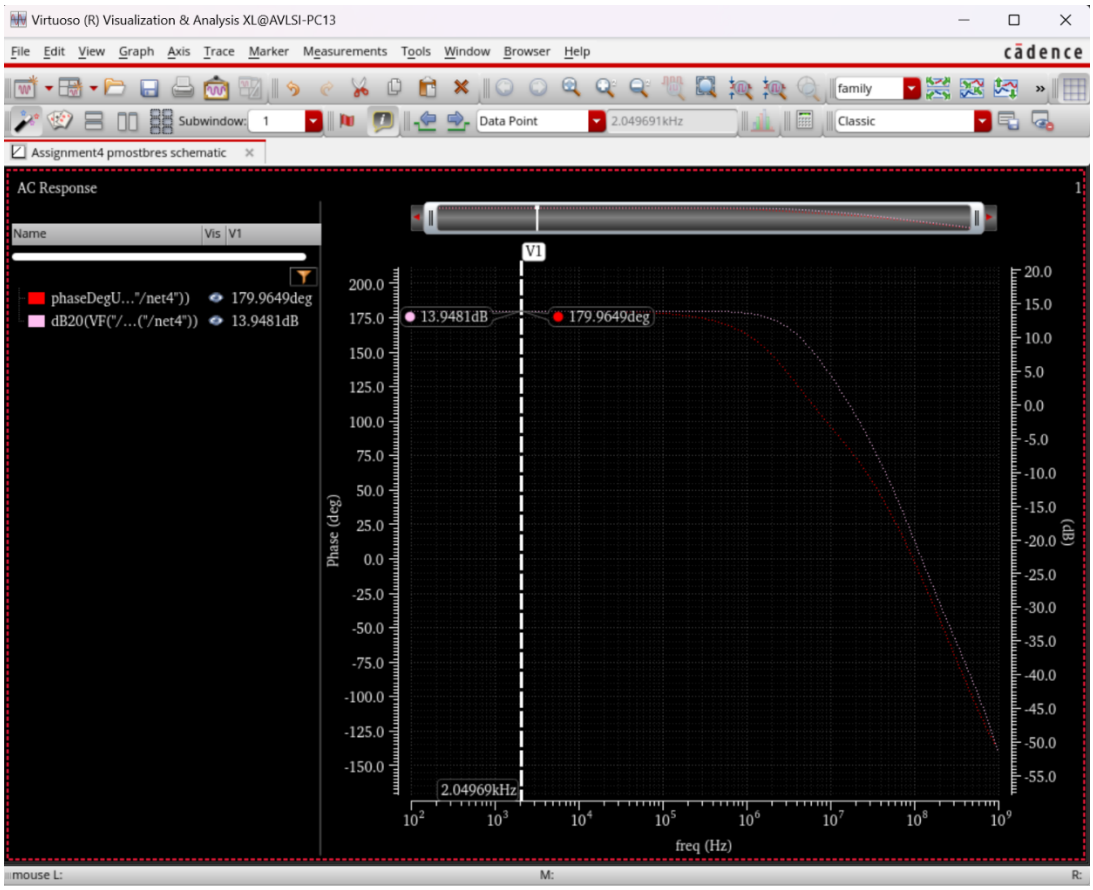
OPAMP inf Negative Feedback

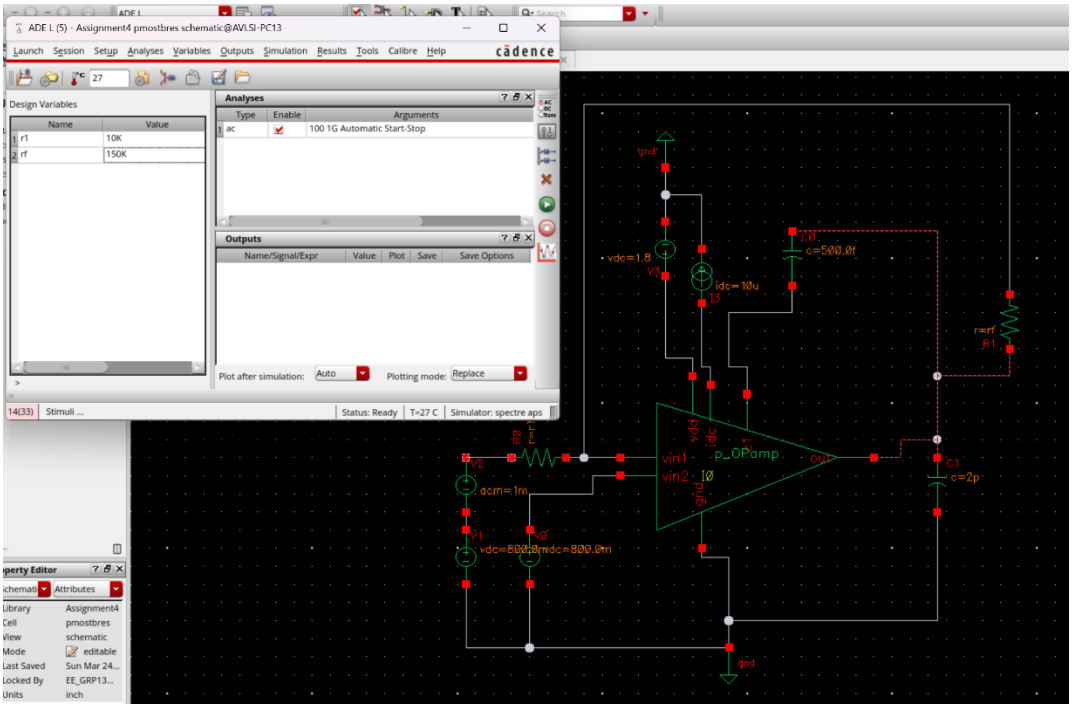


Gain of 5 V/V (14dB) when r1=10k and Rf=50k, so gain = -r1/rf = -5. Which can be seen in the below graph

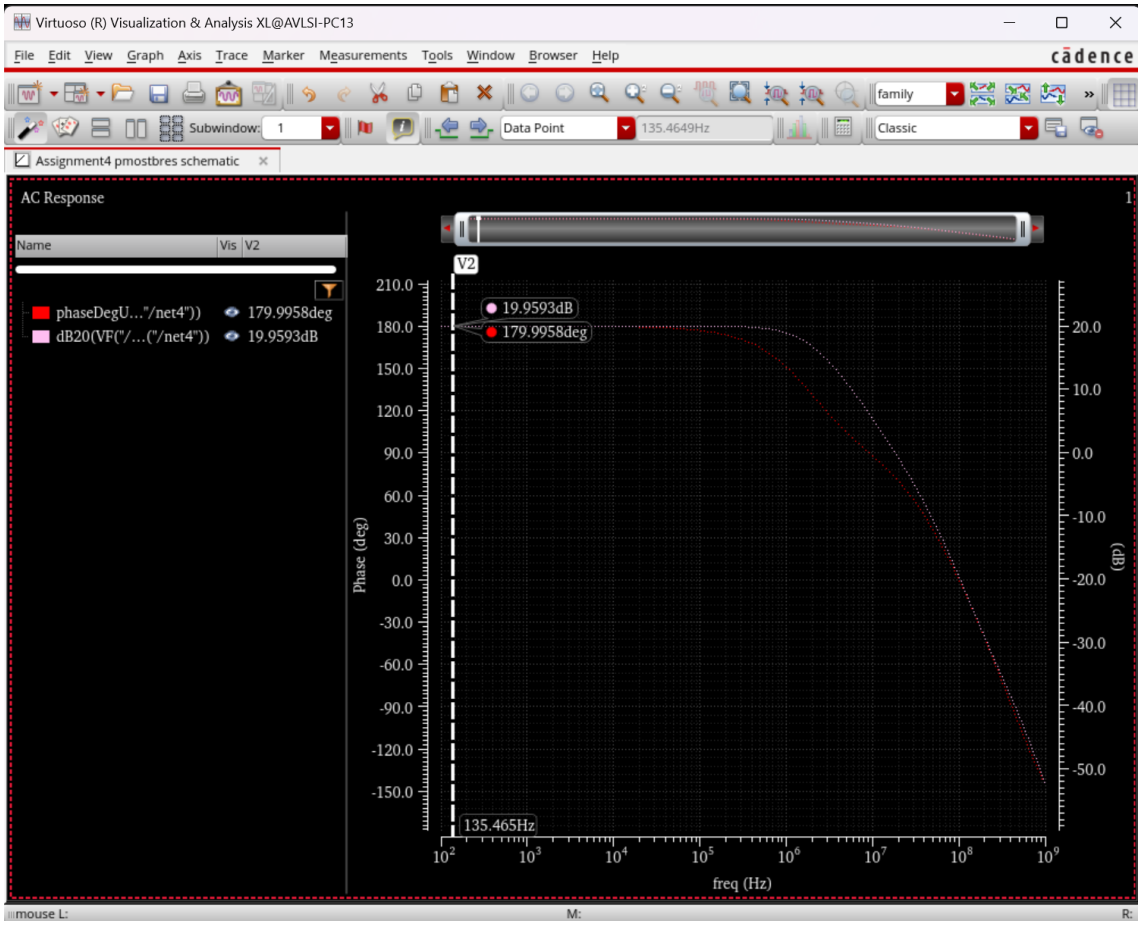


Gain of 10 V/V (20dB) when r1=10k and Rf=110k, so gain = -r1/rf = -10. Which can be seen in the below graph

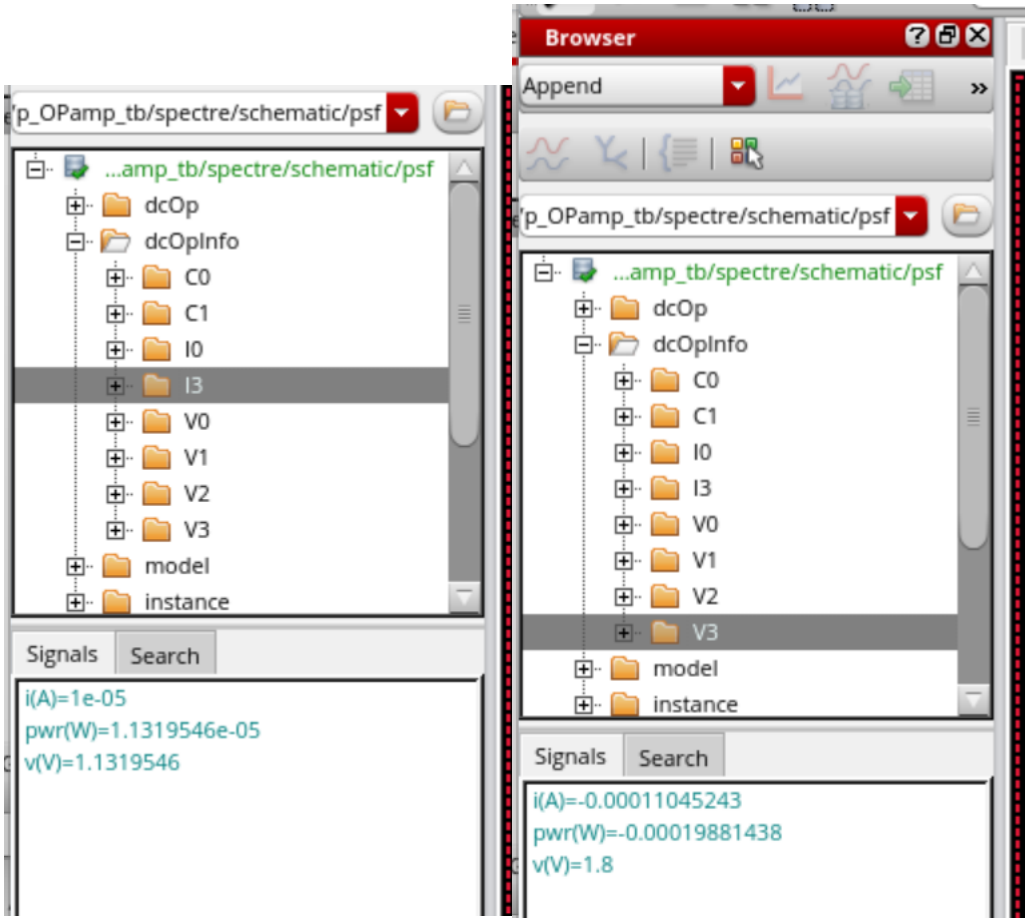




Gain of 20 V/V (24dB) when r1=10k and Rf=200k, so gain = -r1/rf = 20. Which can be seen in the below graph



Power consumption for OPAMP:



The current source and the voltage source (VDD) are the power sources in the circuit, the power consumption = -11.3uW + 0.1mW= 0.1mW