BHARATH INSTITUTE OF SCIENCE AND TECHNOLOGY
DEPARTMENT OF _____

QUESTION BANK

Department : CSE
Program Name/Code : B TECH
Course Name/Code : COMPUTER ORGANAIZATION AND ARCHITECTURE / U20CSCT01

Q.No	Question	Weightage	CO	Bloom's Level
	UNIT I			
	PART – A			
1.	Outline about computer Architecture	2	CO1	2
2.	Compare difference between Computer Architecture and Organization?	2	CO1	2
3.	Show the Functional Components of a computer.	2	CO1	2
4.	Explain digital computer.	2	CO1	2
5.	Summarize about Input Unit	2	CO1	2
6.	Infer the types of output Unit visual, data, print, sound	2	CO1	2
7.	Illustrate Memory Unit of computer	2	CO1	2
8.	Outline about Register.	2	CO1	2
9.	Show the functions of CPU	2	CO1	2
10.	Summarize the functions of ALU	2	CO1	2
	PART – B			
1	Show the various registers and their functions.	4	CO1	2
2	Illustrate block diagram of Control Unit and explain.	4	CO1	2
3	Compare Fetch cycle and Execution Cycle.	4	CO1	2
4	Summarize about memory hierarchy? Cache > register > RAM > secondary storage	4	CO1	2
5	Illustrate the digramatic representation of Instruction cycle state diagram.	4	CO1	2
6	Summarize the Register Indirect mode.	4	CO1	2
7	Explain the key characteristics of Computer Memory Systems	4	CO1	2
8	Outline the basic functional units of a computer with neat sketch	4	CO1	2
9	Relate the knowledge and operation of ALU unit?	4	CO1	2
10	Demonstrate the operations of instruction	4	CO1	2

④a) register is a high-speed memory store unit used in control processing unit (CPU) of a computer
→ The length of the register should be 32-bit
→ memory address saved in multiple register

PART – C				
1	Explain about basic functional blocks of computer.	12	CO1	2
2	Explain about Instruction set architecture.	12	CO1	2
3	Summarize Addressing Mode. Explain any 4 types.	12	CO1	2
4	Classify the types of addressing modes in detail	12	CO1	2
5	Outline the instruction Execution cycle and explain it.	12	CO1	2
6	Show features of register transfer logic with example.	12	CO1	2
7	Summarize the instruction set and its types	12	CO1	2

Instruction architecture is part of abstract mode

PC
AR
INTR
OUTR
DR
TR
AC
IR

Signed bit | is complement of actual binary

Q.No	Question	Weightage	CO	Bloom's Level
	UNIT II			
	PART – A			
1.	Solve the following conversion. Binary to Decimal $(1.00101)_2 \Rightarrow (1.15625)_{10}$	2	CO2	3
2.	Summarize single precision in IEEE 754 format. → 32 bits	2	CO2	2
3.	Outline the phases of pipelining. stage fetch, execute, decode, write back	2	C02	3
4.	Explain the algorithm for restoring division technique .	2	CO2	3
5.	Show the execution unit in pipelining. R, C (Control unit)	2	CO2	2
6.	Classify the types of data hazards. RAW, WAR, WAW	2	C02	2
7.	Explain about Pipelining.	2	CO2	2
8.	Interpret the advantage of pipelining.	2	CO2	3
9.	Summarize about program counter. being executed by current time	2	C02	3
10	Identify the functions of the instruction decoder and control logic.	2	CO2	3
	PART – B			
1	Summarize signed number representation in detail	4	CO2	2
M2	Apply the algorithm and flowchart of Booth's algorithm in detail	4	CO2	3
3	Identify the Fixed and floating point operation in detail	4	C02	2
4.	Organize the ripple carry adder with diagram	4	CO2	3
5.	Construct with example Integer addition and subtraction	4	CO2	3
6.	Solve and explain with example Carry look ahead adder It overcome carry propagation delay	4	C02	3
7	Explain with diagram IEEE 754 format	4	CO2	3
8	Experiment with the execution carry save multiplier	4	CO2	3
9	Explain floating point arithmetic using non restoring algorithm	4	C02	2
M10	Solve 11 divide by 3 using Restoring Division Algorithm	4	CO2	3
	PART – C			
1.	Identify the performance of a pipeline in brief → 3.88	12	CO2	3
(2)	Organize the execution of a complete instruction	12	CO2	3
(3).	Construct ripple carry adder , look -ahead adder with example text diagram	12	C02	3
M 4	Summarize the floating point arithmetic with example	12	CO2	3
5.	Solve integer addition with example	12	CO2	3
M 6	Apply the integer subtraction with example double	12	C02	3
M 7	Explain briefly signed number representation with Example These number require arithmetic sign	12	CO2	3

ripple carry adder → The digital current that produce arithmetic sum of two binary number.
→ It construct full adder connect with carry output

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Q.No	Question	Weightage	CO	Bloom's Level
	UNIT III			
	PART – A			
1.	Summarize about MIPS (million instruction per second)	2	CO3	3
2.	Classify the types of hazards. data, structural, control	2	CO3	3
3.	Construct the stages of pipeline in MIPS architecture.	2	CO3	3
4.	Identify MIPS instruction format coded in binary	2	CO3	3
5.	Illustrate about stalling in pipeline.	2	CO3	3
6.	Outline the construction of data path. (hardware)	2	CO3	3
7.	Summarize about Instruction Fetch	2	CO3	2
8.	Identify Branch Instructions. Jump, call, return	2	CO3	3
9.	Develop control implementation scheme. control sign	2	CO3	3
10.	Summarize Control hazards with example.	2	CO3	3
	It is also known as branch hazard **PART – B**			
11	Explain Implementation of MIPS architecture with multiplexers and control lines Sequence of operations	4	CO3	3
2	Compare between Combinatorial and Sequential elements	4	CO3	3
3	Describe about Building a data path	4	CO3	3
14	Explain the Instruction Fetch with diagram	4	CO3	3
5	Identify the Branch Instruction with diagram	4	CO3	3
6	Build the construction steps for data path.	4	CO3	3
17	Explain about MIPS Architecture.	4	CO3	2
8	Utilize the implementation scheme of control lines with diagram.	4	C03	3
91	Explain different types of hazards that occur in a pipeline.	4	CO3	2
110	Construct the MIPS implementation in detail with advantages and disadvantages.	4	CO3	3
	★ MIPS **PART – C**			
1.	Explain in detail in pipeline and its Execution	12	CO3	2
(2)	Develop in detail about control implementation Scheme	12	CO3	3
3	Explain in detail Instruction Fetch in brief register, load & store, branch	12	CO3	2
4	Organize the MIPS Architecture	12	CO3	3
5	Apply Implementation scheme with control lines with diagram	12	CO3	3
(6)	Illustrate throughput and speed up with appropriate formula.	12	CO3	3
7	Demonstrate data path implementation scheme with appropriate diagrams.	12	CO3	2

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Q.No	Question	Weightage	CO	Bloom's Level
	UNIT IV			
	PART – A			
01.	Summarize the Parallelism.	2	CO4	2
2.	Identify the limitations of multicore processor.	2	CO4	3
3.	Classify the types of Flynn's taxonomy. SISD, SIMD, MISD, MIMD	2	CO4	2
04	Show the challenges in parallel processing?	2	CO4	2
5.	Identify the main difference in SIMD and GPU	2	CO4	3
6.	Organize the features of GPU.	2	CO4	3
07	Explain the influence of instruction sets.	2	CO4	2
8	Explain about graphics processing unit. → single chip processor	2	CO4	2
9	Build the MIMD instruction architecture and explain	2	CO4	3
10	Classify the categories of Flynn's taxonomy.	2	CO4	3
	PART – B			
1	Explain about the architecture of multi-core processor.	4	CO4	2
2	Construct GPU architecture and explain with GPU pipeline.	4	CO4	3
3	Classify the parallel machine. Define different types of parallel machine (block diagram, example).	4	CO4	3
4	Explain about graphics card in parallel processing.	4	CO4	2
5	Illustrate Instruction Level Parallelism.	4	CO4	3
6	Explain about parallel processing.	4	CO4	2
7	Classify organisation of computers using Flynn's criteria.	4	CO4	3
8	Compare CPU and GPU.	4	CO4	2
9	Explain the working principles of GPU	4	CO4	2
10	Explain the challenges of parallel processing	4	CO4	2
	PART – C			
11	Explain the categories of Flynn's taxonomy.	12	CO4	2
12	Build the architecture of multi-core processor.	12	CO4	3
3	Experiment with Instruction Level Parallelism.	12	CO4	3
4	Construct the Parallel processors with neat diagram	12	CO4	3
15	Outline the applications of GPU in brief	12	CO4	3
16	Organize the taxonomy of parallel computers.	12	CO4	3
17	Develop GPU architecture with its configuration.	12	CO4	3

Garbage collection
memory allocation
locality issue
load balancing

Feature of GPU
1) 2D or Three D
2) MPEG coding
3) Texture maping
4) Hard ware overlaps
5) Digital o/p to flat panel

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Q.No	Question	Weightage	CO	Bloom's Level
	UNIT V			
	PART – A			
1	Analyse cache. Temporary memory	2	CO5	4
2	Examine the term TLB? Translation of virtual memory address of physical	2	CO5	4
3	Categorize static memories? RAM, DRAM, SRAM, PROM	2	CO5	4
4	Discover the Hit Ratio. no: of cache hites / Total no of caches	2	CO5	4
5	Compare SRAM and DRAM?	2	CO5	4
6	Simplify the usage of USB in modern world.	2	CO5	4
7	List out the types of data transfer techniques used with IO interface? DMA, memory map, serial communication	2	CO5	4
8	Analyse the flash memory? non volatile storge technology	2	CO5	4
9	List the advantages of write through cache.	2	CO5	4
10	Inspect the disk controller? it control flow of data between storage devices	2	CO5	4
	PART – B			
1	Examine about TLB.	4	CO5	4
2	List the difference between static RAM and dynamic RAM.	4	CO5	4
3	Function about USB with neat architecture.	4	CO5	4
4	Examine Direct Memory Access.	4	CO5	4
5	Relationship between CPU registers, Main memory, Secondary memory and cache memory?	4	CO5	4
6	Examine about various exceptions.	4	CO5	4
7	Analyse memory interleaving?	4	CO5	4
8	Organize the characteristics of some common memory technologies.	4	CO5	3
9	Analyse virtual memory? Discuss how paging helps in implementing virtual memory.	4	CO5	4
10	Inference about interrupts? How are they handled?	4	CO5	4
	PART – C			
1	Dissect about direct and set associative map technique in cache	12	CO5	4
2	Develop how I/O devices can be interfaced with a block diagram	12	CO5	3
3	Construct and explain central storage unit.	12	CO5	3
4	Utilize virtual memory and how it used efficiently in Computer system	12	CO5	3
5	Identify the various types of semiconductor RAMs in detail?	12	CO5	3
6	Analyse the DMA operation? State its advantages?	12	CO5	4
7	Inspect SCSI and USB in computer organization in brief ?	12	CO5	4

(3) main memory of the Computer is known as central storage unit
two different RAM
1) static
2) Dynamic