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Sec 1

Project 1

Spring 2017

`include "full\_addA.v"

`include "full\_addB.v"

`include "full\_addD.v"

`include "full\_addE.v"

module Test();

reg x, y, z;

wire cout;

//full\_addA fa1(x,y, z, cout);

//full\_addB fa2(x,y, z, cout);

//full\_addD fa3(x,y, z, cout);

full\_addE fa4(x,y,z, cout);

initial begin

$display("time x, y, z, cout");

$monitor("%4d %b", $time, cout);

x= 0; y= 0; z= 0; $display("%4d %b %b %b", $time, x,y, z);

#1

x=0; y= 0; z= 1; $display("%4d %b %b %b", $time, x,y,z);

#1

x=0; y=1; z=0; $display("%4d %b %b %b", $time, x, y, z);

#1

x= 0; y=1; z=1; $display("%4d %b %b %b", $time, x, y, z);

#1

x= 1; y=0; z=0; $display("%4d %b %b %b", $time, x, y, z);

#1

x=1; y=0; z=1; $display("%4d %b %b %b", $time, x, y, z);

#1

x=1; y=1; z=0; $display("%4d %b %b %b", $time, x, y, z);

#1

x=1; y=1; z=1; $display("%4d %b %b %b", $time, x, y, z);

#1

$finish;

end

endmodule

module full\_addA

(

input x, y, z,

output cout

);

wire out1, out2, ans, ny;

or o1(out1, x,y);

not not1(ny,y);

or o2(out2, ny, z);

and and1(ans,out1, out2);

endmodule

Chronologic VCS simulator copyright 1991-2014

Contains Synopsys proprietary information.

Compiler version I-2014.03-2; Runtime version I-2014.03-2; Mar 8 13:21 2017

time x, y, z, cout

0 0 0 0

1 0 0 1

2 0 1 0

3 0 1 1

4 1 0 0

5 1 0 1

6 1 1 0

7 1 1 1

$finish called from file "test.v", line 32.

$finish at simulation time 8

V C S S i m u l a t i o n R e p o r t

Time: 8

CPU Time: 0.540 seconds; Data structure size: 0.0Mb

Wed Mar 8 13:21:27 2017

module full\_addB

(

input x, y, z,

output cout

);

wire out1, out2, ans, ny;

nor or1(out1, x,y);

not not1(ny,y);

nor or2(out2, ny, z);

nor and1(ans,out1, out2);

endmodule

Chronologic VCS simulator copyright 1991-2014

Contains Synopsys proprietary information.

Compiler version I-2014.03-2; Runtime version I-2014.03-2; Mar 8 13:21 2017

time x, y, z, cout

0 0 0 0

0 z

1 0 0 1

2 0 1 0

3 0 1 1

4 1 0 0

5 1 0 1

6 1 1 0

7 1 1 1

$finish called from file "test.v", line 32.

$finish at simulation time 8

V C S S i m u l a t i o n R e p o r t

Time: 8

CPU Time: 0.560 seconds; Data structure size: 0.0Mb

Wed Mar 8 13:21:58 2017

module full\_addD

(

input x, y, z,

output cout

);

wire out1, out2, ans, ny;

assign cout= (x|y)&(~y|z);

endmodule

Chronologic VCS simulator copyright 1991-2014

Contains Synopsys proprietary information.

Compiler version I-2014.03-2; Runtime version I-2014.03-2; Mar 8 13:24 2017

time x, y, z, cout

0 0 0 0

0 z

1 0 0 1

2 0 1 0

3 0 1 1

4 1 0 0

5 1 0 1

6 1 1 0

7 1 1 1

$finish called from file "test.v", line 32.

$finish at simulation time 8

V C S S i m u l a t i o n R e p o r t

Time: 8

CPU Time: 0.510 seconds; Data structure size: 0.0Mb

Wed Mar 8 13:24:48 2017

module full\_addE

(

input x, y, z,

output reg cout

);

always@(x or y or z)

begin

case({x,y , z})

3 'b000: begin cout = 0; end

3 'b001: begin cout = 0; end

3 'b010: begin cout = 0; end

3 'b011: begin cout = 1; end

3 'b100: begin cout = 1; end

3 'b101: begin cout = 1; end

3 'b110: begin cout = 0; end

3 'b111: begin cout = 1; end

default: begin cout= 0; end

endcase

end

endmodule

Chronologic VCS simulator copyright 1991-2014

Contains Synopsys proprietary information.

Compiler version I-2014.03-2; Runtime version I-2014.03-2; Mar 8 13:25 2017

time x, y, z, cout

0 0 0 0

0 z

1 0 0 1

2 0 1 0

3 0 1 1

4 1 0 0

5 1 0 1

6 1 1 0

7 1 1 1

$finish called from file "test.v", line 32.

$finish at simulation time 8

V C S S i m u l a t i o n R e p o r t

Time: 8

CPU Time: 0.540 seconds; Data structure size: 0.0Mb

Wed Mar 8 13:25:56 2017

All the results look the same. They are all consistent. Im assuming one of them is correct so they all describe it well because they were all intended to be the same.