Lab 4 answer:

	EX				EX			WB	
Instruction	**RegDst**	**ALUOp1**	**ALUOp0**	**ALUSrc**	**Branch**	**MemRead**	**MemWrite**	**RegWr**	**MemtoReg**
R-format	1	1	0	0	0	0	0	1	0
lw	0	0	0	1	0	1	0	1	1
sw	x	0	0	1	0	0	1	0	x
beq	x	0	1	0	1	0	0	0	x
I-format	0	1	*	1	0	0	0	1	0
addi	1	0	0	1	0	0	0	1	0

*depends on the operation

Instruction-time diagram

	C1	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**	**C9**	**C10**	**C11**	**C12**	**C13**	**C14**
slt	IF	ID	EX	MEM	WB									
la		IF	ID	EX	MEM	WB								
lb			IF	ID	EX	MEM	WB							
lb				IF	ID	EX	MEM	WB						
xori					IF	ID	EX	MEM	WB					
andi						IF	ID	EX	MEM	WB				
xor							IF	ID	EX	MEM	WB			
bne								IF	ID	EX	MEM	WB		
slti									IF	ID	EX	MEM	WB	
sw										IF	ID	EX	MEM	WB

Datapath and control signals for Cycle 9: