الجامعة الإسلامية العالمية ماليزيا
INTERNATIONAL ISLAMIC UNIVERSITY MALAYSIA
يونيورسيتي إسلام انتارابغسا ملايسيا
Garden of Knowledge and Virtue

DATE: 28-APR-2021

Lab Exercise - 3

COMPUTER ARCHITECTURE & ASSEMBLY LANGUAGE

Course: CSC-3402, **Sec:** 02

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Submitted by:

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Multicycle Processor Datapath

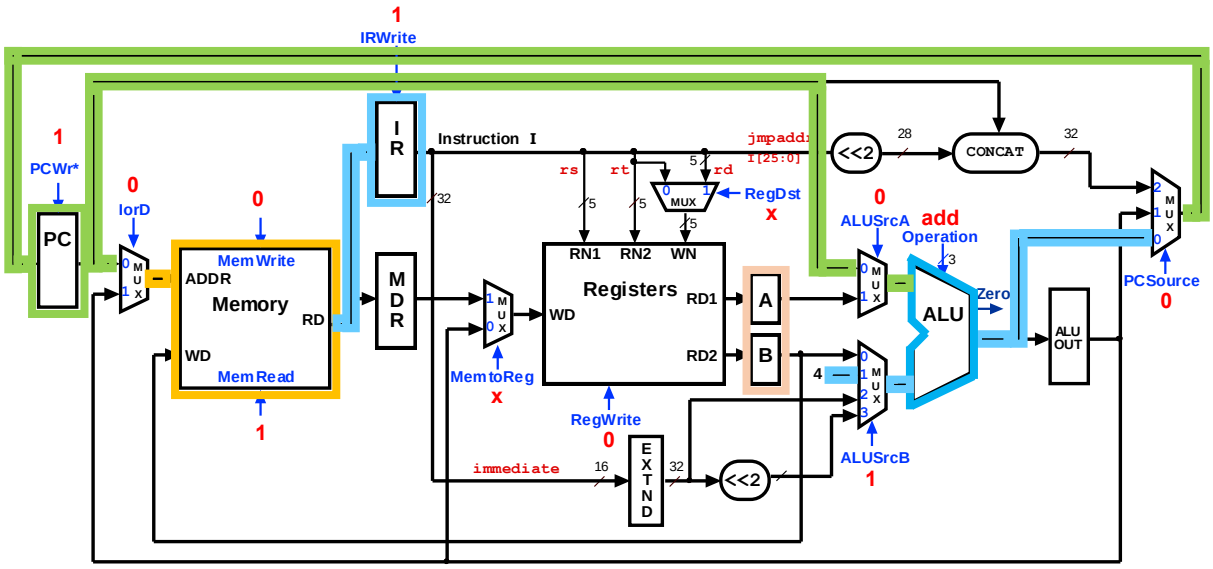

Figure 1 addi instruction

RTL Statement for Figure 1: 1. IF; 2. IR = Memory[PC]; 3. PC = PC+4

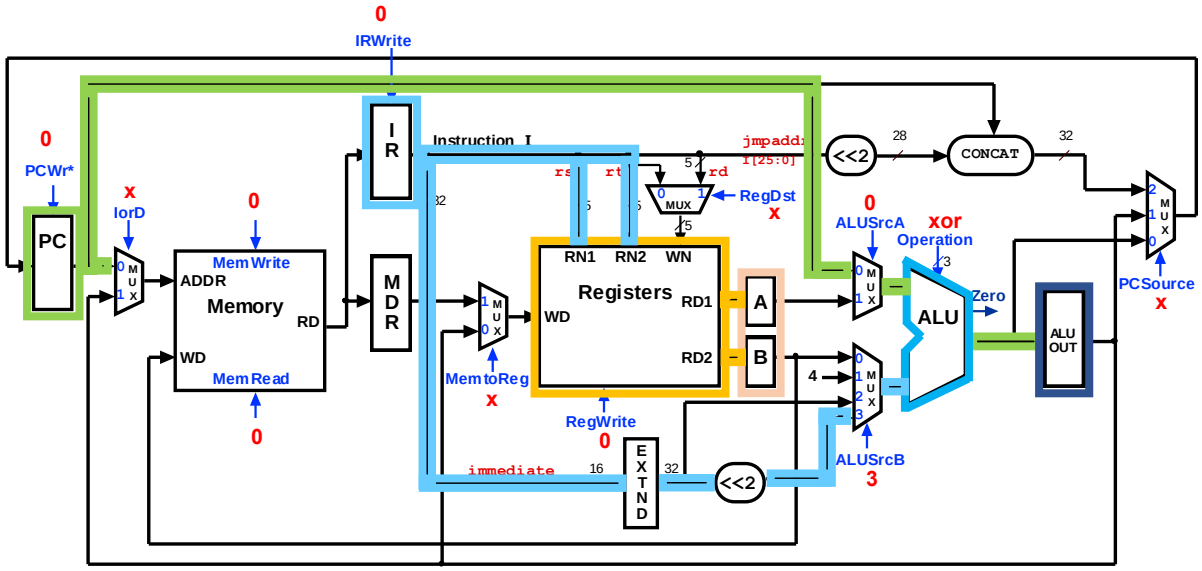

Figure 2 xor instruction

RTL Statement for Figure 2:

1. ID
2. A = Reg[IR[25-21]], B = Reg[IR[20-16]]
3. ALUOut = PC + (sign-extend(IR[15-0] <<2)

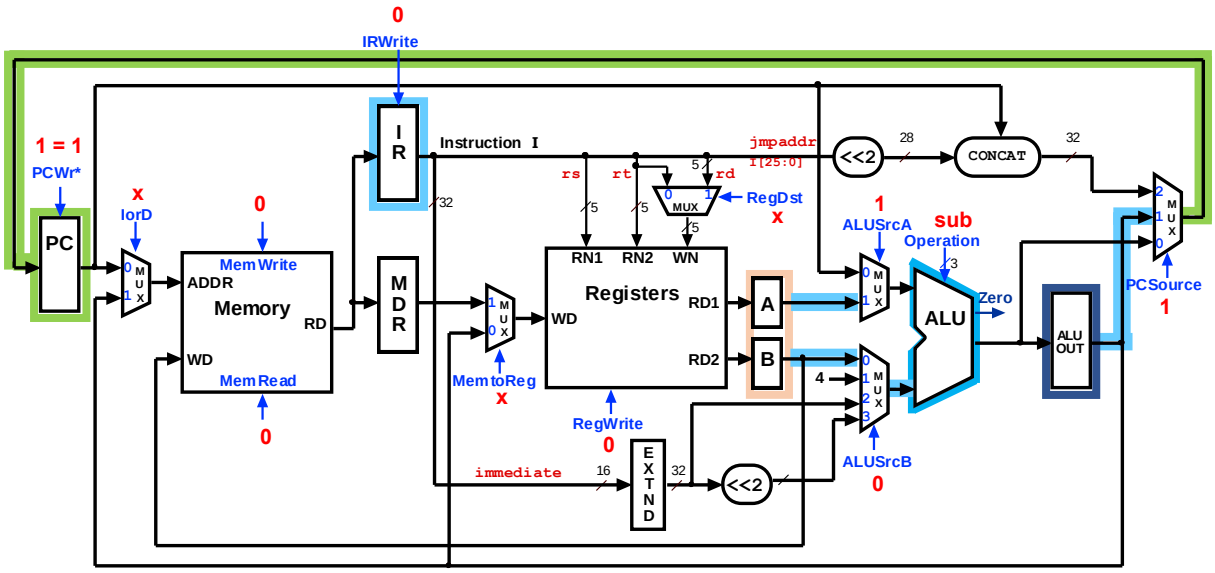

Figure 3 beq Instruction

RTL Statement for Figure 3: 1. Execution Branch; 2. if(A==B) then PC =ALUOut

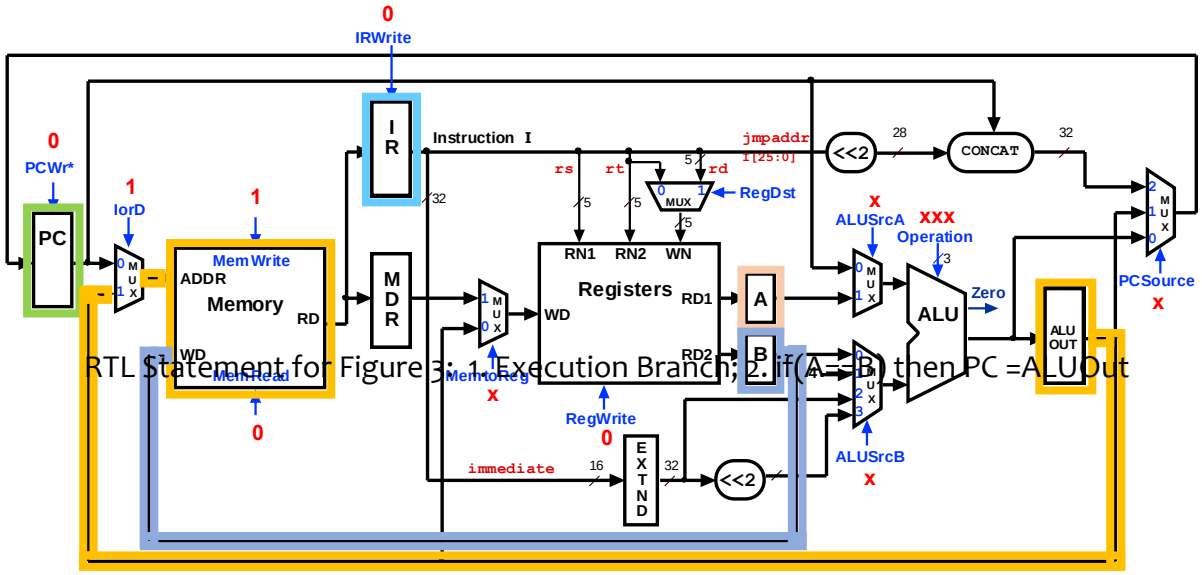

Figure 4 sw instruction

RTL Statement for Figure 4: 1. Memory access completion; 2. Memory[ALUOut] = B;

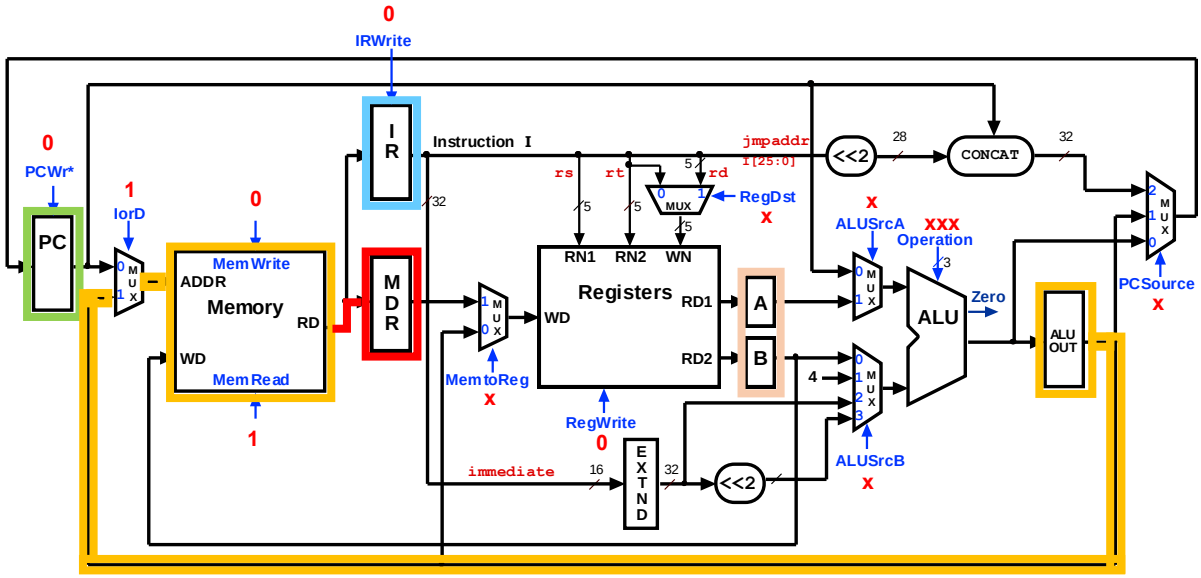

Figure 5 lw instruction

RTL Statement for Figure 5: 1. Memory read completion; 2. MDR = Memory[ALUOut];