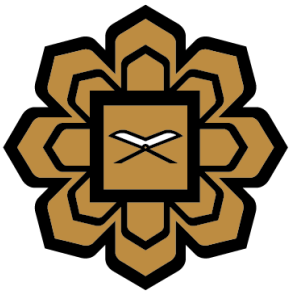


الجامعة الإسلامية العالمية ماليزيا
INTERNATIONAL ISLAMIC UNIVERSITY MALAYSIA
يونيورسيتي إسلام انتارابغسا ملايسيا
Garden of Knowledge and Virtue

DATE: 21-APR-2021

Lab Exercise - 2

COMPUTER ARCHITECTURE & ASSEMBLY LANGUAGE

Course: CSC-3402, **Sec:** 02

Lecturer: Dr. HAFIZAH BINTI MANSOR

Submitted by:

Name: Hasan Tanveer Mahmood
Matric no: 1725413

Single Cycle Processor:

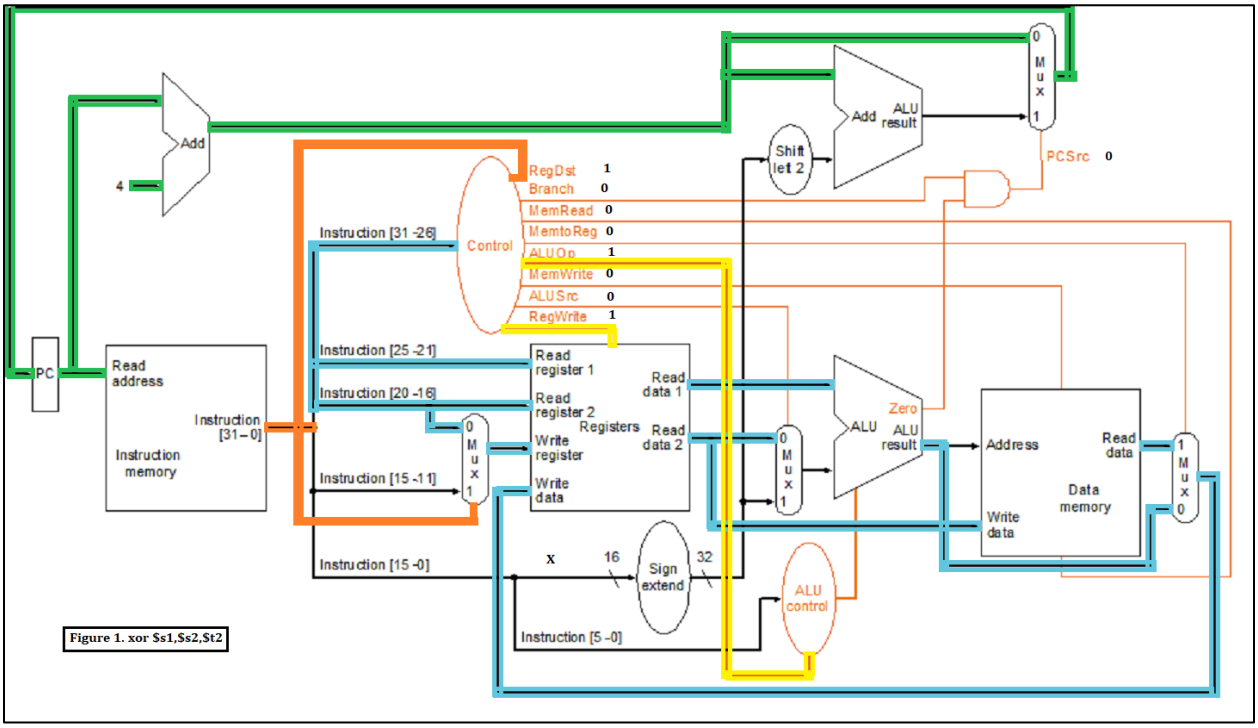


Figure 1: xor $s1,$s2,$t2

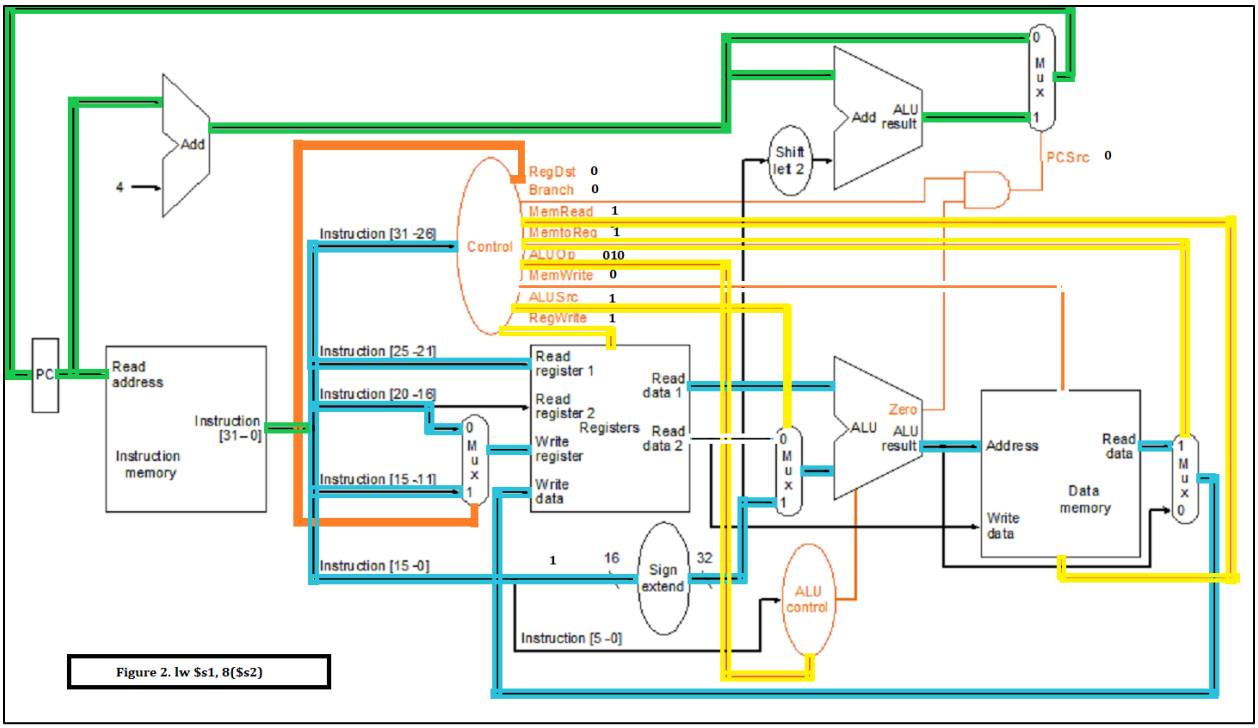


Figure 2: lw $s1, 8($s2)

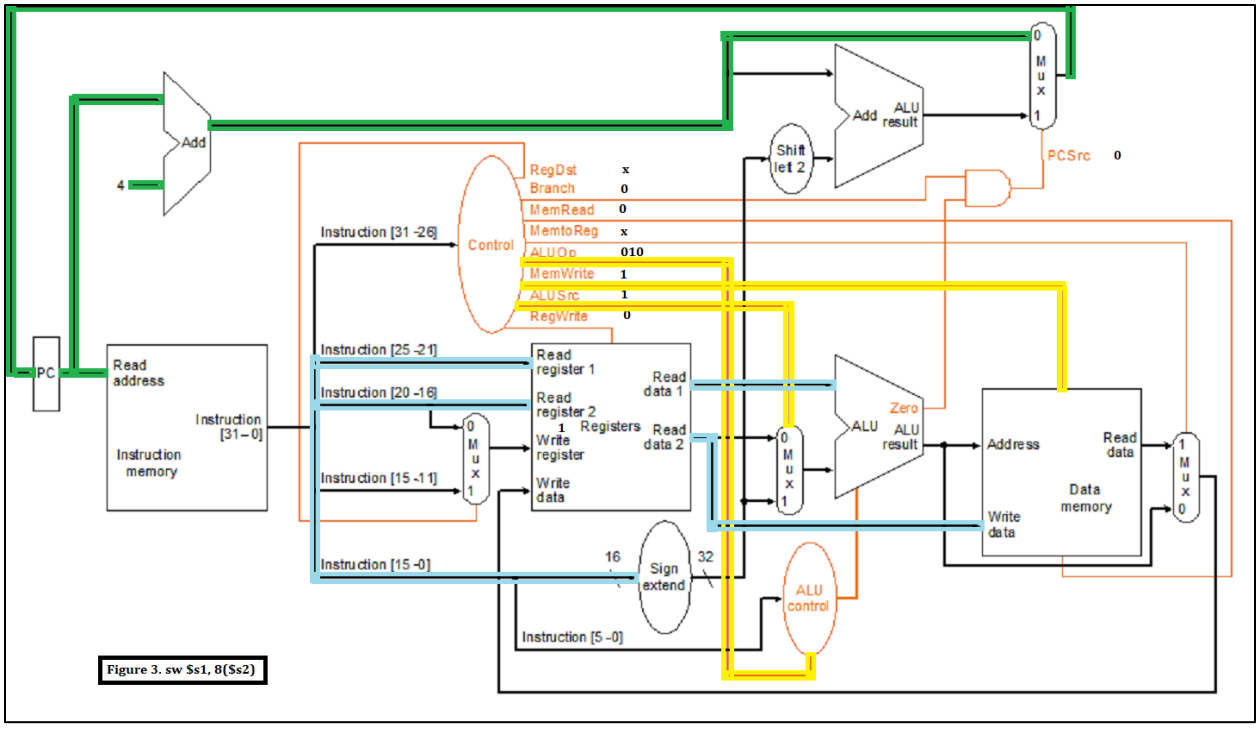


Figure 3: sw $s1, 8($s2)

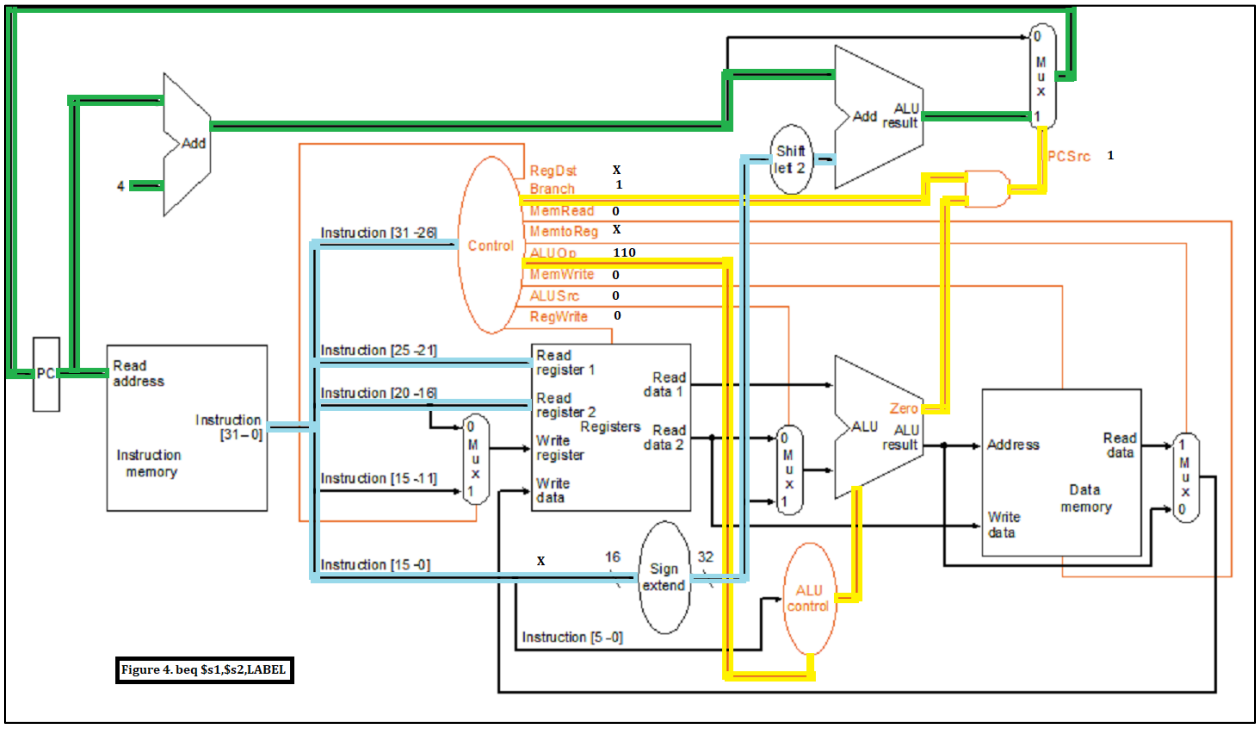


Figure 4: beq $s1,$s2,LABEL

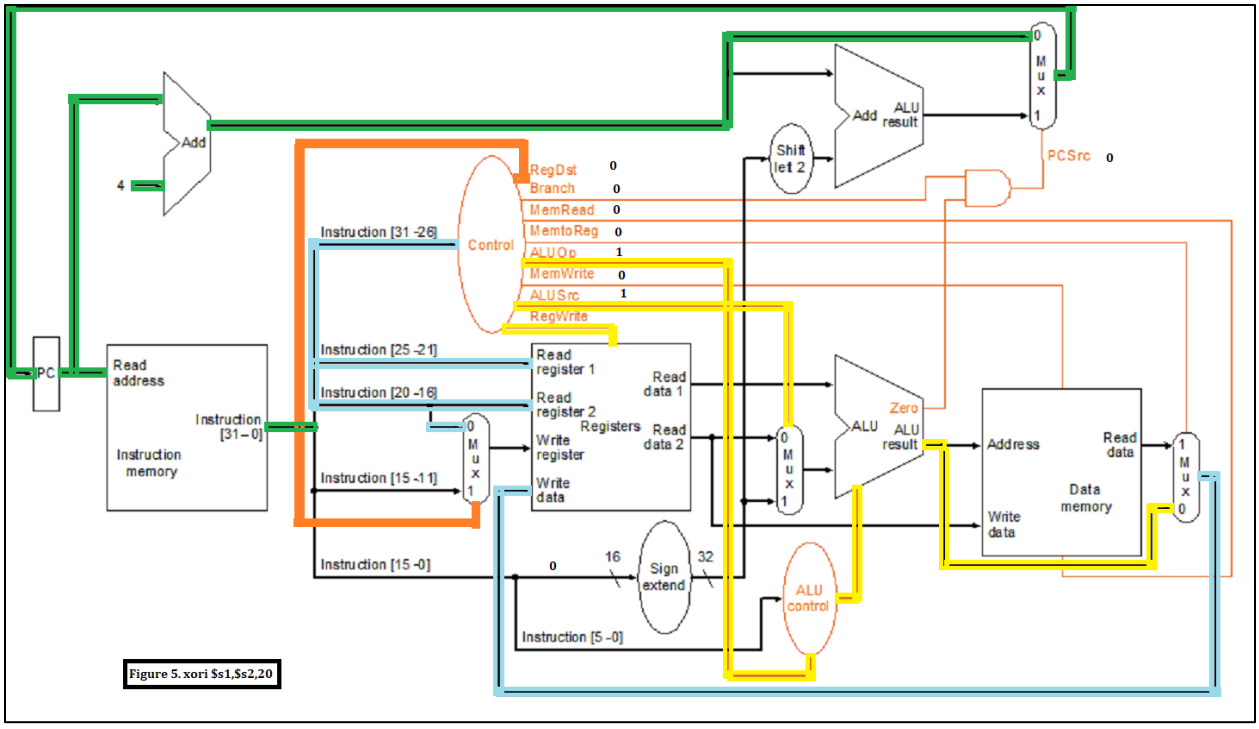
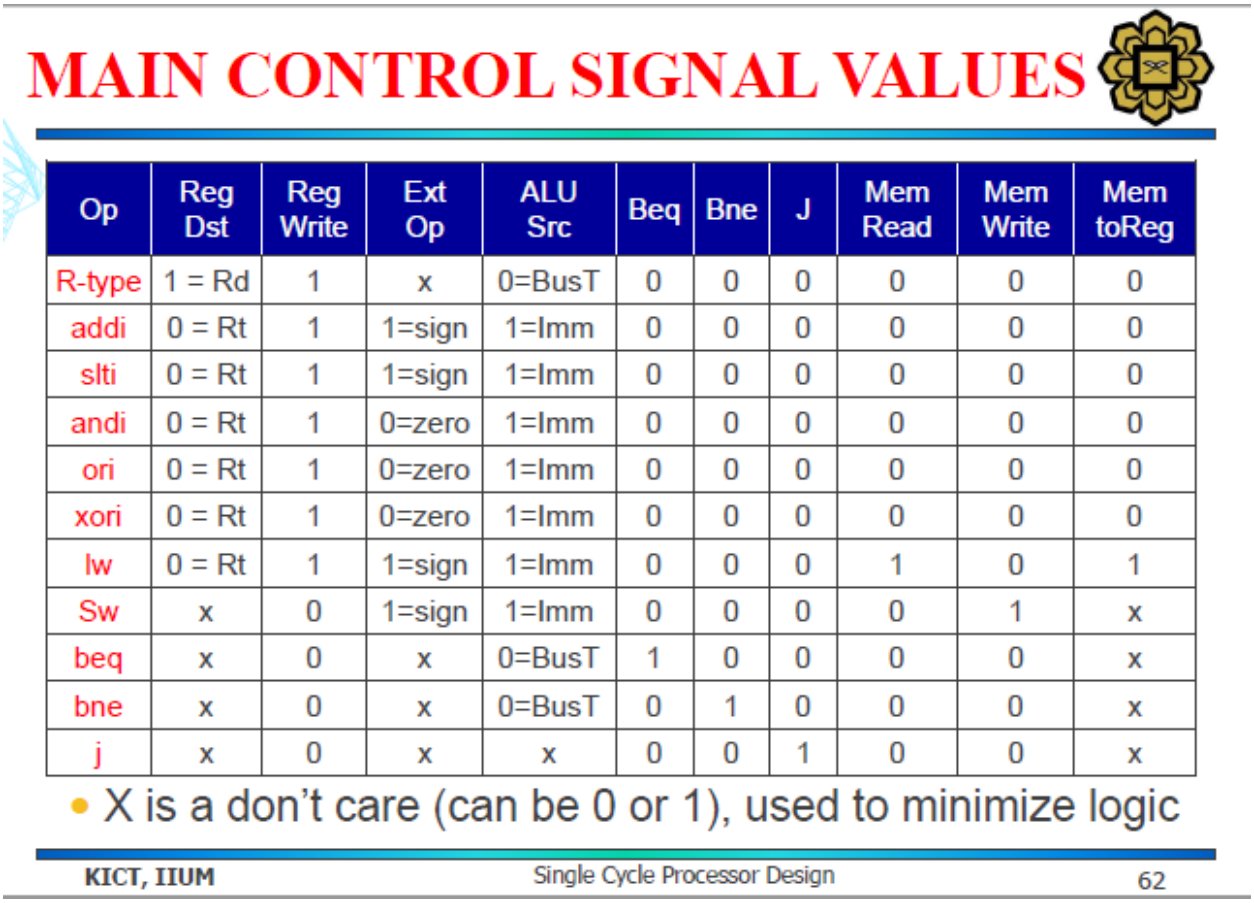


Figure 5. xori $s1,$s2,20

Figure 5: xori $s1,$s2,20

References:

- **For Control Signal Value I took references from:**



MAIN CONTROL SIGNAL VALUES

Op	Reg Dst	Reg Write	Ext Op	ALU Src	Beq	Bne	J	Mem Read	Mem Write	Mem toReg
R-type	1 = Rd	1	x	0=BusT	0	0	0	0	0	0
addi	0 = Rt	1	1=sign	1=Imm	0	0	0	0	0	0
slti	0 = Rt	1	1=sign	1=Imm	0	0	0	0	0	0
andi	0 = Rt	1	0=zero	1=Imm	0	0	0	0	0	0
ori	0 = Rt	1	0=zero	1=Imm	0	0	0	0	0	0
xori	0 = Rt	1	0=zero	1=Imm	0	0	0	0	0	0
lw	0 = Rt	1	1=sign	1=Imm	0	0	0	1	0	1
Sw	x	0	1=sign	1=Imm	0	0	0	0	1	x
beq	x	0	x	0=BusT	1	0	0	0	0	x
bne	x	0	x	0=BusT	0	1	0	0	0	x
j	x	0	x	x	0	0	1	0	0	x

- X is a don't care (can be 0 or 1), used to minimize logic

KICT, IIUM Single Cycle Processor Design 62