

---

## ***INTERIM REPORT***

---

### **Group project name:**

Digital logic circuit simulator

<b>Group Members</b>	<b>Roll numbers</b>
1. Parikh Smit Hemanshu	202501404
2. Dhrishit Bhavin Rajde	202501405
3. Makwana Pratham Jatinkumar	202501406
4. Neil Doshi	202501407
5. Tanvi Gami	202501408
6. Atharva Dave	202501409
7. Parva Sanket Sheth	202501410
8. Patel Yug Rajnikant	202501411
9. Desai Krish Yogeshkumar	202501412
10. Bhimani Meet Prakashbhai	202501413

### **Digital Logic Circuit Simulator:**

---

A digital logic circuit simulator is a software tool that allows us to design, build, and test circuits using logic gates such as NOT, AND, OR, NAND, NOR, and

XOR. It enables users to analyse and verify circuit behaviour virtually, without the need for physically connecting wires or components.

## **Functionalities in our project:**

---

The functionalities that we have decided to include in our project are as below along with their brief description:

### **1. Logic Gate Evaluation**

- i. Each gate type (AND, OR, NOT, XOR, NAND, NOR) is represented by a dedicated function that takes input values and returns the correct logical output.
  - ii. The program evaluates user inputs for each gate and computes the output according to the logic conditions defined.
- 

### **2. Basic Functionalities**

- i. Add new logic gates to the workspace.
  - ii. Run and test the circuit simulation in real-time.
  - iii. Display output values instantly based on user input changes.
- 

### **3. Simple User Input Interface**

- i. Enables user interaction through keyboard and mouse input for adding gates, wiring, and simulating.

- ii. Allows drag and drop of logic gates onto the workspace.
  - iii. Connects gates using virtual wires.
  - iv. Toggles input switches and view the output through LEDs.
- 

#### **4. Automatic Truth Table Generator**

- i. Automatically generates and prints the truth table based on user-defined gate connections and circuit configuration.
  - ii. Displays all possible combinations of input states with corresponding outputs.
- 

#### **5. Input / Output Elements (Input Toggle, Output LED)**

- i. **Input Toggle:** Acts as an on/off switch (0 or 1) for providing binary inputs to the circuit.
  - ii. **Output LED:** Visually displays the result of circuit evaluation (ON = 1, OFF = 0).
- 

#### **6. Error Handling**

- i. Detects and highlights errors made by the user (invalid connections, missing inputs, etc.).
  - ii. Checks for logic loops or improper wiring structures.
  - iii. Displays clear error messages for easy correction.
-

## **7. Selection / Deletion**

- i. Selection Tool: Select components or wires to modify or move them.
  - ii. Deletion Tool: Remove unwanted components or connections.
- 

## **8. Undo / Redo System**

- i. Enables users to undo the most recent action performed.
- ii. Supports redo operation to restore the previously undone step.
- iii. Maintains user-friendly interaction through action history.

Functionalities	People doing it
Logic gate evaluation	Dhrishit Rajde
Basic Functionalities	Atharva Dave
Simple user input interface	Smit Parikh and Tanvi Gami
Automatic truth table generator	Pratham Makwana
Input and output elements	Yug Patel
Error Handling	Parva Sheth
Selection deletion	Neil Doshi
Undo/Redo system	Krish Desai and Meet Bhimani

## **Project Flow (Overview)**

---

1. User Interface Setup → Create a workspace for circuit design.
2. Gate Placement → Users drag and drop gates and connect them with virtual wires.
3. Input Assignment → Binary inputs are toggled using switches.
4. Circuit Evaluation → Logical outputs are computed dynamically.
5. Output Display → Results are shown on LEDs or in a truth table.
6. Error Checking → Invalid connections and missing links are flagged.
7. Editing Options → Users can select, delete, undo, or redo actions.

---

## **Group meets held till now**

---

Till now we have had 2-3 group meets where we decided upon the functionalities that we are going to use alongside the distribution of the people going to do the tasks.

Now since we are divided into smaller groups of 2, we are planning that each of the smaller group will meet up according to their own time and reach out their way of approach.

Additionally, we have set internal deadlines to complete the work on time.