Birla Institute of Technology and Science Pilani
CS F342 Computer Architecture
Second Semester 2020-21
Lab Sheet– 1 (09th Feb. 2021)

Dataflow Modeling Style

In today's lab we shall implement a few combinational circuits which we have studied in digital design using dataflow modeling style and verify their functionality using a suitable test bench prepared using Behavioral Modeling.

Learning Outcome: By the end of this lab. session the learner will be able to

- Implement a combinational circuit design using data flow modeling in Verilog HDL.
- List various operators and their function in Verilog HDL.
- Use the conditional operator effectively in implementing digital systems in Verilog HDL.
- Use concatenation operator and its application in modeling shift and rotate operations.
- Write effective test cases for verifying a design in HDL.
- Simulate and debug the HDL code on a simulator.

Exercise Problems

1. Implement a full adder.
2. Implement a 4:1 Multiplexer using single statement.
3. A combinational circuit is to be implemented such that it can perform various shift operations as listed below. The input is *A* which is a 8-bit number, other input is *Opcode* a 3-bit number. The output is *Y* a 8-bit number. *Use Concatenation Operator*.

S.No.	Function Name & Opcode	Operation
1.	SHL (001)	Shift left input A by 1-bit and fill LSB with 0
2.	SHR (100)	Shift right input A by 1-bit and fill MSB with 0
3.	SAR (101)	Shift right input A by 1-bit and fill MSB with MSB
4.	ROL (010)	Rotate input A Left by 1-bit
5.	ROR (110)	Rotate input A Right by 1-bit

4. Given two BCD numbers each 2-digit, implement a BCD multiplier. Let the two BCD numbers be denoted as ***JKH*** and ***LMH***. The product is a 4-digit BCD number *PQRSH*. (H indicates Hex Mode). Develop a suitable test bench to test this BCD multiplier.

****** The End ******

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