Birla Institute of Technology and Science Pilani
CS F342 Computer Architecture
Second Semester 2020-21
Lab Sheet– 5 (23rd March 2021)

System Level Design

Implement a 8 bit multiplier using a four bit multipliers and a suitable adder.

1. Use necessary hardware to finish the job in a ***single clock cycle***.
2. Use only a single multiplier and a single adder ***multi-cycle implementation.***
3. Use ***Pipelined*** approach for this problem.

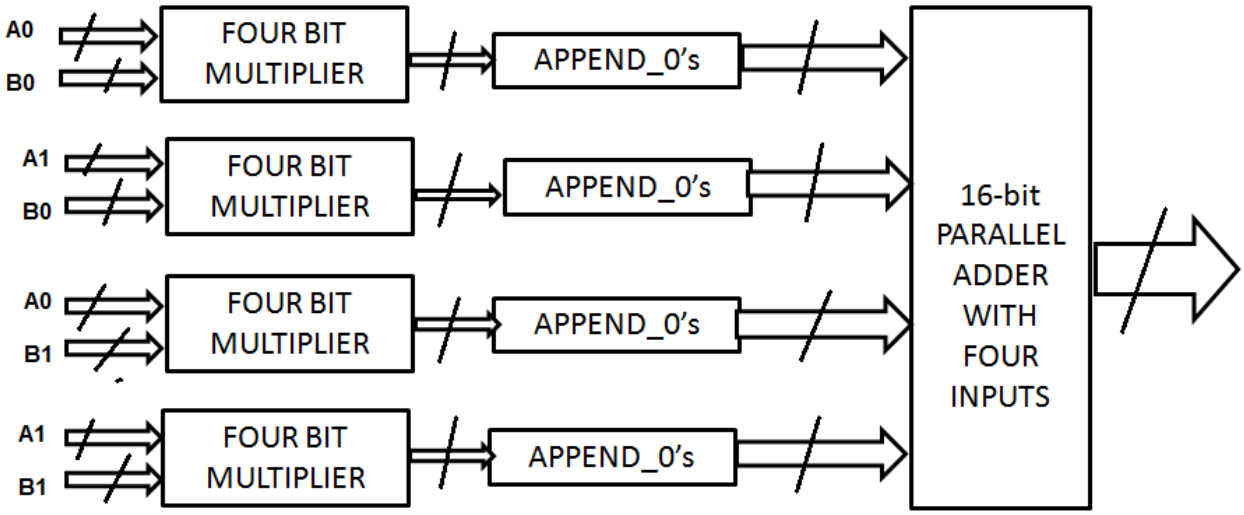

Figure 1 Single Cycle Implementation

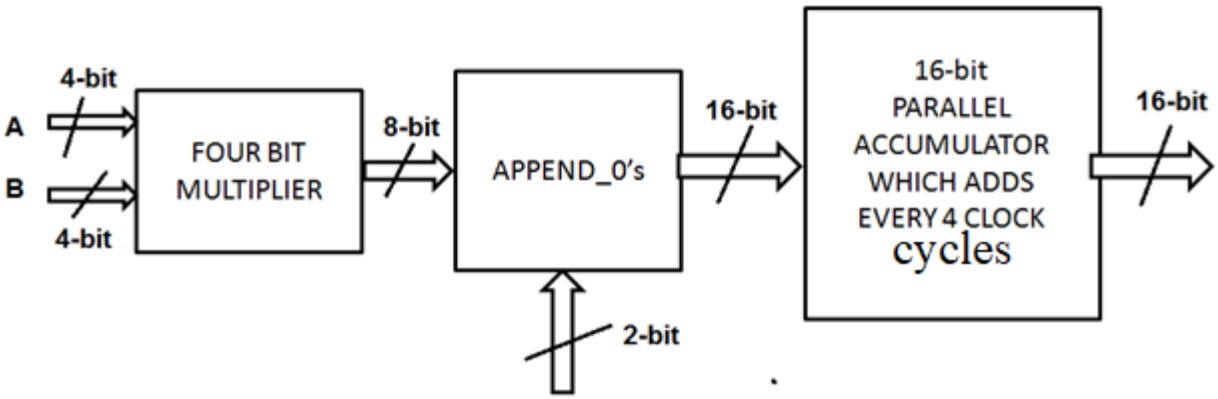

Figure 2 Multi-Cycle Implementation

*** ***The End*** ***

Submission Link: https://forms.gle/yDTRZsWGa85oqSjv7