**Birla Institute of Technology and Science Pilani**
**CS F342 Computer Architecture**
**Second Semester 2020-21**
**Lab Sheet– 3 (09th March 2021)**

---

## Gate Level Modeling Style

*In today's lab we shall implement a few circuits which we have studied in digital design using gate (structural) modeling style and verify their functionality using a suitable test bench prepared using Behavioral Modeling.*

**Learning Outcome:** By the end of this lab. session the learner will be able to

- Implement a digital circuit in Verilog HDL given its structure at gate level.
- Able to use the generate statement effectively to model repetitive instantiations.
- Use positional and named assignments effectively.
- Write effective test cases for verifying a design in HDL.

---

## Exercise Problems

1. Implement a 4-bit Johnson counter using J-K flip-flop. The J-K flip-flop can be implemented using behavioral modeling style.
2. Implement a 4-bit ripple carry adder using full-adder and half-adder cells. Full-adder and half-adder cells can be developed using data flow modeling style.
3. Implement a 6-bit unsigned binary array multiplier. Use structural style for implementing this. Individual Full-adder and Half-adder cells can be used from the previous problem.

****** The End ******

***-Prepared By***
***K. Babu Ravi Teja***
***Assistant Professor***
***EEE Department***
***BITS Pilani, Pilani Campus***