PHYSICAL DESIGN AND DESIGN FOR TEST HIRE AND TRAIN PROGRAM (EDGE)

Final Project Report

Project Title : ALU with Shifter Design

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The Block diagram of the ALU with Shifter is:

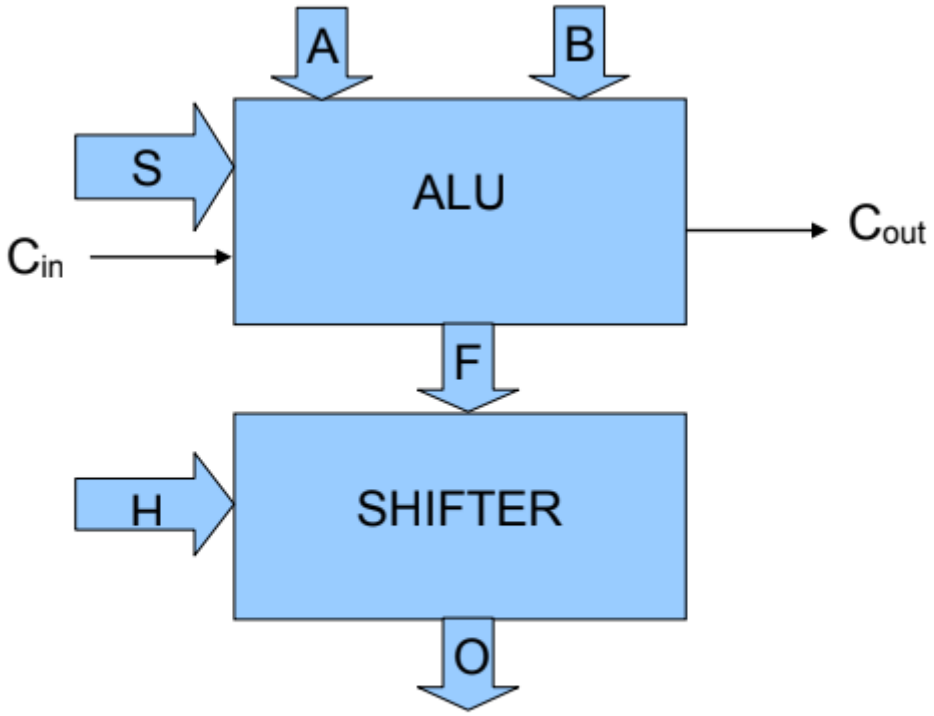


Fig. 1 : Block diagram of ALU with shifter.

Functionality of the ALU is given in the below Table:

Control Signal				F	Cout
S2	S1	S0	Cin		
0	0	0	0	F=A	Cout=0
0	0	0	1	F=A-1	Cout = 1 IF A ≠ 0
0	0	1	0	F=A-B-1	Cout = 1 IF A>B
0	0	1	1	F=A+B+1	Cout=1 if (A+B)>=2^4-1
0	1	0	0	F=A+1	Cout=1 if A=2^4-1
0	1	0	1	F=A+B	Cout=1 if (A+B)> = 2^4
0	1	1	0	F=A-B	Cout=1 if A=2^4-1
0	1	1	1	F=A	Cout=1
1	0	0	1	F=A **OR** B	Cout=0
1	0	1	1	F=A `	Cout=0
1	1	0	1	F=A **XOR** B	Cout=0
1	1	1	1	F=A **AND** B	Cout=0

H1	H0	Operation	Function
0	0	O=F	Transfer (no shift)
0	1	O = SHR (F)	Shift 1-bit right
1	0	O = SHL (F)	Shift 1-bit left
1	1	O = 0	Transfer 0

Write the verilog code of the ALU and test the ALU by designing a testbench in Verilog :

The Design devided into Three module. Two submodules are ALU.v and SHIFTER.v. TOP.v is the top module of the design.

```
module TOP (
        input [3:0] A,
        input [3:0] B,
        input [2:0] S,
        input Cin,
        input clk,
        input reset,
        input [1:0] H,
        output [3:0] O,
        output Cout
        );
wire [3:0] W,
ALU alu_inst (
        .A(A),
        .B(B),
        .S(S),
        .Cin(Cin),
        .clk(clk),
        .reset(reset),
        .Cout(Cout),
        .F(W)
        );
SHIFTER shifter_inst (
        .F(W),
        .H(H),
        .O(O)
        );
endmodule
```

```
module SHIFTER(F,H,O);
input [3:0]F;
input[1:0]H;
output reg O;

always@*
begin
case(H)
2'b00:O=F;
2'b01:O=F>>1;
2'b10:O=F<<1;
2'b11:O=0;
endcase
end
endmodule
```

```
module ALU(A,B,S,Cin,clk,reset,F,Cout);
 input [3:0]A,B;
 input [2:0]S;
 input Cin,clk,reset;
 output reg [3:0]F;
 output reg Cout;
 always@(posedge clk or posedge reset)
  begin
if(reset==1)
begin
        F=4'b0000;
        Cout=0;
end
else
        begin
 case({S,Cin})
//Operation 1 (F=A,Cout=0)
  4'b0000:
begin
    F=A;
    Cout=0;
end
//Operation 7 (F=A-1,Cout=1 on condition)
  4'b0001:
begin
    F=A-1;
  if(A!=0)
        Cout=1;
  else
        Cout=0;
end
//Operation 5 (F=A-B-1,Cout=1 on
condition)
  4'b0010:
begin
    F=A-B-1;
  if((A>B))
    Cout=1;
  else
        Cout=0;
end
//Operation 4
  4'b0011:
begin
    F=A+B+1;
    if((A+B)>=15)
     Cout=1;
    else
        Cout=0;
end
//Operation 2
  4'b0100:
begin
     F=A+1;
    if(A==15)
     Cout=1;
    else
        Cout=0;
end
```

```
//Operation 3
  4'b0101:
begin
     F=A+B;
    if((A+B)>=16)
     Cout=1;
    else
        Cout=0;
end
//Operation 6
  4'b0110:
begin
     F=A-B;
    if((A>=B))
     Cout=1;
        else
        Cout=0;
end
//Operation 8
  4'b0111:
begin
     F=A;
     Cout=1;
end
//Operation 9
  4'b1001:
begin
    F= A | B;
    Cout=0;
end
//Operation 12
  4'b1011:
begin
    F= ~A;
    Cout=0;
end
//Operation 10
  4'b1101:
begin
    F= A ^ B;
    Cout=0;
end
//Operation 11
  4'b1111:
begin
    F=A & B;
    Cout=0;
end
default:
begin
Cout=0;
F=4'b0000;
end
    endcase
end
end
endmodule
```

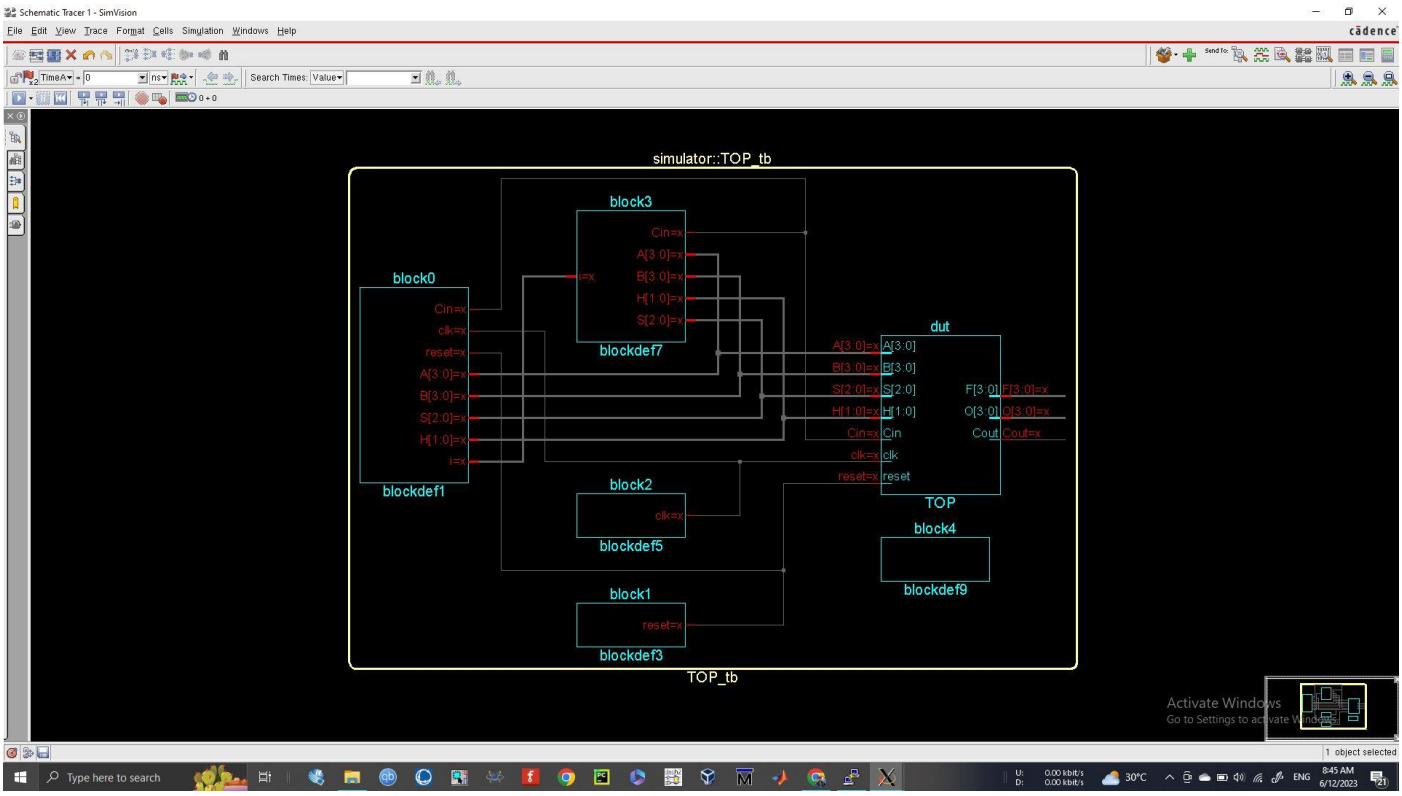


Fig:Block Diagram of DUT

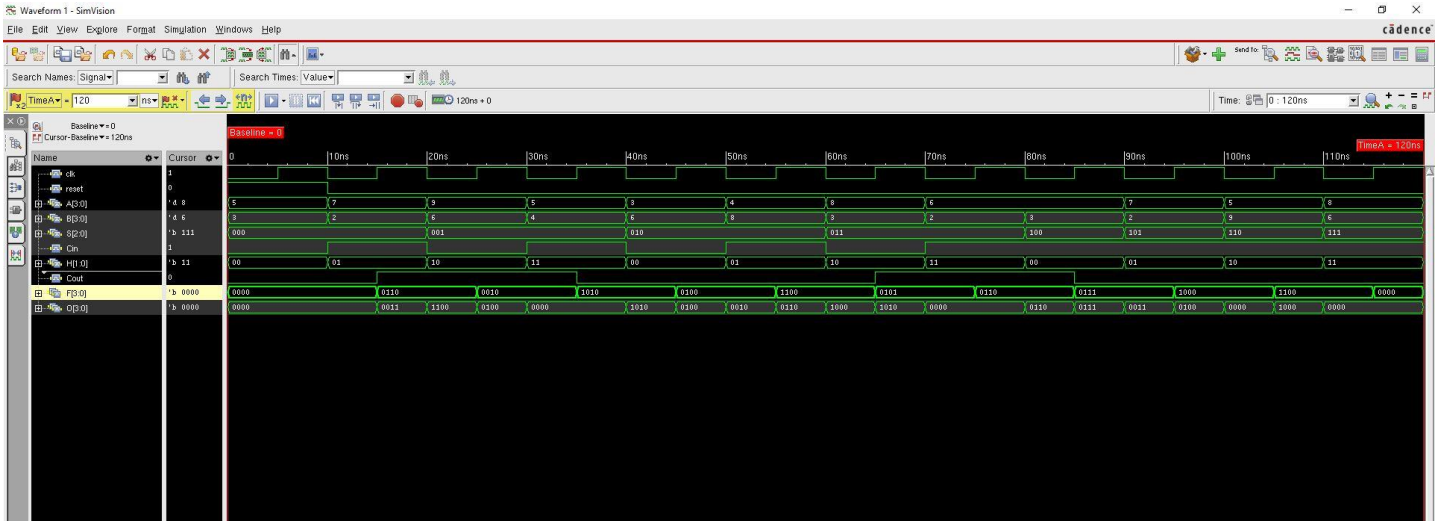
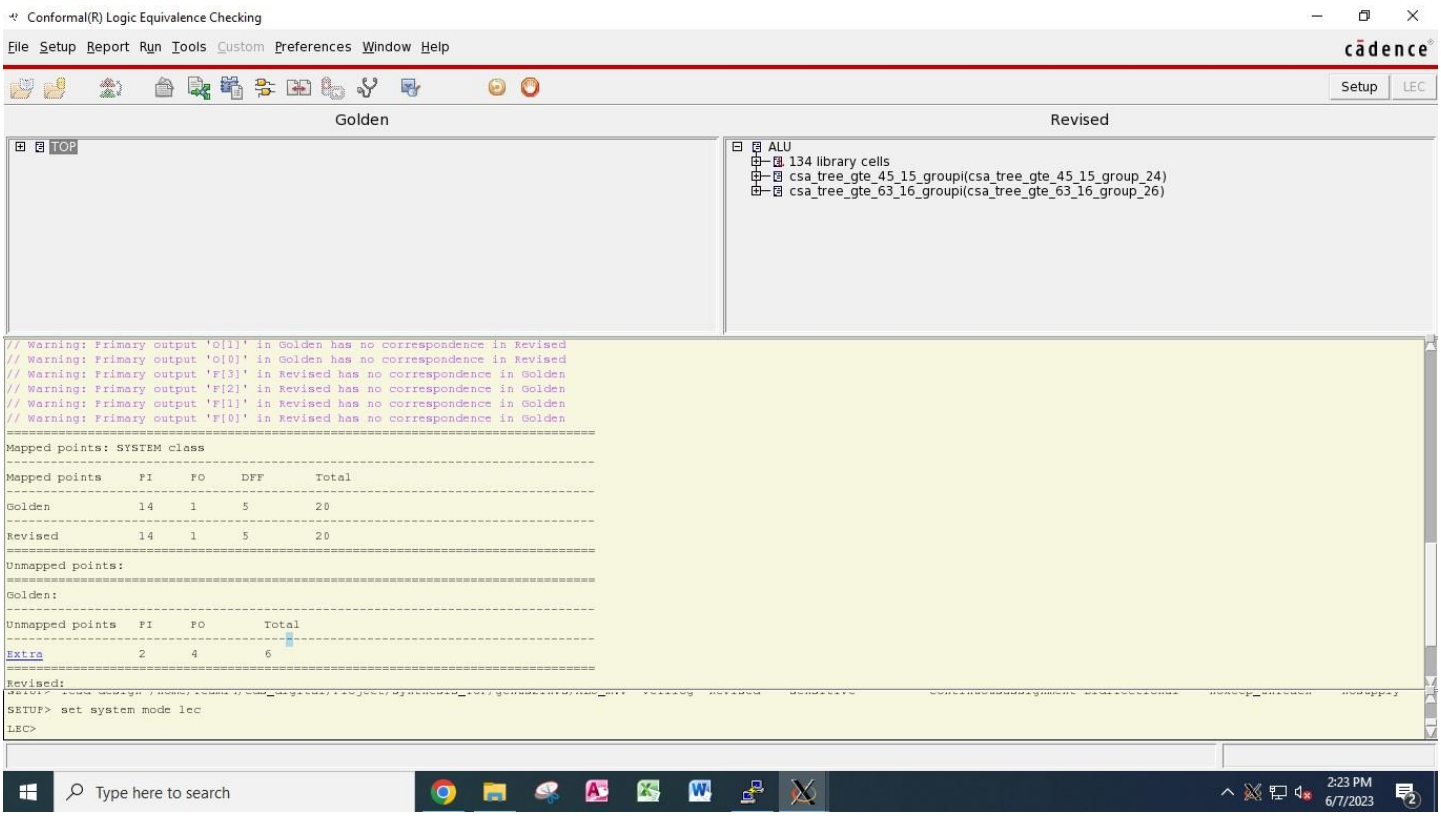


Fig: Output Waveform

Logical Equivalance Check (LEC):



Synthesis

Now synthesis the design in gpdk045 in cadence Genus. Use the following files:

File Name	Uses
slow_vdd1v0_basicCells.lib	Standard cell library for slow corner operation (setup check)
fast_vdd1v0_basicCells.lib	Standard cell library for fast corner operation (hold check)
gsclib045_tech.lef	Process technology .lef file for 45nm tech node
gsclib045_macro.lef	Standard cell physical information for 45nm tech node

Timing report After synthesis

```
legacy_genus:/> report_timing
Warning : Possible timing problems have been detected in this design. [TIM-11]
        : The design is 'TOP'.
============================================================
  Generated by:           Genus(TM) Synthesis Solution 16.13-s036_1
  Generated on:           Jun 13 2023  09:30:02 am
  Module:                 TOP
  Technology libraries:   slow_vdd1v0 1.0
                          fast_vdd1v0 1.0
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

        Pin                  Type      Fanout Load Slew Delay Arrival
                                         (fF) (ps)  (ps)   (ps)
-------------------------------------------------------------------------
(clock func_clk)           launch                                  0 R
(TOP.sdc_line_17_2_1)      ext delay                            +400     400 F
A[1]                       in port         4  1.3    0    +0     400 F
alu_inst/A[1]
  g3755/A                                                      +0     400
  g3755/Y                  INVX1          9  3.2   73   +45     445 R
  g37439867/B                                                  +0     445
  g37439867/Y              NAND2X1        2  0.6   72   +87     532 F
  g37297654/AN                                                 +0     532
  g37297654/Y              NOR2BX1        3  1.1   52   +97     629 F
  g36878867/B                                                  +0     629
  g36878867/Y              XNOR2X1        3  1.2   43  +180     809 R
  g36667765/A1                                                 +0     809
  g36667765/Y              OAI222X1       2  0.6  207  +216    1025 F
  g36496179/A1                                                 +0    1025
  g36496179/Y              OAI22X1        1  0.4   99  +166    1191 R
  g36432001/B0                                                 +0    1191
  g36432001/Y              OAI2BB1X1      1  0.3   59  +104    1295 F
  g36301297/C0                                                 +0    1295
  g36301297/Y              OAI221X1       2  0.8  120   +56    1352 R
  g36262007/C                                                  +0    1352
  g36262007/Y              NAND3X1        1  0.3  103  +130    1482 F
  g36221377/B1                                                 +0    1482
  g36221377/Y              AOI22X1        2  0.8   90  +109    1592 R
  g36187557/B                                                  +0    1592
  g36187557/Y              NAND2X1        1  0.3   61   +88    1679 F
  g36167837/C0                                                 +0    1679
  g36167837/Y              OAI211X1       1  0.3   79   +52    1731 R
  Cout_reg/D          <<<  DFFRHQX1                             +0    1731
  Cout_reg/CK              setup                             0  +147    1879 R
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock func_clk)           capture                                 5000 R
-------------------------------------------------------------------------
Cost Group   : 'func_clk' (path_group 'func_clk')
Timing slack :    3121ps
Start-point  : A[1]
End-point    : alu_inst/Cout_reg/D

legacy_genus:/>
```

power consumption report:

```
legacy_genus:/> report_power
================================================================
  Generated by:           Genus(TM) Synthesis Solution 16.13-s036_1
  Generated on:           Jun 13 2023  09:26:59 am
  Module:                 TOP
  Technology libraries:   slow_vdd1v0 1.0
                          fast_vdd1v0 1.0
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
================================================================

                    Leakage   Dynamic    Total
   Instance    Cells Power(nW) Power(nW) Power(nW)
-----------------------------------------------------
TOP              152     5.931 18719.206 18725.137
  alu_inst       139     5.513 16624.631 16630.143
  shifter_inst    13     0.419  1142.720  1143.138

legacy_genus:/>
```

Mapping report:

```
legacy_genus:/> report gates
================================================================
  Generated by:           Genus(TM) Synthesis Solution 16.13-s036_1
  Generated on:           Jun 13 2023  09:36:04 am
  Module:                 TOP
  Technology libraries:   slow_vdd1v0 1.0
                          fast_vdd1v0 1.0
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
================================================================

   Gate    Instances   Area       Library
-------------------------------------------
AND2X1             1    1.368    slow_vdd1v0
AO21XL             1    2.394    slow_vdd1v0
AOI211XL           2    4.104    slow_vdd1v0
AOI21X1            3    5.130    slow_vdd1v0
AOI221X1           6   14.364    slow_vdd1v0
AOI222X1           2    6.156    slow_vdd1v0
AOI22X1            7   14.364    slow_vdd1v0
DFFRHQX1           5   30.780    slow_vdd1v0
INVX1             29   19.836    slow_vdd1v0
MXI2XL             1    2.394    slow_vdd1v0
NAND2BX1           5    6.840    slow_vdd1v0
NAND2X1           15   15.390    slow_vdd1v0
NAND3X1            1    1.710    slow_vdd1v0
NAND4XL            1    1.710    slow_vdd1v0
NOR2BX1            3    4.104    slow_vdd1v0
NOR2X1            17   17.442    slow_vdd1v0
NOR2XL             1    1.026    slow_vdd1v0
NOR3X1             1    1.710    slow_vdd1v0
NOR4X1             1    1.710    slow_vdd1v0
OA21X1             2    4.104    slow_vdd1v0
OA22X1             1    2.394    slow_vdd1v0
OAI211X1           6   10.260    slow_vdd1v0
OAI21X1            4    6.840    slow_vdd1v0
OAI221X1           5   11.970    slow_vdd1v0
OAI222X1           4   10.944    slow_vdd1v0
OAI22X1           11   22.572    slow_vdd1v0
OAI2BB1X1          4    6.840    slow_vdd1v0
OAI32X1            1    2.394    slow_vdd1v0
OR2X1              5    6.840    slow_vdd1v0
XNOR2X1            6   14.364    slow_vdd1v0
XOR2X1             1    2.736    slow_vdd1v0
-------------------------------------------
total            152  254.790


     Type      Instances   Area  Area %
----------------------------------------
sequential             5  30.780   12.1
inverter              29  19.836    7.8
logic                118 204.174   80.1
physical_cells         0   0.000    0.0
----------------------------------------
total                152 254.790  100.0

legacy_genus:/>
```

Area

```
legacy_genus:/> report_area
====================================================================
  Generated by:           Genus(TM) Synthesis Solution 16.13-s036_1
  Generated on:           Jun 13 2023  09:27:54 am
  Module:                 TOP
  Technology libraries:   slow_vdd1v0 1.0
                          fast_vdd1v0 1.0
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
====================================================================

   Instance     Module  Cells  Cell Area  Net Area   Total Area  Wireload
--------------------------------------------------------------------------------
TOP                       152        255         0          255    <none> (D)
  alu_inst     ALU        139        236         0          236    <none> (D)
  shifter_inst SHIFTER     13         18         0           18    <none> (D)

 (D) = wireload is default in technology library
legacy_genus:/>
```

Schamatic Diagram after synthesis

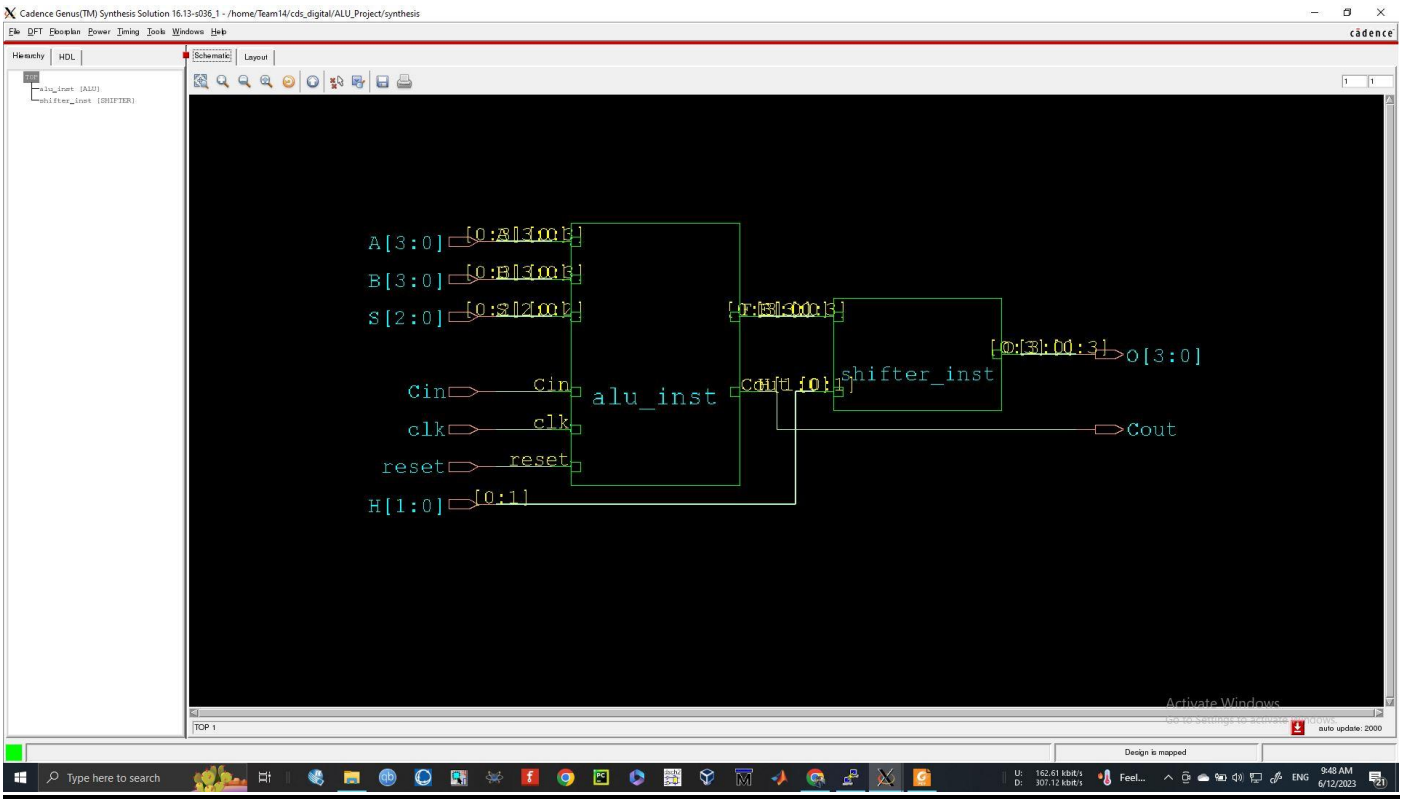


Fig: TOP module

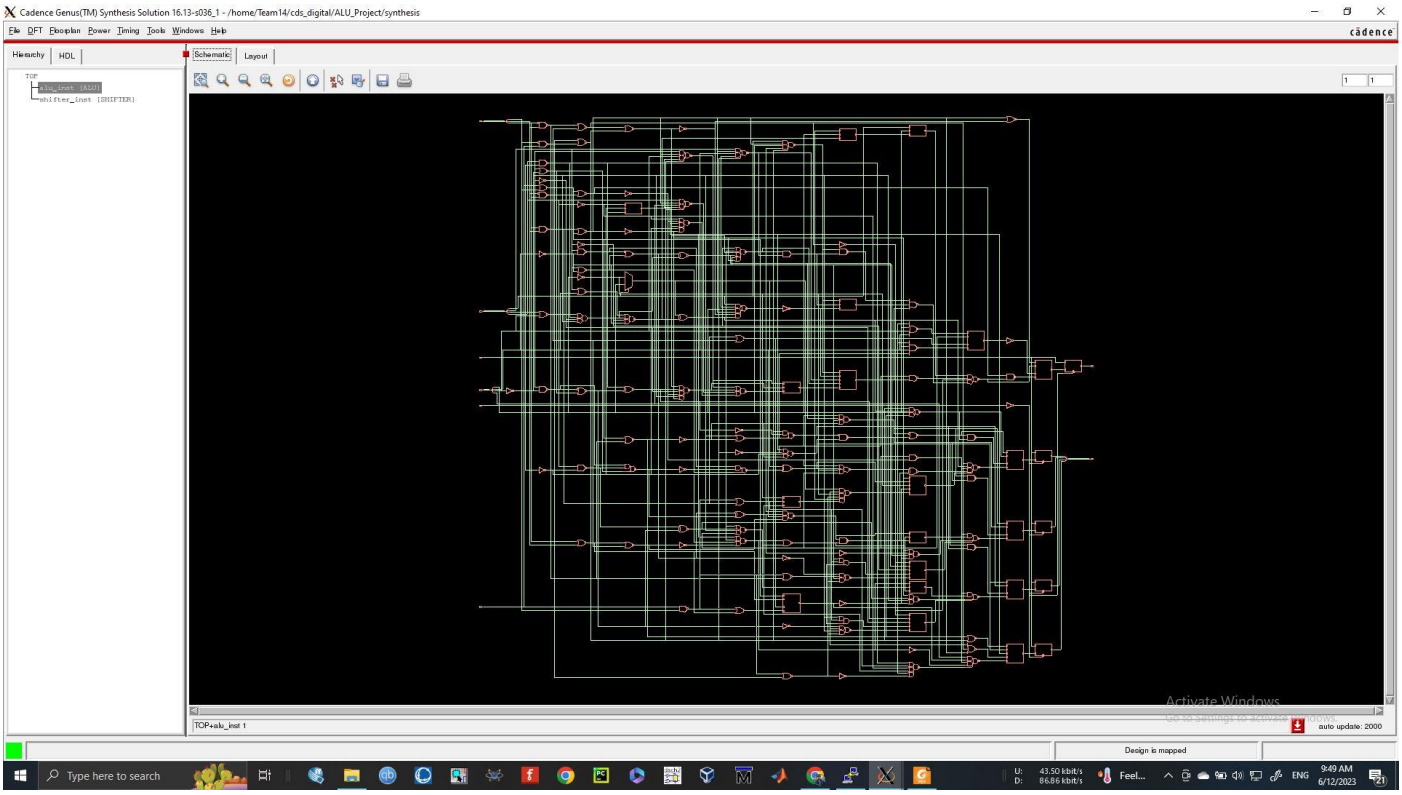


Fig:Sub module -ALU

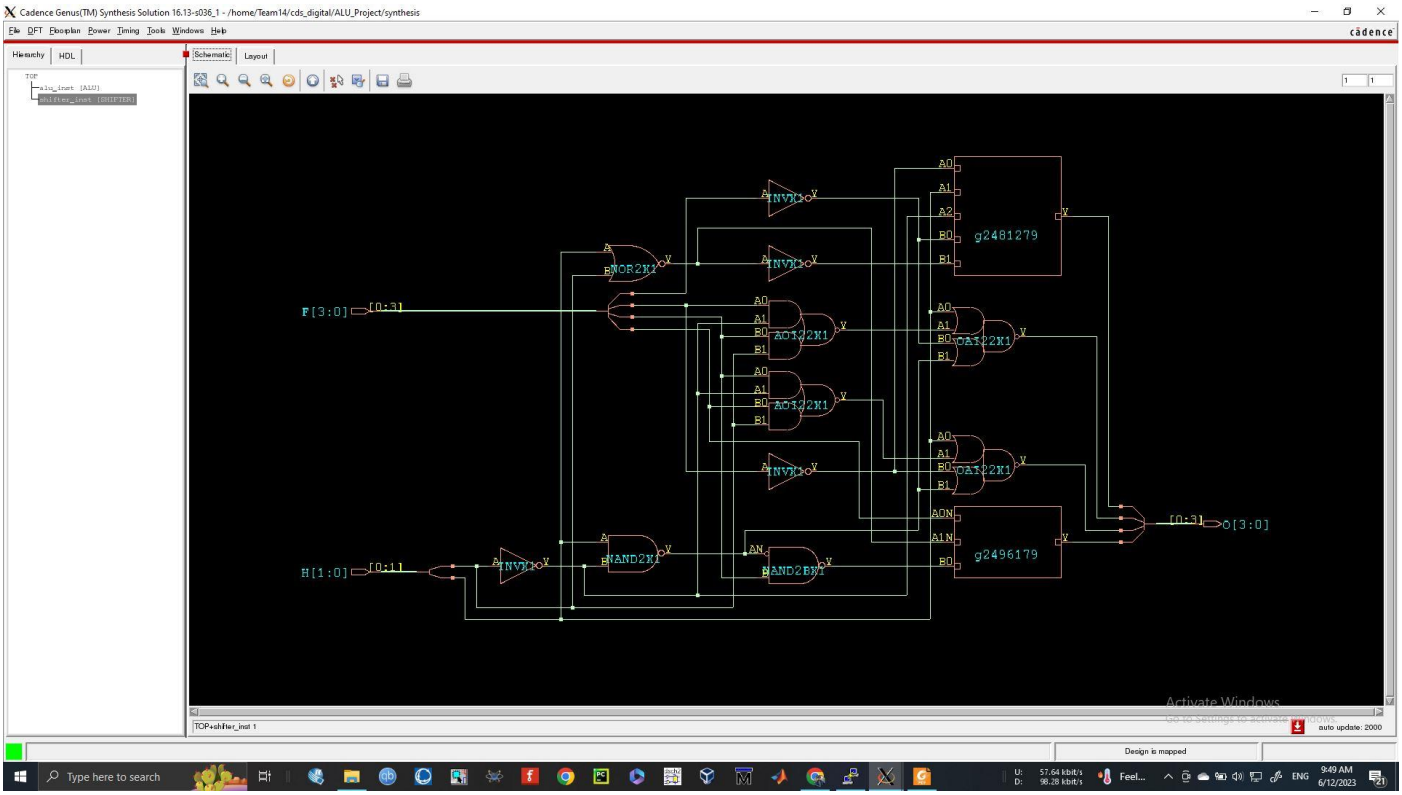


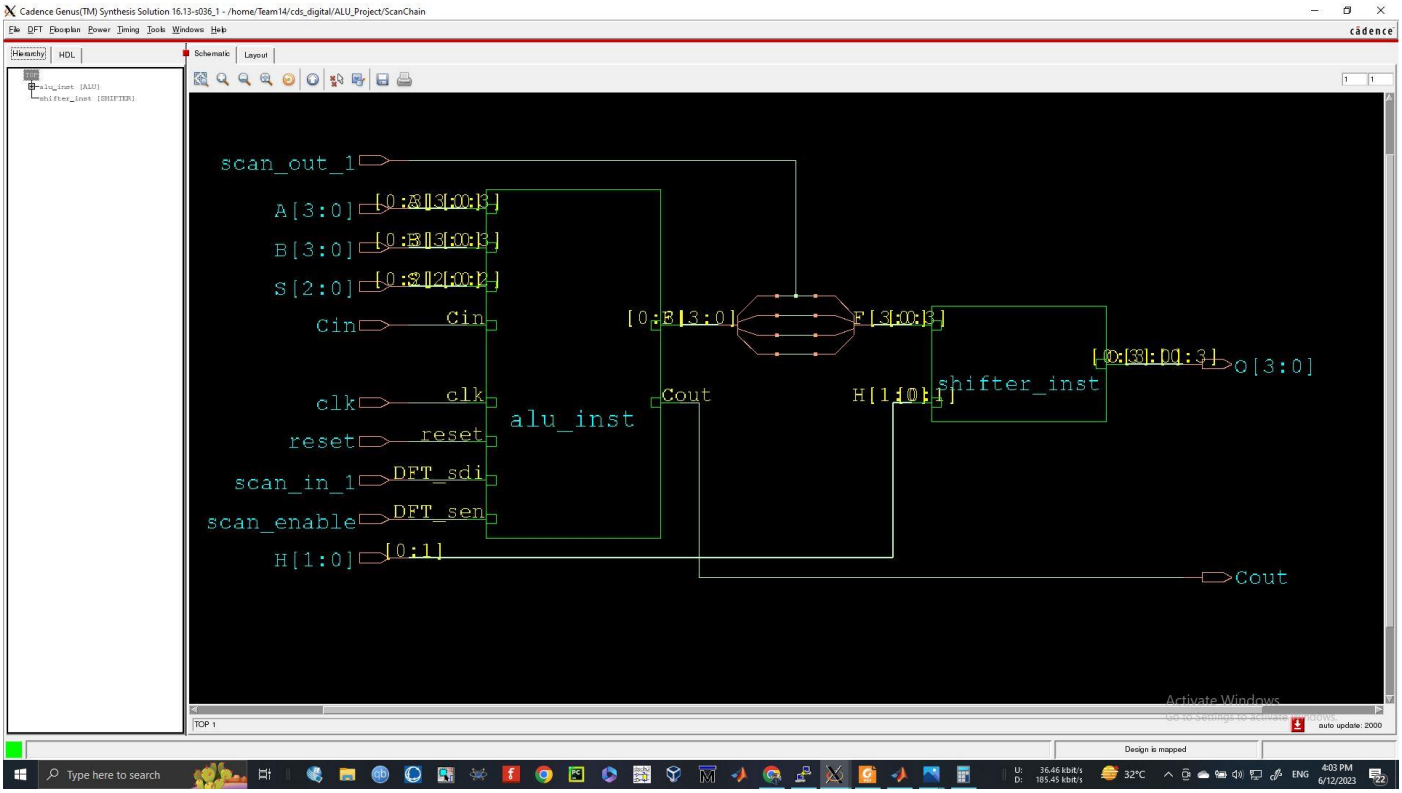
Fig:Sub module- Shifter

DFT

Create Scan for DFT :

```
        Summary of check_dft_rules
        **************************
        Number of usable scan cells: 48
Clock Rule Violations:
----------------------
          Internally driven clock net: 0
              Tied constant clock net: 0
                   Undriven clock net: 0
        Conflicting async & clock net: 0
                      Misc. clock net: 0

Async. set/reset Rule Violations:
---------------------------------
        Internally driven async net: 0
             Tied active async net: 0
                Undriven async net: 0
                   Misc. async net: 0

   Total number of DFT violations: 0

  Total number of Test Clock Domains: 1
      DFT Test Clock Domain: clk
        Test Clock 'clk' (Positive edge) has   5 registers
  Number of user specified non-Scan registers:   0
      Number of registers that fail DFT rules:   0
      Number of registers that pass DFT rules:   5
  Percentage of total registers that are scannable: 100%
0
legacy_genus:/>
```

There are total 5 FFs and all of them are replaced with scannable FFs.



Placement AND Routing

In placement and routing stage, first of all, we have to import design to the innovous using the TOP_placement.tcl file. After that floorPlaning and PowerPlaning can be done using TOP_floorplan.tcl file.

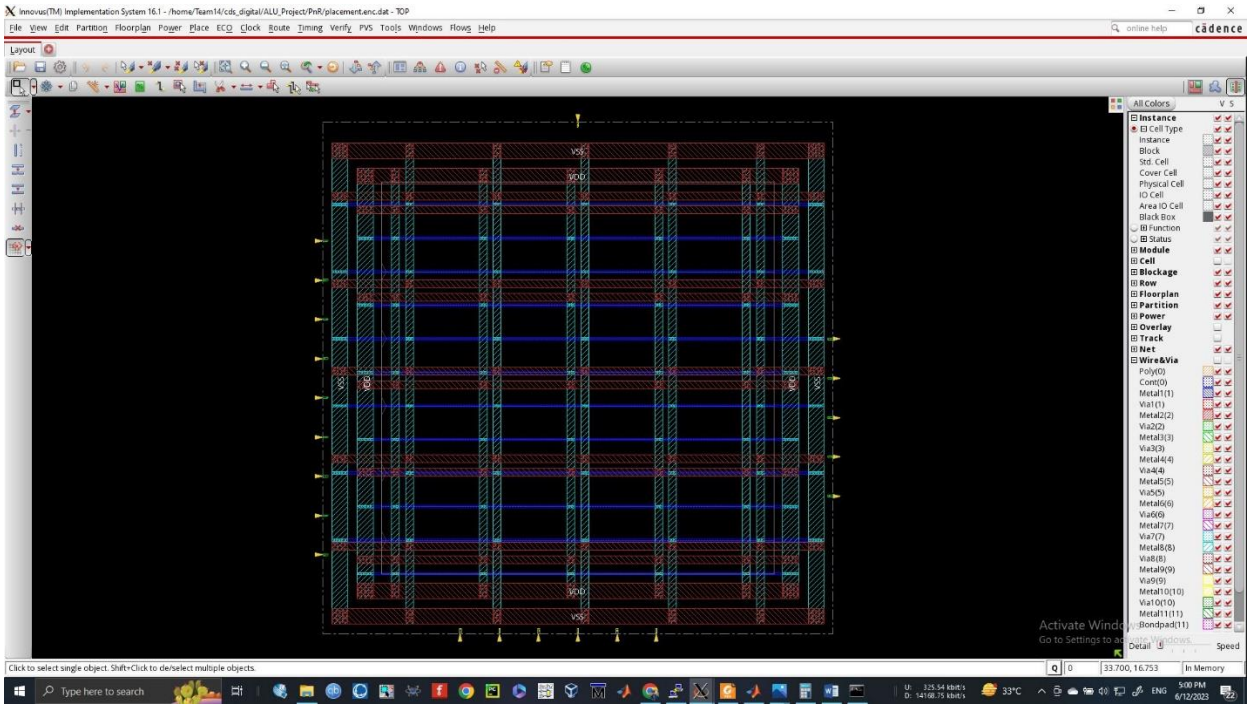


Fig: FloorPlan and PowerPlan

Placement can be done after powerPlan:

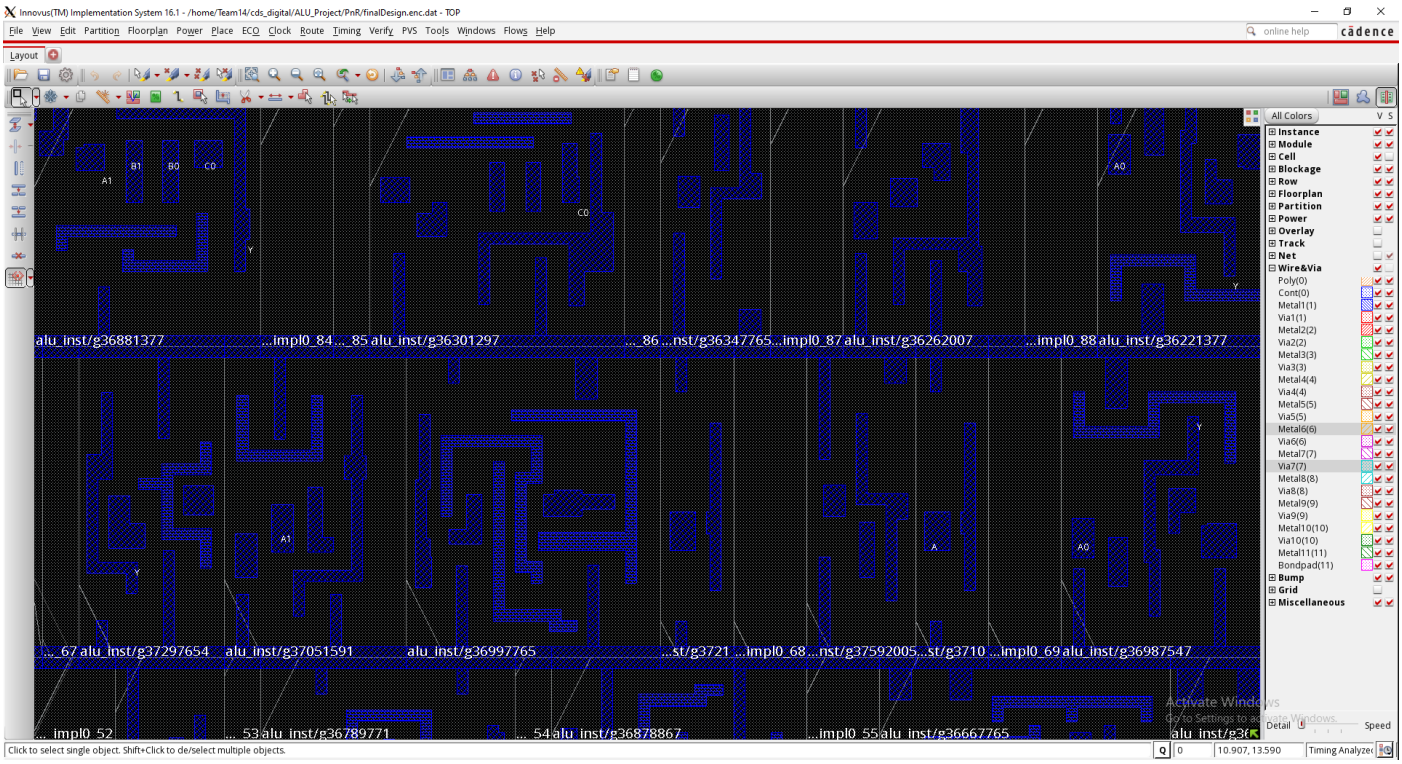


Fig: Placement of the standards cell

```
innovus 21> report_constraint -drv_violation_type max_capacitance -all_violators
#################################################################
#  Generated by:      Cadence Innovus 16.10-p004_1
#  OS:                Linux x86_64(Host ID CadenceServer3.localdomain)
#  Generated on:      Tue Jun 13 11:15:02 2023
#  Design:            TOP
#  Command:           report_constraint -drv_violation_type max_capacitance -all_violators
#################################################################
# format : frame 1 : split 1

Check type : max_capacitance
----------------------------
 No Violations found
innovus 22>
innovus 22> report_constraint -drv_violation_type max_transition -all_violators
#################################################################
#  Generated by:      Cadence Innovus 16.10-p004_1
#  OS:                Linux x86_64(Host ID CadenceServer3.localdomain)
#  Generated on:      Tue Jun 13 11:16:10 2023
#  Design:            TOP
#  Command:           report_constraint -drv_violation_type max_transition -all_violators
#################################################################
# format : frame 1 : split 1

Check type : max_transition
---------------------------
 No Violations found
innovus 23>

innovus 23> report_constraint -drv_violation_type max_fanout -all_violators
#################################################################
#  Generated by:      Cadence Innovus 16.10-p004_1
#  OS:                Linux x86_64(Host ID CadenceServer3.localdomain)
#  Generated on:      Tue Jun 13 11:16:43 2023
#  Design:            TOP
#  Command:           report_constraint -drv_violation_type max_fanout -all_violators
#################################################################
# format : frame 1 : split 1

Check type : max_fanout
---------------------------
 No Violations found
innovus 24>
```

Fig: Checking DRV violations

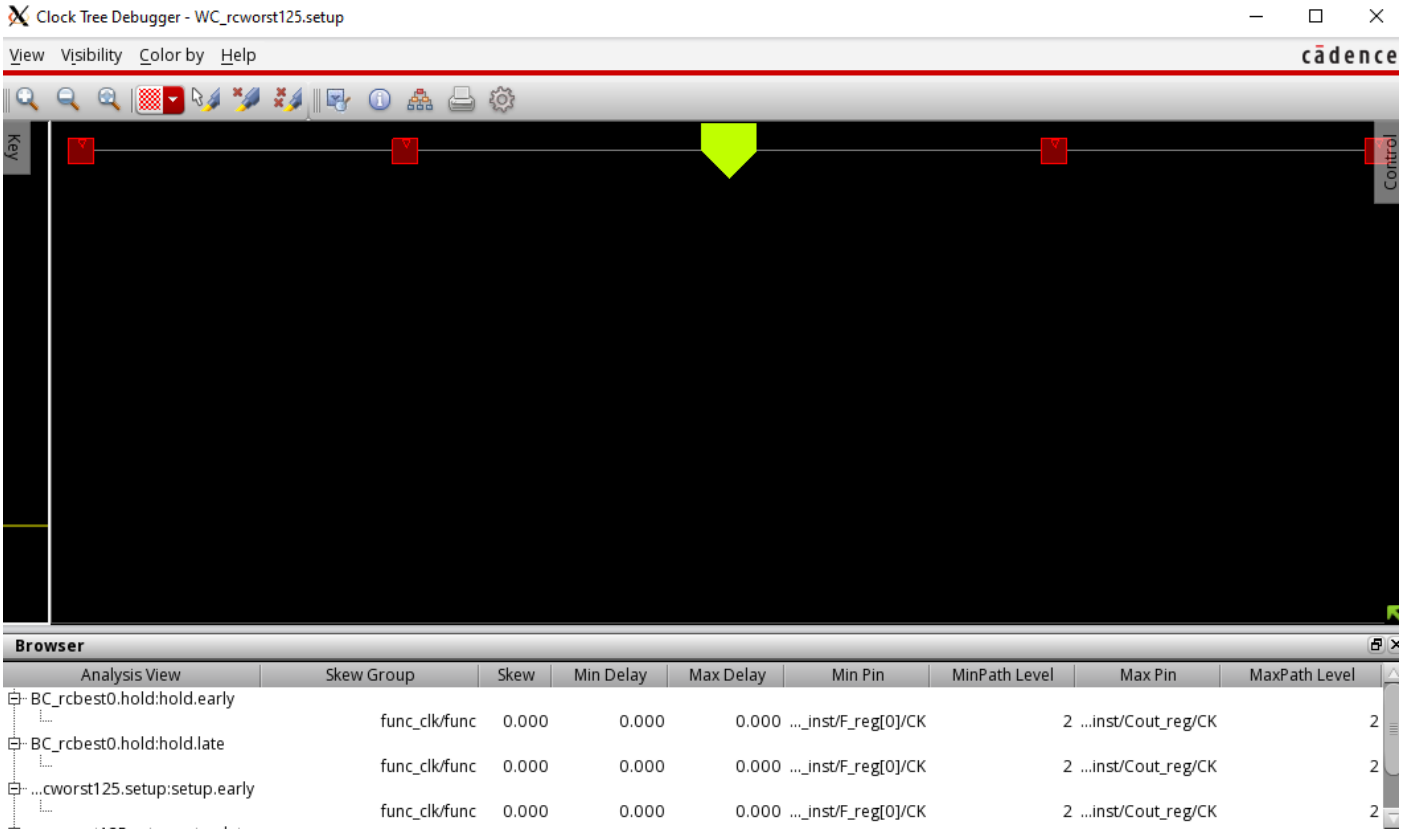
After placement, it is necessary to check timing reports before Clock Tree Synthesis:

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 func@WC_rcworst125.setup

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  2.795  |   N/A   |  2.795  |
|           TNS (ns):|  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |   N/A   |    0    |
|          All Paths:|   15    |   N/A   |   15    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 72.364%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir ./timingReports
Total CPU time: 0.65 sec
Total Real time: 1.0 sec
Total Memory Usage: 1250.578125 Mbytes
```

Fig: Setup check before CTS

Clock Tree Synthesis (CTS):

A clock tree is needed to be built in the design for balancing clock skew and latency after optimizing the design in the placement stage (pre-CTS stage). It is built using a clock buffer or inverter cells.



Setup Time: the amount of time the data at the input must be stable before the active edge of clock.

Hold Time: the amount of time the data at the input must be stable after the active edge of clock.

A positive slack shows that the timing path meets the timing constraint requirements (setup and hold), whereas a negative slack indicates the timing path violates the setup and hold timing constraints requiring further optimization.

Setup check after CTS:

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 func@WC_rcworst125.setup

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  2.800  |   N/A   |  2.800  |
|           TNS (ns):|  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |   N/A   |    0    |
|          All Paths:|   15    |   N/A   |   15    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 72.909%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir ./timingReports
Total CPU time: 0.28 sec
Total Real time: 1.0 sec
Total Memory Usage: 1347.75 Mbytes
```

Hold check After CTS:

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 func@BC_rcbest0.hold

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.013  |   N/A   |  0.013  |
|           TNS (ns):|  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |   N/A   |    0    |
|          All Paths:|   15    |   N/A   |   15    |
+--------------------+---------+---------+---------+

Density: 72.909%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir ./timingReports
Total CPU time: 0.25 sec
Total Real time: 0.0 sec
Total Memory Usage: 1322.796875 Mbytes
```

After CTS, we have to perform routing using **TOP_route.tcl** file.

Power consumption:

```
--------------------------------------------------------------------------------------


Total Power
--------------------------------------------------------------------------------------
Total Internal Power:        0.00799577            71.0889%
Total Switching Power:       0.00324466            28.8477%
Total Leakage Power:         0.00000712             0.0633%
Total Power:                 0.01124756
--------------------------------------------------------------------------------------


Group                           Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
--------------------------------------------------------------------------------------
Sequential                      0.003344   9.213e-05   6.647e-07    0.003437       30.55
Macro                                 0           0           0           0           0
IO                                    0           0           0           0           0
Combinational                   0.004652    0.003153   6.459e-06    0.007811       69.45
Clock (Combinational)                 0           0           0           0           0
Clock (Sequential)                    0           0           0           0           0
--------------------------------------------------------------------------------------
Total                           0.007996    0.003245   7.124e-06     0.01125         100
--------------------------------------------------------------------------------------


Rail                  Voltage   Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
--------------------------------------------------------------------------------------
VDD                       0.9   0.007996    0.003245   7.124e-06     0.01125         100


--------------------------------------------------------------------------------------
*       Power Distribution Summary:
*               Highest Average Power:         alu_inst/F_reg[3] (DFFRHQX1):     0.0007084
*               Highest Leakage Power:            FE_ECOC6_reset (BUFX16):       4.904e-07
*               Total Cap:      2.2083e-13 F
*               Total instances in design:   157
*               Total instances in design with no power:     0
*                Total instances in design with no activty:     0

*               Total Fillers and Decap:     0
--------------------------------------------------------------------------------------

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total)=1093.75MB/1093.75MB)

1
```

Filler cells is used to fill gaps in the layout after placement and routing is completed.

Filler cell insertion was completed before physical verification can begin.

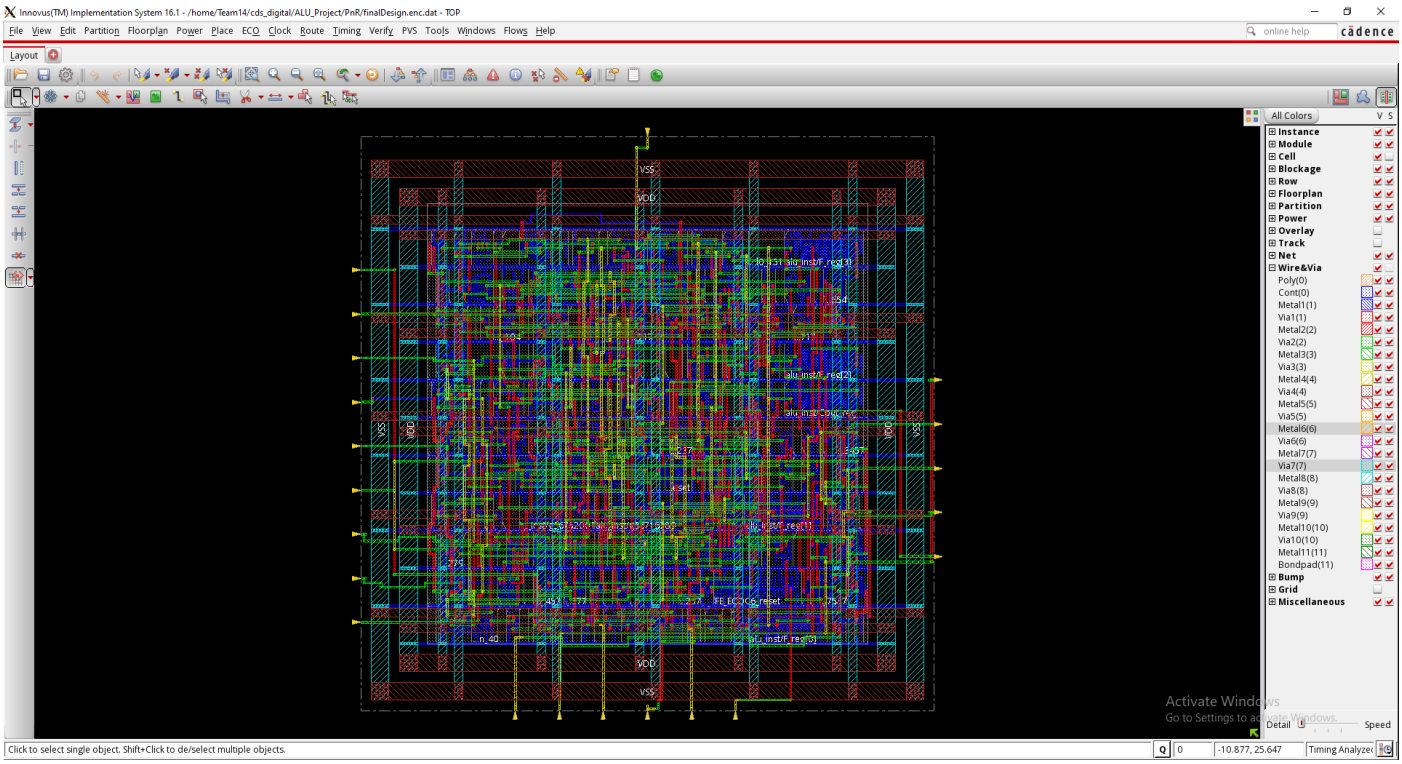


Fig: Final Design

DRC check:

```
innovus 23> verify_drc
 *** Starting Verify DRC (MEM: 1905.8) ***

  VERIFY DRC ..... Starting Verification
  VERIFY DRC ..... Initializing
  VERIFY DRC ..... Deleting Existing Violations
  VERIFY DRC ..... Creating Sub-Areas
**WARN: (IMPVFG-1198):  The number of CPUs requested 8 is larger than that verify_drc used 1. In Multithreading mode, the nu
mber of CPUs verify_drc used is not larger than the number of subareas.
 Use 'setMultiCpuUsage -localCpu' to specify the less cup number if the verify area is not large.
  VERIFY DRC ..... Using new threading
  VERIFY DRC ..... Sub-Area : 1 of 1
  VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

  Verification Complete : 0 Viols.

 *** End Verify DRC (CPU: 0:00:00.2  ELAPSED TIME: 0.00  MEM: 126.2M) ***
```

Connectivity Check:

```
innovus 24> verify_connectivity
VERIFY_CONNECTIVITY use new engine.

******** Start: VERIFY CONNECTIVITY ********
Start Time: Wed Jun 14 15:56:55 2023

Design Name: TOP
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (26.0000, 26.0300)
Error Limit = 1000; Warning Limit = 50
Check all nets
Multi-CPU acceleration using 8 CPU(s).

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Wed Jun 14 15:56:55 2023
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.7  MEM: 7.781M)
```

Verify PG short:

```
innovus 25> verify_PG_short
 *** Starting VERIFY PG SHORT(MEM: 2032.0) ***

  VERIFY PG SHORT ..... Initializing
  VERIFY PG SHORT ..... Deleting Existing Violations
  VERIFY PG SHORT ..... Creating Sub-Areas
                  ..... bin size: 1920
**WARN: (IMPVFG-198):   Area to be verified is small to see any runtime gain from multi-cpus. Use setMultiCpuUsage command t
o adjust the number of CPUs.
  VERIFY PG SHORT ..... SubArea : 1 of 1
  VERIFY PG SHORT ..... Short:  0 Viols.
  Verification Complete : 0 Short Viols.

**********End: VERIFY PG SHORT**********
 *** verify PG short (CPU: 0:00:00.1  MEM: 1.5M)
```

Report area:

```
innovus 12> report_area
Depth  Name            #Inst  Area (um^2)
----------------------------------------
0      TOP             157    281.124
1      alu_inst        143    255.816
1      shifter_inst    13     18.468
1
innovus 13>
```

Exported GDS view on Virtuoso: