ECE 637 Project 3: 16 bit Adder

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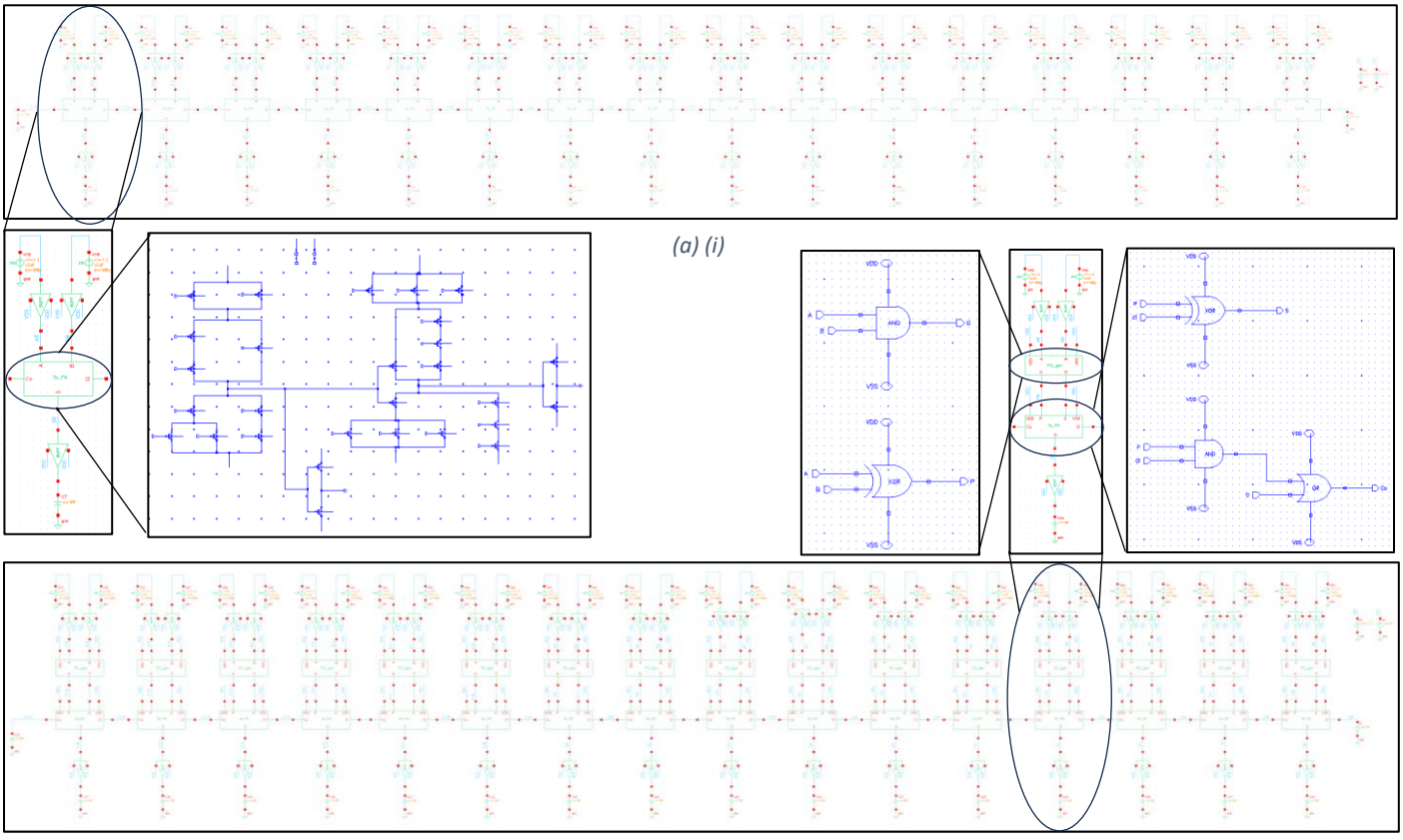
Introduction, review and simulation results of different adder architectures:

This project involves comparing 4 architectures of CMOS 16bit full adders with the aim of achieving highest propagation delay (t_p) as 400ps in all corner/temperature combinations. Once an architecture is settled upon that meets the specified constraints, the impact of power supply voltage (V_{DD}) on the power delay product is observed.

The 4 adder architectures chosen are (1) Ripple Carry Adder (RCA), (2) Carry Bypass Adder, (3) Carry Select Adder, and (4) Radix-2 Kogge Stone Adder. The files of these adders are situated in 'proj3_cadence/proj3_16b_FA'. The delay for each of these adders is (N= no of bits):

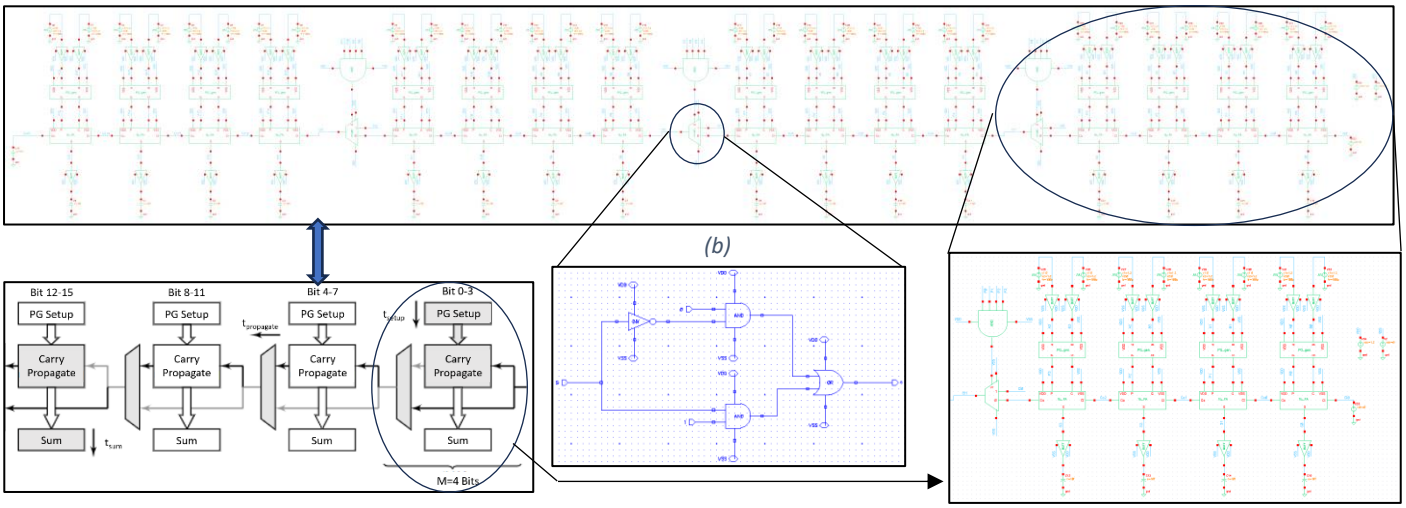
1. $t_{RCA} = t_{setup} + 15t_{carry} + t_{sum} \rightarrow O(N)$
2. $t_{carry\_bypass} = t_{setup} + 7t_{carry} + 3t_{bypass} + t_{sum} \rightarrow O(N)$
3. $t_{carry\_select} = t_{setup} + 4t_{carry} + 4t_{mux} + t_{sum} \rightarrow O(N)$
4. $t_{tree\_adder} \rightarrow O(log_2 N)$

The description of each of the adders along with the adder schematics are given below:



(a) (i)

(a) (ii)



(b)

Fig 1: (a) (i) RCA with Project 2 FA schematic, (ii) RCA with PG; (b) Carry Bypass adder

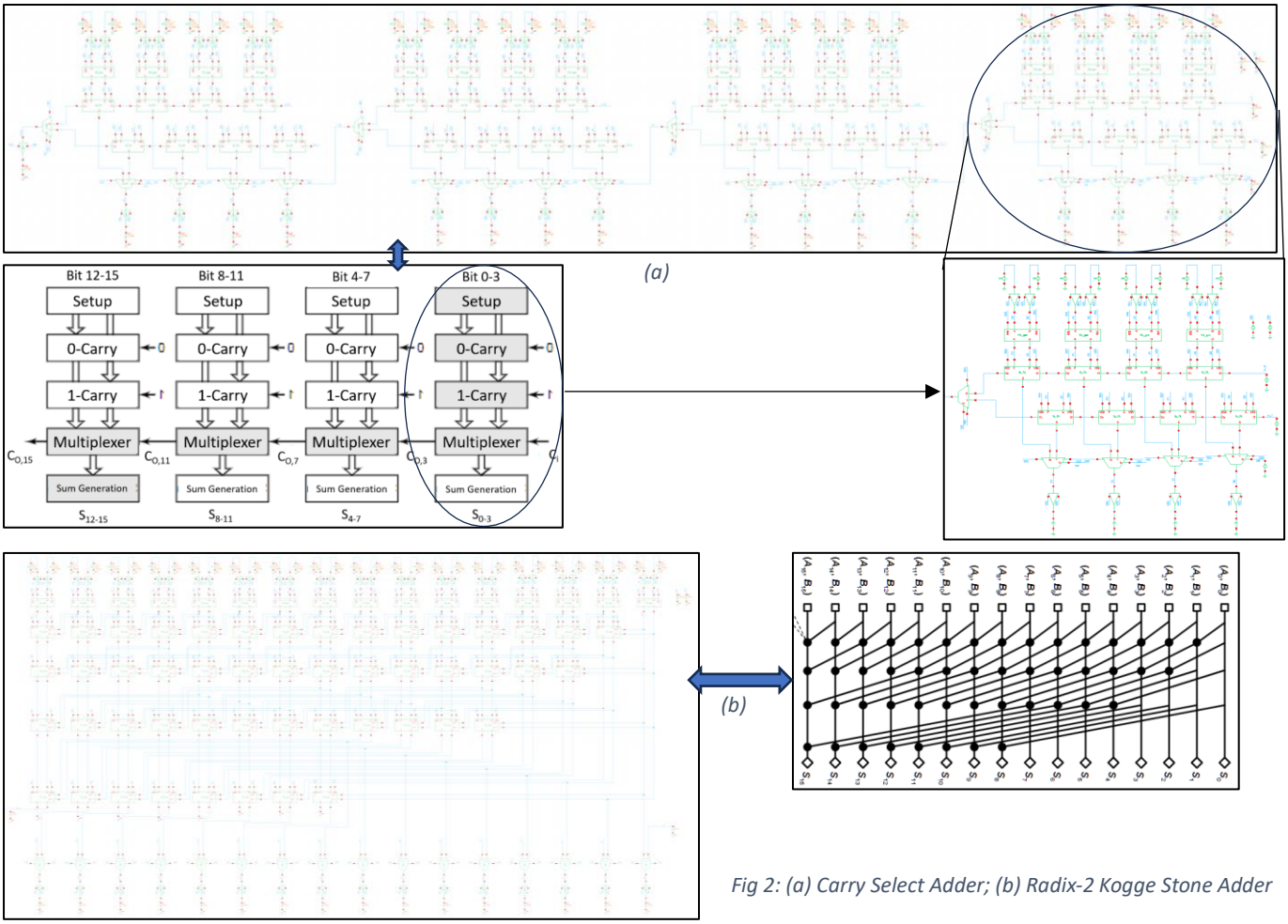


Fig 2: (a) Carry Select Adder; (b) Radix-2 Kogge Stone Adder

Table 1: Worst case Propagation delays associated with adder architectures

FA Architecture	Ripple Carry	Ripple carry (PG)	Carry Bypass	Carry Select	Kogge Tree
Vector A	783.2 ps	620.1 ps	424.1 ps	322.8 ps	210.8 ps
Vector B	99.9 ps	59.79 ps	83.57 ps	111.4 ps	93.14 ps
Vector C	113.6 ps	59.79 ps	83.54 ps	110.4 ps	93.14 ps

Initially the original Full adder used for Project 2 was used to design the ripple carry adder, however, the delay was coming too high ~ 800ps. Hence the Propagate/Generate (PG) version of the full adder was chosen to design the 1bit full adder and the RCA (t_p~600p) as well as subsequent adder circuits in an attempt to keep the delay to a minimum. The adder circuits were designed as shown in the standard diagrams given – setup, carry propagate, mux, sum generation. It was seen (table 1) that two FA circuits – Carry select and Kogge Stone tree adders gave delays lesser than 400ps. However, the carry select adder gave t_p=421.3ps for the SS_85°C condition, hence the final adder circuit chosen is the Radix-2 Kogge Stone Adder.

Architecture and transistor-level circuit design of Radix 2 Kogge-Stone Tree Adder:

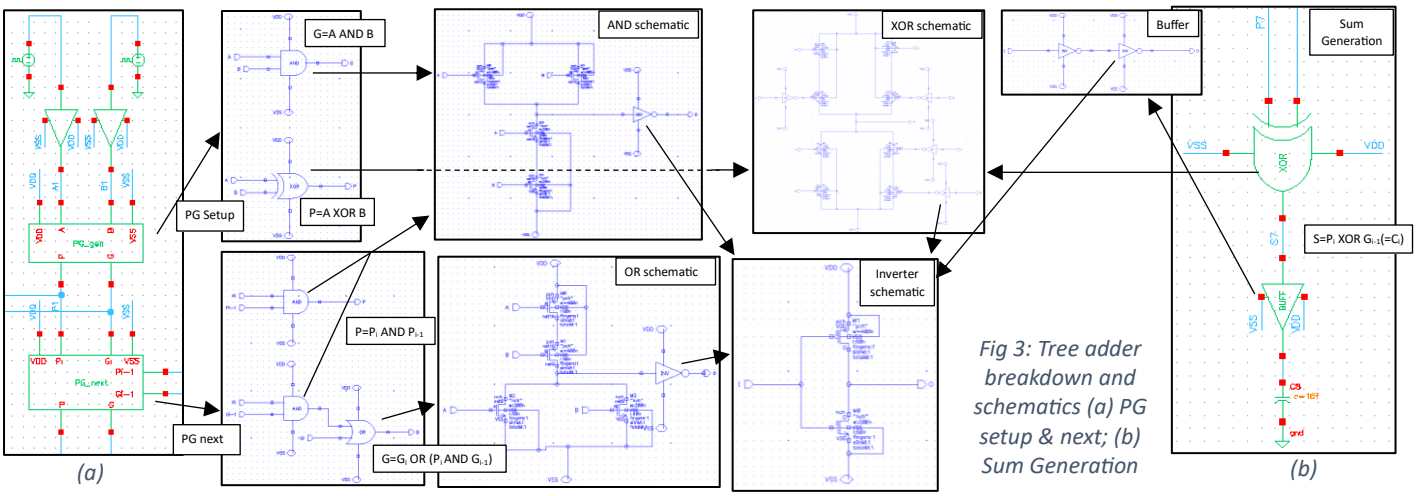


Fig 3: Tree adder breakdown and schematics (a) PG setup & next; (b) Sum Generation

The FA architecture is given in Fig2b, it is built with 3 stages – PG Setup, PG next, and Sum Generation. The breakdown of the structure to the transistor level is given in fig 3a, b. These gates are in 'proj3_cadence/proj3_gates'

Simulation results and analysis

1. Functional waveforms

Three vector additions are performed corresponding to:

- Vector A = 1111 1111 1111 1111 + 0000 0000 0000 0001 = 1 0000 0000 0000 0000
- Vector B = 1111 1111 1111 1111 + 1111 1111 1111 1111 = 1 1111 1111 1111 1110
- Vector C = 1010 1010 1010 1010 + 1010 1010 1010 1010 = 1 0101 0101 0101 0100

The functional waveforms for three vectors are shown in Figure 4.

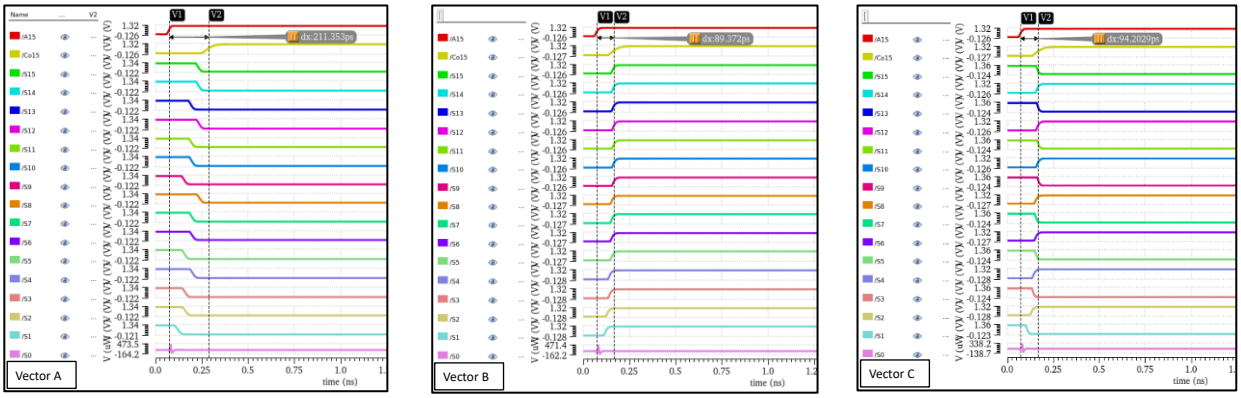


Fig 4: Waveform depicting $S_{0\text{-}15}$ and C_{O15} for vectors A, B and C

2. Global mis-match: corner/temperature

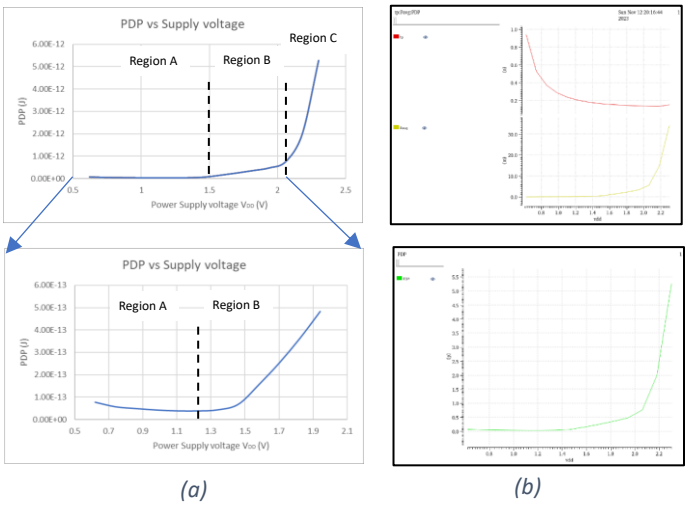
The delay, power and PDP under the three corner simulations is given in table 2. The SS process corner coupled with high temperature (85°C) has the maximum delay (due to decrease in electron mobility at high T). Vector A has the maximum delay, because LSB inputs are of the form 1 and 1 which results in G=A.B=1 in the setup ie generate. Hence the entire block is dependent on the propagate logic: goes through P= P_i AND P_{i-1} multiple times as rest inputs are 1.0=0 (worst case occurs when Carry is generated in LSB and has to be propagated throughout the circuit).

Table 2: Delay, power and PDP of tree adder under three corner simulations & temperatures

	Delay (ps) (=t_P)			Power (uW) (=P_{AVG}=I_{AVG}*V_{DD})			PDP (1e-18 J) (=P_{AVG}*t_P)		
	FF (T=-25°C)	TT (T=27°C)	SS (T=85°C)	FF (T=-25°C)	TT (T=27°C)	SS (T=85°C)	FF (T=-25°C)	TT (T=27°C)	SS (T=85°C)
Vector A	167.8	210.8	274.5	211.3	178.7	163.2	35456.14	37669.96	44798.4
Vector B	74.95	93.14	120.2	327.1	298.8	284.5	24516.145	27830.232	34196.9
Vector C	74.95	93.14	120.2	289.3	259.3	243.3	21683.035	24151.202	29244.66

3. PDP vs. power-supply voltage

It was observed by parametric analysis that the circuit works for 0.611V<V_{DD}<2.4V without major fluctuations in the output waveforms. As seen (fig 5b), the delay is extremely high for low V_{DD} (drive voltages on the gates are reduced, and amount of current passing is reduced) and delay decreases as V_{DD} increases. Trend of Power is opposite. Clear PDP graphs are depicted in fig5a. PDP first decreases (region A) then increases linearly (region B) then almost exponentially (region C). Upon closer inspection of Region A and B; for our design, V_{DD} near 1.2V achieves a good balance between power and delay.



(a) *(b)*

Fig 5: (a) clear PDP graphs; (b) Delay, Power and PDP graphs from Cadence

Conclusion

4 Adder architectures were studied, and a worst case delay of t_P=274.5ps was achieved using the Radix-2 Kogge Stone tree adder which is much lesser than the requirement of t_P=400ps. This can be further decreased by optimizing the Sum and C_{OUT} paths further. The variation of PDP with V_{DD} was also studied and an optimum of 1.2V was deduced.