ECE 637 Project 2: 1 bit Full Adder

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Introduction:

A 1 bit full adder has been designed in this project, aiming to achieve equal rise and fall time propagation delays (t_{pHL}=t_{pLH}) via an inverter. Subsequently, the layout was created and post layout simulations along with corner simulations were performed on the full adder.

Transistor sizing and Full adder design:

To equalize the propagation delays in the 1 bit adder, firstly the pMOS to nMOS transistor size ratio was to be finalised using the inverter (using 'project2_cadence/proj2_inv_sizing'). The schematic and testbench used for the inverter are shown fig 1 and 2. Via hit and trial, different sizes of the pMOS (with nMOS size fixed to be the minimum width = 120nm) and their associated delays were observed as shown in table 1. It was concluded that the delays would be equal when 200nm<W_P<210nm. Hence, by obtaining a parametric sweep of the pMOS size (W_P) (shown in fig 3), and some more delay calculations (shown in table 2, and keeping error < 0.0005ps), equal rise and fall delays were achieved (t_{pHL}=t_{pLH}=7.263ps) at transistor sizes W_N=120nm and W_P=205.9nm.

Table 1: Propagation delays associated with different W_P

W_P /wn	W_P	t_{pHL} (ps)	t_{pLH} (ps)	| t_{pHL} - t_{pLH} |
1	120nm	6.32348p	8.69503p	2.37155
1.67	200nm	7.1993p	7.3152p	0.1159
1.75	210nm	7.30643p	7.22851p	0.07792
2	240nm	7.62879p	7.02837p	0.60042

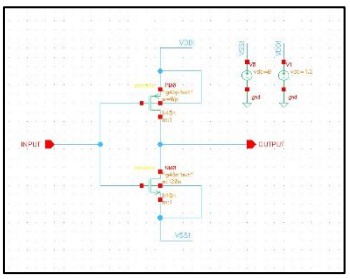

Fig 1: Inverter schematic

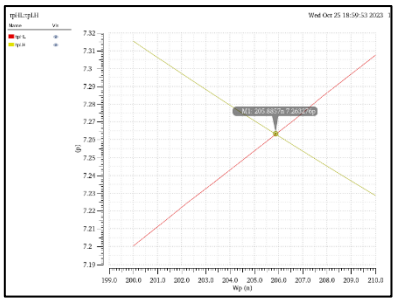

Fig 3: Parametric sweep of W_P

Table 2: Propagation delays after parametric sweep of W_P

W_P/W_N	W_P	t_{pHL} (ps)	t_{pLH} (ps)	| t_{pHL} - t_{pLH} |
1.715	205.8nm	7.26247	7.264	0.00153
1.715417	205.85nm	7.263	7.26357	0.00057
1.715833	205.9nm	7.26353	7.26314	0.00039
1.7167	206n	7.26459	7.26228	0.00231

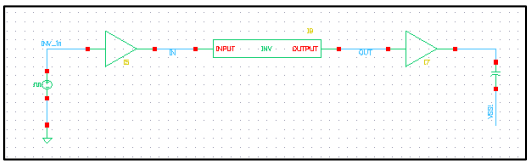

Fig 2: Inverter testbench

Hence, the final reduced size of the full adder is W_P/W_N = 205.9/120 = 1.71583. The full adder was sized accordingly as shown in fig 4 ensuring the reduced size is met. The schematic of the full adder is shown in fig 5 (saved in 'project2_cadence/proj2_schem_sized_5'), and fingers were used to size the nMOS and pMOS in order to ensure they fit in the layout.

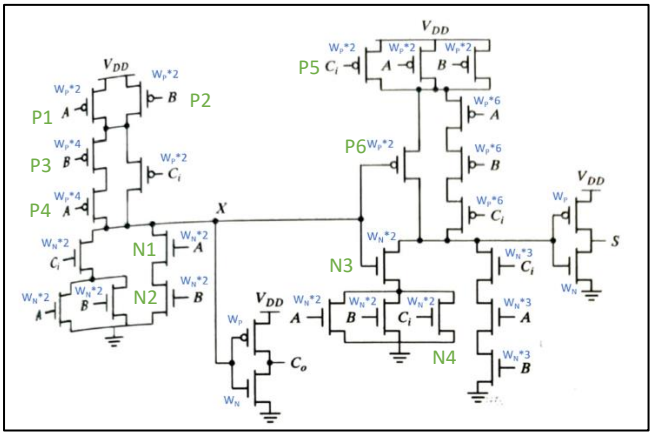

Fig 4: Transistor sizes

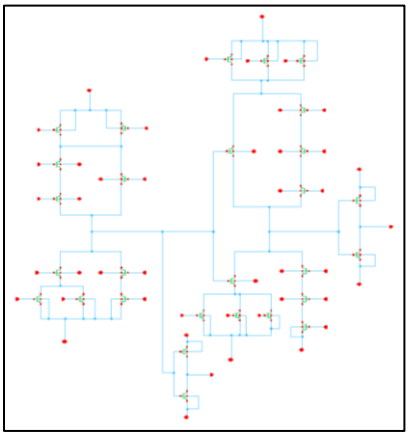

Fig 5: 1b Full Adder schematic

The testbench's schematic is shown in fig 6 (saved in 'project2_cadence/proj2_schem_tb_buff_sized_2'), and the waveform obtained with all the possible combinations in the truth table is shown in fig 7. The delay values for both sum and carry out are shown in tables 3 and 4, and it is seen that sum has the maximum delay corresponding to the (010 10 ⟶ 011 01 ⟶ 100 10) transition with equal delays.

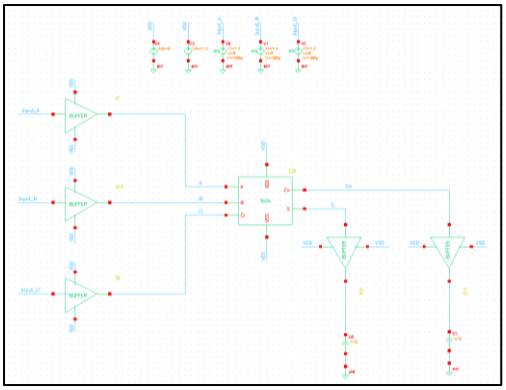

Fig 6: 1b Full Adder testbench schematic

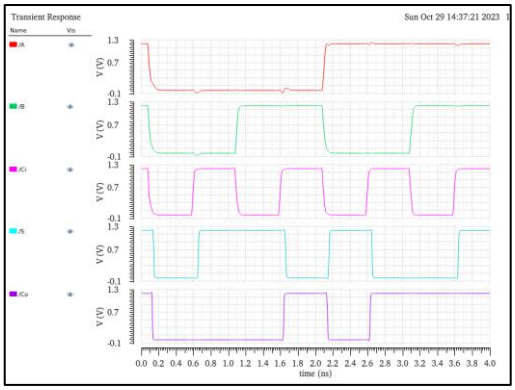

Fig 7: 1b Full Adder output

Table 3 (a) & (b): t_p for fig 7 for Sum

Transition (ABC_i SC_O)	t_{pHL} (ps)
(111 11 → 000 00)	53.5955
(010 10 → 011 01)	63.8625
(100 10 → 101 01)	55.504

Transition (ABC_i SC_O)	t_{pLH} (ps)
(000 00 → 001 10)	60.212
(011 01 → 100 10)	63.249
(110 01 → 111 11)	46.9104

Table 4 (a) & (b): t_p for fig 7 for C_O

Transition (ABC_i SC_O)	t_{pHL} (ps)
(111 11 → 000 00)	38.3613
(011 01 → 100 10)	45.9431

Transition (ABC_i SC_O)	t_{pLH} (ps)
(010 10 → 011 01)	40.8786
(100 10 → 101 01)	32.2138

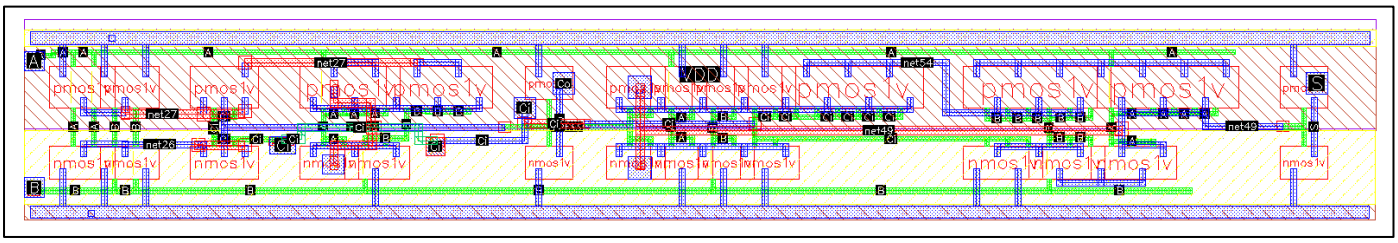

Fig 8: 1b Full Adder layout

Table 5 (a) & (b): t_p for post layout for Sum

Transition (ABC_i SC_O)	t_{pHL} (ps)
(111 11 → 000 00)	100.55p
(010 10 → 011 01)	127.004p
(100 10 → 101 01)	117.211p

Transition (ABC_i SC_O)	t_{pLH} (ps)
(000 00 → 001 10)	105.23p
(011 01 → 100 10)	127.884p
(110 01 → 111 11)	82.2434p

Table 6 (a) & (b): t_p for post layout for C_O

Transition (ABC_i SC_O)	t_{pHL} (ps)
(111 11 → 000 00)	67.0028p
(011 01 → 100 10)	91.4495p

Transition (ABC_i SC_O)	t_{pLH} (ps)
(010 10 → 011 01)	84.8352p
(100 10 → 101 01)	71.213p

The layout of the full adder is shown in fig 8, and it is DRC and LVS free (shown in figs 9 and 10). As mentioned earlier, the concept of fingers was used to reduce the vertical heights of the transistors in the layout. The propagation delays of the post layout simulation are shown in tables 5 and 6 and the maximum delay is corresponding to the (010 10 → 011 01 → 100 10) transition with equal delays, similar to the schematic simulation.

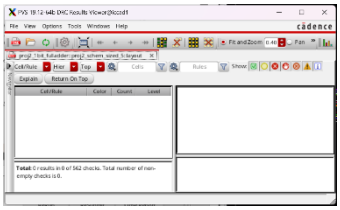

Fig 9: DRC check

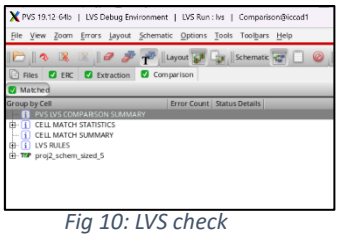

Fig 10: LVS check

Propagation delays:

The propagation delays of the schematic and post layout simulations for Sum and Carry Out for the corner case of TT at 27° covering all input combinations **(except those that do not result in a change in the output)** are presented in tables 7 and 8. A comparison column is also included that shows the drastic change in the delay due to addition of parasitic capacitances in the post layout. As seen by the highlighted blue delays, the maximum delay case or the slowest input combination case in both Sum and Carry out is the (001 10 ↔ 110 01) transition.

Table 7: Propagation delay for Sum for TT 27° for all input combinations

		001 10			010 10			100 10			111 11		
ABC_i SC_O	Delay type (ps)	Schematic	Post Layout	Comparison	Schematic	Post Layout	Comparison	Schematic	Post Layout	Comparison	Schematic	Post Layout	Comparison
000 00	t_{pHL}	42.369	81.5244	92.415%	39.6155	84.1987	112.540%	32.4291	73.0647	125.306%	46.0013	82.9224	80.261%
	t_{pLH}	60.8797	105.901	73.951%	50.9197	96.9521	90.402%	34.8694	72.4225	107.696%	51.8761	90.3535	74.172%
	tp	51.62435	93.7127	81.528%	45.2676	137.767	204.339%	33.64925	72.7436	116.182%	48.9387	86.63795	77.034%
011 01	t_{pHL}	66.5818	135.788	103.942%	63.2237	127.66	101.918%	60.5214	124.224	105.256%	36.5987	79.3336	116.766%
	t_{pLH}	74.7557	145.925	95.203%	72.7808	140.793	93.448%	57.2423	128.702	124.837%	46.4473	94.456	103.362%
	tp	70.66875	140.8565	99.319%	68.00225	134.2265	97.385%	58.88185	126.463	114.774%	41.523	86.8948	109.269%
101 01	t_{pHL}	55.531	116.368	109.555%	58.1197	118.43	103.769%	54.742	117.6	114.826%	44.4795	98.0297	120.393%
	t_{pLH}	51.4596	105.883	105.759%	57.7209	114.162	97.783%	55.4142	112.774	103.511%	42.4223	86.4455	103.774%
	tp	53.4953	111.1255	107.729%	57.9203	116.296	100.786%	55.0781	115.187	109.134%	43.4509	92.2376	112.280%
110 01	t_{pHL}	77.7068	147.517	89.838%	68.2702	142.349	108.508%	69.9992	146.294	108.994%	46.6281	90.697	94.511%
	t_{pLH}	75.9959	150.204	97.648%	63.7095	120.76	89.548%	64.8885	129.24	99.172%	47.6515	83.119	74.431%
	tp	76.85135	148.8605	93.699%	65.98985	131.5545	99.356%	67.44385	137.767	104.269%	47.1398	86.908	84.362%

Table 8: Propagation delay for C_O for TT 27° for all input combinations

ABCi SC_O		011 01			101 01			110 01			111 11		
	Delay type (ps)	Schematic	Post Layout	Comparison	Schematic	Post Layout	Comparison	Schematic	Post Layout	Comparison	Schematic	Post Layout	Comparison
000 00	t_{pHL}	33.8433	62.459	84.554%	28.7744	56.4003	96.009%	33.4773	63.907	90.897%	31.5766	57.1286	80.921%
	t_{pLH}	50.1677	94.429	88.227%	38.8162	75.7527	95.157%	53.27	110.145	106.767%	30.2572	55.9383	84.876%
	tp	42.0055	78.444	86.747%	33.7953	66.0765	95.520%	43.37365	87.026	100.643%	30.9169	56.53345	82.856%
001 10	t_{pHL}	42.1497	86.2106	104.534%	36.4511	76.9987	111.238%	45.6463	91.5202	100.499%	38.5768	79.9029	107.127%
	t_{pLH}	46.3521	94.5938	104.077%	35.5084	75.092	111.477%	50.258	100.553	100.074%	25.156	51.8159	105.978%
	tp	44.2509	90.4022	104.295%	35.97975	76.04535	111.356%	47.95215	96.0366	100.276%	31.8664	65.8594	106.673%
010 10	t_{pHL}	37.605	75.6215	101.094%	34.04	67.4687	98.204%	39.601	77.6628	96.113%	34.5949	66.6986	92.799%
	t_{pLH}	41.5703	85.0863	104.681%	37.3356	74.2987	99.002%	46.8021	97.7293	108.814%	25.7766	50.5744	96.203%
	tp	39.58765	80.3539	102.977%	35.6878	70.8837	98.622%	43.20155	87.69605	102.993%	30.18575	58.6365	94.252%
100 10	t_{pHL}	38.5512	90.595	134.999%	36.0049	74.6626	107.368%	45.4853	90.7919	99.607%	35.7385	79.3848	122.127%
	t_{pLH}	42.656	92.1782	116.097%	32.7105	71.4629	118.471%	47.5034	99.5743	109.615%	21.6873	52.443	141.814%
	tp	40.6036	91.3866	125.070%	34.3577	73.06275	112.653%	46.49435	95.1831	104.720%	28.7129	65.9139	129.562%

(here average propagation delay $t_p = \frac{t_{pHL}+t_{pLH}}{2}$)

The reasons why the (001 10 ↔ 110 01) transition (for both schematic and post layout) has the maximum delay are:

- The sum has to wait for the result of the carry out, resulting in a larger delay for sum.
- In the schematic, when the C_O transitions from 0 to 1 (C_O' changed from 1 to 0), (ie 001 to 110 input), the series transistors N1 and N2 (according to fig 4) create the discharging path to bring the voltage down. All the other transistors in the PDN are off and there is only one series path operating, which results in a large resistance and hence a higher delay. When the sum transitions from 1 to 0 (S' 0⟶1), only the series transistors P5 and P6 create the charging path to bring the voltage up, resulting in higher resistance and hence higher delay (fig 11).
- Similarly, when the C_O transitions from 1 to 0 (C_O' changed from 1 to 0), (ie 110 to 001 input), the series transistors P1, P2, P3, P4 (highest resistance path) create the charging path to bring the voltage up, and for sum the series transistors N3 and N4 create the discharging path to bring the voltage down. All other transistors are in the respective PDN and PUN are off resulting in higher resistance and hence higher delay (fig 12).
- The post layout simulations have higher delays than their schematic counterparts due to the extra parasitic capacitances as shown in the table. The input combo and reason for highest delay is same as schematic result.

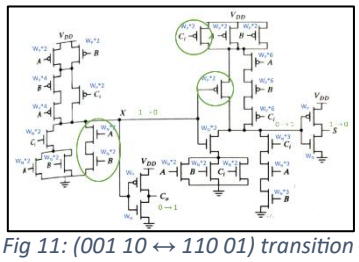

Fig 11: (001 10 ↔ 110 01) transition

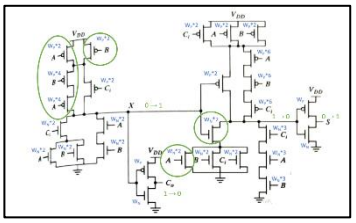

Fig 12: (110 01 ↔ 001 1) transition

Global mismatch (corner simulations):

Tables 4 and 5 record the propagation delays (high to low, low to high and average), average power, and Power Delay Product of the schematic and post layout simulations for the process corners for temperature -25° and 27° respectively. These results are tabulated for the slowest input combination, ie the input combination that resulted in the highest delay: (001 10 ↔ 110 01) transition (testbench used: 'project2_cadence/proj2_schem_tb_buff_sized_4').

Table 9: Constraints for process corners at T=-25°C

Temperature ⟶	T=-25°C									
Corners ⟶	TT		SS		FF		SF		FS	
Values	Schematic	Post layout	Schematic	Post layout	Schematic	Post layout	Schematic	Post layout	Schematic	Post layout
t_{pHL} (ps)	63.8997	123.641	78.822	154.219	53.3754	102.391	70.8998	130.668	59.1775	120.269
t_{pLH} (ps)	60.2158	118.413	74.2846	151.771	50.6986	96.6695	60.2936	121.104	63.1375	119.378
tp (ps)	62.05775	121.027	76.5533	152.995	52.037	99.53025	65.5967	125.886	61.1575	119.8235
P_{AVG} (µW)	7.67918	13.0476	6.70338	12.0331	10.1691	15.6006	7.71544	13.0747	7.88492	13.2587
PDP (1e-18 J)	476.553	1579.112	513.166	1841.004	529.169	1552.732	506.107	1645.922	482.222	1588.704

Table 10: Constraints for process corners at T=27°C

Temperature ⟶	T=27°C									
Corners ⟶	TT		SS		FF		SF		FS	
Values	Schematic	Post layout	Schematic	Post layout	Schematic	Post layout	Schematic	Post layout	Schematic	Post layout
t_{pHL} (ps)	77.7068	147.517	94.875	182.653	65.7857	123.773	84.8062	154.963	73.4134	145.173
t_{pLH} (ps)	75.9959	150.204	93.2479	186.168	64.5581	120.908	77.5622	151.877	77.6885	145.629
tp (ps)	76.85135	148.8605	94.06145	184.4105	65.1719	122.3405	81.1842	153.42	75.55095	145.401
P_{AVG} (µW)	10.7677	16.1676	8.27189	13.6354	15.2342	20.6942	10.896	16.2898	11.1967	16.5936
PDP (1e-18 J)	827.512	2406.717	778.066	2514.511	992.842	2531.739	884.583	2499.181	845.921	2412.726

$$Average\ Power = P_{AVG} = Average\ Current * Supply\ voltage = \ average\ (I_{VDD}) * V_{DD}$$

$$Power\ Delay\ Product = PDP = Average\ power * Average\ delay = \ P_{AVG} * t_p$$

Local Mismatch (MC simulation):

The Monte Carlo simulation was performed for the schematic and post layout to include random mismatch, and the results are tabulated in table 11. The average propagation delay and power statistics for 100 at T=27° samples of Monte Carlo simulations according to the graphs in fig 13 and 14 are summarised in table 12 for schematic. Figures 13 and 14 are the statistical distributions of the average delay and power of the schematic after running the Monte Carlo Simulations.

Table 11: Constraints for process MC at T=27°C

	Monte Carlo	
Values	Schematic	Post layout
t_{pHL} (ps)	77.7068	147.739
t_{pLH} (ps)	75.9959	146.418
tp (ps)	76.85135	147.0785
P_{AVG} (µW)	10.7677	16.1676
PDP (1e-18 J)	827.512	2377.906

Table 12: MC analysis for delay and power

Values	Min	Max (worst case)	Mean	Standard Deviation
tp (ps)	69.75	84.2	77.3459	2.7343
P_{AVG} (µW)	10.13	11.79	10.8742	0.327

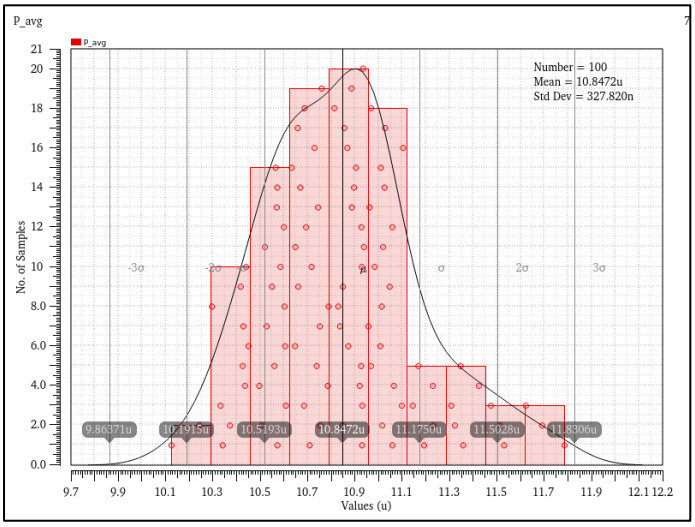

Fig 13: MC analysis average power distribution

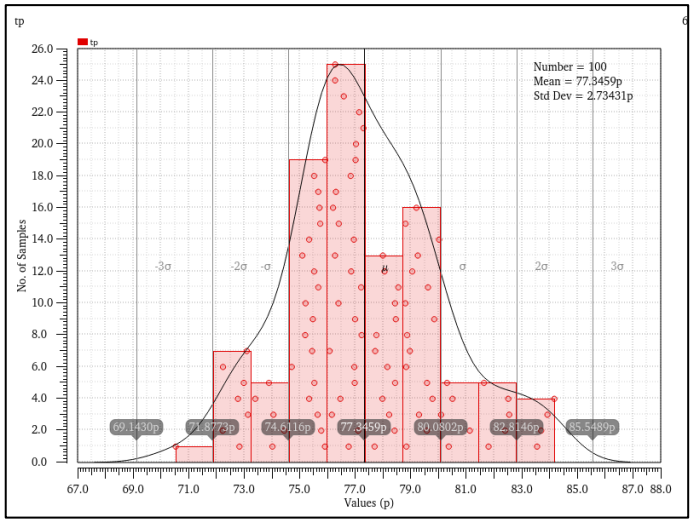

Fig 14: MC analysis propagation delay distribution

Conclusion:

- An inverter was sized in order to get equal rise and fall times delays and the corresponding W_P and W_N were used to design the 1 bit full adder. A graph was plotted that had all the input combinations and it was confirmed that the rise and fall times delays were indeed equal
- Subsequently, the DRC and LVS clear layout of the full adder was created.
- Schematic and post layout simulations were performed under TT 27°C for all input combinations and the highest delay/slowest input combination was identified and explained
- This slowest input combination was used to run the corner simulations for delay, power and PDP, and obtain the MC distributions to identify the worst cases.