

FPGA ASSIGNMENT

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2. $W = 1, X = 0, Y = 1, Z = 0$
3. $W = 0, X = 1, Y = 1, Z = 0$
4. $W = 1, X = 1, Y = 0, Z = 0$

2 Introduction

The above diagram is a 4:1 multiplexer where W, X, Y, Z are the inputs of the multiplexer and A is the output of the multiplexer. R, S are the select lines of the multiplexer, which means:

1. For $R = 0, S = 0$, the first input line W is selected.
2. For $R = 0, S = 1$, the second input line X is selected.
3. For $R = 1, S = 0$, the third input line Y is selected.
4. For $R = 1, S = 1$, the fourth input line Z is selected.

Therefore, the resultant output expression of the multiplexer is $R'S'W + R'SX + RS'Y + RSZ$.

3 Components

Component	Value	Quantity
LED	-	2
Vaman	-	1
Jumper Wires	M-M	20
Breadboard		1

Table 1: contents

4 Truth Table

1 Problem

(GATE EC-2022)

Q.19. Consider the 2-bit multiplexer(MUX) shown in the figure. For output to be the XOR of R and S , the values for W, X, Y and Z are ?

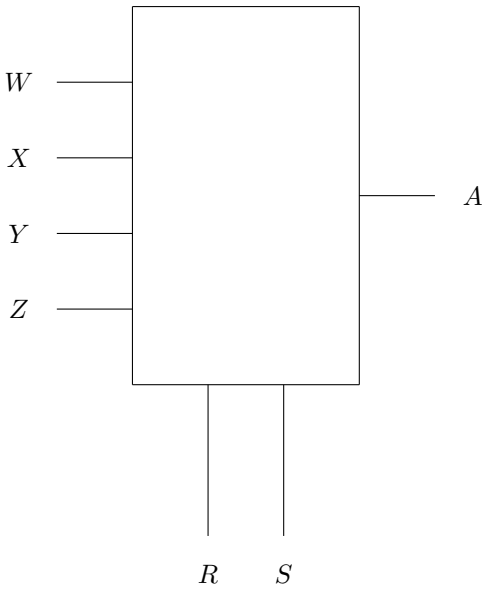


Figure 1: mux

1. $W = 0, X = 0, Y = 1, Z = 1$

Truth table		
R	S	B
0	0	0
0	1	1
1	0	1
1	1	0

```
end
endmodule
```

Table 2: truth table

5 K-map

The K-map for this truth table will be a two variable K-map and it will be as follows:

		<i>R</i>	
		0	1
<i>S</i>	0	0	1
	1	1	0

Figure 2: k-map

6 Hardware

1. Set the GPIO pins: 2,3,4,5,6,7 of Vaman as inputs.
2. Set the GPIO pin 10,11 of Vaman as output.
3. Read the input pins after connecting the Vcc and GND pins.
4. Verify the outputs using the truth table.

7 Software

The embedded code for the given circuit is

```
module helloworldfpga(
    input  wire W,
    input  wire X,
    input  wire Y,
    input  wire Z,
    input  wire R,
    input  wire S,
    output wire A,
    output wire B
);

    always @(*)
    begin
        A = (!R && !S && W) || (!R && S && X) || (R && !S && Y) || (R && S && Z);
        B = (!R && S) || (R && !S);
    end
endmodule
```