ASSEMBLY ASSIGNMENT

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Contents

1 Problem

(GATE EC-2020)

Q.No 50. For the components in the sequential circuitshown below,tpd is the propagation delay, tsetup is the setup time, and thold is the hold time. the maximum clock frequency(rounded off to the nearest integer),at which the given circuit can operate reliably, is MHz.

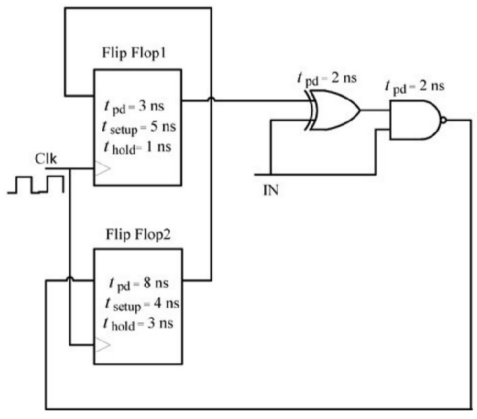

Figure 1:

2 Components

The components required are given in Table 1

Component	Value	Quantity
Arduino UNO	-	1
Breadboard	-	1
7447 IC	-	1
Seven segment display	-	1
Resistor	200ohms	1
Jumper wires	M-M	20

Table 1:

2.1 Arduino

The Arduino Uno has some ground pins, analoginput pins A0-A3 and digital pins D1-D13 that can be used for both input as well as output. It also has two power pins that can generate 3.3V and 5V.

2.2 Seven Segment Display

The seven segment display has eight pins, a,b, c, d, e, f, g and dot that take an active LOW input, i.e. the LED will glow only if the input is connected to ground. Each of these pins is connected to an LED segment. The dot pin is reserved for the · LED.

3 Implementation

3.1 Truth Table

From the above equation, truth table is given in Table 2

3.2 K-map

From the above truth table, Fig 2 represents the K-map:

IN	Q1	Q2	Qy
0	0	0	1
0	0	1	-
0	1	0	-
0	1	1	1
1	0	0	0
1	0	1	-
1	1	0	-
1	1	1	1

Table 2:

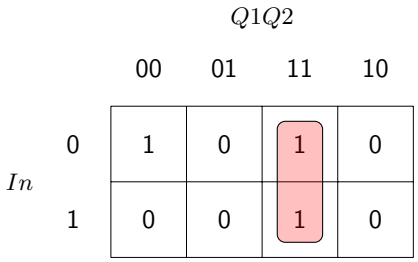

Figure 2:

3.3 Boolean Expression

By Solving the above K-map, we get a boolean equation as: $Qy = Q1Q2 + Q1'Q2'In'$
$Qy = Q1Q2 + In'$

4 Hardware

1. Connect the arduino to computer and upload the code in to the arduino.
2. Make 2,3,4 as input pins and 8,9,10 as output pins.
3. By changing inputs check the corresponding outputs.

5 Software

```
.include "/sdcard/Download/fwc/assembly/
    setup/m328Pdef/m328Pdef.inc"


ldi r16,0b11100011
out DDRD,r16
ldi r16,0b10000111
out DDRB,r16

loop:
ldi r30,0b00000000
out PORTB,r30
ldi r31,250

call delay

ldi r30,0b00000001
out PORTB,r30

in r17,PIND
mov r18,r17
lsr r18
lsr r18

mov r19,r17
lsr r19
lsr r19
lsr r19

mov r20,r17
lsr r20
lsr r20
lsr r20
lsr r20

eor r19,r18
and r19,r18

ldi r21,0b00000001
and r19,r21
mov r24,r19


ldi r22,0b00000111
loopt:
lsl r19
dec r22
brne loopt

out PORTB,r19

mov r23,r20
lsl r23
lsl r24
lsl r24
or r23,r24
or r23,r30

out PORTB,r23

rjmp loop

delay:
dec r30
brne delay
ret

Start:
rjmp Start
```