Fatima Jinnah Women University, Rawalpindi

"PROJECT"

COURSE :

COMPUTER ARCHITECTURE AND LOGIC DESIGN

SUBMITTED TO :

MAM IRUM MATLOOB

SUBMITTED BY :

LAIBA SOHAIL (2021-BSE-016)

TANZEELA ASGHAR (2021-BSE-032)

NEHA AMJAD (2021-BSE-024)

SECTION :

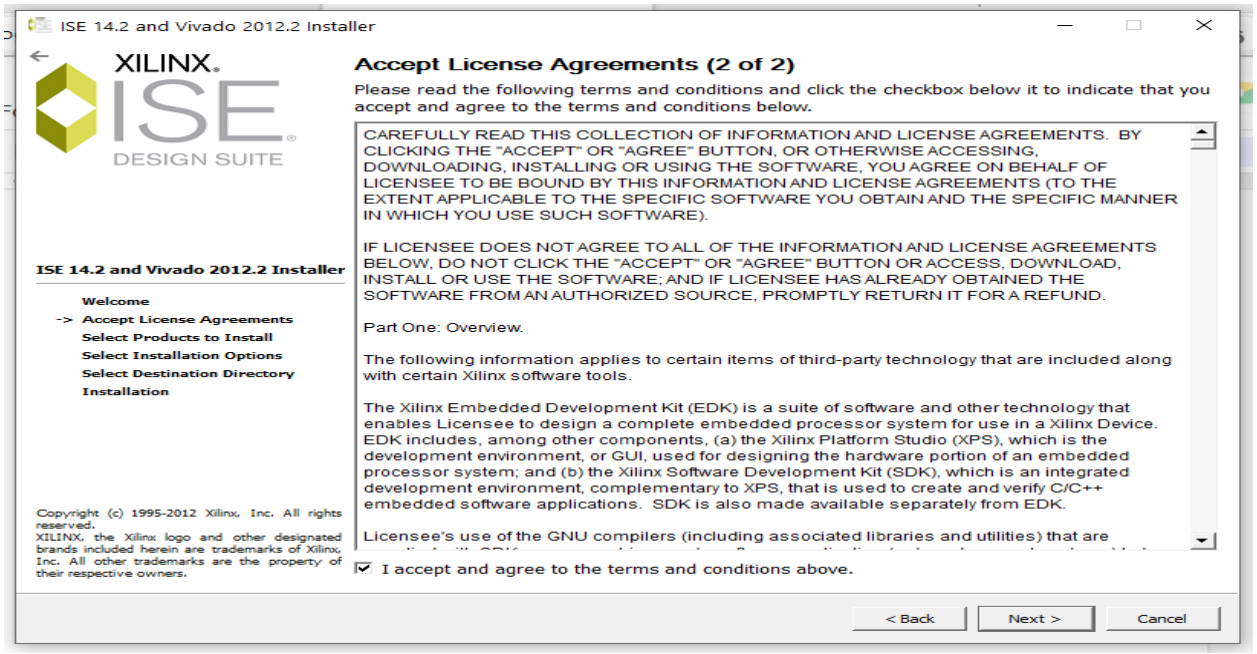
A

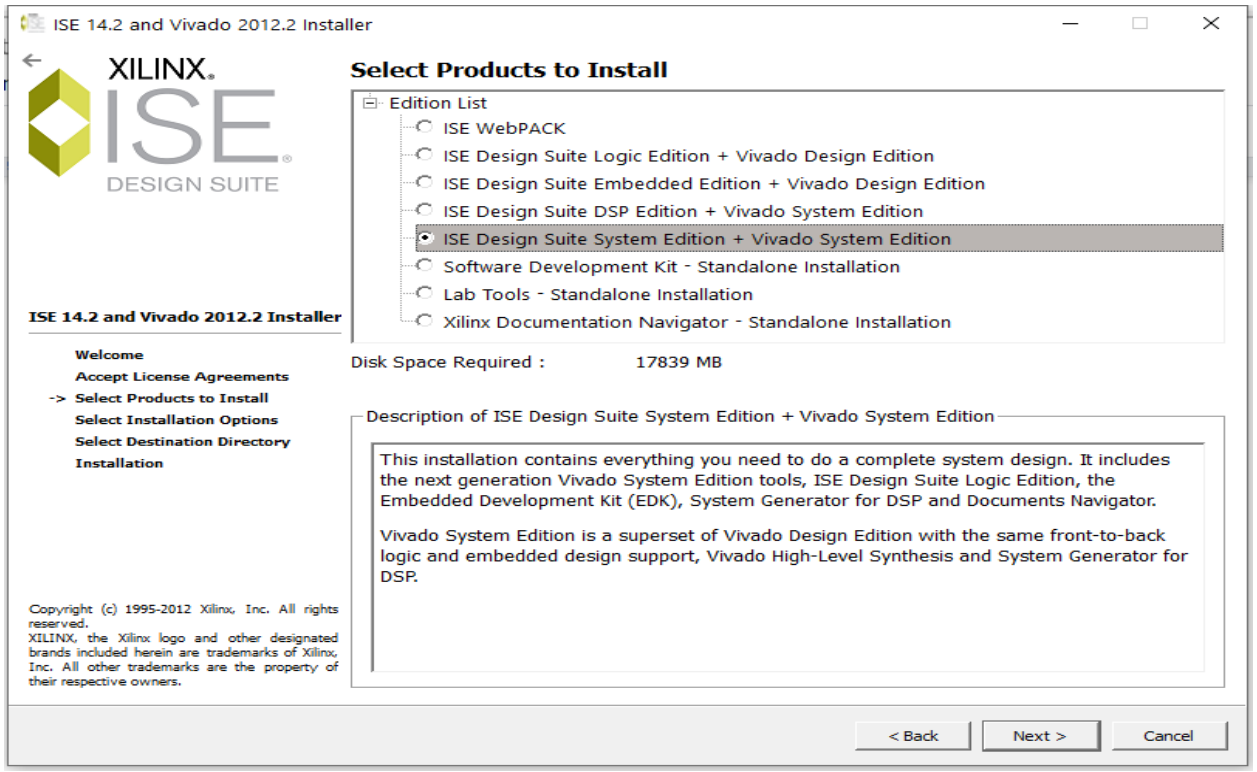
DATE :

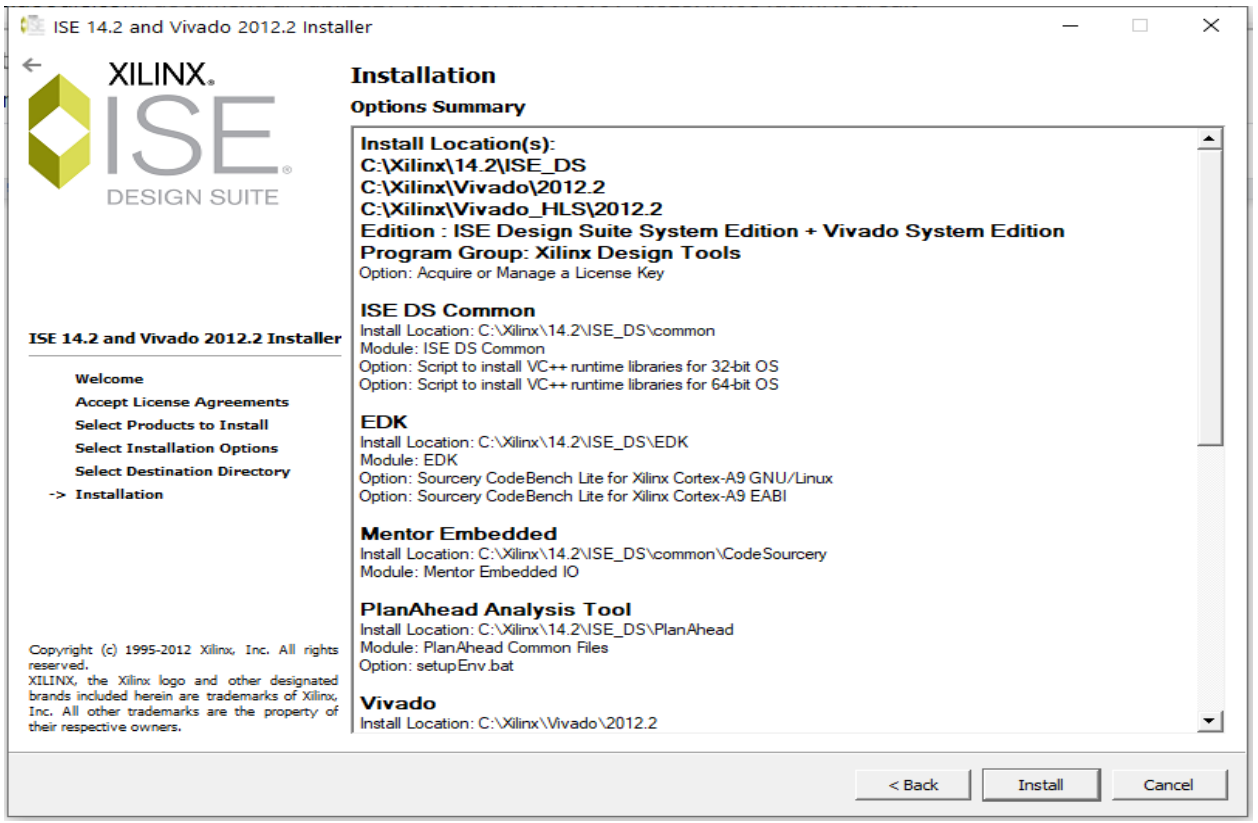
11/01/2023

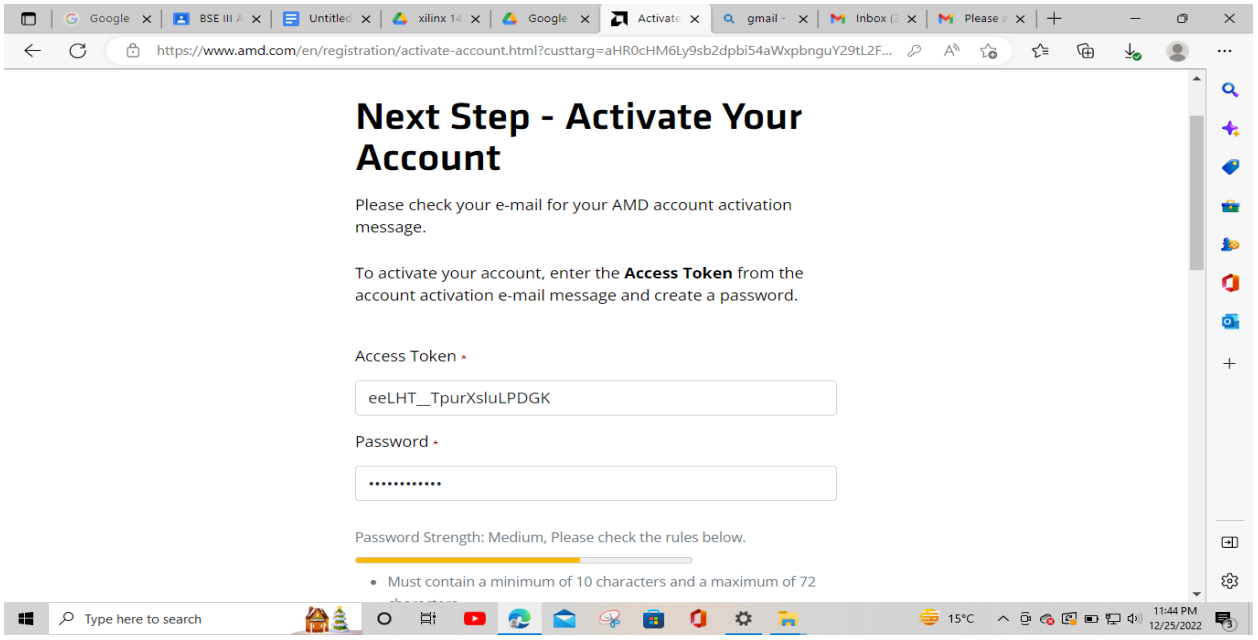
Simulate the instructions on abstract level.

INSTALLATION OF XILINX:



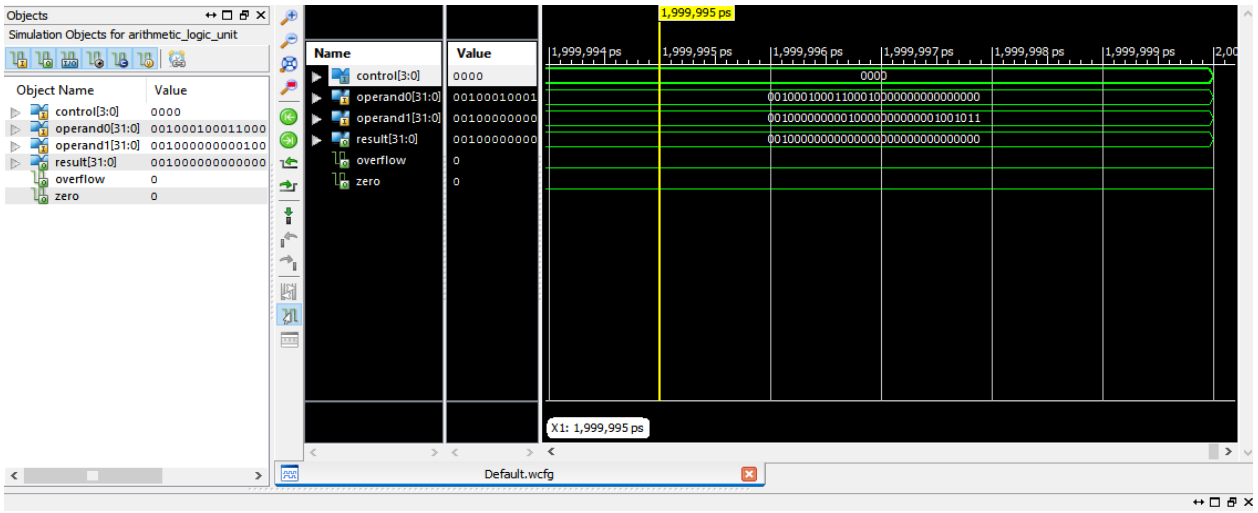



ISE 14.2 and Vivado 2012.2 Installer
XILINX
ISE
DESIGN SUITE
ISE 14.2 and Vivado 2012.2 Installer
Welcome
Accept License Agreements
Select Products to Install
Select Installation Options
Select Destination Directory
-> Installation
Copyright (c) 1995-2012 Xilinx, Inc. All rights reserved.
XILINX, the Xilinx logo and other designated brands included herein are trademarks of Xilinx, Inc. All other trademarks are the property of their respective owners.
Installation
Options Summary
Install Location(s):
C:\Xilinx\14.2\ISE_DS
C:\Xilinx\Vivado\2012.2
C:\Xilinx\Vivado_HLS\2012.2
Edition : ISE Design Suite System Edition + Vivado System Edition
Program Group: Xilinx Design Tools
Option: Acquire or Manage a License Key
ISE DS Common
Install Location: C:\Xilinx\14.2\ISE_DS\common
Module: ISE DS Common
Option: Script to install VC++ runtime libraries for 32-bit OS
Option: Script to install VC++ runtime libraries for 64-bit OS
EDK
Install Location: C:\Xilinx\14.2\ISE_DS\EDK
Module: EDK
Option: Sourcery CodeBench Lite for Xilinx Cortex-A9 GNU/Linux
Option: Sourcery CodeBench Lite for Xilinx Cortex-A9 EABI
Mentor Embedded
Install Location: C:\Xilinx\14.2\ISE_DS\common\CodeSourcery
Module: Mentor Embedded IO
PlanAhead Analysis Tool
Install Location: C:\Xilinx\14.2\ISE_DS\PlanAhead
Module: PlanAhead Common Files
Option: setupEnv.bat
Vivado
Install Location: C:\Xilinx\Vivado\2012.2
< Back
Install
Cancel

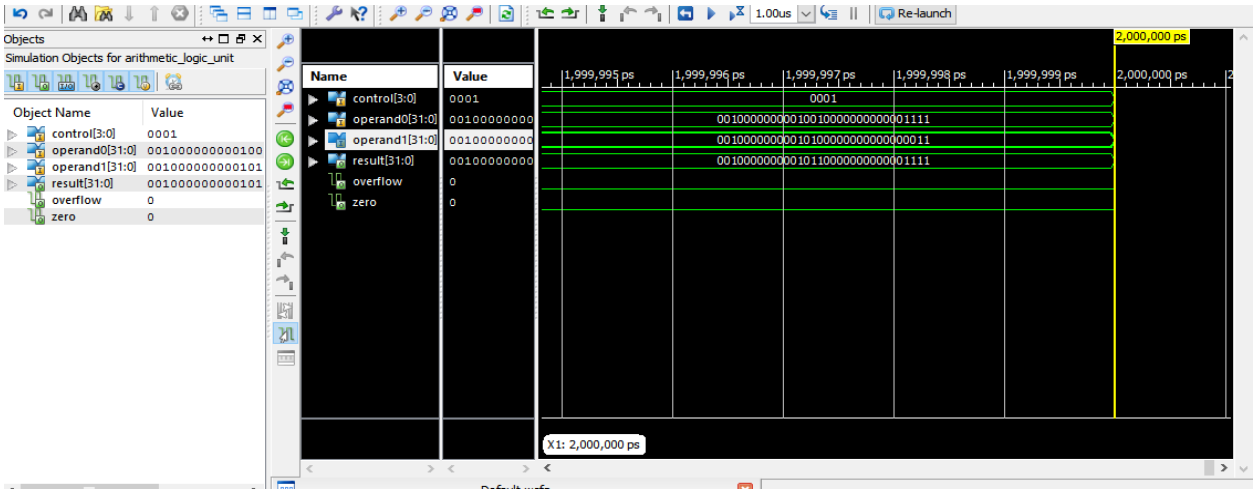

https://www.amd.com/en/registration/activate-account.html?custtarg=aHR0cHM6Ly9sb2dpbi54aWxpbnguY29tL2F...
Next Step - Activate Your Account
Please check your e-mail for your AMD account activation message.
To activate your account, enter the Access Token from the account activation e-mail message and create a password.
Access Token *
eeLHT__TpurXsluLPDGK
Password *
Password Strength: Medium, Please check the rules below.
Must contain a minimum of 10 characters and a maximum of 72
Type here to search
15°C
11:44 PM
12/25/2022

ARITHMETIC AND LOGIC UNIT:

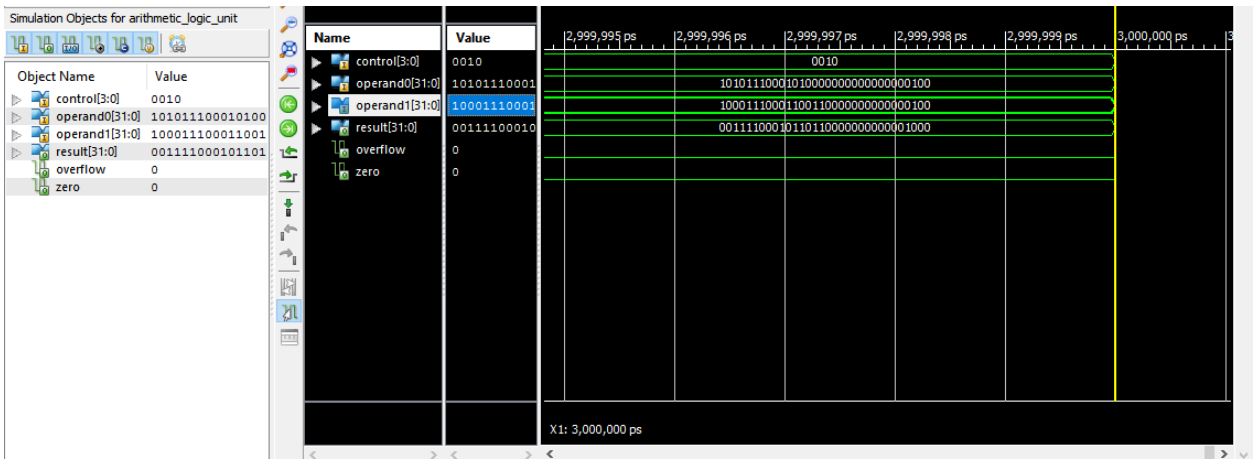
For AND:



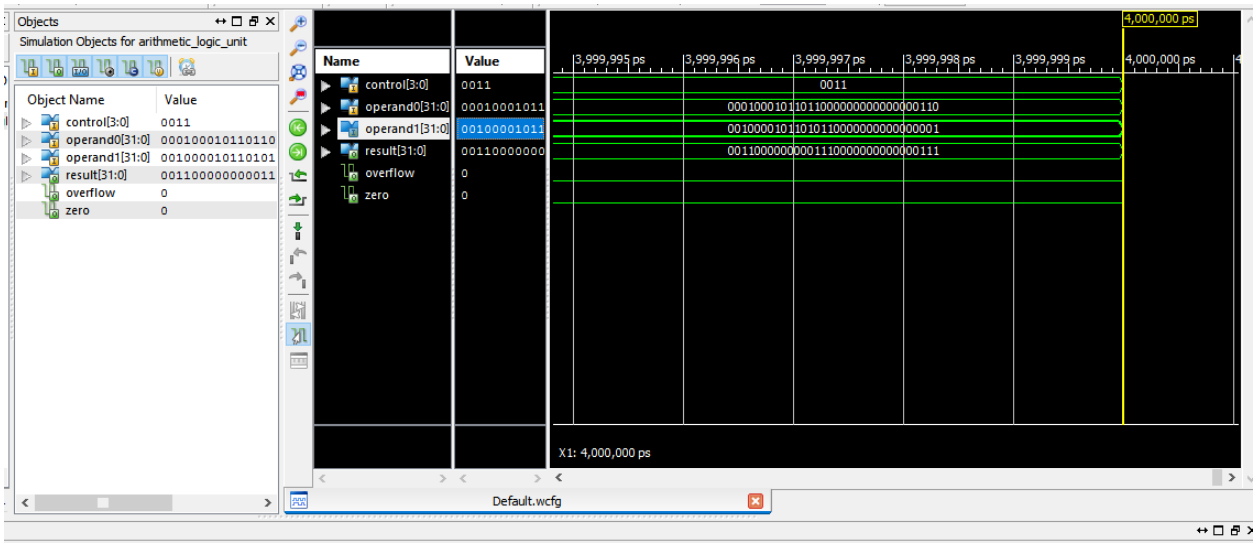
FOR OR:



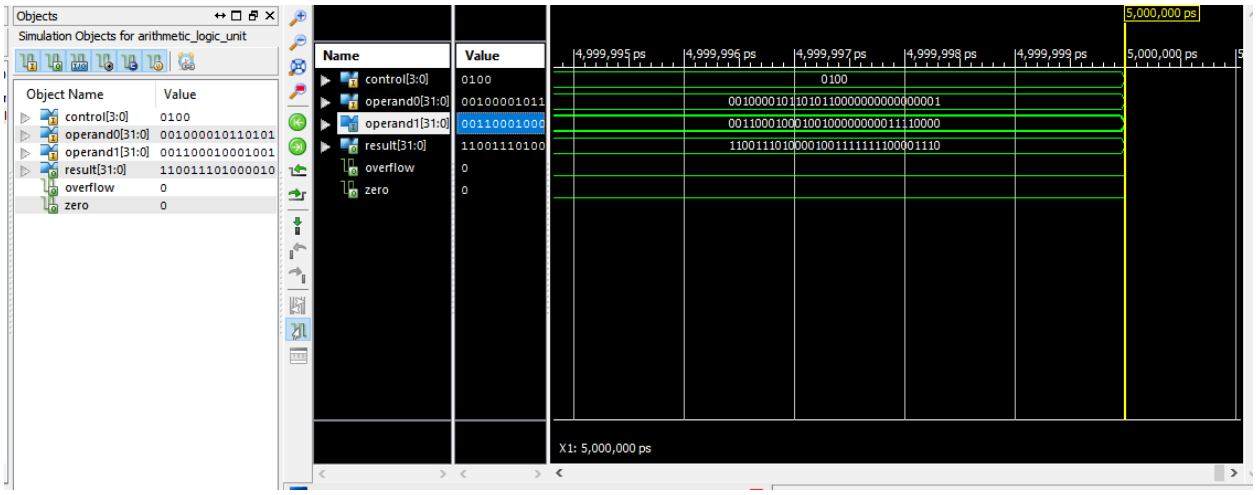
FOR ADD:



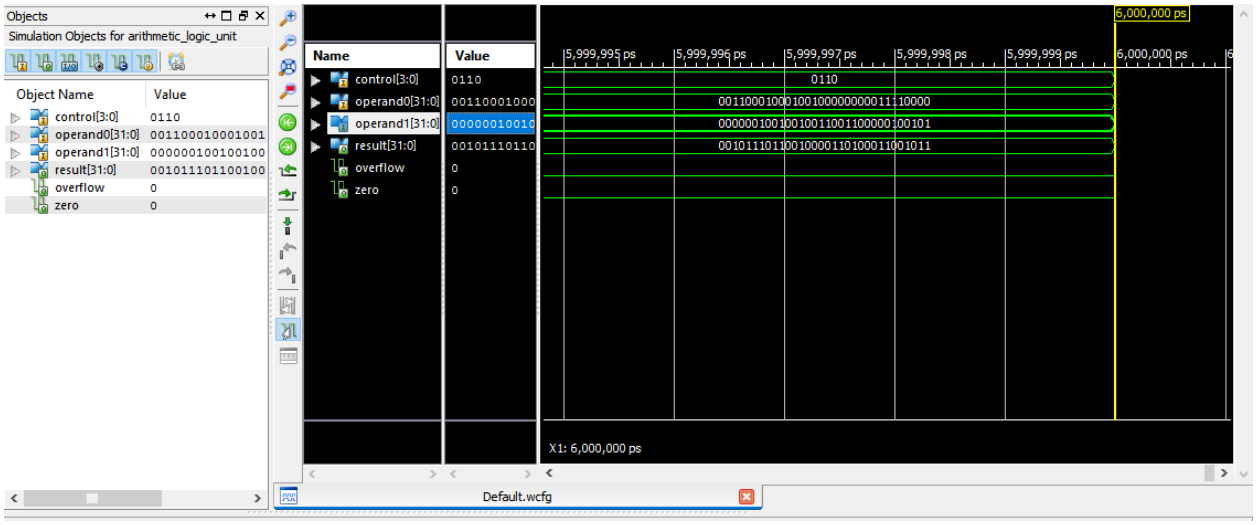
FOR XOR:



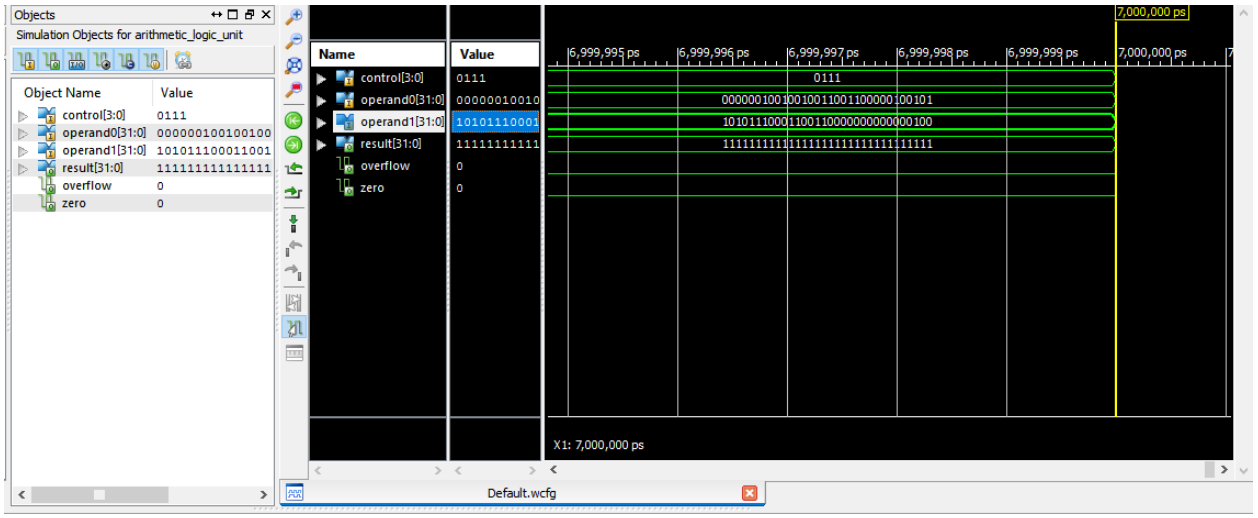
FOR NOR:



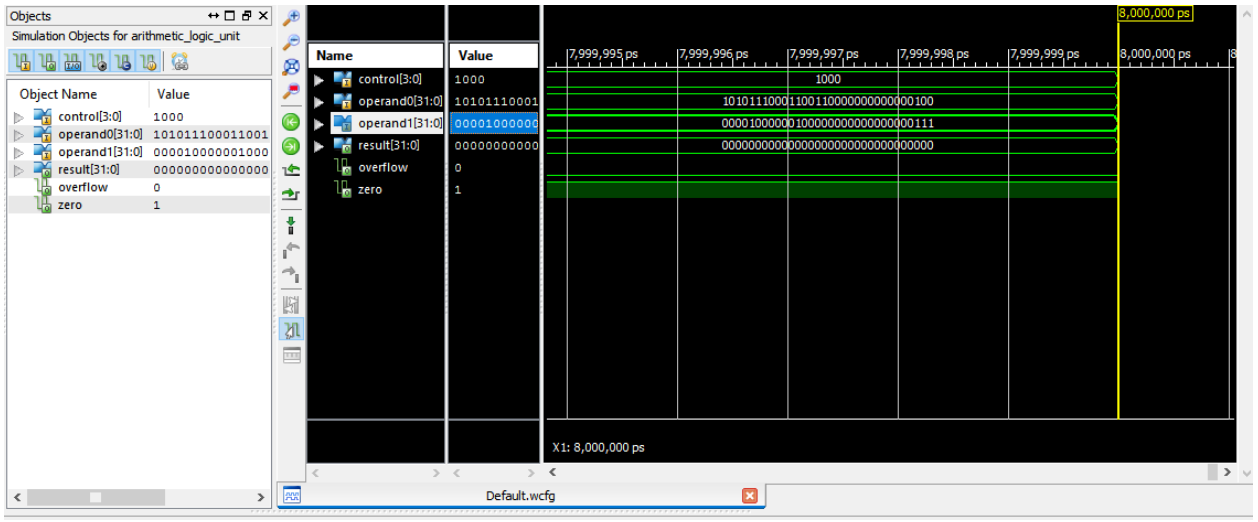
FOR SUBTRACT:



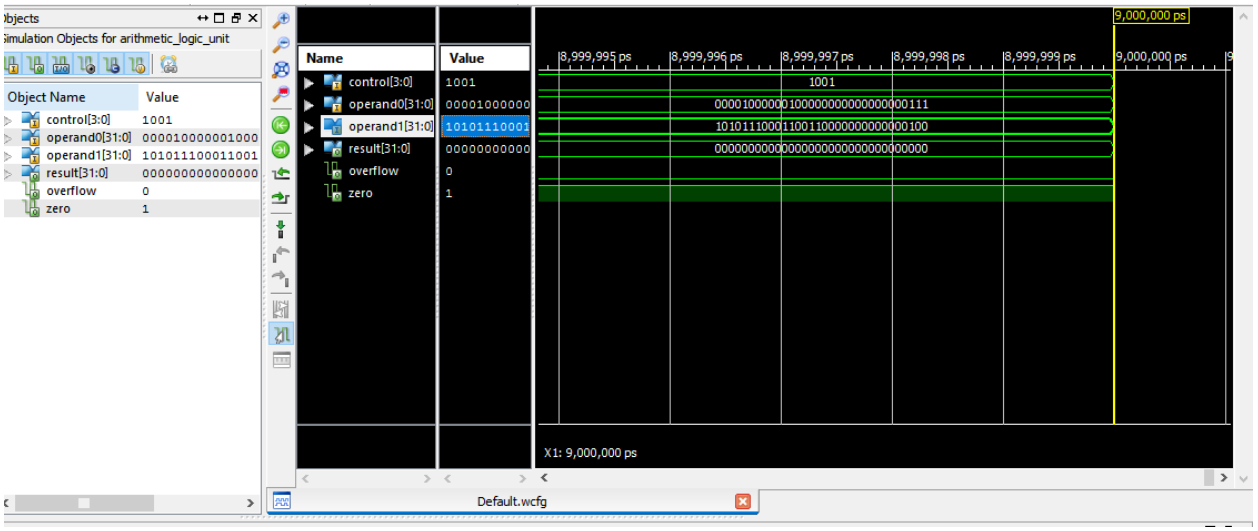
FOR SET ON LESS THAN:



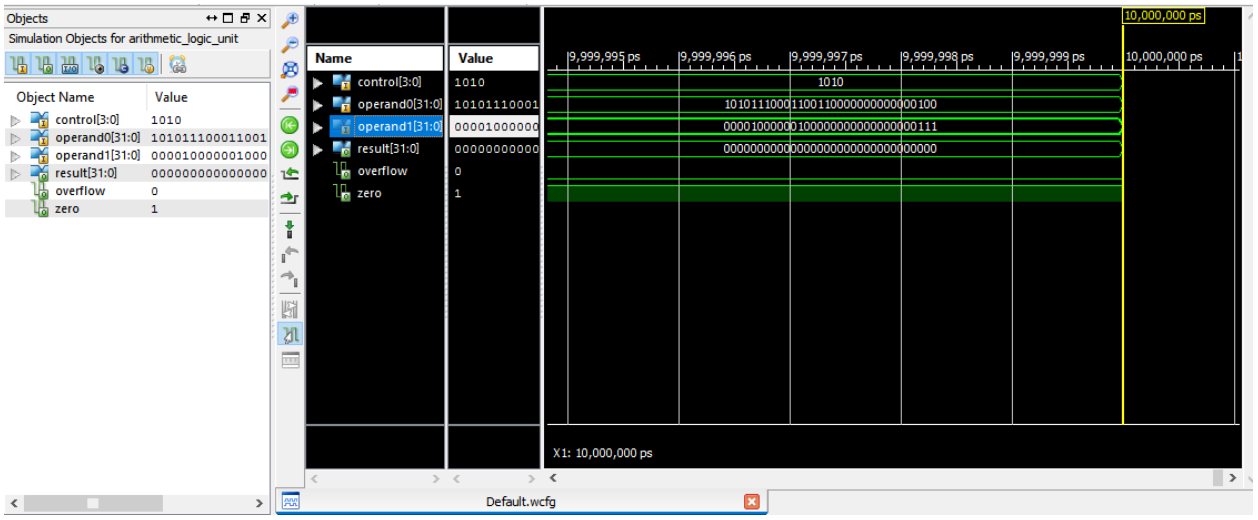
FOR SHIFT LEFT:



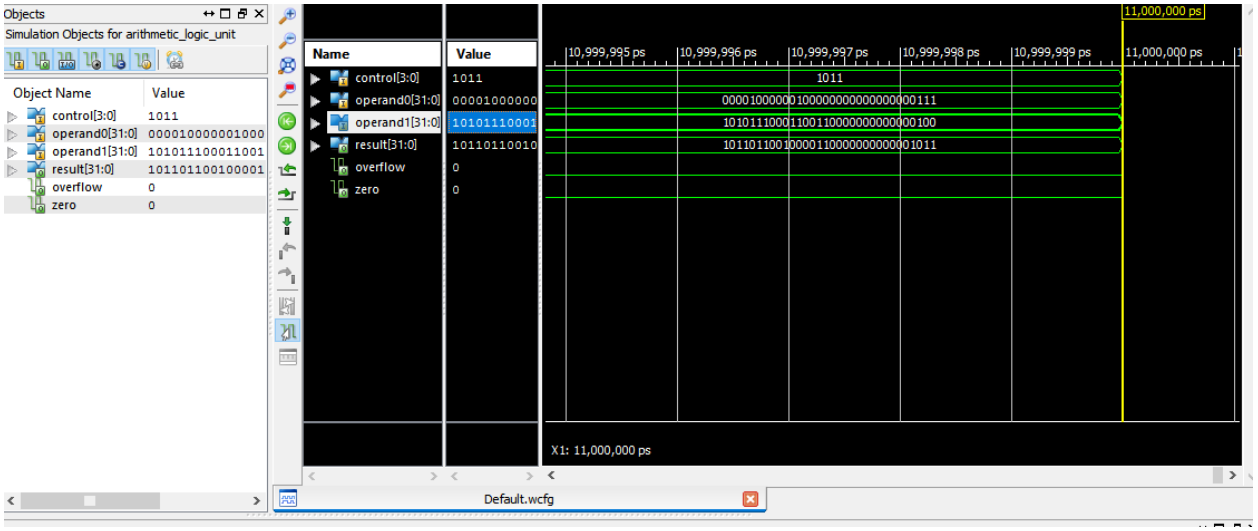
FOR SHIFT RIGHT:



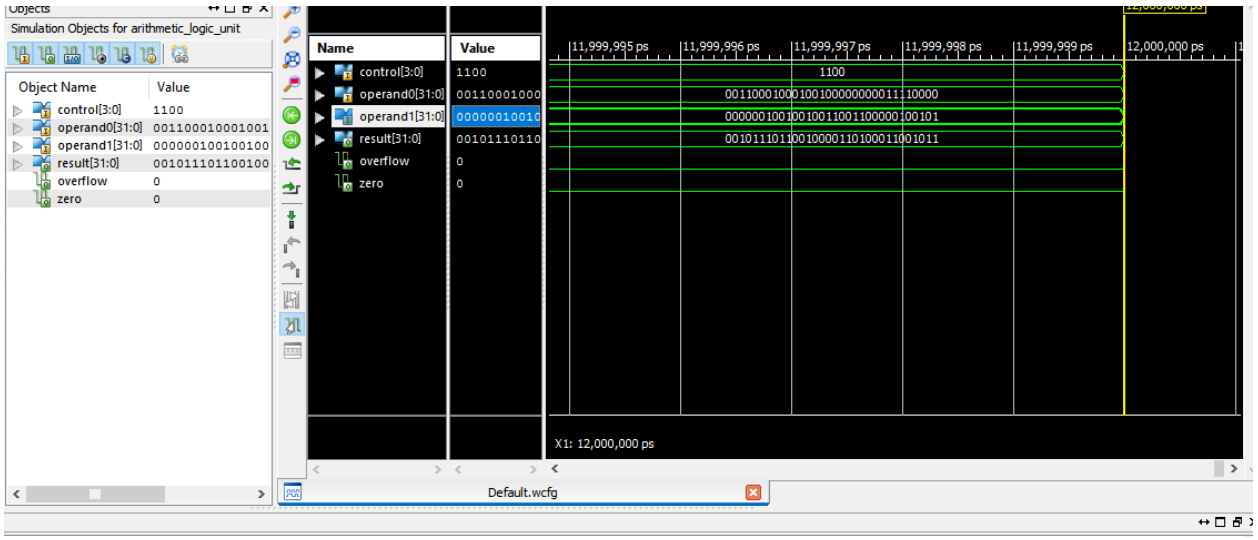
FOR SHIFT RIGHT ARITHMETIC:



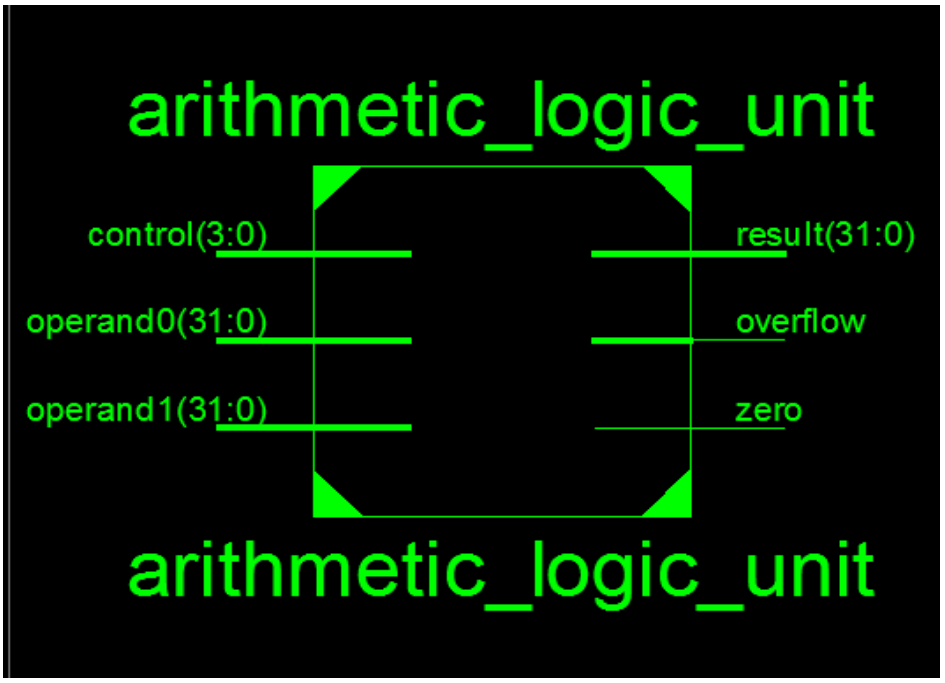
FOR SIGNED ADD:



FOR SIGNED SUBTRACT

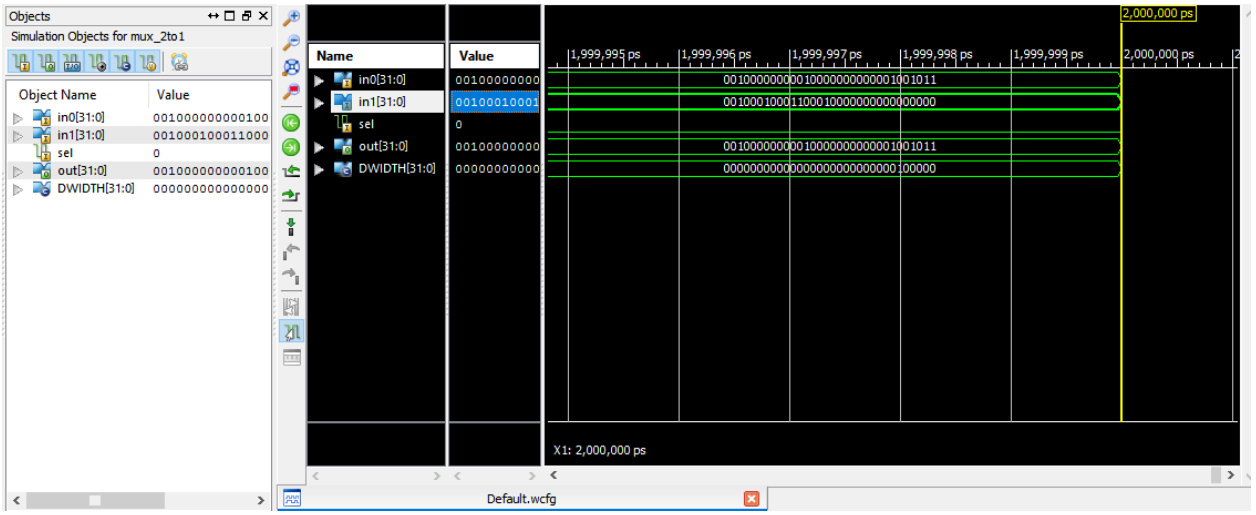


SCHEMATIC DIAGRAM:

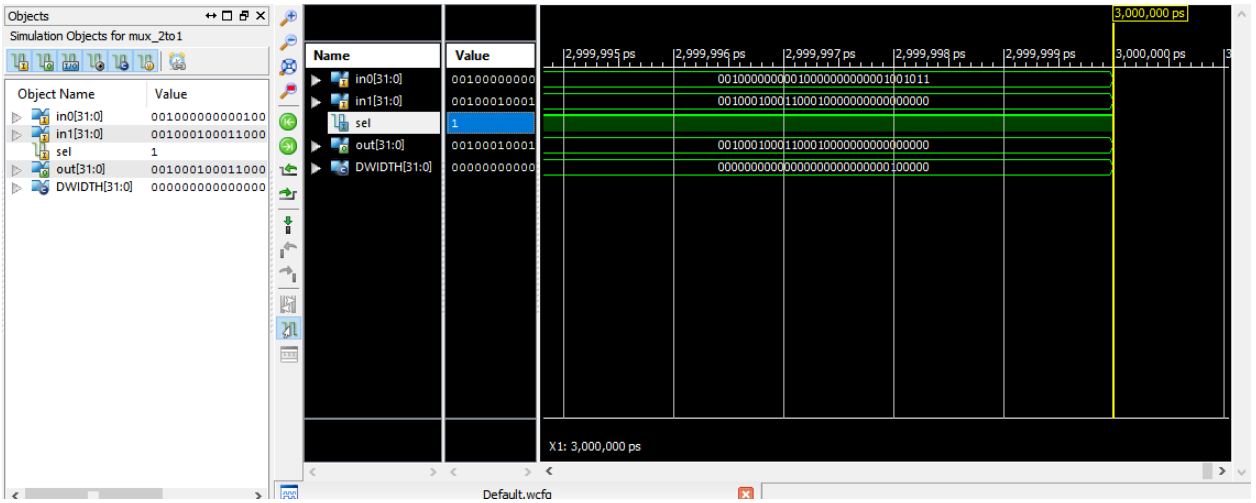


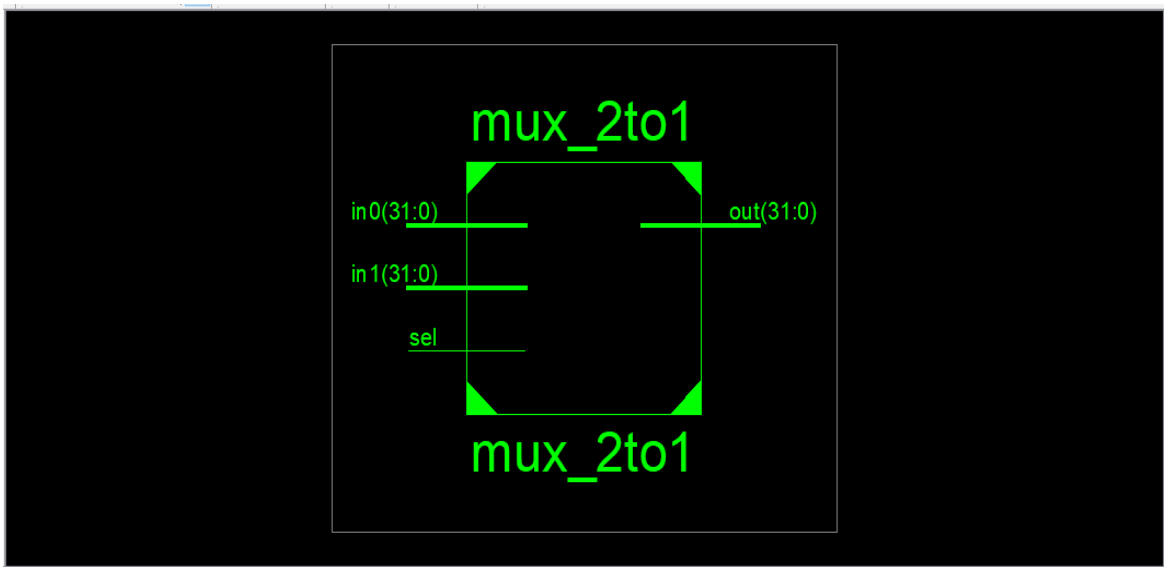
MUX:

FOR SET BIT 0:

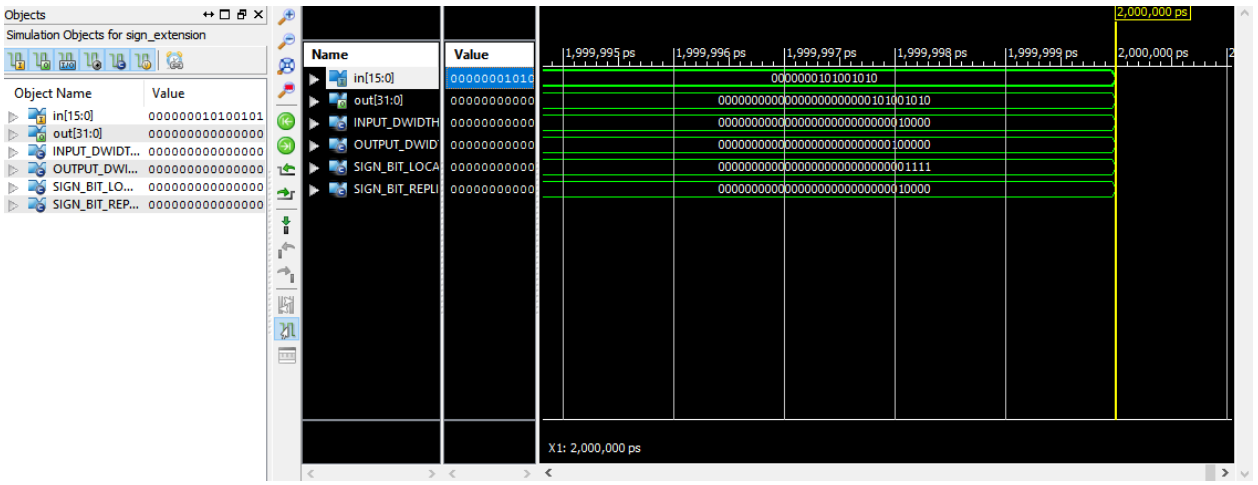


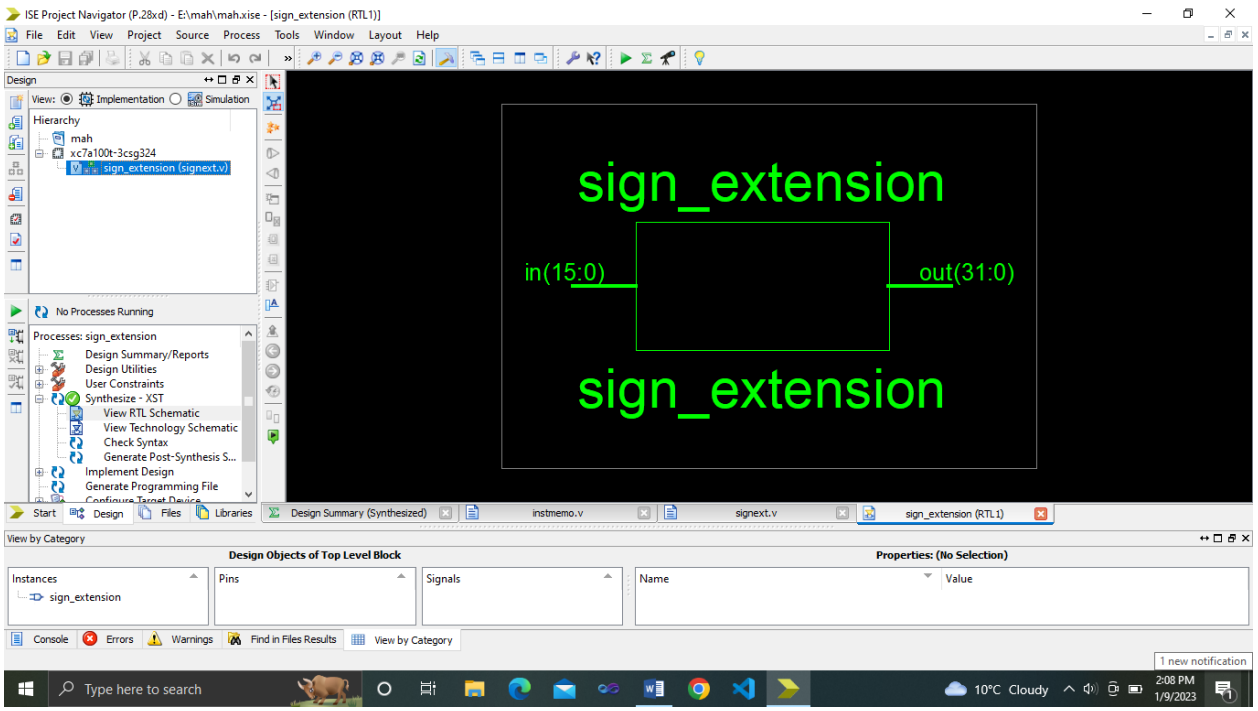
FOR SET BIT 1:



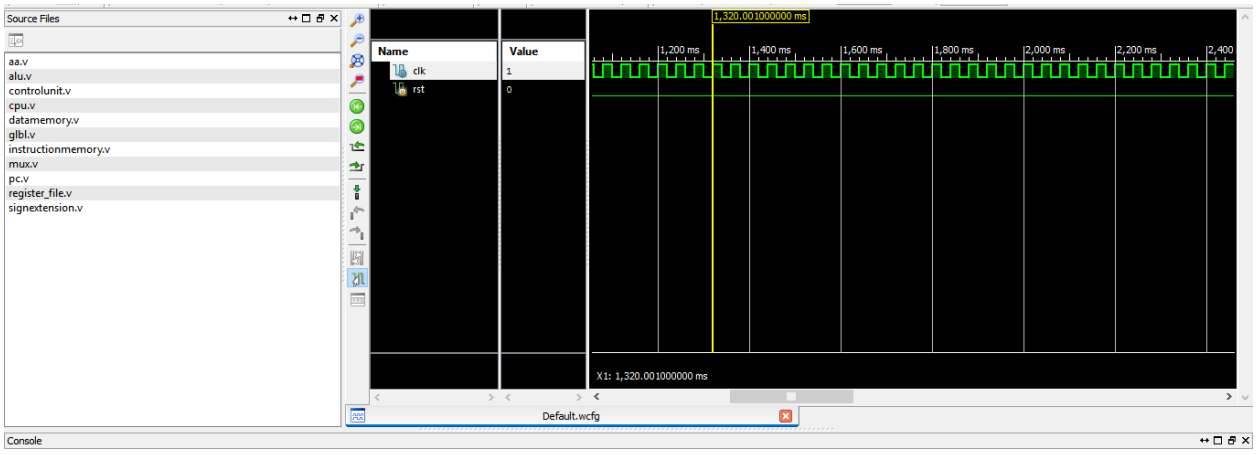


SIGN EXTENSION:

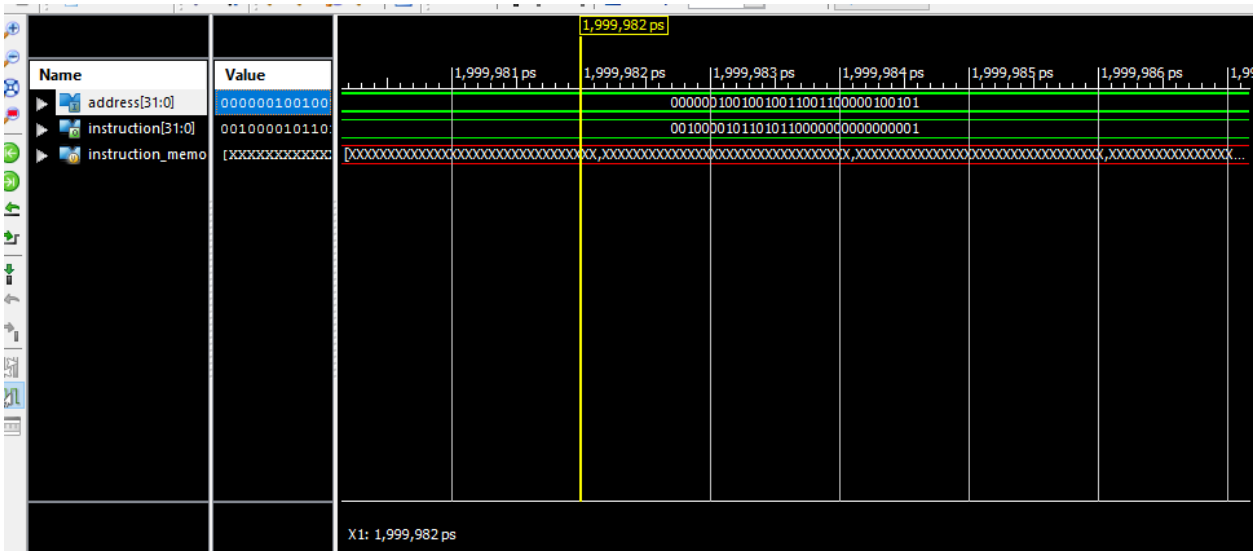

Objects
Simulation Objects for sign_extension
Object Name
Value
in[15:0]
out[31:0]
INPUT_DWIDT...
OUTPUT_DWI...
SIGN_BIT_LO...
SIGN_BIT_REP...
Name
Value
in[15:0]
out[31:0]
INPUT_DWIDTH
OUTPUT_DWID
SIGN_BIT_LOCA
SIGN_BIT_REPLI
1,999,995 ps
1,999,996 ps
1,999,997 ps
1,999,998 ps
1,999,999 ps
2,000,000 ps
X1: 2,000,000 ps

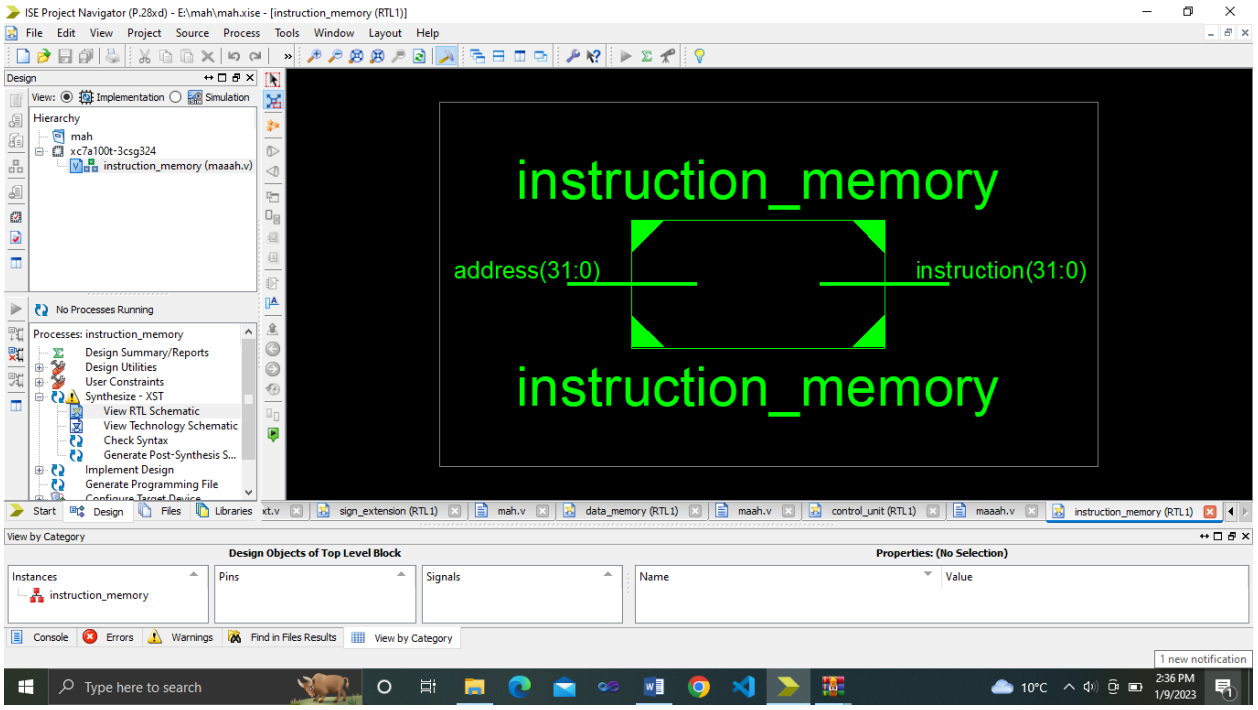

ISE Project Navigator (P.28xd) - E:\mah\mah.xise - [sign_extension (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
mah
xc7a100t-3csg324
sign_extension (signext.v)
No Processes Running
Processes: sign_extension
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis S...
Implement Design
Generate Programming File
sign_extension
in(15:0)
out(31:0)
sign_extension
Start Design Files Libraries
Design Summary (Synthesized) instmemo.v signext.v sign_extension (RTL1)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
sign_extension
Pins
Signals
Name
Value
Console Errors Warnings Find in Files Results View by Category
Type here to search
10°C Cloudy
2:08 PM
1/9/2023
1 new notification

TBCPU:


Source Files
aa.v
alu.v
controlunit.v
cpu.v
datamemory.v
glbl.v
instructionmemory.v
mux.v
pc.v
register_file.v
signextension.v
Name
Value
clk
rst
1,320.001000000 ms
1,200 ms
1,400 ms
1,600 ms
1,800 ms
2,000 ms
2,200 ms
X1: 1,320.001000000 ms
Default.wcfg
Console

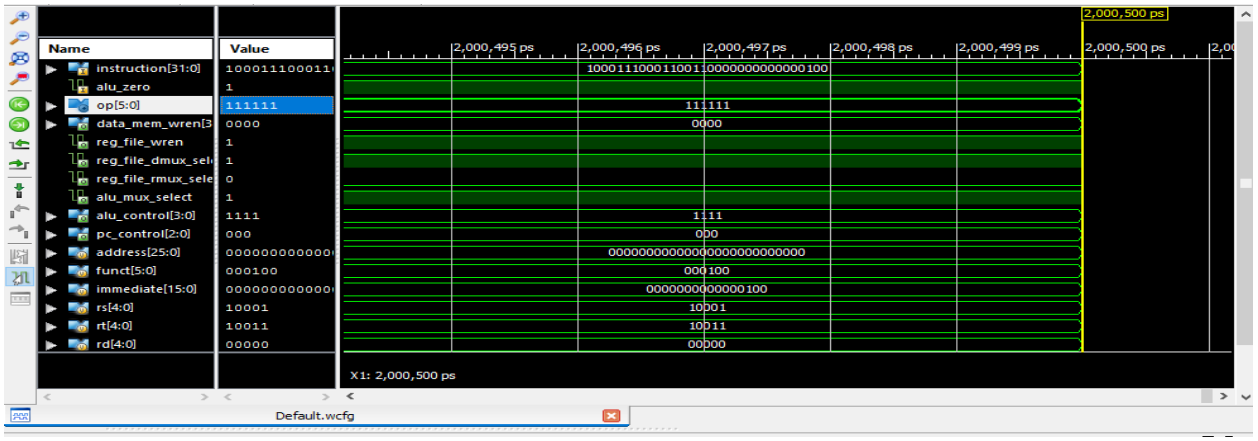
INSTRUCTION MEMORY:



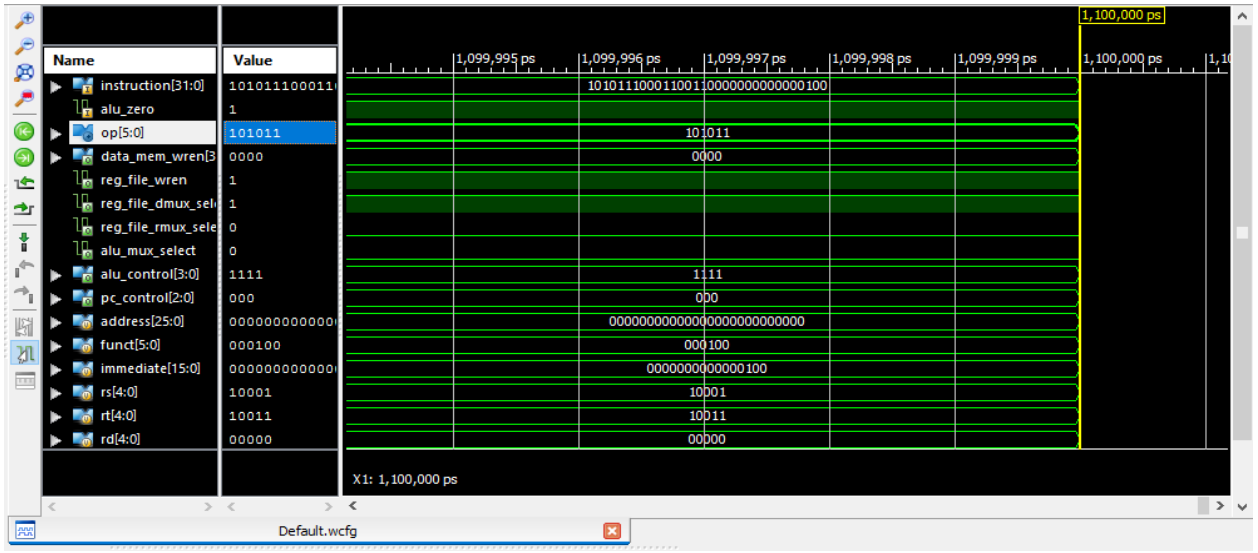


CONTROL UNIT:

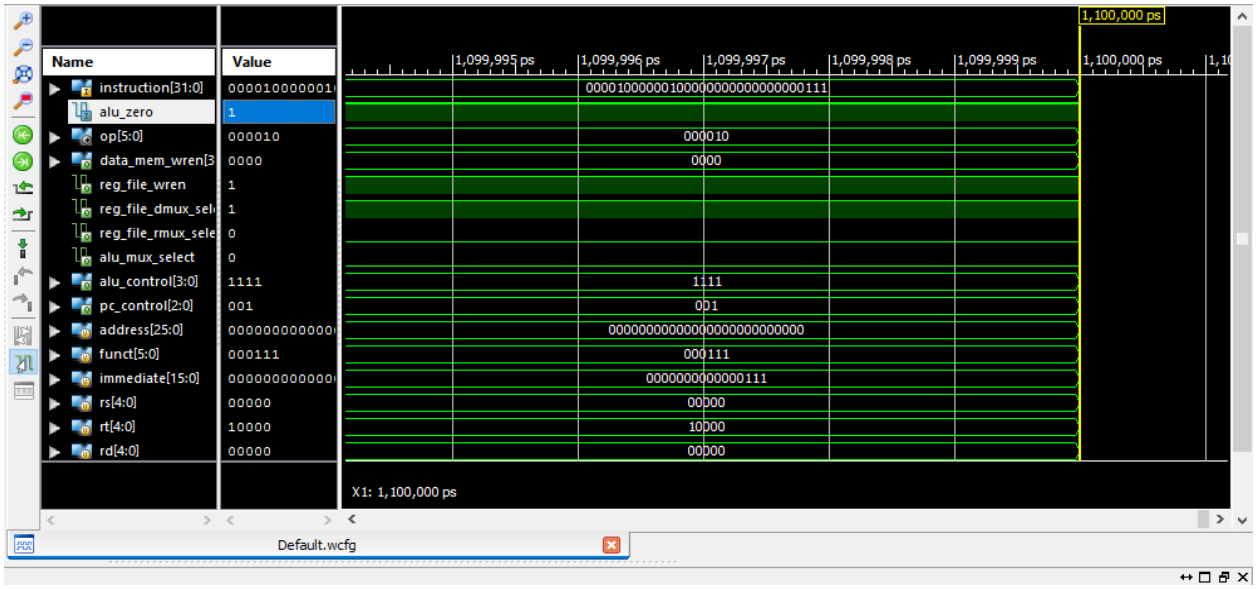
LOAD:

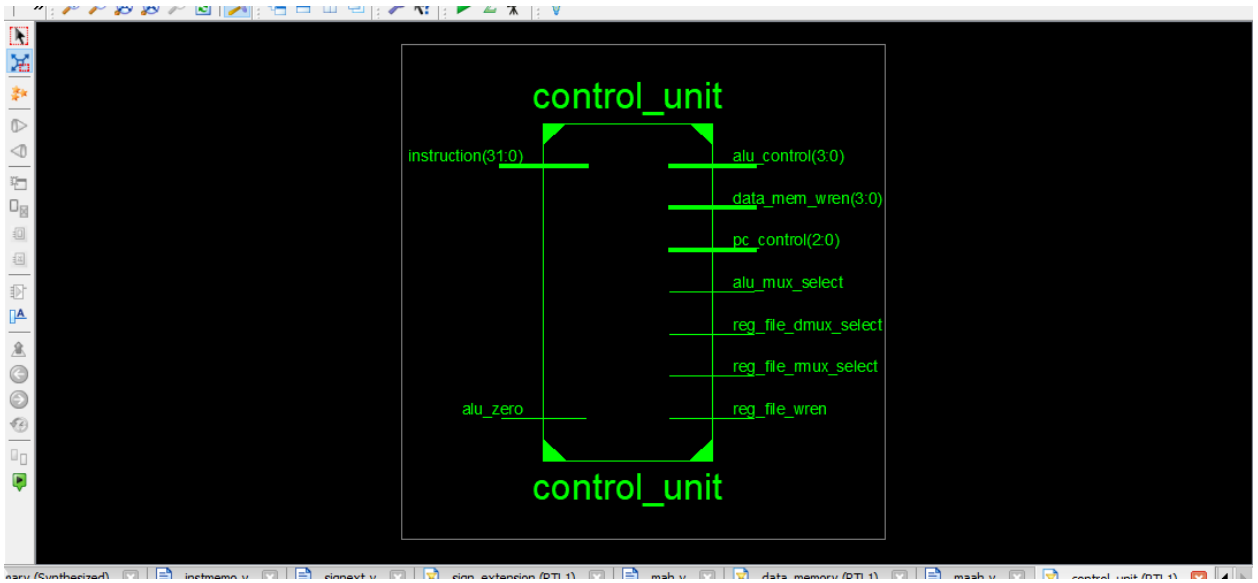

Name
Value
instruction[31:0]
alu_zero
op[5:0]
data_mem_wren[3
reg_file_wren
reg_file_dmux_sel
reg_file_rmux_sele
alu_mux_select
alu_control[3:0]
pc_control[2:0]
address[25:0]
funct[5:0]
immediate[15:0]
rs[4:0]
rt[4:0]
rd[4:0]
100011100011
1
111111
0000
1
1
0
1
1111
000
000100
10001
10011
00000
2,000,495 ps
2,000,496 ps
2,000,497 ps
2,000,498 ps
2,000,499 ps
2,000,500 ps
X1: 2,000,500 ps
Default.wcfg

STORE:

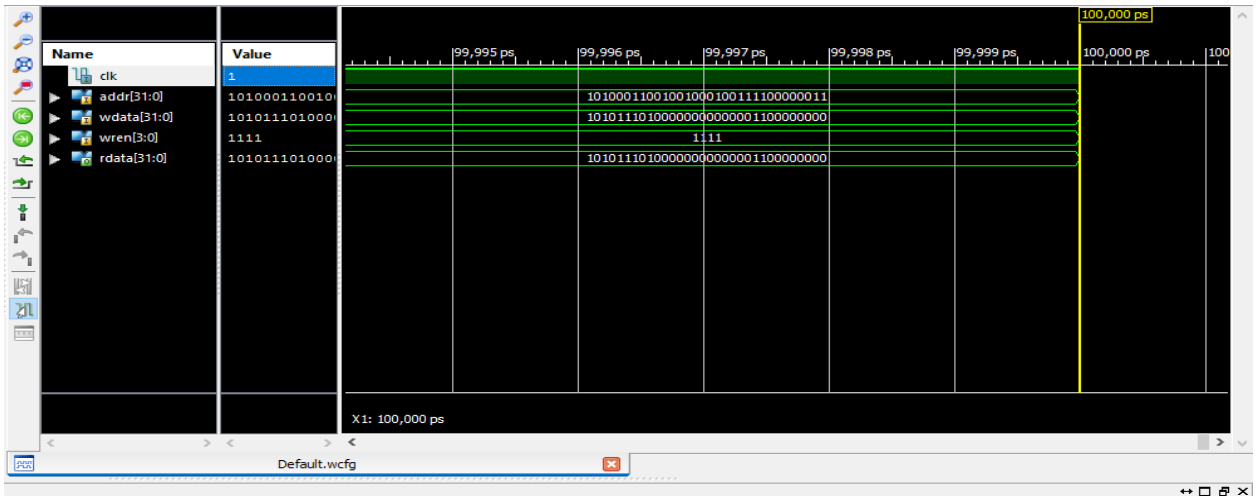

Name
Value
instruction[31:0]
alu_zero
op[5:0]
data_mem_wren[3
reg_file_wren
reg_file_dmux_sel
reg_file_rmux_sele
alu_mux_select
alu_control[3:0]
pc_control[2:0]
address[25:0]
funct[5:0]
immediate[15:0]
rs[4:0]
rt[4:0]
rd[4:0]
101011
1
101011
0000
1
1
0
0
1111
000
000100
10001
10011
00000
1,099,995 ps
1,099,996 ps
1,099,997 ps
1,099,998 ps
1,099,999 ps
1,100,000 ps
X1: 1,100,000 ps
Default.wcfg

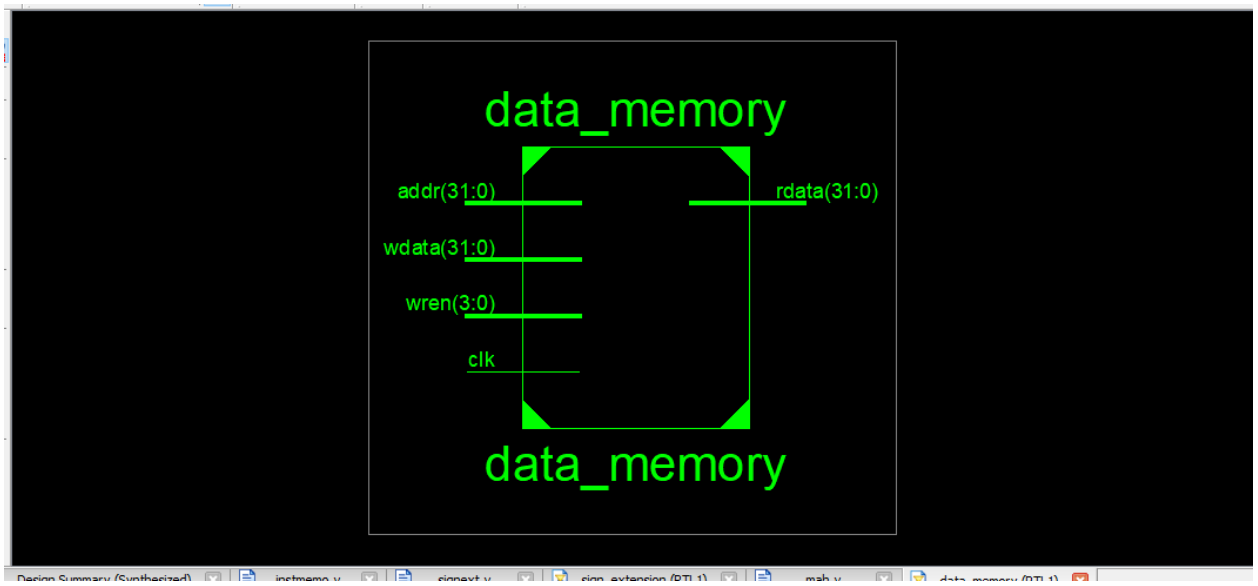
JUMP:


Name
Value
instruction[31:0]
alu_zero
op[5:0]
data_mem_wren[3
reg_file_wren
reg_file_dmux_sel
reg_file_rmux_sele
alu_mux_select
alu_control[3:0]
pc_control[2:0]
address[25:0]
funct[5:0]
immediate[15:0]
rs[4:0]
rt[4:0]
rd[4:0]
000010
1
000010
0000
1
1
0
0
1111
001
000111
00000
10000
00000
1,099,995 ps
1,099,996 ps
1,099,997 ps
1,099,998 ps
1,099,999 ps
1,100,000 ps
X1: 1,100,000 ps
Default.wcfg

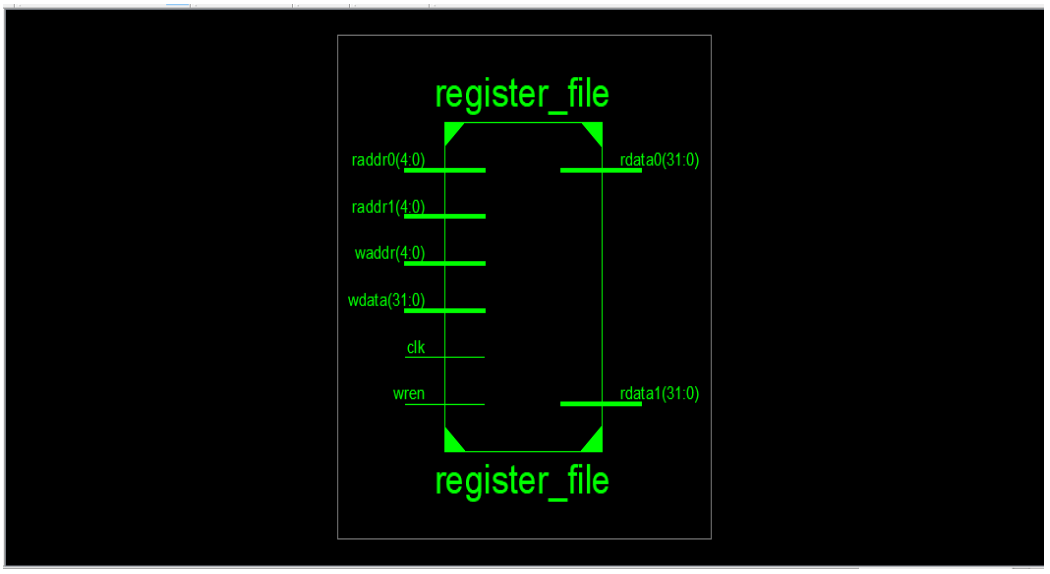


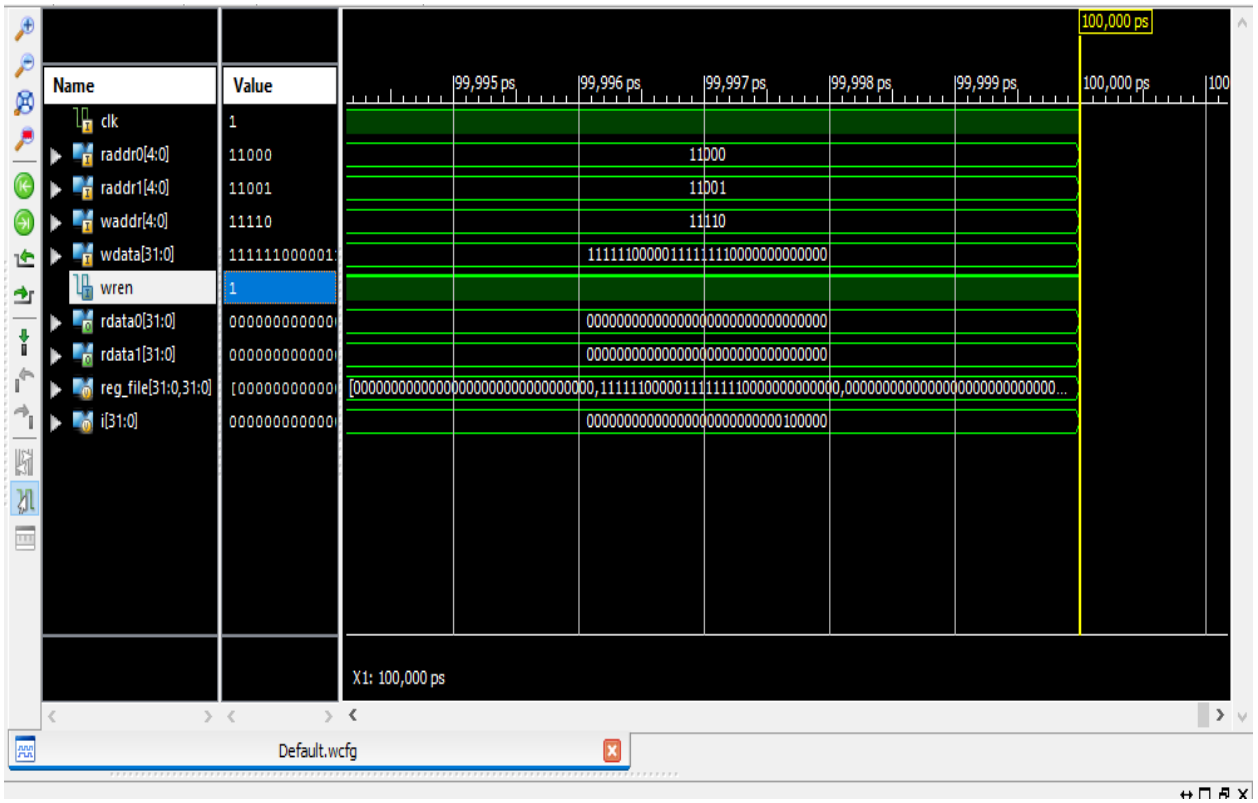
DATA MEMORY:



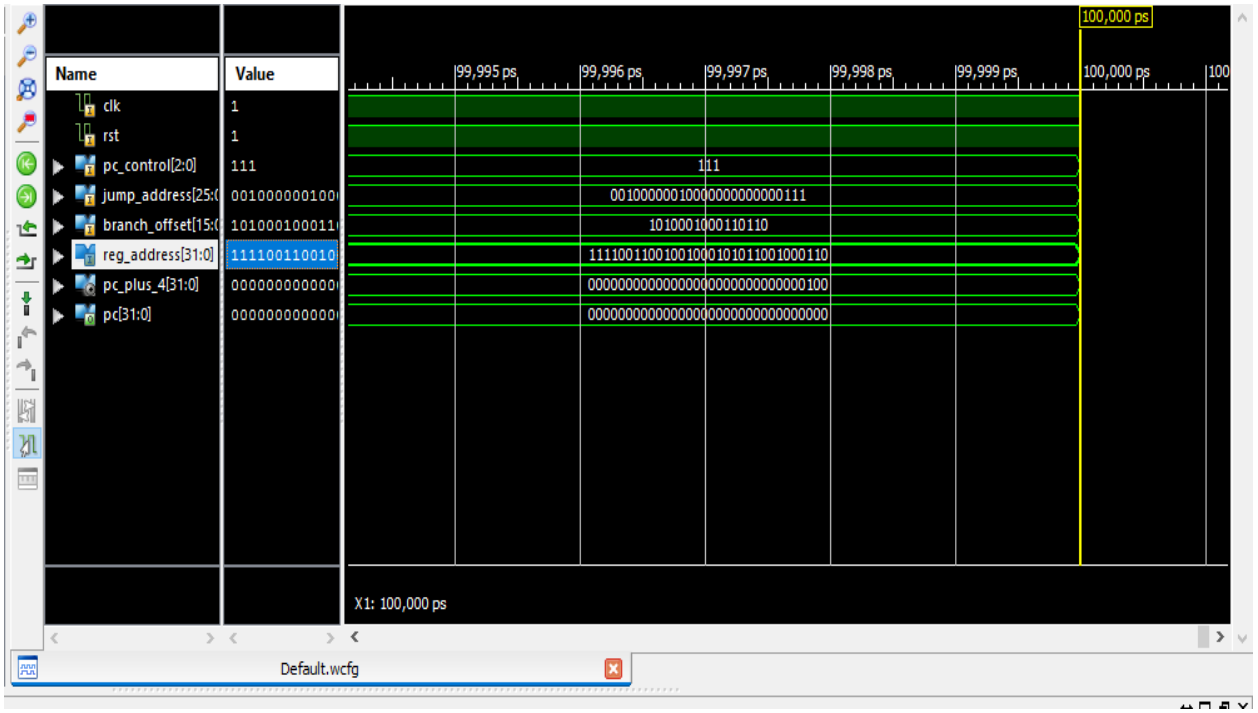


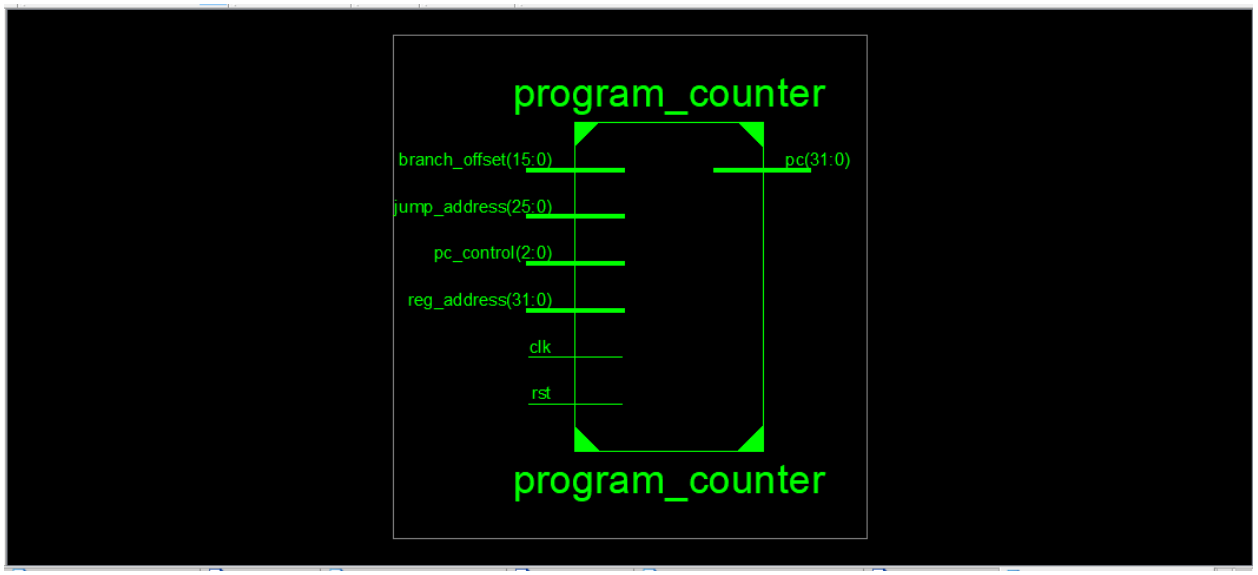
REGISTER FILE:



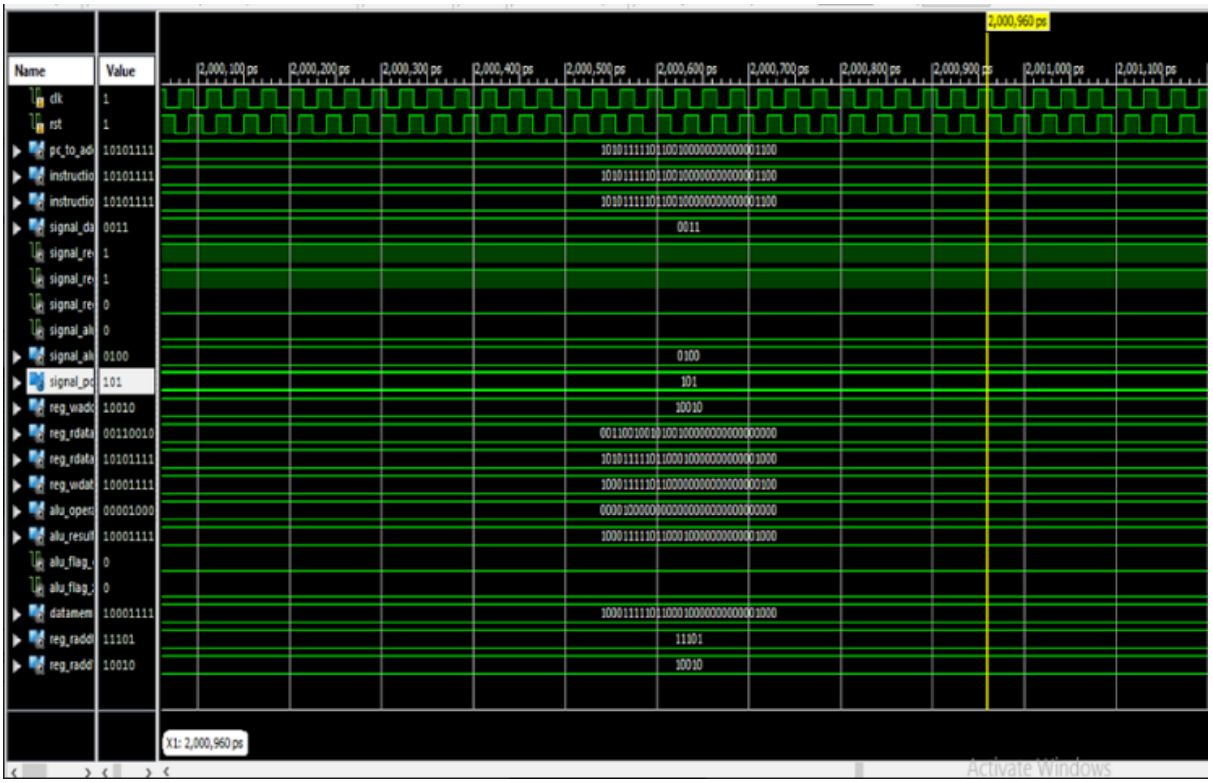


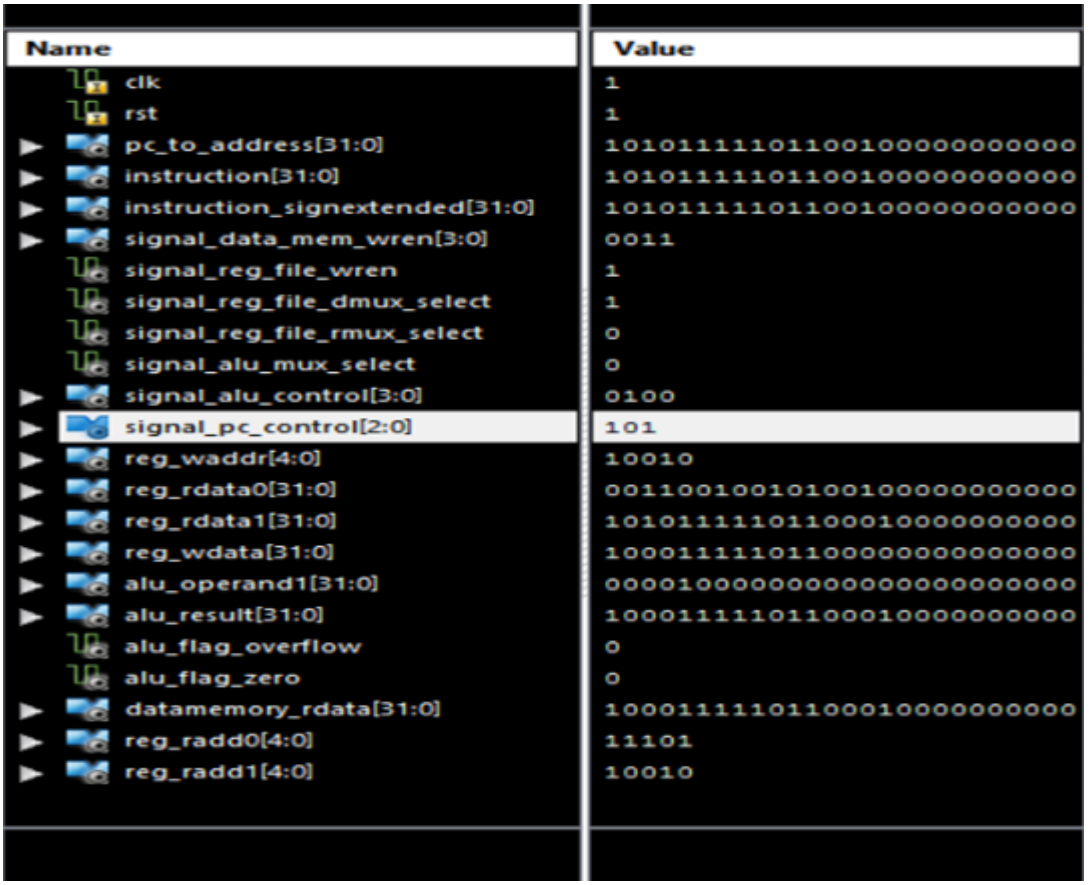
PROGRAM COUNTER:


Name
Value
clk
1
rst
1
pc_control[2:0]
111
jump_address[25:0]
branch_offset[15:0]
reg_address[31:0]
pc_plus_4[31:0]
pc[31:0]
99,995 ps
99,996 ps
99,997 ps
99,998 ps
99,999 ps
100,000 ps
X1: 100,000 ps
Default.wcfg


program_counter
branch_offset(15:0)
jump_address(25:0)
pc_control(2:0)
reg_address(31:0)
clk
rst
pc(31:0)
program_counter

CPU:


Name
Value
clk
rst
signal_data_mem_wren[3:0]
signal_reg_file_wren
signal_reg_file_dmux_select
signal_reg_file_rmux_select
signal_alu_mux_select
signal_alu_control[3:0]
signal_pc_control[2:0]
reg_waddr[4:0]
reg_rdata0[31:0]
reg_rdata1[31:0]
reg_wdata[31:0]
alu_operand1[31:0]
alu_result[31:0]
alu_flag_overflow
alu_flag_zero
datamemory_rdata[31:0]
reg_radd0[4:0]
reg_radd1[4:0]
0011
0100
101
10010
11101
10010
X1: 2,000,960 ps


Name
Value
clk
rst
pc_to_address[31:0]
instruction[31:0]
instruction_signextended[31:0]
signal_data_mem_wren[3:0]
signal_reg_file_wren
signal_reg_file_dmux_select
signal_reg_file_rmux_select
signal_alu_mux_select
signal_alu_control[3:0]
signal_pc_control[2:0]
reg_waddr[4:0]
reg_rdata0[31:0]
reg_rdata1[31:0]
reg_wdata[31:0]
alu_operand1[31:0]
alu_result[31:0]
alu_flag_overflow
alu_flag_zero
datamemory_rdata[31:0]
reg_radd0[4:0]
reg_radd1[4:0]
1
1
0
0
0100
101
10010
11101
10010