General Specification for Electrical/Electronic Components and Subsystems, Electromagnetic Compatibility (EMC)

Global EMC Component / Subsystem Validation Acceptance Process

1 Introduction

In the event of a conflict between the text of this specification and the documents cited herein, the text of this specification takes precedence.

Note: Nothing in the specification, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1.1 Scope.

This document applies to the Electro-magnetic Compatibility (EMC) design, development and validation of electrical/electronic components and subsystems for passenger vehicles, light duty trucks and medium duty trucks.

This document is one out of a series of three global EMC documents that specify EMC test and validation requirements. The complete series consists of the following documents:

GMW3091, GMW3097 and GMW3103 (All three documents of equal revision carry the same release date).

Note: Earlier versions of GMW12003, GMW12004, and GMW3106, have been integrated into GMW3103 for ease of use.

1.2 Mission / Theme.

This document specifies the Global Electromagnetic Compatibility Component/Subsystem Validation Acceptance Process to ensure components and subsystems are properly designed, developed and validated prior to vehicle validation.

2 Reference

Note: Only the latest approved standards are applicable unless otherwise specified.

2.1 External Standards/Specifications.

ISO/IEC 17025, SAE J1850, ISO 9000, QS9000, EN 45001

2.2 GM Standards/Specifications.

GMW3091, GMW3097, GMW3089, GMW3122

2.3 Additional References.

Production Part Approval Process (PPAP), Copyright © 1993, © 1995, Chrysler Corporation, Ford Motor Corporation, General Motors Corporation, ISO Guide 25 and Automotive EMC Lab Recognition Program

3 Requirements

3.1 Requirements.

The Global EMC Component/Subsystem Validation Acceptance Process defined within this document shall be followed for all EMC component/subsystem design, development and validation.

The Appendix B: EMC Lessons Learned should be reviewed and considered prior to the first electrical design and layout of the product. The Appendix A: Component EMC Test Plan shall be completed by the supplier and submitted in an electronic format to vehicle manufacturer for approval 60 days prior to the start of EMC testing.

An editable version of all Appendices can be obtained on request from the applicable vehicle manufacturer EMC department.

3.2 Process

Design, Build and Validate Design Iteration

The objectives of the *Design, Build and Validate Design Iteration* phase shown in Figure 1, include component/subsystem design, development and validation. Design validation shall occur during this phase to confirm all Electromagnetic Compatibility technical requirements contained in the Component/Subsystem Technical Specification are met.

An EMC *Detailed Design Review*, shown in Figure 1, should be conducted for all new components and subsystems and applications, and for revisions to existing components and subsystems that could affect Electromagnetic Compatibility compliance. This process does not apply to carryover components or subsystems. The term *carryover* means that the product qualified for a prior program and is exactly the same product being used for the future program. Modifications, alterations, internal part swaps, hardware and software changes are not considered carryover and must be validated according to the requirements.

Detailed Design Review(s) shall be scheduled and led by the supplier, and attended by the EMC Design Review Team if the supplier desires EMC design guidance.

The vehicle manufacturer Responsible Engineer must be consulted on scheduling and informed of all design review results and supplier action plans. The vehicle manufacturer Responsible Engineer's acceptance of review results and supplier action plans does not relieve the supplier of the obligation to meet contracted performance requirements.

The objectives of the *Detailed Design Review* should be:

- to review component / subsystem schematic design and circuit board layout
- to examine any prior relevant analysis, calculations and test results
- to evaluate potential changes to the component / subsystem design
- to propose solutions to problems and appropriate revalidation
- to verify that the proposed design and circuit board layout satisfies component / subsystem EMC technical and validation requirements

The vehicle manufacturer Responsible Engineer may also schedule a design review on his/her own initiative, or upon the advice of a vehicle manufacturer EMC engineer. The vehicle manufacturer Responsible Engineer may make any appropriate arrangement for leadership of such a review or delegate the actual review activity to other team members.

Supplier Deliverables: Documentation required to be delivered, as one package, to vehicle manufacturer EMC design review team at least 10 working days ahead of the scheduled meeting:

- PCB Layout
- Components list
- Hardware Schematic drawing
- Component placement drawing
- Functional description
- Interface description
- EMC math simulation results (if available)
- EMC test reports (if available)
- EMC Component Test Plan (Appendix A of GMW3103), in electronic editable format

Note: Actual hardware samples or physical mock-up for visual examination is desirable but not required. Electronic documents must be in an editable format compatible with Microsoft Office.

Design analysis & performance. Design analysis & performance is a part of the design review. In a design review the supplier shall demonstrate and give technical rationale for the following:

- EMC filter design & performance, characterization data for proposed I/O filtering, clock circuits, bypassing and decoupling.
- Number of PCB layers in combination with use of selected clock frequency and housing material.
- Identification and protection of critical/susceptible parts to both emission and immunity (incl. Transient and ESD protection).
- Identification of fundamental operating frequencies: clock rates switching frequencies and other potential coherent EMC sources.

Initial EMC test results shall be studied and reviewed, if not available, identify when review of test results can be done. Some of the data may include:

- Output waveforms for all pulsed, PWM or power outputs indicating the dV/dt, and dI/dt.
- Provide output voltage and current time domain measurements for power outputs and inputs.
- Review results of performed radiated emissions and immunity testing.
- Provide data from other modules which may have used similar components

Resources needed for a successful EMC design review (other specialists, engineers, purchasing or managers depending on situation and complexity.)

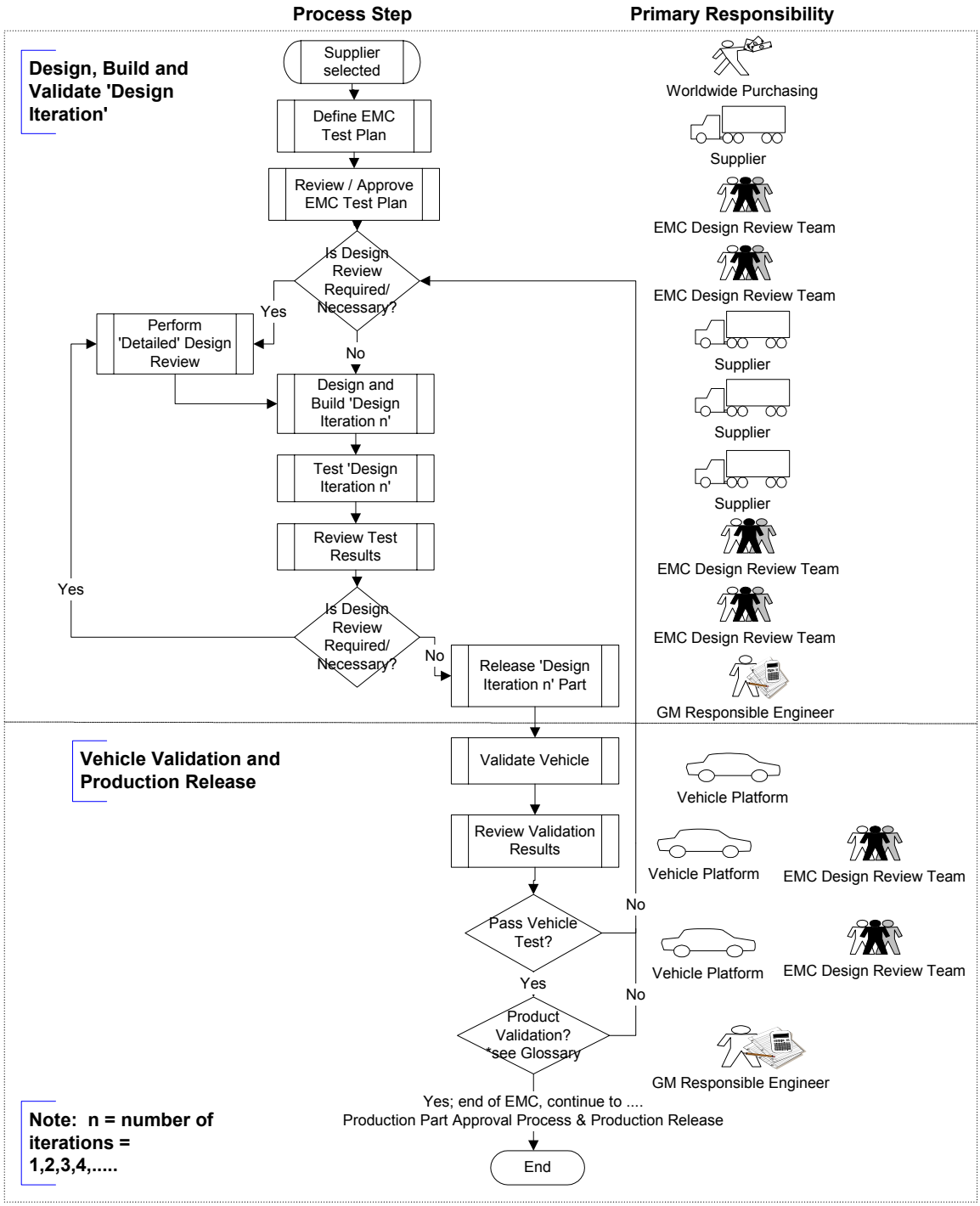
- Vehicle manufacturer:
  - EMC Specialist and/or EMC Release Engineer
  - Design Release Engineer and/or component/system responsible Engineer. (optional)
  - Validation Engineer (optional)
- Supplier:
  - Hardware/design responsible Engineer
  - EMC Engineer/Specialist
  - Project/system responsible Engineer (optional)
  - Validation Engineer (optional)

Vehicle Validation and Component/Subsystem Production Release.

The objectives of the *Vehicle Validation and Component/Subsystem Production Release* phase shown in Figure 1 include product validation and component/subsystem production release. Component/Subsystem validation re-confirmation of all Electromagnetic Compatibility technical requirements contained in the Component/Subsystem Technical Specification shall occur during vehicle level validation.

The component/subsystem shall pass both the component/subsystem level electromagnetic compatibility test(s) and the vehicle level electromagnetic compatibility test(s). In the event that the component/subsystem passes the component/subsystem level electromagnetic compatibility test(s) but does not pass the vehicle level electromagnetic compatibility test(s), the vehicle level test results shall be the determining factor for validation test pass/fail status.

Figure 1: Design, Build and Validate Design Iteration/Vehicle Validation and Component/Subsystem Production Release



4 Notes

4.1 Glossary.

Carryover: The product qualified for a prior program and is exactly the same product being used for the future program. Modifications, alterations, internal part swaps, hardware and software changes are not considered carryover and must be validated according to the requirements.

Design Validation: The process of confirming through analysis, demonstrations, inspections, and/or tests that the product design meets its technical requirements (SSTS, CTS/component drawing) without including the effects of manufacturing induced variations. Variation will exist in the parts on test, but not representative of the variation from the production process. Design Validation must be complete according to the Program Schedule of Engineering Deliverables section of the SOR.

EMC Design Review Team: The EMC Design Review Team should include as a minimum, the vehicle manufacturer Responsible Engineer with release authority over the product, one or more vehicle manufacturer EMC Engineers, the supplier's EMC expert and members of the supplier's project team directly involved with the design, development and validation of the product.

Vehicle Manufacturer Responsible Engineer: Individual with release authority over the product.

Product Validation: The process of confirming through analysis, demonstrations, inspections and/or tests that the product design meets its technical requirements (VTS, SSTS, CTS/component drawing) when including the effects of manufacturing variation. To complete this validation in time to affect pilot, this variation should be simulated in pre-production hardware or analyses, or by exception, with product hardware produced from production tools/equipment.

Shall: Denotes a binding provision; a must

Should: Denotes preferences when specifying alternatives or desired conformance with objectives, standards, etc.

4.2 Acronyms, Abbreviations and Symbol

A/D	Analog to Digital
AC	Alternating Current
BCI	Bulk Current Injection
CAN	Controller Area Network
CE	Conducted Transient Emissions
CI	Conducted Transient Immunity
CTS	Component Technical Specification
DBCI	Differential Bulk Current Injection
DC	Direct Current
DUT	Device Under Test
DV	Design Validation
DWCAN	Dual Wire CAN
EICD	Electrical Interface Control Document
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ESR	Effective Series Resistance
FET	Field-Effect Transistor
FOT	Fiber Optic Transmitter
GM	General Motors
HS	High Speed
I/O	Input / Output
IC	Integrated Circuit
IEC	InternationalElectrotechnical Commission
ISO	International Organization for Standardization
ITDC	International Technical Development Center
LISN	Line Impedance Stabilization Network
LC	Inductive / Capacitive
LED	Light-Emitting Diode
LF	Low Frequency
LS	Low Speed
MOST	A Specific Communication Protocol
MOV	Metal Oxide Varistor
NA	North America

OTP	One Time Programmable	SAE J1850	Communication Protocol (Class 2)
PCB	Printed Circuit Board	SMD	Surface Mounted Device
PLL	Phase Locked Loop	SOR	Statement of Requirements
PV	Production Validation	SSLT	Subsystem Leadership Team
PWM	Pulse Width Modulated	SSTS	Subsystem Technical Specification
R/C	Resistance/Capacitance	SWCAN	Single Wire CAN
RAM	Random Access Memory	uP	Microprocessor
RE	Radiated Emissions	VTS	Vehicle Technical Specification
RF	Radio Frequency	XTAL	CrystalCoding System
RI	Radiated Immunity		

5 Coding System

This specification shall be referenced in other documents, drawings, VTS, CTS, etc. as follows:

GMW3103

Where

GMW Validation Area (GM Worldwide)

3103 Sequential number

Class: General Specification

Type: All Vehicle

Category: Electrical Architecture

Example: “Requirements to GMW3103”

6 Release and Revisions

6.1 Release.

The specification was first approved in January 2000 and distributed in Sept. 2000

It has been prepared by the GM Global EMC Committee.

6.2 Revisions.

Rev.	Approval Date	Description (Org.)
A	Jun 00	New, was also called “revision 1” (ITDC)
B	Oct 00	Reworked, was also called “revision 2” (ITDC)
C	Aug 01	Reworked, is also called “revision 3”. Changes against revision October 2000 (revision 2): List of tests matched to GMW3091, GMW3094, GMW3097 and GMW 3100. More detailed appendices for design review and test plan. Editorial changes. (ITDC)
D	Oct 03	Publication Dec 2003. Reworked, is also called “revision 4”. Changes against revision August 2001 (revision 3): Consolidated appropriate material from GMW3106 (eliminated) into this document, removed Suppliers Questionnaire, moved Appendix “A” into body requirements section, renumbered remaining appendices, modified motor filtering in Lessons Learned appendix, more detailed appendices for design review and test plan. Editorial changes. (GMNA and ITDC)
E	Feb 04	Publication Feb 2004. Editorial revision, also called “revision 4”, typographical errors corrected

Appendix A Global EMC Component Test Plan

A.1 Introduction

The Component EMC Test Plan shall be completed by the supplier and submitted to the vehicle manufacturers EMC Design Review Team member(s)for approval at least 60 days prior to the start of Component EMC testing. All sections shall be included as stated in the outline, only additions of new sections are allowed. If a section is not applicable, this shall be stated in the document after the relevant section description.

Completing the Component EMC Test Plan requires collaborations between the supplier's Design Engineer along with the supplier's EMC Applications and Test Engineers.

A.2 Purpose

The purpose of the Component EMC Test Plan is to develop and document a comprehensive EMC test based on requirements to confirm EMC compliance. The Component EMC Test Plan also provides a mechanism for ongoing enhancements and improvements to the test methodology that improves vehicle level test correlation.

The Component EMC Test Plan section documents the DUT operation and test procedures. It describes all relevant test set-ups and procedures to verify the electromagnetic robustness of the design. In some cases, it may make sense to select a specific sample for test that represents the entire DUT family. The Component EMC Test Plan should contain the justification and rationale for doing this.

In some cases simulation results may be used as a substitute for actual physical testing. This requires specific prior agreement by the vehicle manufacturer's EMC engineer, and shall be documented in Table A.2: Test Requirements Table.

A.3 Component EMC Test Plan.

Table A.1: Component EMC Test Plan.

Device Under Test (no abbreviations):		**Release Date:**	**Revision:**
DUT Part Number(s):	**DUT Manufacturer:**		
Prepared by (Supplier):	**Approved by vehicle manufacturers Responsible Engineer:**		
Approved by (Supplier):	**Approved by vehicle manufacturers / EMC:**		

Revision History

Date	Description

This Test Plan is approved with the following corrections and/or added conditions:

Modifications to GMW3097:

Date	Description

A.3.1 Product Family Description.

Provide a brief DUT product family description, including any similarities and differences of planned hardware and software revisions. In some cases, it may make sense to select a specific sample for test that represents the entire DUT family. Please state the justification and rationale for doing this.

(to be filled by supplier, enlarge this area as necessary)

A.3.2 Product Functional Description.

Provide a brief overview of the DUT functions, including system interfaces. Use wording that describes the system to those not familiar with the product. Define all abbreviations. Provide a list of all used connector pins and their function.

(to be filled by supplier, enlarge this area as necessary)

A.3.3 DUT Component/Subsystem Level Test Requirements

Determine the required tests for the DUT (complete Table A.3, then Table A.2). For each applicable test, indicate the appropriate DUT test mode number listed in Table A.3. Provide justification if all samples of the DUT are not subjected to the same test condition. Also, provide justification for any omissions in testing for any of the DUT test modes listed.

Note: Table 2 of GMW3097 shall be used to aid in the determination of applicable component and subsystem tests.

Table A.2: Test Requirements Table

GMW 3097 Paragraph	Test applies? Y/N	Number of samples (Note 1) DV	Number of samples (Note 1) PV	DUT Setup figure(s)	DUT Test Mode No.	Test Comment
Radiated Emission – RE						
3.3.1 ALSE						
3.3.2 CE, Artificial Network						
3.3.3 Reverb, Mode Stirring						
Radiated Immunity – RI						
3.4.1 Bulk Current Injection						
3.4.2 Anechoic chamber						
3.4.3 Reverb, mode tuning						
3.4.4 Reverb, mode stirring						
3.4.5 Magnetic field						
Transients						
3.5.1 Conducted Emissions						
3.5.2 Power Lines						
3.5.3 I/O Lines						
3.5.4 Sensor Lines						
3.5.5 (Optional) 85V I/O						
Electrostatic Discharge – ESD						
3.6.1 Power-On Mode						
3.6.2 Remote I/O						
3.6.3 Handling						

Note 1 Minimum number of test samples is two. It takes two (2) samples to pass and one (1) to fail

A.3.4 DUT Operating Modes/Functional Performance Level

All DUT hardware I/O shall be examined, list all DUT I/O in Table A.3. Names may be used in the table to reference DUT test modes and functions as long as a subsequent description of the mode/function is included. The Acceptance Criteria shall equal the upper limit of tolerance deviation specified in the DUT's supporting documentation defining acceptable I/O parameter (CTS, SSTS or other relevant technical documentation). If not specified in other specifications use the following tolerance for voltage and current: +10%, -0%. For frequency, pulse width and timing relationship measurement +/-10%.

Note: Supplier must provide all specialized equipment used for monitoring functionality.

Table A.3: DUT I/O Performance Level

DUT Test Mode #	I/O Description	Function	Monitored By	DUT Pin #	Nominal	Acceptance Criteria	Immunity Level

A.3.5 Device Under Test Electrical Input Requirements.

Indicate input conditions that will place the DUT in the desired test mode(s) defined in Table A.3, DUT I/O Performance Level. List all DUT test modes and the input names used in them. Duplicate entries for input names may exist under different modes. Include any additional information required to support DUT operation during test, including data bus messages, and special test software. Table A.4, shown below should be used to provide this information.

Table A.4: Device Under Test Electrical Input Requirements Table

Test Mode #	Input Description/Name	DUT Pin #	Waveform (sq./sine etc)	Amplitude	Freq/Pulse Width/ etc.	Comments / Other

A.3.6 Device Under Test Non-electrical Input Signals/Characteristics.

Provide the non-electrical input signals/characteristics to make the DUT functional (e.g., light, weight, pressure, liquid, temperature, object, etc.). Include mode information for each signal.

Table A.5: Device Under Test Non-Electrical Input Requirements Table

Test Mode #	Input Description/Name	Details

(to be filled by supplier, place holder for images or drawings if appropriate, enlarge this area as necessary)

A.3.7 Simulator/Exercisers Test Support Requirements.

Illustrate the simulator used during component/subsystem testing including pin numbers, I/O labels, actual simulated load values within the simulator including power and ground architecture. Indicate whether it is an input or output and, if loaded, is connected to a real or simulated termination. Also, include information on additional support hardware/software requirements. Include detailed block diagrams of the load box and/or support equipment. Specify how any support equipment used will be configured so as not to influence the test results.

All loads of the simulator load box shall equal the resistance, capacitance and inductance representing the actual vehicle loads called out within the DUT's supporting documentation (EICD, CTS, SSTS, etc.).

(to be filled by supplier, enlarge this area as necessary)

A.3.8 Specific Test Configurations.

Provide specific test set-up information (do not include copies of generic setup diagram from IEC/ISO/SAE or other EMC standards), including block diagrams, photographs etc. indicating DUT connections to facility and test equipment for each required test identified in Table A.2 in the following test sections. The information provided should permit reproduction of the test by another test laboratory. If a specific test will not be performed, mark "N/A" in the applicable sections.

A.3.8.1 Radiated Emissions (RE) setup

A.3.8.1.1 Anechoic or Reverberation Chamber Radiated Emissions (RE) setup

- For Anechoic testing only: Specify which side(s) of the DUT will face the antenna during test.
- Provide information regarding cable/harness layout and grounding
- Specify other special test arrangements that apply to this test
- Include switching power supplies "boosted voltage" mode, if applicable, to DUT

(to be filled by supplier, enlarge this area as necessary)

A.3.8.1.2 RE, Conducted Emissions, test with artificial network setup.

Please include the following items:

- DUT lines that are to be connected to the LISN
- Specify other special test arrangements that apply to this test
- Include switching power supplies “boosted voltage” mode, if applicable, to DUT

(to be filled by supplier, enlarge this area as necessary)

A.3.8.2 Radiated Immunity (RI) setup

- For Anechoic testing only: Specify which side(s) of the DUT will face the antenna during test.
- Provide information regarding cable/harness layout and grounding
- Specify other special test arrangements that apply to this test

(to be filled by supplier, enlarge this area as necessary)

A.3.8.2.1 RI, Bulk current injection test setup

- Specify if DUT is grounded or ungrounded in actual vehicle implementation
- Provide information regarding cable/harness layout and grounding
- Include description of lines to be run outside the injection probe during differential mode injection
- Specify other special test arrangements that apply to this test

(to be filled by supplier, enlarge this area as necessary)

A.3.8.2.2 Immunity to power line magnetic fields test setup

- Specify what DUT orientations are to be tested - Default configurations are:
  a) DUT face with connector parallel to coils, harness perpendicular to coils and
  b) DUT face with connectors perpendicular to coils, harness parallel to coils
- Specify other special test arrangements that apply to this test

(to be filled by supplier, enlarge this area as necessary)

A.3.8.3 Conducted Emissions (CE) and Immunity (CI)

A.3.8.3.1 CE, Conducted transient emissions test setup

- Specify if production intent switching mechanism is available
- Specify modes of switching to be performed (e.g., Off to On to Stall, etc.)
- Specify other special test arrangements that apply to this test

(to be filled by supplier, enlarge this area as necessary)

A.3.8.3.2 CI, Transient on power lines test setup.

Include lines or pins, which are to be injected to during this test. List all individual lines or pins pulled up to battery, switched battery (e.g. ignition, switched ignition, accessory ignition, run) also include those I/O connected through loads (e.g. bulbs, relay, fuel injectors) to battery or switched battery. Specify if injections are to be applied to separate inputs and/or simultaneously the inputs identified below.

Table A.6: Transient application

Type	Pin	1	2a	2b	3a	3b	4	5b	7

Note: Pulse 1 and 2b are applicable to switched battery lines only.

Note: Pulse 4 is only applicable to B+ and switched battery lines which are powered during cranking.

A.3.8.3.3 CI, Coupling to other than supply lines (I/O lines) test setup

- Specify special test arrangements that apply to this test

(to be filled by supplier, enlarge this area as necessary)

A.3.8.3.4 CI, Direct Capacitive Coupling to Sensor Lines

- Specify special test arrangements that apply to this test

(to be filled by supplier, enlarge this area as necessary)

A.3.8.3.5 (Optional) CI, 85V Direct Capacitive Coupling

- Specify special test arrangements that apply to this test

(to be filled by supplier, enlarge this area as necessary)

A.3.8.4 Electrostatic Discharge (ESD)

This section defines criteria used to identify lines, pins or DUT case locations, which are to be subjected to ESD discharge events during Electrostatic Discharge Component Tests. Identify the ESD discharge points. List all individual pins, case discharge locations, discharge type, simulator voltages, discharge network type and a description of the pin signal.

A.3.8.4.1 ESD, test during operation of the device (power-on mode) test setup

- Specify if DUT is accessible from outside the vehicle
- Specify other special test arrangements that apply to this test

Table A.7: ESD, test during operation of the device (power-on mode) test

Mode	Location (Pin/Case)	Discharge Type (Air/Contact)	ESD Simulator Voltage (kV)	Discharge Network (R/C Value)	Signal / Pin Description / Name

(to be filled by supplier, enlarge this area as necessary)

A.3.8.4.2 ESD, remote inputs/outputs test setup

- Specify special test arrangements that apply to this test
- Specify how bus is to be active during discharging

Table A.8: ESD, remote inputs/outputs test

Mode	Location (Pin/Case)	Discharge Type (Air/Contact)	ESD Simulator Voltage (kV)	Discharge Network (R/C Value)	Signal / Pin Description / Name

(to be filled by supplier, enlarge this area as necessary)

A.3.8.4.3 ESD, handling of devices test setup

- Specify special test arrangements that apply to this test

Table A.9: ESD, handling of devices test

Mode	Location (Pin/Case)	Discharge Type (Air/Contact)	ESD Simulator Voltage (kV)	Discharge Network (R/C Value)	Signal / Pin Description / Name

(to be filled by supplier, enlarge this area as necessary)

Appendix B EMC Lessons Learned/Best Practice

The supplier shall review the contents of this appendix and consider incorporating the applicable lessons learned into the design.

The implementation of the recommendations contained within this section is NOT A REQUIREMENT. The list of lessons learned captured is not all inclusive nor binding and may not reflect the latest technology. Implementation of any of these lessons learned should be verified that they do not adversely affect performance of the DUT.

B.1 Beginning Comments:

It is recommended that “place holders” or provisions for all parts are placed in the very first PCB layout. It is easier and cheaper to remove the provisions later (if not necessary based on testing) than to add them.

Always provide test data to support claims that any of these recommendations will have negative results on product performance.

Avoid using expanded memory microprocessors if possible. This is due to the increased radiated emissions due to expanded buss uP's. The cost of meeting radiated emissions is increased substantially due to possibility of having to contain the emissions with the addition of shielding the case and possibly filtered connectors.

B.2 Printed Circuit Board

B.2.1 PCB design partitioning

- The analog circuits and the digital circuits should be in separate zones.
- The PCB design group High Speed (HS) zones should be kept separate from the low speed (LS) areas.

B.2.2 PCB traces

- HS or Digital traces or reset lines should be kept 2.5 cm away from I/O connectors or ports.
- HS data/control traces should not be in parallel with other traces for more than 1 inch.
- HS data/control traces and IC's should be kept 1.5 cm away from the edge of the board.

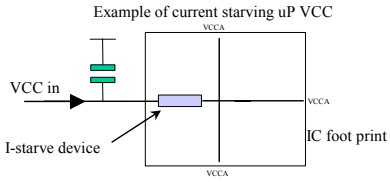
B.2.3 Ground structure

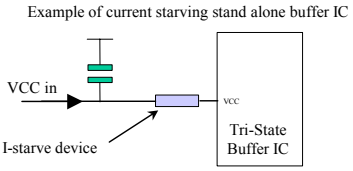
- Multilayer boards are always recommended.
- Keep ground planes uncut, do not route traces on the ground planes.
- Do not have separated grounds (e.g., digital/clean, analog/dirty, 3.3V and 5V) on the board, have only one ground plane.
- All open spaces on outside layers should be filled with ground plane, these ground “islands” need to be tied to the ground plane with multiple via's or many short, thick (low inductance) traces connecting them all together
- PCB - Case connections may need to be made only near the vehicle interface connector, not all 4 corners, keep provisions for connections at all 4 corners if possible (see next guideline)
- Use 0 Ω jumpers to connect the large mounting through hole via's to the ground plane, in preparation for addition or removal of AC or DC connections
- All connections to power and ground planes have to be very short runs - PIN TO PLANE with low inductance paths (unless you are current starving the IC refer to D.2.4)
- Never stack or overlap different power planes over each other
- If using 2 layer board - run power and return side by side or top to bottom - reducing loop area
- If using 2 layer board - run return next to HS digital and critical traces - micro strip protection

- If using 2 layer board - fill all open space with ground plane or grid with many via's
- If using device with 8 MHz clock or higher use at least 4 layers
- Keep high speed lines within inner layers, placed between power and ground planes if possible
- Do not break solid ground plane with high speed, place them on power plane if necessary
- Locate the pins of connectors or devices (if possible) to make room for filling in the area between the legs with copper

B.2.4. Power structure

- Provisions for current starving the uP and/or memory is recommended for IC's with 5V supplies or greater which are known to be a source radiated emissions, or cause high speed conducted transients on its power supply line (*care must be taken to ensure functionality, such as oscillator startup*)
- Power supplied to uP and/or memory should be through properly sized traces, not power planes, this reduces the stray capacitance between the power structure and ground structure and enhances the performance of the current starving device (resistor, inductor or ferrite bead)
- Providing separate power feed structure to main uP is recommended, whether the IC uses a single or multiple VCC's
- Feed all the individual VCC traces under the IC through one point, a single 0 Ω jumper, which may be replaced if necessary with a current starving device after RE testing
- Place any RF "bypass" caps on the VCC feed side of 0 Ω jumper ONLY, NOT on IC side of jumper, this eliminates the function of the current starving device (resistor, inductor or ferrite bead)
- Replacing the 0 Ω jumper with inductor (BLM32801, 1000 Ω @ 100 MHz or equivalent) or series resistor to impede RF current may be necessary after RE development testing
- If it is found necessary to current starve a tri-state buffer for example (see below), it is recommended that each of the inputs referenced to VCC also have provisions for the same current starving device, it has been found that sneak currents will reduce the effectiveness of the single VCC current starving device





B.2.5 IC's with separate Vref (PLL) and VDDA pin or pins

- For uP's with separate Vref (PLL) and VDDA pin(s) provide provisions for a series ferrite bead (1000 Ω @ 100 MHz) between VCC and the PLL pin, this may reduce radiated emissions

B.2.6 IC's with internally connected Vref and VDDA pins

- For uP's with internally connected Vref (PLL) and VDD add single ferrite bead to feed all pins refer to D.2.4

B.2.7 IC'S with internal pull-ups to 12V or require external pull-up to 12V for I/O

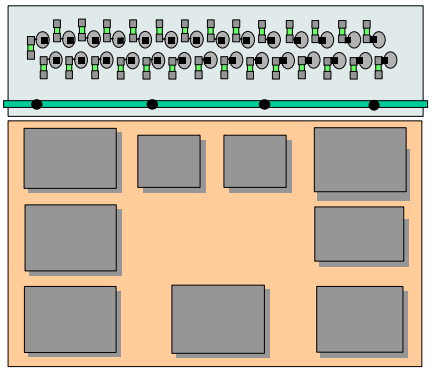
- Provide for adding series 1000 Ω with each I/O referenced to 12 volts
- Provide for external clamping of I/O voltages greater than IC supply voltages.

B.3 Interface Connector and Cables

B.3.1 RF "bypass" capacitors on PCB without filtered header connector

- Use 680 pF to 10 nF on all PCB I/O when not using a filtered header connector
- As a minimum requirement the layout shall include pads to support adding of bypass capacitors directly at the I/O connector
- Use SMD ESD robust capacitors with very little to no trace length to ground (capacitor working voltage DC, WVDC, is not necessarily a good indicator of ESD robustness)

Example: the I/O pin shall be connected directly to the bypass capacitor when entering the device. The bypass capacitor shall be connected directly to the ground plane through the lowest impedance path. The signal to the I/O circuitry should be taken from the bypass capacitor not the I/O pin.

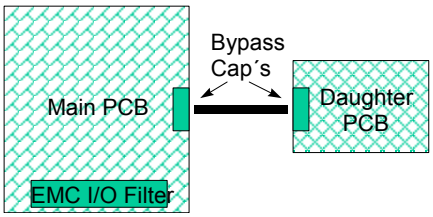


B.3.2 RF "bypass" capacitors on PCB I/O with filtered header connector

- All of the pins should have 1 nF to 15 nF capacitor that will not affect proper functionality.
- The body of the connector should make reliable connection to the ground plane.
- If there is only one ground wire it should be located at the center of the connector.

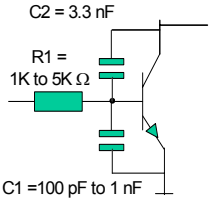
B.3.3 RF “bypass” capacitors on PCB I/O with multi-board module (mother/daughter configuration)

- Use of 680 pF to 10 nF on all signals is recommended
- Minimum requirement the layout should include pads to support the addition of bypass capacitors directly at the I/O connector
- Use SMD capacitors with very little to no trace length to ground

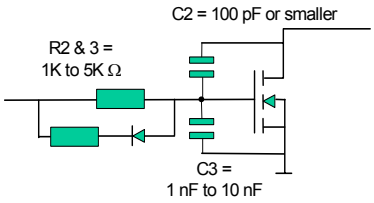


B.3.4 Module I/O slew rates

- All PWM or switching I/O leaving the module should have a dV/dt < 1 V/μs and a dI/dt < 300 mA/μs or slower if possible.



Transistors having high bandwidth should have provisions for C1 & C2

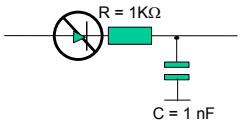


Parallel resistor/diode combination is for edge or slew rate control as well as provisions for feedback capacitors

- Provisions for shield connections and/or specialty connectors (360 degree clamshell) may be considered if the slew rates described above are not met
- Connector pin assignment is important when working with twisted harnessing, be sure to locate the terminals adjacent to each other in the same connector

B.3.5 Diodes on inputs and outputs

- Low pass filters with series diodes should be avoided to minimize radiated immunity issues, caused by RF rectification; this does not include transient suppression on battery or ignition inputs.



- A “snubber” (capacitor or resistor/capacitor) may be required across diodes used in switching applications (e.g. boost transformers, etc.)

B.3.6 Input filter time constants

- Input filter time constant should be at least 1 mS, especially for analog inputs

B.3.7 ESD protection for I/O

- Add appropriate ESD protection (transorbs, back-to-back zener diodes, series inductance, RC-filter, etc) on each I/O that is accessible by the passengers or test equipment, e.g., communication lines. This includes directly accessible faceplates, displays, and remote buttons and test connectors

B.3.8 Ratio metric I/O voltage reference

- Use ratio metric methods using the reference voltage A/D value compared to the input voltage A/D value for measuring analog inputs of the DUT, if fluctuation of the power supply voltage occurs due to RF, the effects will be reduced on A/D's

B.3.9 Transient suppression and inductive loads

- Suppression device, typically a diode or Metal Oxide Varistor (MOV), should be referenced to ground with shortest path as possible
- FET devices may be capable of surviving these transients, however, bipolar devices will require extra protection (e.g. zener diode, MOV etc.)

B.4 Circuits, Traces and RF Bypassing

B.4.1 “Bulk storage” capacitance (RE & CE)

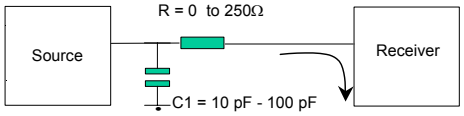
- There should be at least one bulk storage capacitor on the PCB
- The bulk capacitor should have low Effective Series Resistance (ESR) value
- Use bulk capacitor values at least 10x the total individual decoupling capacitor value of the whole PCB. If more than 20 ICs are on the PCB use more than one bulk capacitor, distributed on the PCB so that there is a capacitor close to every 10-15 ICs.
- The capacitance value should be calculated from: C = dI * dt/dV, where dV is the acceptable transient voltage drop in the power supply, typically < 0.1V

B.4.2 RF "bypass/decoupling" capacitance (RI)

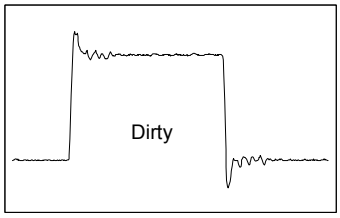
- Use SMD components with very short to no traces to the return plane.
- Do not choose a large value of capacitor. This may result in too low self-resonance $f=1/(2*\pi\sqrt{L*C})$.
- Use the smallest capacitor that will do the job, typical values are 1-10 nF.
- Logic IC's - calculate with 50% of the gates switching simultaneously
- Dynamic RAM - refreshes all cells simultaneously, typically 100 nF is needed for 256K of RAM)

B.4.3 Clocks and address/data traces

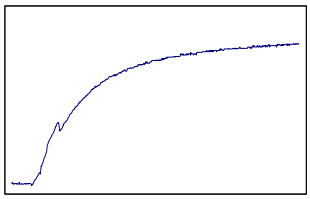
- Unused configurable I/O should be internally configured as an output and internally switched to ground, reducing radiated immunity risk
- Avoid using configurable ports as I/O if they also can be configured as a clock output, to reduce radiated emissions risk due to coupling from the digital core of the µP
- Provisions (zero ohm jumpers) for series resistors on clock address/data lines at their source is recommended where possible, to minimize the transient current and control the slew rates
- Use SMD components with very short traces to the return plane.
- Minimize all traces to be as short as possible
- Route clock traces between power and ground planes if possible
- Do not jump between layers with these traces, via's = 1-2 nH of inductance each
- If an internally slew rate controlled uP is used, these recommendations may not be necessary.
- Provide pads and space for capacitor(s) to ground on each trace located at the source end(s).
- Note: for data busses this may mean splitting the capacitor value between devices
- All high-speed control rise and fall times should be minimized or slowed down as much as possible



Example:50Ω and 50 pF represents a delay of 2,5 ns.

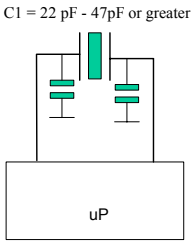


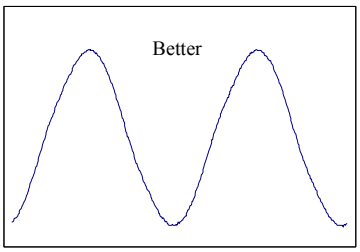
If after placing the capacitance, the waveform develops a non-linear hump (refer to image on right) it may be necessary to current starve the power feed to the uP by adding series device (refer to D.2.4) to reduce risk of radiated emissions.



B.4.4 Crystal or resonator waveform

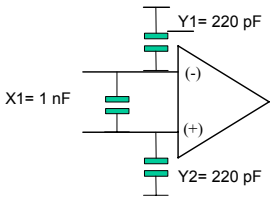
- Waveform should be as sinusoidal as possible
- Use SMD components with very short traces to the µP ground return
- Begin with 22 - 47 pF capacitors, increase until sinusoidal waveform is achieved
- The capacitors may be of different values, typically the driven side (XTAL) is of a higher value





B.4.5 Op-amps and comparators

- Provisions for 1 nF "X" capacitors should be made (between (-) and (+) inputs)
- Provisions for 220 pF "Y" capacitors should be made (between (-) or (+) and ground)
- Traces are required to be symmetrical to each other or balanced with little trace length
- Use resistor dividers, not diodes, to set reference voltages when necessary, diodes can rectify RF

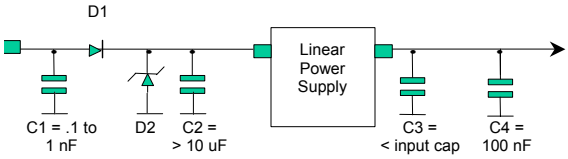


B.4.6 Reset and non-maskable interrupt I/O

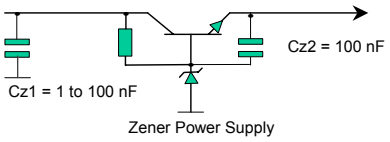
- Provisions for a 1 nF capacitor to ground should to be located at both the reset source and receiver device and source and receiver of non-maskable interrupts, to prevent ESD and RI sensitivities
- Provisions for series 100Ω resistor or proper ferrite bead (depending on RI testing), should also be placed on each reset and non-maskable interrupt trace, populate with 0 Ω jumper

B.4.7 Linear Power Supplies

- Provisions for overvoltage, load dump event and reverse voltage protection should be located on battery 12V input
- Transient protection should be located on all I/O pulled up to battery 12 V
- Input capacitance must be larger than output capacitance
- C1 should be SMD low loss capacitor (100 V) located before C2
- C2 - power input filter should provide 20 dB of attenuation at 100 kHz using bulk storage electrolytic (C[μF] = 16 / R, R [Ω] = DC resistive load or 10 uF which ever is greater)

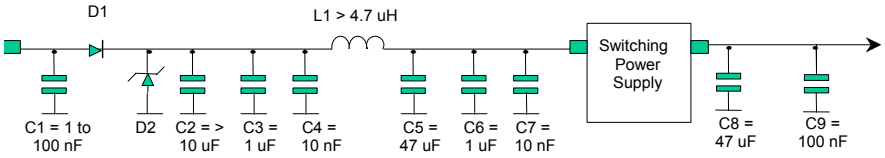


Zener power supply (usually used within the circuit board)



B.4.8 Switching Power Supplies

- Recommend lowest frequency possible to protect AM band from switching harmonics
- The number of capacitors and values are recommendations, you may need more inductors, capacitors and at different values, refer to manufactures recommendations
- Use only low ESR capacitors
- Populate around via's at the pad that is to be referenced to ground, no long paths or traces



B.4.9 Test Connectors and Software

- Place series zero ohm jumpers near the μP on all traces leading to test connectors, to facilitate removal after product development is complete, reducing the radiated emissions risk
- Turn off via software any and all μP clock or data outputs that are not necessary

B.5 Communications

B.5.1 High Speed Dual Wire CAN

- Refer to GMW3122 for physical layer

B.5.2 Optical LED driver (FOT)

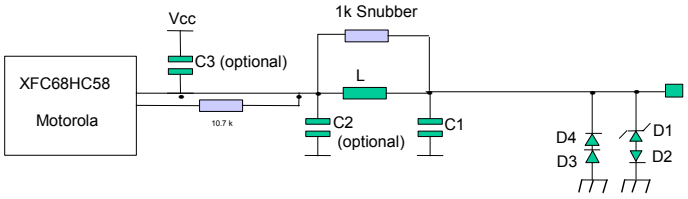
- EMI filtering for the MOST chip and Bigfoot see MOST OS8104 recommendations

B.5.3 Single Wire CAN

- Refer to GMW3089 for the physical layer

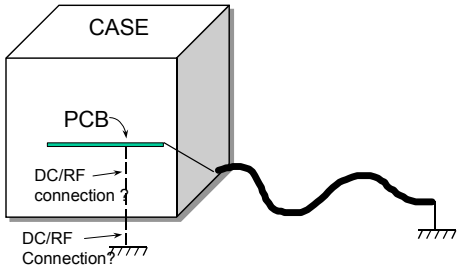
B.5.4 SAE J1850 Buss / Class 2

- **L** = 47uH
- **C1** = 470 pF
- The layout should include pads to fit **D1** for ESD protection (TPSMA 16A recommended (single package) before the 47 μH line inductor **L**
- It may be necessary to protect the IC against (-) transients, if so additional diodes may be necessary **D2/D3/D4** (ES1D SMD), provide provisional pads, if this option is used there will be a risk of Class 2 buss latching if the ground is removed from the module, a reduntant module ground wire and chassis mounting is the only solution to minimize this risk
- Non populated pads for bypass capacitors **C2** and **C3** shall be implemented (typical 100 pF each, for immunity & emission) - either **C2** or **C3** may be populated based on component test data
- If **C2** or **C3** is added they shall not affect the specified total RC constant of the node
- Node capacitance = (C1 + (CD1*CD2)/(CD1+CD2)+(CD3*CD4)/(CD3+CD4) + C2 or C3



Example of SAE J1850 / Class 2 Circuit

B.6 Mechanical Containment



B.6.1 Shielding Dimensions

- The largest dimension of any discontinuity should be less than λ /20 for less than microwave frequencies (commercial) and less than λ /50 at or above microwave frequencies (military)
- λ [m]= 300 / frequency MHz
- Example of λ /20 is 100 MHz = 15 cm, 1 GHz = 15 mm cm

- Cutoff frequency is f_c = C / 2d, where C is propagation velocity of electromagnetic wave
- RF will pass freely through an aperture for wavelengths λ < 2 * longest aperture
- For wavelengths > 2 * maximum dimension, attenuation is R (dB) = 20 Log (λ / 2d), where 2 > d > t, t = material thickness, this does not work if noise source is within the same distance of largest aperture

B.6.2 Seams

- Seams act as capacitors, overlap should be 5 X 1, meaning overlap should be 5 times the spacing between surfaces
- Seam contact points should be placed according to λ /20 or λ /50 rule
- Using screws, fasteners or other forced contact methods

B.6.3 Conductive gaskets

- Conductive gaskets are recommended if: Total shielding needs exceed 40 dB, seam openings > λ /20 or λ /50, emissions/immunity threat > 100 MHz, machined mating impractical, dissimilar materials being used (galvanic reaction), environmental (dust, vapor etc.)

B.6.4 Aperture openings

- If possible, keep all RF generating sources away from aperture openings

B.6.5 PCB ground reference

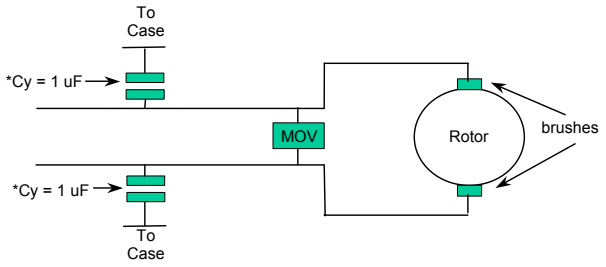
- Connect the PCB ground to case chassis at vehicle connector edge only, not all four corners. Provisions for all 4 corners is acceptable, then determining best configuration during testing
- PCB via's for this connection should be connected using 0 Ω jumpers, allowing them to be replaced with bypass capacitors if found necessary during product development or if requiring an RF instead of DC connection

B.6.6 Additional shielding recommendations

- When possible use the a heat sink (connected to PCB ground) to create an RF “fence” to assist in attenuating stray RF from re-coupling onto the harness I/O connector
- When possible use additional custom details “cage” or “walls” in the metal case or cover to protect or shield the harness I/O connector. These may assist in reducing the need of a filtered header connector to reduce stray emissions.

B.7 Motors

- MOV (for conducted transient emissions)
- Connect case to return at brush holder (single directional motors)
- Cy = 1μF (bi-directional motors)



* Short duration motors (such as seat position, lumbar, windows, mirrors, tilt/telescoping, washer pumps, etc) should be developed with all RF suppression devices in place, allowing for a “parts delete” version depending on the platform needs