

8-bit asynchronous SAR ADC
Based on 180nm CMOS Technology
Critical Review Report

Team 4

Members: Tao Liu, Ding Wang

TA: Jaeung Ko

STEPS to finalization:

This week we finish all the layout and perform the post-simulation for the whole chips. Also, we finalized the structure of ADC to final state. With every block works correctly, before extraction we could get **7.048** bits for ENOB.

Firstly, we finalized the structure of our design, especially the DAC and Clock Generator Blocks. In DAC block, we increased the size of Transmission Gate to make them more stable and have good performance. In Clock Generator part, we modified the different Delay Block, eliminated the capacitors and restructure them with minimum numbers of Delay Blocks.

Then, we made a really neat and compact Layout with all blocks in the center of Gard Rings and Pads. We pour the empty space with strong VDD(M2) and GND(M1). Also, we add 6 additional bypass capacitors to reduce the inductance impacts.

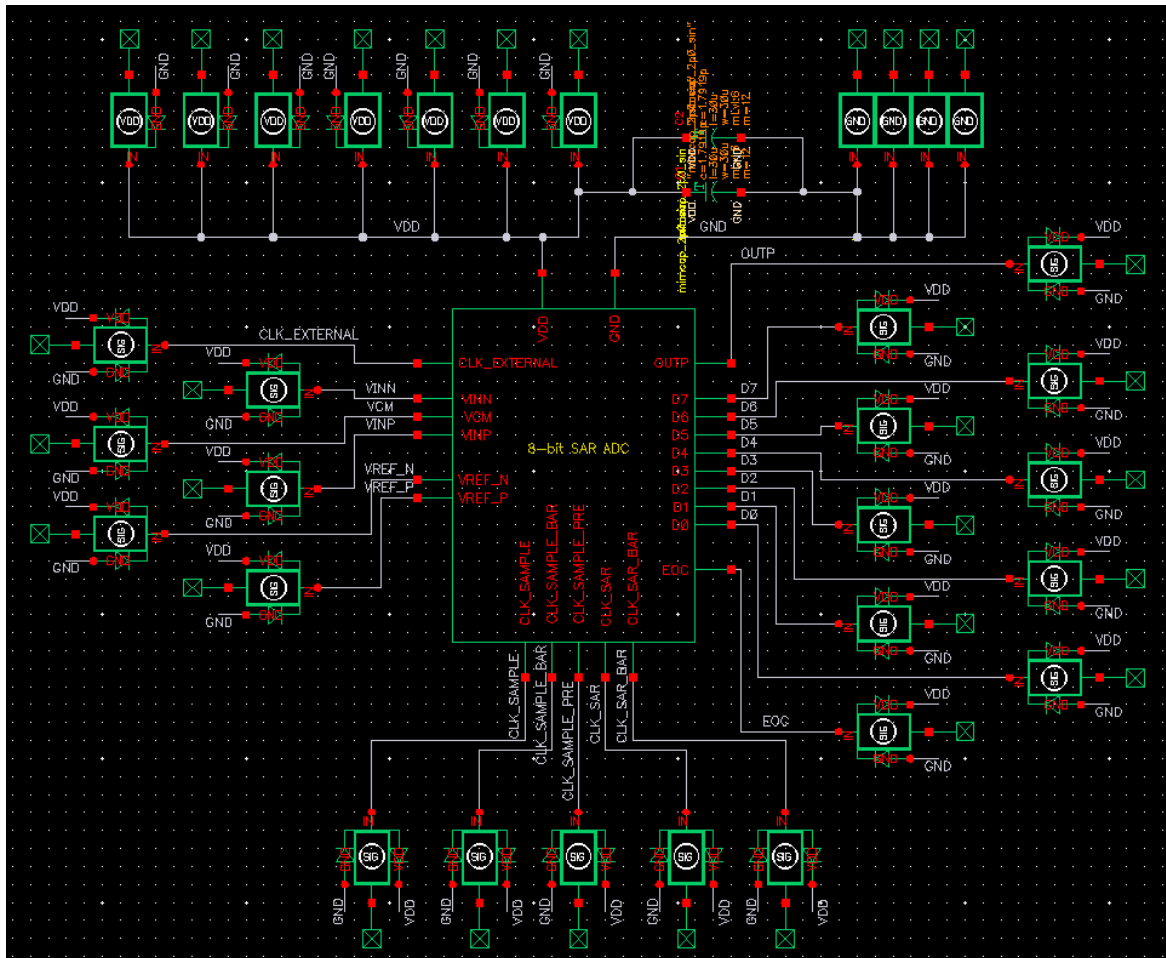
Lastly, we make a symbol for the whole chips, giving them input signals to see the performance of ADC, during which we see the really great performance and also calculate power from it.

Final layout file of the chip:

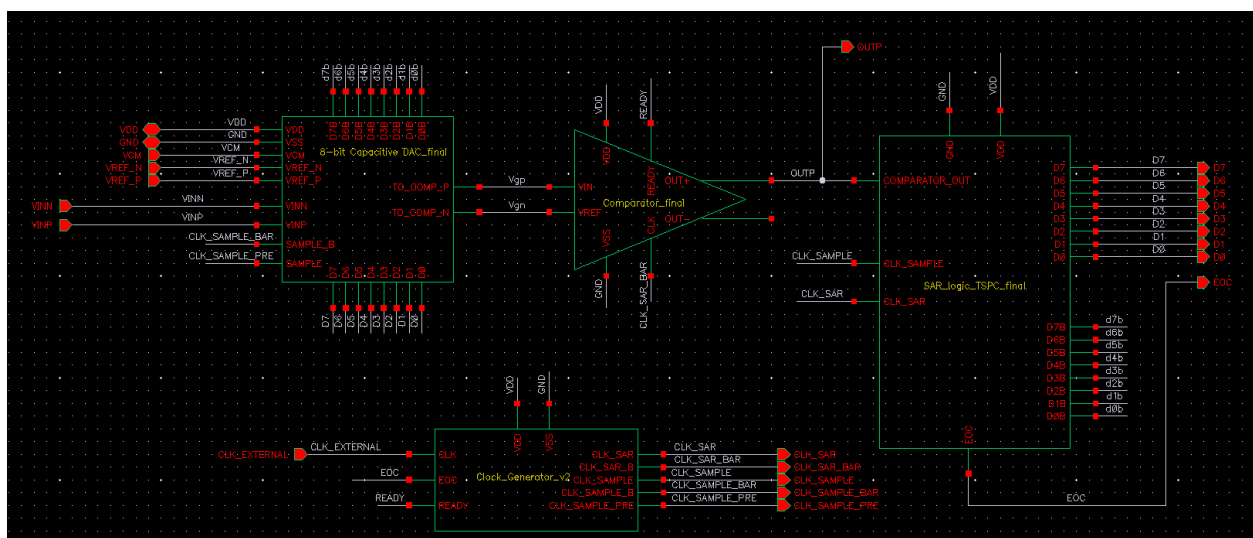
/home/home1/chips2024team4/TSMC_180_work

/final_proj_8bit_SAR_ADC/TOP_LEVEL_with_PADS

Top-Level Schematic with PADS



8-bit SAR ADC: ON-Chip Blocks



Our SAR ADC includes 4 PARTS: Capacitor DAC (Sample & Hold Block exists in it), Comparator, SAR Logic, and Clock Generator.

Update from Design Review 2

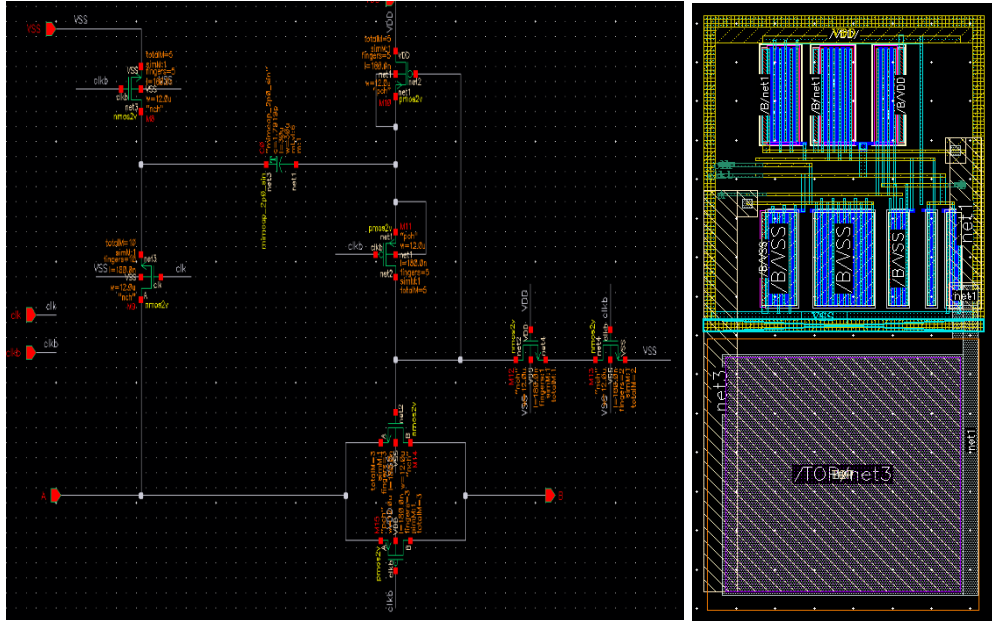
The Main change from Design Review 2 is the Layout. We made the whole layout including Pads and Guard Rings, which gives us the ability to extract the layout to see the post simulations.

Also, we revised the circuits to the best performance as we can, and made a whole symbol for it, so that we could measure the Total Power from our circuits.

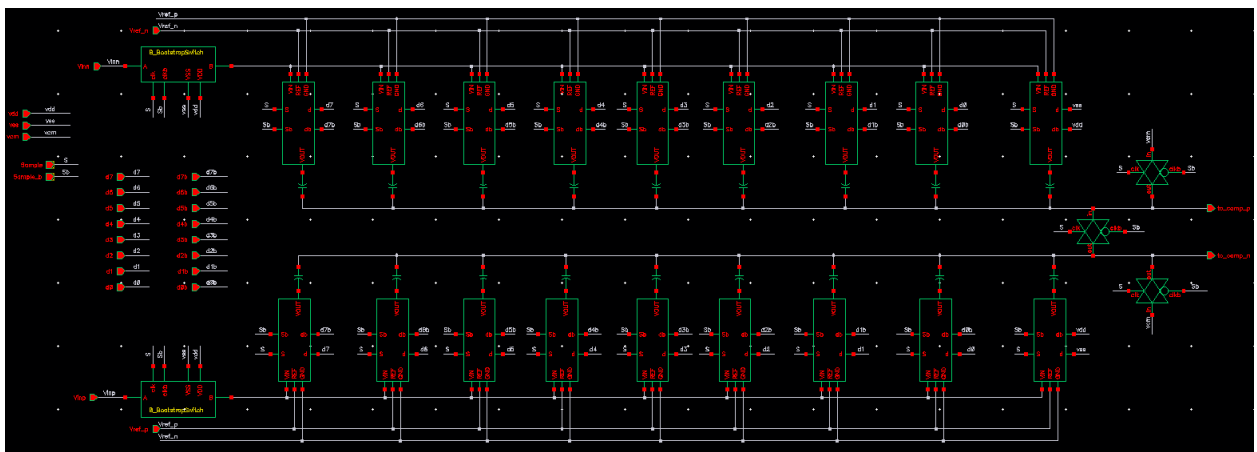
Block And Layout Design

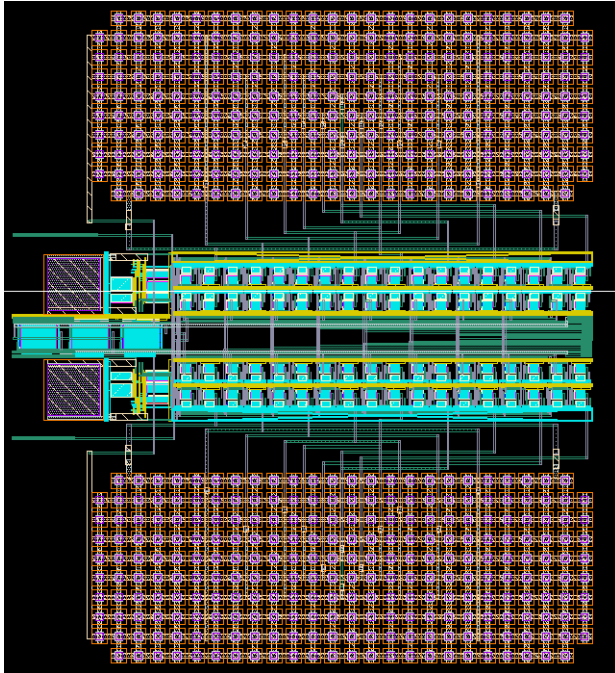
All ROOT file for the simulation & Layout is: /home/home1/chips2024team4/TSMC_180_work/

1. Bootstrapped Sample-And-Hold Circuit (final_proj/Sample_Hold_v2)



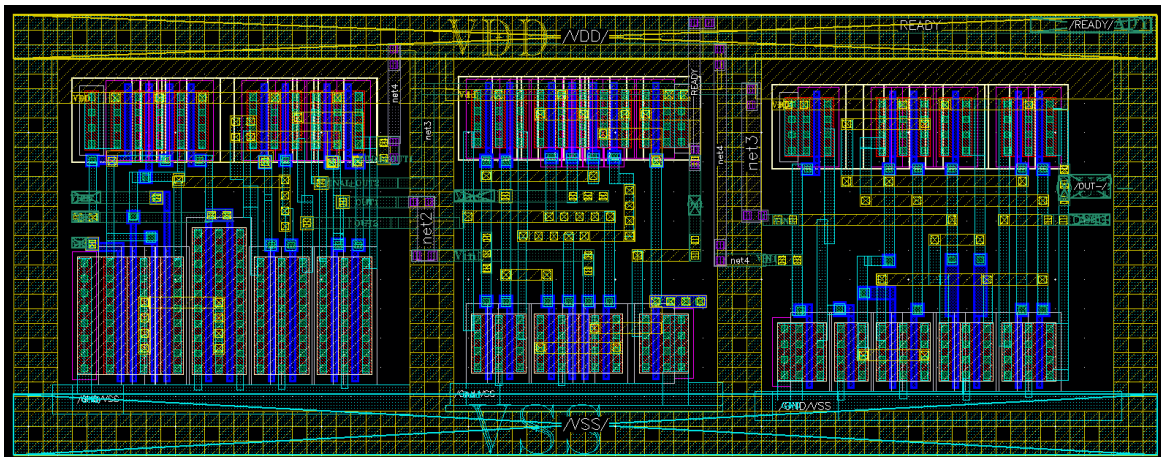
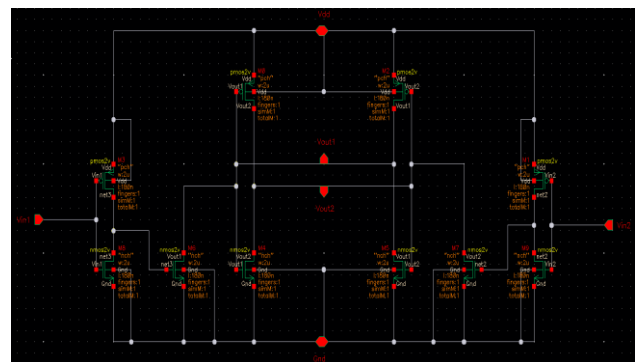
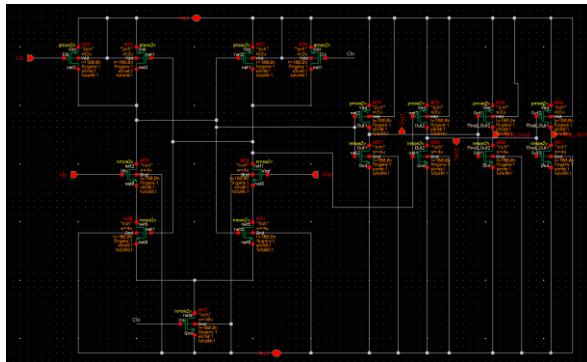
2. Capacitive DAC (final_proj_8bit_SAR_ADC/Capacitive_DAC_final)





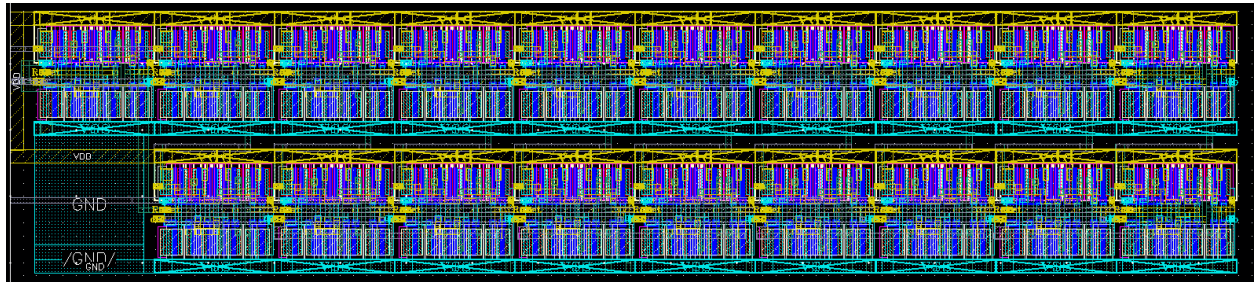
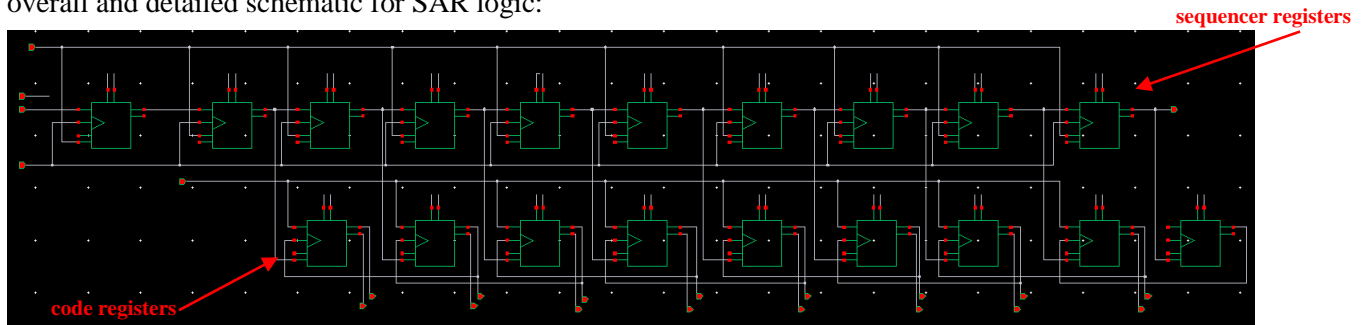
3. Comparator (*final_proj_8bit_SAR_ADC /Comparator_final*)

schematic&layout for Strong-Arm Comparator & RS Latch

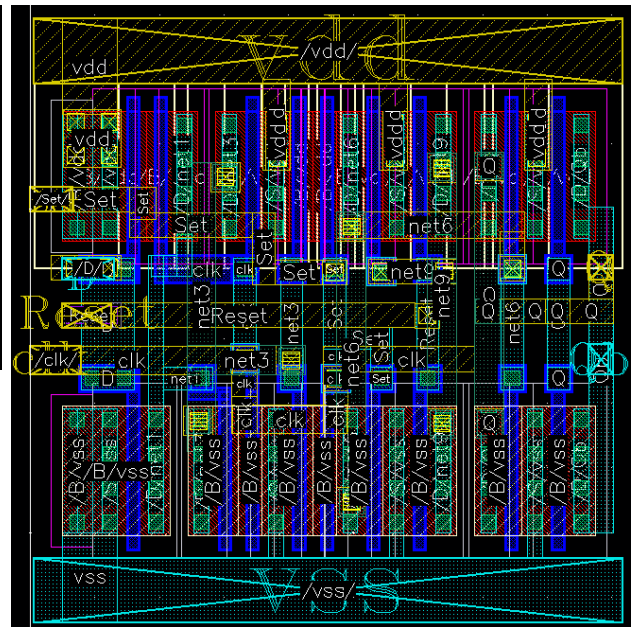
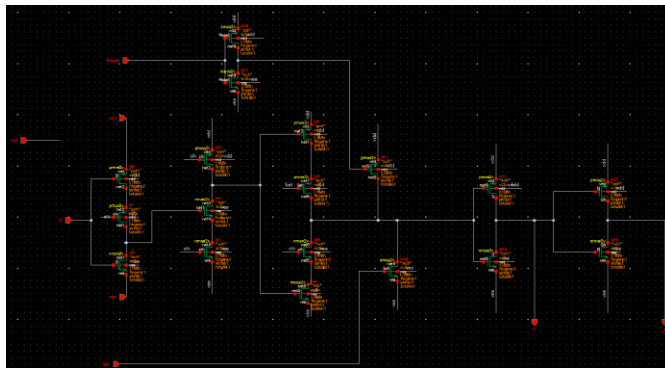


4. SAR Logic Circuit (*final_proj_8bit_SAR_ADC /SAR_final*)

overall and detailed schematic for SAR logic:



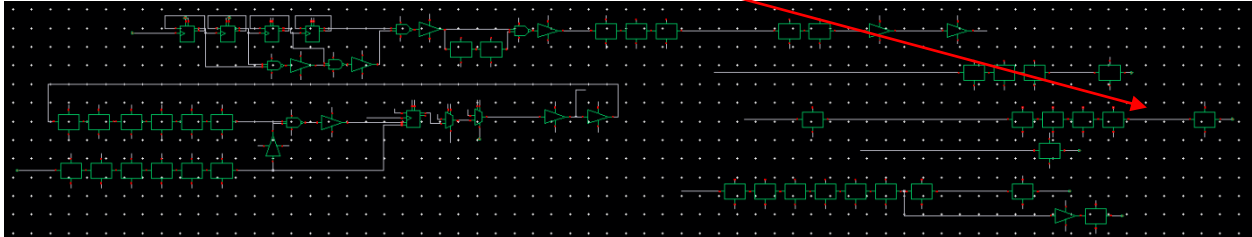
Here below are the schematic and symbol for TSPC FF: (*final_proj_lib /TSPC_ff*)



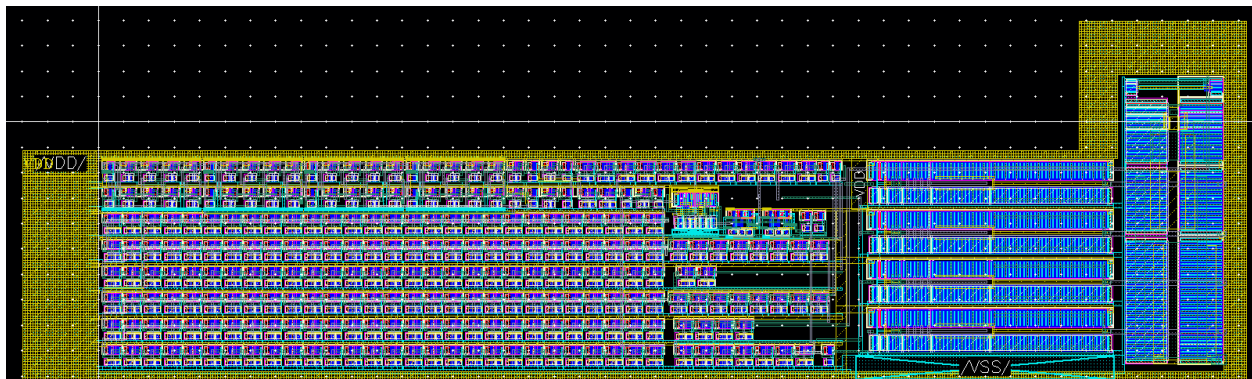
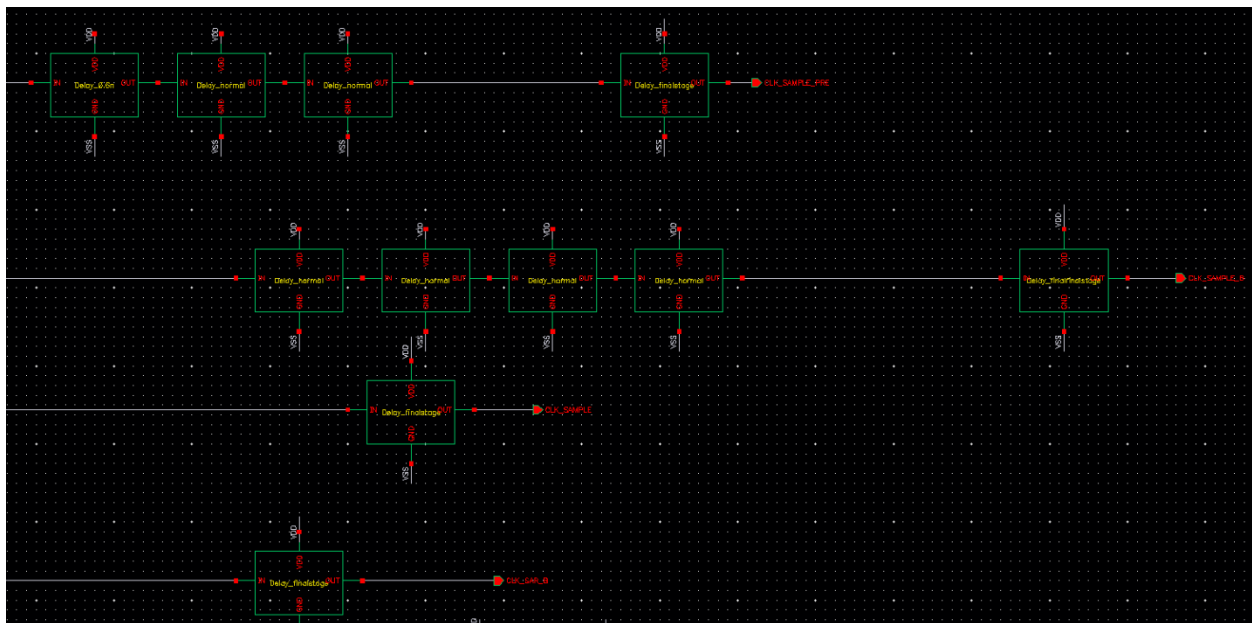
5. Clock Signal (*final_proj_8bit_SAR_ADC /Clock_asyn_final*)

As for **Asynchronous** ADC, each block will apply different Clock Signal with certain delay and different frequency. We build the Clock with this schematic:

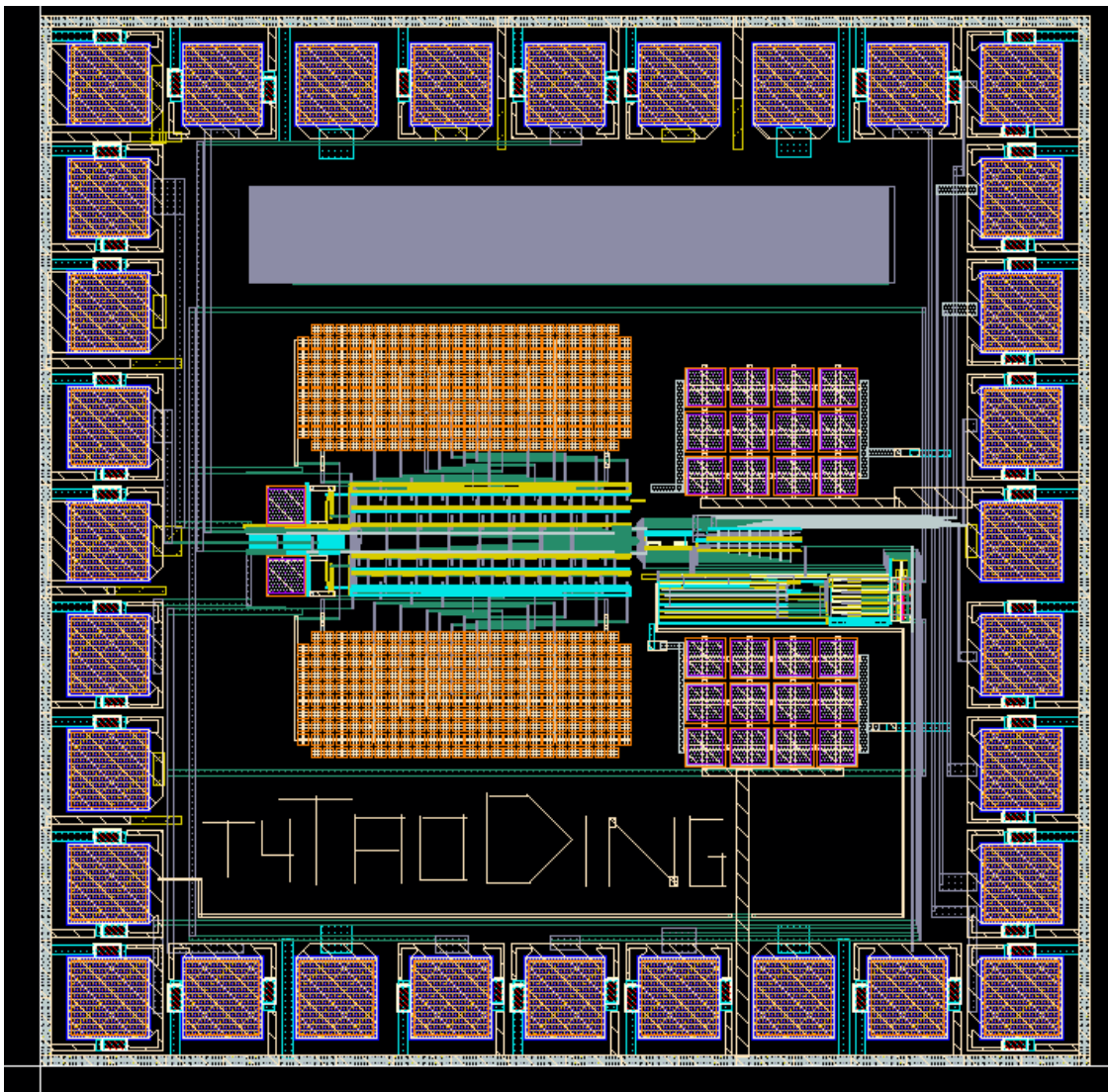
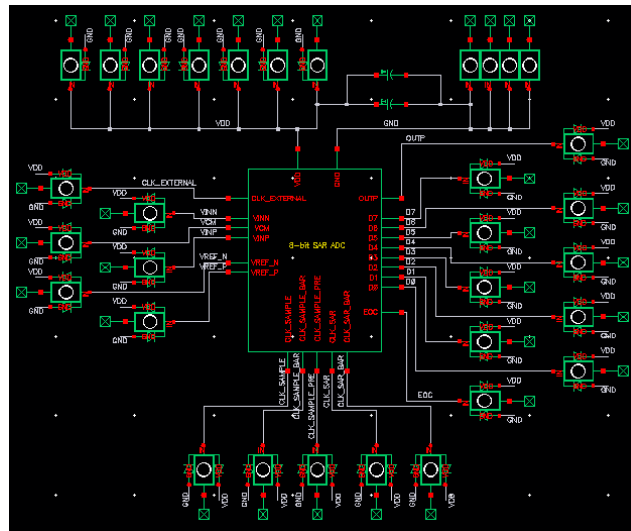
The input is a 100MHz clock. With this clock, we utilize 4 D Flip-Flops (DFF) to generate the sample clock with a 10ns sample time and a 150ns hold time. The reason for allocating a significant hold time is to ensure sufficient time for the SAR clock to iterate 8 times, generating 8 digital bits within one external clock cycle. Following the logic, we apply different buffer blocks to drive the clock signal with a relatively small load, and also to minimize the difference and mismatch with each of clock.



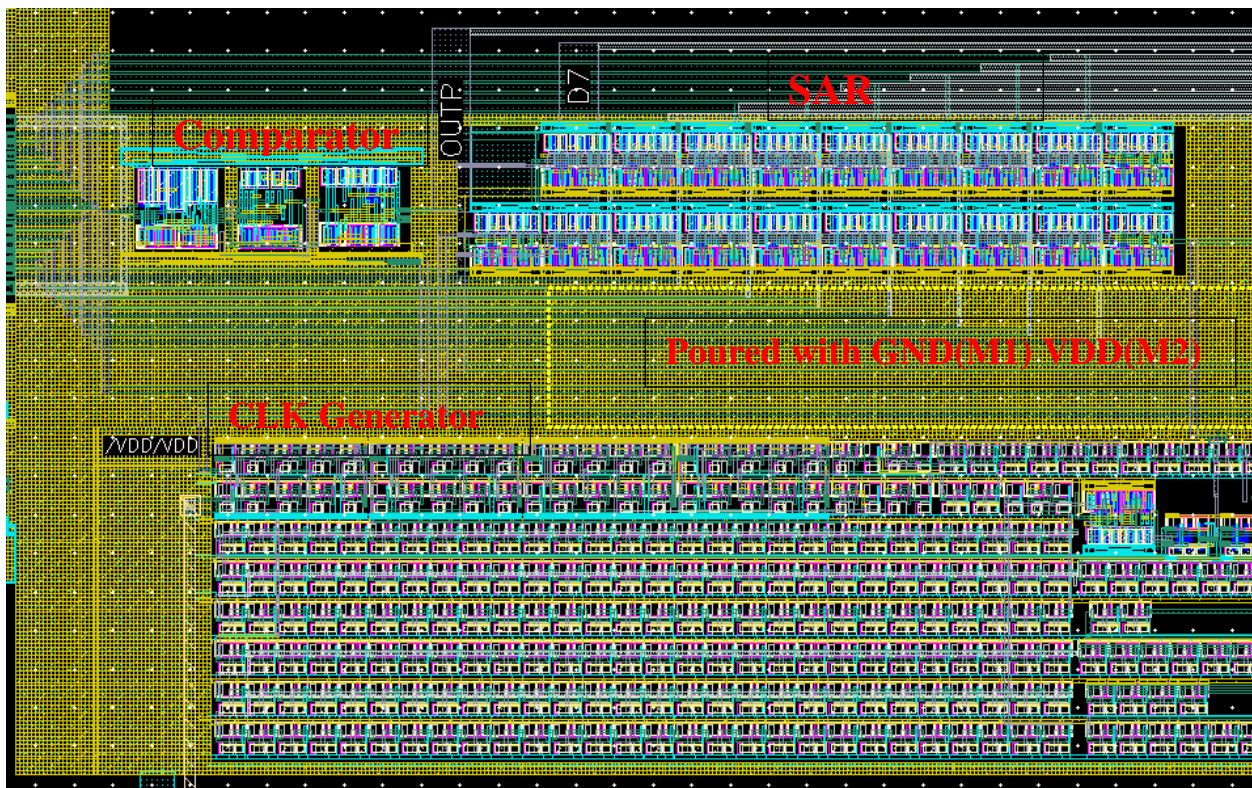
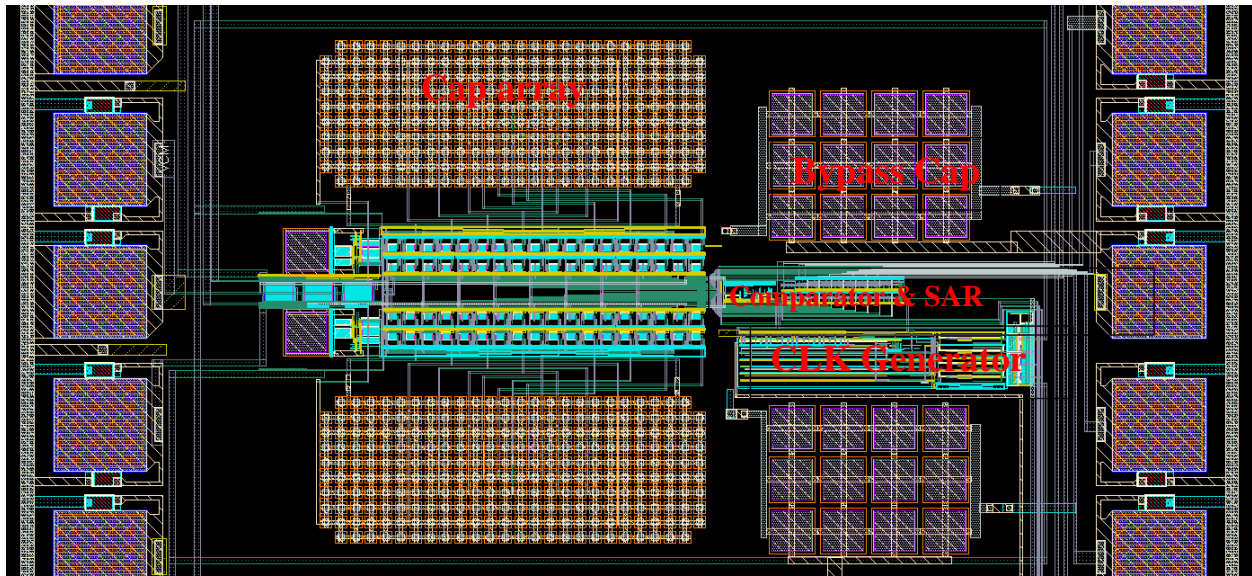
In detail, we design lots of delay block to generate the dedicated delay time to satisfy our needs.



6. Final Chip Layout(final_proj_8bit_SAR_ADC/TOP_LEVEL_with_PADS)



Detailed:



Passing ALL DRC & LVS:

The screenshot displays the Calibre RVE 2023.2.35.23 software interface. The top window shows the 'TOP_LEVEL_with_PADS.drc.summary' report, which includes the following details:

- Execution Date/Time: Mon Apr 22 21:26:21 2024
- Calibre Version: v2023.2_35.23
- Rule File Pathname: /home/101/chips2/ork/DRC/DRC_RUNSET * - v2023.2_35.23
- Rule File Title: _AUT_DRC_
- Layout system: GDS
- Layout Path(s): TOP_LEVEL_with_PADS-calibre.db
- Layout Primary Cell: TOP_LEVEL_with_PADS
- Current directory: /home/101/chips2/ork24team4/TBNC_180_work/DRC/chips2024team4
- User Name:
- Maximum Results/Rulecheck: 1000
- Maximum Result Vertices: 4096
- DRC Results Database: TOP_LEVEL_with_PADS.drc.results (ASCII)
- Layout Depth: All
- Test Depth: PRHABT
- Summary Report File: TOP_LEVEL_with_PADS.drc.summary (REPLACE)
- Geometry Flagging: ACUTE = YES IRM = YES ANGLE = NO OFFROAD = YES
- Nonismpole Polygon: YES Nonismpole Path = NO
- Excluded Cells:
- CheckTest Happings: ALL TEXT
- Layers: MEMORY-BASED
- Notes: Memory checks: YES

The bottom window shows the 'Calibre - RVE 2023.2.35.23: TOP_LEVEL_with_PADS.drc.results' 3D model of a building layout. The model features a central courtyard area labeled 'TYTFOODING' and is surrounded by a grid of buildings. The interface includes a search bar and a 'Show Results Found' button.

The screenshot displays the Calibre DRC (Design Rule Check) software interface. The main window is titled "Calibre Interactive - nmDRG v2023.2.35.23 - home/home1/chips2_erk/DRC/DRC_RunSet *". The left sidebar contains a menu with options: Rules, Inputs, Outputs, Run Control, Search, Transcript, and Run. The main area shows a summary report for the file "TOP_LEVEL_with_PADS.drc.summary". The report details the execution date, version, rule file path, and various settings for the DRC run. The right side of the interface shows a 3D model of the PCB layout, with the text "TYTODING" visible on the board.

Calibre Interactive - nmDRG v2023.2.35.23 - home/home1/chips2_erk/DRC/DRC_RunSet *

File Settings Configurations Help Search

Rules
Inputs
Outputs
Run Control
Search
Transcript
Run

TOP_LEVEL_with_PADS.drc.summary x Calibre

```

===== CALIBRE: DRC-R SUMMARY REPORT =====
Execution Date/Time:      Mon Apr 22 21:25:17 2024
Calibre Version:          v2023.2.35.23   Tue Jun 6 13:39:40 PDT 2023
Rule File Pathname:      _calibre.drc_
Rule File Title:
Layout System:            ods
Layout Path(s):           TOP_LEVEL_with_PADS.calibre.d
Layout Primary Cell:      TOP_LEVEL_with_PADS
Current Directory:        /home/home1/chips2024team4/TSMC_T8MC_work/DRC
User Name:                chips2024team4
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:  4096
DRC Results Database:     TOP_LEVEL_with_PADS.drc.results (ABOI)
Layout Depth:            ALL
Text Depth:              PRIMARY
Summary Report File:      TOP_LEVEL_with_PADS.drc.summary (REPLACE)
Geometry Flagging:       ACUTE = YES GRN = YES ANGLED = NO OFFGRID = YES
                           NONHOLE POLYGON = YES NONHOLE PATH = NO
Excluded Cells:
CheckText Mapping:
Layers:
Keep Empty Checks:       YES
=====

```

Run DRC
Show RVE

Calibre - RVE v2023.2.35.23: TOP_LEVEL_with_PADS.drc.results

nv Highlight Tools Window Setup Help Search

Show Not Waived No Results Found

Check / Cell Results

TYTODING

The left screenshot displays the Calibre RVE interface for a comparison between two PCB layouts. The window title is 'Calibre - RVE v2023.2.35.23: svdb TOP_LEVEL_with_PADS'. The left sidebar contains a tree view with 'Files' selected. The main area shows a comparison report for 'TOP_LEVEL_with_PADS.lvs.report'. The report lists the following details:

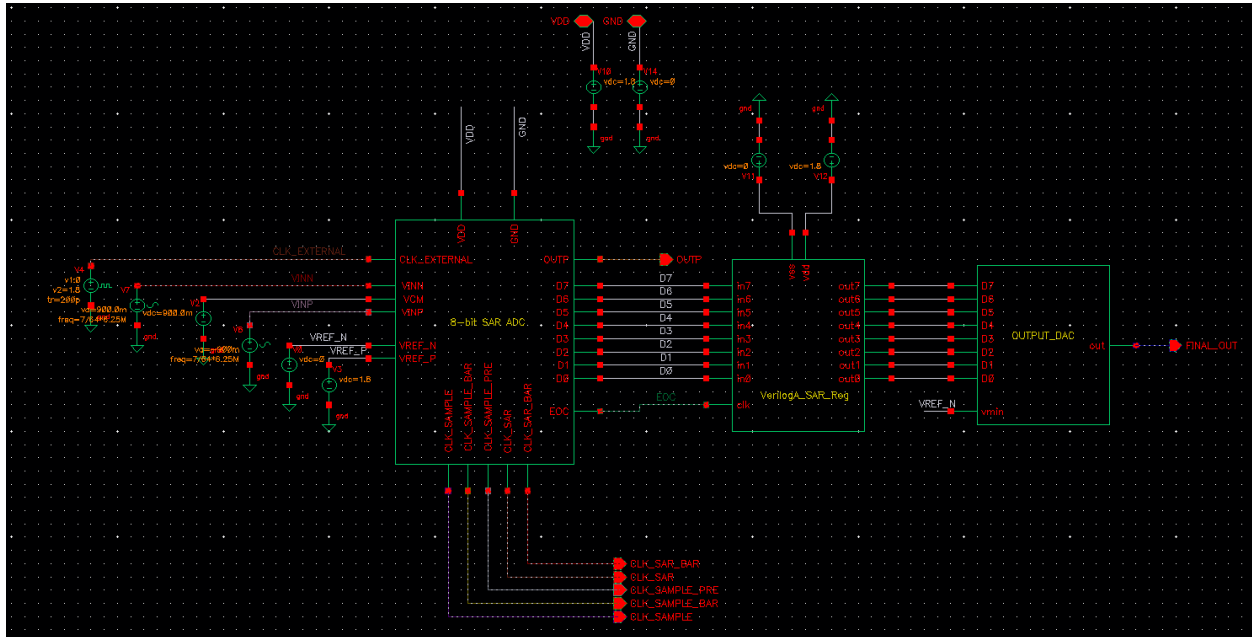
- REPORT FILE NAME: TOP_LEVEL_with_PADS.lvs.report
- LAYOUT NAME: TOP_LEVEL_with_PADS.sp ('TOP_LEVEL_with_PADS')
- SOURCE NAME: TOP_LEVEL_with_PADS.src.net ('TOP_LEVEL_with_PADS')
- BOARD FILE: calibre.lvs
- CREATION TIME: Mon Apr 22 21:33:18 2024
- CURRENT DIRECTORY: /home/home1/chips2024/team4/FSMC_180_work/LVS
- USER NAME: chips2024team4
- CALIBRE VERSION: v2023.2.35.23 Tue Jun 6 15:13:40 PDT 2023

The comparison result is 'CORRECT'. A warning message states: 'Warning: Ambiguity points were found and resolved arbitrarily. Warning: lvs property resolution maximum exceeded.'

The right screenshot shows a 3D model of a PCB layout. The model features a central core with a grid of components, surrounded by a ring of components. The text 'TYTADONG' is visible on the central core.

Simulation Results

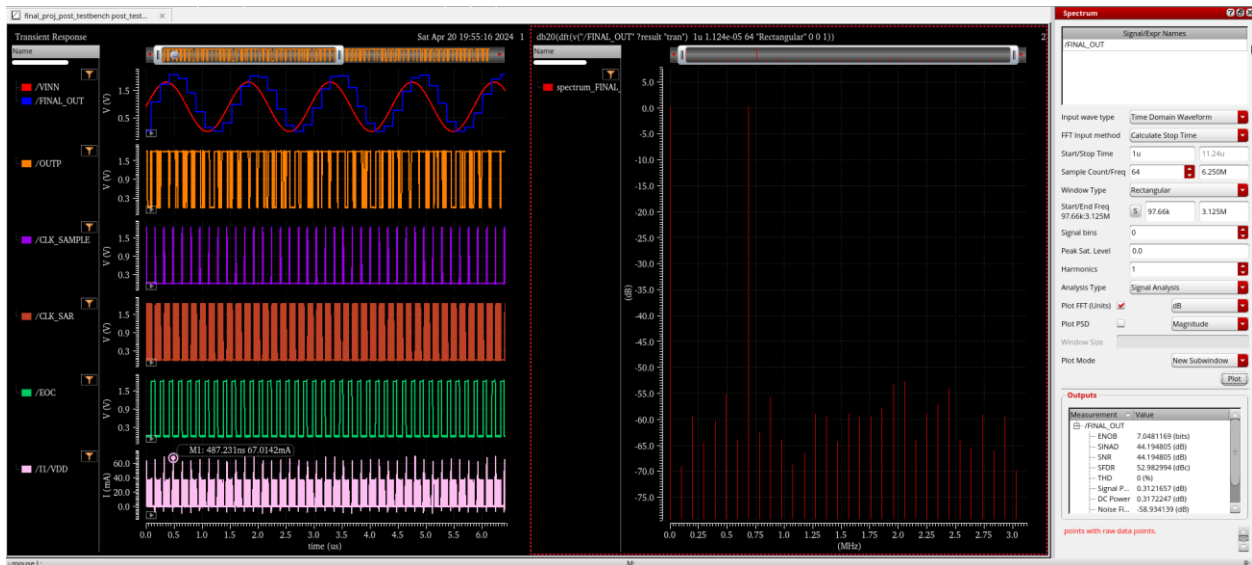
Test Schematic: (final_proj_post_testbench/post_test_with_symbol/schematic)



Before Extraction Simulation:

(final_proj_post_testbench/post_test_with_symbol/test420_Pre_Simu_7.048bit)

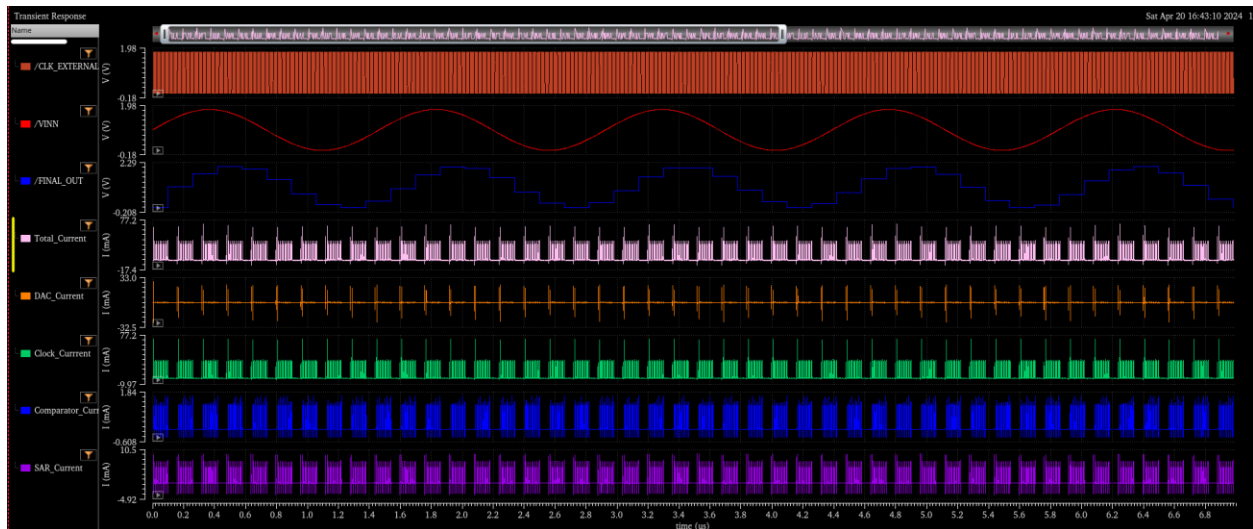
ENOB: 7.048 ENOB



Also, we calculate the Total Power consumption:

(*final_proj_post_testbench/post_test_with_symbol/TOP_LEVEL_POWER*)

According to the Equation $P = UI$, we use the calculate to calculate the average current of total Chips and all 4 components, and then times VDD 1.8V, we can get the All power Consumption and Distribution.



Example of calculating power using Calculator:

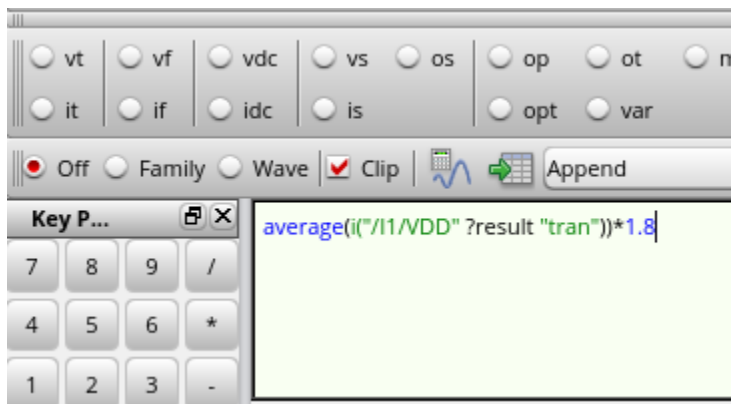
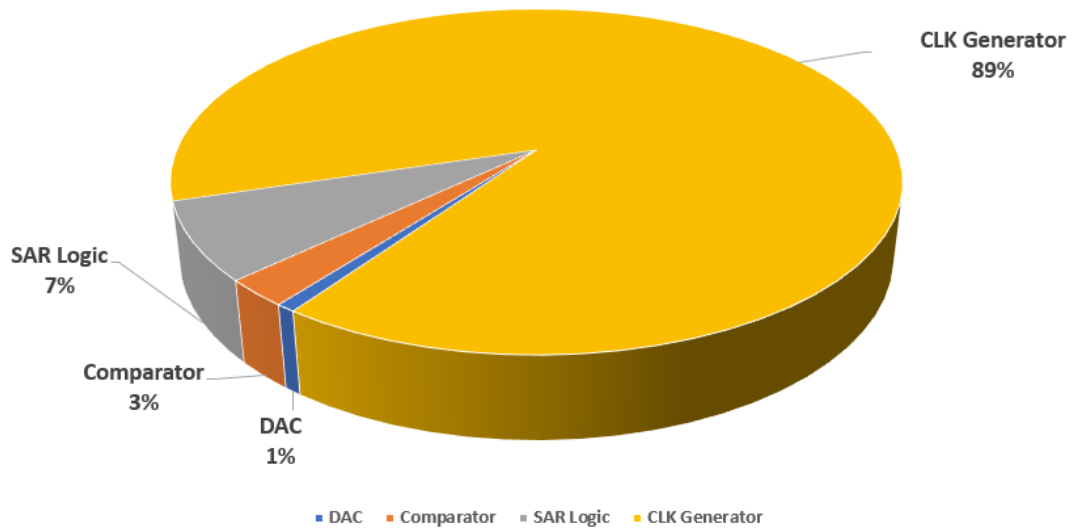


Table and Pi Chart for Power Distribution in Each Blocks:

	TOTAL	DAC	Comparator	SAR Logic	CLK
Current	842.8 μ A	6.318 μ A	21.53 μ A	61.71 μ A	756.3 μ A
Power	1.539mW	11.37 μ W	38.75 μ W	111.1 μ W	1.378 mW

Power Distribution in Each Blocks

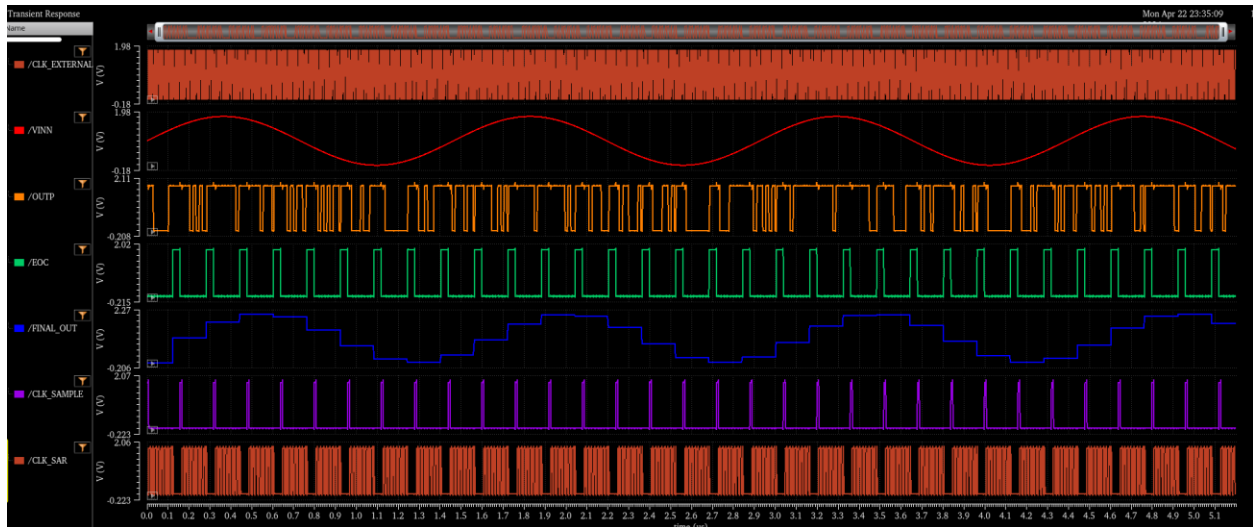


After Extraction Simulation:

(final_proj_post_testbench/post_test_with_symbol/test420_Post_Simu_bit)

We tried to run in Sunday night but the Sever crashed, Now we are running in the Monday evening but cannot finish on time. Right now we can see from the first 5us results:

The final_out signal is basically same as the pre simu ones:



Task Assignment

Tao Liu – Schematic for Sample&Hold, CDAC, SAR Logic, and other small block used in circuits, like TSPC FF... Integrate all circuits as whole,

Layout whole DAC blocks Sample and Hold, DFF, revising on clock generate part. Integrate all blocks including PADS & GardRings

Ding Wang – Schematic for Comparator, simulation for both comparator, Sample&Hold.

Revising on clock generator, DAC circuits and Delay blocks to get the good performance.

Layout SAR, Comparator, TSPC FF, Clock generator. Integrate all blocks including PADS & GardRings

Performance metrics

Parameter	Value
Technology	TSMC 180nm CMOS
Power Supply	1.8 V
Resolution	8 bits
Sampling Rate	6.25 MS/s
Common-Mode Voltage	0.9 V
Sampling Unit Cap	35.6 fF
SINAD	44.19 dB
SFDR	52.98 dB
ENOB	7.05 bits
Total Power	1.539 mW
FOM	1.45 fJ/conversion-step

Where

$$FOM = \frac{P_{total}}{2^{ENOB} * f_s}$$