8-bit asynchronous SAR ADC
Based on 180nm CMOS Technology
Critical Review Report

Team 4

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TA: Jaeung Ko

STEPS to finalization:

This week we finish all the layout and perform the post-simulation for the whole chips. Also, we finalized the structure of ADC to final state. With every block works correctly, before extraction we could get **7.048** bits for ENOB.

Firstly, we finalized the structure of our design, especially the DAC and Clock Generator Blocks. In DAC block, we increased the size of Transmission Gate to make them more stable and have good performance. In Clock Generator part, we modified the different Delay Block, eliminated the capacitors and restructure them with minimum numbers of Delay Blocks.

Then, we made a really neat and compact Layout with all blocks in the center of Gard Rings and Pads. We pour the empty space with strong VDD(M2) and GND(M1). Also, we add 6 additional bypass capacitors to reduce the inductance impacts.

Lastly, we make a symbol for the whole chips, giving them input signals to see the performance of ADC, during which we see the really great performance and also calculate power from it.

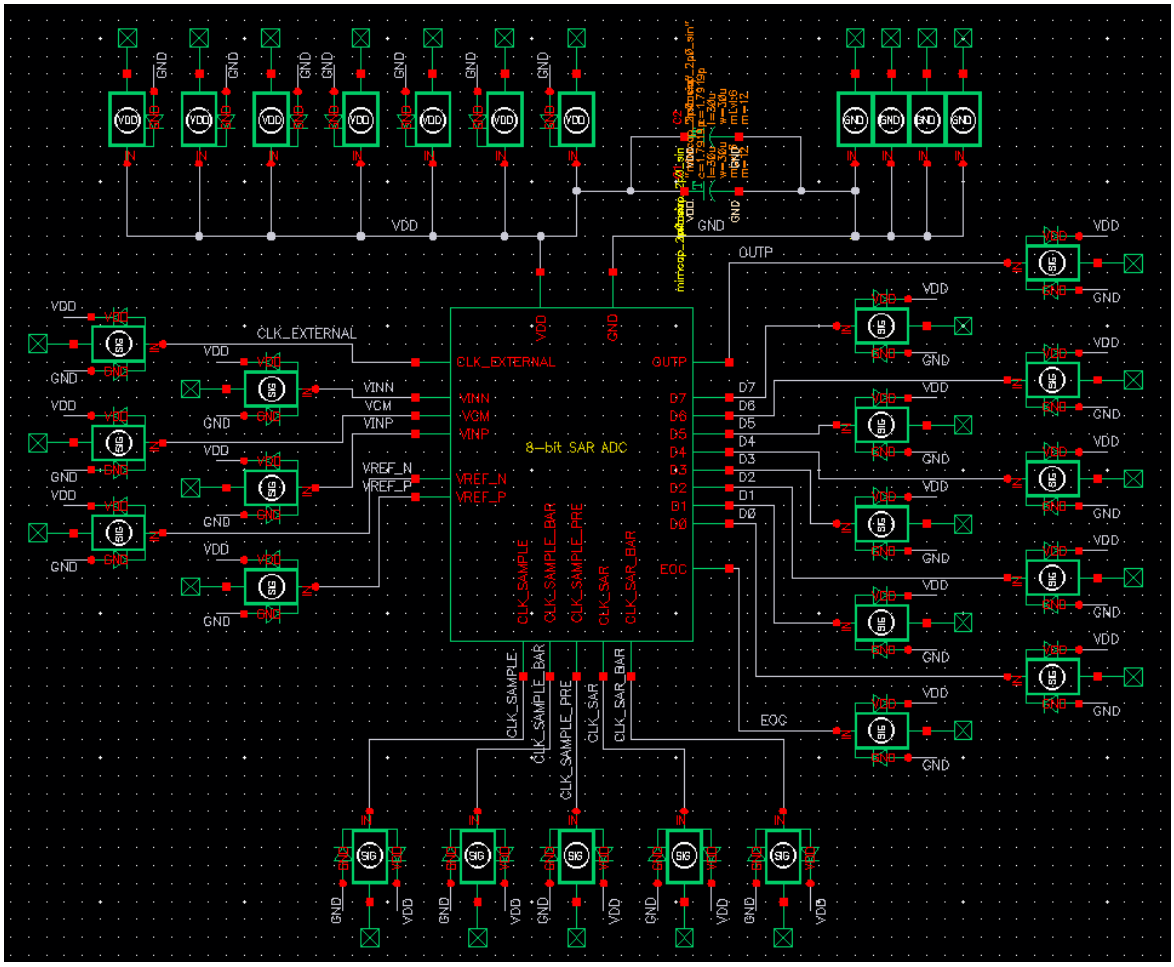
Final layout file of the chip:

/home/home1/chips2024team4/TSMC_180_work

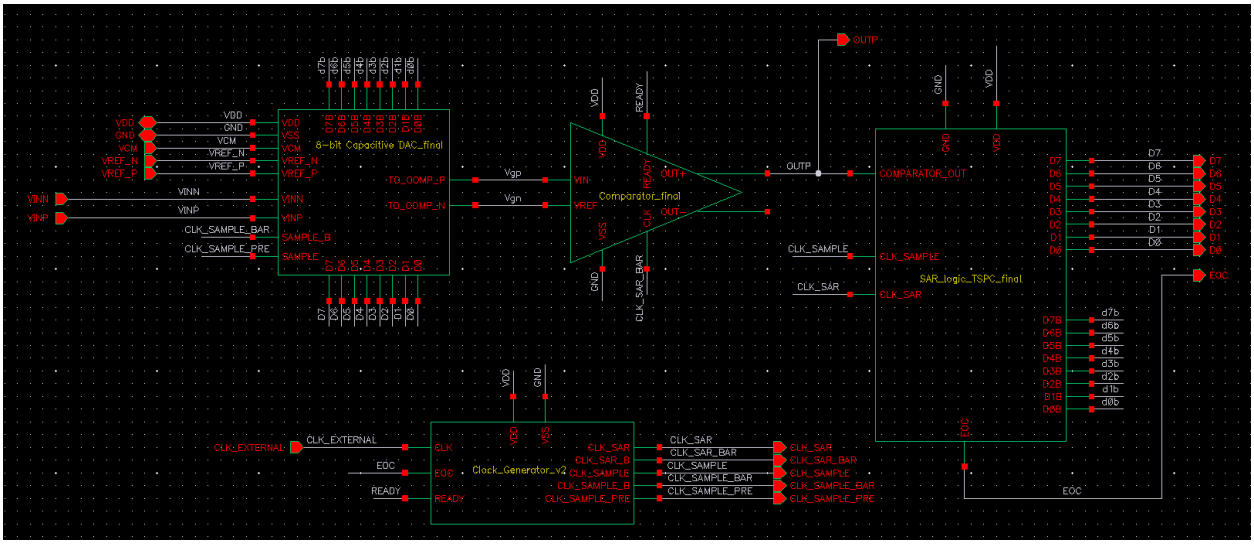
/final_proj_8bit_SAR_ADC/TOP_LEVEL_with_PADS

Detailed System Block:

Top-Level Schematic with PADS



8-bit SAR ADC: ON-Chip Blocks



Our SAR ADC includes 4 PARTS: Capacitor DAC (Sample & Hold Block exists in it), Comparator, SAR Logic, and Clock Generator.

Update from Design Review 2

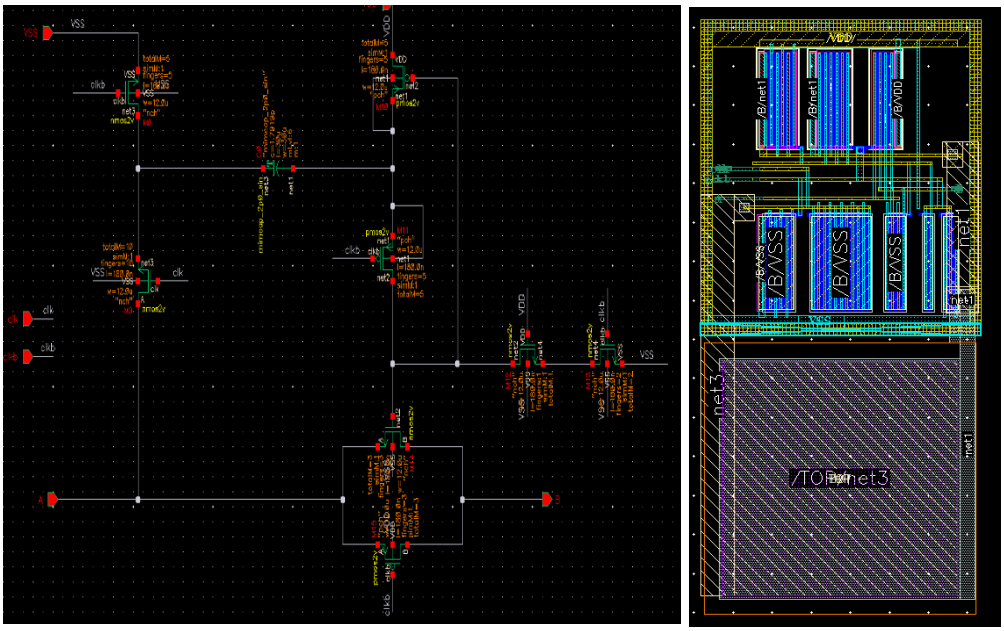
The Main change from Design Review 2 is the Layout. We made the whole layout including Pads and Gard Rings, which gives us the ability to extract the layout to see the post simulations.

Also, we revised the circuits to the best performance as we can, and made a whole symbol for it, so that we could measure the Total Power from our circuits.

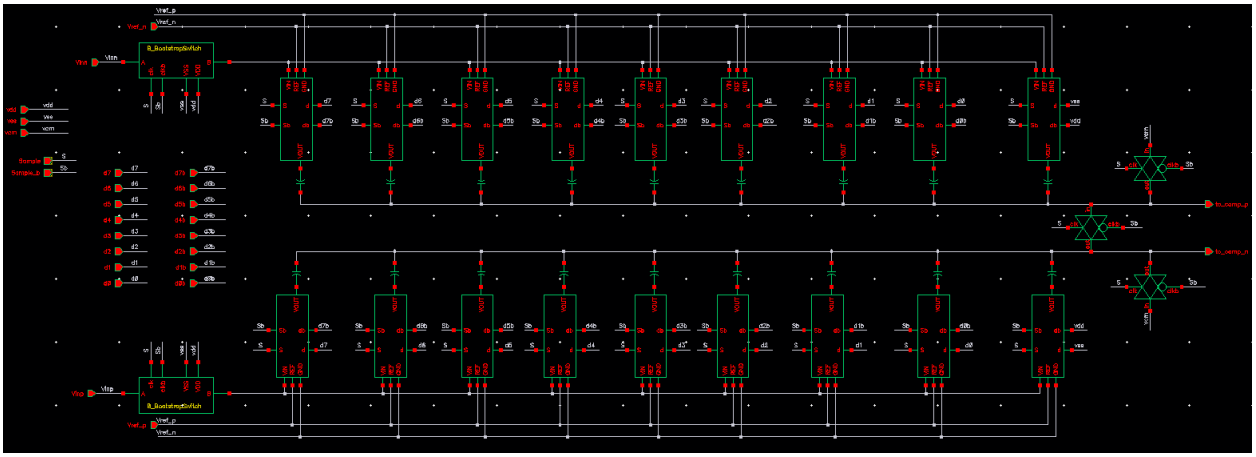
Block And Layout Design

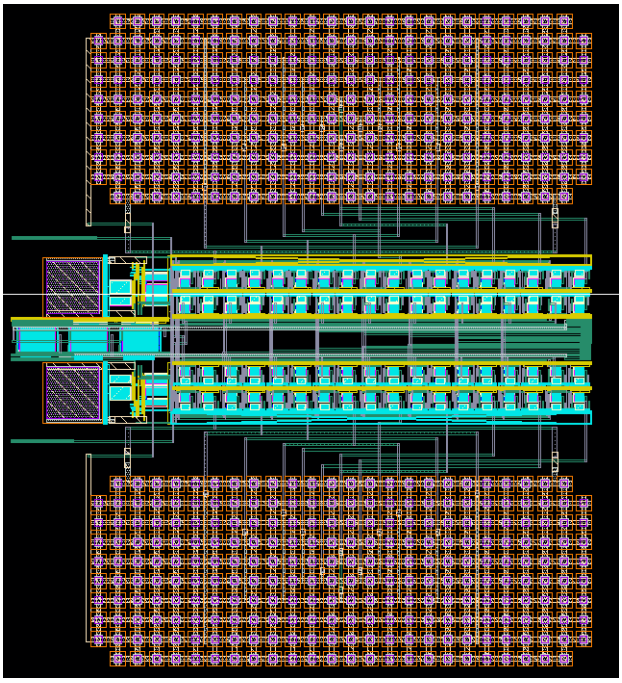
All ROOT file for the simulation & Layout is: ***/home/home1/chips2024team4/TSMC_180_work/***

1. Bootstrapped Sample-And-Hold Circuit ***(final_proj/Sample_Hold_v2)***



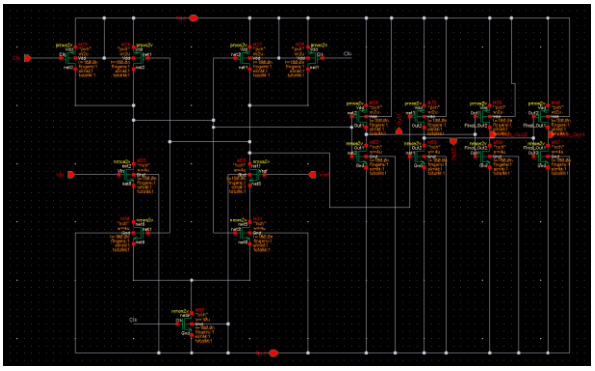
2. Capacitive DAC ***(final_proj_8bit_SAR_ADC/Capacitive_DAC_final)***

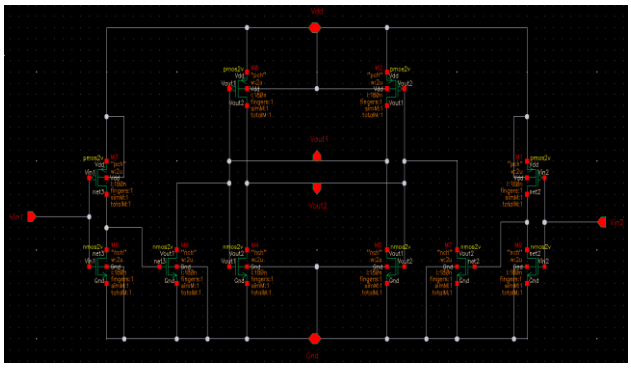


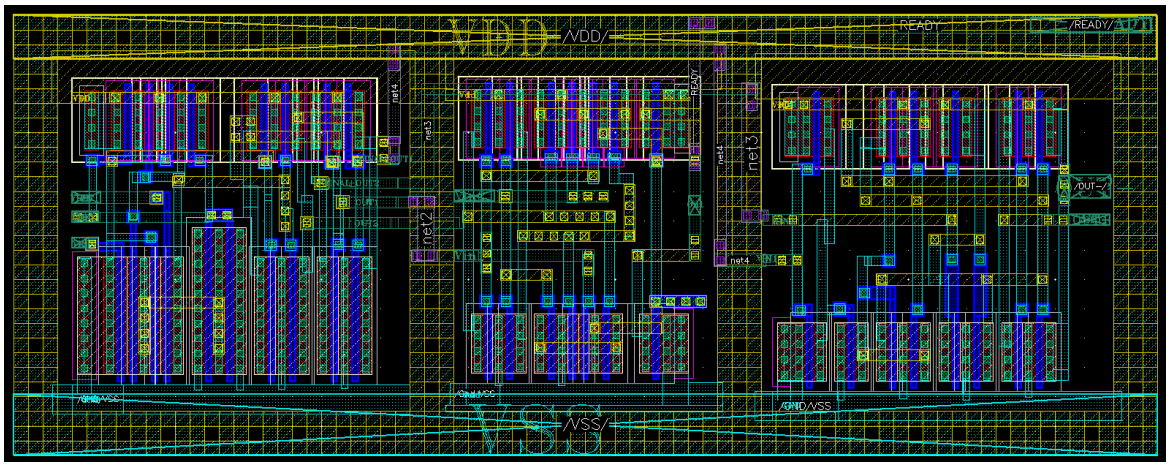


3. Comparator ***(final_proj_8bit_SAR_ADC /Comparator_final)***

schematic&layout for Strong-Arm Comparator & RS Latch

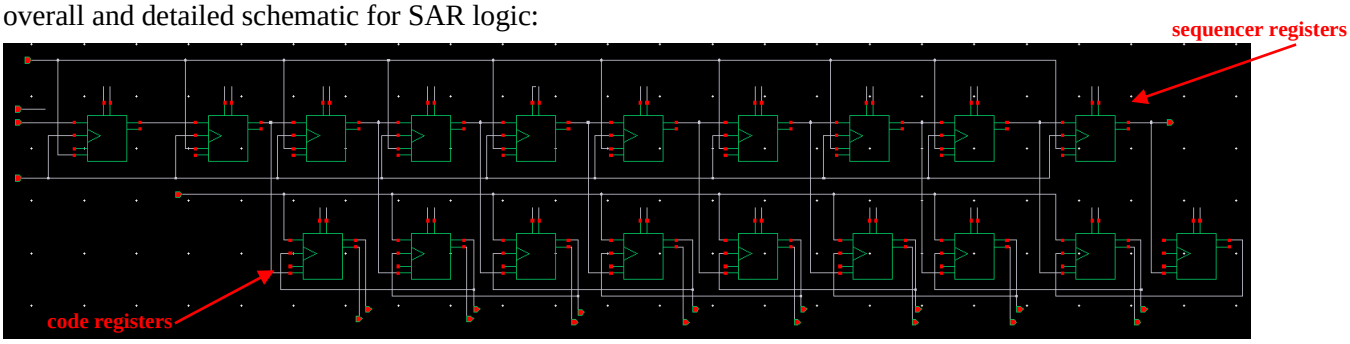


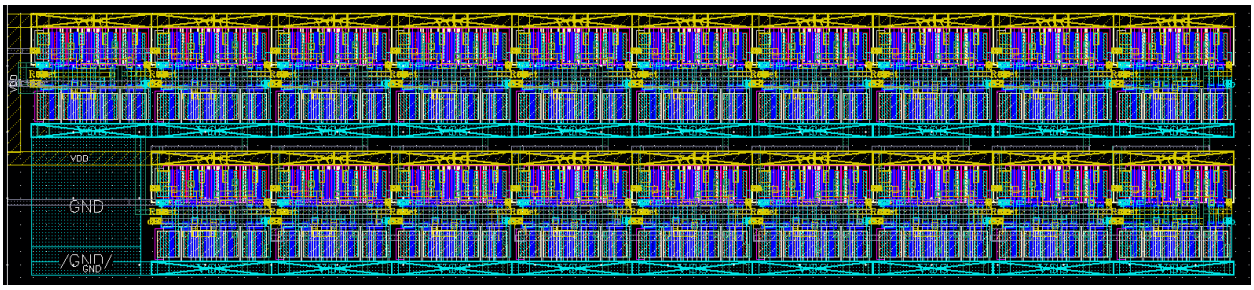




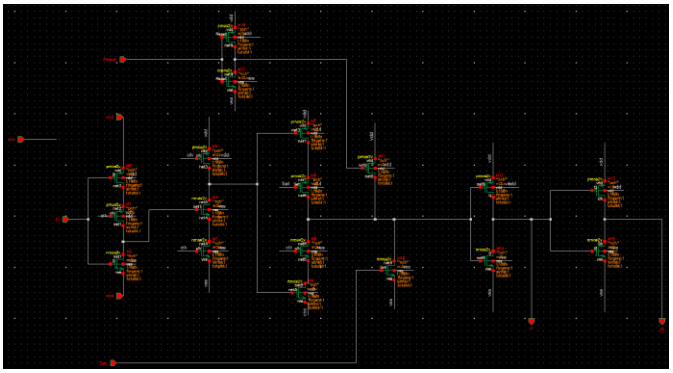
4. SAR Logic Circuit ***(final_proj_8bit_SAR_ADC /SAR_final)***

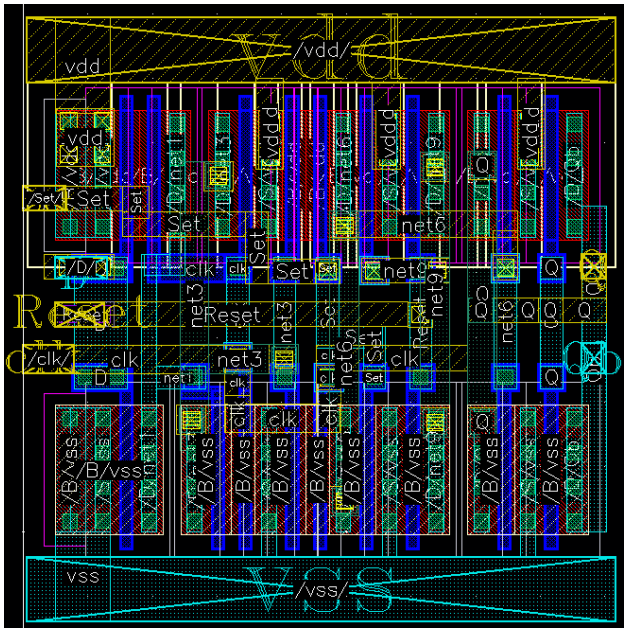
overall and detailed schematic for SAR logic:





Here below are the schematic and symbol for TSPC FF: ***(final_proj_lib /TSPC_ff)***

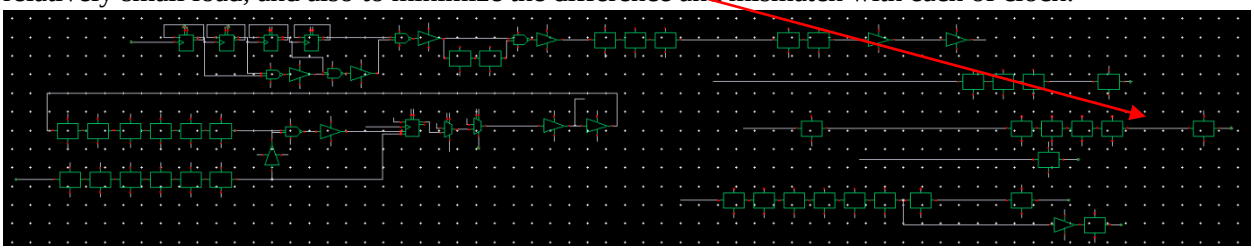




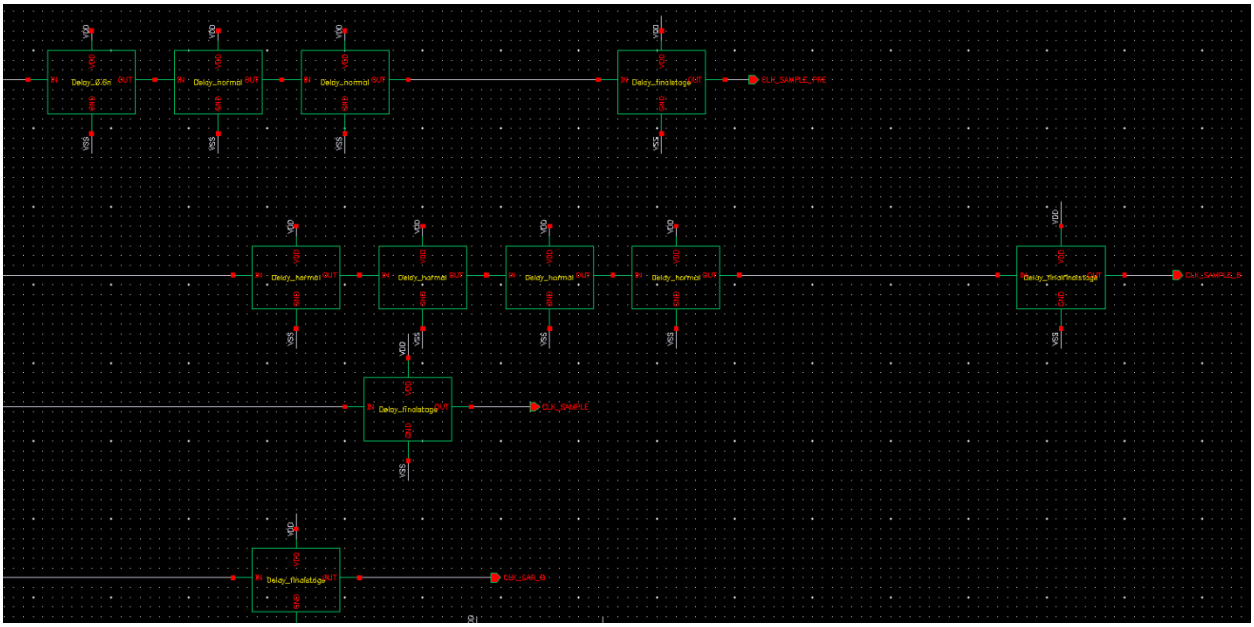
5. Clock Signal ***(final_proj_8bit_SAR_ADC /Clock_asyn_final)***

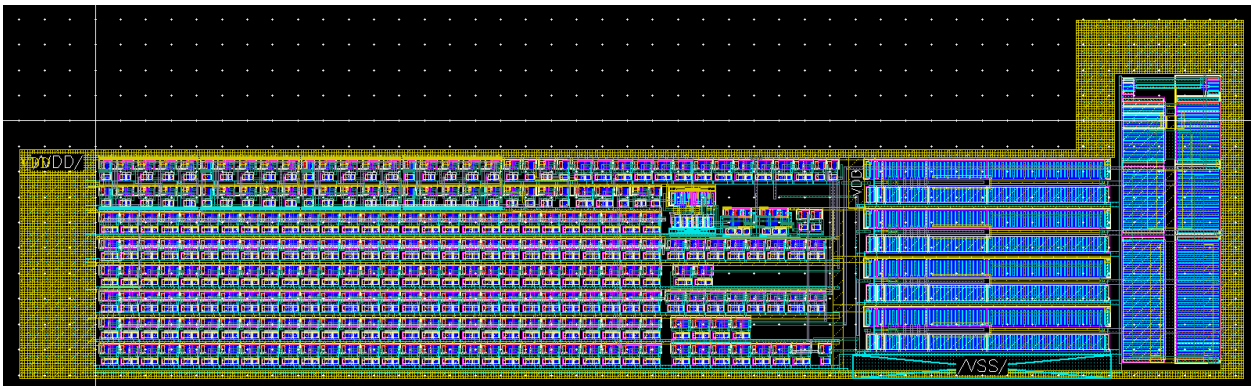
As for **Asynchronous** ADC, each block will apply different Clock Signal with certain delay and different frequency. We build the Clock with this schematic:

The input is a 100MHz clock. With this clock, we utilize 4 D Flip-Flops (DFF) to generate the sample clock with a 10ns sample time and a 150ns hold time. The reason for allocating a significant hold time is to ensure sufficient time for the SAR clock to iterate 8 times, generating 8 digital bits within one external clock cycle. Following the logic, we apply different buffer blocks to drive the clock signal with a relatively small load, and also to minimize the difference and mismatch with each of clock.

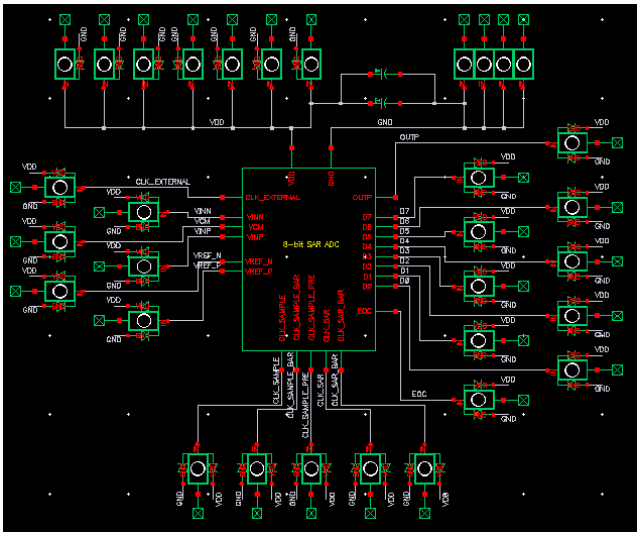


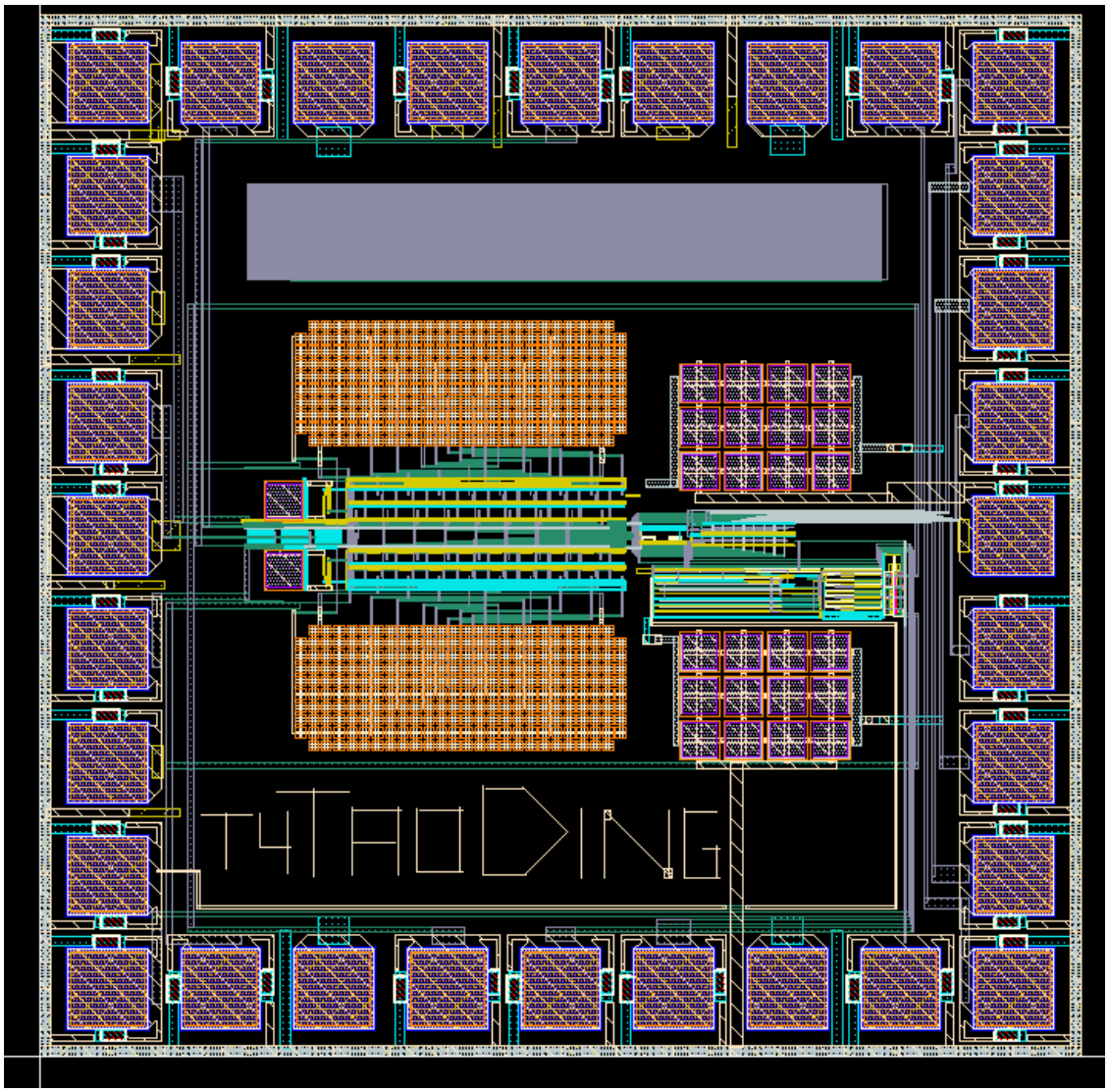
In detail, we design lots of delay block to generate the dedicated delay time to satisfy our needs.



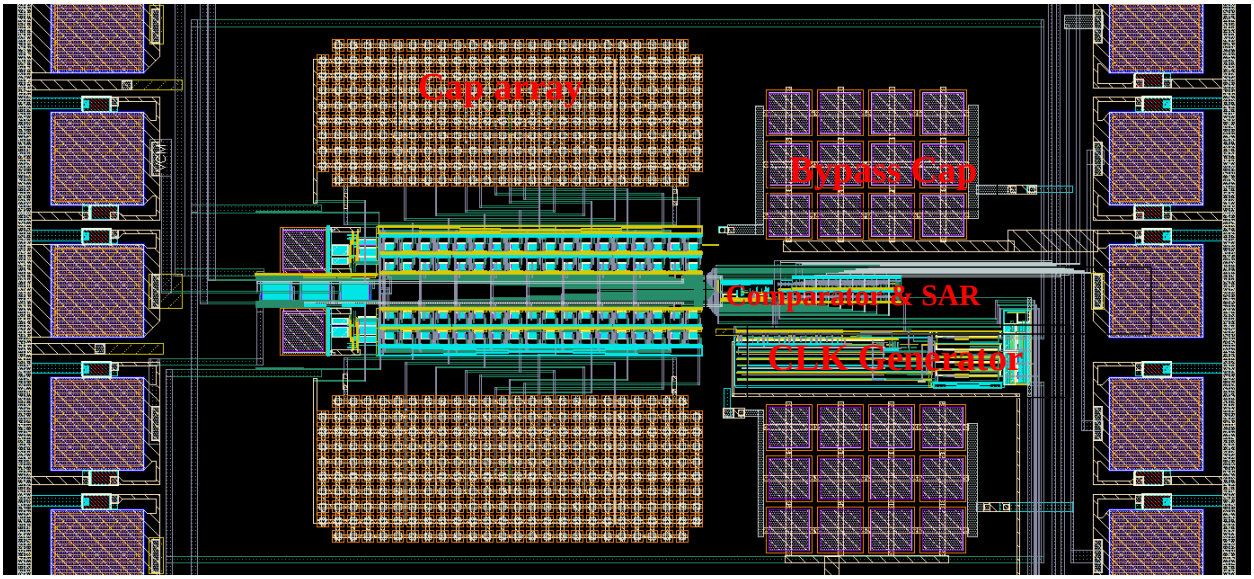


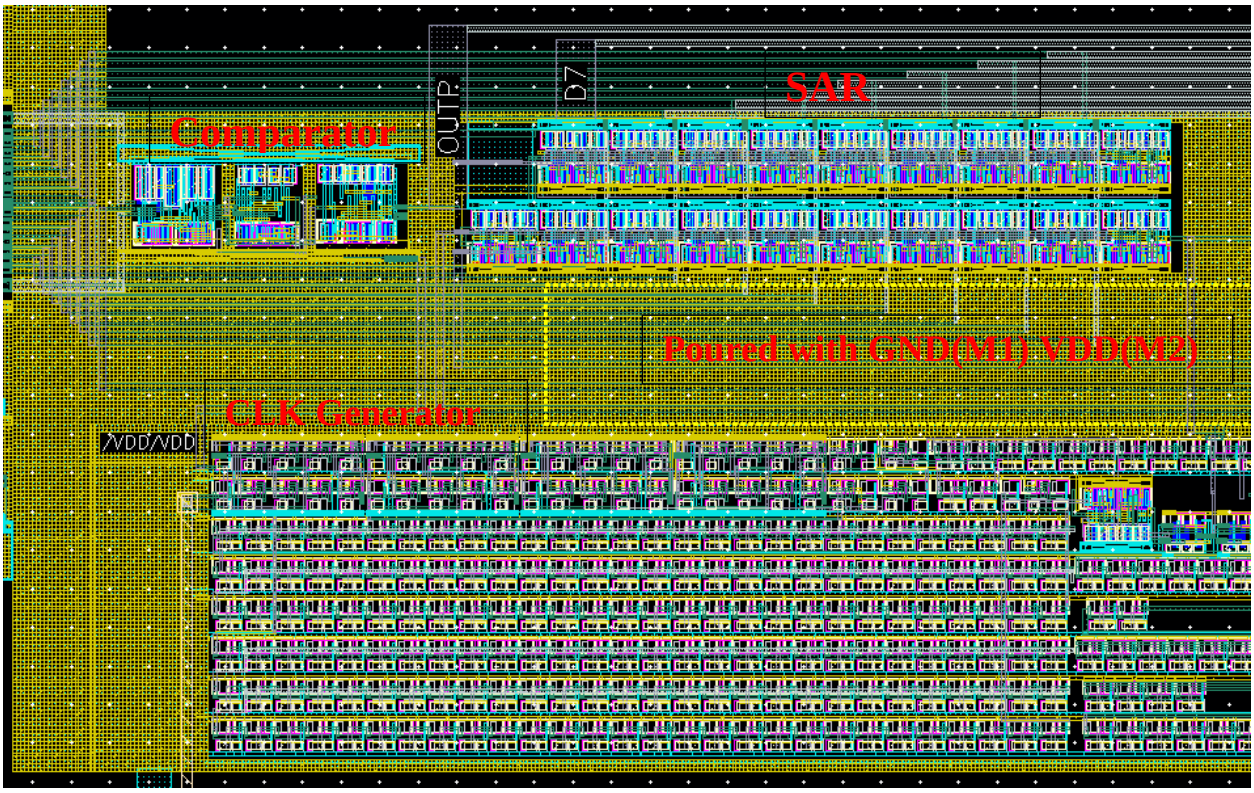
*6. Final Chip Layout(**final_proj_8bit_SAR_ADC/TOP_LEVEL_with_PADS**)*





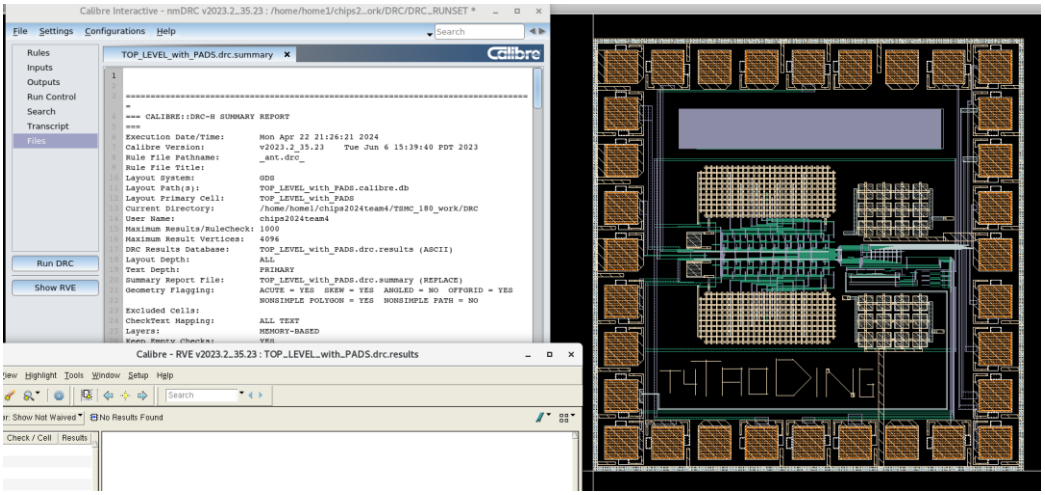
Detailed:



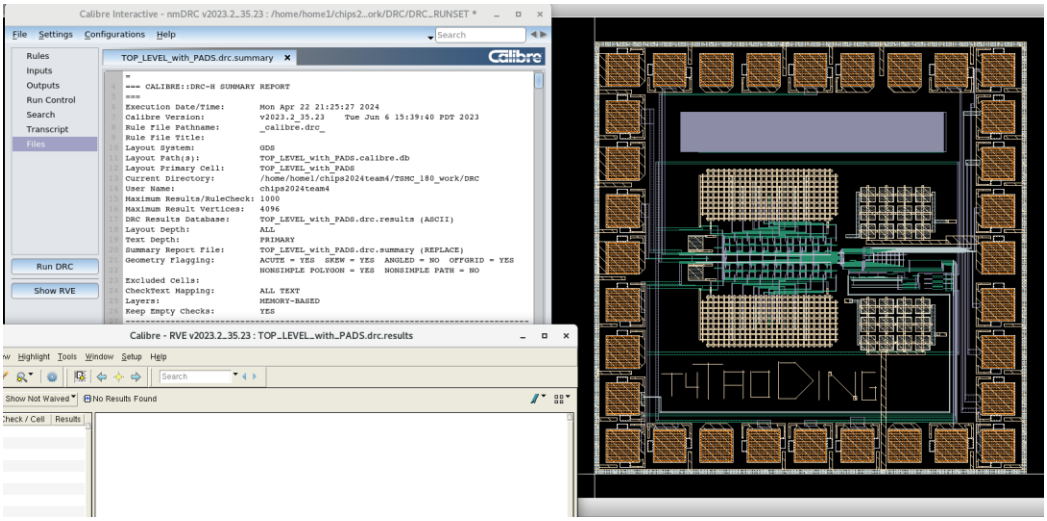


Passing ALL DRC & LVS:

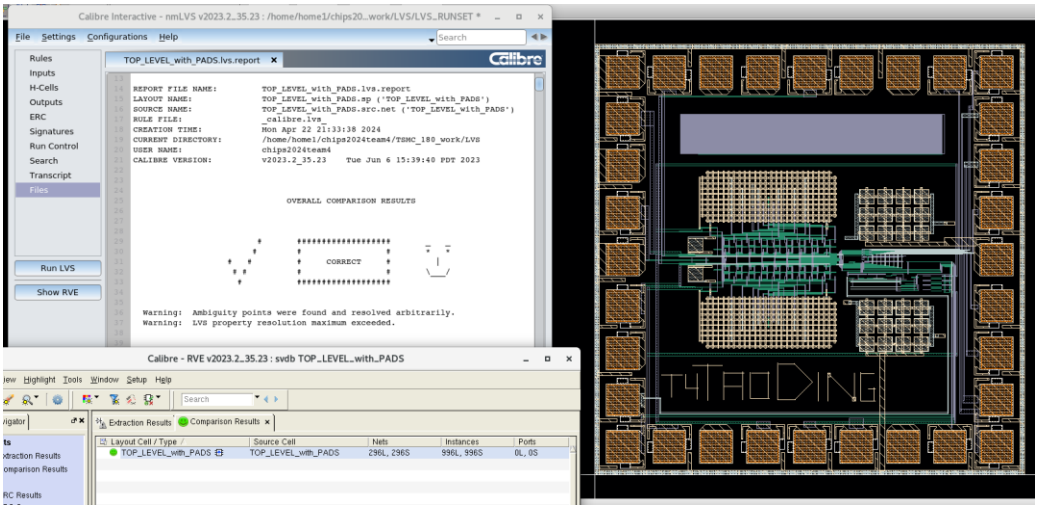
ANT_DRC:



Calibre_DRC:

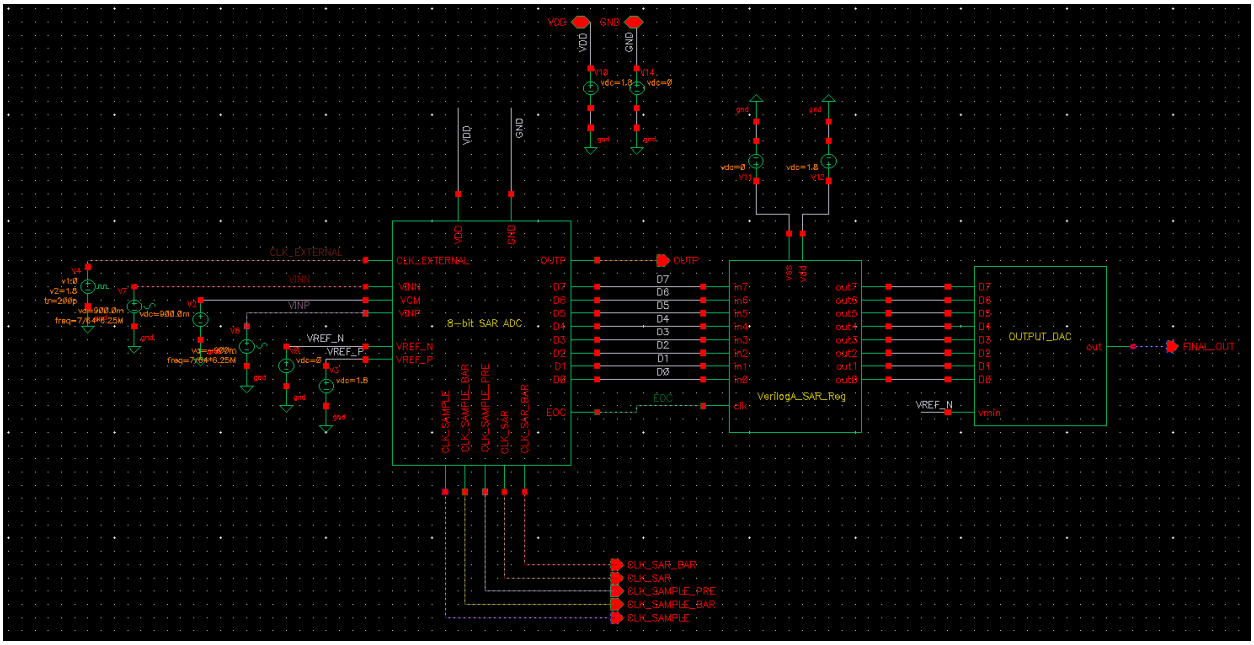


LVS:



Simulation Results

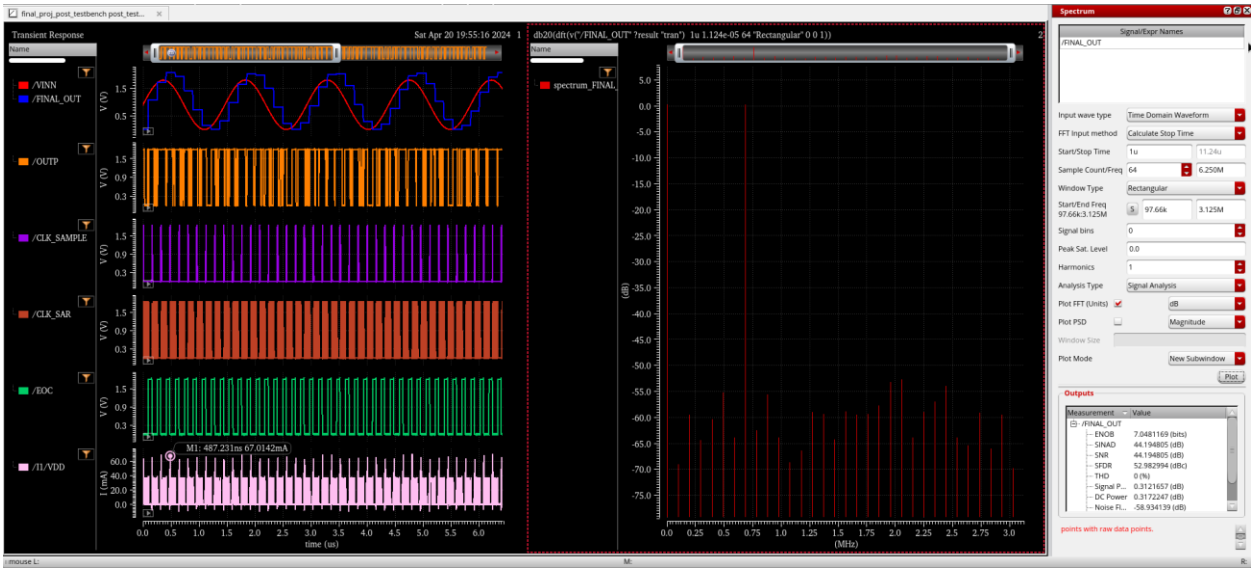
Test Schematic: ***(final_proj_post_testbench/post_test_with_symbol/schematic)***



Before Extraction Simulation:

(final_proj_post_testbench/post_test_with_symbol/test420_Pre_Simu_7.048bit)

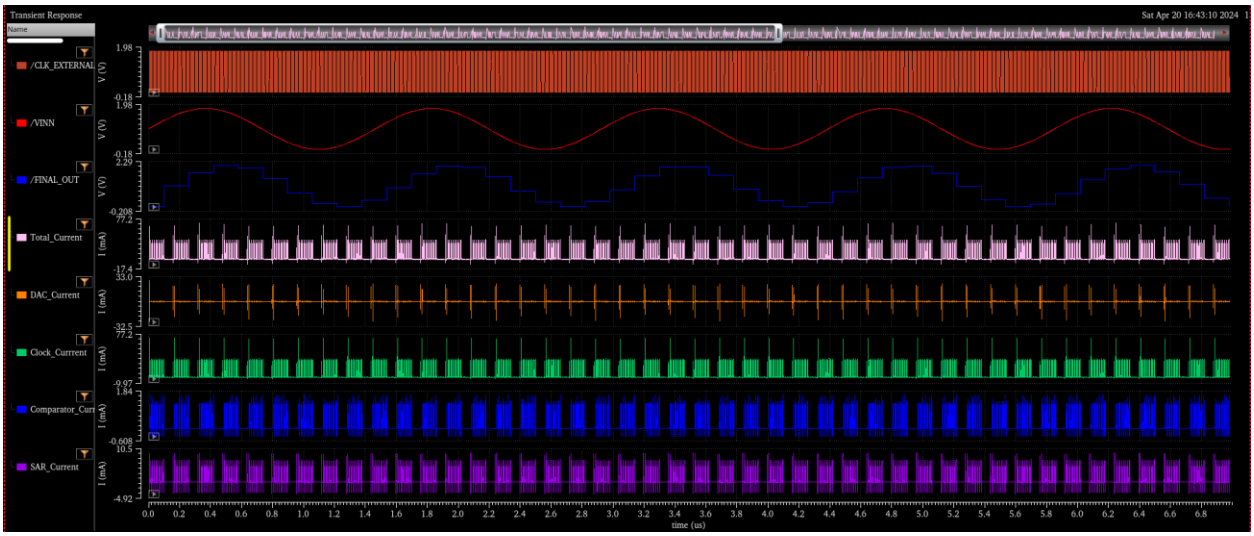
ENOB: ***7.048 ENOB***



Also, we calculate the *Total Power consumption*:

(final_proj_post_testbench/post_test_with_symbol/TOP_LEVEL_POWER)

According to the Equation P = UI, we use the calculate to calculate the average current of total Chips and all 4 components, and then times VDD 1.8V, we can get the All power Consumption and Distribution.



Example of calculating power using Calculator:

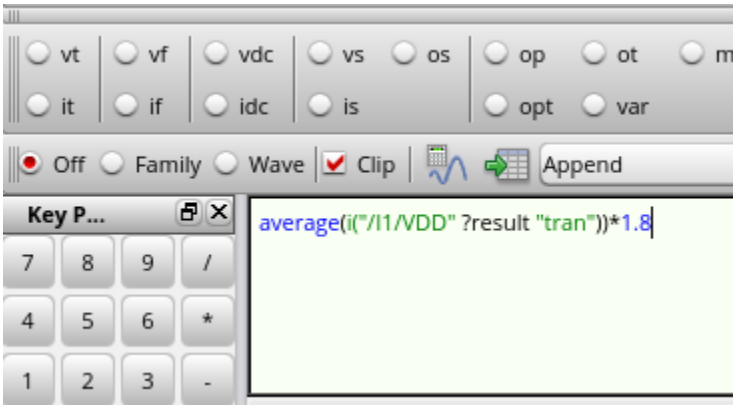
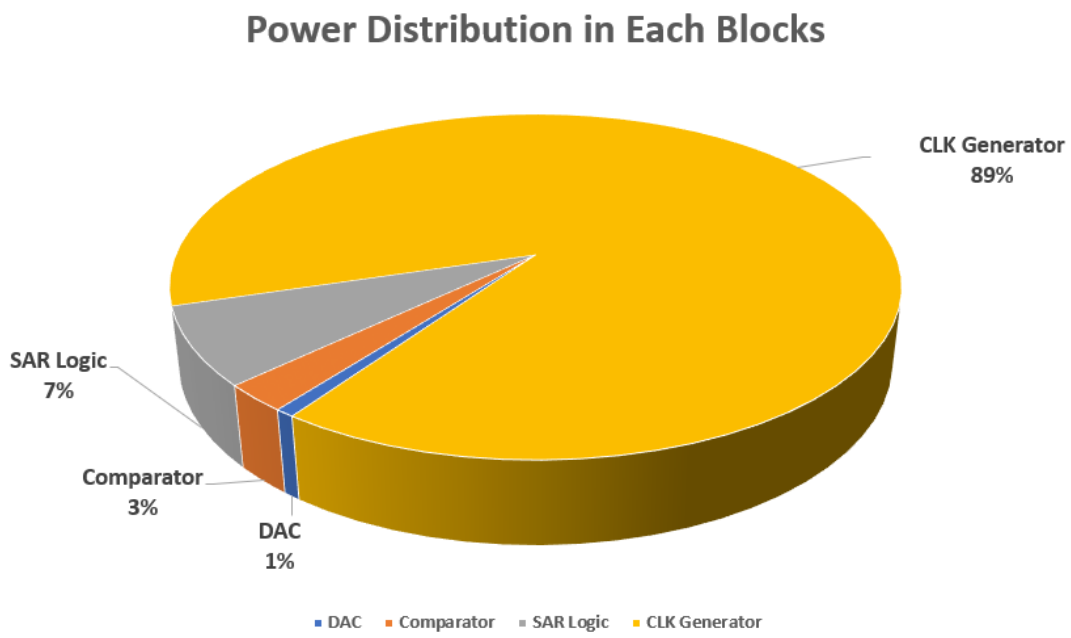


Table and Pi Chart for Power Distribution in Each Blocks:

	TOTAL	DAC	Comparator	SAR Logic	CLK
Current	842.8μA	6.318 μA	21.53 μA	61.71 μA	756.3 μA
Power	**1.539*mW***	11.37 μW	38.75 μW	111.1 μW	1.378 mW

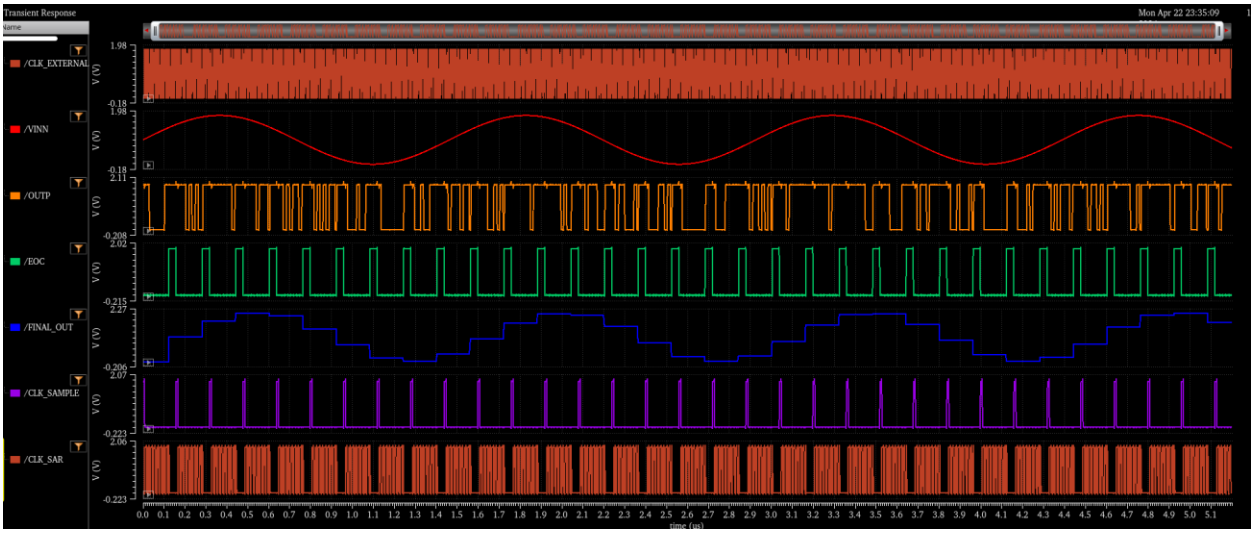


After Extraction Simulation:

(final_proj_post_testbench/post_test_with_symbol/test420_Post_Simu_bit)

We tried to run in Sunday night but the Sever crashed, Now we are running in the Monday evening but cannot finish on time. Right now we can see from the first 5us results:

The ***final_out*** signal is basically same as the pre simu ones:



Task Assignment

Tao Liu – Schematic for Sample&Hold, CDAC, SAR Logic, and other small block used in circuits, like TSPC FF… Integrate all circuits as whole,

Layout whole DAC blocks Sample and Hold, DFF, revising on clock generate part. Integrate all blocks including PADS & GardRings

Ding Wang – Schematic for Comparator, simulation for both comparator, Sample&Hold.

Revising on clock generator, DAC circuits and Delay blocks to get the good performance.

Layout SAR, Comparator, TSPC FF, Clock generator. Integrate all blocks including PADS & GardRings

Performance metrics

Parameter	Value
Technology	TSMC 180nm CMOS
Power Supply	1.8 V
Resolution	8 bits
Sampling Rate	6.25 MS/s
Common-Mode Voltage	0.9 V
Sampling Unit Cap	35.6 fF
SINAD	44.19 dB
SFDR	52.98 dB
ENOB	7.05 bits
Total Power	**1.539 mW**
FOM	**1.45 fJ/conversion-step**

Where

$$\boldsymbol{FOM} = \frac{P_{total}}{2^{ENOB} * f_s}$$