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GENERAL INFORMATION REGARDING ONLINE SUBMISSION:

- Design a simple (**N**) bit RISC Single Cycle processor [**N**= number of bits designated to individual].
- A group should have at best 2 members.
- Projects must be submitted along with a **project report** (listing contributions of each group member).
- Plagiarism will be heavily penalized.** Any reproduction of original materials needs to be **properly referenced**.
- The submission of the project will be taken through Google Classroom portal. **Each group member will have to submit the project individually confirming the group members have the same project file.** Mention your group members' identities inside the simulation file also. Keep an eye on the lab course web page link for further instructions.

Project Report should include the following sections:

- An Introduction of the **N** bit RISC Processor.
- Table of Different types of Formant [Register Type, or **R-Type**, Immediate Type or **I-Type**, Target Type or **J-Type**]
- Detailed Description of Each unit [Register files, ALU, & Control Unit]
- Respective state table for Control Unit.
- Detailed Description with figures and screenshots of each sub-circuits designed inside the simulation file.
- Discussion of task and steps to achieve it with a Conclusion of project outcome.

Project Requirements:

- How Many Functions/Micro Operations/Commands? (**opcode**): This will be assigned to individual group respectively.
- Register File:** How Many Registers? : In terms of total bit size assigned to an individual group the RISC Processor the Data bits will be the same **N** bits for all the registers and number of register will be equal to 2^n bits here n = The Address of Each Register you have assigned in the Format of {**RS, RT RD**}.
- ALU:** ALU Opcode bits will be same for every group: 2 bits. Everyone should have an Adder and a Subtractor unit common. And in terms of assigned Instructions in groups new components like [Shifter, Mul, Div unit] can be added later in 1 BIT ALU.
- Everyone must include Branching mechanism in the Datapath perfectly to obtain full grades.
- For Branch instruction execution, you need the **Zero Signal** and a Control signal from the Control unit for a branch type Instructions. [beq, bne]

LIST of Instructions (will be split among groups):

R-Type: add, sub, and, or, nor, xor, mul, div, sll, srl

I-Type: addi, subi, lw, sw, ori, nori, muli, divi, beq, bne

*** Among these instructions, **4 Instructions will be common** [LW, SW, ADD, SUB] for every groups and **new 4 instructions** will be assigned to each group (Individual group task will be assigned inside the Google Sheet link that is being followed for course grading) ****

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