



Lab Manual

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Experiment No: 08

Experiment Name: Build a pipelined datapath

Introduction:

In single cycle datapath, the datapath components execute an instruction concurrently, in one cycle. As a result, no datapath component can be used more than once per cycle. Here, we will use the single-cycle datapath components to create a multi-cycle (pipelined) datapath, where each step in the fetch-decode-execute sequence takes one cycle. In multicycle particularly in Pipelined datapath each functional unit (e.g., Register File, Data Memory, ALU) can be used more than once in the course of executing an instruction, which saves hardware (and, thus, reduces cost); and

Objective:

We will have following objectives to fulfill:

- 1) Build a pipelined datapath

Experiment Details:

Assume, a 16 bit ISA with following fields. The formats of the instruction are as follows:

R-type

op (4 bit)	rs (4 bit)	rt (4 bit)	rd (4 bit)
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I-type

op (4 bit)	rs (4 bit)	rt (4 bit)	immediate (4 bit)
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J-type

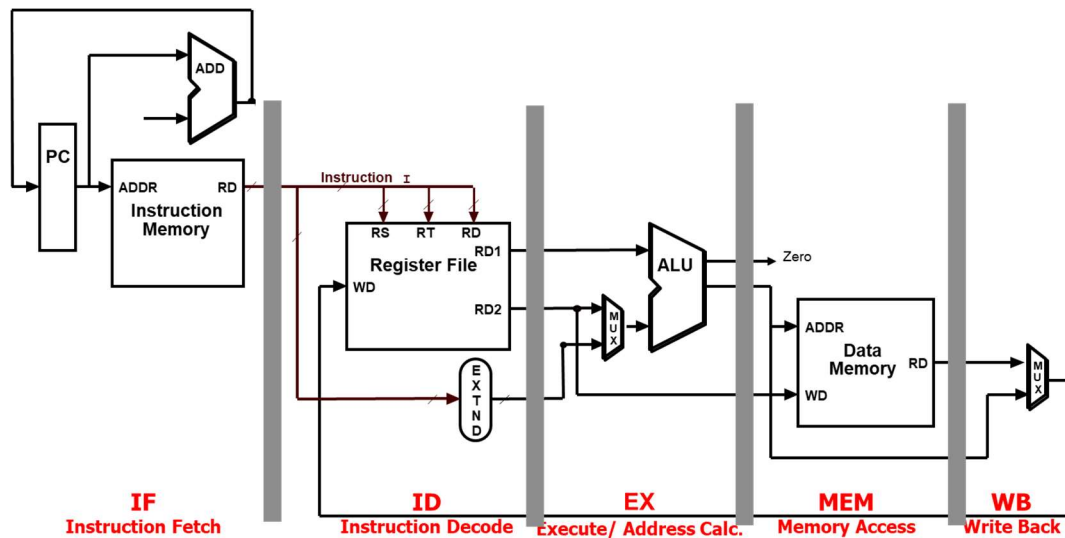
op (4 bit)	Target (12 bit)
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Equipment/Tool

Logisim Tool

Pipelined Datapath:

Following is the schematic diagram of the complete single cycle datapath with pipeline registers inserted in between the stages.



Task Lists

1. How many pipeline stages has been created into the above diagram, Identify
2. Determine the name of the pipeline registers from the diagram.
3. Calculate the width of each of the pipelined registers and show the breakdown of the calculations
4. Build a pipelined datapath by implementing the above diagram.
5. There will be an issue into the pipelined datapath if the write register address is directly sent to the *Write Register* port of Register file gets signal from the *Instruction* port of Instruction Memory as can be seen in the above diagram. Solve this issue.

Assignment:

- 1) Prepare the lab report.
- 2) Take a screenshot of your implementation and later include it in your lab report.