

Department of Computer Science & Engineering
Swami Vivekananda Institute of Science & Technology

Dakshin Gobindapur. P.S.: Sonarpur
Kolkata – 700 145.



*Reversible Priority Encoder using
Quantum-Dot Cellular Automata (QCA)*

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Supervisor Name: **BIKASH DEBNATH**

Submitted by Roll NO:	Regn. No.:	Name
24100114026	142410110026	Don Sarkar
24100114035	142410110035	Paramesh Chakraborty
24100114038	142410110038	Raju Dutta
24100114044	142410110044	Saurav Sarkar
24100114054	142410110054	Tapas Dey
24100115058	152410120002	Krishnendu Halder

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ABSTRACT:

An Encoder is an important component of memory, for address decoding and encoding. The size of Complementary Metal Oxide Semiconductor (CMOS) transistor keeps shrinking to increase the density on chip in accordance with Moore's Law. The scaling affects the device performance due to constraints like heat dissipation and power consumption. A Quantum dot Cellular Automata (QCA) is an alternative to CMOS. Quantum Cellular dot Automata offers higher speed, lower power consumption and higher density. In non-reversible gates some amount of power loss is involved. Interest in reversible logic offers reduced heat dissipation and increases the speed. It is a new transistor-less computation in nanotechnology. In this project propose a reversible gate based encoder architecture. It provides reversibility and area minimization. QCA designer tool has been used to validate the performance of reversible encoders.

Keywords:

- Quantum Cellular Automata (QCA)
- Majority Logic
- QCA Designer
- Reversible Gate
- Reversible Priority Encoder

Objective:

The objectives of this project listed down below:

- To understand the Quantum Cellular Automation technique
- To evaluate the advantages of using Nanotechnology in terms of power consumption of MOSFET circuits
- To understand the methodology and working principal of Majority Gates
- To understand the working principal of Reversible gates using QCA
- Present the proposed model which can be implemented using this technology

Resource Requirement:

- Hardware: Simple 4-bit processor
- Software: QCADesigner tool

1. Introduction:

The increasing demand for low-power very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits. This is because all the important parameters governing power dissipation—switching capacitance, transition activity, and short-circuit currents—are strongly influenced by the chosen logic style. Depending on the application, the kind of circuit to be implemented, and the design technique used, different performance aspects become important, disallowing the formulation of universal rules for optimal logic styles. Investigations of low-power logic styles reported in the literature so far, however, have mainly focused on particular logic cells, namely full-adders, used in some arithmetic circuits. VLSI fabrication process keep on shrinking the physical sizes down to atomic scale dimensions and the operational frequencies of terahertz can be easily obtained if the devices can operate with less no. of electrons. However, there is a need for a trade-off to be made between increasing requirements of performance parameters and the feature size. The eventual saturation of CMOS technology is not due to inability to reduce its physical size further, but the detrimental effects of quantum mechanical effects on tiny transistors. for e.g., In Nano scale transistors, impermissible amounts of current leaks due to such highly narrow channels and ultra-thin insulating layers. Nanotechnology is one of the possible alternatives to the stated trade off problem. ITRS report summarized several possible solutions. The possible variants are i) Deltt (double–electron-layer tunneling transistor) developed by scholars at SN labs, ii) SET (single electron transistors) iii) rapid single quantum flux logic, iv) quantum cellular automata. SET's are a promising technology for non-volatile memory. To the best of our knowledge, the concurrent testing of faults in QCA and QCA-based sequential circuits has not been addressed in the literature. In this paper, we propose novel designs for concurrently testable latches for molecular QCA using conservative reversible logic. Reversible computation in a system can be performed only when the system comprises reversible gates. Reversible circuits do not lose information, and can generate unique output vector from each input vector and vice versa (i.e., there is a one-to-one mapping between the input and the output vectors). Landauer has shown that for irreversible logic computations, each bit of information lost generates $kT \ln 2$ joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which the computation is performed. Bennett showed that $kT \ln 2$ energy dissipation would not occur if a computation is carried out in a reversible way. In this paper an effective approach to analysis and design of priority encoder with reversible NAND gate using quantum dot cellular automata is explored in Nano scale. This paper we use the majority gates is the fundamental component of the QCA circuit implementation. The proposed encoder circuit is designed and simulated using quantum dot cellular automata designer tool and also this simulator tool is more useful for building a complex priority encoder input levels. The proposed structure of encoder required only less number of majority gate functions compared to previous structures.

2. Overview of QCA:

Quantum-dot cellular automata (QCA) is an emerging nan electronic technology that offers a revolutionary approach to computing at nano level . A very extensive research and development in the field device technology for the past several decades made it possible for designers and processing engineers rapidly and consistently reduce semiconductor device size and operating current. But the incessant development in device fabrication on the nanometer scale is limited not only by process technology, but also by fundamental problems arising from scaling, such as quantum-mechanical effects and severe power dissipation. In MOS devices the gate tunneling current increases with the future size going down to deep submicron device geometry process. As a result the device and circuit characteristics drastically are deviated from the designer's expectations of making it better suited from application point of view. Further, in several studies it is predicted that these device technologies are

approaching to its physical limits . Any physical phenomenon that has two separate states can be used to express a logic variable in two valid logic states such as electronic spin. Quantum effect is preferred to utilize in representing logic rather than any other method. Quantum logic devices are presented under this consideration and one of these is known as Quantum-dot Cellular Automata . QCA is an emerging paradigm which allows operating frequencies in the range of THz and device integration densities about 900 times than the current end of CMOS scaling limits. It has been predicted as one of the future nanotechnologies in Semiconductor Industries Association's International Technology Roadmap for Semiconductors (ITRS) . QCA based circuits have an advantage of high speed, high integrity and low power consumption . Also QCA circuits have an advantage of high parallel processing . Recent work showed that QCA can achieve high density, fast switching speed, and room temperature operation . In recent years various QCA based combinational circuit designs have been proposed but comparatively less study efforts have been made with its application in the field of communication. We present here different layouts of QCA based XOR structures that can be used in design and development of specific communication circuits, like parity generators & checkers, error detection & correction circuits and LFSRs. These designs are efficient in terms of cell count, complexity and latency as compared to the already proposed designs. These designs follow the conventional design approach but due to the technology differences, they are modified for the best performance in QCA.

In this paper we propose the seven novel implementations of the QCA based XOR gate and presented the simulation results of these individual designs. A detail comparison with regard to various characteristics of these designs is also presented. The paper has been organized in five sections. The first and second section provides the necessary introduction and review of QCA fundamentals. The third section presents the conventional XOR implementation. The various novel QCA XOR topologies have been presented in the fourth section.

2.1. Basic QCA Cell

A QCA cell is a structure comprised of four quantum-dots arranged in a square pattern as shown in Figure 1. These quantum-dots are sites in which electrons are able to tunnel between them but cannot leave the cell.

QCA information processing is based on the Coulombic interactions between many identical QCA cells. Each QCA cell is constructed using four electronic sites or dots coupled through quantum mechanical tunneling barriers. The electronic sites represent locations that a mobile electron can occupy. The cells contain two mobile electrons (or holes) which repel each other as a result of their mutual Coulombic interaction, and, in the ground state, tend to occupy the diagonal sites of the cell. Therefore the cell has two degenerate ground states. These lead to two polarizations of a QCA cell, denoted as $P = +1$ and $P = -1$ respectively. Binary information can be encoded in the polarization of electrons in each QCA cell. Thus, logic 0 and logic 1 are encoded in polarization $P = -1$ and $P = +1$ respectively. Figure 1 also shows the two possible polarizations of a QCA cell. Binary computation requires interaction among bits, in these devices, among the cells. When a second cell is placed near the first cell, the Coulomb interaction between the cells removes the degeneracy and determines the ground state of the first cell. The interaction between the QCA cells is nonlinear that is with a small perturbation from a neighboring cell clicks it into essentially aligned configuration either with $P = +1$ or $P = -1$ as will be the appropriate.

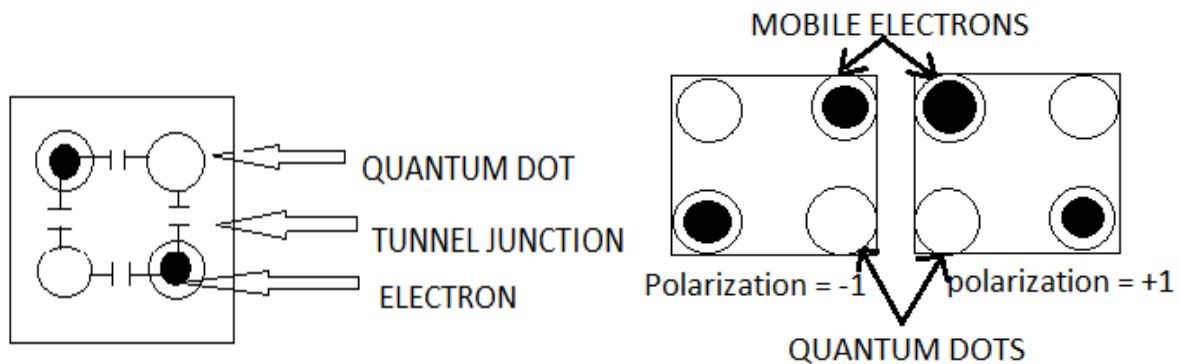


Figure 1. QCA cell and polarizations of QCA cell.

2.2. QCA Wires

In a QCA wire, the binary signal propagates from input to output because of the electrostatic interactions between cells. The propagation in a 90° QCA wire is shown in Figure 2(a). Other than the 90° QCA wire, a 45° QCA wire can also be used as shown Figure 2(b). In this case, the propagation of the binary signal alternates between the two polarizations.



Figure 2. (a) QCA wire (90°); (b) QCA wire (45°).

2.3. QCA Majority Gate

The fundamental QCA logical circuit is the three-input majority gate that appears in Figure 3 [a]. The majority gate produces an output that reflects the majority of the inputs.

The QCA majority gate has four terminal cells out of which three are representing input terminals and the remaining one represents the output cell [5]. Assuming that the three inputs are A, B and C, the logic function of the majority gate is:

$$M(A,B,C)=AB+BC+CA$$

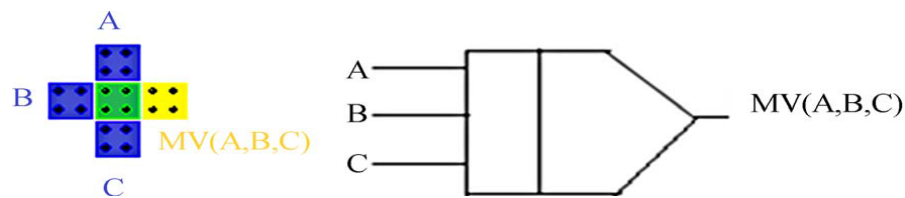


Figure 3. (a) QCA majority gate; (b) Schematic majority gate representation.

2.4 Inverter:

The two different structures of QCA inverter is shown in Figure 4. An inverter is usually formed by placing the cells with only their corners touching. The electrostatic interaction is inverted, because the quantum dots corresponding to different polarizations are misaligned between the cells [20]. The second inverter is built by neighboring QCA cells on the diagonal, which causes Coulomb forces to place the two electrons in opposing wells of the cell with respect to the source.

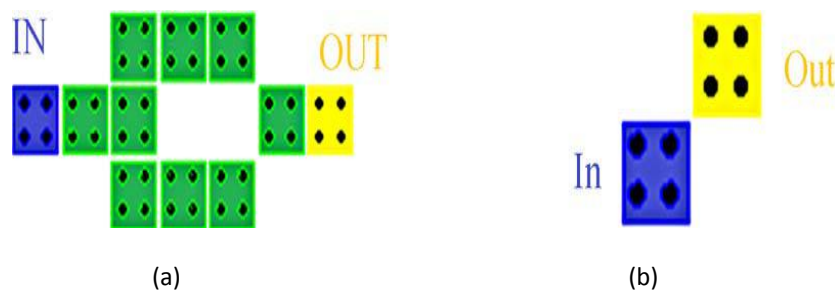


Figure 4. QCA inverters.

2.5 QCA AND GATE

As we work in the field of QCA with the known binary representation, it is preferable to have further logic gates we are already familiar with. By a slight modification, it is possible to turn the majority voter into an AND gate. The boolean AND outputs 1 if all inputs are 1, otherwise 0. Regarding two inputs of the majority voter, as the inputs of an AND gate, and the voter should not output 1 if only one of the two inputs is one, a fixed cell is added as third input, that always is in the 0 state. If both AND inputs are 1, the two 1s sum up to a stronger Coulomb force than the single fixed 0 cell and the majority voter is turned into a two-input AND gate (see figure 5). The fixed cell can be obtained by setting it to the 0 state and never open the electron tunnel junctions



Figure 5.(a) QCA AND Gat

INPUT		OUTPUT
A	B	$Y=A.B$
0	0	0
0	1	0
1	0	0
1	1	1

Fig:5(b) Truth table of AND GATE

2.6 QCA OR Gate:

The OR gate is built almost exactly like the AND gate, but instead of a fixed 0, a fixed 1 QCA cell must be attached as one input. The fixed 1 cell sums up to a stronger Coulomb force with a single other input being adjusted to 1, so that the OR gate will output 1, if one of the free inputs is 1. Qca OR GATE Shown in Figure 6.

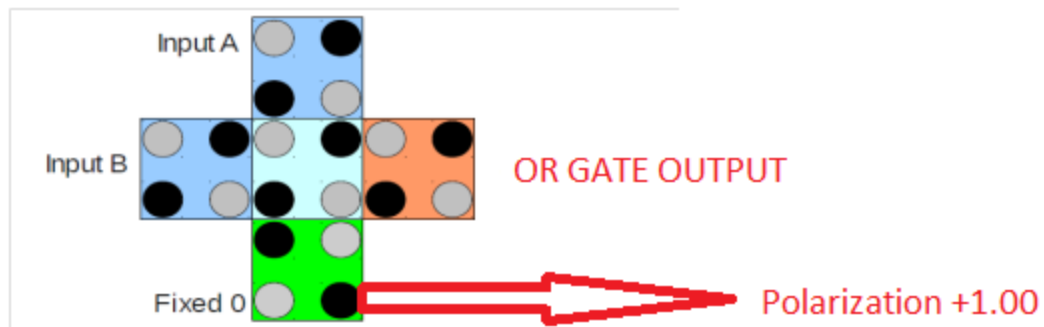


FIG:6(a):QCA OR GATE

INPUT		OUTPUT
A	B	$Y=A+B$
0	0	0
0	1	1
1	0	1
1	1	1

FIG:6(b):OR GATE Truth TABLE

2.7 Crossovers in QCA:

A QCA design permits two options for crossover, termed coplanar crossover and multilayer crossover. While the coplanar crossover uses only one layer but involves usage of two cell types (termed regular and rotated), the multilayer crossover uses more than one layer of cells (analogous to multiple metal layers in a conventional IC). Multilayer crossover is used in this book for wire crossings since we can effectively cross signals over on another layer and the extra layers of QCA can be used as active components of the circuit. Further, multilayer QCA circuits can potentially consume much less area as compared to planar circuits.

2.8. QCA Clocking

The adiabatic switching is firstly proposed by Lent et al. to remedy the metastable state which was one of the disadvantages between successive phases, a QCA system is synchronized. In the switch phase, inter-dot barriers are steadily raised and the electrons can transfer between dots. By taking a certain polarization value during the hold phase, when the inter-dot barriers are completely high, the cell can only bias the neighboring cells. In the release and relax phases, the cell will lose its polarization. QCA Clocking Shown in figure 7.

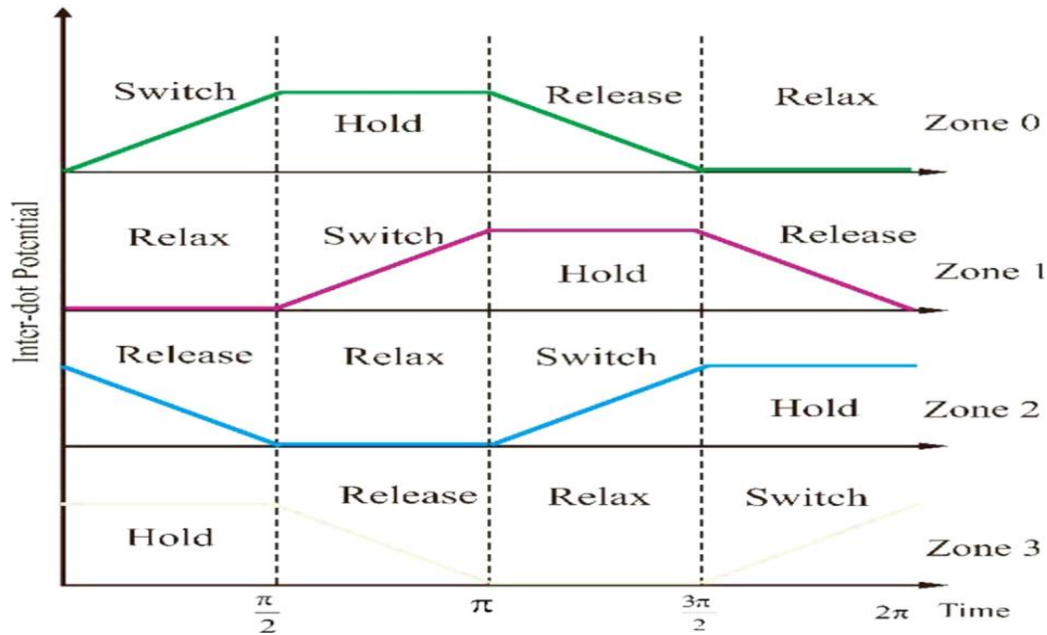


Figure 7. QCA clocking phases within clock zones

3. Overview Reversible Logic Gates:

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-Out is not allowed as one-to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits.

- The number of Reversible gates (N): The number of reversible gates used in circuit.
- The number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.
- Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1×1 or 2×2) required to realize the circuit.

3.1 different type of reversible logic gates are given below

Mainly there are six types of Reversible Gates are mostly used. Those are:

- FEYNMAN Gate
- FREDKIN Gate
- TOFFOLI Gate
- PERES Gate
- TR Gate
- BKN Gate

3.2 Applications

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance .it include the area like

1. Low power CMOS.
2. Quantum computer.
3. Nanotechnology
4. Optical computing
5. Design of low power arithmetic and data path for digital signal processing (DSP).
6. Field Programmable Gate Arrays (FPGAs) in CMOS technology for extremely low power, high testability and self-repair

(qca tool)

4. reversible gates with qca:

In this section we will discuss about the topics we completed so far. We will discuss about the implementation of Feynman gate and Toffoli gate implementation using QCADesigner with its circuit design and simulation result.

4.1 FEYNMAN GATE

Feynman gate is a 2*2 one through reversible gate as shown in figure 8(a). The input vector is $I(A, B)$ and the output vector is $O(P, Q)$. The outputs are defined by $P=A$, $Q=A \oplus B$. Quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs. Truth table of FEYNMAN Gate given in Figure 8(b).

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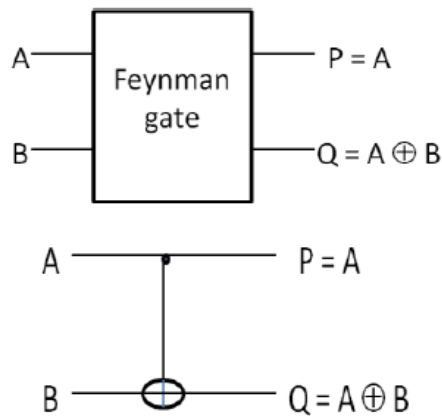


Figure 8 (a) FEYNMAN Gate-Block Diagram

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Figure 8 (b) Truth Table of FEYNMAN Gate

4.1 FEYNMAN Gate circuit design using QCA designer

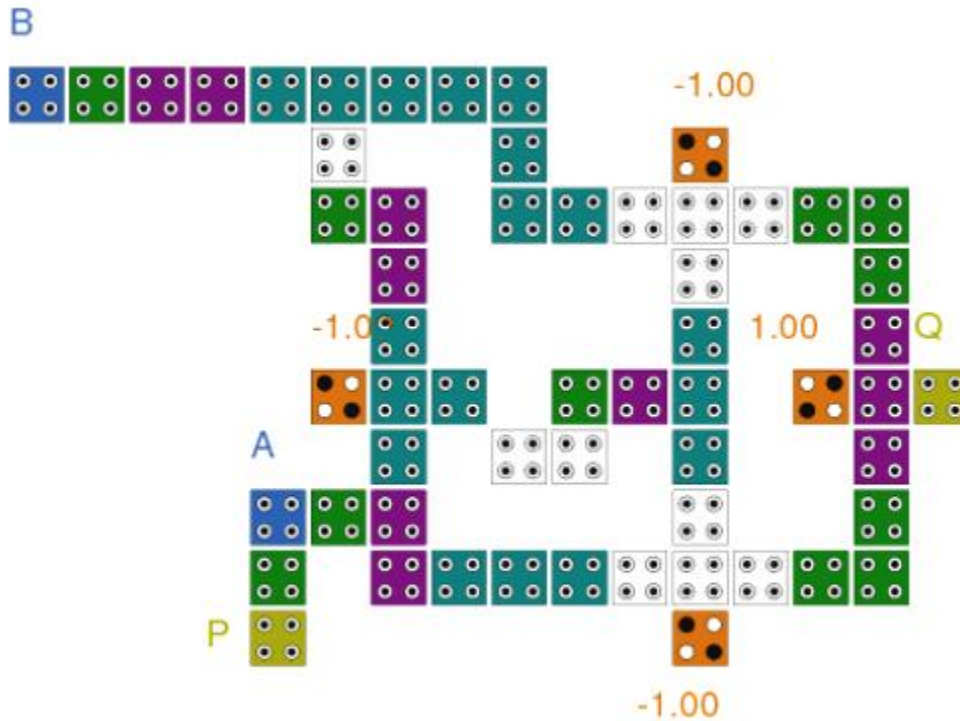
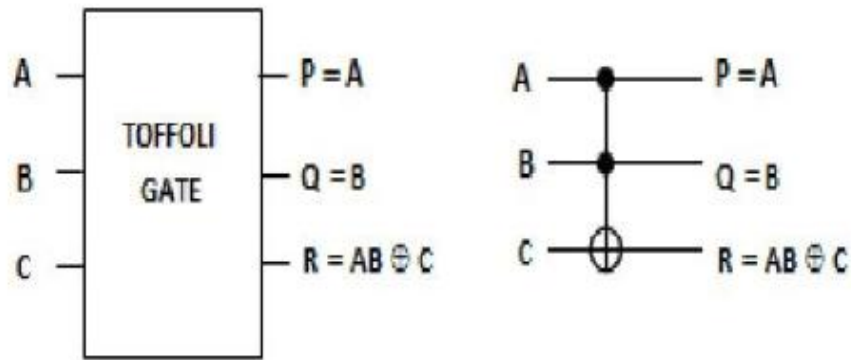


Figure 8(c) FEYNMAN Gate circuit using QCA designer tool

4.2 TOFFOLI Gate

Toffoli gate is a 3*3 reversible gate. The input vector is $I(A, B, C)$ and output vector $O(P, Q, R)$. The outputs are defined by $P=A$, $Q=B$, $R=AB \oplus C$. Quantum cost of a Toffoli gate is 5. TOFFOLI GATE Block Diagram shown in Figure 9(a) and Truth table shown in figure 9(b).



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pic)

Figure 9 (a): Block diagram of Toffoli Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Figure 9 (b): Truth Table of Toffoli Gate

4.3 Circuit design of TOFFOLI Gate using QCA Designe

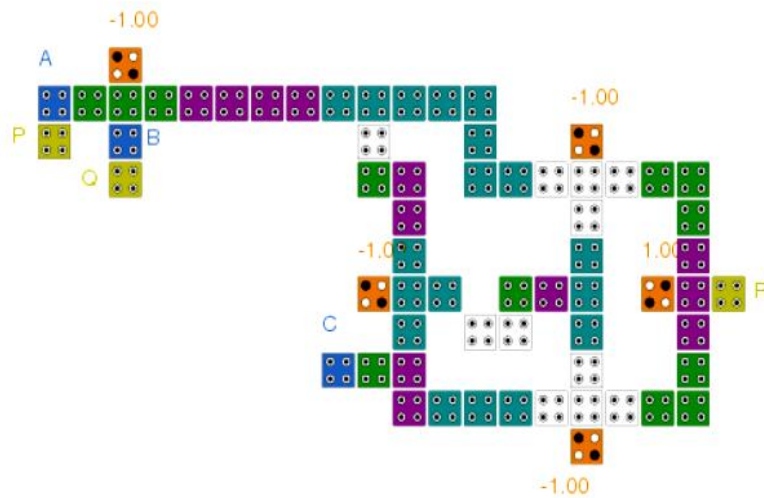
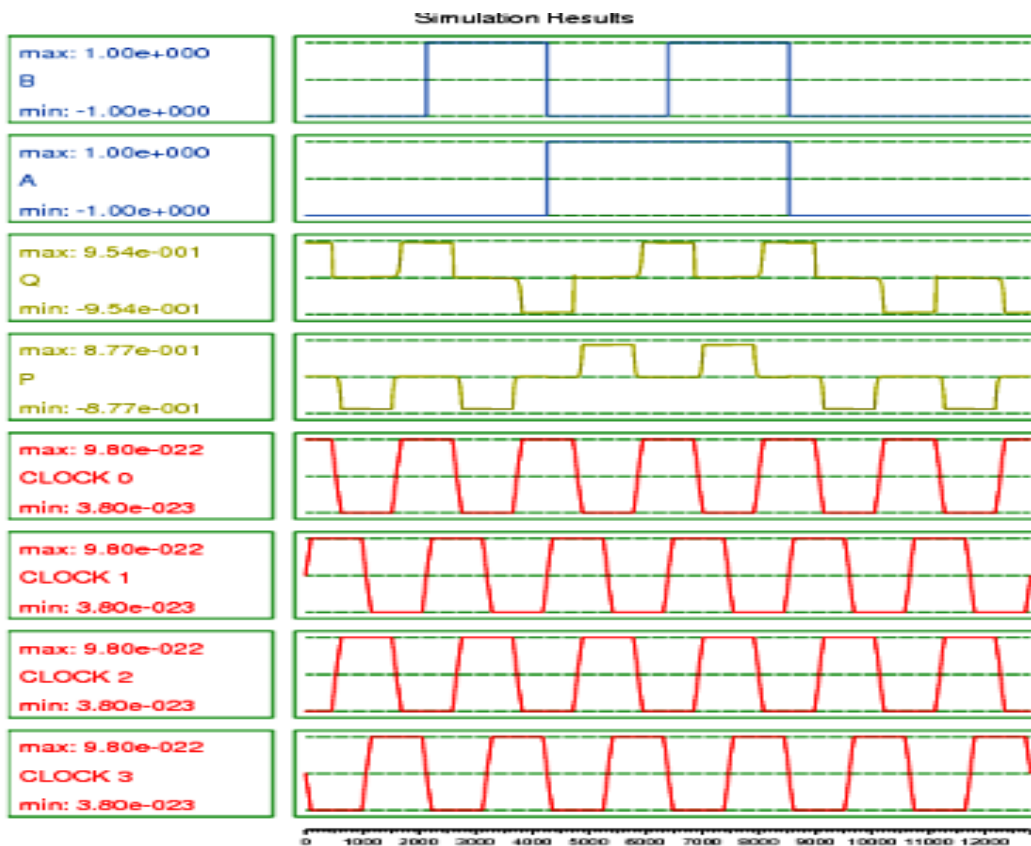


Figure 9 (c): Circuit diagram of TOFFOLI gate(point out i/p and o/p)

(eps tool)

5) Result and Discussion(all simulation add last page)



(input o/p direct)

Figure 10 (a) Simulation result of FEYNMAN Gate circuit

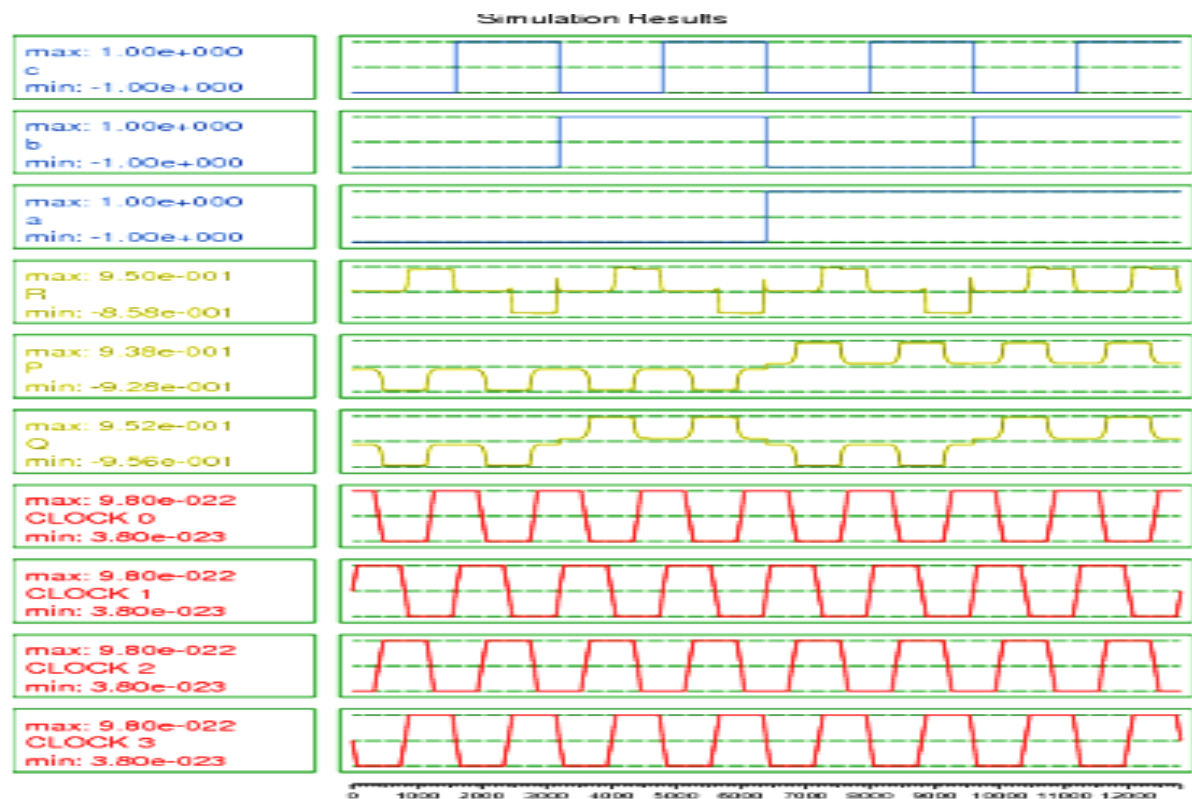


Figure 10 (b): Simulation result of TOFFOLI Gate

6) Proposed Work

In this section we will discuss about the two Reversible priority Encoders which we have developed using the concept of FEYNMAN gate and TOFFOLI gate (Discussed above) so far. These two encoders are 4 to 2 Reversible Priority encoder and 8 to 3 Reversible Priority Encoder. We will understand the circuit design by its block diagrams and also analyze the simulation results of both of the Encoders.

6.1 4 to 2 Reversible Priority Encoder:

A priority encoder is a circuit or algorithm which basically compressed multiple binary inputs into a smaller number of outputs. Here Reversible priority encoder also generates the compressed output in reverse format. In 4 to 2 reversible priority encoder four input lines are there which are the responsible for the input values and three output lines provide the expected priority results in reverse format.

*Refer below the Block diagram of 4 to 2 Reversible Priority Encoder for better understanding

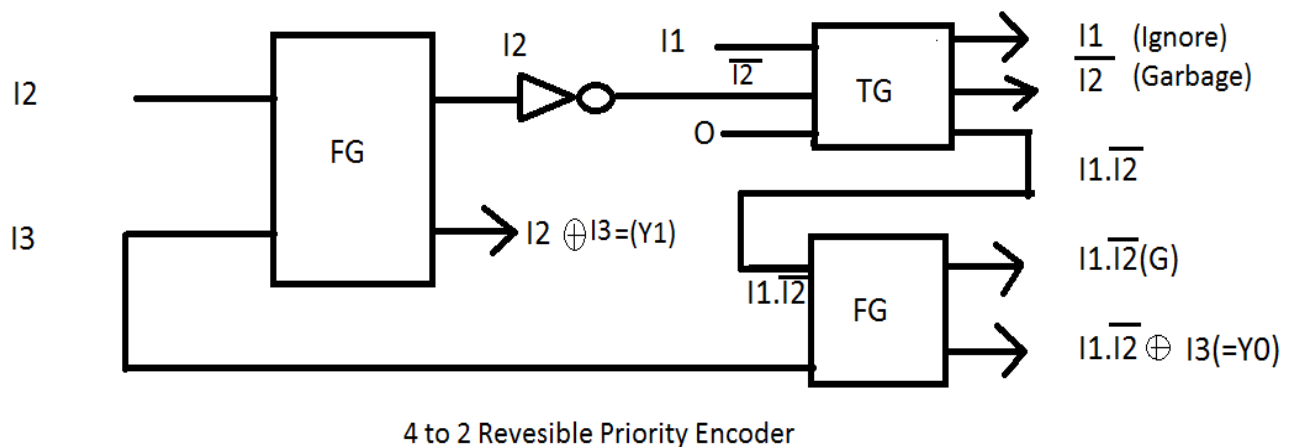


Fig:11(a) Block Diagram of 4 to 2 Reversible Priority Encoder

(change block.diagram)

6.1.2 Truth Table of 4 to 2 Reversible Priority Encoder:

INPUT				OUTPUT	
D3	D2	D1	D0	Q1	Q0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1
0	0	0	0	X	X

6.1.3 Circuit diagram of 4 to 2 Reversible Priority Encoder:

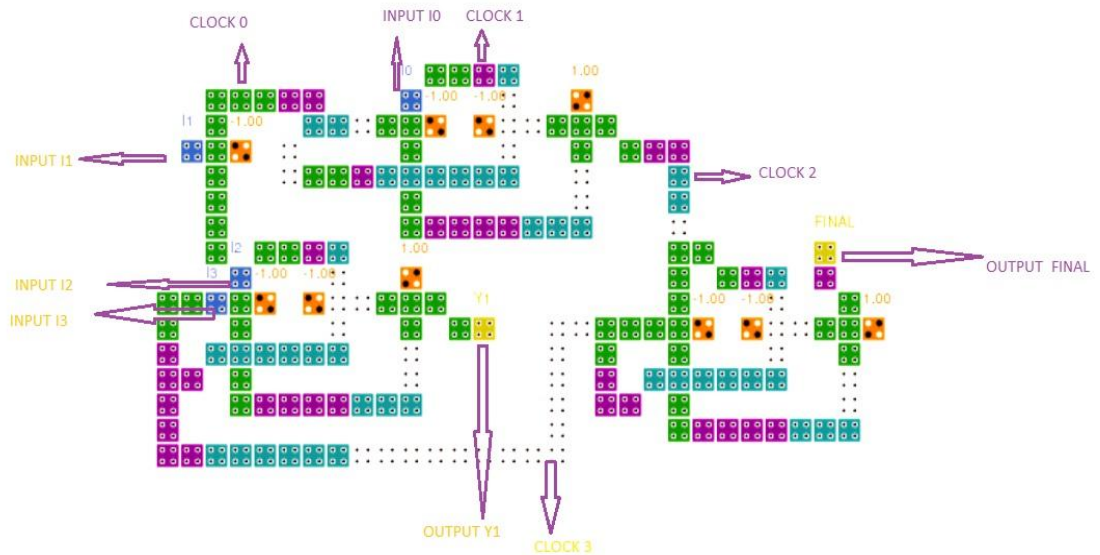


Fig:11(b) Circuit diagram of 4 to 2 Reversible Priority Encoder using QCA Designer (arrow syntax Black)

6.1.4 Diagram Explanation: From the above circuit diagram [Fig: 11(b)] we can describe the followings.

- Blue cells denoted as input cells (like: INPUT I0, INPUT I1, INPUT I2, INPUT I3)
- Yellow cells denoted as Output cells (like: OUTPUT Y1, OUTPUT FINAL)
- Green and Purple cells denoted as Clock applied throughout the circuit (CLOCK 0, CLOCK 1, CLOCK 2 and CLOCK 3).
- Orange colored cells denoted as normal cells with polarity

Now, if we closely observed the whole circuit then it is so clear to us that the circuit represents a 4 to 2 reversible priority encoder, where it's have four input lines (I0,I1,I2,I3) and two output lines (Y1, OUTPUT FINAL). The polarized cells performed a job as a reversible cells and whole circuit is connected using clocks.

6.2 8 to 3 Reversible Priority Encoder

A priority encoder is a circuit or algorithm which basically compressed multiple binary inputs into a smaller number of outputs. Here Reversible priority encoder also generates the compressed output in reverse format. In 8 to 3 reversible priority encoder four input lines are there which are the responsible for the input values and three output lines provide the expected priority results in reverse format.

*Refer below the Block diagram of 8 to 3 Reversible Priority Encoder for better understanding

[Space for Block Diagram]

6.2.2 Truth Table of 4 to 2 Reversible Priority Encoder:

INPUT								OUTPUT		
D7	D6	D5	D4	D3	D2	D1	D0	Q2	Q1	Q0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	X	0	0	1
0	0	0	0	0	1	X	X	0	1	0
0	0	0	0	1	X	X	X	0	1	1
0	0	0	1	X	X	X	X	1	0	0
0	0	1	X	X	X	X	X	1	0	1
0	1	X	X	X	X	X	X	1	1	0
1	X	X	X	X	X	X	X	1	1	1

(block diagram 8 to 3)

6.2.3 Circuit diagram of 8 to 3 Reversible Priority Encoder:

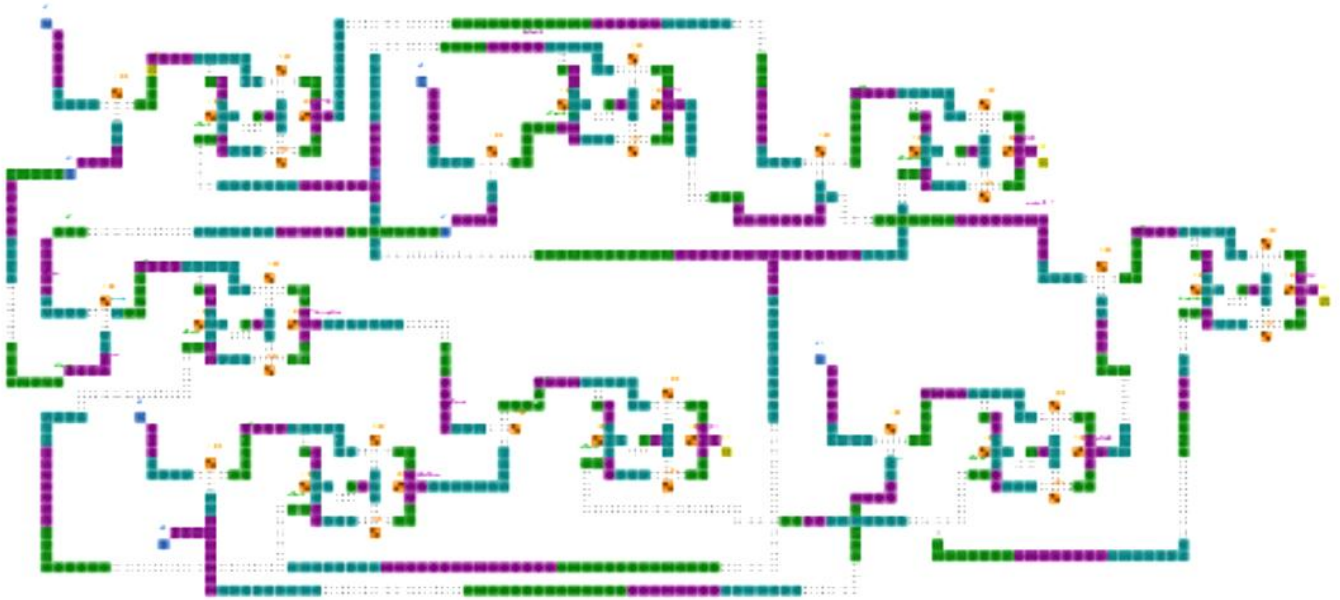


Fig:12(a) Circuit diagram of 8 to 3 Reversible Priority Encoder using QCA Designer

6.2.4 Diagram Explanation: From the above circuit diagram [Fig: 12(a)] we can describe the followings.

- Blue cells denoted as input cells (like: INPUT I0, INPUT I1, INPUT I2, INPUT I3, INPUT I4, INPUT I5, INPUT I6, INPUT I7)
- Yellow cells denoted as Output cells (like: OUTPUT Y1, OUTPUT Y2, OUTPUT FINAL)
- Green and Purple cells denoted as Clock applied throughout the circuit (CLOCK 0, CLOCK 1, CLOCK 2 and CLOCK 3). .
- Orange colored cells denoted as normal cells with polarity

Now, if we closely observed the whole circuit then it is so clear to us that the circuit represents a 8 to 3 reversible priority encoder, where it's have four input lines (I0,I1,I2,I3,I4,I5,I6,I7) and two output lines (Y1, OUTPUT FINAL). The polarized cells performed a job as a reversible cells and whole circuit is connected using clocks.

7) Results and Discussion of Reversible Priority Encoders

7.1 4 to 2 Reversible Priority Encoder

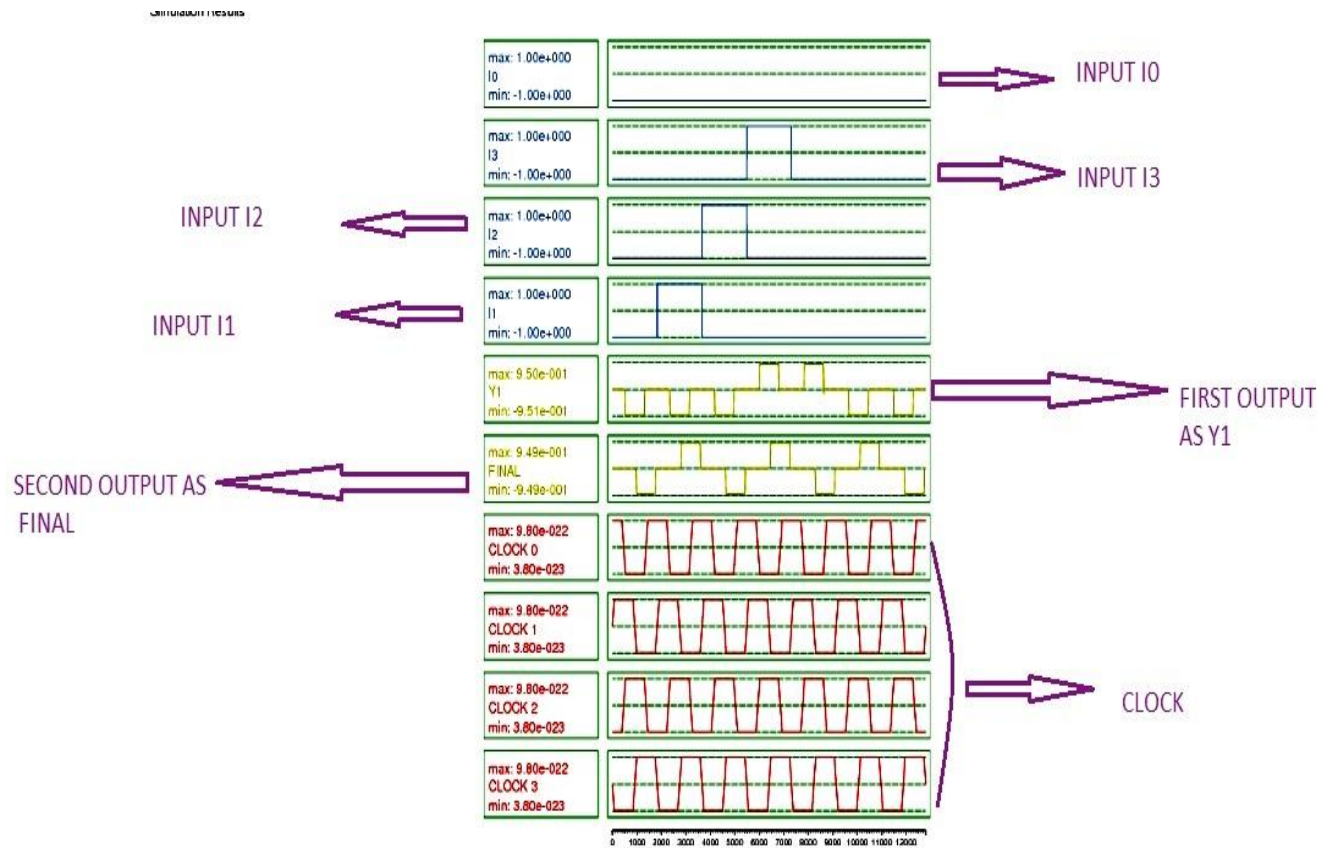


Fig:13(a) Simulation result of 4 to 2 Reversible Priority Encoder using QCA designer

7.2 8 to 3 Reversible Priority Encoder

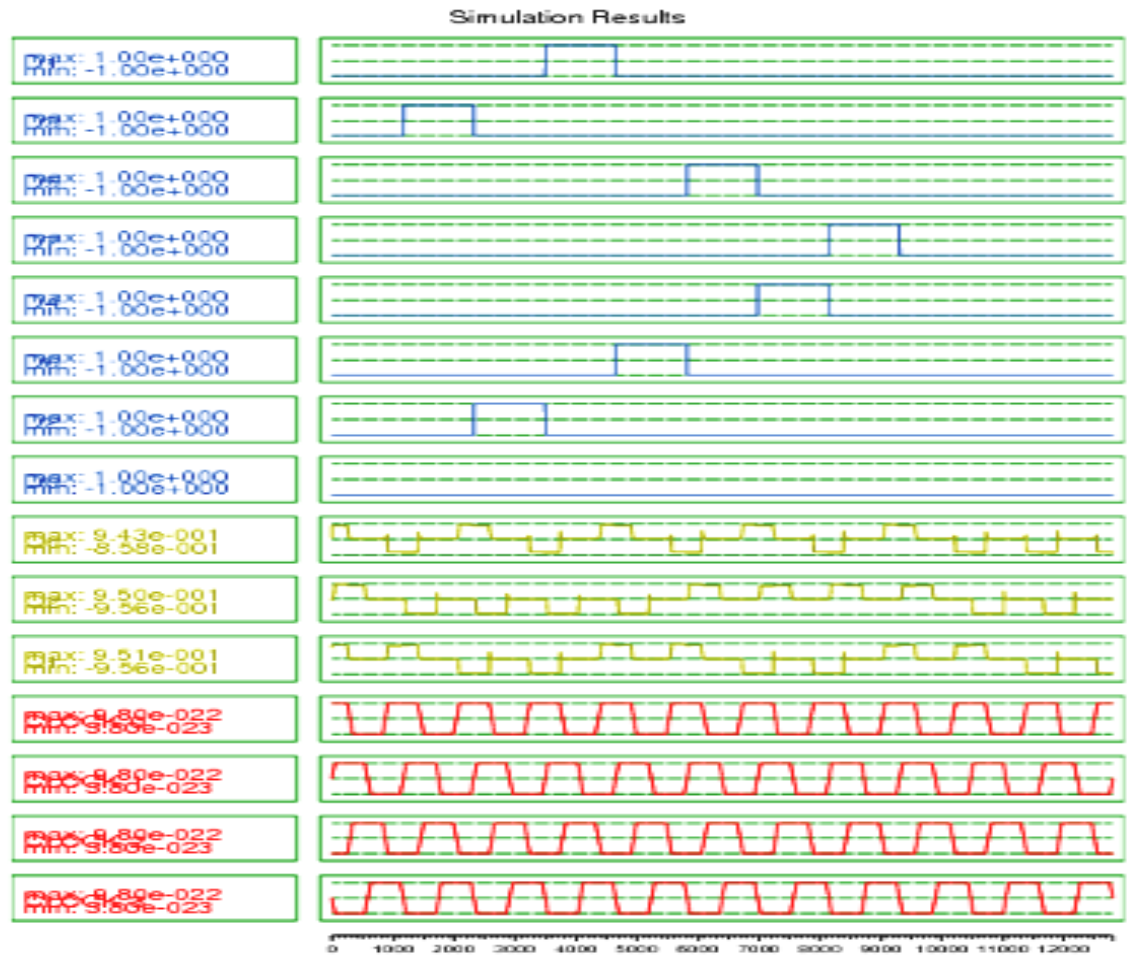


Fig:13(b) Simulation result of 8 to 3 Reversible Priority Encoder using QCA designer

(direction i/p and o/p)

8. Conclusion

We have presented an approach to realize the multipurpose binary reversible gates. Such gates can be used in regular circuits realizing Boolean functions. In the same way it is possible to construct multiple-valued reversible gates having similar properties. The proposed asynchronous designs have the applications in digital circuits like a Timer/Counter, building reversible ALU, reversible processor etc. This work forms an important move in building large and complex reversible sequential circuits.

9. References

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