

1. For the page size, which one is correct
    - A. Small page table size requires a small page size
    - B. Small number of page faults requires a small page size
    - C. A large TLB reach requires a large page size
    - D. All of the above are NOT correct
  2. Which one is correct for the page fault handling
    - A. Page fault will never occur when a mapping exists in the page table for the accessed virtual address
    - B. Page fault can be handled without hardware intervention
    - C. Page fault can be handled purely in unprivileged mode
    - D. The address of the page table is stored inside a privileged register inside CPU and the address is physical address
  3. A system with 32-bit addresses, 1 GB physical memory, and a 1-Megabyte (20-bit) page size will have a page table (assume the page table is single level) that contains:
    - A. 4K entries
    - B. 4M entries
    - C. 1M entries
    - D. 1K entries
  4. Assume that a system with memory mapping done on a page basis and using a single-level page table, the necessary page table is always in memory. The system has TLB. The memory reference takes 100ns, and the TLB access takes 20ns. If the TLB hit rate is 90%, what is the effective memory access time?
    - A. 100ns
    - B. 120ns
    - C. 130ns
    - D. 220ns
  5. Suppose the physical memory is 128 pages, with each page size 32 bytes. The virtual address space for the process in question (assume there is only one) is 1024 pages or 32 KB.
    - a) How many bits are used for the virtual address, page offset and VPN. How many bits are used for physical address space, page offset and PFN.
    - b) Suppose the content of 128 physical pages is as follows.





The PDBR value is 108 (decimal) [This means the page directory is held in this page].

The format of a PTE is thus: VALID | PFN6 ... PFN0. Thus each PTE is one byte.

The format of a PDE is similar : VALID | PT6 ... PT0. Thus each PDE is also one byte.

For VALID bit, 0 means invalid and 1 means valid.

For the virtual address **611c**, and virtual address **3da8**, show the physical address or a generation of fault if the physical address can be translated. If the page translation is successful, show the

content of the physical address. You need to give the detailed process of address translation.  
[15 points]

Two examples are given.

Virtual Address 17f5:

- > pde index:0x5 [decimal 5] pde contents:0xd4 (valid 1, pfn 0x54 [decimal 84])
- > pte index:0x1f [decimal 31] pte contents:0xce (valid 1, pfn 0x4e [decimal 78])
- > Translates to Physical Address 0x9d5 --> Value: 1c

Virtual Address 7f6c:

- > pde index:0x1f [decimal 31] pde contents:0xff (valid 1, pfn 0x7f [decimal 127])
- > pte index:0x1b [decimal 27] pte contents:0x7f (valid 0, pfn 0x7f [decimal 127])
- > Fault (page table entry not valid)

