Homework

For a direct-mapped cache design with a 64-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
63-10	9-5	4-0

(1) What is the cache block size (in words)?
(2) How many blocks does the cache have?
(3) What is the ratio between total bits required for such a cache implementation over the data storage bits?

Beginning from the power on, the following byte-addressed cache references are recorded.

Address											
Hex	00	04	10	84	E8	A0	400	1E	8C	C1C	B4	884
Dec	0	4	16	132	232	160	1024	30	140	3100	180	2180

(1) For each reference, list i) its tag, index, and offset, ii) whether it is a hit or a miss, and iii) which bytes were replaced (if any).
(2) What is the hit ratio?