Recent Advances in GaN-based Semiconductors for Millimeter-Wave and Terahertz Applications

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(Graduate Term Paper)

***Abstract*—Millimeter-wave (mmWave) and terahertz (THz) technologies have witnessed significant progress over the past decade. This progress is due to advances in semiconductor materials, device engineering, circuit design, and system-level integration. These developments have enabled emerging applications in ubiquitous communications, high-resolution imaging, and spectroscopy. III–V compound semiconductors, particularly gallium nitride (GaN), have become indispensable for high-power and high-efficiency mmWave/THz front ends. This paper reviews brief history and recent advances in radio-frequency (RF) semiconductors with an emphasis on GaN-based innovation that extends operation toward the mmWave and THz regimes. Key topics include the physical principles of GaN-based devices, covering high-electron-mobility transistors (HEMTs), diodes, and photonic components, as well as their epitaxial and process innovations that enhance cutoff frequency and power performance. The review also discusses emerging trends in heterogeneous and CMOS-compatible integration. The review concludes with an outlook on the remaining challenges and opportunities for GaN technologies in future mmWave and THz applications.**

***Index Terms*—Device fabrication, gallium nitride (GaN), heterogeneous integration (HI), high-electron-mobility transistor (HEMT), millimeter-wave (mmWave), radio-frequency semiconductors, terahertz (THz).**

I. Introduction

MILLIMETER-WAVE (mmWave) and Terahertz (THz) bands, roughly defined as between 30-300 GHz and 0.3-10 THz, respectively, have attracted enormous attention in numerous emerging technologies, including ultrafast, high-capacity wireless communication [1], [2], high-resolution imaging [3], [4], and spectroscopic sensing [5], due to their unique characteristics such as large available bandwidth and fine spatial resolution. However, realizing practical mmWave/THz systems presents formidable challenges at the hardware level, where device efficiency, power output, linearity, and thermal reliability become critical limiting factors [6].

For mmWave applications, the current state of the art, spanning both silicon (Si)-based and III–V compound devices, has achieved remarkable progress in extending operational frequencies toward the lower THz range [7]. Nevertheless, a persistent performance void remains between the upper limits of electronic circuits and the lower limits of photonic systems, commonly referred to as the "THz gap." Numerous approaches, as illustrated in Fig. 1, have been proposed to bridge this gap, typically classified according to the underlying physics of operation: *electronics*, *photonics*, and *plasmonics* [8]. The electronic and photonic domains are generally constrained within the mmWave and optical ranges, respectively, due to intrinsic carrier transport and photon energy limitations. Extending their boundaries into the THz regime often requires frequency-conversion techniques that exploit material nonlinearities, which inevitably introduce signal distortion and limited bandwidth. Meanwhile, the utilization of plasmonic polaritons in two-dimensional (2D) materials such as graphene [9] offers intrinsic operation within the THz region. Nevertheless, such approaches are still in their early stage of development and still far from practical system-level implementation.

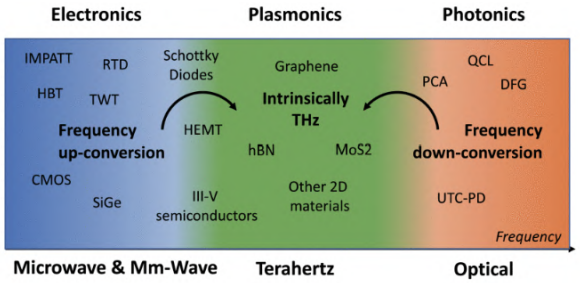

Fig. 1. Technological pathways towards THz operation (adapted from [8])

Given the maturity and large-scale manufacturing capabilities of electronic technologies, they remain the most practical and commercially dominant approach for realizing mmWave and THz systems. Their established presence in 5G transceivers, radar sensors, and imaging modules demonstrates readiness for widespread deployment. Accordingly, this paper focuses on electronic solutions, particularly wide-bandgap III–V compound semiconductors such as gallium nitride (GaN), as leading candidates for extending high-power and high-efficiency operation into the THz regime.

The remainder of this paper is organized as follows. Section II provides an overview of RF semiconductor technologies for mmWave and THz applications, highlighting the evolution of GaN-based devices as key enablers of high-power and high-efficiency front ends. Section III discusses the fundamental device physics and operation priciples of GaN-based HEMTs, diodes, and photonic devices. Section IV discusses major fabrication processes that have driven performance scaling in GaN devices. Section V presents emerging directions in HI, complementary metal–oxide–semiconductor (CMOS) co-

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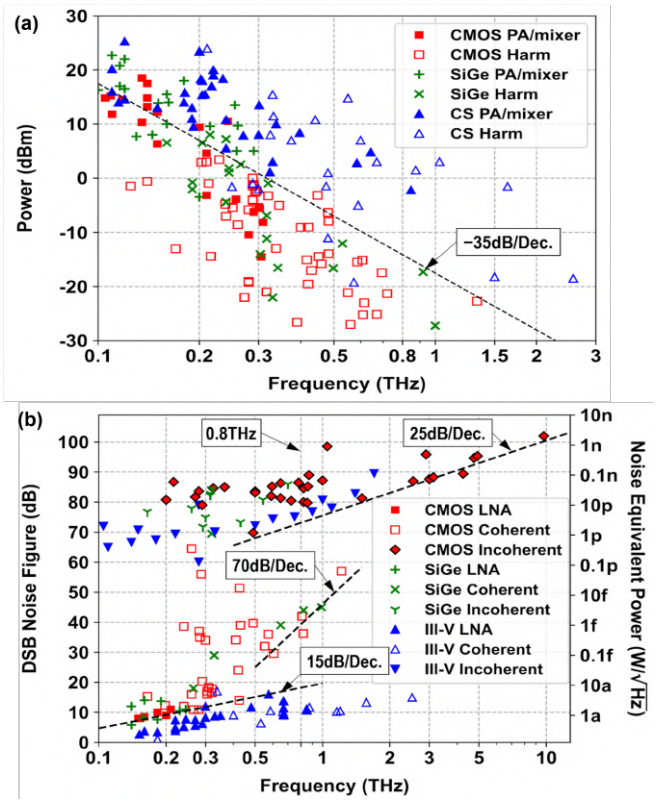

Fig. 2. A survey of mmWave/THz electronics performance: (a) transmitter output per element and (b) double side band (DSB) noise figure and noise equivalent power (adapted from [15]).

integration, and advanced packaging for next-generation RF systems. Finally, Section VI concludes with an outlook on remaining challenges and future opportunities in GaN-based mmWave and THz electronics.

II. An Overview of mmWave/THz Electronics

Decades of continuous development and dominance in the digital market have made Si CMOS technology remarkable for its integration density and manufacturing cost efficiency, leading to the widespread adoption of RF system-on-chip (SoC) implementations [10]. The high-frequency performance of mmWave/THz ICs is primarily characterized by the transit frequency (f_{T}), defined as the frequency at which the short-circuit current gain equals unity, and the maximum frequency of oscillation (f_{max}), defined as the point where the unilateral power gain drops to unity. While f_{T} dictates the intrinsic speed and phase noise of current-mode logic and amplifying circuits, the available gain and transconductance (g_m) are closely tied to f_{Max}. State-of-the-art CMOS processes now achieve $f_{\mathrm{T}}/f_{\mathrm{max}}$ values up to 314/180 GHz in n-type and 285/140 GHz in p-type FinFETs, respectively [11]. RF silicon-on-insulator (SOI) technology offers a cost-effective alternative featuring excellent device matching, reduced parasitic capacitance, and high power efficiency [12]. Meanwhile, silicon–germanium (SiGe) bipolar–CMOS (BiCMOS) technology leverages SiGe heterojunction bipolar transistors (HBTs) to reach $f_{\mathrm{T}}/f_{\mathrm{max}}$ of 505/720 GHz [13]. Despite the advantages in cost and integrability with logics and memories, Si-based technologies remain constrained by low breakdown voltage, modest electron mobility, and thermal limitations, which restrict their efficiency and power handling at mmWave and THz frequencies [14].

TABLE I
Comparisons of RF Semiconductor Material Properties

Properties	Si	GaAs	GaN	InP
Bandgap (eV)	1.12	1.42	3.4	1.34
Breakdown field (MV/cm)	0.3	0.4	3.3	0.5
Electron mobility (cm^2/V·s)	1,450	8,500	2,000	5,400
Hole mobility (cm^2/V·s)	480	400	300	150
Saturation electron velocity ($\times 10^7$ cm/s)	1.0	2.0	2.5	2.0
Dielectric constant	11.8	12.8	9.0	12.4
Thermal conductivity (W/m·K)	150	47-55	130-230	68
Johnson's FoM	1.0	2.7	27.5	0.33

III–V compound semiconductors, on the other hand, exhibit superior electron transport and field-handling capabilities. HEMTs and HBTs exploit these material advantages to achieve high power densities, low noise figures, and operation extending to 2 THz (see Fig. 2) [15]. Monolithic microwave integrated circuits (MMICs) integrate these active devices with passive components into compact, high-performance modules that underpin modern RF, radar, and sensing systems. Furthermore, the direct-bandgap nature of III–V semiconductors enables their use in optoelectronic and photomixing-based THz sources operating beyond 3 THz [16]. The presence of III-V devices in both electronic and photonic domains can open doors for new possibilities in hybrid mmWave and THz systems. Furthermore, recent progress in heterogeneous Si/III–V integration has also aimed to combine the scalability and cost advantages of CMOS with the high-speed and power-handling capabilities of III–V materials, offering a promising path toward hybrid front ends [17]. We will revisit this topic in Section V.

Among III-V compounds, GaN has been proven to be a commercial success in various microwave and mmWave markets, including 5G telecommunications, defense, and automotive. Its wide bandgap of 3.4 eV, high breakdown field exceeding 3 MV/cm, electron saturation velocity of approximately 2.5×10^7 cm/s, and thermal conductivity around 130 W/m·K collectively enable superior power density, efficiency, and thermal robustness compared to gallium arsenide (GaAs) or indium phosphide (InP) counterparts, as shown in Table I [18]–[20]. Notably, GaN possesses a much higher Johnson's figure of merit (FoM), defined as the product of the charge carrier saturation velocity and the electric breakdown field, with a value of 27.5 compared to the presented materials, indicating its outstanding capability to sustain high voltages while maintaining rapid carrier transport. These characteristics make GaN HEMTs dominant for high-efficiency, high-power mmWave power amplifiers (PAs) for base stations, as well as compact arrays where thermal management is critical. Moreover, the maturity of AlGaN/GaN heterostructures on SiC and Si substrates has improved yield, cost scalability,

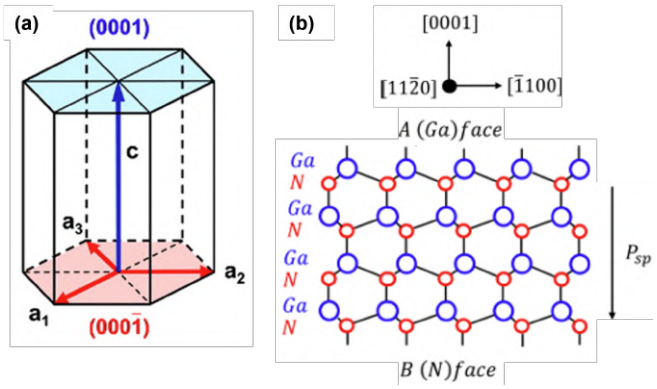

Fig. 3. (a) Hexagonal unit cell of GaN and (b) crystal structure of GaN, indicating the sign and direction of the spontaneous polarization (adapted from [24]).

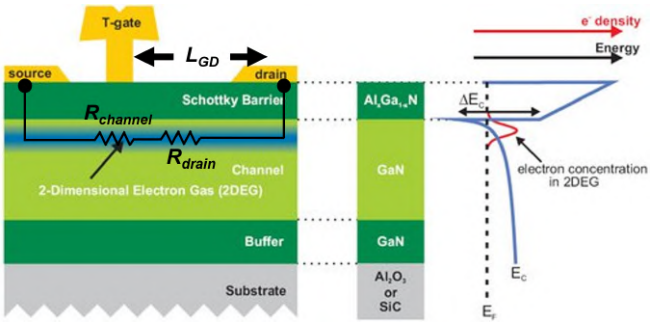

Fig. 4. Basic GaN HEMT schematic with its band diagram (adapted from [27]).

and reliability [21]. Beyond electronics, GaN-based photonic platforms have also demonstrated potential for THz wave generation and detection [22], [23].

III. Principles of GaN-based Devices for mmWave and THz Applications

A. Material and Heterostructure Physics of GaN

GaN is a wide-bandgap (WBG) semiconductor with a direct energy gap of 3.4 eV at room temperature. Historically, its early development was motivated by the demand for ultraviolet optoelectronic devices, including light-emitting diodes and laser diodes, owning to this property. GaN's WBG nature results in a high critical electric field, high electron saturation velocity, and strong thermal stability, as previously mentioned. Additionally, the energy gap of III-N alloys can be continuously tuned by introducing aluminum or indium into GaN, spanning a range from 0.7 eV (InN) to 6.2 eV (AlN), thereby offering broad flexibility for both electronic and optoelectronic device design. In most GaN transistors, the active channel is formed on AlGaN/GaN heterostructures, with AlN and AlGaN layers commonly employed as nucleation and buffer layers, respectively, to accommodate lattice mismatch and reduce dislocation densities [24].

Structurally, GaN crystallizes in a hexagonal wurtzite configuration, as illustrated in Fig. 3(a), which lacks an inversion symmetry along the c-axis (0001). This polar nature distinguishes GaN (and III-N semiconductors) from other III–V compounds such as GaAs and InP. Since nitrogen has a higher electronegativity than gallium, Ga and N atoms become anionic and cationic, respectively, inducing a spontaneous polarization P_{Sp} along the c-axis, as illustrated in Fig. 3 (b). The spontaneous charges in GaN give rise to bound surface charges at the interfaces of GaN layers. In addition to the spontaneous polarization, the strain in the crystal and the displacement of anion sublattice with respect to cation sublattice lead to a piezoelectric polarization P_{Pe} along the [1000] direction [25].

When forming a heterojunction between III-N semiconductors with different bandgaps, such as GaN and AlGaN. The combined effects of P_{Sp} and P_{Pe} leads to a net polarization discontinuity at AlGaIn/GaN heterointerface, resulting in a sheet of fixed positive polarization charges at the interface. These positive charges attract free electrons, which are provided by ionized donor-like surface states or defects in the AlGaN layer. These electrons accumulate in a potential well at the GaN side of the interface, forming a high-density, high-mobility two-dimensional electron gas (2DEG) regardless of intentional doping [26].

B. Device Operation and Scaling of GaN HEMTs

In a GaN-based HEMT, a gate metal is placed on and AlGaN/GaN heterostructure, with a corresponding schematic illustrated in Fig. 4 and its corresponding band diagram [27]. While a AlGaN "barrier" provides isolation between the gate and channel, as well as gate-controlled charge capacity that enable electron flow, the channel at the interface of GaN originated from 2DEGs serves as the conduction path between the source and drain of the device. To constrain the flow in the channel and avoid current leakage into a substrate and neighboring devices, the buffer made of C-doped GaN or AlN is placed beneath the channel. Notably, the distance between the gate and drain (L_{GD}) determines the breakdown voltage V_{br} [24], which should be sufficiently high for high-power applications. However, to enhance the operation speed and lower the ON-resistance R_{on}, which is the sum of the channel resistance $R_{channel}$ and drain-side access resistance R_{drain} (i.e., $R_{on} = R_{channel}+R_{drain}$), both gate length L_G and L_{GD} must be minimized. For this reason, a T-shaped gate is utilized to reduce $R_{channel}$, as well as maximize f_T and f_{max}. Besides the channel properties, lattice mismatch and difference in the coefficient of thermal expansions (CTEs) with the substrate are important factors that dictate the performance of GaN-based devices. We will discuss this in Sec. IV. Notably, the highest f_T of 359 GHz was achieved in In/AlN/GaN on SiC with a 20 nm slef-aligned gate [28], while GaN-on-Si with a recessed gate of L_G = 30 nm yielded the highest f_{max} of 680 GHz [29].

GaN HEMTs can be classified based on their geometries into two major types: *lateral* and *vertical* architectures [30]. For the lateral devices, the current flows parallel to the surface of the substrate, with the source, gate, and drain terminals patterned on the same plane (see Fig. 4). This configuration is inherently ON, i.e., there is current conduction when no gate

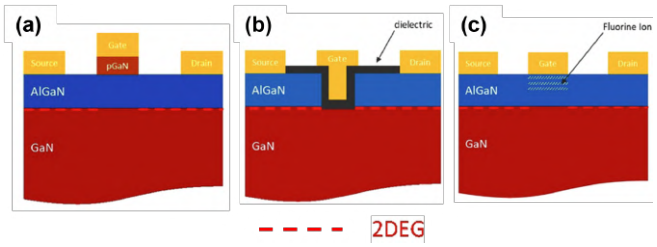

Fig. 5. E-mode GaN HEMTs: (a) p-gated HEMT, (b) Recessed MIS-HEMT, and (c) F-Gate HEMT (adapted from [24]).

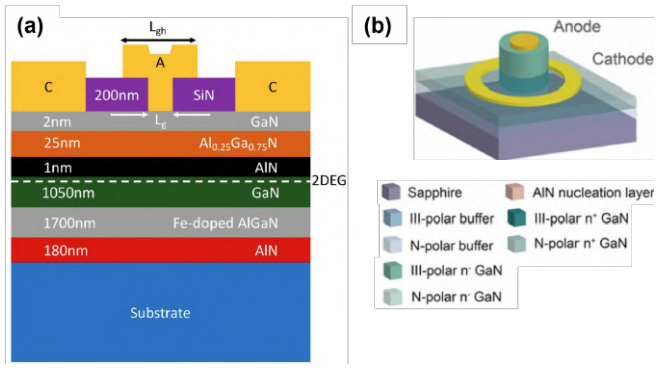

Fig. 6. Examples of GaN-based Schottky Barrier Diodes (SBDs): (a) Generic lateral SBDs [37]; (b) Quasi-vertial SBDs [38].

voltage is applied [24]. However, such characteristics raises concerns regarding a malfunctioning gate that can damage an entire system as well as design complexity due to a required negative supply voltage. Different topologies have been proposed in order to achieve normally-off (a.k.a. enhancement-mode or E-mode) GaN HEMTs, including depositing a p-doped GaN layer under the gate (p-gate) [31], using a gate recessed MIS-HEMT (metal–insulator–semiconductor) with AlGaN barrier removal [32], and implanting fluorine ions under the gate (F-Gate HEMT) [33]. Fig. 5 illustrates the schematic of each technique, while its characteristics are summarized in Table II. Essentially, the common operation of these techniques is to deplete the 2DEG layer under the gate. Apart from these intrinsic E-mode GaN HEMTs [24], incorporating low-voltage Si MOSFET in series with a normally-on GaN HEMT in a cascode configuration is another widely-used technique to realize enhancement mode operation. However, this approach adds parasitic inductance and the limitations of Si-based device. The advantages of the lateral HEMTs include the ease of fabrication, as well as their low parasitic capacitance and mature epitaxial growth on foreign substrates, such as Si and SiC. Nevertheless, the electric field and heat dissipation are confined to the device surface due to the lateral geometry, resulting in limited breakdown voltage, reduced current handling capability, and thermal management challenges under high-power operation [24].

Vertical GaN HEMTs, on the other hand, mitigate localized field and heat issues by distributing the electric field and current flow throughout the bulk of the epitaxial layers rather than confining them to the surface [24]. In this configuration, the current flows perpendicular to the substrate, and the voltage-blocking region is formed vertically within the drift layer. Such a design enables higher breakdown voltages, lower on-resistance per unit area, and superior thermal dissipation compared to their lateral counterparts [34]. Although such features make vertical GaN devices ideal for high-power applications, the vertical geometry introduces higher parasitic capacitances and longer current paths, which limit f_T and f_{max} compared with the lateral GaN HEMTs.

C. GaN-based Diodes

Beyond transistors, GaN has also enabled the realization of high-performance diodes for both power and high-frequency applications. Owing to its wide bandgap (3.4 eV) and high critical electric field (>3 MV/cm), GaN diodes can sustain large reverse biases and exhibit low leakage currents, allowing for compact, high-efficiency rectifiers, detectors, and frequency multipliers. In contrast to traditional Si- or GaAs-based diodes, GaN devices offer superior power density and thermal robustness, which are essential for mmWave and THz front ends operating under high-voltage and high-temperature conditions.

A major GaN diode architecture for THz applications is the Schottky Barrier Diode (SBD). SBDs employ a metal–semiconductor junction to achieve fast carrier transport with minimal charge storage. Their primary applications include frequency conversion functions such as rectification, detection (demodulation of amplitude-modulated signals), multiplication, and mixing. These devices can be modeled as nonlinear resistors, where the current increases exponentially with forward-bias voltage [35].

To achieve THz-level cutoff frequencies, a lateral GaN SBD, as illustrated in Fig. 6(a), is often employed because its planar configuration minimizes R_{on} and V_{on} by shortening the current

TABLE II
COMPARISONS OF LATERAL E-MODE GAN HEMT REALIZATION TECHNIQUES

Technique	Concept	Advantages	Limitations
p-GaN Gate	Inserts a p-type GaN cap above AlGaN	- Straightforward gate control - Highly scalable	- Gate leakage and thermal reliability issues - Precise etch control needed
MIS-HEMT	Locally etches AlGaN barrier under the gate (SiN, Al_2O_3, SiO_2)	- High-quality gate dielectric - Improved stability if well passivated - Highly scalable	- Sensitive to interface states - Complex etch uniformity - Precise etch control
F-gate HEMT	Implant negative fluorine ions beneath gate	- Simple process - Precise threshold voltage tunability	- Ion damage - Charge instability - Drift with temperature

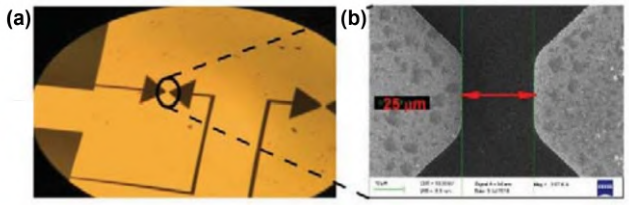

Fig. 7. (a) Optical and (b) SEM images of a GAN-based THz PCA (adapted from [40]).

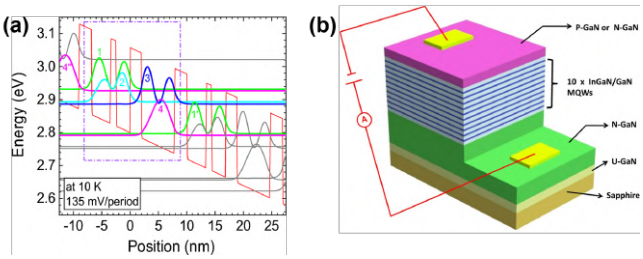

Fig. 8. (a) Intersubband diagram (adapted from [43]) and (b) the schematic structure of an InGaN/GaN THz QCL (adapted from [44]).

path and reducing parasitic capacitances. The short transit time of majority carriers in n-type GaN and the small junction area further enable high-speed rectification and detection, essential for THz mixers and detectors [36]. Notably, the lateral SBD comprises GaN epitaxial layers with a two-dimensional electron gas (2DEG) that provides a low-resistance conduction channel beneath the Schottky anode [37]. Ohmic contacts at the cathode (source) allow electrons from the 2DEG to flow laterally toward the Schottky anode under forward bias. Additionally, a mesa structure is commonly implemented to improve device isolation. In [38], a ringed mesa design was introduced to enhance the power capability of vertical SBDs (see Fig. 6(b)), forming a so-called quasi-vertical SBD. However, sidewall damage introduced during mesa etching can degrade performance [39]. Techniques to mitigate this issue are discussed in Section IV.

D. GaN Photonics for THz Applications

Several approaches have been explored for THz generation and detection through nonlinear optical processes, including photoconductive antennas (PCAs) and optical rectification (i.e. difference frequency generation). In a typical PCA, femtosecond laser excitation creates electron–hole pairs in the GaN active region, and the transient photocurrent generated under an applied bias emits broadband THz radiation. The typical structure, as illustrated in Fig. 7(a) and (b), consists of a biased bow-tie antenna with a micron-scale gap patterned on a GaN or AlGaN/GaN substrate [40]. When illuminated by a femtosecond laser pulse, photogenerated carriers are accelerated by the applied electric field across the gap, resulting in a transient photocurrent that emits a THz pulse.

The THz-to-optical power conversion efficiency can be qualitatively expressed as $\eta \propto \frac{E_{\mathrm{br}} v_{\mathrm{sat}}}{\hbar \omega_{\mathrm{opt}}}$, where E_{br} the material's breakdown electric field, v_{sat} is the saturation velocity reached under high bias electric field, and ω_{opt} is the optical excitation frequency. Owing to GaN's high v_{sat} and E_{br}, GaN-based PCAs potentially enable more than an order of magnitude improvement of THz conversion efficiency compared to GaAS- or InP-based counterparts [41]. Furthermore, GaN's strong thermal conductivity and mechanical robustness allow stable operation under higher optical fluence and bias voltages, making it particularly attractive for high-power and high-repetition-rate THz emitters.

The strong second-order nonlinear susceptibility ($\chi^{(2)}$) of GaN enables efficient optical frequency conversion through optical rectification and difference-frequency generation (DFG) processes. GaN's wide bandgap, high optical damage threshold, and strong electro-optic response have been successfully exploited in near- and mid-infrared DFG systems, such as compact tunable IR sources and frequency comb generation [42]. Although direct DFG-based generation of THz radiation in GaN has yet to be experimentally realized, theoretical studies and ongoing projects suggest that its large optical phonon energy and strong $\chi^{(2)}$ nonlinearity could support efficient THz conversion with appropriate phase-matching and material optimization.

Apart from employing nonlinear optics, intersubband engineering in GaN/AlGaN heterostructures offers another promising route toward terahertz (THz) quantum cascade lasers (QCLs) [23]. A QCL operates via electron transitions between engineered subbands within multiple quantum wells, rather than across the conduction–valence band as in conventional semiconductors. Each electron can emit multiple photons as it cascades through successive stages, enabling efficient and tunable mid-infrared and THz emission, as illustrated in Fig. 8(a) [43]. The device structure is typically formed by stacking alternating layers of a lower-bandgap semiconductor as the well and a wider-bandgap material as the barrier, as shown in Fig. 8(b). This periodic GaN/AlGaN or InGaN/GaN layer configuration allows precise band engineering essential for achieving the lasing and carrier transport characteristics of QCLs [44]. GaN-based QCLs are theoretically and experimentally shown to operate at frequencies ranging from approximately 5 to 12 THz, with some designs achieving lasing at frequencies beyond the range accessible to GaAs-based devices.

The operation of conventional THz QCLs has historically been restricted to cryogenic temperatures due to temperature-activated mechanisms such as thermally induced carrier leakage and enhanced nonradiative recombination, both of which degrade laser gain beyond a critical temperature [45]. In contrast, GaN-based THz QCLs offer the potential for room-temperature operation because GaN's high longitudinal optical (LO) phonon energy suppresses nonradiative losses and thermal backfilling, thereby supporting population inversion and optical gain at elevated temperatures. Recent studies predict or demonstrate GaN THz QCL operation at temperatures up to 280 K [43]. However, realizing high-performance GaN-based QCLs remains challenging due to difficulties in accurately controlling polarization-induced charge densities and mitigating interface roughness, which can distort the polarization charge distribution. Additionally, AlGaN/GaN quantum well

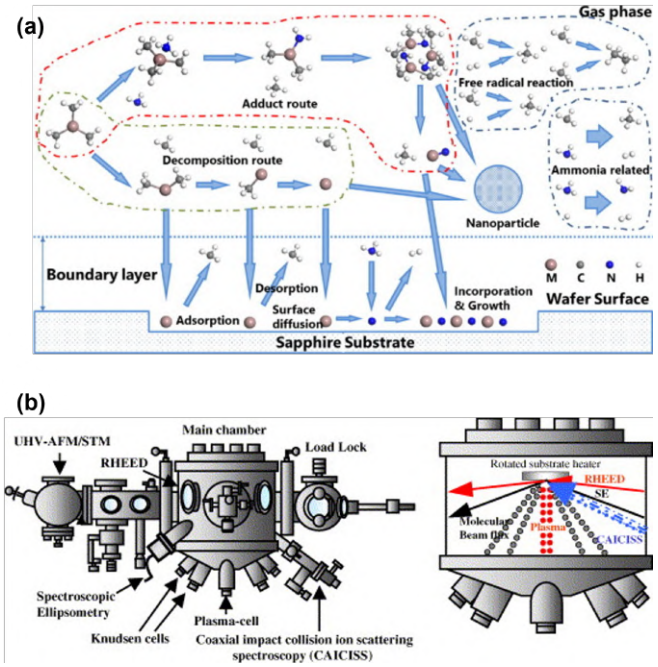

Fig. 9. (a) Chemical reaction pathway during MOCVD-grown GaN (M = metal atom, C = carbon, N = nitrogen, and H = hydrogen; adapted from [46]) and (b) Schematic diagram of MBE, with an in-situ monitoring systems, and its main chamber scheme (adapted from [48]).

structures have also been proposed for THz detection through intersubband absorption mechanisms [23].

IV. Fabrication and Process Innovations

Following the principles of GaN-based devices discussed in Sec III, it is clear that the performance of HEMTs, diodes, and photonic devices critically depends on the formation of high-quality heterojunctions. Consequently, this section discusses advances in growth techniques, substrate selection, and defect reduction of GaN devices. Moreover, this section also covers novel etching techniques crucial for vertical GaN devices.

A. GaN Growth Innovations

Epitaxial growth techniques critically determine the crystal quality, interface abruptness, and overall performance of GaN-based heterostructures. The two primary methods employed are metalorganic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE). Among these, MOCVD remains the dominant process in large-scale manufacturing owing to its capability for highly uniform film growth, high throughput, and compatibility with large-diameter substrates such as sapphire, SiC, and silicon [46]. The main chemical reactions governing GaN formation during MOCVD are illustrated in Fig. 9(a), where two competing pathways are identified: the decomposition route (green dashed line) and the adduct route (red dashed line). Growth typically begins with an AlN or low-temperature GaN nucleation layer to mitigate lattice and thermal mismatches between GaN and the underlying substrate. Careful optimization of growth parameters, such as temperature, V/III precursor ratio, and reactor pressure, has led to smooth interfaces and threading dislocation

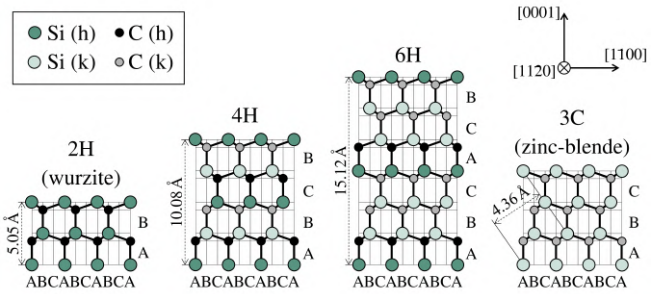

Fig. 10. Stacking sequences and inequivalent lattice sites of most common SiC polytypes viewed from the $[11\bar{2}0]$ direction (adapted from [53]).

densities on the order of 10^8 cm^{-2} [47]. In contrast, MBE is often preferred for advanced structures requiring atomic-level precision, such as quantum dots and quantum cascade lasers, where abrupt interfaces and precise doping control are essential [48]. For epitaxial regrowth processes, however, MOCVD remains favorable due to its greater flexibility in in-situ etching, masking, and planarization.

Recent advances include hybrid MOCVD–MBE growth approaches that leverage the high-temperature capability of MOCVD for buffer and channel formation, combined with the low-temperature precision of MBE for upper cladding and p-type layers. This hybrid strategy enhances heterostructure quality while reducing thermal budget constraints, particularly beneficial for complex device stacks and thermally sensitive layers [49]. In addition, growth variants such as migration-enhanced epitaxy (MEE) and pulsed precursor supply techniques have significantly improved adatom mobility and promoted step-flow growth, resulting in smoother surfaces and higher 2DEG uniformity in AlGaN/GaN heterostructures [50]. Furthermore, the introduction of hot-wall MOCVD reactors has minimized thermal gradients across the wafer, enabling superior thickness and composition uniformity in AlGaN/GaN layers on native AlN substrates. Using these techniques, state-of-the-art 2DEG mobilities exceeding 1800 cm²/V·s have been reported in high-performance GaN HEMTs [51]. Collectively, these innovations continue to push the performance envelope of GaN RF, power, and optoelectronic devices toward higher efficiency, reliability, and scalability.

B. Substrate Selection for GaN-based Devices

Due to an expensive cost and limited size of bulk GaN wafers, most GaN devices are grwon heteroepitaxially on foreign substrates. The choice of a carrier substrate involves balancing lattice and thermal expansion mismatch, thermal conductivity, cost, and scalability. Common substrates include Si silicon carbide (SiC), which offers excellent thermal conductivity and low lattice mismatch; sapphire (Al_2O_3), which is cost-effective but has larger mismatch and lower thermal conductivity; and silicon (Si), which provides large-diameter wafers and CMOS compatibility at the expense of higher lattice mismatch and lower thermal conductivity. These trade-offs directly impact dislocation density, residual stress, and device reliability, making substrate selection a critical step in GaN heterostructure fabrication.

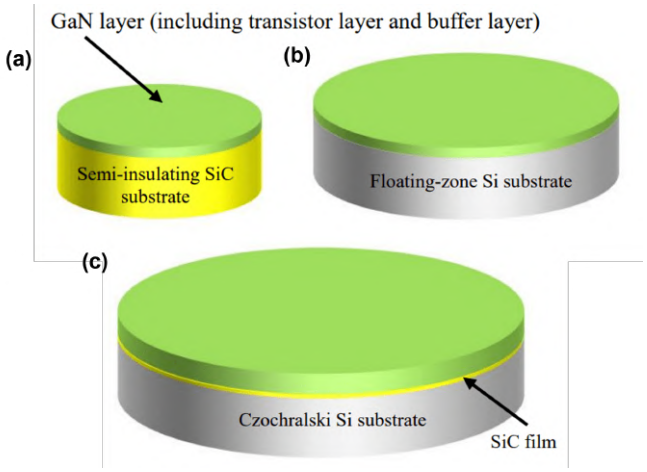

Fig. 11. Structural comparison between (a) GaN on SiC, (b) conventional GaN on FZ-Si, and (c) GaN on SiC on CZ-Si (adapted from [54]).

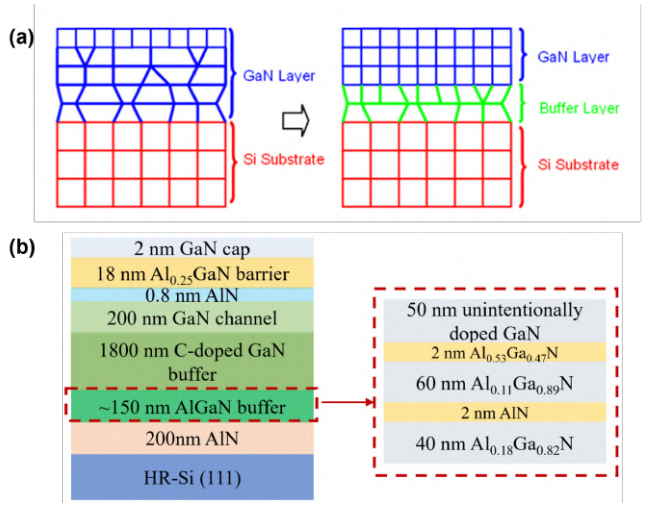

Fig. 12. (a) A role of a buffer layer underneath a GaN layer (adapted from [56]). (b) AlGaN/GaN HEMT structure with a thin AlGaN buffer layer presented in [57].

For photonic applications, sapphire is widely employed as a substrate due to its optical transparency, chemical stability, and low optical absorption across the visible to mid-infrared spectrum [52]. Although sapphire exhibits a large lattice mismatch (∼13%) and low thermal conductivity (∼35 W/m·K), it remains the substrate of choice for GaN-based optoelectronic and THz photonic devices, such as light-emitting diodes, laser diodes, and photoconductive antennas, where optical performance outweighs thermal constraints.

SiC exists in multiple stacking polytypes distinguished by their Si–C bilayer sequences along the c-axis, as illustrated in Fig. 10, each offering different electrical, optical, thermal, and mechanical properties [53]. Among hundreds of the polytypes, 4H-SiC, containing both hexagonal and cubic sites, is used almost exclusively for high-power RF GaN devices due to several advantages. Its relatively small lattice mismatch with GaN reduces threading dislocation densities compared with Si or sapphire, improving mobility, leakage, and reliability. Its high thermal conductivity (350–490 W/m·K) enables efficient heat removal from high-power HEMTs, enhancing power density, gain, and long-term stability. In addition, its thermal expansion coefficient closely matches that of GaN, minimizing wafer bow and cracking during high-temperature MOCVD growth and enabling more uniform, well-controlled epitaxial layers essential for high-performance RF devices.

The high cost and limited wafer diameter of SiC substrates (typically capped at 100 mm) restrict their use to high-end, performance-critical applications. To overcome these limitations, recent research has explored GaN high-frequency transistors grown on high-resistivity floating-zone (FZ) Si substrates, which are cheaper, widely available, and manufactured at diameters up to 150 mm [54]. Notably, FZ-Si substrates exhibit superior crystal purity and higher achievable resistivity compared to conventional Czochralski (CZ) Si wafers, making them well-suited for GaN device fabrication. However, this approach faces significant challenges, including low manufacturing yield due to the Si substrates' susceptibility to plastic deformation during thermal cycling, and energy losses arising from the deterioration of insulating properties when devices self-heat during operation. To mitigate these issues, Air Water Inc. has developed a SiC-on-CZ-Si substrate technology with large diameters up to 200 mm, which combines the thermal and mechanical advantages of SiC with the scalability and cost-effectiveness of CZ-Si [54] (see Fig. 11).

C. Defect Reduction and Dislocation Management

One of the major challenges in heteroepitaxial GaN growth lies in mitigating lattice and thermal expansion mismatches between GaN and foreign substrates, which can introduce threading dislocation densities (TDDs) exceeding 10^9–10^{10} cm^{-2} in as-grown layers [55]. These extended defects degrade carrier mobility, increase leakage currents, and compromise breakdown reliability, posing serious limitations for high-performance electronic and optoelectronic devices. Consequently, regardless of substrate choice, the use of a buffer layer is essential to accommodate lattice mismatch, suppress dislocation propagation, and improve the crystalline quality of the active GaN layer [56] (see Fig. 12(a)). Notably, the buffer layer in GaN devices are commonly made of AlN, a combination of AlGaN and GaN layers (often as a superlattice), or intentionally doped GaN [57], as shown in Fig, 12(b).

There are several techniques proposed to improve the crystalline quality of GaN epilayers above the buffer layer. The use of thin AlGaN buffer layers inserted between AlN and GaN buffers on large-diameter Si(111) substrates promotes dislocation annihilation via dislocation interactions within the initial ∼200–300 nm of the GaN buffer [57]. The incorporation of AlN or AlGaN interlayers has been also shown to significantly suppress dislocation propagation in GaN. For instance, introducing an AlN interlayer between the AlGaN and GaN buffer layers enhances 2DEG density while reducing dislocation density in both GaN and AlGaN epilayers [58]. Moreover, epitaxial lateral overgrowth (ELOG) on patterned substrates has demonstrated the ability to lower threading dislocation densities (TDDs) to approximately 4.6×10^7

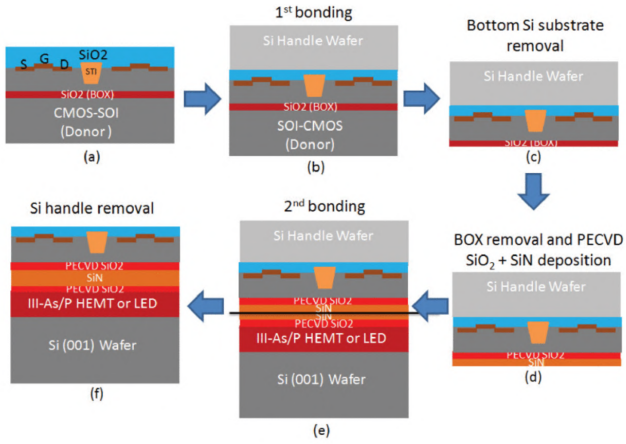

Fig. 13. Schematic of the process flow to realize the integrated CMOS + III-As/P HEMT or LED on a common Si (001) wafer. (a) Si-CMOS on a SOI wafer. (b) First wafer bonding between the Si-CMOS on SOI and a Si handle wafers. (c) Removal of the Si substrate from the SOI wafer. (d) Removal of the BOX layer and deposition of SiO2 and SiN layers. (e) Second wafer bonding between the Si-CMOS-containing handle and a III-As/P HEMT or LED wafer. (f) Removal of the Si handle to realize the integrated Si-CMOS on III-As/P HEMT or LED wafer. (Adapted from [65]).

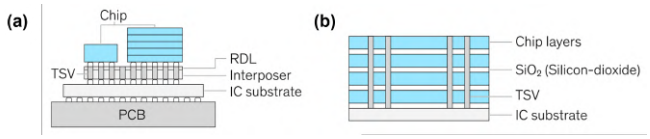

Fig. 14. (a) In 2.5D stacking, ships are directly attached on the package substrate through an interposer layer of a redistribution layer (RDL), Si bridge, through-silicon via (TSV), or glass. (b) In 3D stacking, multiple chip layers are stacked rather than laterally connected, with or without interposers, and bonded using TSV or other material such as copper. (Adapted from [66]).

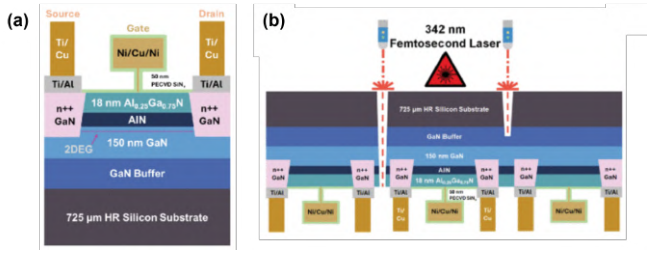

Fig. 15. (a) Epitaxial layers of a gold-free AlGaN/GaN-on-Si HEMT. (b) Backside dicing scheme using femtosecond laser in the dicing process of GaN-on-Si dielets. (Adapted from [67]).

cm^{-2} through facet-controlled lateral growth on sputtered AlN/patterned sapphire substrates (PSS) [59].

D. Etching Techniques for Vertical GaN Devices

Fabrication of vertical GaN devices requires precise etching to define mesas, isolation regions, and vertical conduction paths. Due to GaN's chemical inertness and high bond strength, dry etching techniques dominate, with inductively coupled plasma (ICP) reactive ion etching (RIE) being the method of choice [39]. Chloride-based chemistries, including Cl_2/Ar and BCl_3/Cl_2, are commonly employed as they provide high etch rates while maintaining smooth sidewalls and minimizing damage to active layers [60].

Recent advances include low-damage, high-selectivity ICP-RIE processes using multi-step etch and passivation cycles to protect sensitive surfaces and enable high-aspect-ratio vertical structures. Atomic layer etching (ALE) has emerged as a cutting-edge technique offering near-atomic-scale etch-depth control and dramatically reducing plasma-induced damage and surface roughness, which is critical for improving device performance and reliability [61], [62]. ALE enables precise layer-by-layer material removal with minimal defects and is especially beneficial for GaN or AlGaN film thickness control and selective etching in HEMT fabrication.

V. System Integration and Packaging Innovations

Despite GaN devices' exceptional power density, breakdown strength, and high-frequency performance, their system-level deployment requires efficient electrical and thermal interconnections. Conventional packaging methods, such as wire bonding on PCBs, are simple and low-cost. However, they introduce resistive and inductive parasitics that limit mmWave and THz operation, and are often labor-intensive. Emerging integration and packaging strategies address these challenges by enabling compact, low-parasitic, and thermally robust interconnects, facilitating GaN-based mmWave and THz systems in CMOS-compatible and heterogeneous platforms.

A. CMOS-Compatible Techniques for GaN Device Integrations

The realization of large-scale GaN-based mmWave and THz systems increasingly relies on HI with mature CMOS platforms, which provide high-density signal routing, advanced control circuitry, and cost-effective wafer-scale processing. GaN-on-Si and GaN-CMOS co-integration approaches have emerged as promising pathways to combine GaN's high-power, high-frequency performance with the integration density and yield of silicon electronics [63], [64]. Direct wafer bonding has become one of the most effective methods for integrating GaN with CMOS circuits. For example, monolithic integration of Si-CMOS with III-V-on-Si through direct wafer bonding, as illustrated in Fig. 13, has enabled high-performance transistors with excellent interface quality while remaining compatible with standard back-end-of-line (BEOL) processes [65]. This approach avoids the thermal mismatch and contamination challenges often encountered in sequential GaN epitaxy on Si substrates.

Nevertheless, in practical GaN/CMOS implementations, the active GaN device area is typically much smaller than the surrounding Si CMOS BEOL interconnect area, resulting in low wafer utilization. To address this, recent strategies focus on fabricating GaN HEMTs as small, integration-ready chiplets (or dielets) that can be efficiently co-packaged with CMOS circuitry, maximizing wafer usage and system performance [66]. This approach leverages 2.5D and 3D integration (see Fig. 14), where GaN chiplets are mounted on interposers or interconnected via through-silicon vias (TSVs) to achieve high-density, low-parasitic connections with CMOS layers. Chiplets are pre-fabricated, compact GaN HEMT blocks optimized

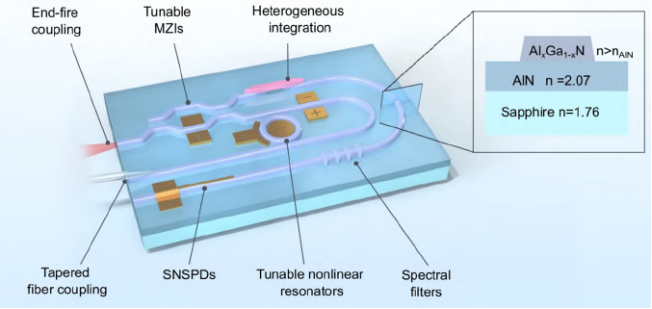

Fig. 16. Illustration of an AlGaN/AlN photonic platform (adapted from [68]).

for performance and yield. Additionally, this methodology benefits from design-technology co-optimization (DTCO) and system-technology co-optimization (STCO), bridging front-end-of-line (FEOL) and back-end-of-line (BEOL) building blocks to enable high-performance heterogeneous mmWave and THz systems.

To enable low-cost, large-scale production, gold-free integration process is required. To address this, metalization of GaN FEOL fabrication must be CMOS-compatible materials, such as Cu. Fig. 15(a) shows the schematic diagram of a gold-free GaN HEMT dielet, in which non-alloyed Ti/Al metal contacts and a Cu T-gate are utilized [67]. These dielets can be interfaced with the BEOL package via Cu-Cu thermocompression bonding. For wafer singulation, femtosecond laser dicing from the backside of the substrate, as depicted in Fig. 15(b), preventing the dielets from debris [67].

B. Integrated Photonic Circuits and Interconnects

For operation beyond 1 THz, photonic platforms offer low-loss, ultra-wideband solutions. Similar to electronic ICs, photonic integrated circuits (PICs) consist of a variety of active and passive components. Beyond the THz photonics discussed in Sec. III, numerous GaN-based components, such as Mach-Zehnder interferometers (MZIs), directional couplers, and microring resonators, can be interconnected via photonic waveguides, as illustrated in Fig. 16, to implement specific functionalities. In [68], AlGaN ridge waveguides on an AlN–sapphire platform were investigated, demonstrating low propagation loss and strong optical confinement, which enables efficient integration of active and passive devices on a single chip. Being GaN-compatible, such platforms allow combining modulators, splitters, detectors, and nonlinear GaN elements to perform on-chip frequency conversion, routing, and signal processing for mmWave and THz applications. For example, integrating these PICs with conventional electronic systems facilitates compact, broadband photonic beamforming [69], [70], as well as chip-scale interfaces between high-speed optical links and electronics in data centers and 5G/6G base stations. Nevertheless, significant research is still required to realize fully functional GaN photonic chiplets for practical system-level deployment.

C. Advanced Packaging Technologies

Emerging 2.5D and 3D HI technologies are becoming essential for realizing high-performance GaN-based mmWave

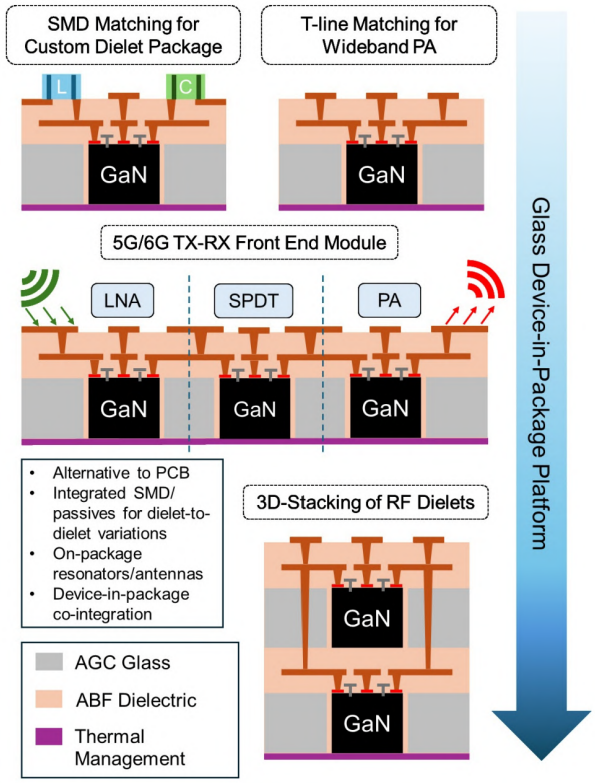

Fig. 17. Device-in-Package glass integration platform for RF GaN dielets (adapted from [68]).

and THz systems. By stacking or co-packaging GaN HEMTs, CMOS control circuits, and photonic modules, 3D HI can overcome footprint limitations, reduce parasitic interconnects, and enhance system-level performance. The design of such systems requires careful consideration of substrate selection, as it affects mechanical stability, thermal conductivity, and RF signal integrity. Electrical design must minimize parasitic resistance, capacitance, and inductance, particularly at mmWave and THz frequencies, while thermal management strategies, such as including heat-spreading interposers and through-substrate vias, are critical to ensure reliability and maintain device performance under high-power operation.

Recent advances in 3D HI increasingly leverage novel substrate and interposer technologies to optimize electrical, thermal, and mechanical performance. For mmWave and THz applications, glass substrates have become attractive platforms due to their low dielectric loss, excellent surface planarity, high thermal stability, and more importantly customizable properties during manufacturing processes [71]. Fig. 17 illustrates the HI of GaN dielets with in-package components, such as through-glass interconnects and antennas, in a glass housing. Notably, continued progress in co-design and co-modeling approaches that link multiple physical domains, including electrical, mechanical, and thermal, is required for high performance, highly-packed mmWave and THz HI systems. Furthermore, advanced additive manufacturing materials and techniques are yet to be explored to enable large-scale, cost effective fabrication and assembly.

VI. Conclusion

This paper reviews recent advancements in full-stack GaN technologies for emerging mmWave and THz applications. It provides a comprehensive overview of GaN-based electronics, focusing on HEMTs and diodes, as well as THz photonics, highlighting key innovations in device fabrication processes. Furthermore, the paper discusses promising heterogeneous integration and advanced packaging techniques that have the potential to transform the design and performance of next-generation mmWave and THz systems.

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