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TEXAS
The University of Texas at Austin

DESIGN OF TWO-STAGE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Lessons learned by an inexperience designer

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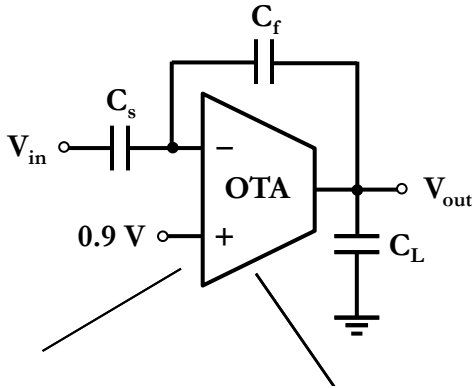
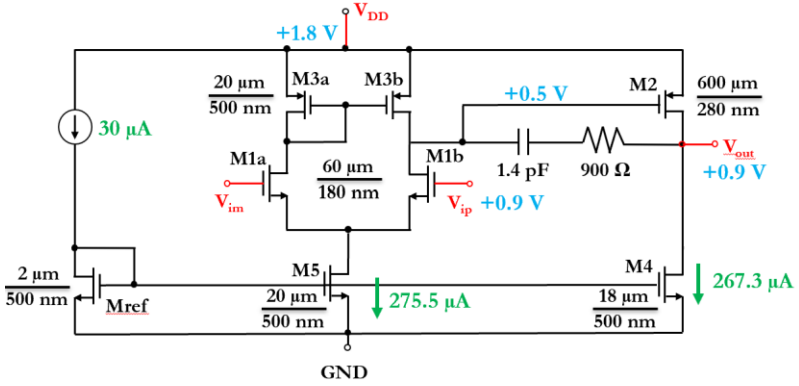
Foreword

This presentation slide contains lessons learned from the final project design of ECE382M. It briefly summarizes both good and bad things that I received during the hard time working on this project. They were all indeed great experiences that I will never forget. It truly showed me how important hands-on experiences are and how much we can learn from mistakes and failures. As an inexperience newbie in IC design, I would like to first extend my heartfelt gratitude to everyone whoever supported me during the project—whether directly or indirectly. I would also like to express my sincere appreciation to the course instructors and staff for creating such a practical and enriching learning environment.

Talking about the project itself, this presentation slide will begin with the overall performance of my two-stage OTA. It will then briefly walk through the rationale behind my design decisions and how I addressed each challenge I encountered. Then, the results from every testbench will be presented and shortly discussed. Finally, results from each testbench will be presented and briefly discussed before concluding the report.

Design Summary

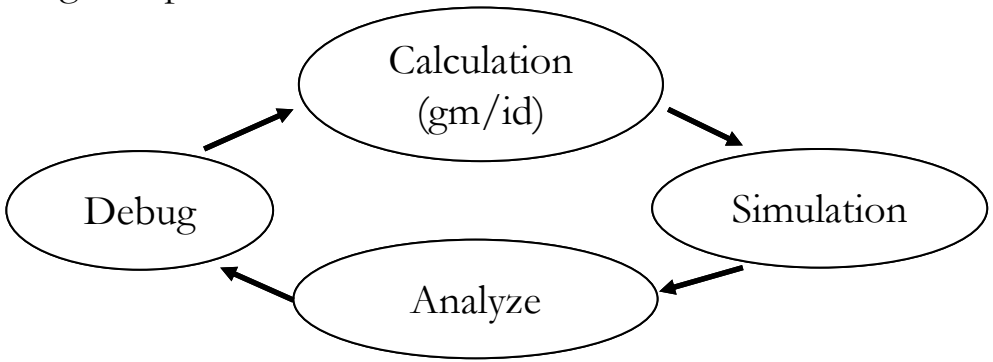


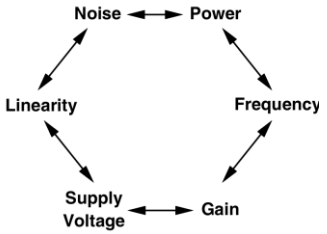


		Specs	Results
Values for C_1, C_2, and C_L		$C_1 = C_2 = C_L = 1$ pF	
Static settling error		≤ 0.1%	≤ 0.1%
Dynamic settling error		≤ 0.1%	≤ 0.1%
Output swing		[0.3, 1.5]	[0.299, 1.515]
Output common mode voltage		0.9 V	0.9 V
Input common-mode range (Vic)			[0.628 1.55]
OTA open-loop DC small signal gain (A_{dm})			67.87 dB
Loop gain at low frequency (βA_{dm})			67.83 dB
Loop gain unity gain frequency			110.44 MHz
Loop gain phase margin (PM)		> 60°	61.89°
Settling time	Up	< 45 ns	27.4 ns
	Down	< 45 ns	10.85 ns
CMRR at DC		> 65 dB	81.83 dB
PSRR at DC		> 65 dB	72.01 dB
Total output noise consumption (RMS value)		≤ 300 µV	185 µV
Power consumption			1.031 mW

Design Procedure Overview

1. Consider the given **constraints:**
   - All the stringent performance requirements
   - Other factors, e.g. time and experience
2. Determine **the right starting point** that is most suitable with the constraints:
   - Compare potential topologies
   - Ideate some possibilities
   - Characterize the technology (180 nm)
3. Design loop start here!

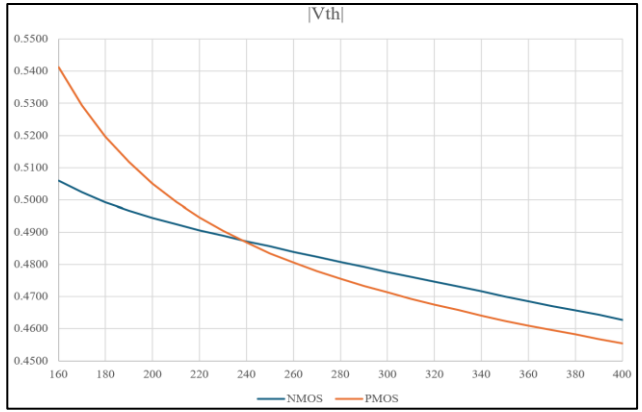




cadence

	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-Stage	High	Highest	Low	Medium	Low
Gain-Boosted	High	Medium	Medium	High	Medium

Razavi 2017



Vth of 180nm tech. vs. transistor length

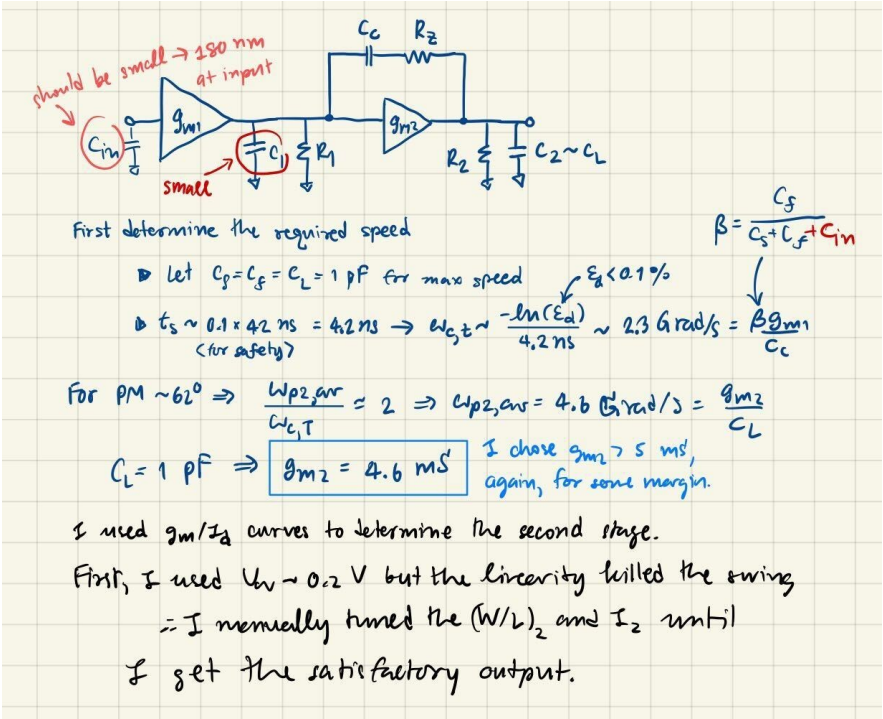
Why a two-stage OTA?

Given stringent requirements, especially on the output voltage swing, a simple two-stage topology was chosen due to its moderate overall performance and design flexibility that could be limited in single-stage OTAs. Initially, I planned to use a telescopic cascode as the first stage, followed by a common-source "swing" stage to improve its limited output swing. However, due to a strict timeline and the steep learning curve as a beginner, I decided to first design a functional, generic two-stage OTA to mitigate risk. I intended to later compare its performance with that of the telescopic design. Unfortunately, I made a critical mistake that significantly affected my progress, allowing me to barely complete the generic version. I will discuss this issue in more detail later.

The key components of the generic single-ended OTA are:

1. Differential-single ended stage (diff pair with active loads)
2. Second CS stage
3. Compensation
4. Current reference

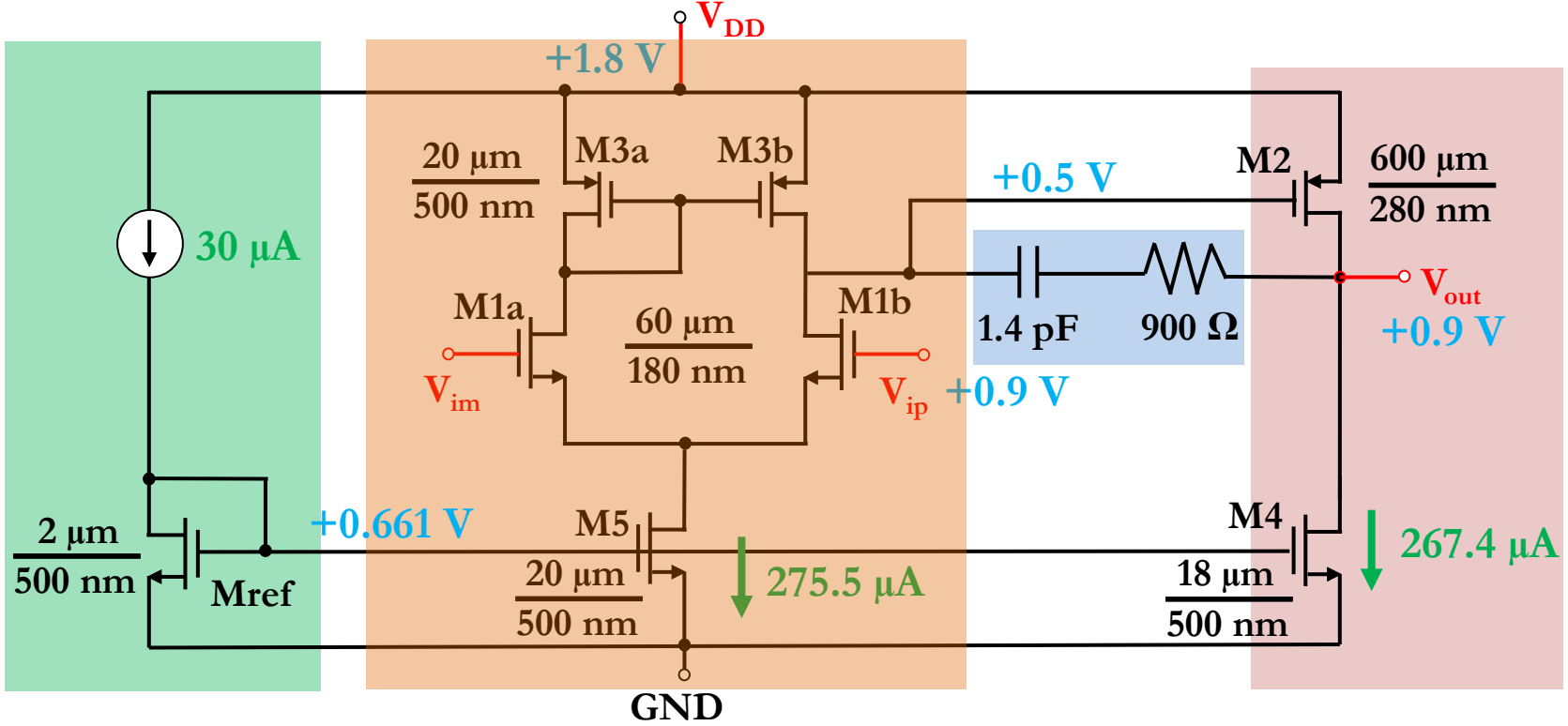
Two-stage OTA calculation



After several attempts, I realized that relying solely on calculations did not yield satisfactory performance, especially under strict design requirements. Therefore, instead of fully calculating all parameters before simulating, I adopted a more iterative approach: estimating initial values for each stage and then tuning them through simulation until achieving acceptable performance.

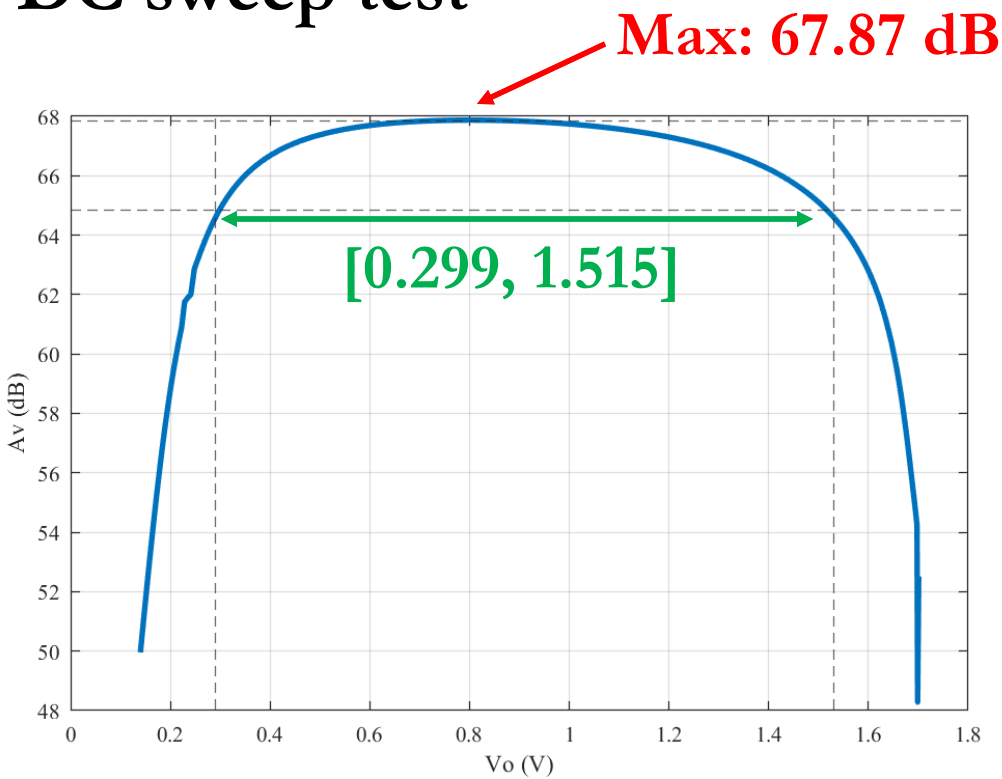
In this case, I got (W/L)s for the second stage from the simulation first and used these parameters to calculate for the next stage. The sweepings in Cadence were performed after each calculation to get the right values.

Two-stage OTA design parameter summary

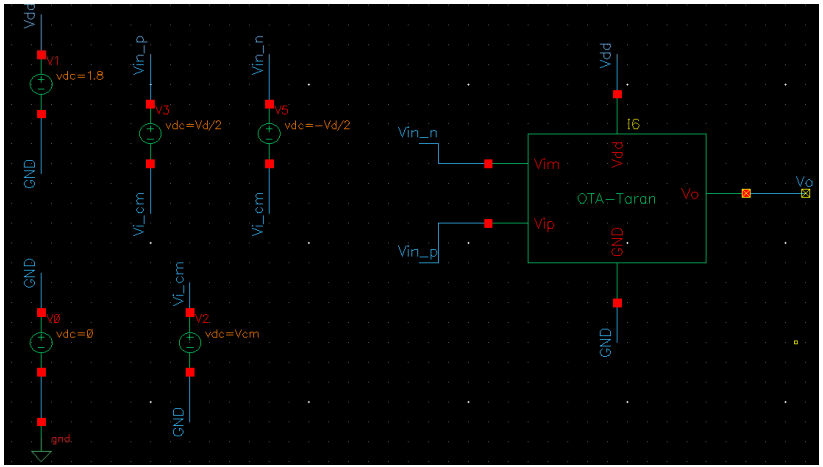


Total current: 572.9 µA → **1.031 mW**

DC sweep test



Skewed profile due to nonlinearity as M2 has very high gm/Id



By sweeping the range of Vcm, we can get the common-mode range, where the gain becomes maximum. However, I differently did that be sweeping Vcm in AC analysis and measured its DC gain at different Vcm and got [0.628 1.55].

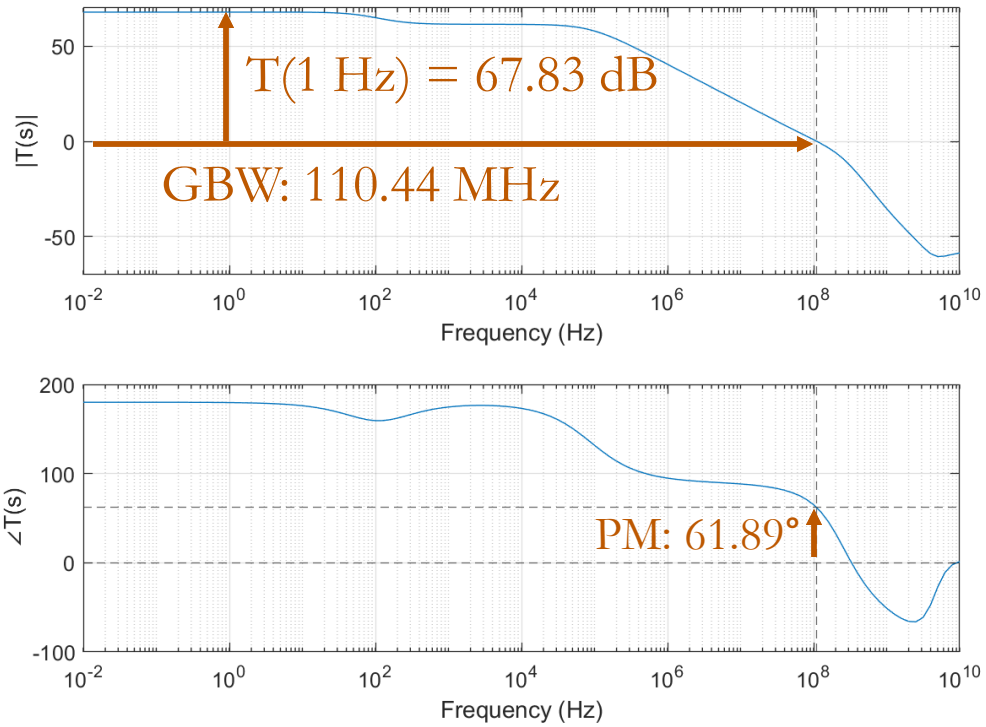
Comments on achieving a wide swing

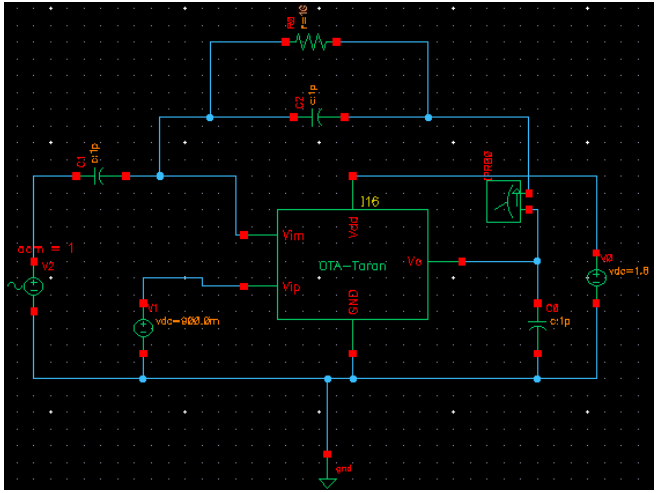
In the very first design cycles, I couldn't get the high-end swing of 1.5 V due to the skewed output profile even I pushed Vov of the second stage to be lower than 0.2 V. To understand such behaviors, I carefully examined the operating point of the CS stage and found that:

- The W/L of M2 must be high enough to get into a weak inversion region in order to have lower Vov. I once tried to operate M2 in a subthreshold region, but the situation became worse. Therefore, M2 should be carefully place somewhere in between triode and subthreshold regions
- The sizing of M2 and its NMOS current source must be chosen properly, as the output impedance of MOS at a transition between saturation and triode regions, and this will be more pronounced if the NMOS has high enough output impedance.

As the swing determines the very first step into the design according to my procedure, it will be easier (to me) to set the swing, and, indeed, Vout of the first stage.

Loop Gain and Stability

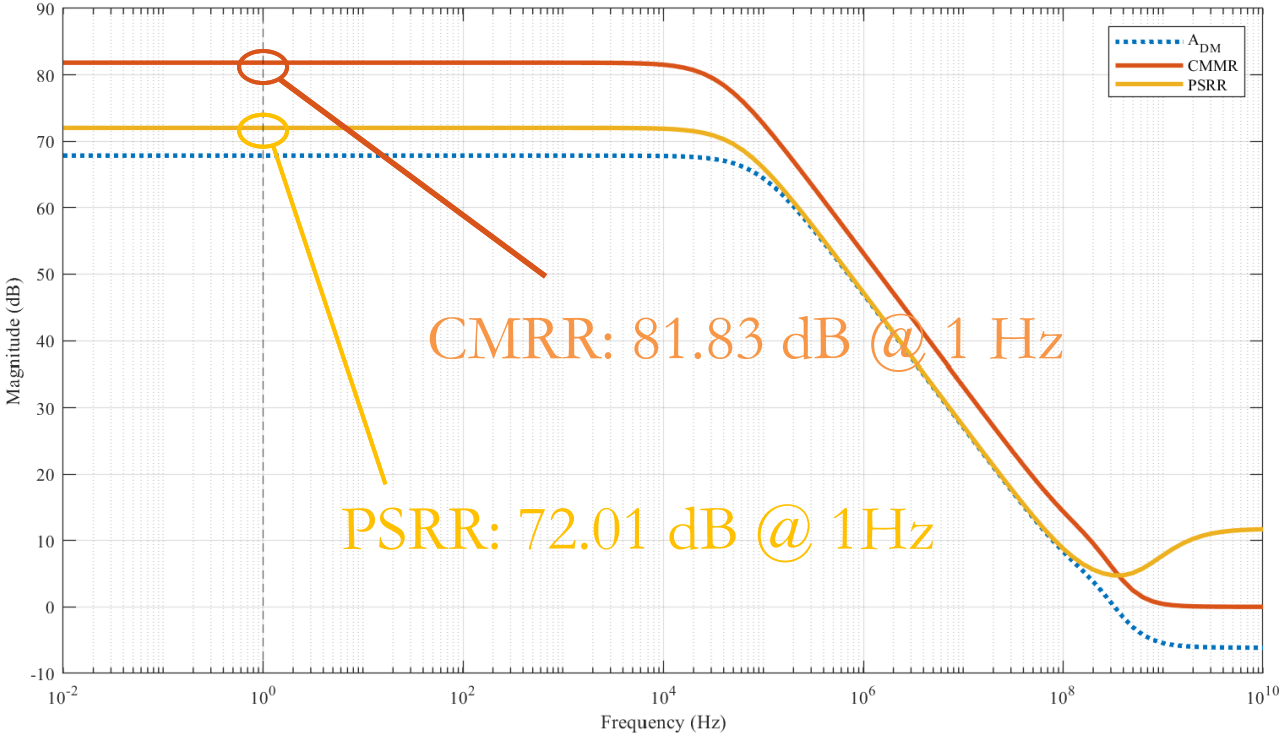


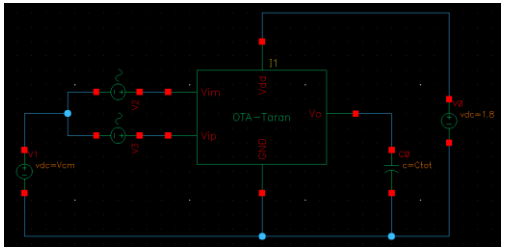


$C_c = 1.4$ pF (calculated: 1 pF)

$R_z = 900\ \Omega\ (>1/g_{m2})$

Frequency Response (Rejections)

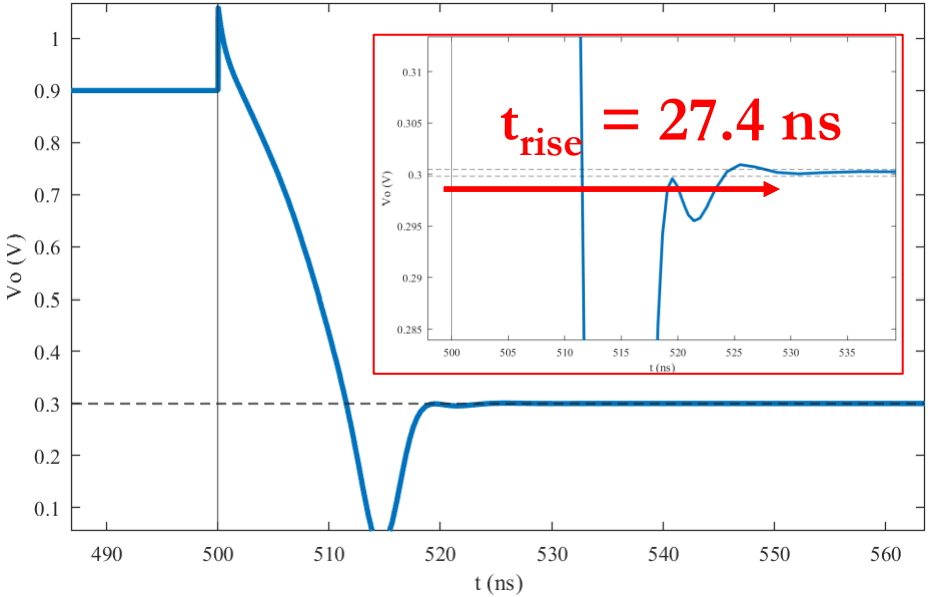


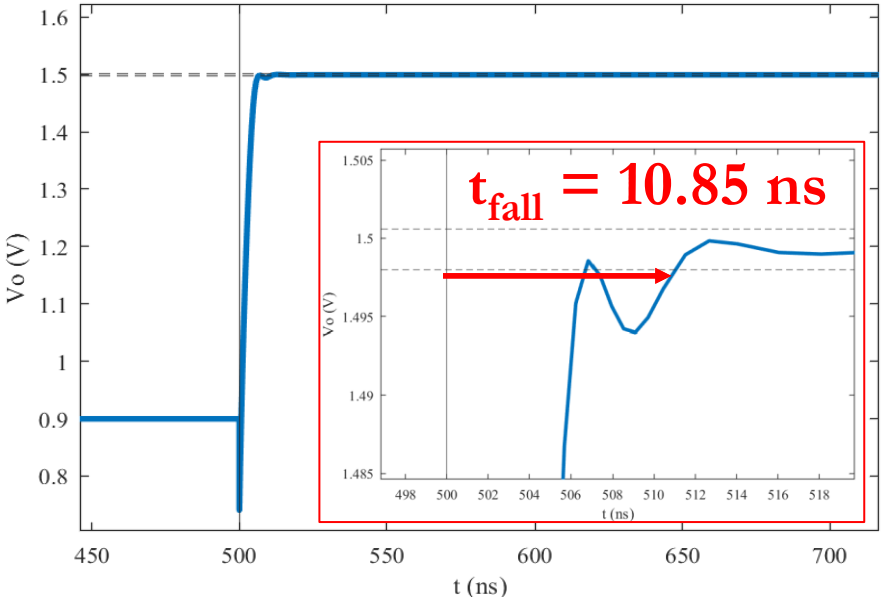


Three different output voltage gains referred to differential mode, common mode, and source fluctuation were simulated and calculated as follows:

- CMRR = Adm/Acm
- PSRR = Adm/Add

Transient Responses





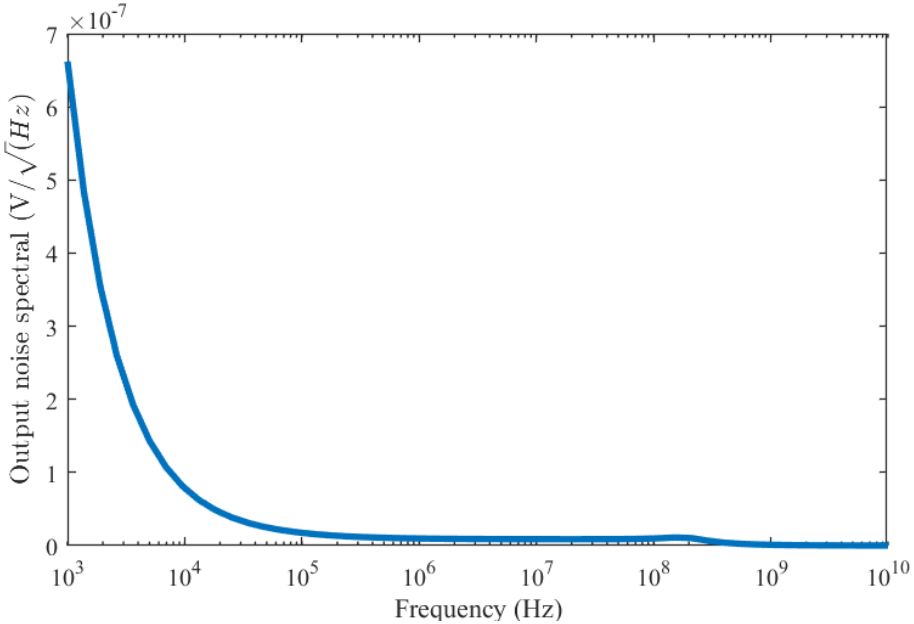
$$\varepsilon_0 = \left|\frac{0.300236 - 0.3}{0.3}\right| = 0.00078 < 0.1\%$$

$$\varepsilon_d(45\text{ ns}) = \left|\frac{0.300237 - 0.300236}{0.300236}\right| < 0.1\%$$

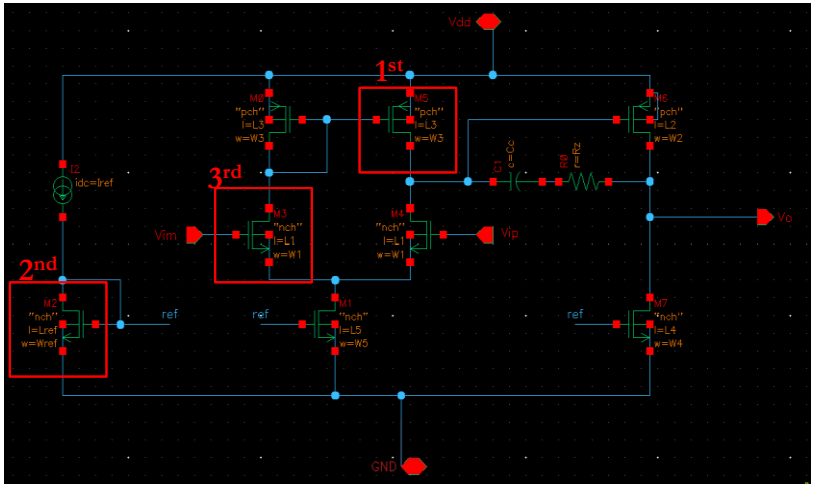
$$\varepsilon_0 = \left|\frac{1.49915 - 1.5}{1.5}\right| = 0.00057 < 0.1\%$$

$$\varepsilon_d(45\text{ ns}) = \left|\frac{0.149913 - 1.49915}{1.49915}\right| < 0.1\%$$

Noise



Even the stage two has relatively high gain, the first stage were designed to avoid excessive noise



/I12/M5	id	7.76844e-05	17.57
/I12/M2	id	7.31271e-05	15.57
/I12/M3	id	6.88476e-05	13.80
/I12/M0	id	6.4196e-05	12.00
/I12/M6	id	6.37273e-05	11.82
/I12/M4	id	6.26835e-05	11.44
/I12/R0	rn	5.19288e-05	7.85
/I12/M7	id	4.52183e-05	5.95
/I12/M1	id	2.59917e-05	1.97
/R0	rn	2.1003e-05	1.28

```
Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.000185331
No input referred noise available
The above noise summary info is for noise data
```

The "unforgiveable" mistake

During the final two weeks of this project, I struggled with issues related to phase margin (PM) and frequency response that I couldn't resolve despite numerous attempts. At the time, I believed the problem stemmed from poor design choices that introduced undesirable poles into the system. Since I had used relatively wide transistors, I suspected their impractical size was causing large parasitic effects within the OTA. I read countless discussion forums and even consulted ChatGPT, but I consistently ended up with severely negative phase margins. I also examined the gain of each stage to identify the source of the issue, but nothing stood out.It wasn't until the last day—when I had nothing ready to present and was feeling desperate—that I decided to look at both the magnitude and phase of each stage's gain individually. That's when I noticed that the first stage had a 0-degree DC phase, which led me to realize that I had mistakenly swapped the positive and negative inputs from the very beginning when drawing the template schematic. After correcting this error, all of my previous designs started working reasonably well. However, by then it was too late to further optimize them or explore alternative designs, as I had originally hoped to do.

Positive feedback ruined everything.

Potential Improvement and Conclusions

- For the current design the current can be carefully reduced to achieve better power consumption. Nevertheless, this will potentially reduce the slew rate, especially in the first stage that can drastically slow down the OTA.
- Different topologies should be investigated more. For example, using a telescopic cascode in the first stage to boost the gain and speed of the two-stage OTA. I've found the old work from this class, published on ResearchGate, which presented a fully differential OTA design using a telescopic first stage and a class AB output stage to optimize performance under low power conditions (252 uW). This work is both impressive and highly insightful, though it remains well beyond my current level of knowledge and experience.
- To summarize, this project truly broadened my expertise and pushed me beyond my comfort zone to explore a new field. I learned many new concepts and also gained experience in managing stress—particularly during the intense final exam week. Although the project didn't turn out exactly as I had hoped, I genuinely enjoyed the process. I'm confident that the knowledge and skills I gained will be valuable in the future, especially as systems continue to become more integrated.