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END-TERM EXAMINATION (2023-24)

Branch: CSE **Subject Code: CS203CA** **Subject: Computer Architecture** **Semester: 4th**
Instructor Name: Dr. Vinay Kumar **Max Marks:50** **Duration: 2 Hrs.** **Date:13-05-2024**
Attempts all questions.

Question 1: Choose the correct alternatives for the following:

i Which of the following is not the cause of possible data hazard?
a) RAR b) RAW c) WAR d) WAW

ii A direct mapped cache memory with n blocks is nothing but which of the following set associative cache memory organizations?
a) 0-way set associative b) 1-way set associative c) 2-way set associative d) n-way set associative.

iii A pipeline stage is
a) sequential circuit b) combinational circuit
c) consists of both sequential and combinational circuits d) none of these

iv The CPU time needed to execute the program is estimated by finding the product of
a) Instruction counts, Cycles per Instruction b) Instruction counts, Cycles per Instruction, cycle time
c) Instruction counts, Cycles per Instruction, frequency d) Instruction counts, frequency, cycle time

v The reciprocal of the clock period is called
a) Throughput b) Efficiency c) Frequency d) None of the above

vi Ideally, a linear pipeline with k stages can process n tasks in _____ clock periods.
a) k-(n+1) b) k*(n-1) c) k+(n+1) d) k+(n-1)

vii Which of the following statements is/are TRUE?
i. RAW data hazard could be reduced by operand forwarding.
ii. A normal in-order 5 stage MIPS pipeline can achieve an IPC larger than 1.
iii. For a MIPS instruction STR R2, 16(R3), some contents stored in its ID/EX pipeline register will bypass the EX-unit directly to EX/MEM pipeline register.
iv. A normal 5 stage in order RISC pipeline without operand forwarding can have RAW and WAR hazards.
a) I only b) I & III only c) II & IV only d) III & IV only

viii Which of the following statements is/are FALSE?
i. In a dynamic scheduled processor, every execution unit writes the result and the name of the reservation station waiting for the result on to the CDB.
ii. In a speculative dynamic scheduled processor, we can issue an instruction if there is an empty reservation station even though operands are not available.
iii. If the register status indicator value of the register is 0, then it means the operand is available in Register File.
iv. In a dynamic scheduled pipeline instructions are issued in order, executed out of order, completed out of order, and committed in order.
a) I only b) I & II only c) II & IV only d) III & IV only

ix What will be the speedup for a 4-segment linear pipeline when no. of instructions n= 64?
a) 4.5 b) 3.82 c) 8.16 d) 2.96 e) None

x Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Then the maximum clock frequency of pipeline is
a) 100 ns b) 90 ns c) 190 ns d) 30 ns

[10X1 = 10]

Question 2: Attempt all questions in brief.

i What is the difference between Computer Organization and Computer Architecture?

ii What are the different approaches taken by pipeline processors to handle branch instructions? Briefly illustrate any two approaches.

iii What do you mean by cache coherence problem? Describe one method to remove this problem and its limitations.

iv What is Instruction Level Parallelism?

v What is loop unrolling? What are the advantages of loop unrolling?

[5X3 = 15]

Question 3:

a) What is dynamic scheduling. List the advantages of dynamic scheduling.

b) Briefly explain how to overcome data hazards with dynamic scheduling using Tomasulo's approach.

[3+7]

Question 4: A program has 2000 instructions in the sequence L.D, ADD.D, L.D, ADD.D,..... L.D, ADD.D. The ADD.D instruction depends on the L.D instruction right before it. The L.D instruction depends on the ADD.D instruction right before it. If the program is executed on the 5-stage pipeline what would be the actual CPI with and without operand forwarding technique?

[5]

Question 5:

a) A computer has 512kB cache memory and 2 MB main memory. If the block size is 64 byte then find subfields for all three types of cache mapping techniques.

b) A cache memory that has a hit rate of 0.8 has an access latency of 10 ns and miss penalty 100 ns. Optimization is done on the cache to reduce the miss rate. However, the optimization results in an increase of cache access latency to 15 ns, whereas the miss penalty is not affected. What is the minimum hit rate (rounded off to two decimal places) needed after the optimization such that it should not increase the average memory access time?

[4+6]

**********ALL THE BEST**********