Open source 25-core processor can be stringed into a 200,000-core computer

Researchers at Princeton University have built a 25-core chip that can scaled easily to create a 200,000-core computer
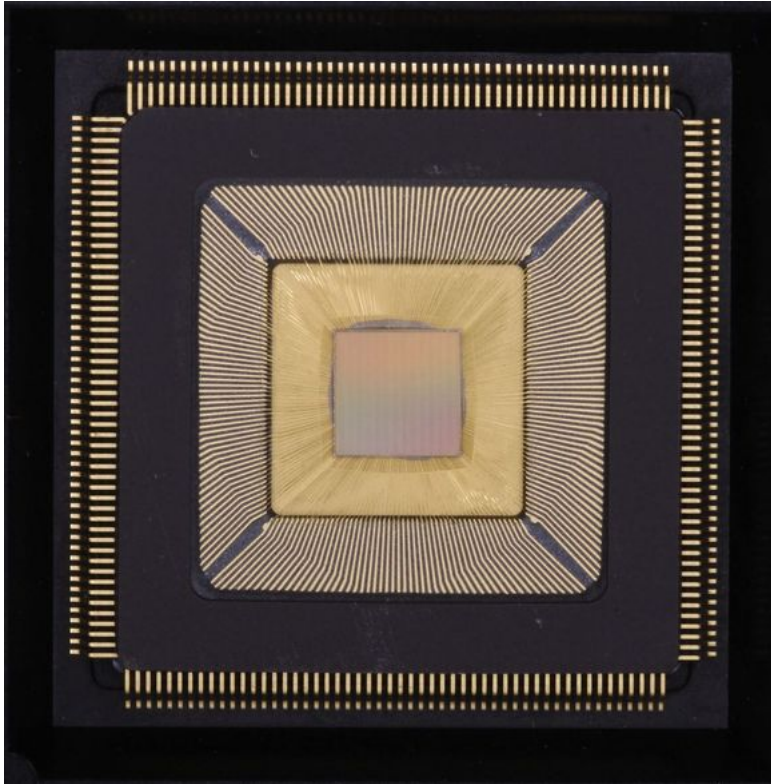
Princeton University's Piton processor has 25 cores, and is based on an OpenSparc design. Credit: Princeton University

4   COMMENTS

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IDG News Service

Researchers want to give a 25-core open-source processor called Piton some serious bite.

The developers of the chip at Princeton University have in mind a 200,000-core computer crammed with 8,000 64-bit Piton chips.

It won't happen anytime soon, but that's one possible usage scenario for Piton. The chip is designed to be flexible and quickly scalable, and will have to ensure the giant collection of cores are in sync when processing applications in parallel.

Details about Piton were provided at the Hot Chips conference this week. The goal was to design a chip that could be used in large data centers that handle social networking requests, search and cloud services. The response time in social networking and search is tied to the horsepower of servers in data centers.

Piton is a rare open-source processor based on the OpenSparc design, which is a modified version of Oracle's OpenSparc T1 processor (http://www.oracle.com/technetwork/systems/opensparc/opensparc-t1-page-1444609.html).

Many open-source CPUs and architectures are already being designed. A notable architecture under development is RISC-V, which is being used by SiFive (https://www.sifive.com/) to design a new processor. Some open-source processor designs are for fun. For example, Open Core Foundation is trying (http://www.pcworld.com/article/2464620/nonprofit-to-bring-sega-game-console-chips-back-to-life.html) to provide an open-source design for the SH2 processor, which was in Sega's 1994 Saturn gaming console.

Companies can take the open-source designs, tweak them, and fabricate chips in factories. Alternately, the chip can be simulated by putting the programmable logic on FPGAs (field-programmable gate arrays), which will then mimic the functionality of the multi-core CPU.

It's interesting that the researchers chose SPARC as the architecture of choice for it's design. SPARC is used by Oracle in its high-end servers designed for databases, but the popularity of the architecture is waning. Fujitsu recently said (http://www.pcworld.com/article/3086249/fujitsu-drops-sparc-turns-to-arm-for-post-k-supercomputer.html) it was booting SPARC in favor of ARM for servers, specifically for the Post-K supercomputer it will deploy in Japan in 2020.

One Piton chip has 25 cores broken up in five lines, a topology widely referred to as a mesh design. Each core operates at 1GHz. Multiple chips in an array can be daisy-chained system through a "bridge" that sits on top of the chip structure. The bridge also links the chip to DRAM and storage.

The mesh design isn't a new idea as it has been used in chips from companies like Tilera, which is now a part of Mellanox. But what's unique about Piton is the distributed cache and unidirectional links that would pull all cores together in a large server. The cores also share memory.

Each core has 64KB of L2 cache, totaling 1.6MB for the chip. A mini-router in each core facilitates fast communication with other cores. Each core also has a floating point unit, mostly for large-scale parallel computing.

The core count in CPUs is climbing—especially in server and gaming chips—to provide more computing horsepower. AMD's upcoming Zen-based chips will have up to 32 cores, while Intel's latest Xeon E7 server chips have up to 24 cores.

The Princeton researchers claim Piton to be the largest chip in academia. That claim cannot be based on the number of cores in the chip. A 1,000 core chip called KiloCore (http://www.pcworld.com/article/3085502/components-processors/meet-kilocore-a-1000-core-processor-so-efficient-it-could-run-on-a-aa-battery.html) has been designed by researchers at the VLSI Computing Lab at University of California, Davis.

But the 460 million transistors could make Piton the largest chip developed by academia in size. It is small though compared to today's beefier server and gaming chips with billions of transistors. The researchers fabricated Piton using IBM's 32-nanometer process.

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