Verilog Testbench Code:

```
‘timescale 1ns/1ns
module testbench;
    reg clk;
    reg rst;
    reg [3:0] f_req;
    reg [3:0] c_req;
    wire [3:0] request;
    wire [1:0] current_floor;
    wire direction;
    wire door_open;
    elevator_controller test_instance (
        .clk(clk),
        .rst(rst),
        .f_req(f_req),
        .c_req(c_req),
        .request(request),
        .current_floor(current_floor),
        .direction(direction),
        .door_open(door_open)         );
    initial begin
        // Generate a continuous clock signal with a 10 ns period
        clk = 0;
        forever #5 clk = ~clk;
    end
    initial begin
        $dumpfile("dump.vcd");
        $dumpvars(0, testbench);
        // Activate reset and initialize request signals
        rst = 1;
        f_req = 4’b0000;
        c_req = 4’b0000;
        #20 rst = 0;
        // Simulate a floor request for the highest floor
        f_req = 4’b1000;
        #10 f_req = 4’b0000;
        #100;
        c_req = 4’b0010;
        #10 c_req = 4’b0000;
        #100;
        c_req = 4’b0100;
        #10 c_req = 4’b0000;
        #100;
        f_req = 4’b0001;
        #10 f_req = 4’b0000;
        #100;
        // Terminate the simulation after test cases are complete
        #50 $finish;
    end
endmodule
```

WaveForms Result: