Modifier 9.0 – Digital IC Design Hackathon

Welcome to the Challenge!

Ready to build something awesome? In **Modifier 9.0**, you'll design a **PWM/Timer Module** using **Verilog** and **QuestaSim** that powers things like motors or IoT devices. It's your chance to show off your digital design skills in just 48 hours! Stick to the basics if you're new, or add cool features for extra points if you're a pro.

Main Challenge:

Design a **PWM/Timer Module** with a Wishbone interface based on **PWM_UM.pdf**. Your design must:

- **PWM Mode:** Generate a PWM signal with adjustable Period and Duty Cycle (DC).
- **Timer Mode:** Trigger an interrupt when the Main Counter hits the Period value.
- **Down Clocking:** Divide the clock using a 16-bit Divisor register (off if Divisor=0 or 1).
- **Wishbone Interface:** Read/write registers (Ctrl, Divisor, Period, DC).
- **Single Clock Domain:** Run on a 50 MHz clock.

Optional Features (for Extra Points):

- **Multi-Channel PWM:** Support up to 4 PWM outputs with separate Period and DC.
- **Error Handling:** Handle issues (Invalid cases) like DC > Period or invalid Divisor.
- **Multi-Clock Domains:** Handle two clocks (e.g., 50 MHz internal, external clock) without glitches.

Rules:

- Use **Verilog** only. No VHDL.
- Simulate with **QuestaSim**. Show results with waveforms.
- Starts: **Sunday, July 27, 2025, 12:00 PM**.
- Ends: **Tuesday, July 29, 2025, 12:00 PM** (48 hours).
- Late submissions lose 5% per hour.

- Stick to the names of the ports in the **PWM_UM.pdf.**
- Core design uses one clock Domain. Multi-Clock domain is optional.
- No technical questions during the hackathon. Non-technical questions via email or the whatsapp group.

Deliverables

Submit a **RAR file** named <Your_Team_Name>.rar (e.g.,TeamOne.rar) with:

1. **Verilog Files:**
    - pwm_timer.v: Main module with core features (and optional ones if added).
    - pwm_timer_tb.v: Testbench checking:
        - PWM output (Period, DC).
        - Timer Mode interrupts.
        - Down Clocking (Divisor=2, Divisor=10).
        - Wishbone read/write.
        - Optional features if added.
    - Code must be clear and commented.
2. **QuestaSim Do File:**
    - pwm_timer.do: Script to run simulation and show the signals.
3. **Simulation Results (PDF):**

<Your_Team_Name>_Simulation_Results.pdf with:

- Waveform screenshots from QuestaSim showing **these specific cases**:
    - PWM output for DC=50% and DC=25% of Period.
    - Timer Mode interrupt generation and clearing.
    - Down Clocking with Divisor=2 and Divisor=10.
    - Wishbone read/write operations.
    - Optional features if added.
- **Note:** These are not all test cases. Your testbench must cover more cases (e.g., Divisor=0, DC > Period), but only the listed cases need to be shown in the PDF.
- Mark key points on the images (e.g., interrupt trigger, PWM edges).

4. **Design Brief:**
    - <Your_Team_Name>_Design_Brief.pdf (1–2 pages) explaining:
        - How your design works.
        - How you handled three tricky challenges.
        - How you tested edge cases to show your code is original.

Submission

Deadline: July 29, 2025 at 12:00 PM

Submission Form:
https://docs.google.com/forms/d/e/1FAIpQLSdpMMK-kGtdC6fAGZnz7-FSwP8h7R5nSCnsvMdEI9LAmOzR8g/viewform?usp=header

Note: Set the Drive link to **Anyone with the link**.