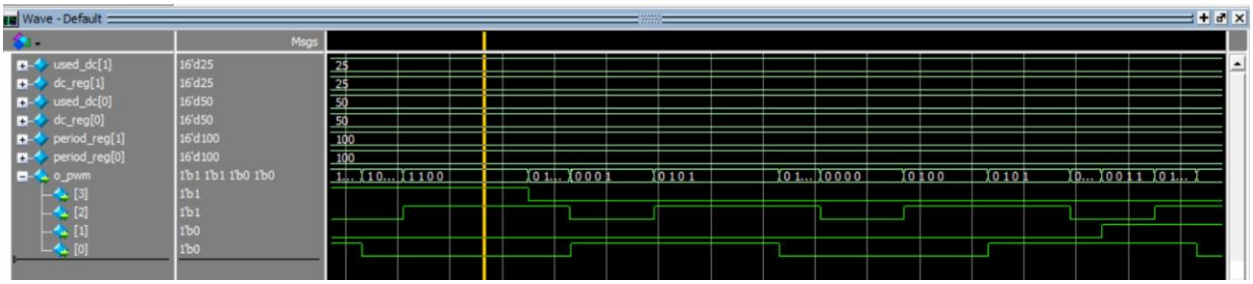
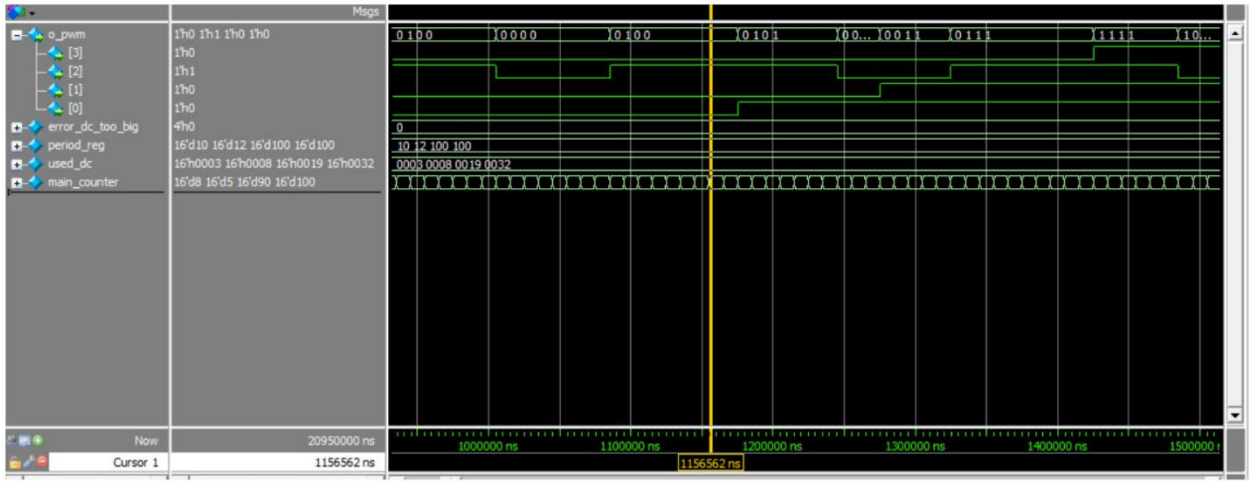
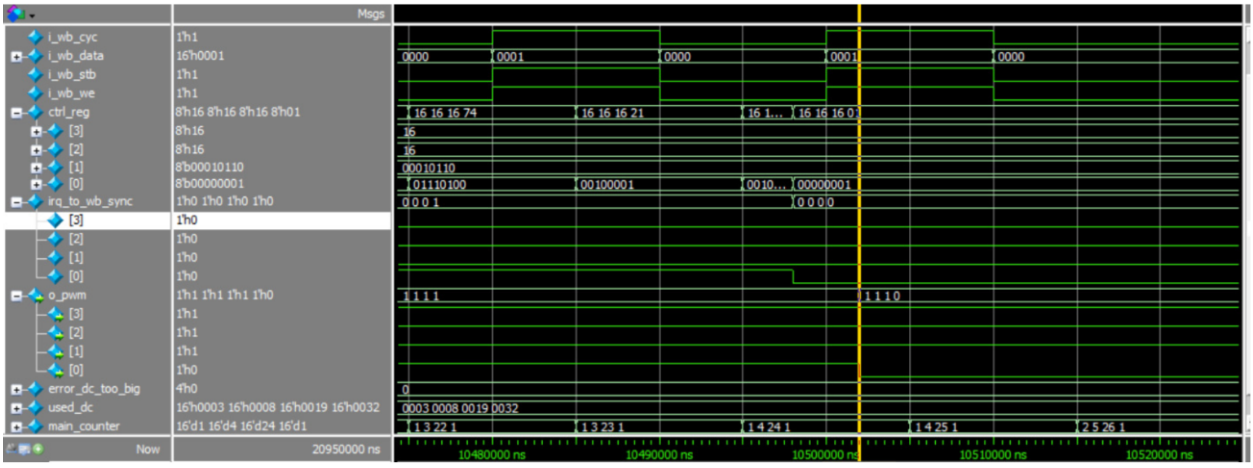
CCEE Wizards Simulation Results

PWM output for DC=50% and DC=25% of Period.

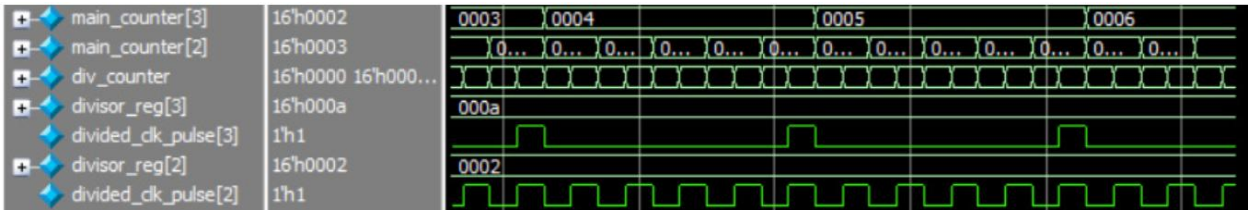


Timer Mode interrupt generation and clearing.



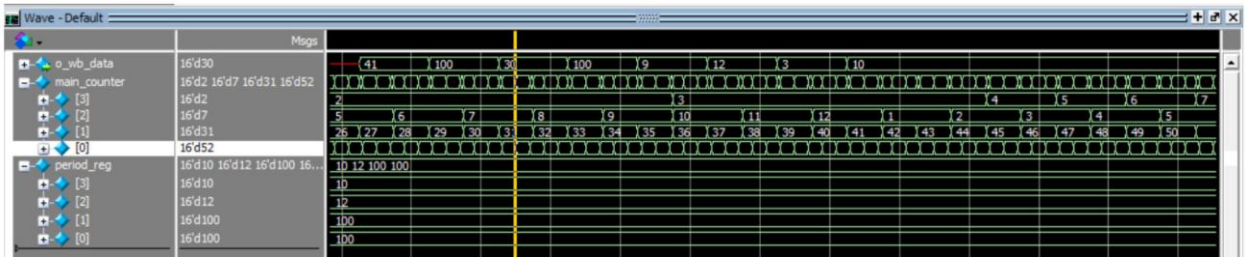


Down Clocking with Divisor=2 and Divisor=10.

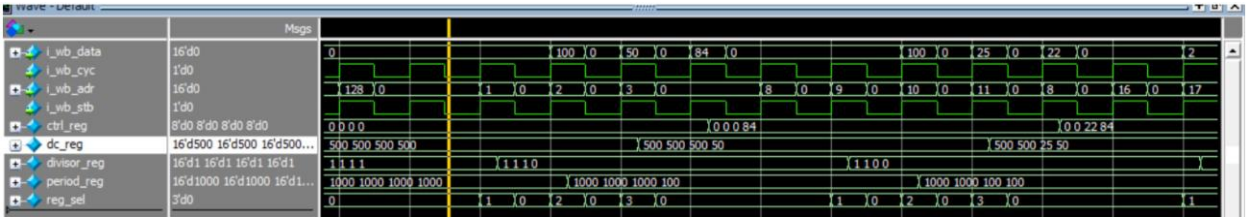


Wishbone read/write operations.

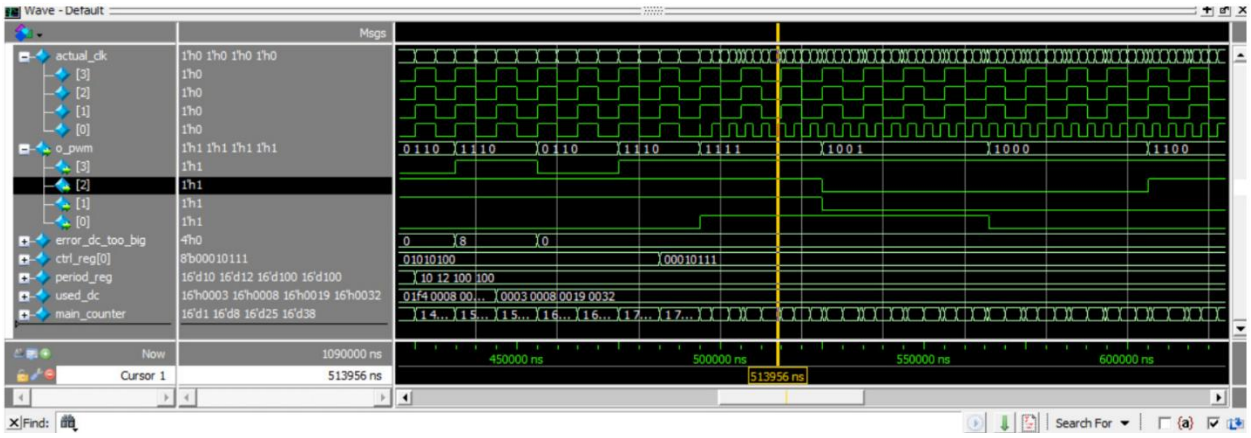
Read



Write



Optional features (multi-channel is added)
- multi-clock domains



- error handling: handle issues like DC> period or invalid divisor