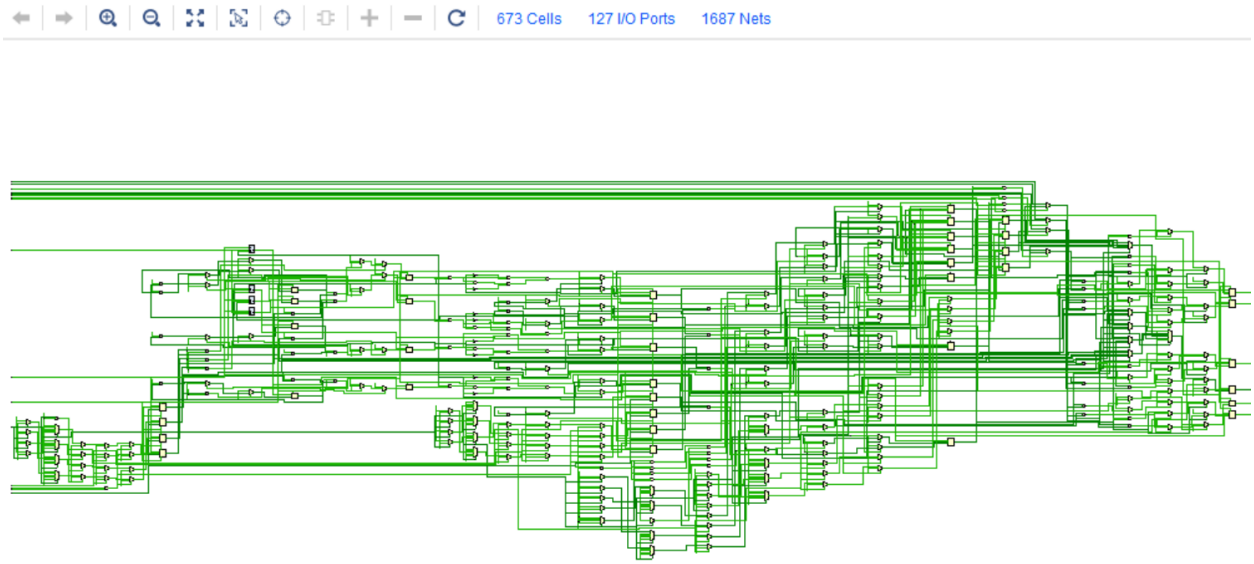
CCEE Wizards Design Brief

Elaborated Design Brief



Challenges

1) Down Clocking

We basically implemented a per-channel clock divided using a counter that feeds to the main counter of each channel.

```
// Per-channel clock divider
always @(posedge actual_clk[i] or posedge i_rst) begin
    if(i_rst) begin
        div_counter[i] <= 0;
        divided_clk_pulse[i] <= 1'b0;
        error_div_invalid[i] <= 1'b0;
    end else begin
        error_div_invalid[i] <= 1'b0; // Reset error flag

        if(divisor_reg[i] <= 1) begin
            div_counter[i] <= 0;
            divided_clk_pulse[i] <= 1'b1;
            if(divisor_reg[i] == 0) begin
                error_div_invalid[i] <= 1'b1;
            end

        end else begin
            if(div_counter[i] < (divisor_reg[i] - 1)) begin
                div_counter[i] <= div_counter[i] + 1;
                divided_clk_pulse[i] <= 1'b0;
            end else begin
                div_counter[i] <= 0;
                divided_clk_pulse[i] <= 1'b1;
            end
        end
    end
end
```

2) Multi-channel

Main counters represent the different counters for the 4 channels as shown all have different periods due to different value of divisor for each one which confirms unique period for each one and the output o_pwm is different channel output on timer and pwm_mode which confirms their functionality.

3) Multi-Clock Domain (switch between 2 clocks for each channel)
We implemented a glitch free clock mux with 1-bit synchronizer.

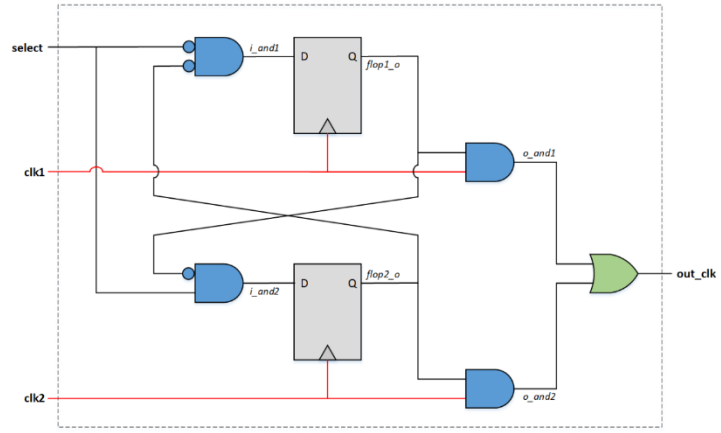


Figure 4: Glitch free clock mux