Computer Organization Project Report
Milestone 2
Team 65

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Memory Instructions:

```
        0000  LDA A  (200C)
        0001 ADD B  (100D)
        0002  SUB C  (500E)
        0003  SZA  (7004)
        0004  BUN N1  (4007)
        0005  LDA B  (200D)
        0006  BUN N2  (400A)
N1,     0007 LDA A (200C)
        0008 INC (7020)
        0009 BUN N3 (400B)
N2,     000A  AND A  (000C)
N3,     000B STA D (300F)
A,      000C DEC 2 (0002)
B,      000D DEC 5 (0005)
C,      000E DEC 7 (0007)
D,      000F DEC 0 (0000)
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ALU Signals

ADD	(001)	D1T5
SUB	(010)	D5T6
Transfer	(011)	D5T5 + D2T5
AND	(100)	D0T5
OR	(101)	—
XOR	(110)	—
INC	(111)	D7I'T4B5

— —

BUS Control

M[AR] (000) D0T4 + D1T4 + D2T4 +D5T4 + T1
AR (001) D4T4
TR (010) —
DR (011) —
AC (100) D7I'T3B5 + D3T4 + D5T5
PC (101) T0
IR (110) T2

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Instructions used

LDA : D2T4 + D2T5
ADD: D1T4 + D1T5
SUB: D5T4 + D5T5 +D5T6
SZA: D7I'T3B2 * (AC=0)
BUN: D4T4
INC: D7I'T3B5 + D7I'T4B5
AND: D0T4 + D0T5
STA: D3T4
AR Load: T0 + T2
Memory Read: D0T4 + D1T4 + D2T4 +D5T4 + T1
PC INC: D7I'T3B2(AC)' +T1
Memory Write: D3T4 + D5T4
AC Load: D7I'T4B5 + D0T5 + D1T5 + D2T5 + D5T6 + D5T5
IR Load: T1
PC Load: D4T4
DR Load: D0T4 + D1T4 +D2T4 + D5T5 + D5T4 +D7I'T3B5
SC CLR: D0T5 + D1T5 + D2T5 + D3T4 + D4T4 + D5T6 +D7I'T3B2 + D7I'T4B5