BIRZEIT UNIVERSITY

FACULTY OF ENGINEERING AND TECHNOLOGY
ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT
ADVANCED DIGITAL DESIGN ENCS533
COURSE PROJECT

Dr. Abdellatif Abu-Issa

Objective:

The task is to design a 2-digit BCD adder (8 bits), and then to write a complete code for functional verification. You should search for information about the following types of adders: Ripple Adder, Look-ahead Adder, BCD Adder.

The Task:

Your task is to create a library element that has the following appearance:

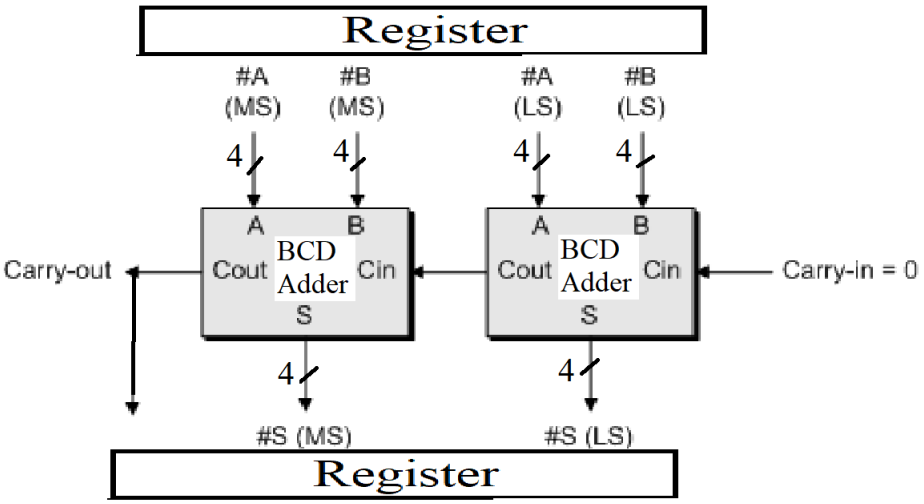
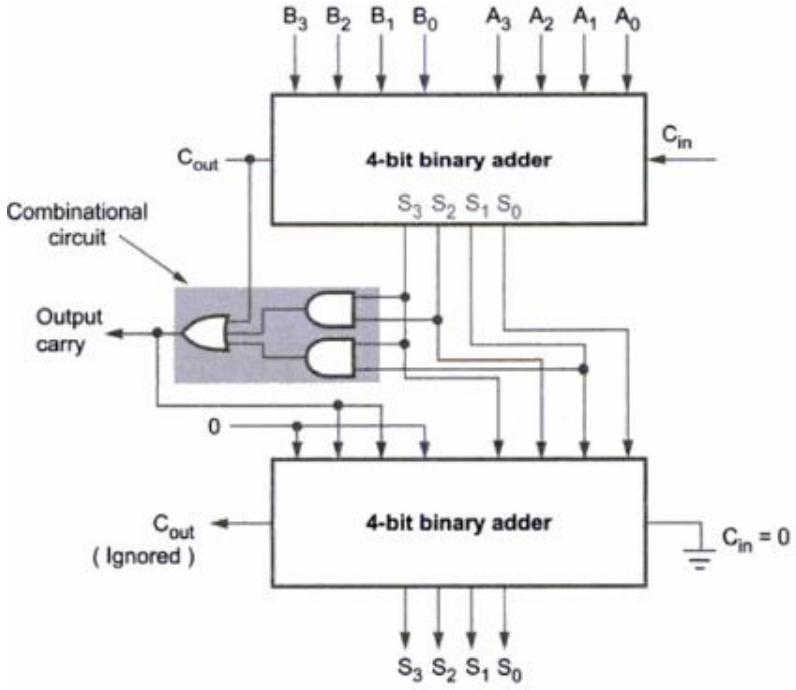


Figure 1: 2-Digit BCD Adder (8-bit)

And here how the BCD Adder looks like:



The inputs and the output of the 2-Digit BCD Adder are fed through/to flip-flops (registers).

The 2-Digit BCD Adder is to be built **structurally from a library of gates**, which contains the following devices:

Gate	Delay
Inverter	3 ns
NAND	6 ns
NOR	6 ns
AND	8 ns
OR	8 ns
XNOR	10 ns
XOR	12 ns

The BCD Adder will use 4-bit binary adders and extra required gates to build the needed circuit. The first type of the adders to be used is the carry ripple adder which should be built structurally as follows:

- Built 1-bit full adder from the basic gates given above.
- Use the full adder to build 4-bit adder.
- Use the 4-bit adders to build 1-Digit BCD Adder
- Use the 1-Digit BCD Adder to build the 2-Digit BCD Adder

The second type of adders to be used is the carry look-ahead adder. You should implement a 4-bit adder structurally using the basic gates given above and then build the 2-Digit BCD Adder in the same way.

Stages of the project:

The project is split into two stages of complexity, and you can choose how complex a system you wish to attempt to implement.

Stage 1

The adders to be used on this stage are the ripple carry adders. You should produce complete functional verification to demonstrate the 2-Digit BCD Adder working. You should determine the maximum latency of the Adder. And therefore, what is the maximum frequency of normal-mode clock that can be applied to the flip-flops. Also, you should introduce an error in your design and to do a verification that will discover the error and write it to a file.

Stage 2

Replace the ripple carry adder in stage 1 with an adder that accelerates addition by using carry look ahead on 4-bit groups. You should produce simulations to demonstrate the 2-Digit BCD Adder working. You should determine the maximum latency of the Adder. And therefore, what is the maximum frequency of normal-mode clock that can be applied. Also, you should introduce an error in your design and to do a verification that will discover the error and write it to a file.

Format of the report:

This project should be written as **formal report.** The report should include sections on the following:

- Brief introduction and background
- Design philosophy
- Results
- Conclusion and Future works

The report shouldn't exceed **8 pages (excluding the code)** with Font = 12 point

The code should be included in the appendix. Also the code should be sent as memo to the instructor after submitting the report.

Key Points:

- Any type of plagiarism or cheating will be penalized by **0** mark, and the cheaters will be treated according to the university laws.
- The design description should include a block diagram of the design, and give a justification of the decisions made.
- Technical achievement in design is linked to the degree of functionality that was attempted, as explained below.
- Technical achievement in implementation is based on the quality of your VHDL code. This includes issues such as legibility of code, use of meaningful variable names, good comments, clear structure, and modifiability of the design.
- Technical achievement in evaluation is based on the quality of your simulation results.

Mark scheme for technical achievement:

Design Attempted	Successful Implementation, using of comments and meaningful variable names, good simulation, good structure of the code…etc.
Stage 1	Up to 80%
Stage 1 and 2	Up to 100%

Deadline:

- The report should be submitted before midnight on Friday 4-12-2020.
- Late submission is penalized at a rate of 10% marks per day.

Assessment Form (Feedback):

The following is the assessment form for this project:

BIRZEIT UNIVERSITY

Electrical and Computer Engineering Department
Project Assessment Feedback
Advanced Digital Design (ENCS 533)

Dr. Abdellatif Abu-Issa

Student Name:…….. **Student ID:**…….

Marks

Report Presentation (10%)
Language (Spelling and Grammar), style of the report, caption of figures, page numbering…etc. ☐

Design Process and Outcome (70%)

- Description of the system and design process **(20%)** ☐
- Technical Achievement in System Design and Evaluation **(50%)** ☐

Judgement and Creativity (20%)

Demonstration of good judgment, imagination and creativity in selecting and applying design methods. Good discussion and analysing of the system and suggested improvements. ☐

Total Mark (Out of 100) ☐

Deducted Marks: ☐ late days * 10% per day ☐

FINAL ALLOCATED MARK (Out of 100) ☐

Any evidence for any type of cheating: yes no