Interface

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| --- | --- | --- |
| Port | Direction | Description |
| wr\_rstn | input |  |
| wr\_flush | input |  |
| wr\_clk | input |  |
| wr\_en | input |  |
| wdata | input |  |
| rd\_rstn | input |  |
| rd\_clk | input |  |
| rd\_en | input |  |
| rd\_flush | input |  |
| aempty\_th | input |  |
| afull\_th | input |  |
| rdata | output |  |
| wafull | output |  |
| raempty | output |  |
| wfull | output |  |
| rempty | output |  |
| overrun | output |  |
| underrun | output |  |
| waddr | output |  |
| raddr | output |  |

Constraints

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| --- | --- |
| Item | Description |
| Clock Definition | wr\_clk  frequency: 333MHz  The maximum external clock generator delay to the clock port is 700ps  The maximum insertion delay from the clock port to all the internal and external register clock pins is 300ps +/- 30ps  The clock period can fluctuate +/- 40ps due to jitter  Apply 50ps of “setup margin” to the clock period  The worst case rise/fall transition time of any clock pin is 120ps  rd\_clk  frequency: 250MHz  The maximum external clock generator delay to the clock port is 700ps  The maximum insertion delay from the clock port to all the internal and external register clock pins is 300ps +/- 30ps  The clock period can fluctuate +/- 40ps due to jitter  Apply 50ps of “setup margin” to the clock period  The worst case rise/fall transition time of any clock pin is 120ps |
| Register Setup Time | Assume a maximum setup time of 0.2ns for any register |
| Input Ports  (Sequential logic) | 1/3 \* clock period |
| Output Ports  (Sequential logic) | 1/3 \* clock period |
| Combinational Logic | No combinational logic currently |
| Design Area | The maximum design area goal is 540 area units |
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