Simple Sigma-Delta ADC

Reference Design

FPGA-RD-02047-1.6

December 2019

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1. Introduction

The Simple Sigma-Delta Analog-to-Digital Converter Reference Design targets the implementation of an analog-todigital converter in a Lattice Semiconductor CPLD or FPGA. This reference design supports the use of an external analog comparator device, or optionally an on-chip LVDS buffer in devices with differential LVDS input support. Implementing this reference design can eliminate the need for dedicated and expensive analog-to-digital circuits (ADC), powersupply monitors, and/or transducers.

The design can be implemented with few logic resources and is flexible enough to meet a variety of applications. The Simple Sigma-Delta ADC is an excellent choice for monitoring various sensors and power rails of a system.

1.1. Features

The Simple Sigma-Delta Analog-to-Digital Converter Reference Design features:

- Parameterized Bit Precision
- Adjustable Sampling Frequency

2. Overview

In this reference design, an analog input signal is over-sampled and converted to a digital value. The Simple Sigma-Delta ADC (SSD ADC) is implemented using a combination of internal and external components: analog comparator, low-pass RC network, sampling element, accumulator and simple digital Low-Pass Filter (LPF). In Lattice CPLDs or FPGAs that support LVDS I/O, only the RC network needs to be implemented externally, reducing parts count and cost. Users are able to enter parameter values to define the bit precision and sampling rate of the ADC.

2.1. Block Diagram

This section describes the SSD ADC functional block diagram shown in Figure 2.1.

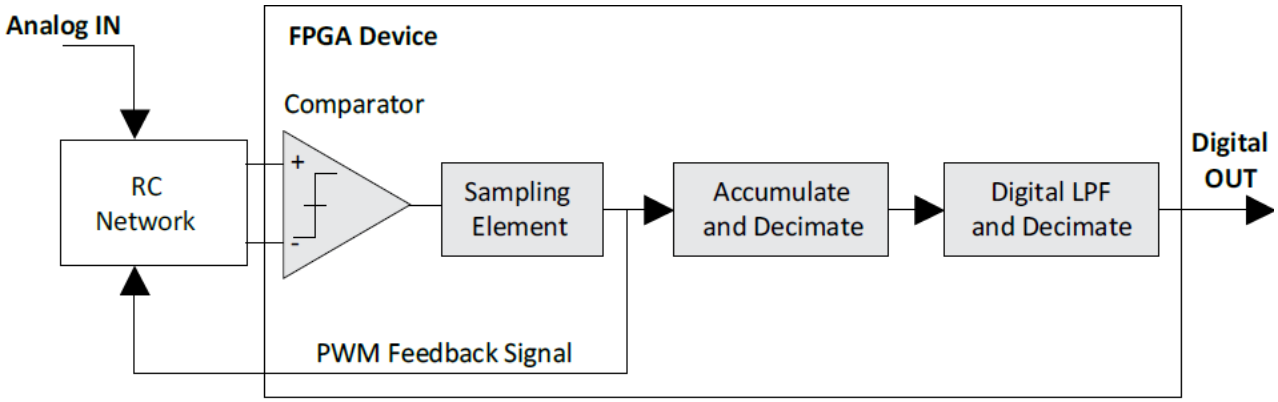

Figure 2.1. SSD ADC Functional Block Diagram

The following logic blocks are implemented in the PLD:

- Comparator (only in LVDS input capable devices)
- Sampling element
- Accumulator with decimation
- Digital Low-Pass Filter with decimation

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3. Parameter Descriptions

Table 3.1. Parameter Descriptions

Standard	Top
ADC_WIDTH	This parameter defines the width of the ADC output, in bits.
ACCUM_BITS	This parameter defines the depth of the first stage accumulation and decimation filter. 2^{ACCUM_BITS} is the accumulator depth and decimation factor. ACCUM_BITS must be greater than or equal to ADC_WIDTH.
LPF_DEPTH_BITS	The parameter defines the depth of the second stage digital low-pass filter (averaging circuit). $2^{LPF\_DEPTH\_BITS}$ is the LPF depth and decimation factor.
INPUT_TOPOLOGY	The parameter defines the topology, DIRECT or NETWORK, of the external analog input.

4. Signal Descriptions

Table 4.1. Reference Design Signal List

Standard		Top
clk	Input	SSD ADC operating clock signal (over-sampling clock).
rstn	Input	SSD ADC active low reset signal.
analog_cmp	Input	Data received from the output of the analog comparator.
analog_out	Output	PWM digital feedback signal to the analog RC network.
digital_out	Output	Digital representation of the analog signal converted by the SSD ADC. Bus width is defined by the ADC_WIDTH parameter [ADC_WIDTH-1:0].
sample_rdy	Output	Active high flag, indicating the digital value of the SSD ADC is valid. The output high pulse is 1 *clk* period wide.

5. Sigma-Delta Analog to Digital Conversion

In general, Sigma-Delta (or equivalently, Delta-Sigma) analog-to-digital converters trade expensive, high-precision analog components and simple digital circuits for simple analog converters and sophisticated, and relatively inexpensive, digital techniques.

Likewise, in this reference design an inexpensive RC network and a simple 1-bit ADC (the comparator) are used to feed high-speed digital circuits that produce higher-resolution digital output at reasonable accuracy.

5.1. RC Network Design

The output of the RC network is the average of the digital pulse train over a period of time, and is used to accurately track the analog input voltage at the terminals of the comparator. Figure 5.1 and Figure 5.2 illustrate two possible RC network input stages for use with this reference design.

Figure 5.1 is the simplest network, a single resister and capacitor in the feedback path. They comprise a low-pass filter for the PWM feedback signal analog_out. It has the advantage of low parts count. Its chief disadvantage is that the analog signal is limited to the input voltage range of the comparator.

The PWM feedback signal swings between 0V and VCCIO of the PLD or FPGA pin. Thus, the filtered feedback signal at the negative input of the comparator can theoretically match any input voltage between 0V and VCCIO. However, when using an internal LVDS buffer for the comparator, the working input voltage range can be significantly less than the V_{CCIO}, depending upon the device (as an example, for MachXO™ LVDS, it is approximately V_{CCIO} - 0.5 V), which puts a practical upper bound on the analog input voltage range.

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The time-constant, τ = RC, should be made large enough to adequately filter the PWM stream, but not so large to dampen response time. Given the over-sampling clock frequency, f_{CLK}, then $\tau \times f_{CLK}$ = 200 to 1000 is recommended. An optional resister can be placed in line with the analog input to protect the high-impedance input of the comparator.

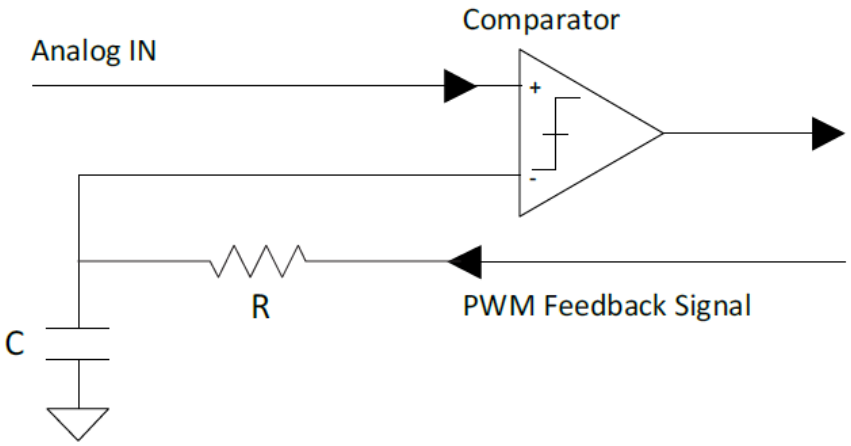

Figure 5.1. SSD ADC DIRECT Analog Input Topology

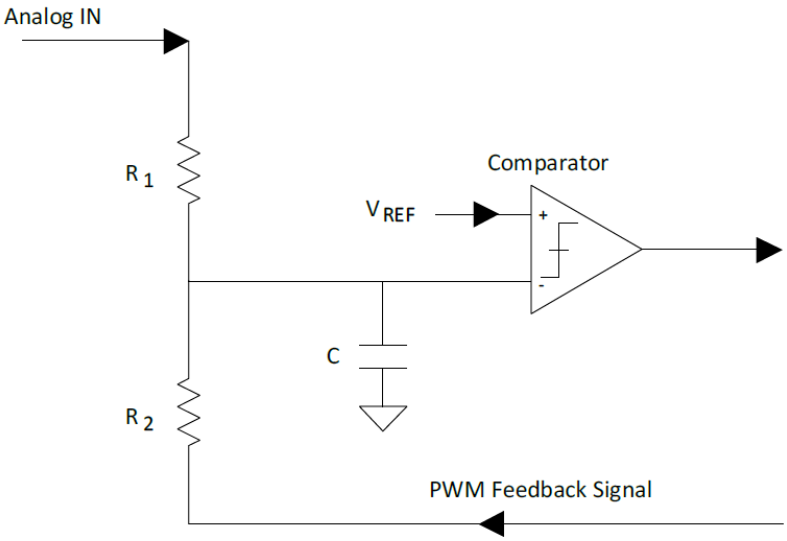

Figure 5.2. SSD ADC NETWORK Analog Input Topology

Figure 5.2 is a more sophisticated and flexible network. With a modest component count increase, it has the advantage of a flexible analog input voltage range while at the same time fixing the input voltage to the terminals of the comparator.

Given the analog input voltage swing, ΔVIN, and the PWM feedback voltage swing, VCCIO, the component value can be calculated with the aid of the following equations:

where: $$\Delta V_{IN}/V_{CCIO}=R_1/R_2 \quad (1)$$

and: $$\Delta V_{IN}=(V_{INMAX}-V_{INMIN}) \quad (2)$$

and: $$V_{REF}=V_{INMAX}\ x\ R_2/(R_1+R_2) \quad (3)$$

For example, if V_{IN} swings from 0 V to 12 V, and V_{CCIO} = 3.3 V, then R_1 / R_2 = 3.64, and V_{REF} = 2.59 V.

The actual values chosen for R_1 and R_2 depend on two factors. First, the input impedance seen by the analog input and second, the low-pass filter time constant. The input impedance is R1 + R2 // (ωC)-1 and is usually desired to be large. The time constant equation is τ = RPC, where $R_P = R_1 // R_2$. As in the previous topology, τ × fCLK ≈ 200 to 1000 is recommended.

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It is important to note that the ΔV_{IN} range used in the equations above will be represented by a zero-to-full scale of the ADC digital output. Analog input values exceeding that range will not be compensated fully by the PWM feed- back and cause the comparator negative terminal to offset from V_{REF}.

To set V_{REF}, various methods can be used, including a simple resistor voltage divider, a zener diode, or a precision band-gap voltage reference device. The method used is a possible source of measurement error and a contributing factor to the overall accuracy of the ADC, as discussed below. It is also possible to work the circuit equations backwards, starting with a desired or practical VREF, to determine the analog input voltage range for a given circuit.

5.2. SSD ADC Comparator

The simple sigma delta reference design utilizes a comparator as a 1-bit analog-to-digital converter. This comparator may be a discrete external device, such as a National Semiconductor LMV311 or equivalent. Alternatively, several Lattice CPLD and FPGA devices support LVDS signaling with on-board LVDS input buffers. These buffers are, in fact, very fast analog comparators. While optimized for use within the LVDS specifications, these buffers are very serviceable for use as a 1-bit ADC, especially in conjunction with the 'NETWORK' input topology shown above.

In the reference design, the LVDS buffer is instantiated via the design preferences with IO_TYPE=LVDS25. If an external comparator is used instead, then a suitable digital IO type is used instead, such as IO_TYPE=LVCMOS33. The HDL source file remains unchanged with either selection.

5.3. SSD ADC Sampling Element

Key to Sigma-Delta ADC is the notion of over-sampling. A single flip-flop is utilized in the reference design to capture the output of the comparator, driven at the over-sampling clock rate, fCLK. The signal CLK_IN serves as this clock in the reference design. The output of the sampling element is a high-frequency pulse-width modulated (PWM) representation of the analog input.

5.4. SSD ADC Digital Filter Design

The Simple Sigma-Delta ADC Reference Design utilizes a two-stage digital filter design, as shown in Figure 2.1. The filters provide the basic integration of the PWM stream and some amount of anti-aliasing.

The first stage filter (the integrator or accumulator) converts the PWM stream from a 1-bit, high-frequency data stream to a multi-bit, intermediate-frequency data stream. The bit depth of the accumulator must be at least as large as the desired digital output bit width.

The accumulator can be modeled as a FIR filter with all coefficients equal to one. The output data width of the accumulator is ACCUM_BITS, and the decimation rate is 2^{ACCUM_BITS}. Thus, the output frequency of the accumulator is:

$$F_{ACCUM} = f_{CLK} / 2^{ACCUM\_BITS} \quad (4)$$

A greater range of f_{ACCUM} can be achieved by customizing the accumulator counter to values other than a power of 2.

The second state filter performs an arithmetic average function on the accumulator data, providing further decimation to the output frequency of the ADC as well as an anti-aliasing function. Again, the average function can be modeled as a FIR filter with all coefficients equal to one, also known as a 'box'-type FIR filter. The output data width of the accumulator is ADC_WIDTH, and the decimation rate is 2 LPF_DEPTH_BITS. Thus the output frequency of the averaging circuit is:

$$F_{ADC} = F_{ACCUM} / 2^{LPF\_DEPTH\_BITS} = f_{CLK} / 2^{ACCUM\_BITS+LPF\_DEPTH\_BITS} \quad (5)$$

In the reference design, fCLK = 62.5 MHz, ACCUM_BITS = 10 and LPF_DEPTH_BITS = 3. Thus, the output sample frequency f_{ADC} = 7.629 KHz.

While the box-filter provides implementation simplicity, it is a relatively poor anti-aliasing filter, providing only -13 dB of stop-band attenuation. While the SSD ADC is suitable for low-frequency sensor inputs and voltage rail monitoring, it is not suitable, as-is, for applications that require a faithful reconstruction of the digitized input waveform, such as audio. More sophisticated digital filter implementations may be possible within larger Lattice CPLD and FPGA devices, but these are beyond the scope of this reference design.

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5.5. SSD ADC Resolution

The maximum theoretical resolution is related to the number of bits of the converter:

$$V_{RESOLUTION} = \pm\frac{1}{2}\Delta V_{IN} / 2^{ADC\_BITS} \quad (6)$$

where ΔV_{IN} is defined as in the section RC Network Design above. Thus, an 8-bit convertor can theoretically resolve 3.3 V to ± 6.44 mv. Actual resolution is affected by uncertainty errors and noise in the measurement circuit, as discussed below.

The resolution of Sigma-Delta type converters can be very good compared to other ADC converters of similar complexity. Table 5.1 shows some example Signal-to-Noise ratio and ENOB results when converting sine-wave inputs.

Table 5.1. Reference Design Signal List

Operation Frequency	Output Sample Rate	Input Frequency (Hz)	8-Bit SSD SNR	8-Bit SSD ENOB1	10-Bit SSD SNR	10-Bit SSD ENOB*	Operation Frequency
62.5 MHz	7.63 KHz	50	47.0	7.12	54.9	8.60	62.5 MHz
62.5 MHz	7.63 KHz	1000	46.7	7.18	52.8	8.25	62.5 MHz
62.5 MHz	7.63 KHz	3800	42.5	6.74	53.1	8.53	62.5 MHz

Note: ENOB = Equivalent Number of Bits of resolution.

5.6. SSD ADC Absolute Accuracy

Many factors contribute to the absolute accuracy of the ADC. The accuracy of any analog measurement is directly related to the accuracy of the reference, in this case V_{REF} and V_{CCIO}. The stability and accuracy of the VCCIO voltage source that supplies the PWM output buffer is the largest single limiting factor to absolute measurement ability of the SSD ADC. Proper filtering and decoupling of voltage sources must be observed. Any noise present on V_{CCIO} directly impacts the measurement circuit.

Typical digital devices such as CPLDs and FPGAs specify supply voltage tolerances to within 5%. This is equivalent to 1 in 20, or 4.3 bits. The supply voltage tolerance can be tightened by the designer at added cost and complexity to perhaps 1%, or 1 in 100, or 6.6 bits. Subtracting from these maximum resolutions are the uncertainty of V_{REF}, input resistor divider component tolerances, poor power-supply filtering, and noise on V_{CCIO} due to switching of other I/Os. Also, component values can drift over time and temperature.

Table 5.2. Voltage Supply Tolerance vs. Absolute Accuracy

V_{CCIO} , V_{REF} Tolerance	Max. Absolute Accuracy
10%	3.3 bits
5%	4.3 bits
2%	5.6 bits
1%	6.6 bits
10%	3.3 bits

Due consideration of these factors must be taken to ensure the desired absolute measurement performance of this, or any, ADC application.

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6. Timing Diagram

The following timing diagram shows the Simple Sigma-Delta ADC tracking an analog input. (This simulation is included as the reference design testbench.)

The integrator signal is a testbench construct to emulate the RC filter network driven by the SSD ADC feedback PWM analog_out. The output of the testbench comparator is analog_cmp and is the input to the SSD ADC. In functional simulation, an internal accum signal shows an accumulation and decimation over 1024 samples.

The output of the SSD ADC is digital_out. It demonstrates the average function over the previous eight accum values.

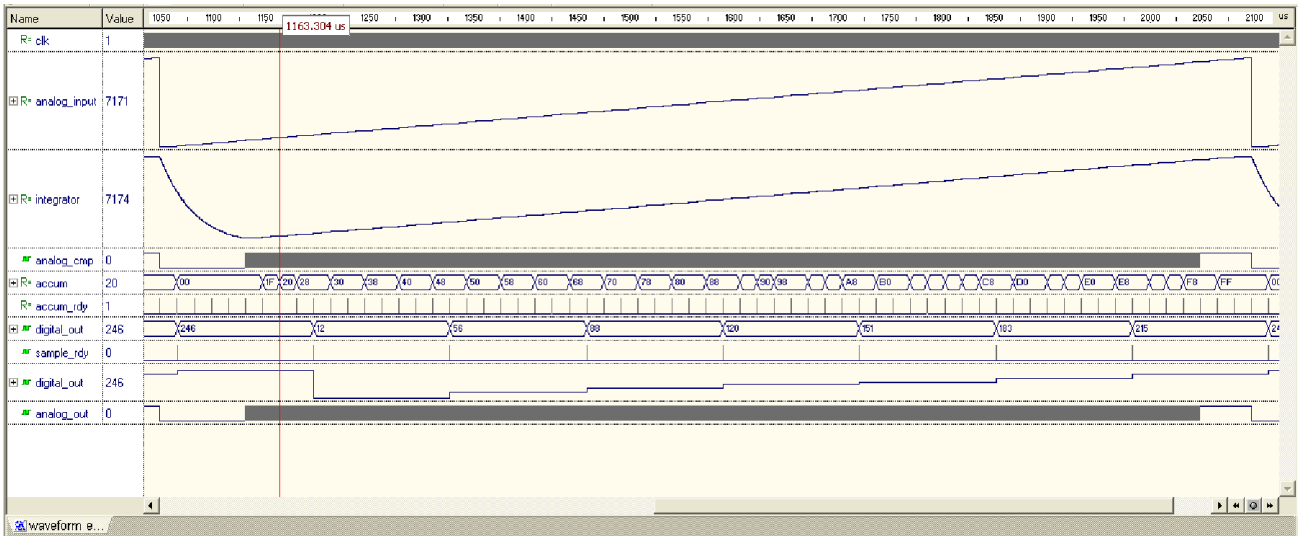

Figure 6.1. Tracking a Sawtooth Waveform (Functional Simulation)

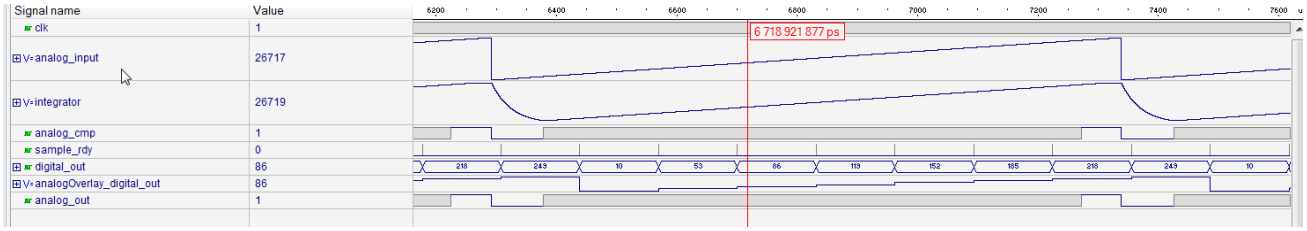

Figure 6.2. Functional Simulation for iCE40 UltraPlus™

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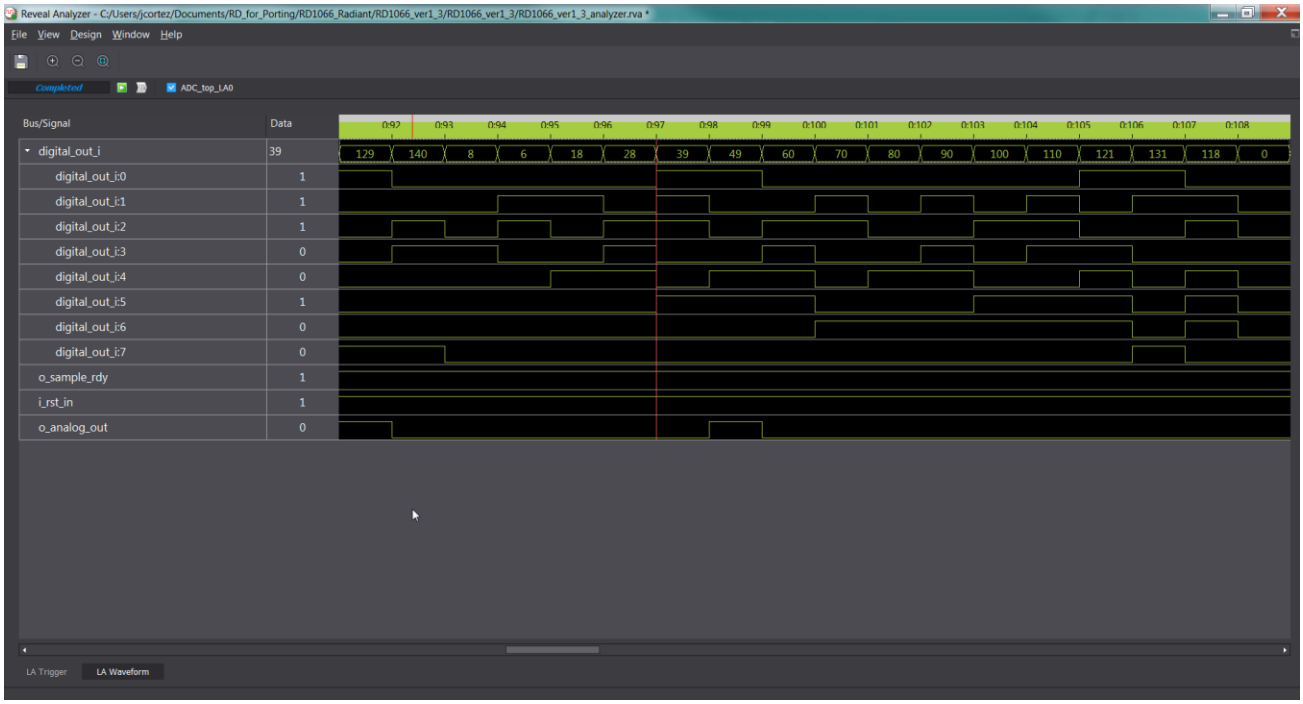

Figure 6.3. Actual Reading for iCE40 UltraPlus

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7. Implementation

Table 7.1. Performance and Resource Utilization[1]

Device	Tool/Coding Language	Speed Grade	Utilization (LUTs)	fMAX (MHz)	I/Os	Architecture Resources
iCE40 UltraPlus[5]	Verilog-LSE	NA	99	>150	13	NA
	Verilog-Syn	NA	101	>150	13	NA
MachXO2™ [2]	Verilog-LSE	–6	49	>150	13	NA
	Verilog-Syn	–6	61	>150	13	NA
	VHDL-LSE	–6	49	>150	13	NA
	VHDL-Syn	–6	61	>150	13	NA
MachXO[3]	Verilog-LSE	–5	46	>150	13	NA
	Verilog-Syn	–5	48	>150	13	NA
	VHDL-LSE	–5	46	>150	13	NA
	VHDL-Syn	–5	48	>150	13	NA
LatticeXP2™ [4]	Verilog-Syn	–5	62	>150	13	NA
	VHDL-Syn	–5	62	>150	13	NA

Notes:

1. The parameter settings for this implementation include: ADC_WIDTH = 8, ACCUM_BITS = 10, and LPF_DEPTH_BITS = 3, 'Network' topology and internal LVDS buffer.
2. Performance and utilization characteristics are generated using LCMXO2-1200HC-6MG132CES, with Lattice Diamond® 3.3 software with LSE and Synplify Pro®. When using this design in a different device, density, speed, or grade, performance and utilization may vary.
3. Performance and utilization characteristics are generated using LCMXO2280C-5FT256C, with Lattice Diamond 3.3 software with LSE and Synplify Pro. When using this design in a different device, density, speed, or grade, performance and utilization may vary.
4. Performance and utilization characteristics are generated using LFXP2-5E-5FT256C, with Lattice Diamond 3.3 software with Synplify Pro. When using this design in a different device, density, speed, or grade, performance and utilization may vary.
5. Performance and utilization characteristics are generated using ice40UP5K-SG48I, with Radiant 1.0 SP1 software with LSE and Synplify Pro. When using this design in a different device, density, or speed, performance and utilization may vary.

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Revision History

Revision 1.6, December 2019

Section	Change Summary
Disclaimers	Added this section.

Revision 1.5, September 2018

Section	Change Summary
All	• Changed document number from RD1066 to FPGA-RD-02047.
Timing Diagrams	Added timing diagrams for iCE40 UltraPlus: • Figure 6.2. Functional Simulation for iCE40 UltraPlus™ • Figure 6.3. Actual Reading for iCE40 UltraPlus
Implementation	Updated Table 7.1. Performance and Resource Utilization1.

Revision 1.4, January 2015

Section	Change Summary
All	Updated Implementation section. Updated Table 5, Performance and Resource Utilization. • Updated values. • Added support for LSE and Synplify Pro. • Added support for Lattice Diamond 3.3 design software.

Revision 1.3, November 2010

Section	Change Summary
All	Added support for MachXO2 device family and Diamond design software.

Revision 1.2, February 2010

Section	Change Summary
All	Added support for LatticeXP2 device family.

Revision 1.1, January 2010

Section	Change Summary
All	Removed references to RD1063, cleaned up various typos.

Revision 1.0, December 2009

Section	Change Summary
All	Initial release

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