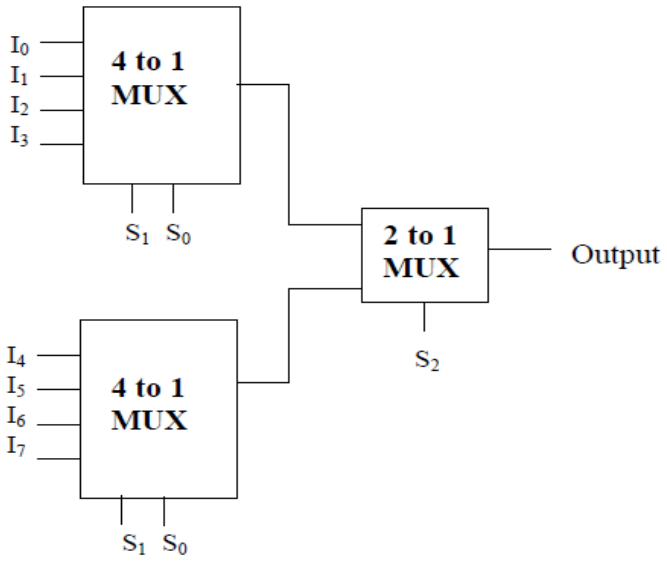
Faculty of Engineering & Technology – Electrical & Computer Engineering Department
Digital Systems ENCS234

HDL Homework

Q1: Given the following Combinational circuit, Use Verilog HDL on Quartus tool to



1. Write a Verilog HDL code to describe the module mux4×1 // this module name must be your last name
2. Write a Verilog HDL code to describe the module mux2×1// this module name must be your first name
3. Write a Verilog HDL code to describe the whole system structurally from its subsystems // this module name must be your university number

Q2:

Problem: Design and Simulation of 8-bit ALU

Design an 8-bit ALU circuit that receives two 8-bit input numbers `X[7:0]` and `Y[7:0]`, and produces a 8-bit output `Z[7:0]`, an output carry `Cout`, an overflow flag `OV`, and `Zero` flag. The circuit implements the following 12 functions based on a 3-bit control input `C[3:0]`:

Code	Function
000	Addition: `Z=X+Y`
001	Subtraction: `Z=X-Y`
010	Reminder: `Z=X%Y`
011	Bitwise AND: `Z=X&Y`
100	Bitwise OR: `Z=X|Y`
101	Concatenate: `Z={X[3:0] , Y[3:0]}`
110	Equality: Zero=`X==Y`
111	Less than: `Cout=X<Y`

Notes:

a) Show the block diagram design of your 8-bit ALU using components like Adder, Multiplexor, etc. as needed.
b) Model each component separately. You should have different modules for the adder, multiplexer, etc.
c) Write a Verilog test scenarios to test both the 8-bit ALU. Verify the correctness by simulation.
d) Show snapshots of all simulation waveforms.
e) Submit a report (Word or PDF document) should contain Problem description, the block diagram, a copy of the Verilog modules and the waveforms taken directly as snapshots from the simulator.

In addition to building the Quartus project, you need to write down one report for **each student** that includes the following items:

1. System Design.
2. Verilog code.
3. Simulation results.

There would be a discussion for each project with date allocated by the instructors.
Note: There is no group work

Note: Screenshot is not allowed in writing the code (copy the code from Quartus software)