BIRZEIT UNIVERSITY

FACULTY OF ENGINEERING AND TECHNOLOGY
ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT
ADVANCED DIGITAL DESIGN ENCS3310
COURSE PROJECT

Dr. Abdellatif Abu-Issa

Objective:

The task is to design an 8-bit Comparator for signed 2's complement representation numbers, and then to write a complete code for functional verification. You should search for information about the following types of circuits: Ripple Adder/subtractor, Look-ahead Adder/subtractor, and magnitude (unsigned) comparator.

The Task:

Your task is to create a library element that compares between 2 numbers (A and B) represented in signed 2's complement representation and to produce 3 outputs F1(A=B), F2(A>B), and F3 (A<B). You should implement the design structurally in different ways and to verify that your design works properly. The inputs and the output of the comparator are fed through/to flip-flops (registers).

The Comparator is to be built **structurally from a library of gates**, which contains the following devices:

Gate	Delay
Inverter	2 ns
NAND	5 ns
NOR	5 ns
AND	7 ns
OR	7 ns
XNOR	9 ns
XOR	12 ns

Stages of the project:

The project is split into two stages of complexity, and you can choose how complex a system you wish to attempt to implement.

Stage 1

Use the adder (ripple and/or look ahead) to implement the Signed Comparator. You should produce complete functional verification to demonstrate the Signed Comparator working. You should determine the maximum latency of the comparator. And therefore, what is the maximum frequency of normal-mode clock that can be applied to the flip-flops. Also, you should introduce an error in your design and to do a verification that will discover the error and write it to console.

Stage 2

Use the Magnitude comparator and the sign bit to implement the signed comparator. You should produce simulations to demonstrate the signed comparator working. You should determine the maximum latency of the unit. And therefore, what is the maximum frequency of normal-mode clock that can be applied. Also, you should introduce an error in your design and to do a verification that will discover the error and write it to the console.

Format of the report:

This project should be written as **formal report.** The report should include sections on the following:

- Brief introduction and background
- Design philosophy
- Results
- Conclusion and Future works

The report shouldn't exceed **8 pages (excluding the code)** with Font = 12 point

The code should be included in the appendix (also to be submitted in different text file on Ritaj).

Key Points:

- Any type of plagiarism or cheating will be penalized by **0** mark, and the cheaters will be treated according to the university laws.
- The design description should include a block diagram of the design, and give a justification of the decisions made.
- Technical achievement in design is linked to the degree of functionality that was attempted, as explained below.
- Technical achievement in implementation is based on the quality of your VHDL code. This includes issues such as legibility of code, use of meaningful variable names, good comments, clear structure, and modifiability of the design.
- Technical achievement in evaluation is based on the quality of your simulation results.

Deadline:

- The report should be submitted by Sunday 12-12-2021.
- Late submission is penalized at a rate of 10% marks per day.

Assessment Form (Feedback) :

The following is the assessment form for this project. This feedback will be given back to the student after finishing the assessment process:

Electrical and Computer Engineering Department
Project Assessment Feedback
Advanced Digital Design (ENCS3310)

Dr. Abdellatif Abu-Issa

Student Name:……..	**Student ID:**…….

Marks

Report Presentation (10%)
Language (Spelling and Grammar), style of the report, caption of figures, page numbering…etc. ☐

Design Process and Outcome (70%)

- Description of the system and design process **(20%)** ☐
- Technical Achievement in System Design and Evaluation **(50%)** ☐

Judgement and Creativity (20%)

Demonstration of good judgment, imagination and creativity in selecting and applying design methods. Good discussion and analysing of the system and suggested improvements. ☐

Total Mark (Out of 100) ☐

Deducted Marks: ☐ late days * 10% per day ☐

FINAL ALLOCATED MARK (Out of 100) ☐

Any evidence for any type of cheating: yes no