AMERICAN INTERNATIONAL UNIVERSITY–BANGLADESH (AIUB)

FACULTY OF ELECTRICAL & ELECTRONICS ENGINEERING (EEE)

DIGITAL LOGIC AND CIRCUITS LAB

Summer 2023-2024

Section: I, Group: 03

Experiment no: 9

LAB REPORT ON

Design of a Digital to Analog and Analog to Digital Converters.

Supervised By

RETHWAN FAIZ

Submitted By

Name	ID	Department
1. Md. Nur Rahatul Islam	23-51007-1	CSE
2. Md. Tariqul Islam Sesir	23-51017-1	CSE
3. Amina Ferdous	22-47822-2	CSE
4. Tofazzel Hossain Himu	22-47832-2	CSE

Date of Performance: 18/09/2024

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18/9/24

Open Ended Laboratory Experiment Guideline

American International University- Bangladesh (AIUB)
Faculty of Engineering (EEE)

Performance test: 10 Marks

Course Name:	Digital Logic and Circuits Lab	**Course Code:**	EEE 3102	Section: I
Semester:	Summer 23-24	**Faculty:**	Rethwan Faiz	

Task:	Perform Lab task following the instructions of course teacher.
Experiment title:	Design of a Digital to Analog and Analog to Digital Converters.

Group Members	**ID**	**Name**	**Dept.**
1.	Md. Nur Rahatul Islam	23-51007-1	CSE
2.	Md. Tariqul Islam Sesir	23-51017-1	CSE
3.	Amina Ferdous	22-47822-2	CSE
4.	Tofazzel Hossain Himu	22-47832-2	CSE
5.			

Marking Rubrics (to be filled by Faculty) **Performance test: 10 Marks**

Objectives	Unacceptable (0.5)	Needs Improvement (1)	Good (1.5)	Excellent (2)	Secured Marks
Use of Appropriate Tools	Students Fail to identify and utilize appropriate software and hardware tools for prediction and modeling of the proposed solution	Students identified some software and hardware tools for prediction and modeling but failed to use them appropriately.	Students identified and utilized the closely related software and hardware tools for prediction and modeling but failed to use them effectively.	Students identified and utilized the most effective appropriate software and hardware tools for prediction and modeling of the proposed solution	
Analysis of Implemented Model	The software and/or hardware implementation has not been addressed and provided only incomplete analysis.	The software and/or hardware implementation has been partially addressed and provided only incomplete analysis.	The software and/or hardware implementation has been successfully addressed but provided only incomplete analysis.	The software and/or hardware implementation has been successfully addressed and provided an in-depth analysis	
Depth of Knowledge about the Tools [P1]	The student has provided some processes for using appropriate tools but demonstrated no knowledge of the utilized tools	The student has provided a partial process for using appropriate tools and does not demonstrate in-depth knowledge of the utilized tools	The student has provided a detailed process for using appropriate tools but fails to demonstrate the in-depth knowledge of the utilized tools	The student has provided a detailed process for using appropriate tools, which demonstrated the in-depth knowledge of the utilized tools.	
Infrequent encounter Issues [P4]	Students have failed to address how the Infrequent encounter Issues were resolved.	Students have partially addressed how the Infrequent encounter Issues were resolved but not related to used tools.	Students have addressed how the Infrequent encounter Issues were resolved but not related to used tools.	Students have effectively addressed how the Infrequent encounter Issues were resolved using the appropriate tools.	
The models developed by tools meet the applicable codes [P5]	Failed to address any outside problems.	Addressed some outside problems but not encompassed by standards and codes of practice for professional engineering	Addressed some outside problems encompassed by standards and codes of practice for professional engineering	Effectively addressed that the external issues surrounded by standards and regulations of practice for professional engineering	
Comments:				**Total Marks:**	

18/9/24

Abstract: In this experiment, we explore the design and testing of a Digital-to-Analog Converter (DAC) and Analog-to-Digital Converter (ADC) emphasizing practical implementation. It covers the fundamental concepts, utilizing hands-on experience with components and circuits. We analyze the trade-offs and challenges, providing valuable insights into DAC functionality. The experiment concludes by discussing the broader applications and significance of DACs and ADCs in modern electronic systems, offering a comprehensive understanding of analog signal generation.

Part I: Design of a Digital to Analog Converter

Introduction: The design of a digital to analog converter (DAC) is covered in this lab. This lab displays two different design types: R/2R ladder DAC design and binary weighted DAC design. In the end, we will contrast the two designs to determine which is more effective and why. [2]

Methodology: Signals are primarily divided into two categories: digital and analog. Real-world data and information exist in analog form, but digital equipment like computers, calculators, and cellphones can only comprehend data signals in the digital domain. The two types of converters we utilize on a daily basis to convert signals into one another are analog to digital (ADC) and digital to analog (DAC). [3]

Digital-to-Analog Converters: An electronic circuit known as a "digital to analog converter" may change any digital signal, such a binary signal, into an analog signal, like voltage or current. Digital signals, like binary signals, are made up of combinations of 1s and 0s, or high and low voltage levels, and exist in the form of bits. These bits are transformed into an analog voltage or current by the DAC. [3]

Real-world information is available in analog format. A digital computer's processing speed is extremely quick, it can compute or process any amount of data in a few microseconds. It helps process complex data in accordance with our needs and saves time. However, in the actual world, we are unable to comprehend digital data. We must translate the data we process from the digital domain into the analog domain in order to comprehend it. An instance of that would be the audio and video editing procedure. In order to transform the analog data into digital, we record it using our digital camera and microphone. We use our computers to process it and alter it to meet our purposes. In order to view our edited work, we use DACs to convert it back into the analog domain to view & listen it through our screen & speakers. [3]

There are various DAC architectures. The physical size, power consumption, resolution, speed, accuracy, and cost are the six primary factors that define a DAC's usefulness for a given application. All but the most specialized DACs are built as integrated circuits (ICs) due to their complexity and requirement for perfectly matched components. Signal degradation can occur during digital-to-analog conversion, hence a DAC with negligible faults for the intended use should be chosen. [4]

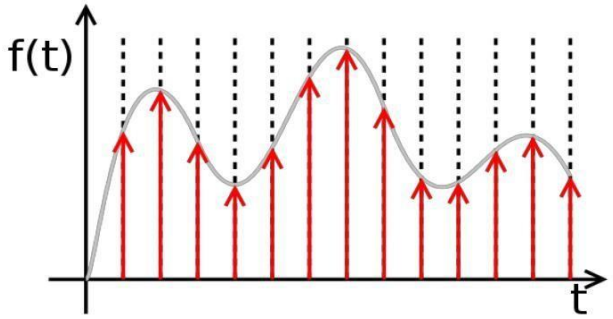


Fig: Ideally sampled signal[2]

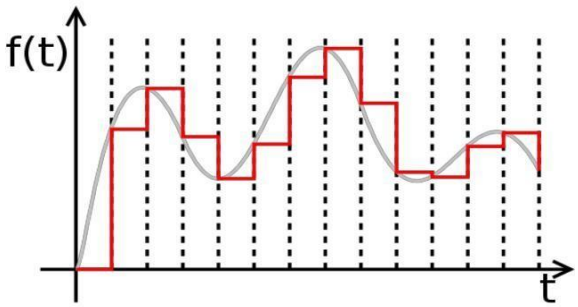


Fig: Piecewise constant output of an idealized DAC lacking a reconstruction filter. In a practical DAC, a filter or the finite bandwidth of the device smoothes out the step response into a continuous curve[2]

A voltage that is proportionate to a digitally coded number is produced by a device known as a digital-to-analog converter, or DAC for short. For instance, a DAC's output voltage will be proportional to N if it receives a number N: $V_{out} = N \times B$. The constant of proportionality, B, is normally determined from the ratio of the reference voltage, V_{ref}, and the maximum value that N can have, N_{max}, $B = V_{ref} / N_{max}$ so that $V_{out} = V_{ref} N / N_{max}$. A popular circuit used to create a DAC is an OpAmp circuit [2].

Binary Weighted Digital-to-Analog Converter:

A digital to analog converter that uses a network of binary weighted resistors to transform a digital input signal into an analog output signal is called a binary weighted resistor digital to analog converter (DAC). To put it simply, a binary weighted resistor DAC creates an analog output signal that corresponds to the digital input signal by means of a network of precision resistors with binary-weighted values. To provide an analog output, the binary weighted resistor DAC connects a resistive ladder network to a summing amplifier. Every resistor in the ladder network has a resistance value that is a binary proportion to the resistor before it. The correct weighting and conversion of the digital input signal into the analog output signal is guaranteed by this kind of DAC. [5]

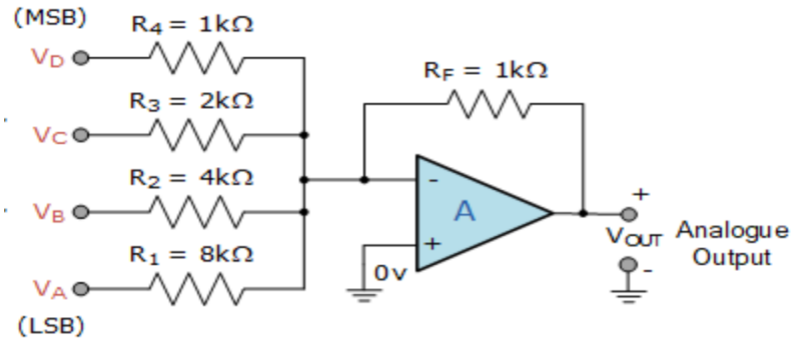


Fig: Binary Weighted Digital to Analog converter[10]

The disadvantage of the weighted resistor DAC is the numerous resistor values. For instance, if we take an 8-bit converter, the 8 resistors will range from R to 128R in binary weighted steps. This type of DAC is very difficult to mass produce due to the range of resistors required where the tolerance is less than 0.5% to accurately convert the input. [6]

R/2R Ladder Digital-to-Analog Converter:

R-2R Digital-to-Analogue Converter, or DAC, is a data converter which use two precision resistor to convert a digital binary number into an analogue output signal proportional to the value of the digital number. The binary weighted digital-to-analogue converter, in contrast to the R-2R DAC, produces an analog output voltage that is the weighted sum of the separate inputs. Because of this, the ladder network of this design necessitates a wide variety of precision resistors, rendering it both costly and unfeasible for the majority of DACs that require lower resolution levels.

Given that the binary weighted DAC is built upon a summing amplifier topology-based closed-loop inverting operational amplifier, this kind of data converter design would be suitable for a D/A converter with a few bits of resolution. However, building an R-2R digital-to-analogue converter with an R-2R resistive ladder network is a far easier method that only needs two precise resistances. The R-2R resistive ladder network uses just two resistive values. One resistor has the base value “R”, and the second resistor has twice the value of the first resistor, “2R”, no matter how many bits are used to make up the ladder network.

So for example, we could just use a standard 1kΩ resistor for the base resistor “R”, and therefore a 2kΩ resistor for “2R” (or multiples thereof as the base value of R is not too critical). Thus the resistive value of 2R will always be twice the value of the base resistor, R. That is 2R = 2*R. This means that it is much easier for us to maintain the required accuracy of the resistors along the ladder network compared to the previous weighted resistor DAC. But what is a “R-2R resistive ladder network” anyway. [7]

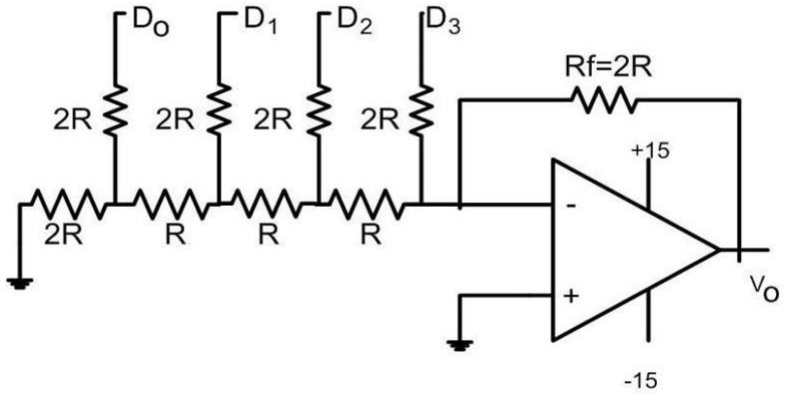


Fig: R/2R Ladder DAC[2]

Part II: Design of a flash Analog to Digital Converter

Introduction: The quickest method for converting an analog signal to a digital signal is by flash analog-to-digital converters, sometimes referred to as parallel ADCs. Although flash ADCs are often only capable of 8-bit resolution and use more power than other ADC architectures, they are perfect for applications demanding very wide bandwidth. Flash converters will be covered in this session along with comparisons to other converter types.

Methodology: Flash analog-to-digital converters, also known as parallel ADCs, are the fastest way to convert an analog signal to a digital signal. Flash ADCs are suitable for applications requiring very large bandwidths. However, these converters consume considerable power, have relatively low resolution, and can be quite expensive. This limits them to high-frequency applications that typically cannot be addressed any other way. Typical examples include data acquisition, satellite communication, radar processing, sampling oscilloscopes, and high-density disk drives. [8]

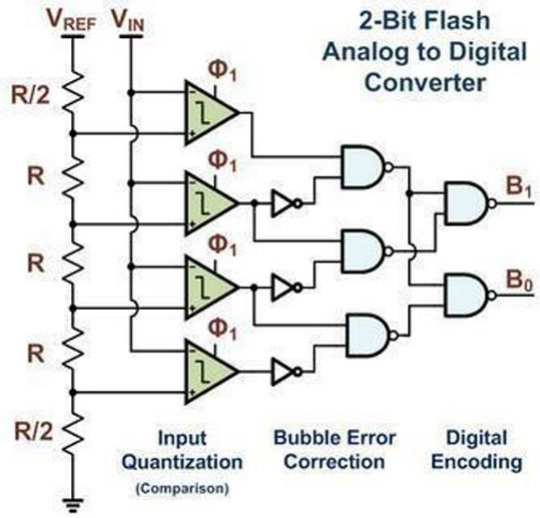


Fig: A 2-bit Flash ADC Example Implementation with Bubble Error Correction and Digital Encoding[2]

Not only is the flash converter the simplest in terms of operational theory, but it is the most efficient of the ADC technologies in terms of speed, being limited only in comparator and gate propagation delays. Unfortunately, it is the most component-intensive for any given number of output bits. This three-bit flash ADC requires seven comparators. A four-bit version would require 15 comparators. With each additional output bit, the number of required comparators doubles. An additional advantage of the flash converter, often overlooked, is the ability for it to produce a non-linear output. [9]

With equal-value resistors in the reference voltage divider network, each successive binary count represents the same amount of analog signal increase, providing a proportional response. For special applications, however, the resistor values in the divider network may be made non-equal.

This gives the ADC a custom, nonlinear response to the analog input signal. No other ADC design is able to grant this signal-conditioning behavior with just a few component value changes. [9]

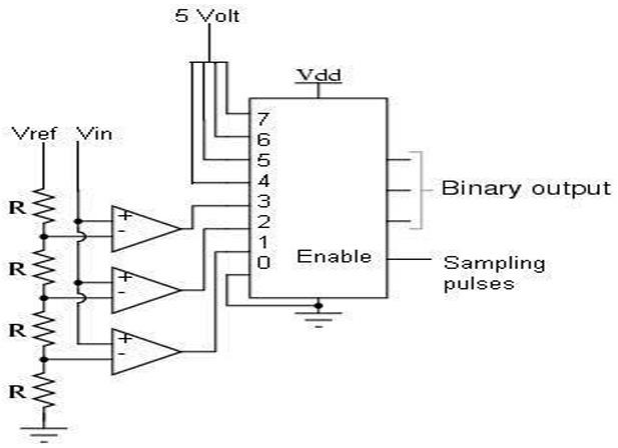


Fig: A 2 bit flash ADC[2]

V_{ref} is a stable reference voltage provided by a precision voltage regulator as part of the converter circuit, not shown in the schematic. As the analog input voltage exceeds the reference voltage at each comparator, the comparator outputs will sequentially saturate to a high state. The priority encoder generates a binary number based on the highest-order active input, ignoring all other active inputs[2].

IC Pin Configurations:

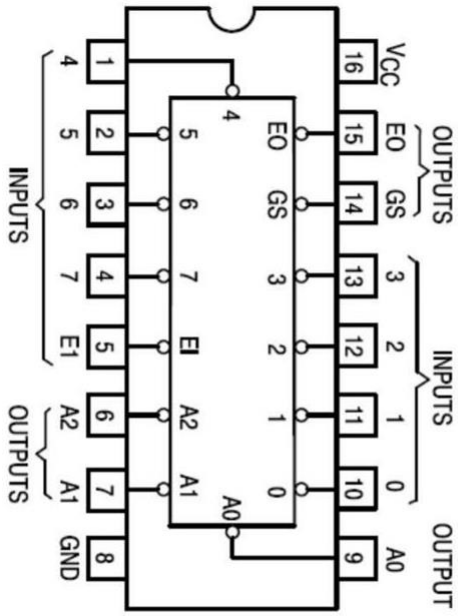


Fig: IC74148 [2]

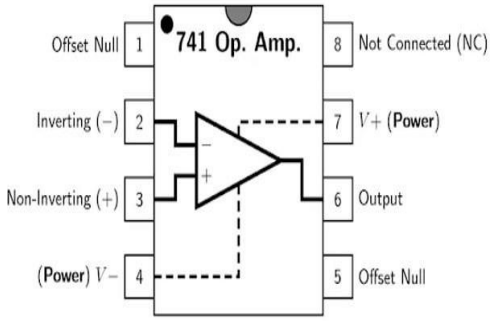
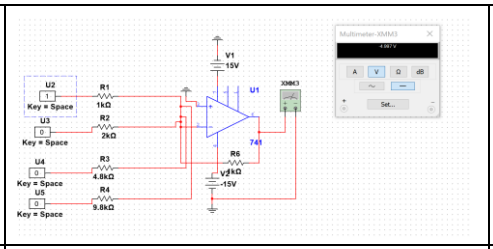
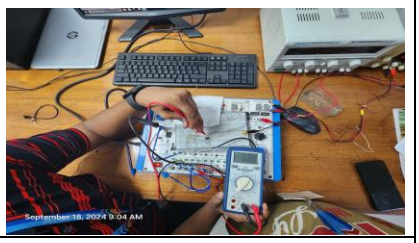
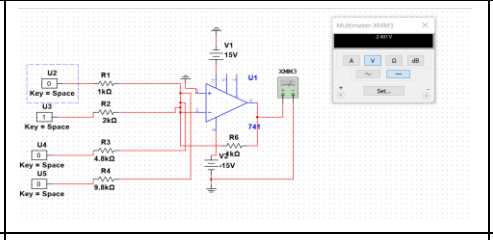
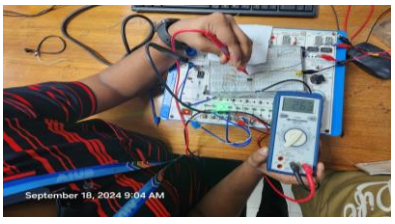
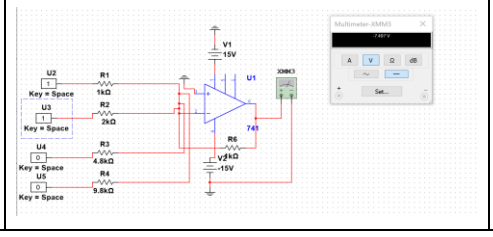
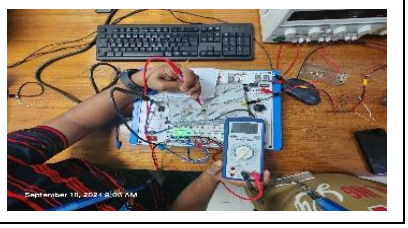


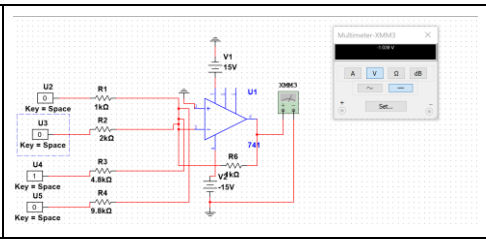
Fig: IC741 [11]

Result and Simulation:

Data table for Binary Weighted Digital to Analog Converter:

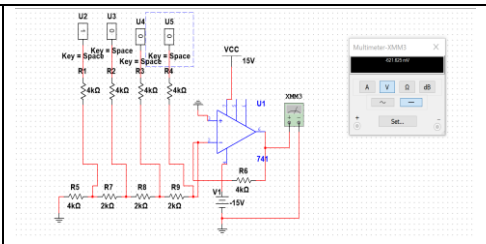
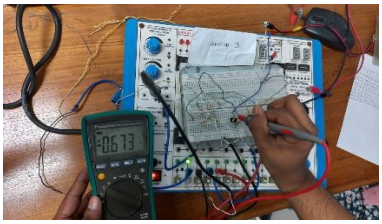
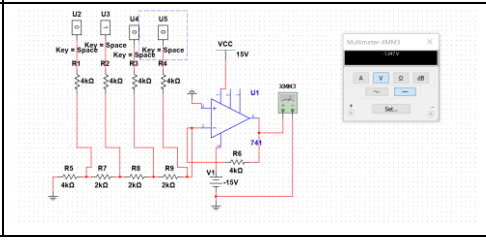
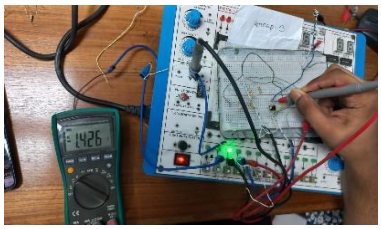
D_3	D_2	D_1	D_0	Output
0	0	0	0	0
0	0	0	1	-5.22
0	0	1	0	-2.63
0	0	1	1	-8.07
0	1	0	0	-1.19
0	1	0	1	-6.59
0	1	1	0	-3.80
0	1	1	1	-9.39
1	0	0	0	-0.58
1	0	0	1	-6.06
1	0	1	0	-3.22
1	0	1	1	-8.60
1	1	0	0	-1.77
1	1	0	1	-7.10
1	1	1	0	-7.08
1	1	1	1	-9.75

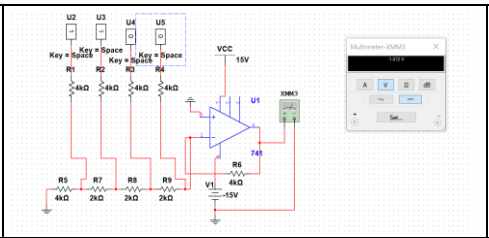
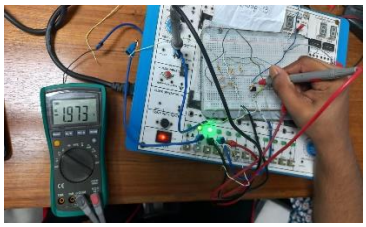
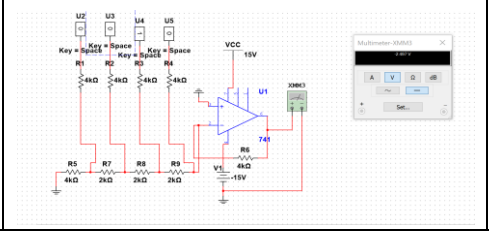
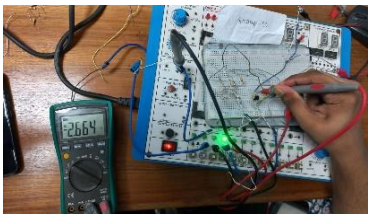
Circuit	Simulation	Actual Picture
Binary Weighted Digital to Analog Converter		
D_0=1 D_1=0 D_2=0 D_3=0		
D_0=0 D_1=1 D_2=0 D_3=0		
D_0=1 D_1=1 D_2=0 D_3=0		

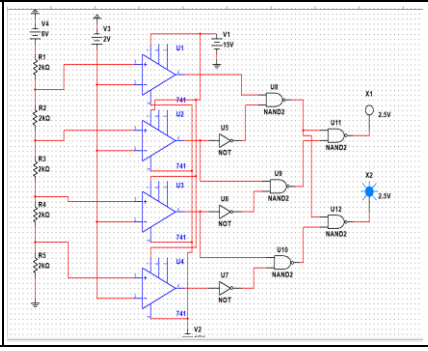
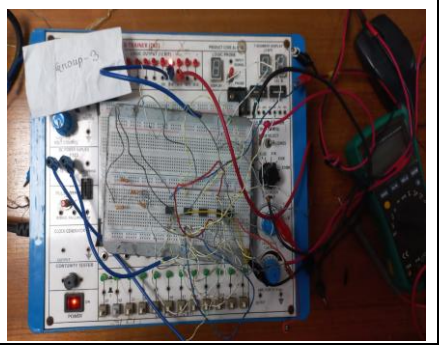
D_0=0 D_1=0 D_2=1 D_3=0		

Data table for R/2R Ladder DAC :

D_3	D_2	D_1	D_0	Output
0	0	0	0	0
0	0	0	1	-0.673
0	0	1	0	-1.428
0	0	1	1	-1.973
0	1	0	0	-2.66
0	1	0	1	-3.278
0	1	1	0	-3.90
0	1	1	1	-4.56
1	0	0	0	-5.03
1	0	0	1	-5.67
1	0	1	0	-6.43
1	0	1	1	-7.00
1	1	0	0	-7.62
1	1	0	1	-8.30
1	1	1	0	-8.94
1	1	1	1	-9.57

Circuit	Simulation	Actual Picture
Binary Weighted Digital to Analog Converter		
D_0=1 D_1=0 D_2=0 D_3=0		
D_0=0 D_1=1 D_2=0 D_3=0		

D_0=1 D_1=1 D_2=0 D_3=0		
D_0=0 D_1=0 D_2=1 D_3=0		

Circuit	Simulation	Actual Picture
A 2 bit flash ADC		

Discussion: The design of a Digital to Analog Converter (DAC) was explored in this experiment, with two specific types being investigated: the binary weighted DAC and the R/2R ladder DAC. Both designs were implemented and scrutinized in order to comprehend their distinct characteristics and efficiencies. Resistors in a binary sequence are employed by the binary weighted DAC for simplicity and easy adjustment, while a resistor network in a ladder configuration is utilized by the R/2R ladder DAC to achieve a broad range of output voltages. Insights into their respective strengths and limitations were yielded through the comparison of these designs. Another part of this experiment is implementation of a 2-bit Flash Analog-to-Digital Converter (ADC), renowned for its unparalleled speed in converting analog signals to digital, making it well-suited for high-bandwidth applications. Despite the simplicity and direct binary output, the inherent need for numerous comparators poses challenges in power consumption, size, and cost, limiting practicality beyond 8-bit precision. The discussion spanned historical implementations, technological variations, and advancements, including power-saving features, offset calibration, and digital error correction.

Conclusion: Valuable insights into Digital to Analog Converter (DAC) design challenges were revealed by the experiment. Despite its theoretical simplicity, practical issues were faced by the binary weighted DAC, highlighting the impact of inaccuracies in digital logic gates and limitations in resistor loading. Consideration of these constraints is necessitated in real-world applications. The importance of both theoretical understanding and practical constraints was acknowledged, making further experimentation vital for optimizing DAC performance. Significant contributions were made by the experiment in grasping the complexities of DAC implementation in signal processing and communication systems. Again the experiment extensively explored 2-bit flash Analog-to-Digital Converters (ADCs), highlighting their inherent speed for rapid analog-to-digital conversion in applications requiring high bandwidth. Despite this advantage, challenges such as the need for numerous comparators and precision limitations were recognized. The historical evolution from early resistor ladder designs to modern advancements like offset calibration and digital error correction reflects ongoing efforts to overcome practical constraints, contributing to a deeper comprehension of flash ADCs and their design complexities**.**

Reference:

[1] Thomas L. Floyd, *Digital Fundamentals*, 9Edition, 2006, Prentice Hall.
[2] American International University–Bangladesh (AIUB) – DLC Lab_9_student_Spring 2023-2024
[3] Electrical Technology. (2020, April 29). Digital to Analog Converter (DAC) - Types, Working & Applications. ELECTRICAL TECHNOLOGY. https://www.electricaltechnology.org/2020/04/digital-to-analog-converter-dac.html
[4] Sciencedirect.com. Retrieved September 13, 2024, from https://www.sciencedirect.com/topics/engineering/digital-to-analog-converter

[5] Saini, M. K. (n.d.). *Binary Weighted Resistor DAC*. Tutorialspoint.com. Retrieved September 13, 2024, from https://www.tutorialspoint.com/binary-weighted-resistor-dac
[6] Brainly.In. Retrieved September 13, 2024, from https://brainly.in/question/56362817#:~:text=The%20disadvantage%20of%20the%20weighted,128R%20in%20binary%20weighted%20steps.
[7] Electronics-Tutorials.Ws. Retrieved September 13, 2024, from https://www.electronics-tutorials.ws/combination/r-2r-dac.html
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