KEITHLEY

Application Note Series

Number 2239

Gate Dielectric Capacitance-Voltage Characterization Using the Model 4200 Semiconductor Characterization System

Introduction

Maintaining the quality and reliability of gate oxides is one of the most critical and challenging tasks in any semiconductor fab. With feature sizes shrinking to 0.18μm or less, gate oxides are often less than 30Å thick. For perspective, the atomic spacing between silicon atoms is 3.1Å, so that a 30Å gate oxide is less than ten atomic layers thick. Vigorous characterization and monitoring is critical for maintaining gate oxide uniformity and quality across an eight-inch or twelve-inch wafer. Further, industry projections over the next few generations of CMOS technology indicate that gate oxides will become even thinner, shrinking to approximately 15Å. This trend signals an urgent need to replace silicon dioxide with gate materials having higher dielectric constants.

Many electrical techniques have been developed over the years to characterize gate dielectric quality. In particular, various current-voltage (I-V) characterization methods have been developed, including the following:

- Time-Dependent Dielectric Breakdown (TDDB), Charge to Breakdown (QBD)
- Tunneling Current (Fowler-Nordheim or Direct Tunneling)
- Stress-Induced Leakage Current (SILC) testing

However, the most commonly used tool for studying gate-oxide quality in detail is the Capacitance-Voltage (C-V) technique. C-V test results offer a wealth of device and process information, including bulk and interface charges and many MOS-device parameters.

This application note discusses how to use the Keithley Model 4200 Semiconductor Characterization System (4200-SCS) to make C-V measurements. It also addresses basic MOS physics, proper C-V measurement techniques, and parameter extraction from C-V test results. For additional information, refer to the manual for your C-V analyzer and to the 4200-SCS Reference Manual.

Understanding MOS-Capacitor C-V Measurements

C-V measurements are typically made on a capacitor-like device, such as a MOS capacitor (MOS-C). A MOS-C is essentially composed of an oxide that is sandwiched between a semiconductor and a metal/polysilicon gate. The MOS-C can be fabricated directly on the semiconductor substrate or on a p-well or n-well. However, as will be discussed under "Understanding MOS Capacitor C-V Curves," MOS-C behavior is not as simple as this structure may suggest.

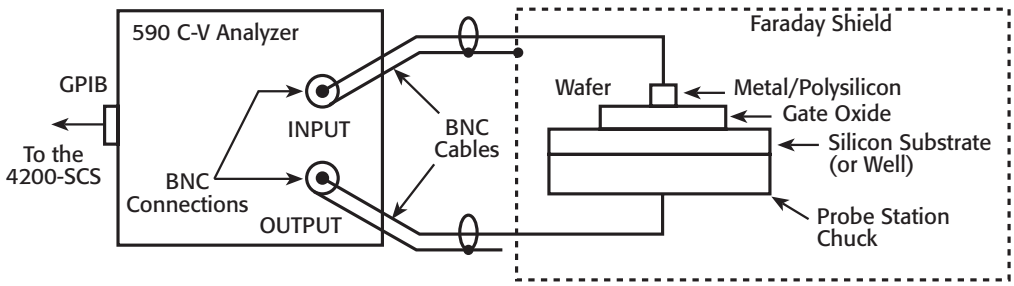
Understanding C-V Measurement Signals

If the MOS-C is fabricated directly on the substrate, the backside of the substrate is used as one of the two electrical contacts needed for a C-V test. See ***Figure 1***.

To measure MOS-C C-V curve, the MOS-C is typically connected to a C-V analyzer, such as the Keithley Model 590 or Agilent 4284A or 4980A. The C-V analyzer applies a high frequency (1MHz or 100kHz) drive signal to the backside of the substrate, via the chuck of a prober. (The prober chuck must be "floating" electrically to avoid diverting the drive signal to ground.) This high frequency AC drive signal is superimposed on a relatively slow DC bias sweep. The signal is picked up through the gate via the manipulator or probe needle.

NOTE If the polarity of the measurement is reversed—the drive signal is applied to the gate via the probe needle, and the signal is measured at the substrate—the additional capacitance of the chuck on which the substrate rests complicates interpretation of the results. Additionally, the chuck acts as an antenna, picking up RF noise from the environment.

Sometimes, as with a MOS-C on a production wafer, the substrate-to-oxide interface is replaced with a well-to-oxide interface. In such cases, a conductor is available at the top of the wafer that connects to the well. The analyzer drive signal is applied to the



Fivgure 1. MOS Instrument Connection

well through this conductor, and the signal is measured at the gate as usual.

Understanding MOS Capacitor C-V Curves

Figure 2 illustrates a high-frequency C-V curve for a p-type semiconductor substrate. A C-V curve can be divided into three regions: accumulation, depletion, and inversion. Each of the three regions is described for a p-type MOS-C.

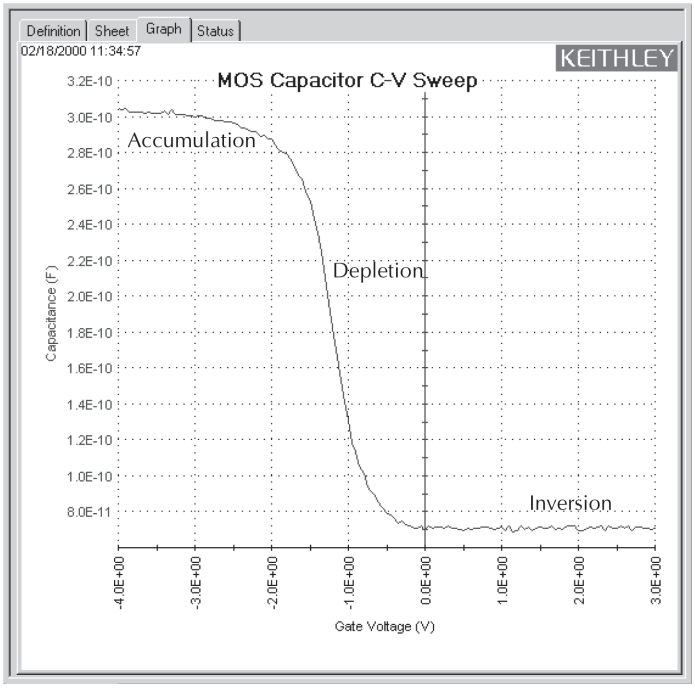


Figure 2. C-V Curve Example for P-type MOS-C

The C-V curve for an n-type MOS-C is analogous to a p-type, except that 1) the majority carriers are electrons, 2) the n-type MOS-C curve shape is essentially a mirror image of the p-type MOS-C curve shape, 3) the accumulation region occurs at positive polarities, and 4) the inversion region occurs at negative polarities.

Accumulation Region

For a p-type MOS-C, the accumulation region of the C-V curve is observed when negative voltages are applied to the gate. The negative polarity causes majority carriers (holes) to be attracted toward the gate. Because the oxide is a good insulator, these holes accumulate at the substrate-to-oxide/well-to-oxide interface.

A C-V test measures the oxide capacitance in the strong accumulation region—where, for a p-type MOS-C, the voltage is negative enough that the capacitance is essentially constant and the C-V curve slope is essentially flat. There, the oxide thickness can be extracted from the oxide capacitance. However, the C-V curve for a very thin oxide often does not "saturate" to a flat slope. In that case, the measured oxide capacitance differs from the true oxide capacitance.

Depletion Region

For a p-type MOS-C, as the gate voltage moves toward positive values, the MOS-C starts to differ from a parallel-plate capacitor. Roughly at the point where the gate voltage becomes positive, the following occurs:

- The positive gate electrostatically repels holes from the substrate-to-oxide/well-to-oxide interface.
- A carrier-depleted area forms beneath the oxide, creating an insulator. (Recall that the absence of free-moving charges distinguishes an insulator from a conductor.)

As a result, the high-frequency C-V (HF-CV) analyzer measures two capacitances in series: the oxide capacitance and the depletion capacitance. As the gate voltage becomes more positive, the following occurs:

- The depletion zone penetrates more deeply into the semiconductor.
- The depletion capacitance becomes smaller, and, consequently, the total measured capacitance becomes smaller.

Therefore, the C-V curve slope is negative in the depletion region.

Inversion Region

For a p-type MOS-C, as the gate voltage increases beyond the threshold voltage, dynamic carrier generation and recombination[1] move toward net carrier generation. The positive gate voltage both generates electron-hole pairs and attracts electrons—the minority carriers—toward the gate. Again, because the oxide is a good insulator, these minority carriers accumulate at the substrate-to-oxide/ well-to-oxide interface. The accumulated minority-carrier layer is called the *inversion layer*, because the carrier polarity is inverted. Above a certain positive gate voltage, most available minority carriers are in the inversion layer, and further gate-voltage increases do not further deplete the semiconductor. That is, the depletion region reaches a maximum depth.

However, inversion-charge generation is slower than the 1MHz or 100kHz frequency of the HF-CV (High Frequency-CV) measurement. The average time to generate an inversion charge is $\approx 10\,\tau_g N_a/n_i$, where τ_g is the generation lifetime (seconds), N_a is the doping concentration (cm^{-3}), and n_i is the intrinsic carrier concentration (cm^{-3}). For a 10^{15} cm^{-3} doping concentration and microsecond generation lifetime, electron-hole-pair (ehp) generation cannot keep up with the high frequency measurement signal. Therefore, once the depletion region reaches a maximum depth, the capacitance that is measured by the HF-CV analyzer is still based on the majority carrier position and distribution. The following applies:

- The capacitance that is measured by the HF-CV analyzer is the oxide capacitance in series with maximum depletion capacitance. This capacitance is often referred to as minimum capacitance.
- The C-V curve slope almost flat.

NOTE The measured inversion-region capacitance at the maximum depletion depth depends on the measurement frequency. Therefore, C-V curves measured at different frequencies may have different appearances. Generally, such differences are more significant at lower frequencies and less significant at higher frequencies.

Performing MOS-Capacitor C-V Measurements

Understanding Key Requirements for Successful C-V Measurements

Successful measurements require compensating for stray capacitance, recording capacitance values only at equilibrium conditions, and applying and measuring signals in an appropriate sequence. These issues are addressed in the following paragraphs to provide guidance for choosing and/or writing test routines (refer to the next subsection) and preparing for C-V tests.

Compensating for Stray Capacitance

On-wafer C-V measurements are typically performed via a prober (probe station). Signals to multipad test structures are routed between the C-V analyzer and the prober through a switch matrix and interconnecting cables. The cables and switch matrix add stray capacitance to the measurements. However, an integral Keithley Model 590 function can be used to compensate for this stray capacitance. Additionally, a Model 590 offset-cancellation function (ZERO) can be used to eliminate the small offset capacitance that is due to the cables inside the prober and probe card/manipulators. By combining cable compensation and offset correction, the system can be fully compensated from the C-V analyzer to the tip of probe needle, thus ensuring highly accurate capacitance or C-V measurements.

The compensation procedures are summarized below. For more information, refer to the Model 590 Instruction Manual and to Appendix C of the 4200-SCS Reference Manual.

Cable Compensation — The Model 590 provides three different methods to compensate for cable effects. The most common and accurate method uses calibration capacitors. Precisely known capacitance sources (for example, the Keithley Model 5909 calibration sources) are connected in place of the test fixture. These known capacitors are then measured using the Model 590. Thereafter, the nominal and measured values are then compared and cable compensation factors are derived. Four parameters are derived, based on the two-port network model. These four parameters allow compensation for even a complicated path, such as through switch matrix relays.

The 4200-SCS comes with Keithley User Library Tool (KULT) user modules that facilitate cable compensation for the Model 590. The Agilent 4284A, 4980A, and 4294A all use the "open/short" method to compensate for the cables. The drivers supplied with the Model 4200-SCS assume that the user has performed "open/short" correction from the instrument front panel.

NOTE Cable compensation needs to be performed only after a system configuration change or during a routine metrology calibration.

Offset Cancellation — *Before each measurement*, a probes-up ZERO (offset cancellation) must be performed. The main purpose of ZERO is to cancel the small residual offset capacitance due to the cables inside the prober and probe card/manipulators. After performing the probes-up ZERO, offset capacitance is subtracted from subsequent measurements. The 4200-SCS comes with KULT user modules that can be used to automate the ZERO process for the Keithley Model 590 C-V Analyzer.

Measuring at Equilibrium Conditions

The most important, but often neglected, C-V measurement requirement is to record data only under equilibrium conditions. A MOS-C takes time to become fully charged after a voltage step is applied. The fully charged condition is generally referred to as the equilibrium condition. Therefore, to allow the MOS-C to reach equilibrium, 1) after initially applying voltage to a MOS-C, allow an adequate hold time before recording the capacitance, and 2) after each step of the MOS-C voltage, allow an adequate delay time before recording the capacitance.

C-V curves swept from different directions may look different. Allowing adequate hold and delay times minimizes such differences.

NOTE One way to determine adequate hold and delay times is to generate a series of C-V curves in both directions. Change the hold and delay times for each pair of inversion → accumulation and accumulation → inversion curves until the curves look essentially the same for both sweep directions.

Hold and Delay Times When Sweeping from Inversion → Accumulation — When the C-V sweep starts in the inversion region and the starting voltage (bias) is first applied, a MOS-C is driven into deep depletion. Thereafter, if the starting voltage is maintained, the initial HF-CV capacitance climbs toward and ultimately stabilizes to C_{min} — the minimum capacitance at equilibrium (the specifics of this process depending on the device parameters, such as generation lifetime.) However, if the *hold* time is too short, the MOS-C cannot adequately recover from deep depletion, and the measured capacitance is smaller than the minimum capacitance at equilibrium.

However, once the MOS-C has reached equilibrium after applying the initial bias, an inversion → accumulation C-V curve may be swept with relatively small *delay* times. This is possible because minority carriers recombine relatively quickly as the gate voltage is reduced. Nonetheless, if the *delay* time is too short (the sweep is too fast), nonequilibrium occurs, and the capacitance in the inversion region is slightly higher than the equilibrium value. The upper dotted line in ***Figure 3*** illustrates this phenomenon.

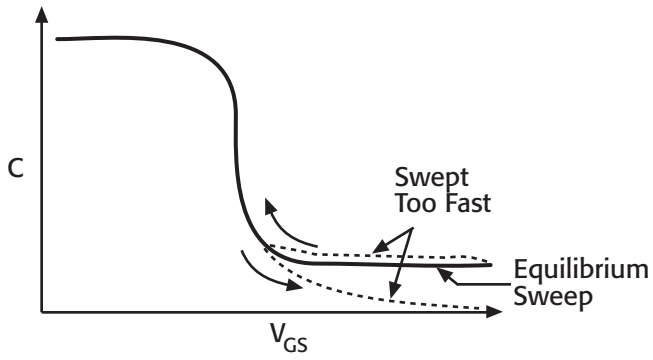


Figure 3. Effect of Sweeping a C-V Measurement Too Quickly

Hold and Delay Times When Sweeping from Accumulation → Inversion — When the C-V sweep starts in the accumulation region, the effects of hold and delay time in the accumulation and depletion regions are fairly subtle. However, in the inversion region, if the delay time is too small (the sweep is too fast), the MOS-C does not have enough time to generate minority carriers to form an inversion layer. On the HF-CV curve, the MOS-C never achieves equilibrium and eventually becomes deeply depleted. The measured capacitance values fall well below the equilibrium minimum value. The lower dotted line in ***Figure 3*** illustrates this phenomenon.

Using the Preferred Measurement Sequence

Generating a C-V measurement by sweeping the MOS-C from inversion to accumulation is faster and more controllable than sweeping from accumulation to inversion, for reasons discussed under "Measuring at Equilibrium Conditions." ***Figure 4*** illustrates the preferred measurement sequence.

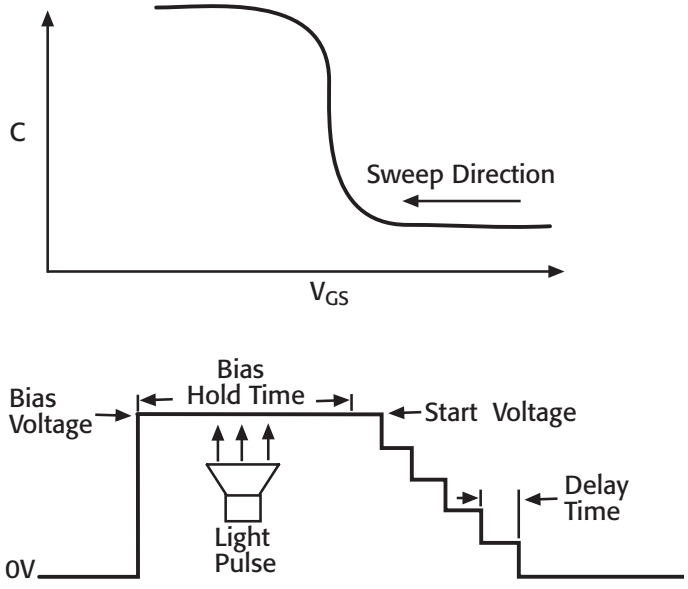


Figure 4. Preferred C-V Measurement Sequence

The device is first biased for the *hold* time. The bias voltage should be the same as the sweep start voltage to avoid a sudden voltage change when the sweep starts.

During biasing, if necessary, a short light pulse can be applied to the sample to help generate minority carriers. However, before the sweep starts and before any data is recorded, all lights should be turned off. All measurements should be performed in total darkness, because silicon can be very light-sensitive.

During the sweep, the *delay*-time parameter should be chosen to optimally balance measurement speed and measurement integrity, which requires adequate equilibration time.

Measuring C-V Curves with the Keithley 4200-SCS

The Keithley 4200-SCS has built-in support for the control of external C-V analyzers. It supports the Keithley 590 C-V Analyzer and the Agilent 4284A, 4294A, and 4980A Precision LCR meters, controlling them via Keithley User Library Tool (KULT) user modules through Keithley Interactive Test Environment (KITE) User Test Modules (UTMs).

Configuring the 4200-SCS for C-V Measurement

Before using a C-V analyzer with the 4200-SCS, system software parameters must be configured to properly recognize the analyzer. For example, to add a Keithley Model 590 to the system, first start KCON (Keithley Configuration Utility). From the pull-down menu under **Tools → Add External Instrument**, select **Add Capacitance Meter/Keithley 590 CV Analyzer**. Next, in the window that appears, set the 590's GPIB address in the **Instrument Properties** area. After validating the system, save the configuration. (Use an analogous procedure to add an Agilent 4284A, 4294A, or 4980A.) For more details, refer to Section 7 of the 4200-SCS Reference Manual, "Keithley Configuration Utility (KCON)."

Choosing/Writing C-V User Modules

Before performing C-V measurements, you must choose and/or write KULT *user modules* to control external C-V analyzers such as the Keithley 590 or the HP 4284A. User modules are written in the C programming language and are compiled and linked using KULT. User modules are then executed in projects by connecting them to KITE UTMs.

Keithley provides several user modules for the most common C-V measurements, including C-V sweep, pulsed C-V, C-t sweep (sampling), and Cmeas (single point) measurements. Supplied user modules are also available for cable compensation. If you need additional C-V user modules, you can write them using KULT. For details about writing user modules and building user libraries, refer to Section 8 of the 4200-SCS Reference Manual, "Keithley User Library Tool (KULT)."

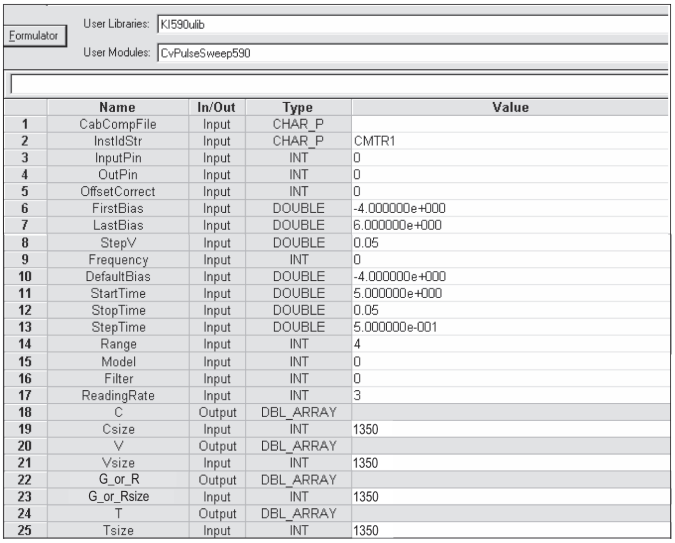
NOTE When selecting and writing C-V user modules, be sure to address the requirements discussed under "Understanding Key Requirements for Successful C-V Measurements."

Adding C-V Tests to a 4200-SCS Project

After choosing/writing a C-V user module(s), build a KITE test project and create a User Test Module (UTM) for each user module. UTMs can be mixed with Interactive Test Modules (ITM) to perform a sequence of C-V and I-V tests. For example, a tunneling-current I-V measurement can be done first on a MOS-C, followed by a C-V measurement on the same device, and followed thereafter by a breakdown voltage test. With the help of switch-matrix UTM(s) and a switch matrix, such as a Keithley 707A matrix equipped with ultra-low-current 7174A switch cards, these tests can be done automatically in sequence.

For example, to create a Model 590 CV sweep UTM, do the following: 1) add an unconfigured UTM to the project, 2) in the KITE Project Navigator, double-click the UTM, 3) in the UTM **Definition** tab that appears, select the **KI590ulib** User Library and **Cvsweep 590** User Module, and 4) type in the measurement parameters such as **FirstBias**, **LastBias**, **StepV**, **StepTime**, etc. to configure the test. See ***Figure 5***.

Save the project before continuing.



Formulator — User Libraries: KI590ulib — User Modules: CvPulseSweep590

	Name	In/Out	Type	Value
1	CabCompFile	Input	CHAR_P	
2	InstIdStr	Input	CHAR_P	CMTR1
3	InputPin	Input	INT	0
4	OutPin	Input	INT	0
5	OffsetCorrect	Input	INT	0
6	FirstBias	Input	DOUBLE	-4.000000e+000
7	LastBias	Input	DOUBLE	6.000000e+000
8	StepV	Input	DOUBLE	0.05
9	Frequency	Input	INT	0
10	DefaultBias	Input	DOUBLE	-4.000000e+000
11	StartTime	Input	DOUBLE	5.000000e+000
12	StopTime	Input	DOUBLE	0.05
13	StepTime	Input	DOUBLE	5.000000e-001
14	Range	Input	INT	4
15	Model	Input	INT	0
16	Filter	Input	INT	0
17	ReadingRate	Input	INT	3
18	C	Output	DBL_ARRAY	
19	Csize	Input	INT	1350
20	V	Output	DBL_ARRAY	
21	Vsize	Input	INT	1350
22	G_or_R	Output	DBL_ARRAY	
23	G_or_Rsize	Input	INT	1350
24	T	Output	DBL_ARRAY	
25	Tsize	Input	INT	1350

Figure 5. Example UTM Definition Tab

Connecting the C-V Analyzer

Connect a Keithley Model 590 C-V analyzer as shown in ***Figure 1***. Connect an HP 4284A LCR meter as described in Appendix D of the Reference Manual.

Running a C-V Test

Before running a C-V test, ensure that you have performed a probes-up ZERO (offset cancellation) for stray capacitance, as described under "Compensating for Stray Capacitance." Then, run the C-V test by executing a UTM alone or by executing a project, subsite plan, or device plan containing C-V test UTM(s). For more details, refer to "Executing projects and individual subsite plans, device plans, and tests" in Section 6 of the 4200-SCS Reference Manual.

Compensating C-V Measurements for Series Resistance

After generating a C-V curve, you may need to compensate the measurements for series resistance. The series resistance (R_{SERIES}) can come from either the substrate (well) or the backside of the wafer. For wafers typically produced in fabs, the substrate bulk resistance is fairly small (<10Ω) and has negligible impact on C-V measurements. However, if the backside of the wafer is used as an electrical contact, the series resistance due to oxides can significantly distort a measured C-V curve. This extra series resistance particularly affects HF-CV curves, because the high-frequency capacitance calculations are based on amplitude change and phase shift. The extra series resistance cannot be reduced to a simple two-element (series or parallel) model that the HF-CV analyzer can use to calculate capacitance and conductance. However, you can compensate for this series resistance via post-test calculations using the formulas below (Nicollian and Brews p. 224) which are based on the simplified three-element model.

$$C_C = \frac{\left(G_M^2 + \omega^2 C_M^2\right) C_M}{a^2 + \omega^2 C_M^2} \qquad (1)$$

$$G_C = \frac{\left(G_M^2 + \omega^2 C_M^2\right) a}{a^2 + \omega^2 C_M^2} \qquad (2)$$

In these equations, C_M is the measured capacitance, C_C is the corrected capacitance, G_M is the measured conductance, G_C is the corrected conductance, $a = GM - (G^2M + \omega^2C^2M)R_{SERIES}$, R_{SERIES} is the series resistance, and ω is the angular frequency (radians sec^{-1}).

R_{SERIES} may be calculated from the capacitance and conductance values that are measured while biasing the DUT (device under test) to the accumulation region. Use the following equation:

$$R_{SERIES} = \frac{\left(\frac{G_M}{\omega C_M}\right)^2}{\left[1 + \left(\frac{G_M}{\omega C_M}\right)^2\right] G_M} \qquad (3)$$

NOTE Equations (1), (2), and (3) require that the C-V analyzer reports results using the parallel model.

Using the KITE Formulator, compensated capacitances and conductances can be automatically calculated via the above formulas at the end of the C-V test and then be automatically entered into the **Data** worksheet for the test. For more information, refer to "Analyzing test data using the Formulator" in Section 6 of the 4200-SCS Reference Manual.

NOTE Although you can correct for oxide series resistance, Keithley strongly recommends that you minimize this resistance by thoroughly cleaning the wafer backside before using it as a contact.

Extracting MOS Device Parameters from C-V Measurements

The real importance of C-V measurement techniques is that a large number of device parameters can be extracted from two seemingly simple curves: the high frequency C-V curve that is described in this note and the quasistatic C-V curve. These parameters can provide critical device and process information. We can divide the parameters roughly into three groups. The first group includes typical MOS device parameters such as flatband voltage, threshold voltage, etc. The next group, oxide charge parameters, includes interface trap charge density, mobile ion charge density, etc. The third group consists of doping-related parameters. Also, using C-t data, carrier generation lifetime and recombination lifetime can be extracted.

This application note addresses the following parameters that can be extracted from a high-frequency C-V (HF-CV) curve:

- Oxide thickness
- Flatband capacitance and flatband voltage
- Threshold voltage
- Effective and total bulk oxide charge

Using the KITE Formulator, parameters can be automatically calculated from test data at the end of the C-V test, and then be automatically entered into the **Data** worksheet for the test. For more information, refer to "Analyzing test data using the Formulator" in Section 6 of the 4200-SCS Reference Manual.

Extracting the Oxide Thickness

For a relatively thick oxide (>50Å), extracting the oxide thickness is fairly simple. The oxide capacitance (C_{OX}) is the high-frequency capacitance when the device is biased for strong accumulation. In the strong accumulation region, the MOS-C acts like a parallel-plate capacitor, and the oxide thickness may be calculated from C_{OX} and the gate area using the following equation:

$$t_{OX} = \frac{A \in_{OX}}{(1\times 10^{-19})\, C_{OX}} \qquad (4)$$

where t_{OX} is the oxide thickness (nm), A is the gate area (cm^2), $\in_{OX}$ is the permittivity of the oxide material (F/cm), and C_{OX} is the oxide capacitance (pF).

Oxide thickness calculations based on C-V measurements can be very precise, unless improperly extracted. Oxide thickness *must be extracted from the strong accumulation region*, where the capacitance measured truly reflects the oxide capacitance. If possible, ASTM procedures should be followed.

Extracting the Flatband Capacitance and Flatband Voltage

Application of a certain gate voltage, the *flatband voltage* (V_{FB}) results in the disappearance of band bending. At this point, known as the *flatband condition*, the semiconductor band is said to become *flat*. Because the band is flat, the surface potential is zero (with the reference potential being taken as the bulk potential deep in the semiconductor). Flatband voltage and its shift are widely used to extract other device parameters, such as oxide charges.

We can identify V_{FB} from the C-V curve. One way is to use the *flatband capacitance method*. In this method, the ideal value of the flatband capacitance (C_{FB}) is calculated using equations *(5)* and *(6)*. Once the value of C_{FB} is known, the value of V_{FB} can be obtained from the C-V curve data, by interpolating between the closest gate-to-substrate (V_{GS}) values (from Nicollian and Brews pp. 487–488).

Equation *(6)* calculates the *Debye length* parameter (λ) that is used in equation *(5)*. Based on the doping profile, the calculation of λ requires one of the following doping concentrations: N at 90% of W_{MAX} (refer to Nicollian and Brews), a user-supplied N_A (bulk doping concentration for a p-type, acceptor, material), or a user-supplied N_D (bulk doping concentration for an n-type, donor, material).

NOTE The flatband capacitance method is invalid when the interface trap density (D_{IT}) becomes very large (10^{12} – 10^{13} or greater). However, the method should give satisfactory results for most users. Those dealing with high D_{IT} values should consult the appropriate literature for a more suitable method.

Use equations *(5)* and *(6)* to calculate the flatband capacitance:

$$C_{FB} = \frac{C_{OX} \in_S A/(1\times 10^{-4})(\lambda)}{(1\times 10^{-12})(C_{OX}) + \in_S A/(1\times 10^{-4})(\lambda)} \qquad (5)$$

where C_{FB} is the flatband capacitance (pF), C_{OX} is the oxide capacitance (pF), $\in_S$ is the permittivity of the substrate material (F/cm), A is the gate area (cm^2), and λ is the extrinsic Debye length, as calculated:

$$\lambda_D = \left(\frac{\in_S kT}{q^2 N_X}\right)^{1/2} \qquad (6)$$

where kT is the thermal energy at room temperature (4.046×10^{-21} J), q is the electron charge (1.60219×10^{-19} coul), and $N_X = N$ at 90% W_{MAX} (refer to Nicollian and Brews) or, when input by the user, $N_X = N_A$ or $N_X = N_D$.

The extrinsic Debye length is an idea borrowed from plasma physics. In semiconductors, majority carriers can move freely. The motion is similar to a plasma. Any electrical interaction has a limited range. The Debye length is used to represent this inter-

action range. Essentially, the Debye length indicates how far an electrical event can be sensed within a semiconductor.

Extracting the Threshold Voltage

The turn-on region for a MOSFET corresponds to the inversion region on its C-V plot. When a MOSFET is turned on, the channel formed corresponds to strong generation of inversion charges. It is these inversion charges that conduct current. When a source and drain are added to a MOS-C to form a MOSFET, a p-type MOS-C becomes an n-type MOSFET—a so-called n-channel MOSFET. Conversely, an n-type MOS-C becomes a p-channel MOSFET.

The threshold voltage (V_{TH}) is the point on the C-V curve where the surface potential (ϕ_S) equals twice the bulk potential (ϕ_B). This curve point corresponds to the onset of strong inversion. For an enhancement-mode MOSFET, V_{TH} corresponds to the point where the device begins to conduct. The physical meaning of the threshold voltage is the same for both a MOS-C C-V curve and a MOSFET I-V curve. However, in practice, the numeric V_{TH} value for a MOSFET may be slightly different, due to the particular method used to extract the threshold voltage.

Calculate V_{TH} from a C-V curve as follows:

$$V_{TH} = \left[\pm \frac{A}{C_{OX}} \sqrt{4 \in_S q \left| N_{BULK} \right| \left| \phi_B \right|} + 2 \left| \phi_B \right| \right] + V_{FB} \quad (7)$$

where V_{TH} is the threshold voltage (V), A is the gate area (cm^2), C_{OX} is the oxide capacitance (pF), $\in_S$ is the permittivity of the substrate material (F/cm), q is the electron charge (1.60219×10^{-19} coul), N_{BULK} is the bulk doping (cm^{-3}), ϕ_B is the bulk potential (V), and V_{FB} is the flatband potential.

Calculating the Metal-Semiconductor Work Function Difference

The metal-semiconductor work function difference (W_{MS}) is commonly referred to as simply the work function. It contributes to the shift in V_{FB} from the ideal zero value, along with the effective oxide charge (Nicollian and Brews, pp. 462–477; Sze, pp. 395–402). The work function represents the difference in work necessary to remove an electron from the gate and from the substrate.

W_{MS} is needed in the next subsection, "Extracting Effective and Total Bulk Oxide Charge." Therefore, it is derived here as follows:

$$W_{MS} = W_M - \left[W_S + \frac{E_G}{2} - \phi_B \right] \quad (8)$$

where W_M is the metal work function (V), W_S is the substrate material work function (electron affinity) (V), E_G is the substrate material bandgap (V), and ϕ_B is the bulk potential (V).

For silicon, silicon dioxide, and aluminum:

$$W_{MS} = 4.1 - \left[4.15 + \frac{1.12}{2} - \phi_B \right] \quad (9)$$

Therefore,

$$W_{MS} = -0.61 + \phi_B \quad (10)$$

and

$$W_{MS} = -0.61 - \left(\frac{kT}{q} \right) ln \left(\frac{N_{BULK}}{n_I} \right) (DopeType) \quad (11)$$

where k is the Boltzmann constant (1.38066×10^{-23} J/°K), T is the test temperature (°K), q is the electron charge (1.60219×10^{-19} coul), N_{BULK} is the bulk doping (cm^{-3}), n_I is the intrinsic carrier concentration (1.45×10^{10} cm^{-3}), and *DopeType* is +1 for p-type materials and –1 for n-type materials.

For example, for an MOS capacitor with an aluminum gate and p-type silicon ($N_{BULK} = 10^{16}$ cm^{-3}), $W_{MS} = -0.95$V. Also, for the same gate and n-type silicon ($N_{BULK} = 10^{16}$ cm^{-3}), $W_{MS} = -0.27$V.

The supply voltage of modern CMOS devices is decreasing. Also, aluminum reacts with silicon dioxide. Therefore, the present practice is to use heavily doped polysilicon as the gate material. The goal is to achieve a minimal work-function difference between the gate and the semiconductor, while maintaining the conductive properties of the gate.

Extracting Effective and Total Bulk Oxide Charge

The effective oxide charge (Q_{EFF}) represents the sum of the oxide fixed charge (Q_F), the mobile charge (Q_M), and the oxide trapped charge (Q_{OT}).

NOTE Q_{EFF} is distinguished from the interface trapped charge (Q_{IT}) in that Q_{IT} varies with gate bias, whereas $Q_{EFF} = Q_F + Q_M + Q_{OT}$ does not (Nicollian and Brews pp. 424–429; Sze, pp. 390–395).

Simple room temperature C-V measurements do not distinguish the three components of Q_{EFF}. These three components can be distinguished from each other by temperature cycling (Nicollian and Brews, p. 429, Figure 10.2). Also, since the charge profile in the oxide is not known, Q_{EFF} should be used as only a relative, not absolute, measure of charge. The calculation of Q_{EFF} is based on the assumption that the charge is located in a sheet at the silicon-to-silicon dioxide interface.

From Nicollian and Brews, Eq. 10.10, we have:

$$V_{FB} - W_{MS} = -\frac{Q_{EFF}}{C_{OX}} \quad (12)$$

where V_{FB} is the flatband voltage (V), W_{MS} is the metal-semiconductor work function, and C_{OX} is the oxide capacitance.

For example, assume a 0.01cm², 50pF, p-type MOS-C with a flatband voltage of –5.95V; its N_{BULK} of 10^{16} cm^{-3} corresponds to a W_{MS} of –0.95V. For this example, Q_{EFF} calculates to be 2.5×10^{-8} coul/cm², which in turn causes the threshold voltage to shift ≈ 5V in the negative direction. Note that in most cases where the bulk charges are positive, there is a shift toward negative gate voltages. The effective oxide charge concentration (N_{EFF}) is computed from effective oxide charge (Q_{EFF}) and the electron charge as follows:

$$N_{EFF} = \frac{Q_{EFF}}{q} \qquad (13)$$

For this example, the effective oxide charge concentration (N_{EFF}) is 1.56×10^{11} units/cm³.

Because fixed and trapped charges are typically further away from the oxide-semiconductor interface, they do not interact with the semiconductor. As long as the total number of these charges is not too large, the only effect is the shift of flatband and threshold voltage. Therefore, they are not a cause for concern, unless they are related to reliability, radiation effects, etc.

Conclusions

The C-V characteristics of MOS capacitors contain a wealth of information about the semiconductor characteristics, which extend to MOSFETs. The powerful and user-friendly features of the Keithley Model 4200-SCS, when teamed with a C-V analyzer, such as the Keithley Model 590 or Agilent 4284A, 4294A, or 4980A, can simplify and automate both the sweeping of C-V curves and the extraction of the semiconductor characteristics.

References

Nicollian, E.H. and Brews, J.R., MOS Physics and Technology, Wiley, New York (1982).

Sze, S.M., Physics of Semiconductor Devices, 2nd edition. Wiley, New York (1985).

1. Although the average net concentration of carriers in a semiconductor is stable at equilibrium, carrier generation and recombination occur dynamically.

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Printed in the U.S.A. No. 2239 Rev. 04062KGW