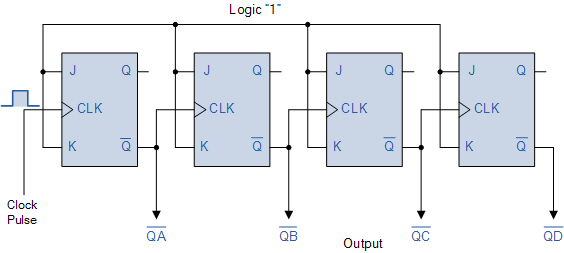
**EXPERIMENT -7**

**AIM:** WRITE VHDL CODE FOR 4 BIT UP/DOWN COUNTER AND SIMULATE IT USING

MODELSIM.

**THEORY:** Both Synchronous and Asynchronous counters are capable of counting “Up” or counting “Down”, but there is another more “Universal” type of counter that can count in both directions either Up or Down depending on the state of their input control pin and these are known as **Bidirectional Counters**.

Bidirectional counters, also known as Up/Down counters, are capable of counting in either direction through any given count sequence and they can be reversed at any point within their count sequence by using an additional control input.



**VHDL CODE:**

LIBRARY ieee;

USE ieee.std\_logic\_1164.all;

USE ieee.std\_logic\_arith.all;

USE ieee.std\_logic\_unsigned.all;

ENTITY BIT4\_UPDOWN\_COUNTER IS

port(CLOCK,up\_down: in std\_logic; Q:out std\_logic\_vector(3 downto 0));

END ENTITY BIT4\_UPDOWN\_COUNTER;

--

ARCHITECTURE BIT4\_UPDOWN\_COUNTER\_BEHAV OF BIT4\_UPDOWN\_COUNTER IS

SIGNAL tmp: std\_logic\_vector(3 downto 0):="0000";

BEGIN

process (CLOCK)

begin

if (rising\_edge(CLOCK)) then

if (up\_down='1') then

tmp <= tmp + "1";

else

tmp <= tmp - "1";

end if;

Q <= tmp;

end if;

end process;

END ARCHITECTURE BIT4\_UPDOWN\_COUNTER\_BEHAV;

**RESULT:**

